PRELIMINARY
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AR8113 10/100 Mbps Fast Ethernet LAN Controller with Integrated Transceiver

General Description

The AR8113 is the second generation 10/100 Mbps Ethernet controller solution from Atheros. It is a high performance, low cost, fully integrated 10/100 Mbps Ethernet controller targeting PC and embedded applications. The AR8113 combines a 10/100BASE-T Ethernet media access controller (MAC), a double-speed Ethernet physical layer transceiver (PHY), a PCI Express bus interface, and embedded buffer memory in a single device. The AR8113 is compliant with the IEEE 802.3u specification for 10/100 Mbps Ethernet. The AR8113 device combines pulse shaping, Tx/Rx PCS, equalizer, decoder, and timing recovery functions to deliver robust signal performance in noisy environments.

The AR8113 10/100 Mbps controller supports checksum offload features for IP, TCP, and UDP, lowering CPU utilization and optimizing network performance. The AR8113 device supports advanced power management functions, and Wake-On-LAN (WOL).

MAC Features

- IEEE 802.3x compliant flow control support
- Interrupt coalescing
- Internal transmit and receive FIFO buffers
- Descriptor ring management for Tx

Device and Technology Features

- Single power supply required: 3.3 V
- Supports 25 MHz external clock source
- Loop back modes for diagnostics
- TWSI
- Programmable LED functionality
- 48-pin QFN (6mm x 6mm) package

PHY Features

- Integrated PHY for 10/100 Mbps
- IEEE 802.3ab Auto-Negotiation support
- IEEE 802.3ab PHY compliance and compatibility
- Advanced DSP architecture
- Cable Diagnostic Test (CDT)
- Implements Atheros Super-Low Power power saving mode

Host Offloading Features

- IPv4, IPv6, TCP, and UDP checksum offload capabilities
- Transmit TCP segmentation
- Supports receive-side scaling (RSS)
- Advanced packet filtering, including promiscuous (unicast and multicast) transfer mode support and multicast frame
- IEEE 802.1q VLAN support

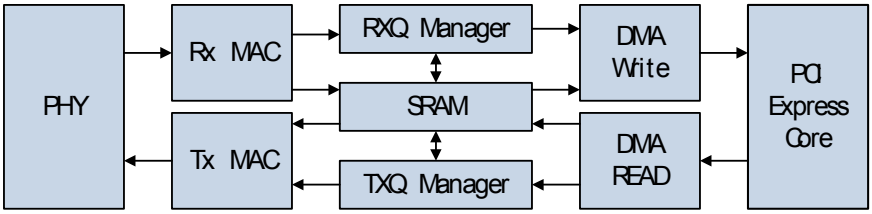
Power Management Features

- Supported PM states: L1
- Support wake event generation from all PM states including D3hot
- Compliance with PCI Express power management and ACPI
- Wake on LAN support
- Supports de-assertion of clock request signal for further reduction in power requirement

PCIE Features

- PCI Express base 1.0a compliant
- Interrupt messaging
- PCIE baseline and advanced error reporting
- Supports SM Bus initialization
- Supports PME and error messaging
- Supports MSI and MSI-X
- Supports up to 25% over-clocking

AR8113 Functional Block Diagram



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1. Pin Descriptions

This section contains a package pinout for the AR8113 QFN 48 pin and a listing of the signal descriptions (see Figure 1-1).

The following nomenclature is used for signal names:

NC	No connection is made between this pin and the internal die
NO CONN	This pin is reserved for testing, no PC trace should lead to this pin
n	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types described in Table 1-1:

D	Open drain
IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal
PD	Internal pull-down for input
PU	Internal pull-up for input

Figure 1-1 shows the pinout diagram for the AR8113.

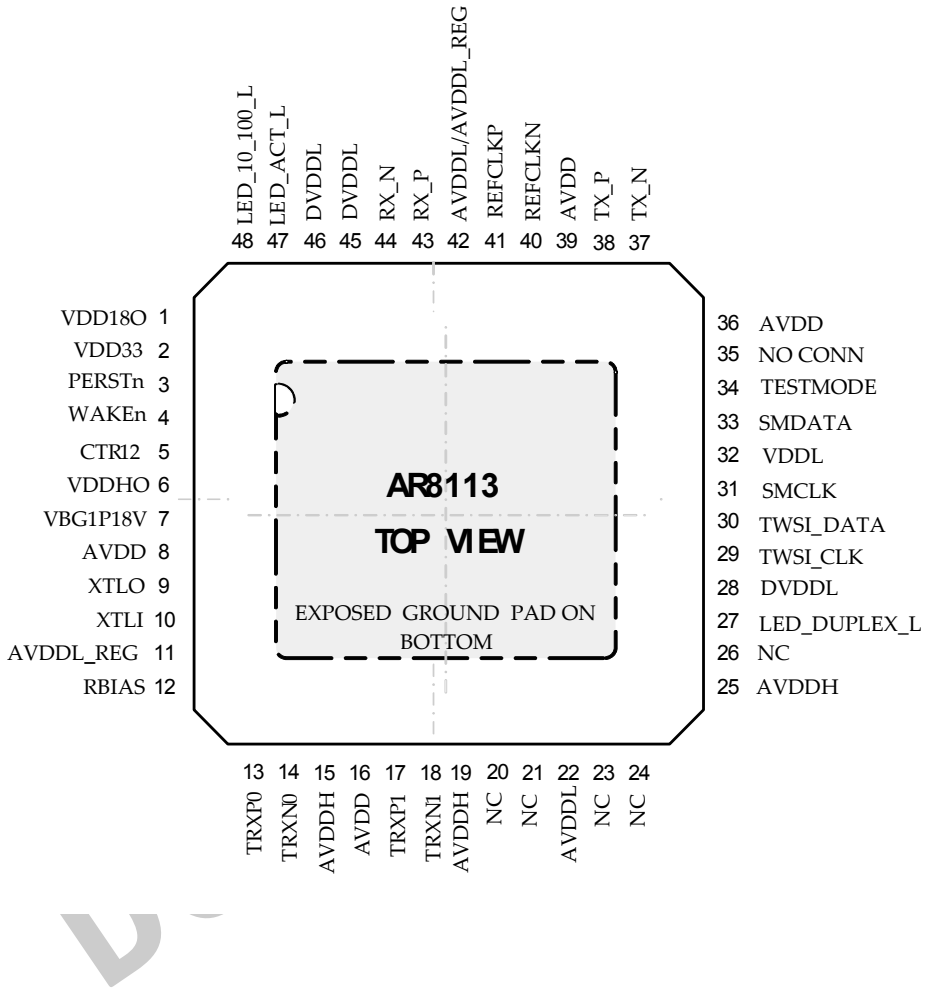

Figure 1-1. **Pinout Diagram (Top View)**

NOTE: An exposed ground pad exists on the back side of the package.

NOTE: Pin 35 is reserved for testing; no PC trace should lead to this pin.

Table 1-1. **Signal to Pin Relationships and Descriptions**

Symbol	Pin	Type	Description
EEPROM			
TWSI_CLK	29	I/O, D, PU	TWSI bus clock line to serial EEPROM
TWSI_DATA	30	I/O, D, PU	TWSI bus data line to serial EEPROM
LED			
LED_DUPLEXn	27	I/O, PU	Parallel LED output for full-duplex/collision indicator; Lit when a valid full-duplex link is present — blinking when a collision is detected; active low
LED_ACTn	47	I/O, PU	Parallel LED output activity indicator; blinking when data is being transmitted or received; active high
LED_10_100n	48	I/O, PU	Parallel LED output for 10/100 BASE-T; active low
			0 — 100 BASE-TX
			1 — 10 BASE-T
PCIE/Media Interface			
REFCLKN	40	IA	PCIE reference clock negative line (100 MHz differential low-voltage interface), AC coupled with 0.1 uF cap, or DC coupled if input common-mode voltage is below 0.5 V.
REFCLKP	41	IA	PCIE reference clock positive line (100 MHz differential low-voltage interface), AC coupled with 0.1 uF cap, or DC coupled if input common-mode voltage is below 0.5 V.
RX_N	44	IA	PCIE 2.5 Gbps data negative input; low swing, high speed
RX_P	43	IA	PCIE 2.5 Gbps data positive input; low swing, high speed
TX_N	37	OA	PCIE 2.5 Gbps data negative output; low swing, high speed
TX_P	38	OA	PCIE 2.5 Gbps data positive output; low swing, high speed
TRXN0	14	IA/OA	Media dependent interface 0 Terminated with two 49.9 Ω resistors and connect to XFMR
TRXP0	13		
TRXN1	18	IA/OA	Media dependent interface 1 Terminated with two 49.9 Ω resistors and connect to XFMR
TRXP1	17		
WAKEn	4	I/O, PU	PCIE wake signal
System Management Bus			
SMCLK	31	I, PU	System management bus clock line
SMDATA	33	I/O, D, PU	System management bus data line

Table 1-1. **Signal to Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
System Signal Group/Reference			
RBIAS	12	OA	Connect 2.37 K 1% to GND to set bias current
PERSTn	3	IH	System reset, active low, connect 5.1 K to 3.3V and 0.1 uF to GND, or to external system reset with at least 400 ns low duration.
XTLI	10	IA	Crystal oscillator input; 27 pF to GND An external 25 MHz clock source with swing from 0 to 1.5V can inject from this pin in application with the two 27 pF caps removed.
XTLO	9	OA	Crystal oscillator output; 27 pF to GND An external clock source with 0-1.5 V swing can inject to this pin in application with the 27 pF cap removed and the 27 pF cap at XTLI maintained.
VBG1P18V	7	OA	Reference voltage; 1 nF to GND
Test			
TESTMODE	34	I, PD	Test mode control; tie to GND
NO CONN	35		This pin is reserved for testing, no PC trace should lead to this pin

Symbol	Pin	Description
Power		
CRT12	5	Connect to base of the PNP to form the 1.2V linear regulator.
AVDDL	8, 16, 22, 36, 39	1.2 V analog power. Connect pin 8 to collector of the PNP to form the 1.2V linear regulator. See the *AR8113 Design Guide* for more information.
AVDDL_REG	11	1.2 V regulator output for supply at pin 42. 0.22 uF to GND to stabilize.
AVDDL/ AVDDL_REG	42	Connect to Analog 1.2 V with a ferrite bead and a 0.1 uF capacitor to GND.
DVDDL	28, 32, 45, 46	1.2 V digital power.
VDD18O	1	1.8 V regulator output. Connect to XFMR center taps.
AVDDH	15, 19, 25	2.5 V analog power. Connect to pin 6 “VDDHO”.
VDDHO	6	2.5 V regulator output
VDD33	2	3.3 V power supply
—	—	Exposed ground pad on the back side of the chip. Tie to ground.

2. Functional Description

The AR8113 is a high-performance, fully integrated Ethernet LOM/NIC controller that provides physical layer functions for half/full - duplex 10 BASE-T and 100 BASE-TX Ethernet to transmit and receive high-speed data over standard category 5 (CAT5) unshielded twisted pair cable.

The AR8113 10/100 PHY is 802.3ab compliant and combines feed-forward equalizer, feedback equalizer, and timing recovery to enhance signal performance in noisy environments. The AR8113 uses PCI Express to efficiently collaborate with on chip scatter/gather logic to uni-directionally move data between system and memory at 2.5 Gbps. The AR8113 implements IPv6, IPv4, TCP and UDP checksum generation and validation and employs a flexible scheme to effectively coalesce host system interrupts.

See the "AR8113 Functional Block Diagram" on page 1.

2.1 Transmit Functions

Table 2-1 describes Tx function encoder modes.

Table 2-1. **Tx Function Decoder Modes**

Mode	Description
100 BASE-TX	MII 4-bit data is 4B/5B serialized, scrambled, and encoded to a 3-level MLT3 sequence transmitted by the PMA.
10 BASE-T	The AR8113 transmits and receives Manchester-encoded data.

2.2 Receive Functions

2.2.1 Decoder Modes

Table 2-2 describes Rx function decoder modes.

Table 2-2. **Rx Function Decoder Modes**

Mode	Description
100 BASE-TX	In 100 BASE-TX mode, the Rx data stream is recovered and descrambled to align to symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to the MII Rx data pins after data stream delimiters have been translated.
10 BASE-T	In 10 BASE-T mode, the recovered 10 BASE-T signal is decoded from Manchester then aligned.

2.2.2 Analog-to-Digital Converter

The AR8113 device employs an advanced high speed ADC on each Rx channel with high resolution, which results in better SNR and lower error rates.

2.2.3 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for an optimized signal-to-noise (SNR) ratio.

2.2.4 Baseline Wander Canceller

Baseline wander results from Ethernet links that AC-couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. The AR8113 device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

2.2.5 Auto-Negotiation

The AR8113 device supports 10/100 BASE-T Copper auto-negotiation in accordance with IEEE 802.3 clauses 28 and 40. Auto-negotiation provides a mechanism to transfer information between a pair of link partners to choose the best possible mode of operation in terms of speed, duplex modes, and master/slave preference. Auto-negotiation is initiated upon:

- Power-up reset
- Hardware reset
- Software reset
- Auto-negotiation restart
- Transition from power-down to power-up
- The link goes down

If auto-negotiation is disabled, 10 BASE-T or 100 BASE-TX can be manually selected using the IEEE MII registers.

2.2.6 Automatic Polarity Correction

If cabling has been incorrectly wired, the AR8113 automatically corrects polarity errors on the Rx pairs in 10 BASE-T modes.

2.3 Media Access Control

The media access control (MAC) is an integral part of the AR8113 and the interface to the integrated Fast Ethernet transceiver. The MAC operates at 10/100M full-duplex or 10/100M half-duplex depending on mode. The AR8113 supports VLAN tag insertion on a per-packet base, and VLAN tag stripping is based on VLAN_REMV_EN over software configuration. During normal operation, PAUSE frames are automatically dropped after setting the corresponding delay counter.

2.4 Packet and Descriptor Memory

The AR8113 employs an internal SRAM as the Tx FIFO and Rx FIFO for data traffic elasticity.

2.5 Receive-Side Scaling

The AR8113 supports Rx-side scaling (RSS) to scale the Rx path across multiple CPUs in a multiple-CPU system.

2.6 Host Coalescing

Host coalescing is achieved through automatic coalescing message block and statistics message block.

2.7 CPU Offload

2.7.1 Checksum Offload

The AR8113 supports checksum offload:

Tx	The AR8113 calculates needed checksums and supports checksum on all frame types, IP datagram, and TCP segment with options
Rx	The AR8113 fills in the Rx descriptor structure and sets the appropriate bits. If for any reason the AR8113 cannot perform the checksum, it does not set any bits, and indicates the packet and leaves it to OS to process the frame.

The AR8113 also supports custom checksum offload when the device driver specifies the payload offset position where to start the checksum calculation, and the offset position where to fill the checksum when the calculation is completed. The custom checksum calculation can be combined with IP checksum offload.

2.7.2 TCP Segmentation Offload

With TCP segmentation offload (TSO), TCP can pass a buffer to be transmitted bigger than the maximum transmission unit (MTU) supported by the medium. The AR8113 implements large sends using prototype TCP and IP headers of the incoming send buffer to carve out segments of required size. Copying prototype headers and options then calculating the sequence number and checksum fields creates TCP segment headers. All other information, such as options and flag values, are preserved.

2.7.3 UDP Large Send Offload

When a large UDP datagram is greater than MTU, it must be fragmented into several smaller frames compliant to the MTU constraint. The UDP checksum is calculated over the entire UDP datagram, and Ethernet header and IP header are copied and attached to these fragments individually.

2.8 Message Signaled Interrupts (MSI)

The AR8113 generates interrupts via the PCIE message-signaled interrupt (MSI) or INTx interrupt signaling to inform host CPU of interrupt events. At high data rates, interrupts related to Ethernet frame reception and transmission can quickly overwhelm a host system processor. The AR8113 incorporates an interrupt coalescing scheme to minimize the number of interrupts issued and maximize system performance. An IRQ moderation timer can queue and moderate non-critical interrupts.

2.9 Power Management

2.9.1 ACPI Support

The AR8113 supports OS-controlled power management based on the Advanced Configuration and Power Interface Specification, Rev2.0 (ACPI). Power management registers are in the PCI configuration space. Table 2-3 describes the states supported by the AR8113.

Table 2-3. **Supported Power Mgmt. States**

State	Description	
D0	Uninitialized	Entered after hardware reset or after a transition from D3hot to D0, during which the AR8113 responds to PCI configuration cycles only.
	Active	When configuration registers are initialized, the AR8113 enters the D0 active sub-state, and is then in normal operation power mode and able to respond to PCI I/O memory and configuration.
D1	The AR8113 supports this state optionally based on configuration. In D1, the AR8113 does not initiate PCI transactions with the exception of a PME message due to the wake and link state events. The AR8113 can respond to the PCI configuration accesses to allow the system to change the power state.	
D3	D3hot	The full power-down state. The AR8113 responds to PCI configuration accesses to allow the system to change the power state back to D0 uninitialized. In D3hot, the AR8113 does not respond to any PCI I/O or memory accesses and does not initiate any PCI transactions with the exception of a PME message due to the wake events and link state events.
	D3cold	Power-off state; the AR8113 does not function at all.

2.10 Wake-on-LAN

The AR8113 supports wake-on-LAN (WOL). These wake-up events cause the device to pass the PME message over PCIE to the system in D1, and D3 states:

Table 2-4. **Wake-Up Events**

Event	Description
Wake-Up Frame	The wake-up frame detection logic consists of the pattern RAM and a state machine that is controlled by the register "WOL Control" on page 37. The pattern RAM is shared with packet memory and is filled by software before enabling the wake-up frame detection.
Magic Packet	The ingress data stream is compared against the "magic packet frame", an AMD defined special data pattern. If a data sequence is found, the magic packet frame event is created. The Rx packet must have a valid destination address or multicast address.
Link Status Change	Link status wake events are useful to indicate a change in the network's availability.

Wake-up events are enabled by the register WAKEUP_CTL, and when they occur, are latched in the register WAKEUP_EVENT and are cleared on read.

2.11 Promiscuous Mode

The AR8113 driver normally processes only those network frames containing the matching unicast, multicast or broadcast MAC addresses. When promiscuous mode is enabled, network frames bound for any MAC address are received and passed to the CPU, which can be useful for network troubleshooting; network monitors and other tools rely on promiscuous mode.

2.12 LED Interface

The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. Four status LEDs are available (LED_ACT_L, LED_DUPLEX_L, and LED_LINK10_100_L). These indicate operation speed, duplex mode, and link status. The LEDs can be programmed to different status functions from their default value. They can also be controlled directly from the registers "LED Control" on page 32 and "Manual LED Override" on page 33.

Table 2-5. **LED Modes**

Mode	Description
Single-Color LED	LED interface outputs are all low active. The positive terminal of the LED should be connected to VAUX with a 510Ω resistor, and the negative terminal to the LED interface.

Table 2-5 shows the LED links.

Table 2-6. **LED Link Table**

LED_ACT_L	LED_LINK_10/ 100_L	LED_DUPLEX_L	Selected Speed	Link Status
High	High	High	Any Speed	Link Down
Low	High	High	10 Mbps; Half-Duplex	Link Up
Low	High	Low	10 Mbps; Full Duplex	Link Up
Low	Low	High	100 Mbps; Half-Duplex	Link Up
Low	Low	Low	100 Mbps; Full Duplex	Link Up

2.13 Serial EEPROM Loader

The serial EEPROM Loader is the internal state-machine that retrieves the configuration data from external serial EEPROM. Shortly after the de-assertion of hardware reset, or after the internal power-on-reset cycle, the loader will automatically read the contents out of EEPROM and program the many features of the AR8113.

2.14 Power Supplies

The AR8113 device requires a single power supply: 3.3 V.

2.14.1 Digital Loopback

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the AR8113 device. The registers "100 BASE-TX Test Mode Select", "Debug Register 11", and "Test Configuration for 10 BASE-T" on page 34 are used to determine at which point the signal loops back (for different modes, 10, and 100, respectively). Figure 2-1 shows a block diagram of digital loopback.

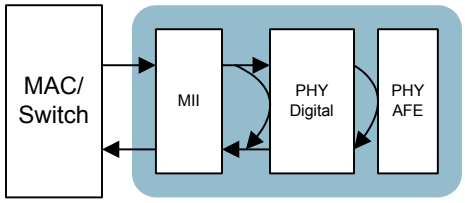

Figure 2-1. **Digital Loopback**

2.14.2 External Cable Loopback

External cable loopback loops MII Tx to MII Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. Figure 2-2 shows a block diagram of external cable loopback.

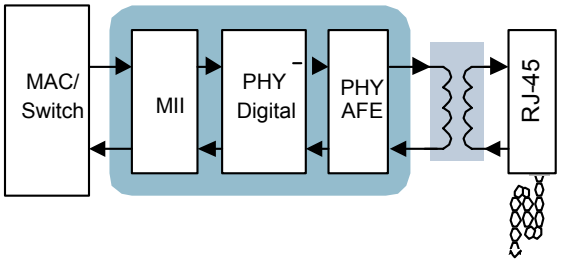

Figure 2-2. **External Cable Loopback**

2.14.3 Cable Diagnostic Test

The Cable Diagnostic Test (CDT) feature in the AR8113 device uses time domain reflectometry (TDR) to identify remote and local PHY malfunctions, bad/marginal cable or patch cord segments, or connectors. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics. CDT can be performed when there is no link partner or when the link partner is auto-negotiating.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the AR8113. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 3-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max Rating	Unit
V_{DD33}	3.3 V Supply Voltage	3.8	V
T_{store}	Storage Temperature	–65 to 150	°C
ESD	Electrostatic Discharge Tolerance	2000	V

3.2 Recommended Operating Conditions

Table 3-2. **Recommended Operating Conditions**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD33}	3.3 V Supply Voltage	—	3.0	3.3	3.6	V
T_A	Ambient Temperature	—	0		70	°C
T_J	Junction Temperature	—		TBD		°C
θ_{JA}	Junction to Ambient Temperature	2-Layer PCB		63.5		°C/W
		4-Layer PCB		33.3		°C/W
θ_{JC}	Junction to Case Temperature	2-Layer PCB		16.3		°C/W
		4-Layer PCB		15.9		°C/W
θ_{JT}	Junction to Top Center	2-Layer PCB		TBD		°C/W
		4-Layer PCB		3.8		°C/W

3.3 TWSI Characteristics

Table 3-3 shows the TWSI_DC characteristics.

Table 3-3. **TWSI_DC Characteristics**

Symbol	Parameter	Min	Max	Unit
V_{OH}	Output High Voltage	—	0.4	V
V_{IH}	Input High Voltage	1.8	3.2	V
V_{IL}	Input Low Voltage	–0.6	0.8	V
I_{IL}	Input Low Current	—	3	µA

Figure 3-1 shows the TWSI timing diagram.

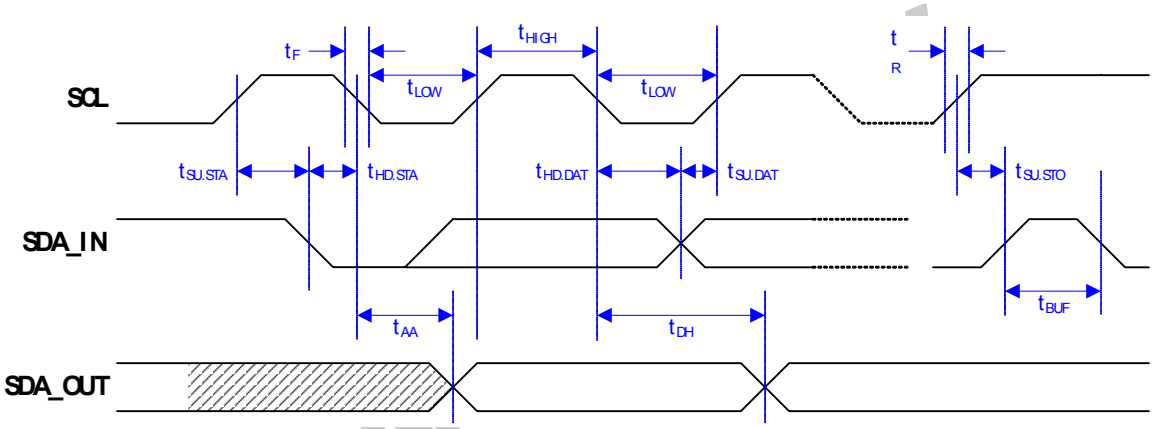

Figure 3-1. **TWSI Timing Diagram**

Table 3-4 shows the TWSI_AC characteristics.

Table 3-4. **TWSI_AC Characteristics**

Symbol	Parameter	Min	Max	Unit
$t_{HD.STA}$	Start Hold Time	0.6	—	µs
$t_{SU.STA}$	Start Setup Time	0.6	—	µs
$t_{HD.DAT}$	Data in Hold Time	0	—	
$t_{SU.DAT}$	Data in Setup Time	100	—	ns
t_R	Inputs Rise Time	0.3	—	µs
t_F	Inputs Fall Time	300	—	ns
$t_{SU.STO}$	Stop Setup Time	0.6	—	µs
t_{DH}	Data Out Hold Time	50	—	ns
t_{WR}	Write Cycle Time	5	—	ms

3.4 Typical Power Consumption Parameters

Table 3-5 shows the typical power drain as a function of the AR8113's operating mode.

Table 3-5. **Total System Power**

Mode	3.3 V (mA)	Power Consumption (mW)
10 Mbps	TBD	TBD
100 Mbps	TBD	TBD

4. Register Descriptions

Table 4-1 shows the reset types used in this document.

Table 4-1. **Register Reset Types**

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or a reset occurs.

Table 4-1. **Register Reset Types (continued)**

Type	Description
Retain	Value written to a register field takes effect without a software reset.
SC	Self-Clear. Writing a one to this register causes the desired function to execute immediately, and the register field clears to zero when the function is complete.
Update	The value written to the register field does not take effect until a software reset is executed. The value can still be read after it is written.

4.1 General Register Summary

Table 4-2 summarizes the general registers for the AR8113.

Table 4-2. **General Register Summary**

Offset	Register	Page
0x00	Control	page 20
0x01	Status	page 21
0x02	PHY Identifier [18:3]	page 22
0x03	PHY Identifier [19:24]	page 22
0x04	Auto-Negotiation Advertisement	page 22
0x05	Link Partner Ability (Base Page)	page 23
0x06	Auto-Negotiation Expansion	page 24
0x07	Reserved	—
0x08	Reserved	—
0x0F	Reserved	—
0x10	Reserved	—
0x11	PHY-Specific Status	page 25
0x12	Interrupt Enable	page 26
0x13	Interrupt Status	page 27
0x14	Extended PHY-Specific Control	page 28
0x16	Cable Defect Tester Control	page 31
0x18	LED Control	page 29
0x19	Manual LED Override	page 30
0x1C	Cable Defect Tester Status	page 31

4.1.1 Control

Offset: 0x00
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	SW Reset	Description				
15	RESET	SC	PHY software reset				
			0	Normal operation			
			1	PHY reset Writing a 1 to this bit causes immediate PHY reset. Once the operation is done, this bit clears to 0 automatically.			
14	LOOPBACK	0	When loopback is active, the transmitter data on TXD loops back to RXD internally. The link breaks when loopback is enabled.				
			0	Disable loopback			
			1	Enable loopback			
13	SPEED_SELECTION (LSB)	Retain	Upon hardware reset: if RESTART_AUTO_NEGOTIATION (bit [9]) = 1, this bit has no effect. If RESTART_AUTO_NEGOTIATION = 0, bit [6] and bit [13] must be set by the power-on strapping pins SPEED[1:0]. See Table 1-1, "Signal to Pin Relationships and Descriptions," on page 7.				
			Speed [1]	**Speed [0]**	**Speed Selection**	**Bit [6]**	**Bit [13]**
			0	0	10 Mbps	0	0
			0	1	100 Mbps	0	1
			1	0	Reserved	1	0
			1	1	Reserved	1	1
12	AUTO_ NEGOTIATION	Retain	On hardware reset, this bit depends on the power-on strapping pin: AN_EN. See Table 1-1, "Signal to Pin Relationships and Descriptions," on page 7.				
			0	Disable auto-negotiation process			
			1	Enable auto-negotiation process			
11	POWER_DOWN	0	When the port switches from power-down to normal operation, software reset and restart auto-negotiation perform even if RESET (bit [15]) and RESTART_AUTO_NEGOTIATION (bit [9]) are not set.				
			0	Normal operation			
			1	Power-down			
10	RES	0	Reserved				
9	RESTART_AUTO_ NEGOTIATION	SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not this bit is set.				
			0	Normal operation			
			1	Restart auto-negotiation process			
8	DUPLEX MODE	Retain	On hardware reset, this bit depends on the power-on strapping pin DUPLEX. See Table 1-1, "Signal to Pin Relationships and Descriptions," on page 7.				
			0	Half-duplex			
			1	Full-duplex			
7	COLLISION TEST	0	Setting this bit to 1 causes the COL pin to assert whenever the TX_EN pin is asserted. This bit takes effect only in 10M loopback mode.				
			0	Disable COL signal test			
			1	Enable COL signal test			
6	SPEED SELECTION (MSB)	Update	See description in bit ["13"]				
5:0	RES	00000	Reserved. Always set to 00000.				

4.1.2 Status

Offset: 0x01
Mode: Read-Only
Hardware Reset: 0x7949
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
15	100BASE-T4	0	100 BASE-T4 (this protocol is not available)	
			0	PHY not able to perform 100 BASE-T4
14	100BASE-X FULL-DUPLEX	1	Capable of 100-Tx Full Duplex operation	
13	100BASE-X HALF-DUPLEX	1	Capable of 100-Tx Half Duplex operation	
12	10 MBPS FULL-DUPLEX	1	Capable of 10 BASE-T full duplex operation	
11	10 MBS HALF-DUPLEX	1	Capable of 10 BASE-T half duplex operation	
10	100BASE-T2 FULL-DUPLEX	0	Not able to perform 100 BASE-T2	
9	100BASE-T2 HALF-DUPLEX	0	Not able to perform 100 BASE-T2	
8	EXTENDED STATUS	1	Extended status information	
7	RESERVED	0	Always 0	
6	MF PREAMBLE SUPPRESSION	1	PHY accepts management frames with preamble suppressed	
5	AUTO-NEGOTIATION COMPLETE	0	0	Auto negotiation process not complete
			1	Auto negotiation process complete
4	REMOTE FAULT	0	This bit clears after read “SC”	
			0	Remote fault condition detected
			1	Remote fault condition not detected
3	AUTO-NEGOTIATION ABILITY	1	PHY able to perform auto negotiation	
2	LINK STATUS	0	Indicates whether the link was lost since the last read. For the current link status, read LINK_REAL_TIME (bit [10]) of the register “PHY-Specific Status” on page 25. Latching low function.	
			0	Link is down
			1	Link is up
1	JABBER DETECT	0	This bit clears after read “SC”	
			0	Jabber condition not detected
			1	Jabber condition detected
0	EXTENDED CAPABILITY	1	Extended register capabilities	

4.1.3 PHY Identifier [18:3]

Offset: 0x02
Mode: Read-Only
Hardware Reset: 0x004D
Software Reset: 0x004D

Bit	Name	Description
15:0	Unique Identifier Bit	Organizationally unique identifier bits [18:3]

4.1.4 PHY Identifier [19:24]

Offset: 0x03
Mode: Read-Only
Hardware Reset: 0xD04E
Software Reset: 0xD04E

Bit	Name	Description
15:0	OUI LSB Model Revision	Organizationally unique identifier bits [19:24]

4.1.5 Auto-Negotiation Advertisement

Offset: 0x04
Mode: Read/Write
Hardware Reset: 0x0DE1
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
15	NEXT_PAGE	Retain	This bit should be set to 0 if no additional next pages are needed.	
			0	Not advertised
			1	Advertise
14	ACK	0	Must be set to 0	
13	REMOTE FAULT	Retain	Write a 1 to set remote fault	
12	RES	0	Reserved	
11	ASYMMETRIC PAUSE	Retain	Write a 1 to set asymmetric pause	
10	PAUSE	Retain	Write a 1 to set pause.	
9	100BASE-T4	0	Not able to perform 100 BASE-T4	
8	100BASE-TX FULL DUPLEX	Retain	Write a 1 to advertise	
7	100BASE-TX HALF DUPLEX	Retain	Write a 1 to advertise	
6	10BASE-TX FULL DUPLEX	Retain	Write a 1 to advertise	
5	10BASE-TX HALF DUPLEX	Retain	Write a 1 to advertise	
4:0	SELECTOR FIELD	00001	Selector field mode	
			00001	802.3

4.1.6 Link Partner Ability (Base Page)

Offset: 0x05
Mode: Read-Only
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description	
15	NEXT PAGE	Received code word bit [15]	
		0	Link partner not capable of next page
		1	Link partner capable of next page
14	ACK	Acknowledge; received code word bit [14]	
		0	Link partner does not have next page ability
		1	Link partner received link code word
13	REMOTE FAULT	Received code word bit [13]	
		0	Link partner has not detected remote fault
		1	Link partner detected remote fault
12	TECHNOLOGY ABILITY FIELD	This bit clears when the link goes down and loads when a base page is received. Received code word bit [12].	
11	ASYMMETRIC PAUSE	Received code word bit [11]	
		0	Link partner does not request asymmetric pause
		1	Link partner requests asymmetric pause
10	PAUSE	Received code word bit [10]	
		0	Link partner is not capable of pause operation
		1	Link partner is capable of pause operation
8	100BASE-TX FULL DUPLEX	Received code word bit [8]	
		0	Link partner is not 100 BASE-TX full-duplex capable
		1	Link partner is 100 BASE-TX full-duplex capable
7	100BASE-TX HALF DUPLEX	Received code word bit [7]	
		0	Link partner is not 100 BASE-TX half-duplex capable
		1	Link partner is 100 BASE-TX half-duplex capable
6	10BASE-TX FULL DUPLEX	Received code word bit [6]	
		0	Link partner is not 10 BASE-T full-duplex capable
		1	Link partner is 10 BASE-T full-duplex capable
5	10BASE-TX HALF DUPLEX	Received code word bit [5]	
		0	Link partner is not 10 BASE-T half-duplex capable
		1	Link partner is 10 BASE-T half-duplex capable
4:0	SELECTOR FIELD	Received code word bit [4:0]	

4.1.7 Auto-Negotiation Expansion

Offset: 0x06
Mode: Read-Only
Hardware Reset: 0x0004
Software Reset: Decided by the PHY inner state

Bit	Name	Description	
15:5	RES	Reserved. Must be set to 0.	
4	PARALLEL DETECTION FAULT	Software resets this bit to 0; clear after read	
		0	No fault has been detected
		1	A fault has been detected
3	LINK PARTNER NEXT PAGE ABLE	Software resets this bit to 0; clear after read	
		0	Link partner is not next page capable
		1	Link partner is next page capable
2	LOCAL NEXT PAGE ABLE	The software reset value is determined by bit [15] of the "Auto-Negotiation Advertisement" register	
		0	Local device is not next page capable
		1	Local device is next page able
1	PAGE RECEIVED	On software reset, this bit value is reserved; LH; cleared after a read.	
		0	No new page has been received
		1	A new page has been received
0	LINK PARTNER AUTO-NEGOTIATION ABLE	Software reset to 0.	
		0	Link partner is not auto-negotiation capable
		1	Link partner is auto-negotiation capable

Offset: 0x0F
Mode: Read-Only
Hardware Reset: 0x2000
Software Reset: 0

Bit	Name	Description
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11:0	RES	Reserved

4.1.8 PHY-Specific Status

Offset: 0x11
Mode: Read-Only
Hardware Reset: 0x0010
Software Reset: 0

Bit	Name	Description	
15:14	SPEED	Valid only after resolved bit [11] of this register = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.	
		00	10 Mbps
		01	100 Mbps
		10	Reserved
		11	Reserved
13	DUPLEX	Valid only after resolved bit [11] of this register = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.	
		0	Half-duplex
		1	Full-duplex
12	PAGE_RECEIVED (real-time)	0	Page not received
		1	Page received
11	SPEED_DUPLEX_ RESOLVED	When Auto-Negotiation is not enabled, this bit = 1 for force speed	
		0	Not resolved
		1	Resolved
10	LINK (real-time)	0	Link down
		1	Link up
9:7	RES	Reserved. Always set to 0.	
6	MDI_CROSSOVER_ STATUS	Valid only after resolved bit [11] of this register = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.	
		0	MDI
		1	MDIX
5	SMARTSPEED_ DOWNGRADE	0	Smartspeed downgrade does not occur
		1	Smartspeed downgrade occurs
4	ENERGY_DETECT_ STATUS	0	Active
		1	Sleep
3	TRANSMIT_PAUSE _ENABLED	Valid only after resolved bit [11] of this register = 1. The resolved bit is set when auto-negotiation is completed or disabled. A reflection of the MAC pause resolution.	
		0	Tx pause disabled
		1	Tx pause enabled
2	RECEIVE_ PAUSE_ENABLED	A reflection of the MAC pause resolution. This status bit is valid only after resolved bit [11] of this register = 1. The resolved bit is set when auto-negotiation is completed or disabled.	
		0	Rx pause disabled
		1	Rx pause enabled
1	POLARITY (real-time)	0	Normal
		1	Reversed
0	JABBER (real-time)	0	No jabber
		1	Jabber

4.1.9 Interrupt Enable

Offset: 0x12
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
15	Auto-Negotiation Error Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
14	Speed Changed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
13	Duplex Changed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
12	Page Received Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
11	Auto-Negotiation Completed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
10	Link Status Changed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
9	Symbol Error Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
8	False Carrier Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
7	FIFO Over/ Underflow Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
6	MDI Crossover Changed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
5	Smartspeed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
4	Energy Detect Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
3:2	RES	0	Reserved. Always set to 00.	
1	Polarity Changed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
0	Jabber Interrupt Enable	0	0	Interrupt disable
			1	Interrupt enable

4.1.10 Interrupt Status

Offset: 0x13
Mode: Read-Only
Hardware Reset: 0

Note: All bits clear on read.

Bit	Name	Description	
15	AUTO _NEGOTIATION_ ERROR	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed.	
		0	No Auto-Negotiation Error
		1	Auto-Negotiation Error
14	SPEED_CHANGED	0	Speed not changed
		1	Speed changed
13	DUPLEX_ CHANGED	0	Duplex not changed
		1	Duplex changed
12	PAGE_RECEIVED	0	Page not received
		1	Page received
11	AUTO_ NEGOTIATION_ COMPLETED	0	Auto-negotiation not completed
		1	Auto-negotiation completed
10	LINK_STATUS _CHANGED	0	Link status not changed
		1	Link status changed
9	SYMBOL_ERROR	0	No symbol error
		1	Symbol error
8	FALSE_CARRIER	0	No false carrier
		1	False carrier
7	FIFO_OVER/ _UNDERFLOW	0	No FIFO error
		1	Over/underflow error
6	MDI_CROSSOVER _CHANGED	0	Crossover not changed
		1	Crossover changed
5	SMARTSPEED _INTERRUPT	0	No Smartspeed interrupt detected
		1	Smartspeed interrupt detected
4	ENERGY_DETECT _CHANGED	0	No energy detect state change detected
		1	Energy detect state changed
3:2	RES	Reserved. Always set to 00.	
1	POLARITY_ CHANGED	0	Polarity not changed
		1	Polarity changed
0	JABBER	0	No jabber
		1	Jabber

4.1.11 Extended PHY-Specific Control

Offset: 0x14
Mode: Read/Write
Hardware Reset: 0x02C
Software Reset: See field descriptions

Bit	Name	Reset	Description	
15:6	RES	0	Reserved. Must be set to 00000000.	
5	SMARTSPEED_EN	Reset to respective bit value 0x002C	Default = 1; if this bit is set to one and cable inhibits completion of the training phase, then after a few failed attempts, the device automatically adjusts the highest ability to the next lower speed: from 100 to 10.	
4:2	SMARTSPEED_RETRY _LIMIT	Reset to respective bit value 0x002C	The default value is three; if set to three, then the device attempts five times before adjusting; the number of attempts can be changed through setting these bits.	
			000	2 retries
			001	3 retries
			010	4 retries
			011	5 retries (default)
			100	6 retries
			101	7 retries
			110	8 retries
			111	9 retries
1	BYPASS_SMARTSPEED _TIMER	Reset to respective bit value 0x002C	0	The stable link condition is determined 2.5 seconds after the link is established (default)
			1	The stable link condition is determined as soon as the link is established
0	RES	Reset to respective bit value 0x002C	Reserved. Must be set to 0.	

4.1.12 Cable Defect Tester Control

Offset: 0x16
Mode: Read-Only
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description	
15:10	RES	Reserved	
9:8	MDI_PAIR_ SELECT	Cable defect tester (CDT) control registers Use the cable defect tester control registers to select which MDI pair is shown in the register "Cable Defect Tester Status" on page 31.	
		00	MDI[0] pair
		01	MDI[1] pair
		10	Reserved
		11	Reserved
7:1	RES	Reserved	
0	ENABLE_TEST	When set, hardware automatically disable this bit when CDT is done	
		0	Disable CDT Test
		1	Enable CDT Test

4.1.13 LED Control

Offset: 0x18
Mode: Read/Write
Hardware Reset: 0x4100
Software Reset: No default on software reset

Bit	Name	Description	
15	DISABLE_LED	0	Enable
		1	Disable
14:12	LED_ON_TIME	000	5 ms
		001	10 ms
		010	21 ms
		011	42 ms
		100	84 ms
		101	168 ms
		111:110	Reserved
11	FORCE_INTERRUPT	Always set to 0	
10:8	LED_OFF_TIME	000	21 ms
		001	42 ms
		010	84 ms
		011	168 ms
		100	330 ms
		101	671 ms
		111:110	Reserved
7:5	RES	Reserved	
4:3	LED_LINK_ CONTROL	00	Direct LED mode
		11	Master/slave LED mode
		01, 10	Combined LED modes
2	LED_DUPLEX_ CONTROL	0	Duplex
		1	Duplex/Collision
1	LED_RX_CONTROL	0	Rx activity
		1	Rx activity and link
0	LED_TX_CONTROL	0	Tx activity
		1	Tx activity and link

4.1.14 Manual LED Override

Offset: 0x19
Mode: Read/Write
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description	
15:12	RES	Reserved	
11:10	LED_DUPLEX	■ LED OFF: LED pin output is high ■ LED ON: LED pin output is low	
		00	Normal
		01	Blink
		10	LED Off
		11	LED On
9:8	LED_LINK10	■ LED OFF: LED pin output is high ■ LED ON: LED pin output is low	
		00	Normal
		01	Blink
		10	LED Off
		11	LED On
7:6	LED_LINK100	■ LED OFF: LED pin output is high ■ LED ON: LED pin output is low	
		00	Normal
		01	Blink
		10	LED Off
		11	LED On
3:2	LED_RX	■ LED OFF: LED pin output is high ■ LED ON: LED pin output is low	
		00	Normal
		01	Blink
		10	LED Off
		11	LED On
1:0	LED_TX	■ LED OFF: LED pin output is high ■ LED ON: LED pin output is low	
		00	Normal
		01	Blink
		10	LED Off
		11	LED On

4.1.15 Cable Defect Tester Status

Offset: 0x1C
Mode: Read-Only
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description	
15:10	RES	Reserved	
9:8	STATUS	The content of this register applies to the cable pair selected in the register "Cable Defect Tester Control" on page 28.	
		00	Valid test, normal cable (no short or open in cable)
		01	Valid test, short in cable (Impedance < 33 Ω)
		10	Valid test, open in cable (Impedance > 333 Ω)
		11	Test fail
7:0	DELTA_TIME	Delta time to indicate distance	

4.2 Device Configuration Register Summary

Table 4-3 summarizes the PCI configuration registers for the AR8113.

Table 4-3. **PCI Configuration Register Summary**

Offset	Register	Page
0x140C	Enable PHY	page 32
0x14A0	WOL Control	page 32

4.2.1 Enable PHY

Offset: 140C
Mode: Read/Write
Reset: See field descriptions

Bit	Name	Reset	Description
15:1	RES	0	Reserved
0	PHY_RESET	0	PHY reset; PHY is in reset state at power-on, the software driver must set this bit to bring the PHY online.

4.2.2 WOL Control

Offset: 0x14A0
Mode: See field descriptions
Reset: 0

Bit	Name	Mode	Description
31	RES	RO	Reserved
30	PT6_MATCH	RC	Pattern 6 match
29	PT5_MATCH	RC	Pattern 5 match
28	PT4_MATCH	RC	Pattern 4 match
27	PT3_MATCH	RC	Pattern 3 match
26	PT2_MATCH	RC	Pattern 2 match
25	PT1_MATCH	RC	Pattern 1 match
24	PT0_MATCH	RC	Pattern 0 match
23	RES	RO	Reserved
22	PT6_EN	RW	Pattern 6 enable
21	PT5_EN	RW	Pattern 5 enable
20	PT4_EN	RW	Pattern 4 enable
19	PT3_EN	RW	Pattern 3 enable
18	PT2_EN	RW	Pattern 2 enable
17	PT1_EN	RW	Pattern 1 enable
16	PT0_EN	RW	Pattern 0 enable
15	CLK_SWH_EN	RW	Enable clock switch in sleep mode;
14:11	RES	RO	Reserved
10	LINK_ST_CHG_ST	RC	Link status changed from down to up
9	MAGIC_FRAME_ST	RC	Magic frame detected
8	WAKEUP_FRAME_ST	RC	Wakeup frame detected
7:6	RES	RO	Reserved
5	LINK_ST_CHG_PME	RW	Link status change PME enable
4	LINK_ST_CHG_EN	RW	Link status change enable
3	MAGIC_FRAME_PME	RW	Enable PME on magic frame detection
2	MAGIC_FRAME_EN	RW	Enable magic frame detection

Bit	Name	Mode	Description
1	WAKEUP_FRAME_PME	RW	Enable PME on wakeup frame detection
0	WAKEUP_FRAME_EN	RW	Enable wakeup frame detection

5. Package Dimensions

The AR8113 is packaged in a 48-pin QFN package. The package drawings and dimensions are provided in Figure 5-1 and Table 5-1.

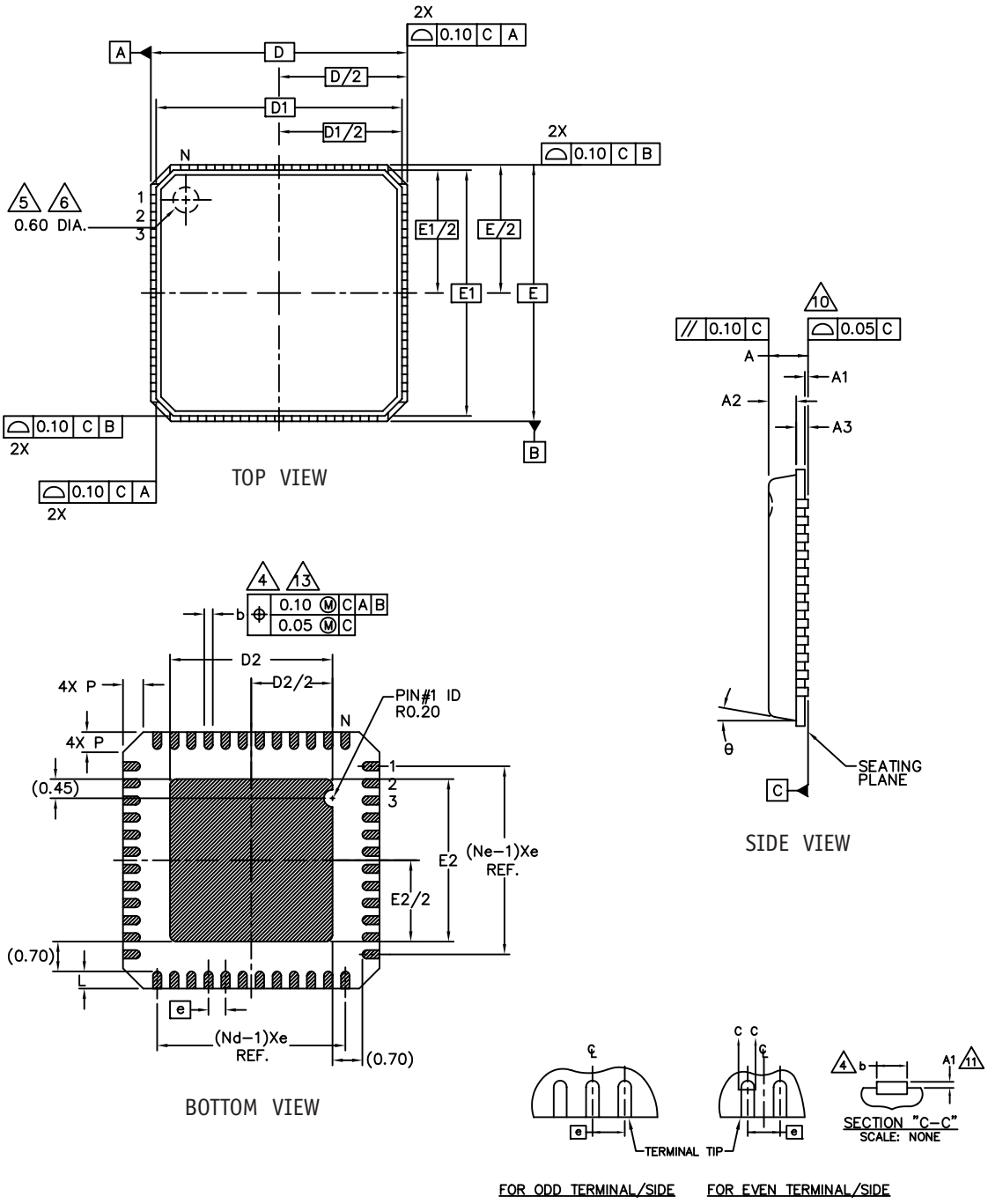

Figure 5-1. **Package Views**

Table 5-1. **Package Dimensions**

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm	0.031	0.033	0.035	inches
A1	0.00	0.01	0.05	mm	0.000	0.001	0.002	inches
A2	0.60	0.65	0.70	mm	0.024	0.026	0.028	inches
A3	0.20 REF				0.008 REF			
b	0.15	0.20	0.25	mm	0.006	0.008	0.010	inches
D/E	6.00 BASIC			mm	0.236 BASIC			inches
D1/E1	5.75 BASIC			mm	0.226 BASIC			inches
D2/E2	3.70	3.80	3.90	mm	0.145	0.149	0.153	inches
e	0.40 BASIC			mm	0.016 BASIC			inches
L	0.30	0.40	0.50	mm	0.012	0.016	0.020	inches
N	48				48			
Nd	12				12			
Ne	12				12			
P	0.24	0.42	0.60	mm	0.009	0.016	0.023	inches
θ	—	—	12	°	—	—	12	°

Notes:

1. Die thickness allowable is 0.305 mm (0.012 inches) maximum.
2. Dimensioning and tolerances conform to ASME Y14.5M. – 1994.
3. N is the number of terminals.
   Nd is the number of terminals in the X-direction and
   Ne is the number of terminals in the Y-direction.
4. Dimension b applies to plated terminal and is measured between 0.20 and 0.25 mm from the terminal tip.
5. The pin#1 identifier must exist on the top surface of the package by using an identification mark or other feature of the package body.
6. The exact shape and size of this feature is optional.
7. All dimensions are in millimeters.
8. The shape shown on four corners are not actual I/O.
9. Package warpage maximum 0.05 mm.
10. Bilateral coplanarity zone applies to the exposed pad as well as the terminals.
11. Applied only for terminals.
12. Q and R apply only for straight tiebar shapes.
13. For 0.40 mm lead pitch, the lead position tolerance must be 0.07 mm at the actual mean value of body size.

6. Ordering Information

The order number AR8113-AL1E specifies a lead-free version of the AR8113.

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