Cortina Systems® CS8032/CS8033 EPON Optical Networking Unit

Preliminary Datasheet

The Cortina Systems® CS8032/CS8033 EPON Optical Networking Unit Optical Network Unit (ONU) chip (CS8032/CS8033 EPON ONU) implements functions for Customer Premise Equipment (CPE). Equipment vendors can build a complete CPE box with the CS8032/CS8033 EPON ONU and add extra features using the embedded CPU, spare Flash memory space, external SRAM interface, and flexible GPIO bus.

The CS8032/CS8033 EPON ONU is an IEEE 802.3ah* standard-compliant device. It allows equipment vendors and network operators to build an EPON system mixing and matching with different IEEE 802.3ah* compliant devices. The standard-compliant solution enables network operators to preserve their investment and save their cost in the long run.

Applications

应用

- POTS Migration Application
- Power Meter Applications
- MDU Application
- Single Family Unit (SFU) Applications (SFU1-5)
- HGW Application

Product Features

产品特点

- Full compliance with the IEEE 802.3-2008 specification for EPON SNI, GE/FE UNI
- Supports Ethernet, EPON, and CTCv2.1 OAM
- Compliance with 802.1Q
- Integrated 802.1ad and stacked VLAN support
- Advanced L2/L3/L4 traffic classification
- Supports 802.1D bridging 64 MAC addresses
- Support for frame sizes 64-2000 Bytes
- On-chip frame buffer for packet storage
- Advanced traffic management for traffic policing, scheduling, and shaping
- Ingress rate limiting for the UNI GE, the EPON, and the UNI/Management FE ports
- 32 flow rate limiters and 4 aggregate rate limiters for data or control traffic rate limiting
- Egress shaping for the UNI port
- IPv4 and IPv6 support
- IP Multicast Support - IGMPv3/MLD snooping, and packet replication to multiple ports or VLANs
- Tail Drop threshold support for both upstream and downstream traffic
- SP, DWRR, and SP+DWRR output scheduling
- Queue level reporting to support DBA
- EPON FEC in upstream & downstream channels
- 128-bit AES and Churning Encryption
- Built-in ARM926EJ-S* 32-bit RISC Processor
- Industrial ambient temperature: -40 ºC to 85 ºC
- 225-pin TFBGA package
- ~530 mW power dissipation in typical operation
- Supports Timing Synchronization
- IEEE1588 Transparent Clock support with hardware assist for accurate timestamping
- Integrated SerDes for the EPON port
- Energy Efficient Ethernet support for UNI port
- Supported Interfaces:
  - 1 × RGMII for UNI data
  - 1 × RMII for UNI/Management
  - 1 × SerDes for external EPON transceiver
  - MDIO master for PHY management
  - Parallel Flash and External SDRAM
  - PCM
  - SPI for Serial Flash, EEPROM, SLAC
  - GPIO/LED, multiple UARTs, I^2C, and JTAG
  - 1.0 V core and 2.5/3.3 V I/O LVCMOS I/Os

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Revision History

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Revision 1.1 Revision Date: 10 December 2010
Advance draft. Information in this document subject to change without notice. Changes for this draft: • Updated ball map and corresponding signal names. • Added information watchdog timer. • General edits.

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Advance draft. Information in this document subject to change without notice.

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1.0 Introduction

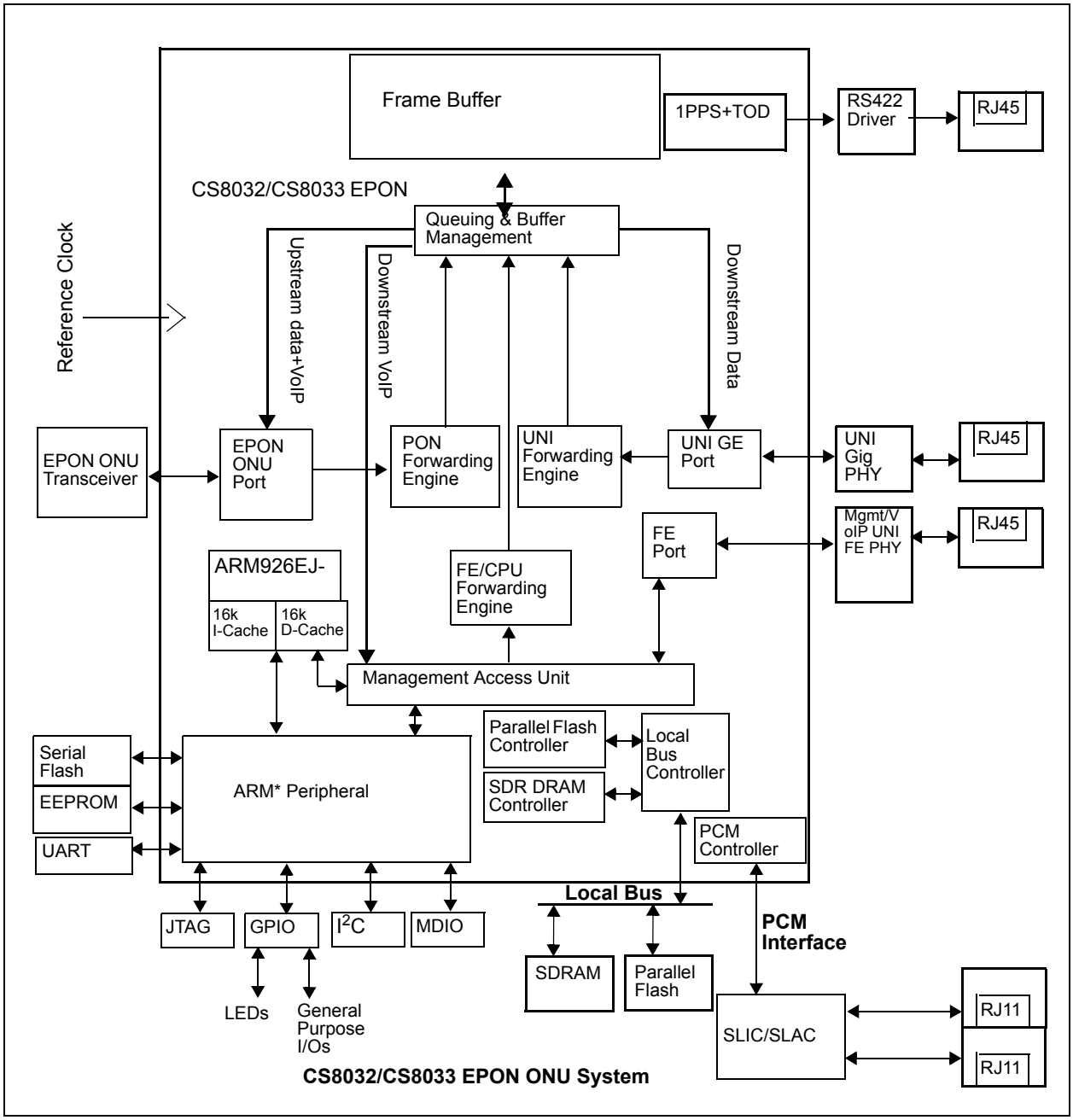
This document highlights major functions as well as electrical and thermal characteristics of the Cortina Systems® CS8032/CS8033 EPON Optical Networking Unit.

The CS8032/CS8033 EPON ONU is a highly integrated low cost, fourth generation EPON ONU device from Cortina Systems, Inc. targeted to FTTH application with support for on-chip VoIP solution. It interfaces on one side with a single EPON transceiver and on the other side with two Ethernet UNI ports. One of the UNI ports is a Gigabit Ethernet (GE) port that can operate at 10/100/1000 Mbps. The second UNI port is a Fast Ethernet (FE) port that can be alternatively used as a management port or for connecting to an external device with an Ethernet port. The CS8032/CS8033 EPON ONU has an embedded EPON SerDes that can interface directly with an external EPON ONU transceiver. The CS8032/CS8033 EPON ONU has an embedded ARM926EJ-S* Processor with DSP extensions and 16k I-cache and 16k D-cache. The CS8032/CS8033 EPON ONU supports several ARM* peripherals: UARTs, EEPROM, serial Flash, and parallel flash. The processor stores data and instructions in an off-chip SDRAM device or an internal SiP SDRAM die. The ARM* processor can run at 125 MHz for data application or switch to 500 MHz operating frequency, dynamically, for applications like VoIP DSP that require higher performance or for power saving mode. A dedicated PCM interface can support at most two narrowband VoIP channels. In addition, it supports 16 GPIOs that can be used for driving LEDs or can be used for any other purposes.

The CS8032/CS8033 EPON ONU supports packet Classification, Layer2 switching, rate limiting, queuing, and scheduling. It supports both IPv4 and IPv6 protocols. It can also detect many special packets like ARP, DHCP, BPDU, etc. The CS8032/CS8033 EPON ONU supports multiple rate limiters including 32 flow rate limiters and 4 aggregate rate limiters that can help prevent DoS attacks to the CPU.

Figure 1 illustrates an ONU system with the CS8032/CS8033 EPON ONU. It highlights some of the functional blocks in the device. Section 2.0 provides an overview of some of the salient features of the device. Section 3.0 briefly describes the data flow inside the device.

Figure 1 High Level Block Diagram



2.0 Overview

The CS8032/CS8033 EPON ONU is designed to have separate data paths for Upstream and Downstream traffics. All features and functions (except of AES and Triple churning) are available for both directions. The software has complete control over the configuration of each feature at subscriber (LLID//VLAN) granularity.

Following is a list of the high level features of the CS8032/CS8033 EPON ONU:

- Full compliance with the IEEE 802.3-2008 specification for EPON SNI, GE/FE UNI functions
- Ethernet, EPON, and CTCv2.1 Operation, Administration and Management (OAM) support
- Compliance with 802.1Q
- Integrated 802.1ad and stacked VLAN support
- Advanced L2/L3/L4 traffic classification
- Support for 802.1D bridging with at most 64 learned MAC addresses
- Support for frame sizes 64-2000 bytes
- On-chip frame buffer for packet storage
- Advanced traffic management for traffic rate limiting, scheduling and shaping
- Ingress rate limiting for the UNI GE, the EPON, and the UNI/Management FE ports
- 32 flow rate limiters and 4 aggregate rate limiters for data or control traffic rate limiting
- Egress shaping for the UNI port
- IPv4 and IPv6 support
- IP Multicast Support - IGMPv3/MLD snooping, and packet replication to multiple ports or VLANs
- Tail Drop threshold support for both upstream and downstream traffic
- SP, DWRR, and SP+DWRR output scheduling
- Queue level reporting to support Dynamic Bandwidth Allocation (DBA) algorithms
- EPON Forward Error Correction (FEC) in upstream and downstream channels
- 128-bit AES and Churning Encryption
- Integrated SerDes for the EPON port
- Built-in ARM926EJ-S* 32-bit RISC Processor and peripherals for management and control:
  - 16k I-cache and 16k D-cache
  - Can dynamically switch between 125 MHz and 500 MHz clock for high performance applications like VoIP DSP
  - Supports one SDR SDRAM for instruction and data which can be one of the following:
    - An external SDRAM up to 32 MB
    - An internal 2 MB or 8 MB SiP SDRAM
- Industrial ambient temperature range -40 ºC to 85 ºC
- 225-pin TFBGA package
- ~530 mW power dissipation in typical operating conditions with parts from typical corner

- Supports Timing Synchronization:
  - IEEE1588 Transparent Clock support with hardware assist for accurate timestamping of SYNC packets
  - 1PPS+TOD support
  - IEEE802.1as Clause 13 EPON TOD support
- Supported Interfaces:
  - 1 × RGMII interface for UNI data
  - 1 × RMII interface for UNI/Management port
  - 1 × SerDes interface for external EPON transceiver
  - MDIO master for PHY management
  - Parallel Flash interface
  - PCM interface for VoIP application
  - Generic Serial interface (SSP) that supports Serial Flash, EEPROM and SLIC/SLAC devices
  - Support for GPIO/LED, multiple UARTs, I^2C, and JTAG
  - 1.0 V core and 2.5/3.3 V I/O LVCMOS I/Os

3.0 Data Flow

The CS8032/CS8033 EPON ONU is an Ethernet Passive Optical Network (EPON) ONU with one GE and an EPON port. In addition, there is an on-chip CPU to run control software and one dedicated FE management port. Figure 1 illustrates the functional blocks in the CS8032/CS8033 EPON ONU. A brief description of the functional blocks is presented in this section along with an overview of data flow. The functional blocks are described in details in other sub-sections of this documents.

The CS8032/CS8033 EPON ONU data starts at the Network interface for packets received from one of the following sources:

- EPON SNI port
- GE UNI port
- UNI/Management FE port
- Software running on the on-chip Control CPU

Bit streams received on a port is processed by the appropriate MAC in the functional block from all EPON/GE/FE port. The port logic then sends the packet through the respective Forwarding Engine. One Forwarding Engine is dedicated for each one of the following:

- EPON port
- GE UNI port
- UNI/management FE port

The respective Forwarding Engine parses the packet and then performs functions like Classification, access control, forwarding decision, packet editing etc. The packet coming out of the respective Forwarding Engine is the final edited packet. An edited packet will be either stored in the upstream or downstream packet memory or dropped. A packet may be dropped because of an error condition like CRC mismatch or because of forwarding decision made by the Forwarding Engine. Besides packet editing the destination of the packet and the queue in which it can be stored are decided by the Forwarding Engine. The packet then is stored in the Frame Buffer by the Queuing and Buffer Management functional block.

The stored packets are scheduled by the Scheduler, read out of the Frame Buffer, and transmitted on the destination port that was decided by the Forwarding Engine.

For example, if a downstream packet is received on the EPON port, the EPON MAC will process bit streams from the EPON transceiver. The EPON MAC will then send the packet to the EPON Forwarding Engine along with CRC error indication. The EPON Forwarding Engine will parse the packet and do Classification, access control, forwarding decision, packet editing etc. The packet from the EPON Forwarding Engine will pass through the EPON Port FIFO and will be stored in the appropriate queue by the Queuing and Buffer Management Unit if there is no CRC error. The destination port is also decided by the EPON Forwarding Engine. If, for example, the destination port is the UNI GE port, the packet will be transmitted to the UNI GE Port functional block that has the GE transmit MAC in it. The packet will then go to the GE PHY and will be transmitted on the Ethernet line by the GE PHY.

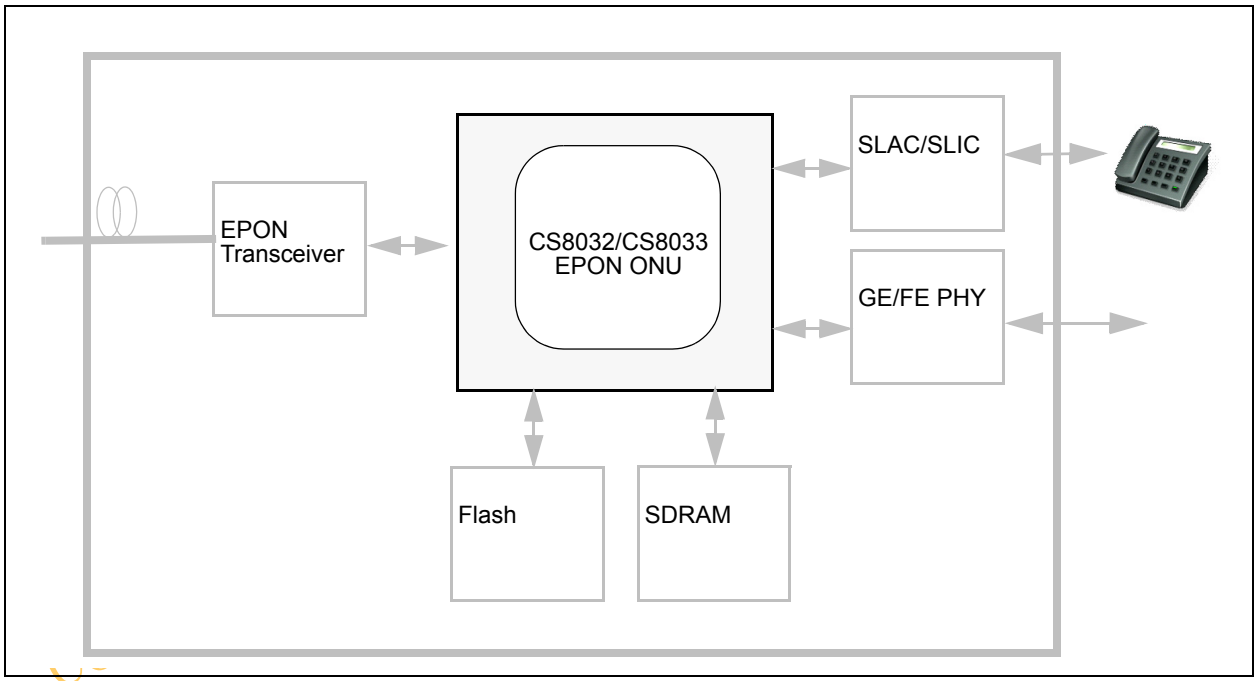
4.0 EPON ONU Applications

The CS8032/CS8033 EPON ONU can be used in various ONU applications. The following sub-sections describe some of those applications.

4.1 POTS Migration Application

In this application the CS8032/CS8033 EPON ONU based ONU is primarily used for migrating POTS (Plain Old Telephone System) to EPON based VoIP networks. Figure 2 illustrates the application. The GE/FE copper connection in the application may or may not be used.

Figure 2 POTS Migration Applications



4.2 SFU Applications

In this application the CS8032/CS8033 EPON ONU-based ONU is primarily for users in a single family and hence is referred to as an Single Family Unit (SFU). The CS8032/CS8033 EPON ONU supports at least five known types of SFUs. Those are referred to as SFU1 (Figure 3), SFU2 (Figure 4), SFU3 (Figure 5), SFU4 (Figure 6), and SFU5 (Figure 7) in this section. SFU2 and SFU3 require external 4-port FE Ethernet switch ASIC from a third party. If the software code and data does not fit into a SiP SDRAM in the CS8032/CS8033 EPON ONU package, then the SDRAM in the illustrations is an external SDRAM connected to the device pins. Otherwise, the SDRAMs in the illustrations are internal SiP SDRAM mounted on the CS8032/CS8033 EPON ONU die.

Figure 3 SFU1 Applications

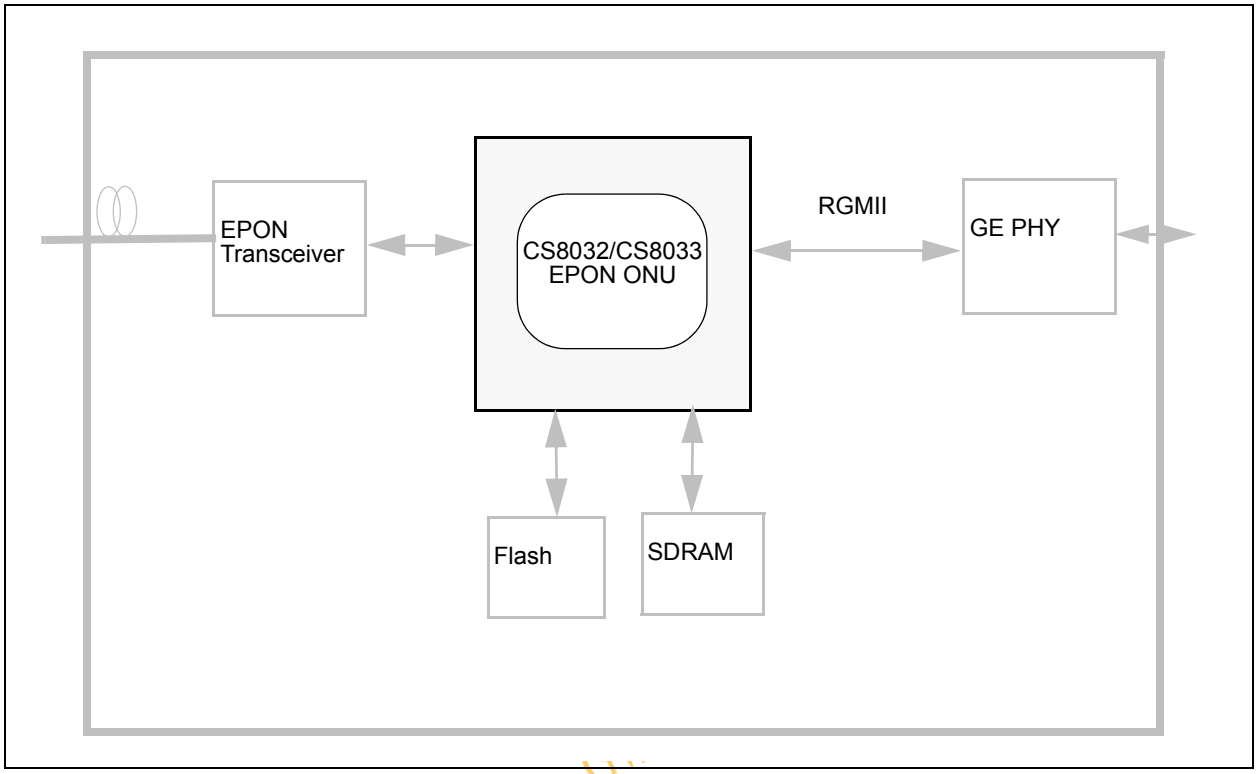


Figure 4 SFU2 Applications

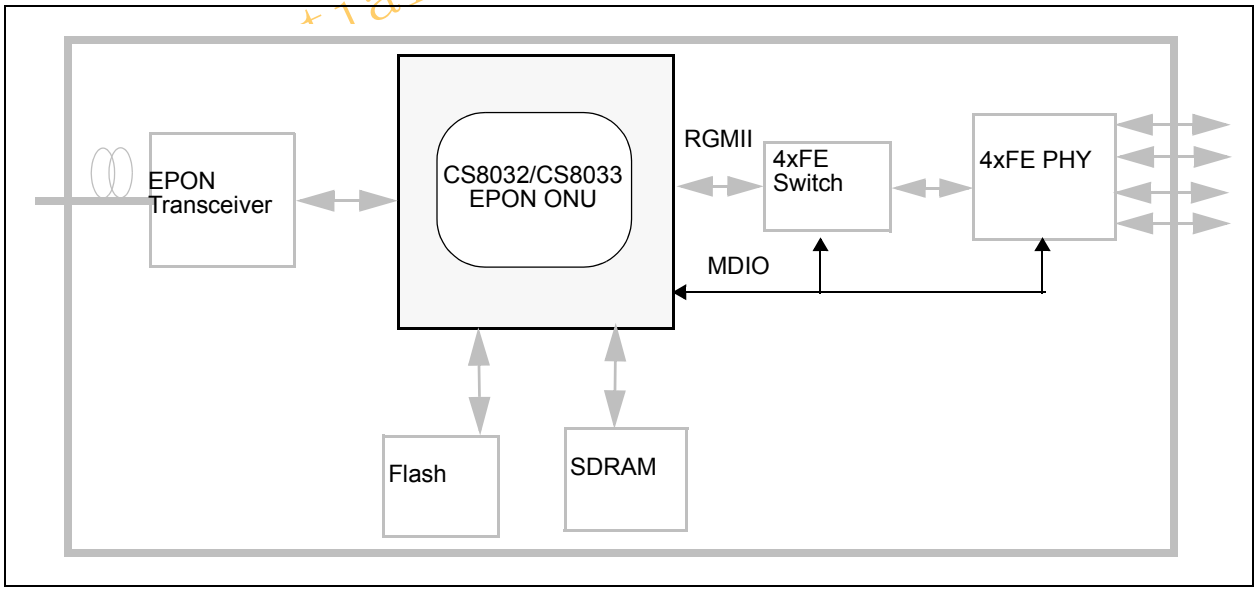


Figure 5 SFU3 Applications

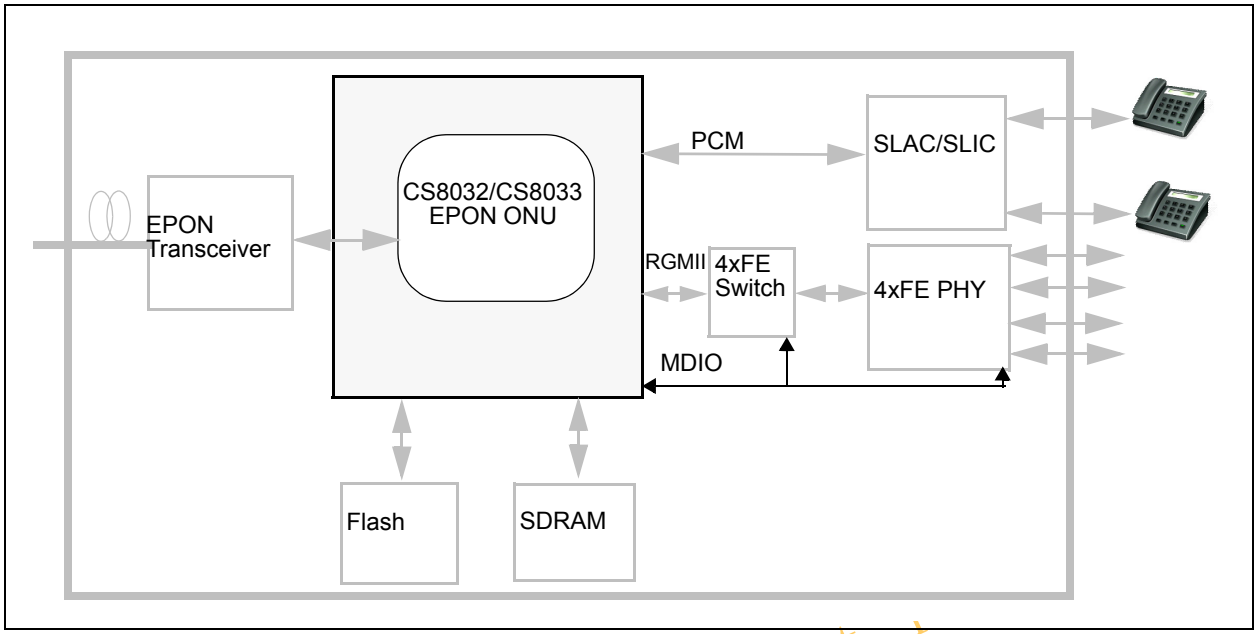


Figure 6 SFU4 Applications

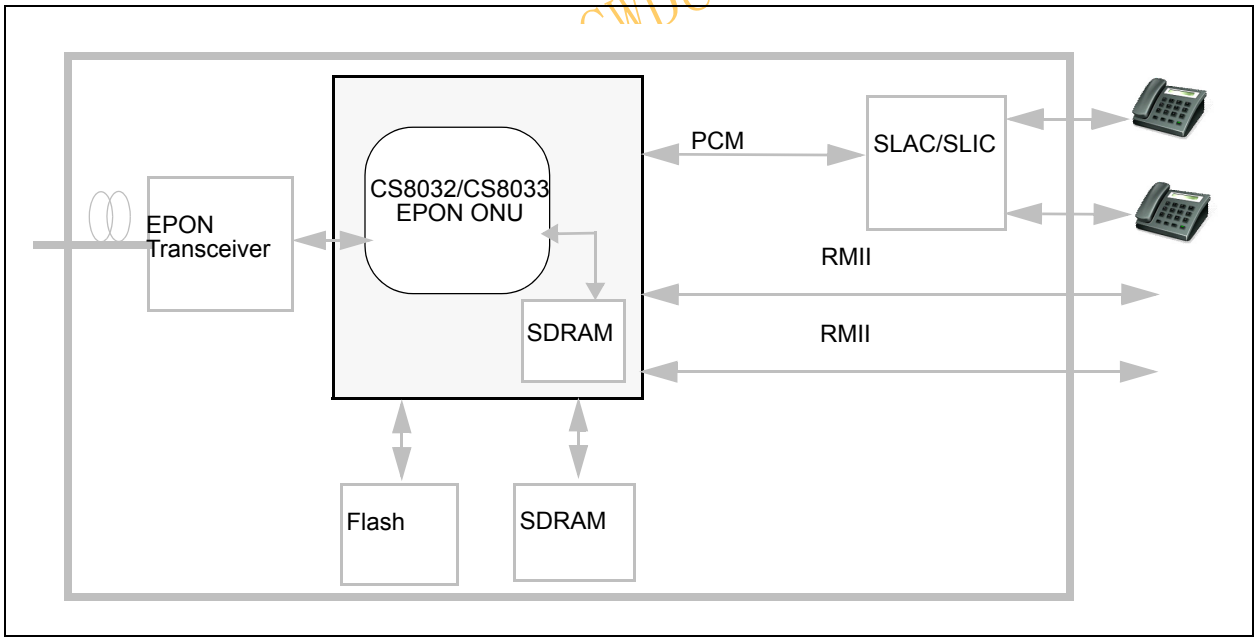
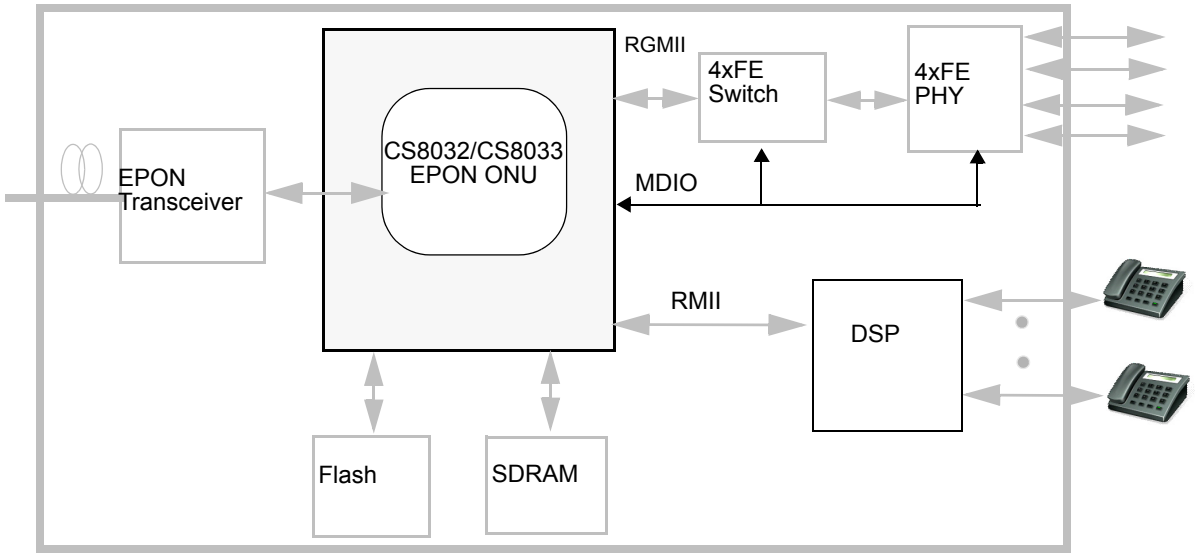


Figure 7 SFU5 Applications

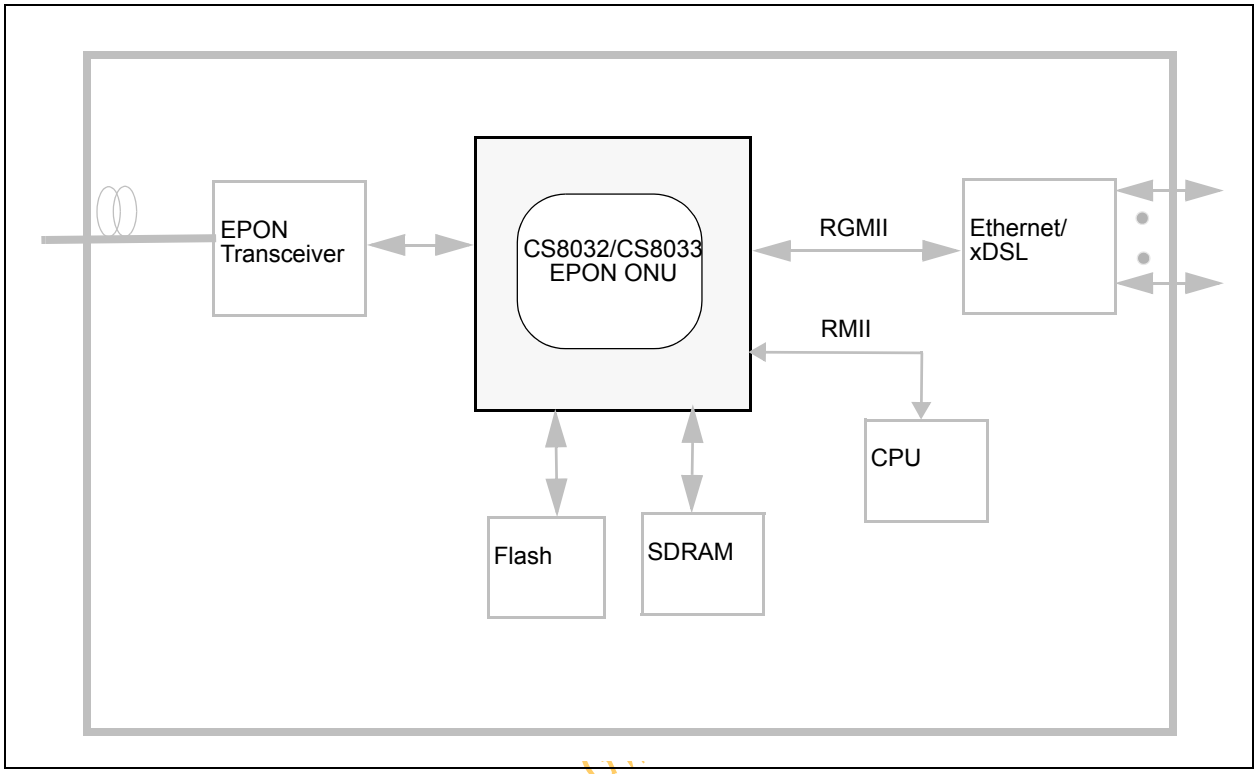


Note: This application illustrates support for two or more voice channels.

4.3 MDU Applications

In this application the CS8032/CS8033 EPON ONU based system is primarily for multiple families or a small business and hence is referred to as an Multi-dwelling Unit (MDU). If the software code and data does not fit into a SiP SDRAM in the CS8032/CS8033 EPON ONU package, then the SDRAM in the illustrations is an external SDRAM connected to the device pins. Otherwise, the SDRAMs in the illustrations are internal SiP SDRAM mounted on the CS8032/CS8033 EPON ONU die. Figure 8 illustrates one MDU application.

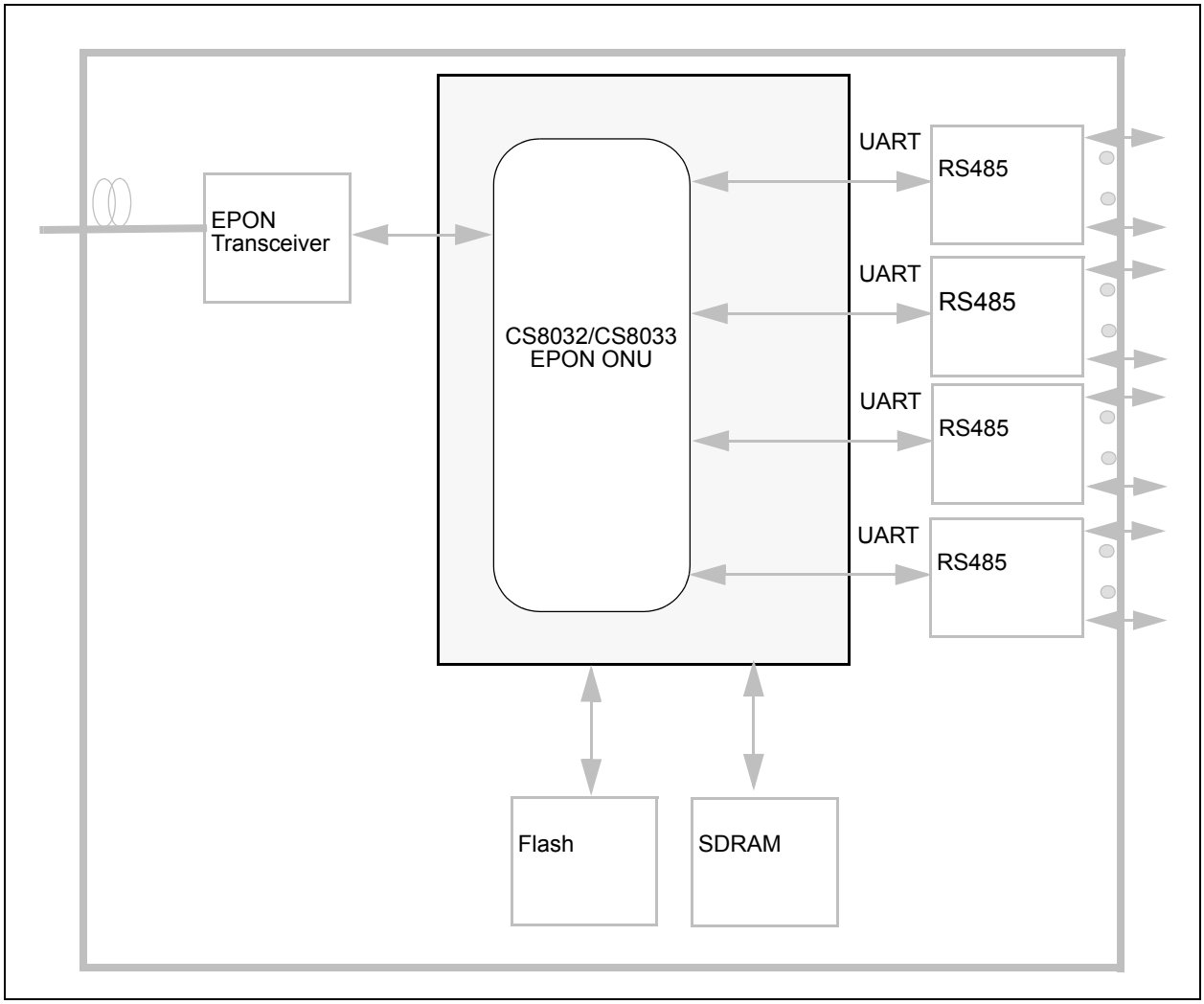
Figure 8 MDU Application



4.4 Power Meter Applications

In this application the CS8032/CS8033 EPON ONU based ONU is primarily for connecting multiple Power meters to the EPON network.

Figure 9 Power Meter Applications



5.0 Feature Highlights

The CS8032/CS8033 EPON ONU is a EPON ONU for data and VoIP applications. It supports one EPON ONU optical transceiver; a UNI Gigabit Ethernet PHY with optional Energy Efficient Ethernet (EEE) support; and a UNI/Management FE port. The UNI Gigabit Ethernet port can be connected directly or can be optionally connected through an external, third-party switch ASIC to Ethernet PHYs. The UNI/Management FE port can support an off-chip VoIP SoC, or other Ethernet enabled devices, or can be used for managing the CS8032/CS8033 EPON ONU. In addition, a standard PCM interface on the CS8032/CS8033 EPON ONU can support POTS (Plain Old Telephone System) through a SLIC device. The CS8032/CS8033 EPON ONU supports either one wide-band or at most two narrowband VoIP phones.

An on-chip SRAM based packet buffer stores packets before forwarding those to destination ports. The CS8032/CS8033 EPON ONU has an embedded ARM926EJ-S* Processor for running software for ONU control; VoIP DSP and SIP (Session Initiation Protocol); or other applications. Software can dynamically configure to run the ARM926EJ-S* Processor at either 500 MHz or 125 MHz depending on application needs. Either a serial or a parallel flash can store software image and can be connected to the CS8032/CS8033 EPON ONU. An optional external SDRAM device or an internal SiP SDRAM die can store program and data for the ARM926EJ-S* Processor. Both IEEE1588 ([5] on page 86) standard and IEEE802.1AS Draft ([6] on page 86) are supported by the CS8032/CS8033 EPON ONU hardware for applications that require precise timing synchronization over EPON. In addition, the CS8032/CS8033 EPON ONU has a dedicated 1PPS+TOD interface compliant with the CTCv2.1 ([7] on page 86) Timing Synchronization standard.

Finally, EEPROM, UART, and I^2C interfaces are provided. The following sub-sections highlight the features of the CS8032/CS8033 EPON ONU.

5.1 EPON Port

The EPON port consists of an embedded EPON SerDes, an EPON MAC, and a proprietary EPON crypto function.

5.1.1 EPON SerDes

An embedded EPON SerDes supports the following features:

- Downstream rate of 1.25 Gbps
- Upstream burst mode rate of 1.25 Gbps
- Diagnostic serial loopback
- Remote and local loopback functions specified in IEEE802.3-2008 Clause 57

5.1.2 EPON MAC

The 1 Gbps EPON MAC embedded in the CS8032/CS8033 EPON ONU is compliant with the IEEE802.3 standard ([2] on page 86) for the EPON interface. It supports the following:

- 1 Gbps full duplex EPON MAC operation:
  - Schedules transmission based on grants
- Standard Ethernet frames
- Timestamping and correction field update at the MAC for software assisted IEEE1588 1-step and 2-step Transparent Clock

- Frame sizes 64-2000 Bytes
- Standard compliant EPON FEC:
  - Corrects up to 8 bytes
  - Monitors number of bits and bytes corrected
  - Supports enabling/disabling FEC feature
- Standard MPCP protocol
  - EPON ONU discovery
  - Ranging and time stamping

5.1.3 EPON Crypto

The CS8032/CS8033 EPON ONU supports 128-bit AES encryption/decryption modes to protect EPON data traffic.

5.2 UNI Port

This UNI port can operate in either RGMII or RMII mode based on the Power-on state of the external pin GTXD_3. An embedded IEEE802.3 standard [2] compliant MAC supports the following:

- MDIO master interface for PHY management
- Triple speed:
  - 1 Gbps/100 Mbps/10 Mbps full-duplex
  - 100 Mbps/10 Mbps half-duplex
- Auto-negotiated or configured speed and duplex modes
- Standard Ethernet frames
- Full Ethernet MIB statistics
- Port based flow control
- Energy Efficient Ethernet IEEE802.3az ([8] on page 86)
- Timestamping and correction field update at the MAC for software assisted IEEE1588 1-step and 2-step Transparent Clock

5.2.1 RGMII Mode

To eliminate the need for a clock driver, the CS8032/CS8033 EPON ONU provides a 25 MHz reference clock output for an external RGMII PHY. It also supports a standard [3] compliant RGMII Interface with 4-bit data on both edges of clock at 2.5 MHz/25 MHz/125 MHz clock rate depending on port speed. On RGMII interface it supports:

- Both half-duplex and full-duplex modes of operations at 10/100 Mbps interface data rate
- Full-duplex mode of operation in 1000 Mbps interface data rate

The speed and duplex modes can be auto-negotiated or configured

5.2.2 RMII Mode

The CS8032/CS8033 EPON ONU provides a 50 MHz reference clock for an external RMII PHY. It also supports a standard [4] compliant RMII Interface with 2-bit data at 50 MHz reference clock rate. On RMII interface it supports both half-duplex and full-duplex modes of operations at 10/100 Mbps data rate. The speed and duplex modes are configured.

5.3 UNI/Management FE Port

The FE UNI/management port can be operated in RMII mode only. The port is primarily meant for one of the following purposes:

- Management of the CS8032/CS8033 EPON ONU
  - Image downloading
- Connecting the CS8032/CS8033 EPON ONU to an external device like a VoIP SoC
- UNI FE port

An embedded IEEE802.3 standard [2] compliant MAC for the UNI interface supports 100 Mbps/10 Mbps full-duplex and full MIB.

The CS8032/CS8033 EPON ONU provides a 50 MHz reference clock for an external RMII PHY. It supports a standard [4] compliant RMII Interface with 2-bit data at 50 MHz reference clock rate. The following features are supported:

- MDIO master interface for PHY management
- Supports:
  - Dual speed (10 Mbps/100 Mbps) full duplex
  - Standard Ethernet frames
  - Full Ethernet MIB statistics
  - Configured speed

5.4 PCM Port

The PCM port can be connected to a SLIC/SLAC device. It supports the following features:

- Hardware PCM framer to:
  - Frame samples received from the PCM interface under software control
  - Create PCM transmit signals from voice frames received from CPU
- Efficient frame movement to and from software
- VoIP processing by the on-chip *ARM926EJ-S* Processor*
- PCM clock frequency can be configured from 256 kHz up to 8192 kHz
- Supports 4 KB (kByte) buffer to store samples for two narrow-band VoIP channels, each with 8 kbps sample rate, or one wide-band VoIP channel with 32 kbps sample rate:
  - Samples received from the SLIC/SLAC by hardware and processed by software to form VoIP packets
  - VoIP packets processed by software and samples are transmitted by hardware to the SLIC/SLAC

5.5 Forwarding Engine

The hardware Forwarding Engine in the CS8032/CS8033 EPON ONU performs various table lookups and makes packet forwarding decisions at line rate. The packets are parsed and the fields from the packet header are extracted. Based on these the destination port, class of service and VLAN processing is determined.

5.5.1 Packet Parsing

The Packet Parsing hardware function extracts the following fields from the packet that are used for other hardware functions like Classification, L2 Processing in the CS8032/CS8033 EPON ONU:

- MAC DA
- MAC SA
- Ethernet Type/Length
- VLAN Tag1
- VLAN Tag2
- IPv4/IPv6 Header:
  - Protocol
  - DSCP
  - IP DA
  - IP SA
  - IP TOS/DSCP
- TCP/UDP Source and Destination Port and Flags
- IGMP, ICMP, and MLD types

5.5.2 L2 Processing

The L2 MAC SA learning and MAC DA lookup hardware function is common for all ports: EPON, GE UNI, and FE. Total of 64 L2 entries are supported and used for MAC SA learning as well as MAC DA forwarding for EPON, UNI GE, and the FE port. The hardware function has the following features:

- L2 MAC DA lookup
- MAC address filtering (MAC, or MAC+VLAN)
- Optional dropping of packets with unknown L2 DA
- Configured static entries
- Aging under hardware or software control
- Limiting maximum number of entries learned from each port
- Multicast DA lookup
- Least Recently Used (LRU) algorithm to replace entries when a newly learned source address exceeds source address learning limit

5.5.3 Packet Classification

The CS8032/CS8033 EPON ONU supports a separate Classification Engine for EPON, GE, and UNI/Management ports. Each engine supports:

- 48 separate L2/L3 Classification entries with TCP/UDP port range support for each of downstream and upstream and 16 entries for the UNI/Management port
  - Highest precedence match
  - IPv4/IPv6 Protocol type, IPv4/IPv6 addresses, TCP/UDP source port, destination port, port ranges, VLAN ranges, outer and inner VLAN as fields of the key
  - Results of this block may include permit/deny, connection id for policing, CoS, VLAN push/pop/swap commands

5.5.4 Filtering or VLAN Translation

The CS8032/CS8033 EPON ONU supports many VLAN filtering or translation operations. It supports:

- One 32-entry VLAN table to perform one or more of the following operations:
  - Ingress VLAN translation:
    - Optional Ingress VLAN translation before Packet Classification (Section 5.5.3)
  - Ingress/Egress VLAN membership check:
    - Permit/deny packets to a VLAN after Packet Classification and VLAN Operations (Section 5.5.3)
  - Egress VLAN translation:
    - Optional Egress VLAN translation after Packet Classification and VLAN Operations (Section 5.5.3)
- VLAN TPID filtering
  - Drop packets if configured TPID matches

5.6 Buffer Manager

The Buffer Manager manages the Frame Buffer that stores incoming packets before those are forwarded to respective destinations. It supports:

- A queue manager (Section 5.6.1) to split available Frame Buffer memory into multiple queues
- Three separate traffic scheduler (Section 5.6.2)

5.6.1 Queue Manager

- CS8016 Mode: 768 kB of internal SRAM for packet buffering for upstream and downstream:
  - Dynamic packet buffers allocated
  - Packets in lower priority queues optionally removed to store high priority packets in the event of buffer congestion
  - Per port and shared buffers dynamically split into:
    - 8 queues for upstream traffic
    - 8 queues for downstream traffic
    - 8 queues for CPU and the UNI/Management FE ports

– 9th. queue for OAM traffic from CPU

5.6.2 Traffic Scheduler

- CS8016 Mode: Three separate scheduler and a TDM scheme chooses one of those three:
  - One TDM based scheduler for each of the following:
    - EPON port
    - UNI GE port, and
    - MA port that is a combination of two other packet destinations: CPU and UNI/Management FE port
  - Nine VOQs for each of the three scheduler: Flexible assignment of nine shared VOQs to the ports and support for the following:
    - 8 priorities
    - SP, DRR, SP+DRR supported for the EPON and GE scheduler
    - SP supported for the MA scheduler

5.7 Rate Limiters

A rate limiter admits traffic below a configured PIR and denies all packets above the PIR. It also can limit the burst size to a configured value.

- 32 individual flow based single token bucket rate limiter (PIR) and four aggregate rate limiters for data or control traffic
  - 0-1 Gbps PIR range with 100 kbps resolution in the whole range
  - 0-1 MB burst size in 1 kB units

  A packet can be associated to one of the 8 flows based by the Classification Engine. Any one or more of those flows can also be configured to be rate limited by the aggregate flow rate limiters.
- Three single token bucket (PIR): one for the UNI port and one for PON and the third one for the UNI/Management port:
- Three single token bucket rate limiters (PIR) for storm control for each one of the source ports for the following types or a flexible combination of the following types of traffic:
  - Known and unknown unicast
  - Known and unknown multicast
  - Broadcast
- One single token bucket rate limiter (PIR) to limit total traffic to the CPU

5.8 ARM926EJ-S* Processor

The CS8032/CS8033 EPON ONU has an embedded ARM926EJ-S* 32-bit RISC Processor with 16k instruction cache and 16k data cache:

- 1 dedicated UART interface for easy access Baud rate can be configured to support 300, 600, 1200, 2400, 9600, 19200, 38400, 115K and 192K baud rates
- 4 optional multi-drop UART interfaces for power grid support:
  - Pins shared with GPIO, PCM, and 1PPS+TOD

- 5 timers
- SPI controller for external EEPROM, serial flash and SLAC devices
- Built-in RX/TX SRAM frame buffers for frame transfer to/from the ARM926EJ-S* Processor
- 16 GPIOs
- I^2C interface
- MDIO interface for controlling external PHY
- JTAG I/F for Software debugging
- An SDRAM controller to access one of the following SDRAM devices to store instruction and data when the processor is running:
  - An external 125 MHz SDRAM device with at most 32 MB capacity
    - Accessible through the Local Bus pins (Section 6.8.2, *External Memory*, on page 44) or
  - An internal 2 MB or 8 MB SiP SDRAM die
    - Mounted on top of the CS8032/CS8033 EPON ONU die in the CS8032/CS8033 EPON ONU package
- A programmable 32 bit Watchdog timer provides interrupt or reset to CPU subsystem

5.9 Timing Synchronization

- Supports the following Timing Synchronization schemes:
  - IEEE1588 ([5] on page 86) Transparent Clock support with hardware assist for accurate timestamping of SYNC packets
  - CTC2.1 ([7] on page 86) 1PPS+TOD support
  - IEEE802.1as Clause 13 ([6] on page 86) EPON TOD support

5.10 Power Saving Mode

- Supports the following power saving schemes on UNI port:
  - IEEE 802.3az Energy Efficient Ethernet signaling on UNI port
  - Special Buffer management scheme to manage traffic through EEE enabled UNI port
- Supports optical power saving scheme in either OLT initiation or ONU initiation modes, refer to IEEE P1904.1 SIEPON specification
- Supports automatic power saving scheme with DBA grant monitoring

6.0 Pin Descriptions

The CS8032/CS8033 EPON ONU is housed in a 225-pin TFBGA package. The package is described in Section 8.0, *Package Specification*. The following sub-sections describe various functional interfaces and lists signal, power, and ground balls of the CS8032/CS8033 EPON ONU.

All the CS8032/CS8033 EPON ONU differential pair signals must be AC coupled unless DC coupling is specified as an option for any specific pair. In addition, polarities of all differential pair signals can be swapped based on configured register settings in order to avoid swapping signal traces in the pair.

In the CS8032/CS8033 EPON ONU, all LVTTL output pins are driven by 8 mA drivers except for the LED drivers that can source and sink 12 mA current (Section 6.2.1).

6.1 System Clock and Reset

There are 1 main clock sources in the system which is a 25 MHz LVTTL oscillator that provides the main clock to run the CS8032/CS8033 EPON ONU and external components like PHYs (Figure 10).

Table 1 System Controls (Sheet 1 of 2)

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
RESETN	P2	—	INPUT LVTTL	Active low hardware chip reset
TEST_MODE	L4	—	INPUT	This pin selects a special test mode. It should be 0 in normal functional mode.
JTAG_MODE	N3	—	INPUT	This pin selects one of the two tap controllers in the CS8032/CS8033 EPON ONU to be connected to the JTAG Controller pins (Table 19 on page 51) 0 = Selects the internal tap controller for production test purposes only 1 = Selects the ARM926EJ-S* Processor tap controller
PLL_LOCK	N4	—	DC Output LVTTL 2 mA	
EXT_CLOCK_SEL	N5	—	INPUT	This pin selects if the source of the core and ARM926EJ-S* Processor clock: 0 = Use PLL's output as ARM/AHB/core clock 1 = Use external clock pad EXT_CLOCK as ARM/AHB/core clock There is an additional strapping option to select one of two possible frequencies for the ARM926EJ-S* Processor when PLL is selected as the ARM/AHB/core clock. Refer to Section 6.16, *Mode Selection*, on page 52 for more details on external strapping options. A a glitch-free clock multiplexer is used for selecting one of the two clock frequencies. The strapping option can be changed dynamically by software.

Table 1 System Controls (Sheet 2 of 2)

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
EXT_CLOCK	P3	75 MHz- 25 MHz	INPUT	External clock source when the EXT_CLOCK_SEL is pin is high
CPLL_REFCLK_P CPLL_REFCLK_N	R10 P10	25 MHz ±50 PPM	INPUT LVTTL	25 MHz differential clock input that is multiplied by the internal PLL to generate: • 125 MHz core clock • independent ARM926EJ-S* Processor clock selected in the range of 125 MHz-500 MHz • 50 MHz RGMII PHY reference clocks • 50 MHz RMII PHY Reference clocks To use a signal-ended clock source, connect the clock source to CPLL_REFCLK_P and pull down CPLL_REFCLK_N through a capacitor. (See Figure 10.)
SYNC_CLKO	R3	8 kHz- 125 MHz	OUTPUT LVTTL 4 mA	The output clock is derived either from the clock recovered from EPON receive data or the PLL output clock. The output clock can be used in a system that requires some device to run synchronously on the clock from OLT. This ball should be unconnected: • if synchronous Ethernet functionality is not required or • if this clock is not the preferred clock source in a synchronous Ethernet application The frequency of the clock output is determined by the configured value of an internal register. The recovered 125 MHz EPON clock is divided by a factor determined by the value in that register.

Figure 10 Single-Ended Clock Connections

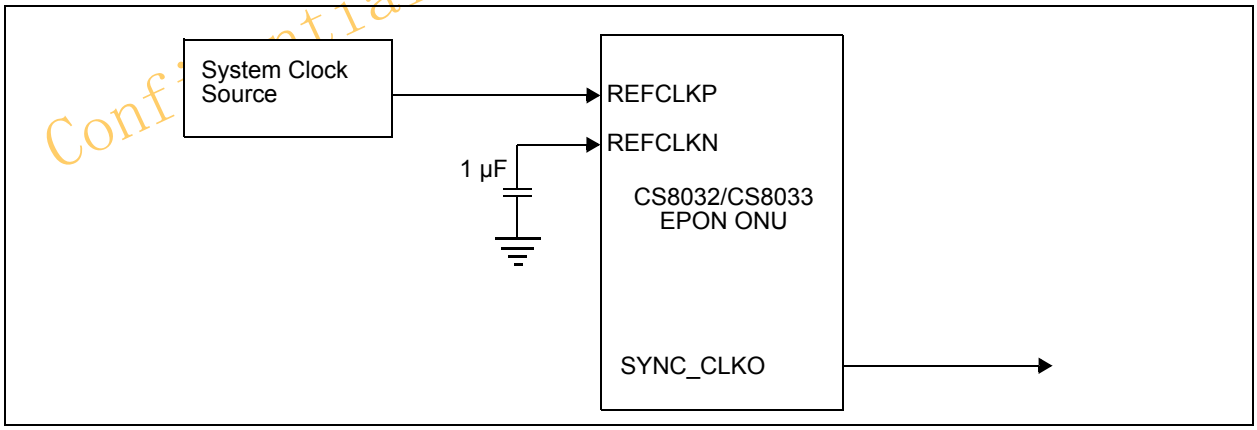
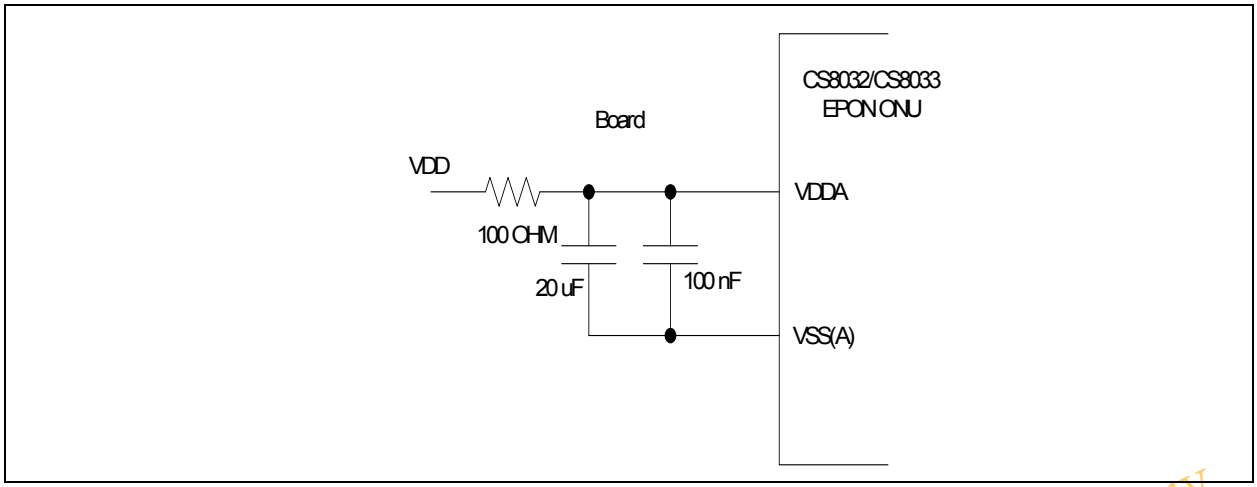


Figure 11 System PLL Input (Clock Reference is Provided Internally)



6.2 GPIOs

The CS8032/CS8033 EPON ONU supports several GPIOs that can be used for many different applications. If enabled, a GPIO can interrupt the Control CPU. In addition, the value on GPIOs can be read by the Control CPU. The GPIOs are described in Table 2.

Table 2 GPIOs

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
GPIO_15 GPIO_14 GPIO_13 GPIO_12 GPIO_11 GPIO_10 GPIO_09 GPIO_08 GPIO_07 GPIO_06 GPIO_05 GPIO_04 GPIO_03 GPIO_02 GPIO_01 GPIO_00	F1 C2 D2 E2 F2 C1 G3 F3 M3 L3 K3 J3 H3 E1 D1 B3	10 MHz	INPUT/OUTPUT LVTTL[1]	**General Purpose I/Os** Any GPIO can be sampled or driven by the on-chip CPU for any purpose including driving an LED. GPIO_[15:10] can be optionally configured by software to be driven by the dedicated on-chip special LED hardware. The LED hardware can be configured to drive at most six single-color or a mix of bi-color and single color LEDs. Refer to Section 6.2.1, *LED Interface*, on page 32 for more details on the signals and modes when one or more of the GPIO_[15:10] pins are configured as LED interface. If CS8032/CS8033 EPON ONU supports power measurement, GPIO_09 is used as RSSI to the transceiver.

Note:
1. GPIO_15-GPIO_10 are 12 mA drivers
   GPIO_09-GPIO_00 are 4 mA drivers

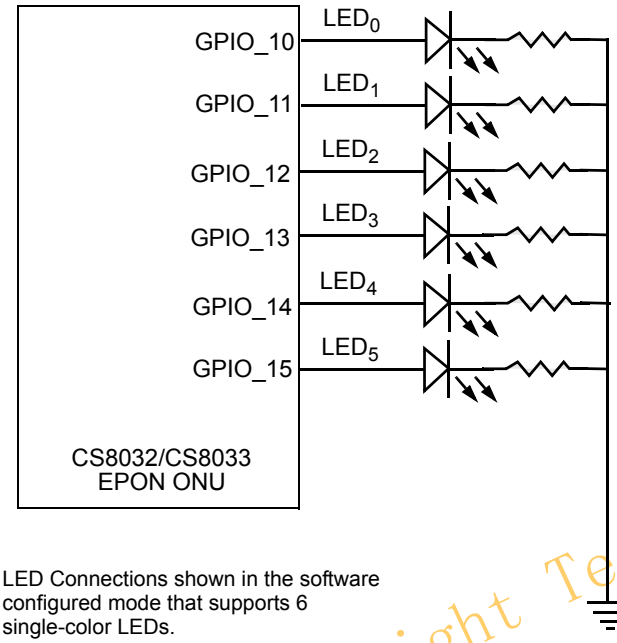
6.2.1 LED Interface

A dedicated LED hardware can drive an LED interface consisting of one or more of the GPIO_[15:10] signals. Software must configure each GPIO_[15:10] pin to be part of the LED interface for the dedicated LED hardware to drive those pins. At most 6 LED signals can be driven by the ASIC. Table 3 describes various LED modes, the functions of the LED pins are driven in those modes, and the mapping between GPIO pins and LED pins. Figure 12 illustrates LED connections. The drivers on GPIO_[15:10] pins can source and sink 12 mA of current. Hence, in most cases, LEDs may be driven directly without any external component.

Table 3 LED Interface Definition

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
LED_5 LED_4 LED_3 LED_2 LED_1 LED_0	See Table 2	≤ 20 Hz	OUTPUT LVTTL[1]	The LEDs are driven with the following GPIO balls: GPIO_15 = LED_5 GPIO_14 = LED_4 GPIO_13 = LED_3 GPIO_12 = LED_2 GPIO_11 = LED_1 GPIO_10 = LED_0 LED signals that can be configured by software in one of the following modes: • 3 bi-color LEDs • 2 bi-color and 2 single-color LEDs • 1 bi-color and 4 single-color LEDs • 6 single-color LEDs In each mode an LED can be configured to be turned on, off, or blink independent of any other LED.
Note: 1. GPIO_15-GPIO_10 are 12 mA drivers GPIO_09-GPIO_00 are 4 mA drivers				

Figure 12 LED Connections



Note: LED Connections shown in the software configured mode that supports 6 single-color LEDs.

6.3 EPON ONU Interface

The CS8032/CS8033 EPON ONU has an embedded EPON ONU burst mode SerDes that can be connected to an external EPON optical transceiver.

If the EPON ONU transceiver is capable of power measurement, the CS8032/CS8033 EPON ONU can trigger the feature on its RSSI signal of the transceiver directly and read out the measured power using the I^2C (Section 6.9) interface.

An energy efficient EPON ONU or MDU requires that the transmit and receive power of the Optical ONU transceiver can be independently controlled. The CS8032/CS8033 EPON ONU has integrated hardware functions that monitor traffic and can perform one or both the following functions:

- Optionally control the transmit power of the optical transceiver through GPIO6
- Optionally control the receive power of the optical transceiver through GPIO4

Refer to Figure 13 on page 35 for an illustration of an energy efficient EPON system.

6.3.1 EPON Receive (ERX) Interface

Table 4 EPON Receive Signals

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
ERX_P ERX_N	R8 P8	1.25 Gbps	INPUT CML	EPON Serial data input with 100 Ω differential termination

6.3.2 EPON Transmit (ETX) Interface

Table 5 EPON Transmit Signals

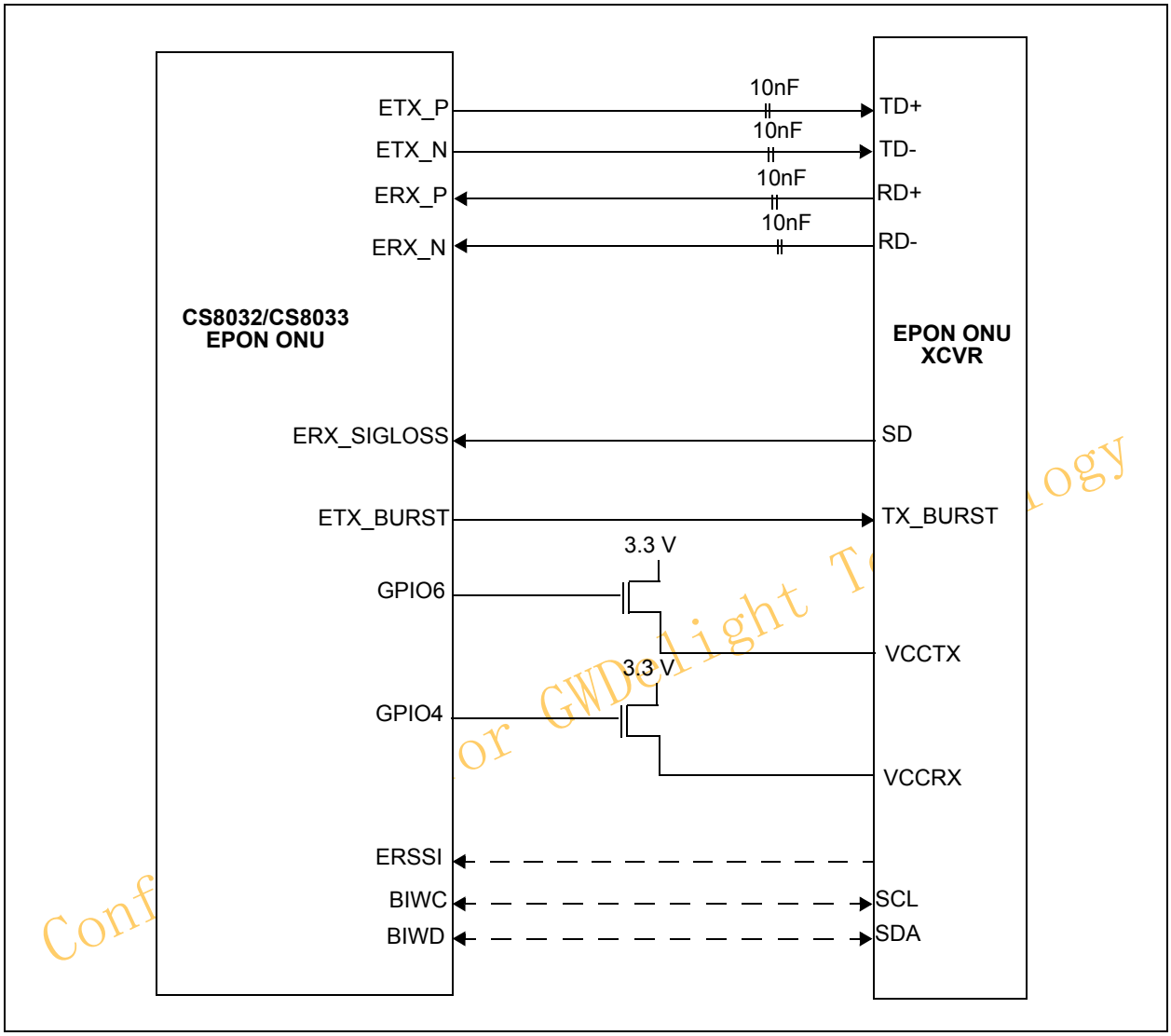
Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
ETX_P ETX_N	R6 P6	1.25 Gbps	OUTPUT CML	EPON Serial data output

6.3.3 EPON Optical Interface Control and Status

Table 6 EPON Optical Interface Control and Status

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
ETX_BURST	R2	1	OUTPUT LVTTL 4 mA	Active High PON Port Optical Transceiver Tx Burst.
ERX_SIGLOSS	R12	1	INPUT LVTTL 2 mA	PON port Loss Of Signal.

Figure 13 EPON ONU Connections



6.4 UNI GE Interface

The CS8032/CS8033 EPON ONU has one IEEE802.3-2008 compliant Gigabit Ethernet MAC primarily meant for network traffic. It supports:

- 10/100 Mbps half- and full-duplex operation
- 1 Gbps full-duplex operation
- MII/RGMII interfaces for copper PHY or SerDes

Section 6.4.1 and Section 6.4.2 describe the MII/RGMII receive and transmit signals, respectively. Figure 14 and Figure 15 illustrate connections from the CS8032/CS8033 EPON ONU to RGMII and RMII PHYs, respectively.

6.4.1 RGMII/RMII Receive Interface

Table 7 RGMII/RMII Receive Signals

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
GRXCLK	J1	2.5 MHz/ 25 MHz/ 125 MHz	INPUT LVTTL	RGMII/RMII UNI port receive clock **RMII mode**: • Not used in RMII mode **RGMII mode:** • 2.5 MHz receive clock in 10 Mbps mode • 25 MHz receive clock in 100 Mbps mode • 125 MHz receive clock in 1 Gbps mode

GRXD_3
GRXD_2
GRXD_1
GRXD_0
	H2
	J2
	K2
	L2
		5 Mbps/ 50 Mbps/ 250 Mbps	INPUT LVTTL	RMII/RGMII UNI port receive data
				RMII mode:
				• GRXD[3:2]: Not Used
				• GRXD[1:0]: receive data from RMII PHY
				RGMII mode:
				• GRXD[3:0]:
				  • receive data bits 3:0 on rising edge of GRXCLK
				  • receive data bits 7:4 on falling edge of GRXCLK

GRXCTL	K1	5 Mbps/ 50 Mbps/ 250 Mbps	INPUT LVTTL	RGMII/RMII UNI port receive control/data **RMII mode**: • RMII CRS_DV **RGMII mode:** • RXDV rising edge of GRXCLK • RXER on falling edge of GRXCLK
GPHY_INTR	R1		INPUT LVTTL	RGMII/RMII UNI PHY event interrupt

6.4.2 RGMII/RMII Transmit Interface

Table 8 RGMII/RMII Transmit Signals (Sheet 1 of 2)

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
GREFCLK	H1	25 MHz/ 50 MHz	OUTPUT LVTTL 8 mA	RMII/RGMII PHY Reference clock driven by the CS8032/CS8033 EPON ONU to eliminate clock distribution device and reduce system cost **RMII mode**: • 50 MHz Reference clock from the CS8032/CS8033 EPON ONU to a RMII PHY in both 10 Mbps and 100 Mbps modes **RGMII mode:** • 25 MHz reference clock from the CS8032/CS8033 EPON ONU to an RGMII PHY

Table 8 RGMII/RMII Transmit Signals (Sheet 2 of 2)

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
GTXCLK	M1	50 MHz/ 2.5 MHz/ 25 MHz/ 125 MHz	OUTPUT LVTTL 8 mA	RGMII UNI PHY transmit clock **RMII mode**: • Not used **RGMII mode:** • 2.5 MHz transmit clock in 10 Mbps mode • 25 MHz transmit clock in 100 Mbps mode • 125 MHz transmit clock in 1 Gbps mode

GTXD_3
GTXD_2
GTXD_1
GTXD_0
	M2
	N1
	N2
	P1
		5 Mbps/ 50 Mbps/ 250 Mbps	OUTPUT LVTTL 8 mA	RMII/RGMII UNI port transmit data
				RMII mode:
				• GTXD[3:2]: Not used
				• GTXD[1:0]: Transmit data from the CS8032/CS8033 EPON ONU
				RGMII mode:
				• GTXD[3:0]:
				  • transmit data bits 3:0 on rising edge of GTXCLK
				  • transmit data bits 7:4 on falling edge of GTXCLK

GTXCTL	L1	5 Mbps/ 50 Mbps/ 250 Mbps	OUTPUT LVTTL 8 mA	RMII/RGMII UNI PHY transmit control
				RMII mode:
				• RMII TX_EN
				RGMII mode:
				• GTXCTL
				  • TXEN rising edge of GRXCLK
				  • TXER on falling edge of GRXCLK

Figure 14 UNI GE (RGMII) PHY Connections

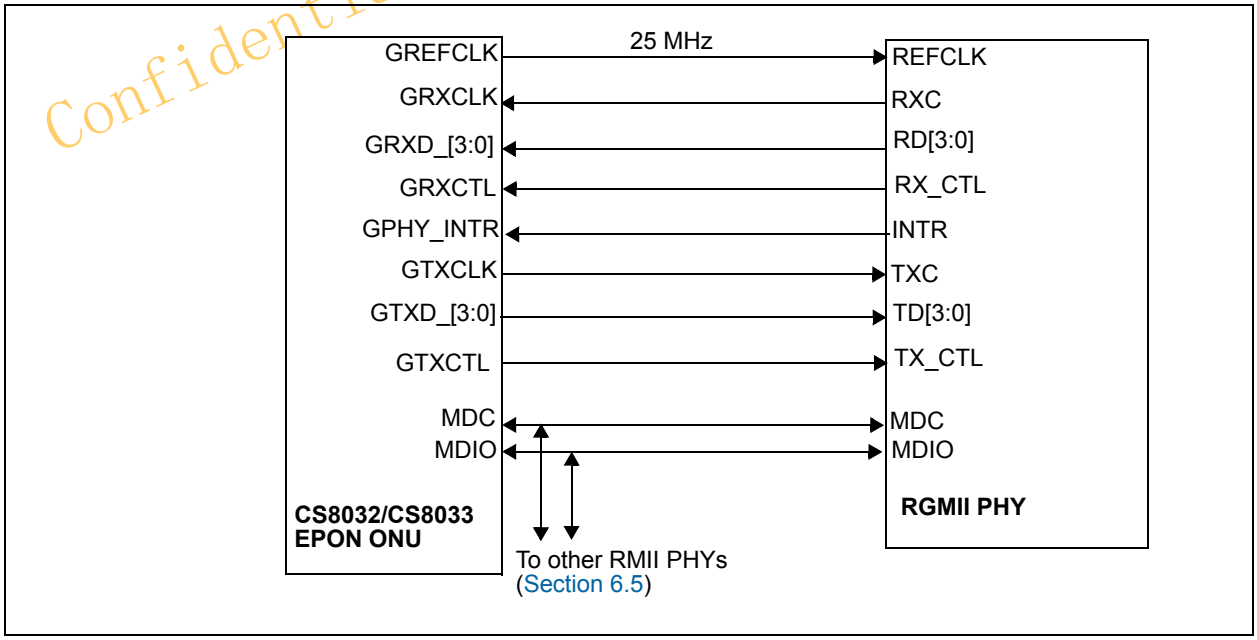
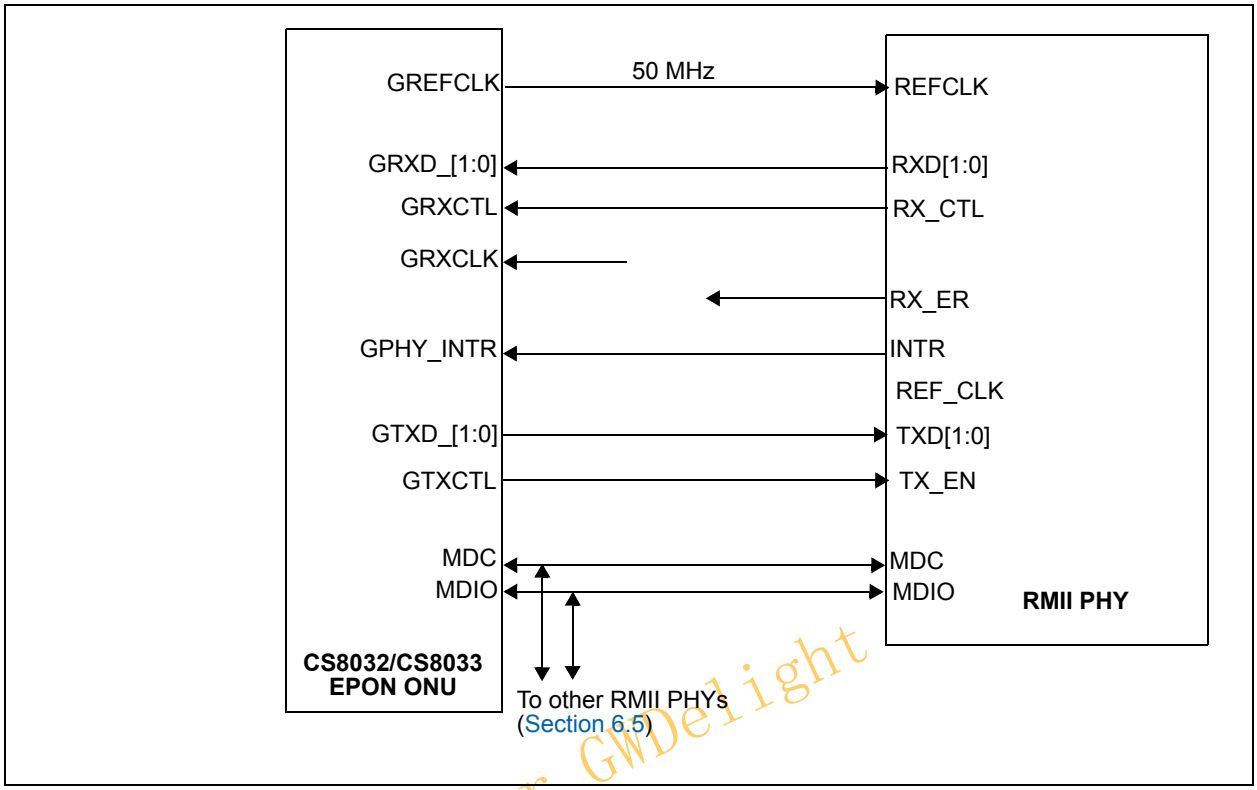


Figure 15 RMII PHY Connections



6.5 Management/VoIP Interface

The CS8032/CS8033 EPON ONU has a separate 10/100 Mbps full-duplex Ethernet MAC for either management or for connecting a VoIP SoC. As a management port it can be used for image download or for debug purposes. As a VoIP port, it may be connected to a VoIP device that supports fast ethernet interface for VoIP packet transmit and receive. Section 6.5.1 and Section 6.5.2 describe the Management RMII receive and transmit signals, respectively. Figure 16 illustrate connections from the CS8032/CS8033 EPON ONU to an RMII PHY.

6.5.1 RMII Receive Interface

Table 9 RMII Receive Signals

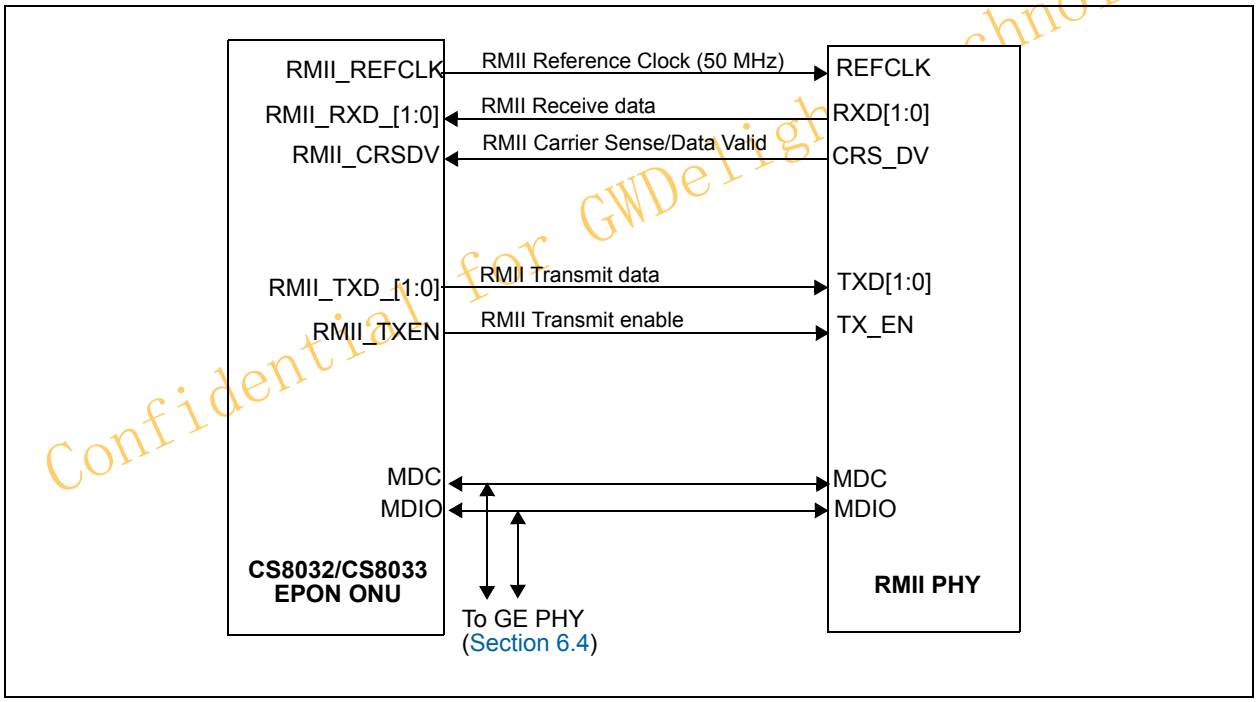
Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
RMII_RXD_1 RMII_RXD_0	A9 A8	50 Mbps	INPUT LVTTL	RMII Management/VoIP port receive data signals.
RMII_RXDV	A7	—	INPUT LVTTL	RMII Management/VoIP port Carrier Sense/Receive Data Valid

6.5.2 RMII Transmit Interface

Table 10 RMII Transmit Signals

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
RMII_REFCLK	B9	50 MHz	OUTPUT LVTTL 8 mA	RMII Management/VoIP PHY reference clock from the CS8032/CS8033 EPON ONU to the RMII PHY
RMII_TXD_1 RMII_TXD_0	B8 B7	50 Mbps	OUTPUT LVTTL 4 mA	RMII Management/VoIP port transmit data.
RMII_TXEN	A6	—	OUTPUT LVTTL 4 mA	RMII Management/VoIP PHY transmit enable

Figure 16 Management/VoIP (RMII) Port Connection



6.6 PHY Management (MDIO) Interface

Table 11 PHY Management Signals

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
MDC	P13	1.25 M	OUTPUT/ LVTTL 4 mA	PHY Management interface clock
MDIO	R13	1.25 M	INPUT/ OUTPUT LVTTL 4 mA	PHY Management interface data synchronized with MDC

6.7 Serial (SSP) Interface

The serial interface in the CS8032/CS8033 EPON ONU is powered by a special 3.3 V power supply. It may be connected to a 3.3 V serial EEPROM and/or a 3.3 V serial flash. The serial EEPROM can store configurations and the serial flash can store Control CPU image. If an application requires running the CPU image from a flash, a parallel flash may be used (Section 6.8.1) instead of the serial flash. Table 12 describes the interface signals for EEPROM and Serial Flash. Three separate chip selects are available for 3 devices to share the serial interface. If VoIP is supported through the SLAC/SLIC device, it is also connected through this serial interface, in addition to the PCM interface. Section 6.7.1 describes Serial Flash and Section 6.7.2 EEPROM.connections to the CS8032/CS8033 EPON ONU.

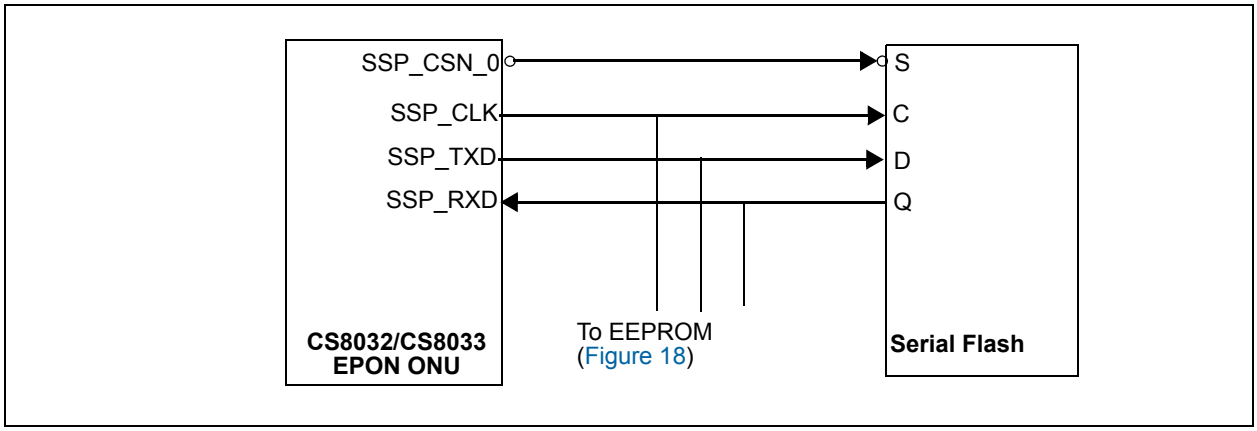
Table 12 EEPROM Signals

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
SSP_CSN_2 SSP_CSN_1 SSP_CSN_0	A1 A2 B1	25 M	OUTPUT 3.3 V 8 mA	Serial interface Chip Selects - one for each serial device
SSP_RXD	A3	25 M	INPUT 3.3 V 2 mA	Serial data in
SSP_TXD	B2	25 M	OUTPUT 3.3 V 8 mA	Serial data out.
SSP_CLK	A4	50 Mhz	OUTPUT 3.3 V 8 mA	Serial clock.

6.7.1 Serial Flash

A Serial Flash can be used to store software image for the embedded ARM926EJ-S* Processor. One of the serial bus select pins is dedicated for the serial flash. The serial flash shares the serial bus with the EEPROM (Section 6.7.2).

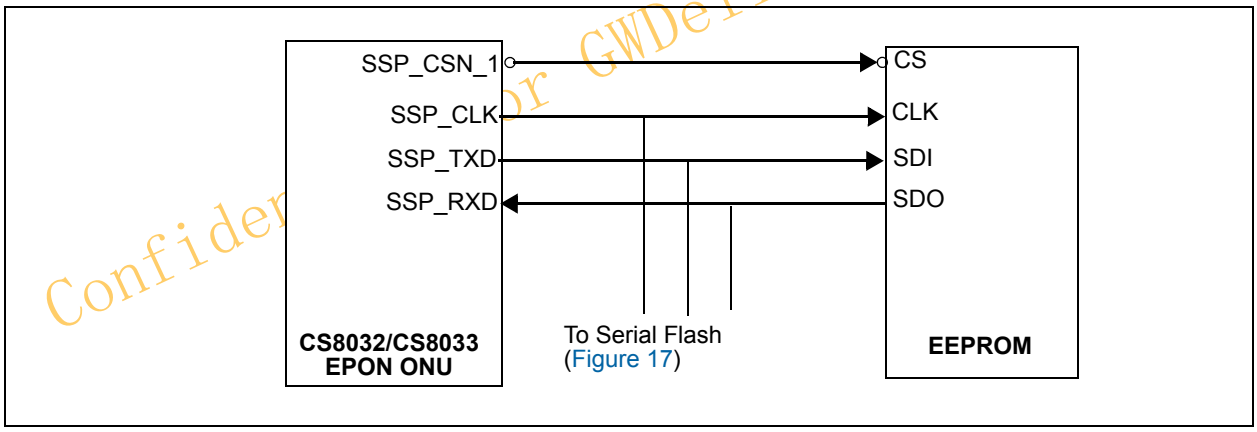
Figure 17 Serial Flash Connections



6.7.2 EEPROM

The EEPROM can contain the configuration information including modes set by the various mode pins (Section 6.16) of the CS8032/CS8033 EPON ONU. One of the serial bus select pins is dedicated for the EEPROM. The EEPROM shares the serial bus with the Serial Flash (Section 6.7.1).

Figure 18 EEPROM Connections



6.8 Local Bus Connections

The local bus can be connected to different devices. Table 13 describes the Local Bus signals. The following sub-sections describe various devices that can be connected to the CS8032/CS8033 EPON ONU on the Local Bus.

Table 13 Local Bus Signals (Sheet 1 of 2)

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
LPB_ADDR_25 LPB_ADDR_24 LPB_ADDR_23 LPB_ADDR_22 LPB_ADDR_21 LPB_ADDR_20 LPB_ADDR_19 LPB_ADDR_18 LPB_ADDR_17 LPB_ADDR_16 LPB_ADDR_15 LPB_ADDR_14 LPB_ADDR_13 LPB_ADDR_12 LPB_ADDR_11 LPB_ADDR_10 LPB_ADDR_09 LPB_ADDR_08 LPB_ADDR_07 LPB_ADDR_06 LPB_ADDR_05 LPB_ADDR_04 LPB_ADDR_03 LPB_ADDR_02 LPB_ADDR_01 LPB_ADDR_00	F13 E13 C13 D13 E14 C12 C14 E15 C11 C15 D14 C10 B15 D15 C9 B14 A14 C8 B13 A15 C7 A13 C6 C5 C4 C3	62.5 MHz	OUTPUT LVTTL 8 mA	Output: FLASH or SDRAM address/control bus FLASH/SRAM Address Bus. The internal control CPU drives this bus. This bus should be connected directly to the address bus input of a parallel flash. This bus should be connected in the following ways to an external SDRAM Address Bus and control signals: • Bits [25:24] can be connected to the Bank Address BA[1:0] inputs of an SDRAM • Bit [23] can be connected to the $\overline{\text{RAS}}$ pin of an SDRAM • Bit [22] can be connected to the $\overline{\text{CAS}}$ pin of an SDRAM • Bit [21:20]: SDRAM Data Mask $\overline{\text{DM}}$[1:0] of a 16-bit wide SDRAM. • Bits [12:0] can be used as the row/column address A[12:0] of an SDRAM
LPB_XDATA_15 LPB_XDATA_14 LPB_XDATA_13 LPB_XDATA_12 LPB_XDATA_11 LPB_XDATA_10 LPB_XDATA_09 LPB_XDATA_08 LPB_XDATA_07 LPB_XDATA_06 LPB_XDATA_05 LPB_XDATA_04 LPB_XDATA_03 LPB_XDATA_02 LPB_XDATA_01 LPB_XDATA_00	J13 H13 G13 J15 H15 H14 M15 L15 K15 N14 M14 L14 F14 F15 J14 K14	62.5 MHz	INPUT/ OUTPUT LVTTL 8 mA	FLASH/SDRAM Data bus. Either internal control CPU or a Flash/SDRAM drives this bus. This bus should be connected directly to the bi-directional data bus of: • a parallel Flash or • an SDRAM

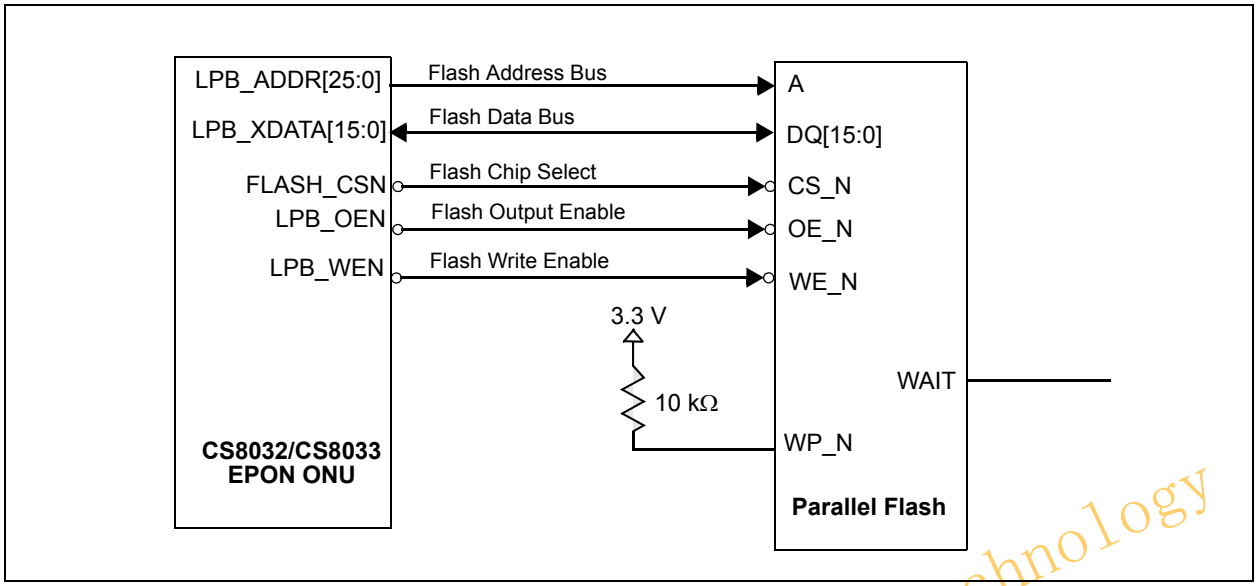
Table 13 Local Bus Signals (Sheet 2 of 2)

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
LPB_WEN	K13	62.5 MHz	OUTPUT LVTTL 8 mA	FLASH/SDRAM Write Enable. The internal control CPU drives this signal. This signal should be connected directly to the active low write enable input of: • a parallel Flash or • an SDRAM
SDRAM_CSN	L13	62.5 MHz	OUTPUT LVTTL 8 mA	Active low Chip Select connected to the chip select pin of an SDRAM device.
FLASH_CSN	M13	10 MHz	OUTPUT LVTTL 8 mA	Active low chip select connected to the chip select pin of a parallel flash device.
LPB_OEN	N15	62.5 MHz	OUTPUT LVTTL 8 mA	FLASH output enable connected to a parallel FLASH device. SDRAM Clock Enable connected to the CKE pin of an SDRAM device.
CPD_CLK_OUT	P15	125 MHz	OUTPUT LVTTL 8 mA	SDRAM Clock Output
CPD_DAT_EN_OUT	R15	62.5 MHz	OUTPUT LVTTL 8 mA	SDRAM Read Data Enable Out
CPD_DAT_EN_IN	P14	62.5 MHz	INPUT LVTTL	SDRAM Read Data Enable Input connected to CPD_DAT_EN_OUT for delay compensation
CPD_CLK_FB_IN	R14	125 MHz	INPUT LVTTL	SDRAM Read Clock Input connected to CPD_CLK_OUT for delay compensation

6.8.1 Parallel Flash

A 16-bit wide Parallel Flash is required only when the embedded ARM926EJ-S* Processor executes code from the flash (otherwise a serial flash may be used). A Parallel Flash shares the Local Bus with an SDRAM (Section 6.8.2). At most 128 MB parallel flash may be connected to the CS8032/CS8033 EPON ONU. Figure 19 illustrates the connections.

Figure 19 Parallel Flash Connections



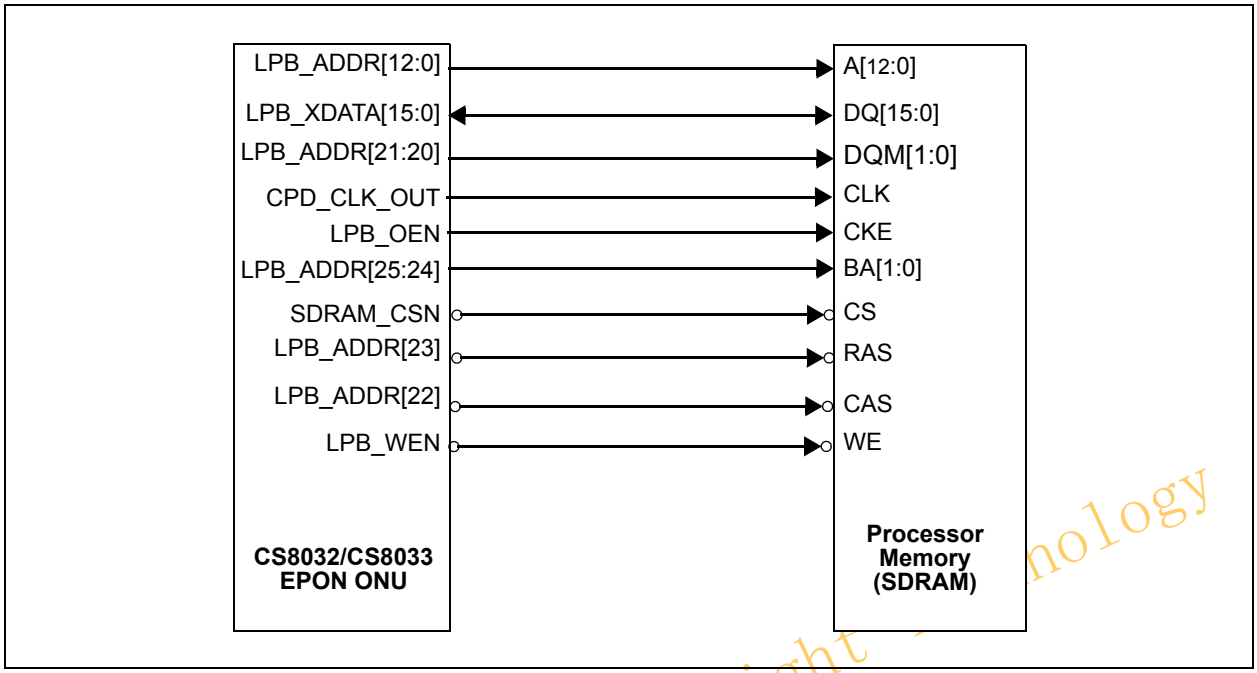
6.8.2 External Memory

The external processor memory is an SDRAM device connected to the external pins of the CS8032/CS8033 EPON ONU and used by the embedded ARM926EJ-S* Processor processor to store instruction and data. The minimum external processor memory is typically 8 MB. The CS8032/CS8033 EPON ONU also has an internal SDRAM that is provided as a SiP or a System in a Package connected to the CS8032/CS8033 EPON ONU die and can be used only when a system requires less than 8 MB of instruction and data storage. In an application either the internal SIP or the external SDRAM can be used by the ARM926EJ-S* Processor. A bootstrap option is provided during power-on reset to select either external SDRAM or SiP SDRAM.

In addition, software can optionally partition the internal Frame Buffer memory to create a dedicated segment for the ARM926EJ-S* Processor to store code and data segments for time critical applications like VoIP.

This section only illustrates the connection between the CS8032/CS8033 EPON ONU and the external SDRAM device. The memory must be at least 125 MHz or faster. Figure 20 illustrates the connections between the CS8032/CS8033 EPON ONU and a 125 MHz SDRAM device.

Figure 20 SDRAM Connections



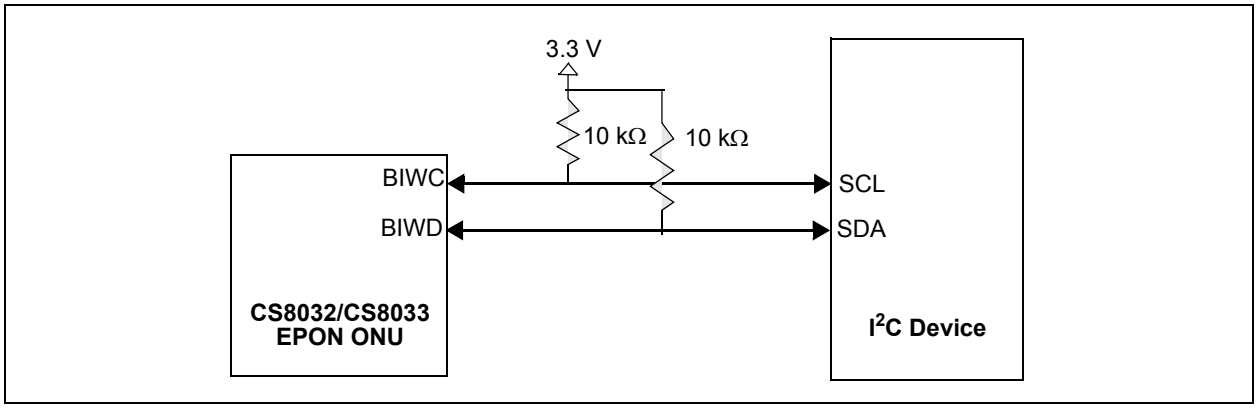
6.9 I2C (Bi-Wire) Interface

The I2C interface of the CS8032/CS8033 EPON ONU may be connected to an I2C interface of a shared I2C bus. The interface is primarily for the embedded Control CPU in the CS8032/CS8033 EPON ONU to read measured receive optical power from an EPON transceiver that supports optical power measurement feature. Table 14 describes the I2C pins and Figure 21 illustrates the connections between the CS8032/CS8033 EPON ONU and an external I2C device.

Table 14 I2C Signals

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
BIWC	D3	4 M	INPUT/ OUTPUT LVTTL 4 mA	I2C Clock
BIWD	E3	4 M	INPUT/ OUTPUT LVTTL 4 mA	I2C Data

Figure 21 I²C Connections



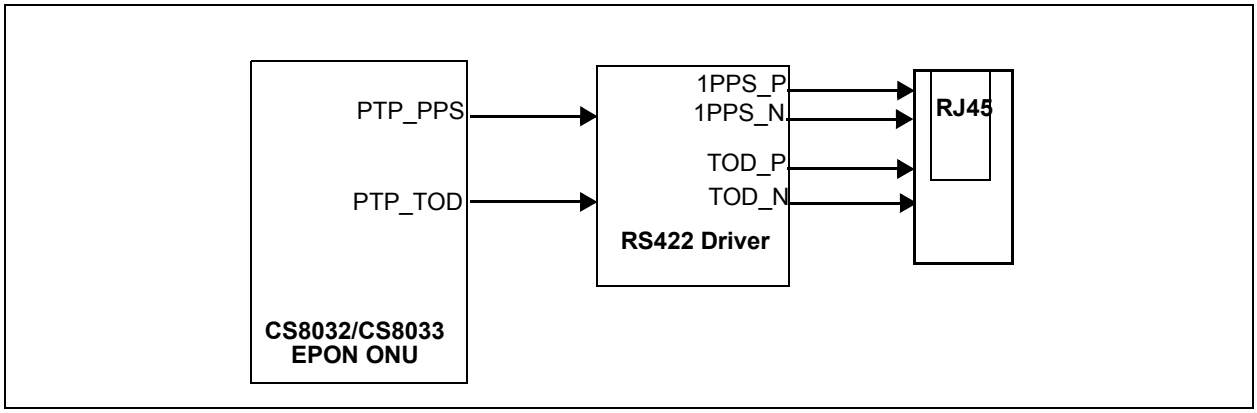
6.10 Timing Synchronization

CTC2.1 specifies that the 1PPS+ToD signals are generated by the ONU and are RS422 compliant signals to an RJ-45 connector. Table 15 describes the signals and Figure 22 illustrates the connections compliant with CTC2.1.

Table 15 Timing Synchronization Signals

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
PTP_PPS	A5	1 Hz-20 kHz	INPUT/ OUTPUT LVTTL 4 mA	CTC2.1 1PPS output from the ONU or UART Input in UART mode.
PTP_TOD	B6	20 kHz	INPUT/ OUTPUT LVTTL 4 mA	CTC2.1 TOD output from the ONU or UART output in UART mode

Figure 22 Timing Synchronization Connections



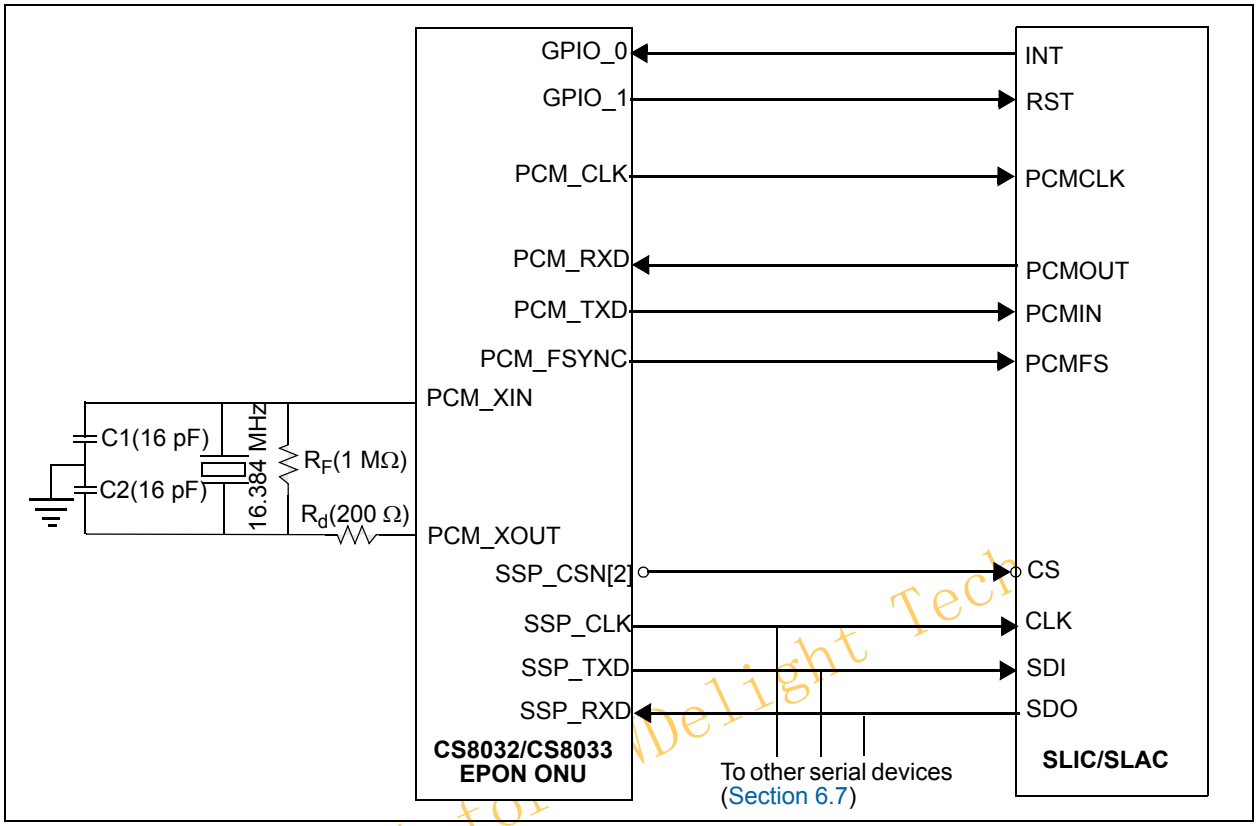
6.11 PCM Interface

A standard SLIC/SLAC device may be connected to this interface. Table 16 describes the PCM pins and Figure 23 illustrates the connections between the CS8032/CS8033 EPON ONU and an external SLIC. The $\overline{INT}$ and the $\overline{RST}$ pins are optional connections from the SLIC/SLAC device to the CS8032/CS8033 EPON ONU GPIO pins.

Table 16 PCM Signals

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
PCM_CLK	A10	256 kHz-8 MHz	OUTPUT LVTTL 2 mA	PCM Clock
PCM_FSYNC	B12	8 Mbps	OUTPUT LVTTL 4 mA	PCM Frame Synchronization Signal ***Note:*** This pin must be pulled down on the board during reset.
PCM_TXD	B10	8 Mbps	OUTPUT LVTTL 4 mA	PCM Serial Transmit Data
PCM_RXD	A11	8 Mbps	INPUT LVTTL 2 mA	PCM Serial Receive Data
PCM_XIN PCM_XOUT	B11 A12	16.384 MHz	INPUT LVTTL	PCM Reference Clock

Figure 23 PCM Connections



6.12 UART Interfaces

The CS8032/CS8033 EPON ONU supports 5 UARTs:

- One full-duplex point-to-point UART with two dedicated pins recommended for software debug
- Four UARTs that are capable of operating either half-duplex or full-duplex mode with 4 pins each

Each point-to-point or multi-drop UART supports at least the following BAUD rates:

- 300
- 600
- 1200
- 2400
- 4800
- 9600
- 19,200
- 38,400
- 115 K
- 192 K

Each one of the four multidrop UARTs uses shared multi-function pins and is connected to an external RS-485 device for driving the UART signals. Each UART can be enabled by a separate enable bit that can be configured by software. If an UART is not enabled, the pins support normal functions. Section 6.12.1 and Section 6.12.2 describe the signal pins used for Point-to-point and multi-drop UARTs, respectively.

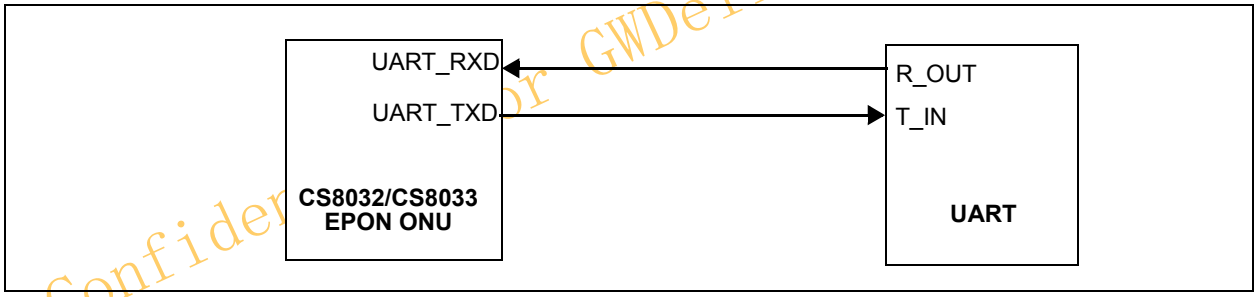
6.12.1 Point-to-Point UART

A standard asynchronous transceiver may be connected to this dedicated 2-pin UART interface. Table 17 describes the UART pins and Figure 24 illustrates the connections between the CS8032/CS8033 EPON ONU and an external UART device.

Table 17 Point-to-Point UART Signals

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
UART_RXD	B5	1 M	INPUT LVTTL	UART Rx input
UART_TXD	B4	1 M	OUTPUT LVTTL 4 mA	UART Tx output

Figure 24 Point-to-Point UART Connections



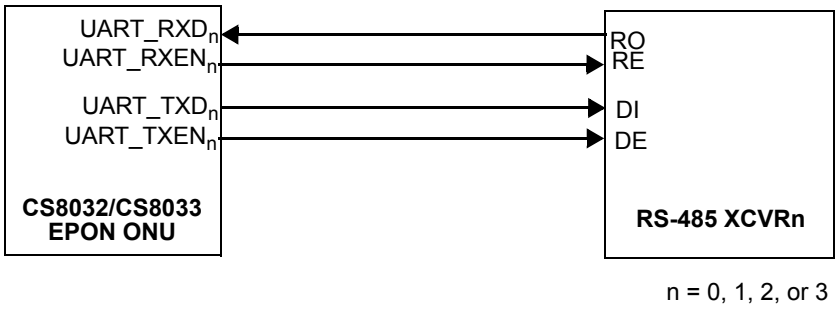
6.12.2 Multi-Drop UARTs

The CS8032/CS8033 EPON ONU supports one, two, three or four standard multi-drop asynchronous transceivers on shared pins. Each of the 4 multi-drop UARTs can be enabled independent of the other UARTs. Since the 4 pins used by an UART are shared with some other function, either the UART or the other function can be used for an application. The option is exercised by software, statically, by configuring the appropriate UART enable CSR bit. Table 18 on page 50 describes the multi-function pins used by the multi-drop UARTs and Figure 24 illustrates the connections between the CS8032/CS8033 EPON ONU and an external UART device. The polarities of transmit enable (TXEN and RXEN signals on each multi-drop UART can be separately configured by the CPU to adapt to the external RS-485 transceiver device requirement).

Table 18 Multi-Drop UART Signals

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
MUART_RXD3 MUART_RXD2 MUART_RXD1 MUART_RXD0	See Table 2, Table 15 Table 16	40 k	INPUT LVTTL	UART Rx input. • MUART_RXD4 is for multi-drop UART4 and shares the *PTP_PPS* pin • MUART_RXD3 is for multi-drop UART3 and shares the *PCM_RXD* pin • MUART_RXD2 is for multi-drop UART2 and shares the *PCM_FSYNC* pin • MUART_RXD1 is for multi-drop UART1 and shares the *GPIO_08* pin
MUART_RXEN3 MUART_RXEN2 MUART_RXEN1 MUART_RXEN0	See Table 2	5 k	OUTPUT LVTTL	UART Rx output enable with configured polarity • MUART_RXEN4 is for multi-drop UART4 and shares the *GPIO_00* pin • MUART_RXEN3 is for multi-drop UART3 and shares the *GPIO_02* pin • MUART_RXEN2 is for multi-drop UART2 and shares the *GPIO_04* pin • MUART_RXEN1 is for multi-drop UART1 and shares the *GPIO_06* pin
MUART_TXD3 MUART_TXD2 MUART_TXD1 MUART_TXD0	See Table 2, Table 15 Table 16	40 k	OUTPUT LVTTL	UART Tx output • MUART_TXD4 is for multi-drop UART4 and shares the *PTP_TOD* pin • MUART_TXD3 is for multi-drop UART3 and shares the *PCM_TXD* pin • MUART_TXD2 is for multi-drop UART2 and shares the *PCM_CLK* pin • MUART_TXD1 is for multi-drop UART1 and shares the *GPIO_09* pin
MUART_TXEN3 MUART_TXEN2 MUART_TXEN1 MUART_TXEN0	See Table 2	5 k	OUTPUT LVTTL	UART Rx output enable with configured polarity • MUART_TXEN4 is for multi-drop UART4 and shares the *GPIO_01* pin • MUART_TXEN3 is for multi-drop UART3 and shares the *GPIO_03* pin • MUART_TXEN2 is for multi-drop UART2 and shares the *GPIO_05* pin • MUART_TXEN1 is for multi-drop UART1 and shares the *GPIO_07* pin

Figure 25 Multi-Drop UART Connections



6.13 Boundary Scan Interface

Table 19 JTAG Signals

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
TCK	P12	10 M	INPUT LVTTL	JTAG TEST CLOCK In
TDI	N12	10 M	INPUT LVTTL Pull-up	JTAG TEST data In
TDO	N11	10 M	OUTPUT LVTTL 2 mA	JTAG TEST data Out
TMS	N13	10 M	INPUT LVTTL Pull-up	Test Mode Select.
TRSTN	K12	10 M	INPUT LVTTL Pull-up	Active Low JTAG Reset

6.14 Analog Pins

Table 20 Analog Signals

Signal Name	Ball Location	Freq/ IO Rate	Pad Type	Description
ATST_REXT_VTOI	P11	—	INPUT / OUTPUT	External resistor 3.03kohm to ground is added at this port
REXT_PMC	R11	—	INPUT / OUTPUT	External resistor port. This pin should be shorted to GND on the PCB via 240 Ohm ESD secondary protection resistor and 5.76K Ohm external resistor(E96).
THERMAL	L10	—	INPUT/ OUTPUT	Thermal diode to ground. This is for Cortina test purpose only. It should be NC on the PCB.

6.15 Power and Ground

6.15.1 Power Balls

Table 21 lists the balls that provide voltage for analog and digital cells in the device. These reference voltage planes must be isolated and filtered separately on the PCB.

Table 21 Core and I/O Power Supply Balls

Signal Name	Ball Location	Nominal Voltage	Description
VDD10A	F7, F8, F9, F10, G7, G8, G9, G10, H6, H7, H8, H9, H10, J6, J7, J8, J9, J10, K6, K7, K8	1.0 V	Nominal 1.0 V for digital core
VDD25A	D7, D8, D11, E4, E12, F4, G2, G4, G14, J4, K4, L11, L12, M4, M5, M12	2.5 V	Nominal 2.5 V for all I/Os except for Serial Flash I/Os
VDD25B	G11, H11, J11	2.5 V	SDRAM IO VDD
VDD25C	F12, G12, H4	2.5 V	SDRAM core VDD
VDD33	D4	3.3 V	Nominal 3.3 V for Serial Flash I/Os
GND1	D5, D6, D9, D10, D12, E5, E6, E7, E8, E9, E10, E11, F5, F6, F11, G1, G5, G6, G15, H5, H12, J5, J12, K5, K9, K10, K11, L5, L6, L7, L8, L9, M11	0 V	Ground for digital core and I/O

Table 22 Analog Power Supply Balls

Signal Name	Ball Location	Nominal Voltage	Description
VDD10B	M7, M8, N6, N7, N8, N9, N10	1.0 V	Analog power
GND2	P5, P7, P9, R5, R7, R9	0 V	Analog ground
AB_PLL_VDDA	P4	2.5 V	PLL Power
AB_PLL_VSSA	R4	0 V	PLL Ground

6.16 Mode Selection

The CS8032/CS8033 EPON ONU supports various static functional modes that must be selected by pulling certain pins up or down. The functional modes are latched by hardware on the rising edge of the *RESETN* pin. The mode selection pins are described in Table 23.

Table 23 Functional Mode Selections

Mode Name	Ball Location	Internal Resistor (Default Mode)	Description
IMAGE_DOWNLOAD_1 IMAGE_DOWNLOAD_0	Table 13		CPD_CLK_OUT = IMAGE_DOWNLOAD_1 CPD_DAT_EN_OUT = IMAGE_DOWNLOAD_0 Image download source select. IMAGE_DOWNLOAD_[1:0]: Selects the source port for downloading image 00 = UART 01 = Parallel Flash 10 = Serial Flash 11 = Ethernet port (Management FE or GE)
BOOT_MODE_1 BOOT_MODE_0	Table 10		RMII_TXD_1 = BOOT_MODE_1 RMII_TXD_0 = BOOT_MODE_0 Control CPU Boot Mode BOOT_MODE: 00 = Parallel Flash Boot 01 = ROM boot 10 = Serial Flash Boot 11 = Reserved
GE_IF_MODE	Table 8		GTXD_3 = GE_IF_MODE NNI Interface mode. 0 = RGMI 1 = RMII
MEM_MAP_SEL	Table 8		GTXD_2 = MEM_MAP_SEL External CPU Memory Selection for boot up 0 = SDR SDRAM 1 = Internal SRAM
SDM_SRAM_SHARE	Table 8		GTXD_1 = SDM_SRAM_SHARE SIP or external SDRAM select 0 = SIP SDRAM 1 = External SDRAM
INT_CLK_SEL	Table 8	INPUT	GTXD_0 = INT_CLK_SEL[1], PCM_TXD = INT_CLK_SEL[0] ARM926EJ_S Processor/AHB clock ratio select: 00 = ARM core runs at 500 Mhz, AHB runs at 125 Mhz; 10 = ARM and AHB both run at 125 Mhz 01 or 10 = Reserved 1 =

7.0 Clock Distribution (TBD)

This section describes how clocks are distributed in the CS8032/CS8033 EPON ONU.

8.0 Package Specification

The CS8032/CS8033 EPON ONU is housed in a 225-pin TFBGA (Thin & Fine-Pitch Ball Grid Array), 13 mm × 13 mm package. The ball pitch is 0.8 mm.

Figure 26 Package Outline Top View

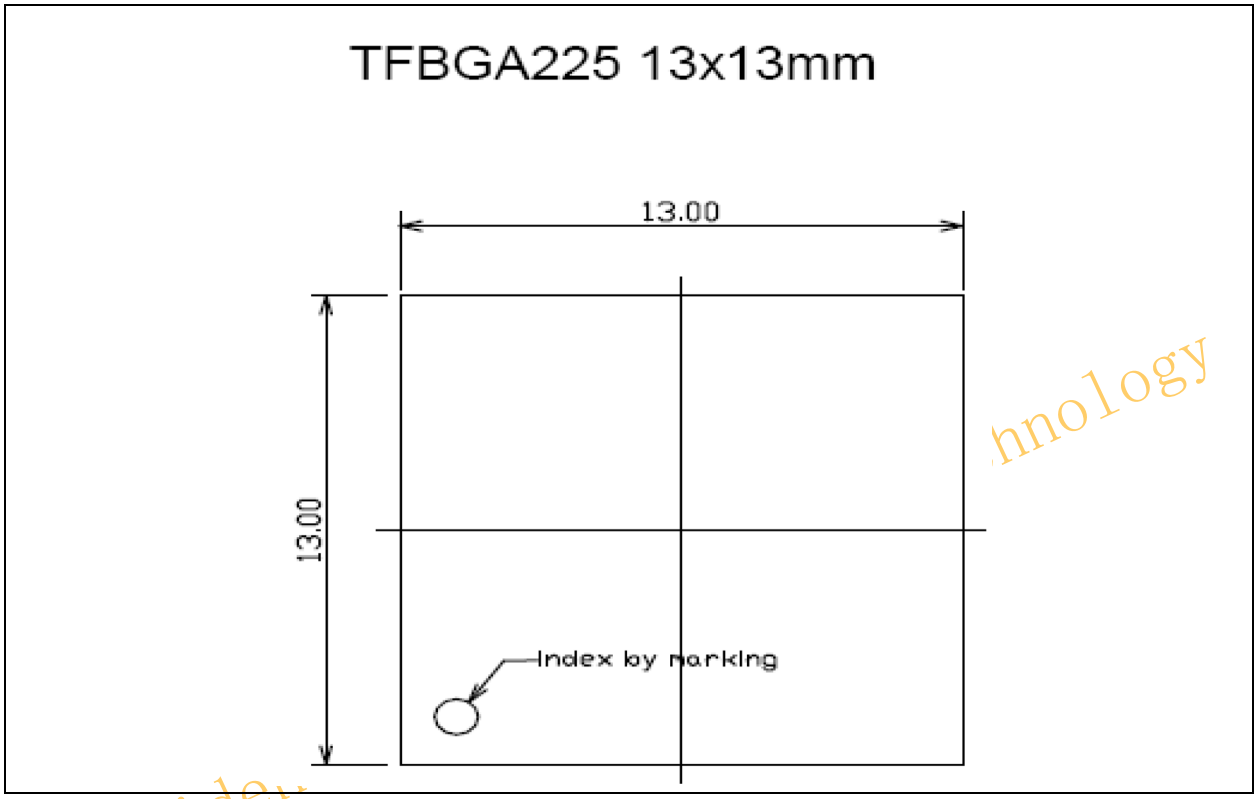


Figure 27 Package Bottom View

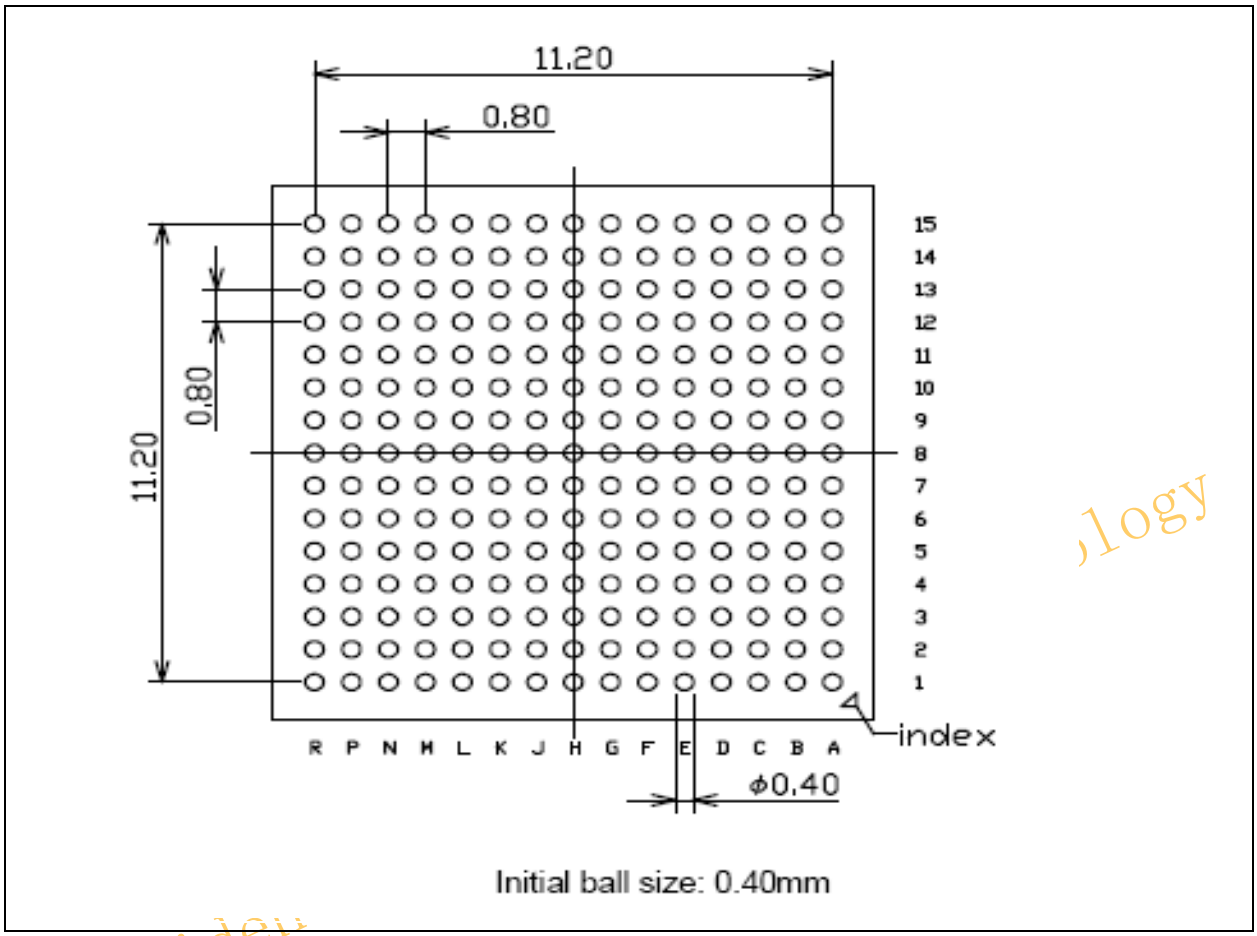
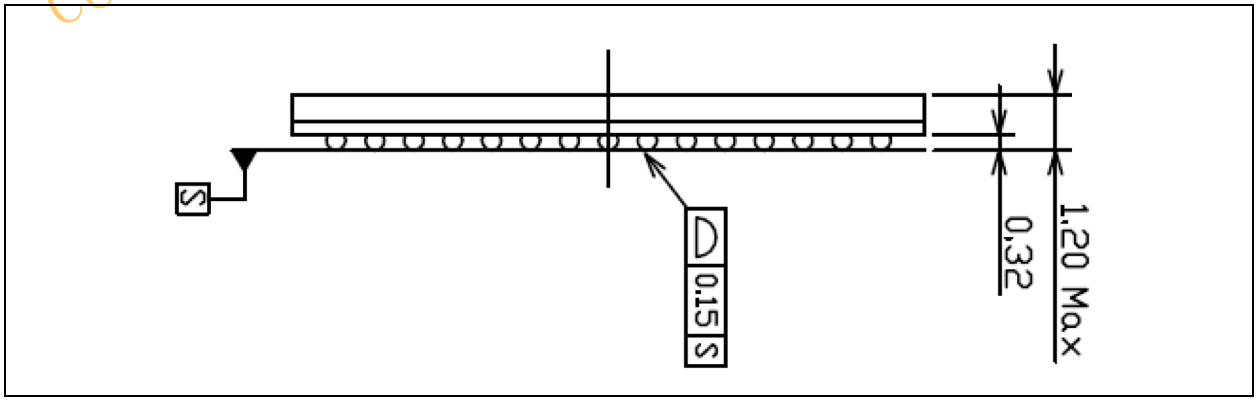


Figure 28 Package Side View



9.0 Thermal Specification

The CS8032/CS8033 EPON ONU is designed to operate over a wide temperature range.

9.1 Device Thermal Specification

The thermal parameters of this device are specified in Table 24:

Table 24 Thermal Parameters

Parameter	Definition	Min	Typ	Max
T_j	Junction temperature at which functional performance is guaranteed.	-40 ºC	50 ºC	125 ºC
T_A	Ambient temperature at which functional performance is guaranteed.	-40 ºC	25 ºC	85 ºC
T_S	Storage temperature	-50 ºC	—	130 ºC

The life of a the CS8032/CS8033 EPON ONU part may be shortened or it may be permanently damaged if any of the specifications in Table 24 is violated.

Table 25 Thermal Resistance Values

Parameter	Definition	Value	Comment
θ_{ja}	Thermal resistance; junction-to-ambient	36 ºC/W	0 m/s air flow
θ_{jc}	Thermal resistance; junction-to-case	8 ºC/W	–
θ_{jb}	Thermal resistance; junction-to-ball	17 ºC/W	–

10.0 Electrical Characteristics

This device shall meet the functional requirements detailed herein when operated over the specified timing, electrical and temperature range.

10.1 Power Supply Sequencing

There are four main supply voltage domains for the CS8032/CS8033 EPON ONU:

- CORE
  - 1.0 V for digital logic (VDD10)
  - 1.0 V for analog cells (AVDD10)
- I/O
  - 2.5 V (VDD25) for all I/Os other than those meant for the Serial Flash
  - 3.3 V (VDD33) for Serial Flash I/Os

Power supplies can be ramped up or down in any order as long as they occur within 500 ms from each other.

It is recommended, but not mandatory, to power up from lower voltage to higher. The lowest voltage rail first and the highest voltage rail last.

It is recommended, but not mandatory, to apply power before clock.

10.2 Absolute Maximum Ratings

The absolute maximum ratings, as specified below, are those ratings beyond which the device's lifetime may be impaired. The meeting of electrical specifications is not implied when the device is subjected to the absolute limits. Table 26 identifies the device's minimum and maximum ratings along with the operating conditions that define the limits for testing the device.

Table 26 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD25}	I/O Supply voltage at the VDD25 balls relative to V_{SS} for all I/Os except for the SSP interface I/Os (Section 6.7)	-0.5	2.7	V
V_{DD33}	I/O Supply voltage at the VDD33 balls relative to V_{SS} for all SSP interface I/Os (Section 6.7)	-0.5	3.6	V
AVDD10, V_{DD10}	Core Supply voltage at the VDD10 balls relative to V_{SS}	-0.5	1.15	V
V_{IN}	Voltage at an input pin	-0.5	3.6	V
—	Electrostatic Discharge Voltage (HBM) - analog balls - digital balls	 -1000 -2000	 1000 2000	V

Caution: Stresses beyond those listed in Table 26 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Table 27 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

10.3 Power Supply Settings

The operating ranges shall be in accordance with Table 27.

Table 27 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD25}	I/O Supply voltage at the VDD25 balls relative to V_{SS} for all I/Os except for the SSP interface I/Os (Section 6.7)	2.375	2.5	2.625	V
V_{DD33}	I/O Supply voltage at the VDD33 balls relative to V_{SS} for all I/Os except for the SSP interface I/Os (Section 6.7)	3.135	3.3	3.465	V
AV_{DD10}, V_{DD10}	Core Supply voltage at the VDD10 balls relative to V_{SS}	0.95	1.0	1.05	V

Notes:
1. All 1.0 V Powers are connected to a common plane on PCB through Filter components.
2. All Grounds are connected to a common plane on PCB through Filter components.

Table 28 Power Estimates

Description	Typical[1]	Worst Case[2]	Units
Core Power (VDD10 plane)	310	800	mW
I/O Power (VDD25 and VDD33 planes)	220	290	mW
Total	530	1090	mW

1. Typical power is estimated at 1.0 V Core Supply Voltage and 2.5 V I/O Supply Voltage with 25 ºC junction temperature at Typical Process
2. Worst Case power is estimated at 1.1 V Core Supply Voltage and 2.625 V I/O Supply Voltage with T_j = 125 ºC at Fast Process

10.4 DC Characteristics

10.4.1 2.5 V Input/Output Characteristics

Table 29 identifies the characteristics for all 2.5 LVTTL balls. LVTTL logic interfaces include all signal pins described in Section 6.0, *Pin Descriptions*, on page 29 except for EPON ONU SerDes and SSP balls:

- RGMII/RMII interface signals
- PCM interface signals
- All ARM* Peripheral Interface signals except for the SSP (Section 6.7) signals
- GPIOs
- SDRAM
- Reference Clock and clock outputs

Table 29 2.5 V I/O DC Characteristics[1]

Symbol	Parameter		Min	Typ	Max	Units	Test Conditions
V_{OL}	Output Low Voltage		—		0.7	V	
V_{OH}	Output high Voltage		1.7			V	
I_{OZ}	Tri-state output leakage current				±10	µA	V_{dd} = Max. V_o = VDDIO
I_{OH}	Output High current	2 mA	3.0	6.2	10.8	mA	VOH = VOH_{min}
		4 mA	6.1	12.5	21.5	mA	
		8 mA	12.2	25.0	43.1	mA	
		12 mA	18.3	37.5	64.6	mA	
I_{OL}	Output Low current	2 mA	3.0	5.2	7.9	mA	VOL = VOL_{max}
		4 mA	6.1	10.5	16.0	mA	
		8 mA	12.3	21.0	32.1	mA	
		12 mA	18.4	31.5	48.1	mA	
V_{IL}	Input Low Level (input and I/O)		-0.3		0.7	V	
V_{IH}	Input High Level (input and I/O)		1.7		3.6	V	
V_H	Input Hysteresis			5		mV	
I_I	Input leakage Current				10	µA	VI = 2.5 V
I_{IH}	Input High current				15	µA	VDDIO = Max
C_{in}	Input pin Capacitance			4			pF
C_{out}	Output pin Capacitance			4			pF
C_{IO}	I/O pin Capacitance			4			pF

1. Unless specified, VDD (Core Power Supply) = 0.95 V to 1.05 V, VDDIO (I/O Power Supply) = 2.375 V to 2.625 V
   TJ = -40 °C to 115 °C
2. Note that LVTTL inputs and IOs are 3.3 V tolerant.
3. Not more than one output should be shorted at one time. Duration should not be more than one second.

10.4.2 3.3 V Input/Output Characteristics

Table 30 identifies the characteristics for the 3.3 V balls of the SSP (Section 6.7) interface signals.

Table 30 3.3 V I/O DC Characteristics[1]

Symbol	Parameter		Min	Typ	Max	Units	Test Conditions
V_{OL}	Output Low Voltage		—		0.7	V	
V_{OH}	Output high Voltage		VDD33 - 0.2			V	
I_{OZ}	Tri-state output leakage current				±10	µA	V_{dd} = Max. V_o = VDDIO
I_{OH}	Output High current	2 mA	3.0	6.2	10.8	mA	VOH = VOH_{min}
		4 mA	6.1	12.5	21.5	mA	
		8 mA	12.2	25.0	43.1	mA	
		12 mA	18.3	37.5	64.6	mA	
I_{OL}	Output Low current	2 mA	3.0	5.2	7.9	mA	VOL = VOL_{max}
		4 mA	6.1	10.5	16.0	mA	
		8 mA	12.3	21.0	32.1	mA	
		12 mA	18.4	31.5	48.1	mA	
V_{IL}	Input Low Level (input and I/O)		-0.3		0.7	V	
V_{IH}	Input High Level (input and I/O)		1.7		3.6	V	
V_H	Input Hysteresis			5		mV	
I_I	Input leakage Current				10	µA	VI = 2.5 V
I_{IH}	Input High current				15	µA	VDDIO = Max
C_{in}	Input pin Capacitance			4			pF
C_{out}	Output pin Capacitance			4			pF
C_{IO}	I/O pin Capacitance			4			pF

Notes:
1. unless specified, VDD10, VDD25, and VDD33 are within the ranges specified in Table 27, *Recommended Operating Conditions*, on page 59
2. TJ = -40 °C to 115 °C
3. All inputs and I/Os are 3.3 V tolerant.
4. Not more than one output should be shorted at one time. Duration should not be more than one second.

10.5 AC Characteristics

10.5.1 SerDes Interfaces

The CS8032/CS8033 EPON ONU line interface blocks support the IEEE802.3 ([2] on page 86) EPON standard.

10.5.1.1 SerDes Limiting Receiver Characteristics

Figure 29 SerDes Receive Data Eye Mask

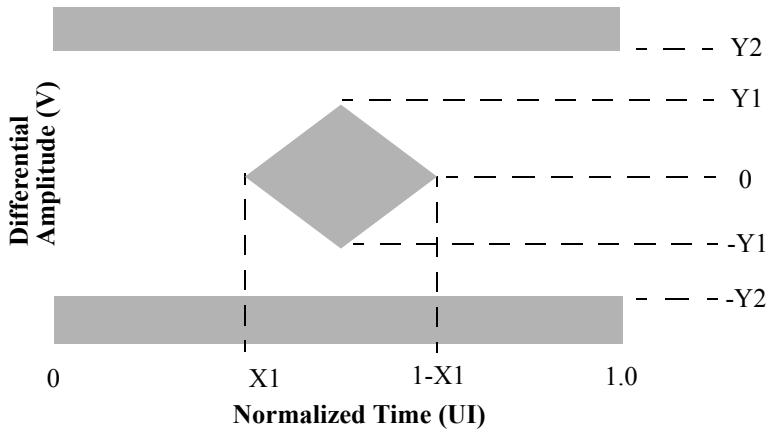


Table 31 SerDes Receive Eye Mask Parameters

Parameter	Limit	Unit
X1	0.375	UI max
Y1	50	mV min
Y2	800	mV max

Table 32 SerDes Receive Data Input Characteristics

Parameter	Min	Typ	Max	Units	Comment
Input Voltage Range	0.1	—	1.0	V	—
Differential Termination Impedance	90	100	110	Ω	—
Differential Input Return Loss (100 Ω reference): *0.010 to 2.5 GHz:*	—	—	-10	dB	—
Common Mode Voltage for optional DC Coupled EPON Signals	—	0.7	—	Volt	Not applicable if the EPON signals are AC coupled
Common Mode Return Loss (25 Ω reference; 0.1 to 2.5 GHz)	—	—	-6	dB	—
Differential Receive Voltage:	100	—	800	mVpp (differential)	—
Jitter Tolerance (JitTol)	0.749	—	—	UIpp	—
Note: 1. Differential Input Return Loss is given by the equation RL = 10 - 16.6 Log 10 (f/7.5) where “f” is in GHz.					

10.5.1.2 SerDes Transmitter Characteristics

Figure 30 SerDes Transmit Data Eye Mask

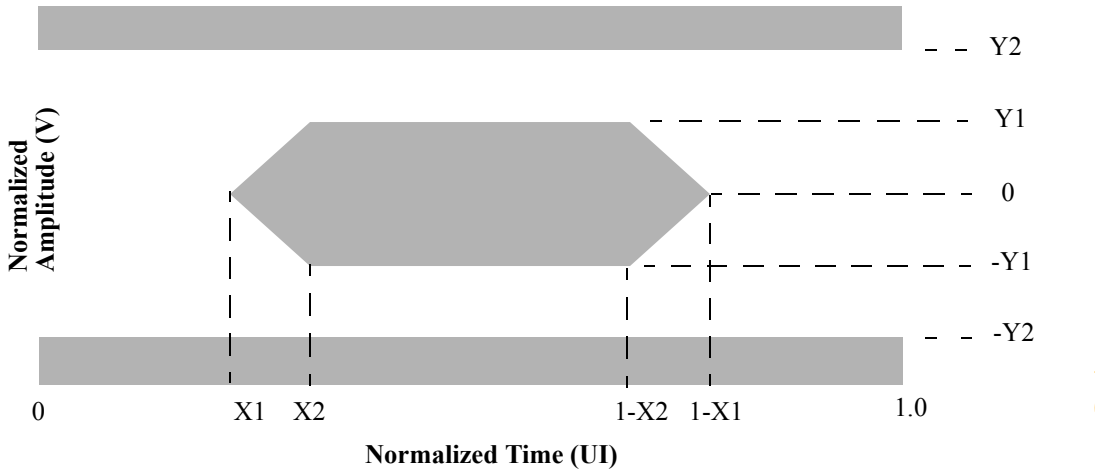


Table 33 SerDes Transmit Eye Mask Parameters

Parameter	Limit	Unit	Comment
X1	.125	UI max	—
X2	.390	UI max	—
Y1	300	mV min	—
Y2	600	mV max	—

Table 34 SerDes Transmit Data Output Characteristics

Parameter	Min	Typ	Max	Units	Comment
Differential Termination Impedance	80	100	120	Ω	—
Differential Output Return Loss (90-110 ohm reference):	—	—	-5	dB	At 2GHz[2]
Output rise/fall time (20% to 80% with 0.4 pF plus 50 Ω load)	—	—	175	ps	—
Differential Skew	—	—	15	ps	—
Differential Output Swing	600	—	1200	mVp[3]	—
Transmit Jitter (JitGen)	—	—	.24	UI	—

Notes:
1. Return Loss is given by the equation RL = 10 - 16.6 Log 10 (f/7.5), where "f" is in GHz.
2. Compliant with IEEE 802.3 Section 47.3.3.4 specification on return loss:
   –10 dB for 312.5 MHz < Freq (f) < 625 MHz, and
   –10 + 10log(f/625) dB for 625 MHz ≤ Freq (f) ≤ 3.125 GHz
3. Transmit Output level can be programmed by up to ±25%. As much as 20% pre-emphasis can be added to transmit output. Both the default transmit level and pre-emphasis are TBD.

10.5.2 Local Bus Interface Timing

The CS8032/CS8033 EPON ONU uses the local bus to communicate with either an optional parallel flash device (Section 10.5.2.1) or an external SDRAM (Section 10.5.2.2).

10.5.2.1 Parallel Flash Timing

When a Parallel Flash is connected on the local bus, the address LPB_ADDR, active-low read/write control LPB_WEN are setup prior to the assertion of the active-low chip select FLASH_CSN and remain valid throughout the read cycle as shown in Figure 31. The configured Read Cycle delay N_{rd} is in number of internal HCLK cycles. HCLK is the internal 62.5 MHz bus clock. The configured delay guarantees that read data is stable from the target device when the CS8032/CS8033 EPON ONU will latch the read data. Read Data is sampled from the LPB_XDATA signals on the rising edge of the internal clock at the end of the Read Cycle delay. All control and address lines remain stable after chip_select FLASH_CSN is deasserted.

The relative control signal pulse positions, for read access, can be configured for an external parallel flash. The following timing parameters can b e configured:

- First segment duration component of FLASH_CSN
- Second segment duration of FLASH_CSN and duration of LPB_OEN
- Final segment of duration component of FLASH_CSN
- a2a/access - interposing segment duration for Access2Access single access sequence
- Cskew - delay component to skew (make later) FLASH_CSN relative to LPB_ADDR
- Oskew - delay component to skew LPB_OEN relative to LPB_ADDR

Note that all configuration parameter units are HCLK cycles.

Figure 31 Internal CPU Local Bus Read Timing Diagram

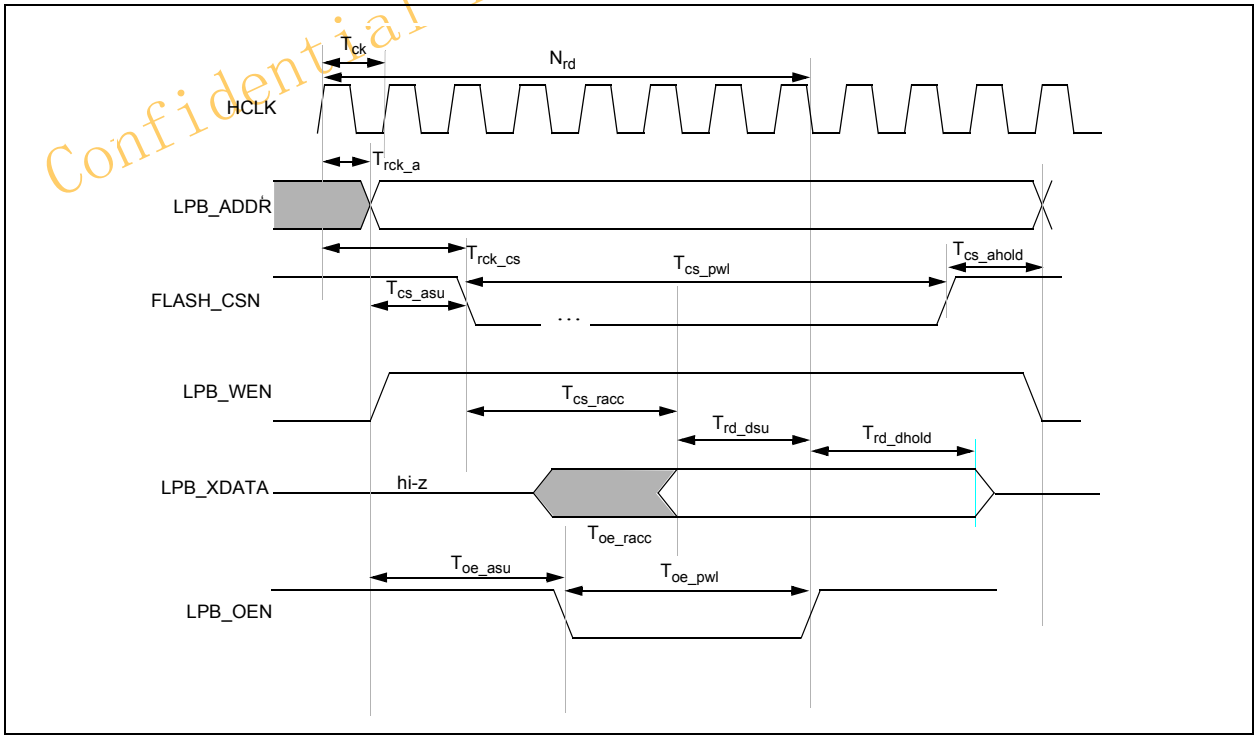


Table 35 Internal CPU Local Bus Interface Read Timing

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{ck}	Internal state clock cycle time	16	—	—	ns	HCLK = bus clock (nominally 62.5 MHz)
T_{Nrd}	Length of Read access time derived from configuration settings	16	—	—	ns	Duration of LPB_CSN and LPB_OEN
T_{rck_a}	Address clock to output delay	10	—	—	ns	—
T_{rck_cs}	LPB_CSN to output delay	15	—	—	ns	—
T_{cs_asu}	Address setup to LPB_CSN going LOW	10 + Cskew * T_{ck}	—	—	ns	LPB_CSN assertion skewed by the configured Cskew in number of HCLK cycles
T_{oe_asu}	Address setup to LPB_OEN going LOW	10+ Oskew* T_{ck}	—	—	ns	LPB_OEN assertion skewed by the configured Oskew in number of HCLK cycles
T_{cs_racc}	Read access time of slave device from assertion of LPB_CSN	15	—	—	ns	Example only
T_{oe_racc}	Read access time of slave device from assertion of LPB_OEN	15	—	—	ns	Example only
T_{cs_pwl}	Width of LPB_CSN active pulse, set by configured value	csum*T_{ck}	—	—	ns	Delay is sum of configured porch values: **csum = front+middle+back**
T_{oe_pwl}	Width of OE active pulse, set by register value	middle*T_{ck}	—	—	ns	Delay is configured porch value: middle or if SRAM_ACK is enabled, width determined by external SLAVE
T_{rd_dsu}	Read setup time relative to end of either LPB_CSN or LPB_OEN active pulse	15 + 2*T_{ck}	—	—	ns	Input read setup is device delay component plus a number HCLK cycles
T_{rd_dhold}	Read hold time relative to end of either LPB_CSN or LPB_OEN active pulse	T_{ck}	—	—	ns	One HCLK cycle of hold required
T_{cs_ahold}	Address hold after deassertion of LPB_CSN	T_{ck}* (A2A-Cskew)-2	—	—	ns	A2A and Xtra are configuration values for back to back and single access tail delay before starting next access
T_{oe_ahold}	Address hold after deassertion of LPB_OEN	T_{ck}* (A2A-Oskew)-2	—	—	ns	A2A and Xtra are configuration values for back to back and single access tail delay before starting next access

As in the Read case, the Internal Local bus Write cycle starts with the assertion of LPB_ADDR and LPB_WEN control prior to the assertion of the chip select FLASH_CSN as shown in Figure 32. After FLASH_CSN is asserted, the CS8032/CS8033 EPON ONU LPB_DATA lines are driven in the Lo-Z state. The write data is stable after the FLASH_CSN output delay. Write data remains valid for the duration of the Write Cycle delay (N_{wr}+1) FLASH_CLK cycles. The write cycle terminates on either the deassertion of LPB_WEN, or FLASH_CSN, whichever occurs first. The Address (LPB_ADDR), chip select (FLASH_CSN), and Write data (LPB_DATA) are held stable for 1 additional FLASH_CLK cycle after the deassertion of LPB_WEN. After chip select is de-asserted, the SRAM_DATA balls return to the Hi-Z state.

Many of the relative control signal pulse positions, for WRITE ACCESS, are configured for each of the (FLASH, SDRAM)_CSN decoded device spaces. The each decoded address space has an independent set of configuration values as listed below:

- Front - first segment duration component of xxx_CSN, LPB_WEN, LPB_DATA
- Middle - second segment duration component of xxx_CSN, LPB_WEN, LPB_DATA
- Back - final segment of duration component of xxx_CSN, LPB_WEN, LPB_XDATA
- A2a/access - interposing segment duration for Access2Access single access sequence
- Cskew - delay component to skew (make later) xxx_CSN relative to LPB_ADDR
- Wskew - delay component to skew LPB_WEN relative to LPB_ADDR
- Dskew - delay component to skew LPB_DATA driven relative to LPB_ADDR

Note that all configuration parameter units are HCLK cycles. Table 37 on page 70 and Figure 33 on page 69 show the SDRAM interface timing.

Figure 32 Internal CPU Local Bus Write Timing Diagram

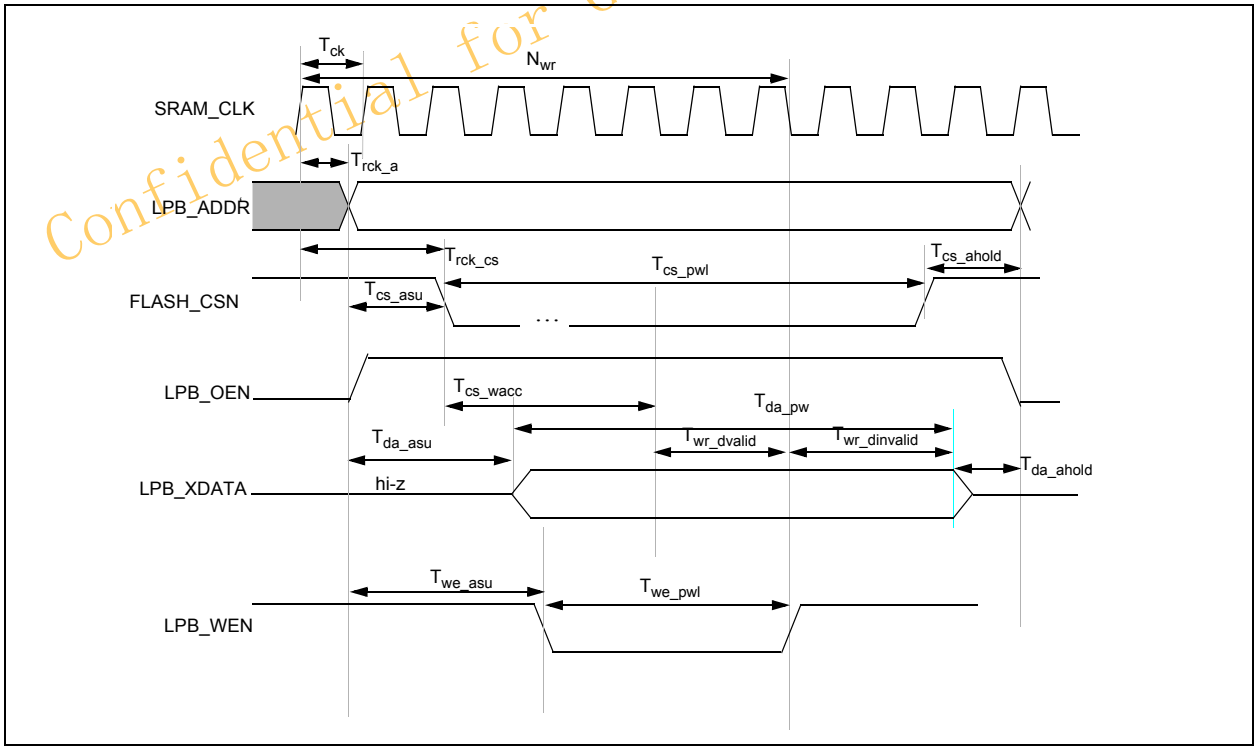


Table 36 Internal CPU Local Bus Interface Write Timing (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{ck}	Internal state clock cycle time	5	—	—	ns	HCLK = 1/2 CPU core clock (nominally 200 MHz, or 5 ns)
T_{Nwr}	Length of Write access time derived from configuration settings	5	—	—	ns	Duration if CSN ends access: **front+middle+back** Duration if OE ends access: **front+middle**
T_{rck_a}	Address clock to output delay	10	—	—	ns	—
T_{rck_cs}	LPB_CSN clock to output delay	15	—	—	ns	—
T_{cs_asu}	Address setup to LPB_CSN going LOW	10 + Cskew * T_{ck}	—	—	ns	LPB_CSN assertion is skewed by the configured amount Cskew
T_{da_asu}	Address setup to Data drivers going LO-Z	10+ Dskew* T_{ck}	—	—	ns	Write data window skew is configuration value.Dskew
T_{we_asu}	Address setup to LPB_WEN going LOW	10+ Wskew* T_{ck}	—	—	ns	LPB_WEN assertion skew is configuration value Wskew
T_{cs_wacc}	Write access time of slave device from assertion of LPB_CSN	15	—	—	ns	Example only
T_{we_wacc}	Write access time of slave device from assertion of LPB_WEN	15	—	—	ns	Example only
T_{cs_pwl}	Width of LPB_CSN active pulse, set by register value	csum*T_{ck}	—	—	ns	Delay is sum of configured porch values: **csum = front+middle+back**
T_{da_pw}	Width of LPB_XDATA write valid window, set by register value	csum*T_{ck}	—	—	ns	Delay is configured porch value: **csum = front+middle+back**
T_{we_pwl}	Width of LPB_WEN active pulse, set by register value	middle*T_{ck}	—	—	ns	Delay is configured porch value: middle
T_{wr_dvalid}	Write valid time before the end of either LPB_CSN or LPB_WEN active pulse	T_{ck}*(csum -Dskew + Cskew) -15	—	—	ns	Available Write Data window width is controlled by register values, modified by skew applied to Data window and skew applied to LPB_CSN If cycle ends via LPB_WEN, then Cskew is replaced with Wskew
$T_{wr\_dinvalid}$	Write valid time after the end of either LPB_CSN or LPB_WEN active pulse	T_{ck}* (Dskew - Cskew) - 5	—	—	ns	Write LPB_XDATA output hold will be increased when Dskew is increased and decreased when Cskew is increased If cycle ends via LPB_WEN, then Cskew is replaced with Wskew

Table 36 Internal CPU Local Bus Interface Write Timing (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{cs_ahold}	Address hold after deassertion of LPB_CSN	T_{ck}* (A2A-Cskew)-2	—	—	ns	A2A and Xtra are configuration values for back to back and single access tail delay before starting next access
T_{da_ahold}	Address hold after LPB_XDATA drivers enter HI-Z state	T_{ck}* (A2A-Dskew)-2	—	—	ns	A2A and Xtra are configuration values for back to back and single access tail delay before starting next access
T_{we_ahold}	Address hold after deassertion of LPB_WEN	T_{ck}* (A2A-Wskew)-2	—	—	ns	A2A and Xtra are configuration values for back to back and single access tail delay before starting next access

10.5.2.2 External SDRAM Interface Timing

The embedded ARM926EJ-S* Processor can use an external 125 MHz, 16-bit wide SDRAM device to store instruction and data instead of the internal SIP. The CS8032/CS8033 EPON ONU supports CAS latency 3. Figure 33 on page 69 is the SDRAM interface timing diagram and Table 37 on page 70 specifies the AC characteristics of the SDRAM interface.

Figure 33 SDRAM Interface Timing

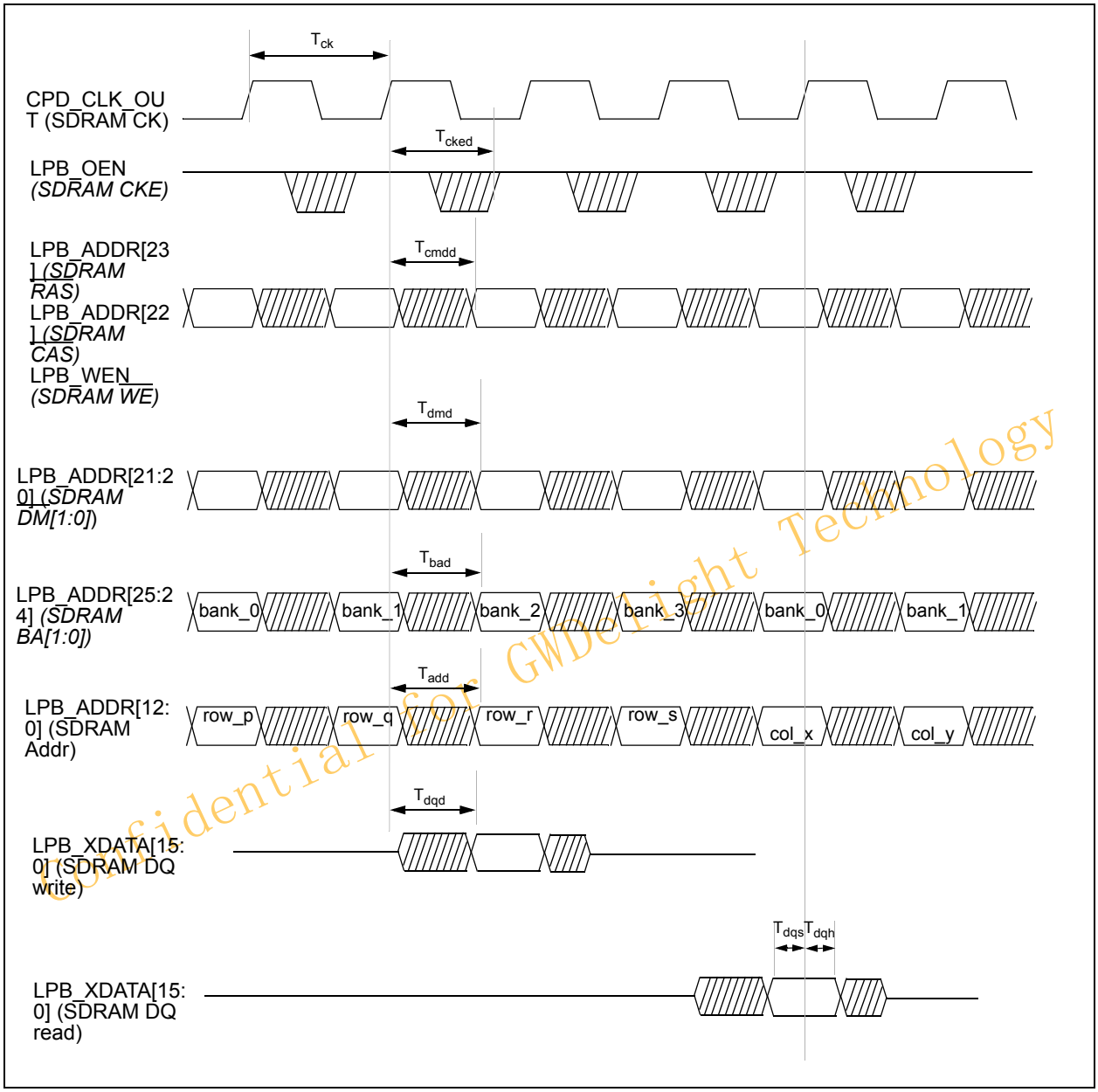


Table 37 SDRAM Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{ck}	External SDRAM clock CPD_CLK_OUT cycle time	7.996	8	8.004	ns	External SDRAM clock reference. 125 MHz ±50 PPM
T_{cked}	CKE delay from SDRAM reference clock rising edge	—	—	—	ns	—
T_{cmdd}	SDRAM Command ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$) delay from SDRAM reference clock rising edge	—	—	—	bits	—
T_{dmd}	$\overline{DM}$ delay from SDRAM reference clock rising edge	—	—	—	ns	—
T_{bad}	BA[1:0] delay from SDRAM reference clock rising edge	—	—	—	ns	—
T_{add}	Address [14:0] delay from SDRAM reference clock rising edge	—	—	—	ns	—
T_{dqd}	DQ [15:0] delay from SDRAM reference clock rising edge	0.0	—	—	ns	SDRAM write cycle
T_{dqs}	DQ [15:0] setup to SDRAM reference clock rising edge	0.0	—	—	ns	SDRAM write cycle
T_{dqh}	DQ [15:0] hold from SDRAM reference clock rising edge	0.0	—	—	ns	SDRAM write cycle

10.5.3 Synchronous Serial Interface (SSP) Timing

The SSP interface supports synchronous serial protocols to at least three external devices. The timing of the serial clock and data is programmable up to 25 Mbps. Protocol defines that outputs change coincident with the falling edge of clock and are sampled with the rising edge of the clock. (CPOL = 0, CPHA = 0) As such there is an inherent setup and hold time allowance of 1/2 of a clock cycle. Figure 34 on page 71 is the SSP interface timing diagram and Table 38 on page 71 specifies the AC characteristics of the interface.

Figure 34 Synchronous Serial Interface Timing Diagram

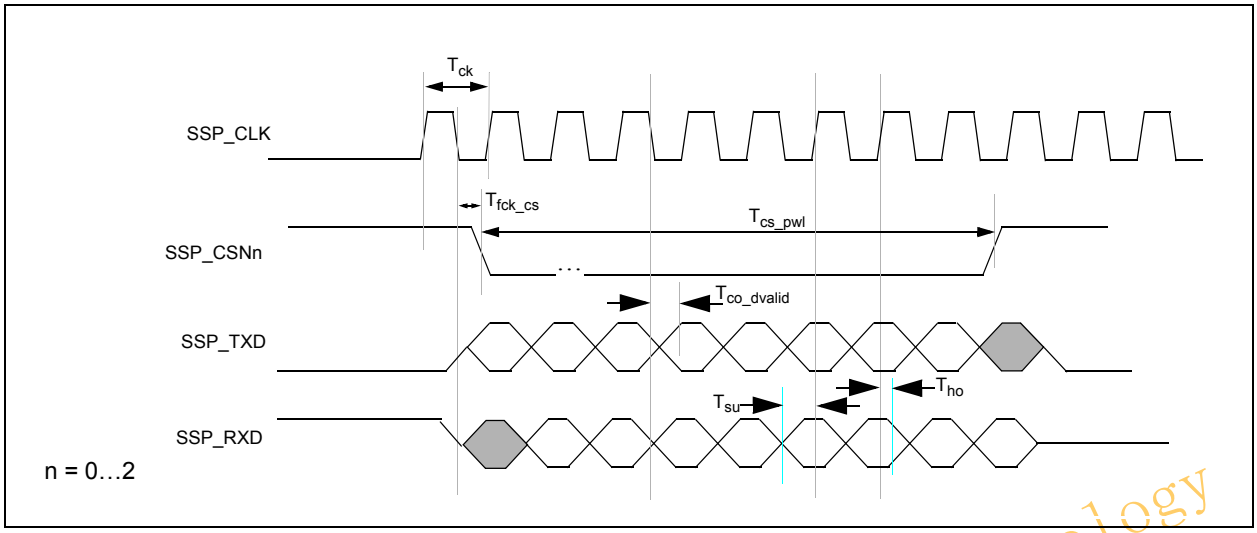


Table 38 Synchronous Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{ck}	External transfer clock cycle time	40	—	1000	ns	SSI clock period is programmable for each of the three (3) device selects
T_{fck_cs}	Skew SSP_CSNn to SSP_CLK	-1.0	—	0.5	ns	—
T_{cs_pwl}	Duration of Burst transfer	16	—	64	bits	Command width and data width is configurable for each of the three (3) device selects
T_{co_dvalid}	Data output valid time from falling edge of SSP_CLK	0.20	—	1.1	ns	—
T_{su}	SSP_RXD setup time to rising edge of SSP_CLK	8.3	—	—	ns	—
T_{ho}	SSP_RXD hold time from rising edge of SSP_CLK	0.0	—	—	ns	—

10.5.4 I²C (BiWire) Interface Timing

The BiWire interface is a two signal protocol providing bidirectional data exchange using wired-or data and clock signals. The transfer frequency is set via configuration registers. Figure 35 on page 72 is the BiWire interface timing diagram and Table 39 on page 72 specifies the AC characteristics of the interface.

Figure 35 BiWire Interface Timing Diagram

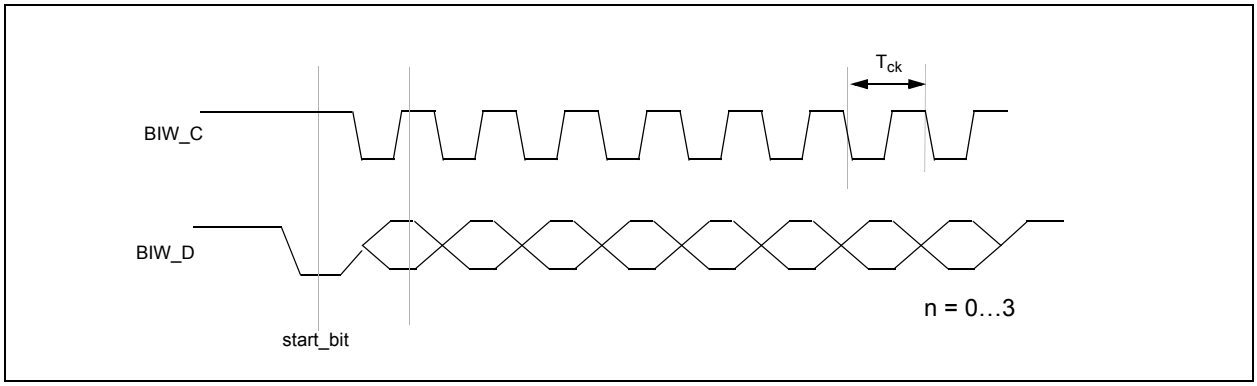


Table 39 BiWire Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{ck}	External transfer clock cycle time	50ns	—	131 ms	—	BiWire clock period is configured by software
T_{co}	BIWC to BIWD Output valid	5	—	15	ns	—
T_{sul}	BIWD input setup relative to rising edge of BIWC	15	—	—	ns	—
T_{ho}	BIWD input hold after rising edge of BIWC	15	—	—	ns	—

10.5.5 PHY Interface Timings

10.5.5.1 RGMII Mode

The GE UNI interface of the CS8032/CS8033 EPON ONU supports RGMII ([3] on page 86) protocol. This section specifies the AC electrical characteristics of the RGMII reference clock (Figure 36 on page 72), receive (Figure 37 on page 73), and transmit (Figure 38 on page 73) signals. Table 40 on page 73 specifies various the timing parameters of the RGMII interface. It is strongly recommended to use normal mode on PHY for CS8032/CS8033 EPON ONU Receive Interface, and use delay mode on PHY for CS8030 EPON ONU Transmit Interface.

Figure 36 RGMII Reference Clock Timing

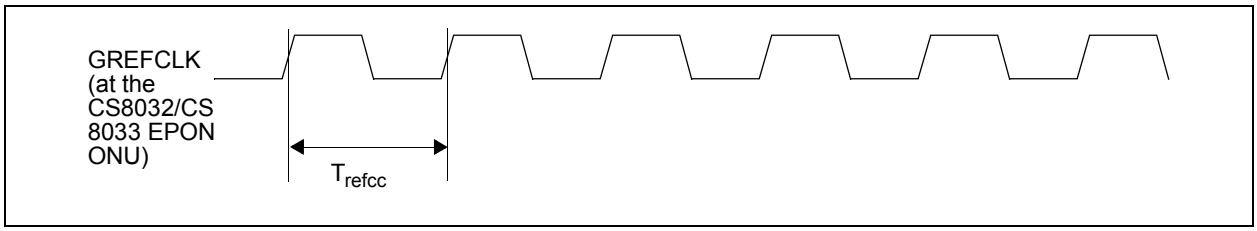


Figure 37 RGMII Receive Timing

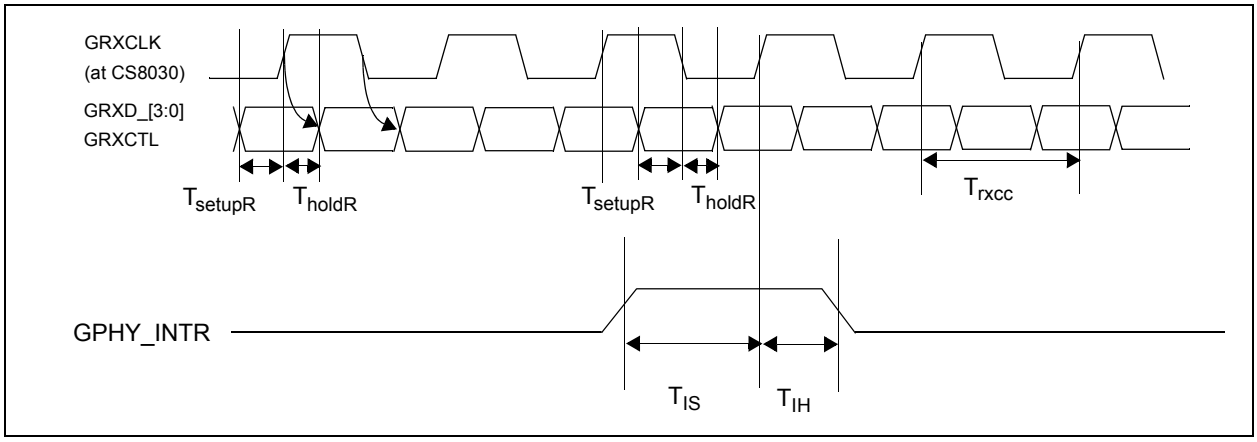


Figure 38 RGMII Transmit Timing

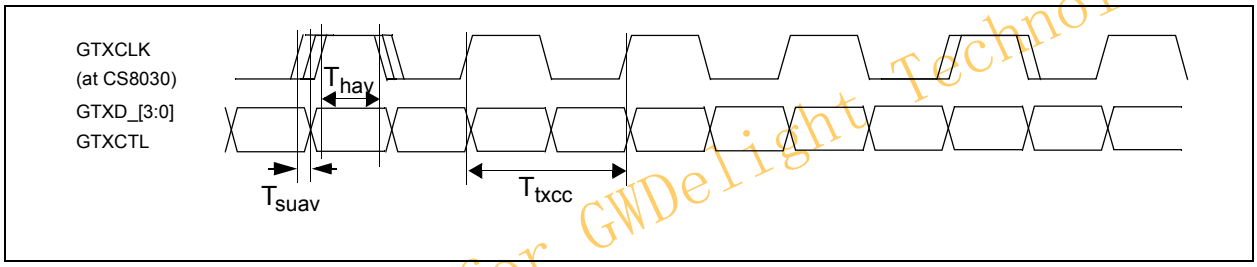


Table 40 RGMII Mode (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{refcc}	GREFCLK cycle time	36	40	44	ns	25 MHz ±50 PPM (Figure 36)
T_{rxcc}	GTXCLK cycle time in 1000 Mbps mode	7.9992	8	8.0008	ns	125 MHz ±100 PPM (Figure 37)
	GTXCLK cycle time in 100 Mbps mode	32	40	48	ns	25 MHz ±100 PPM (Figure 37)
	GTXCLK cycle time in 10 Mbps mode	320	400	480	ns	2.5 MHz ±100 PPM (Figure 37)
T_{setupR}	GRXD_[3:0] or GRXCTL input to GRXCLK Clock rising or falling setup time	0.5	—	—	ns	Figure 37
T_{holdR}	GRXCLK Clock rising or falling edge to GRXD_[3:0] or GRXCTL input hold	0.5	—	—	ns	Figure 37
T_{IS}	GPHY_INTR input to GRXCLK Clock rising setup time	0.5	—	—	ns	Figure 37
T_{IH}	GRXCLK Clock rising to GPHY_INTR input to hold time	1.0	—	—	ns	Figure 37

Table 40 RGMII Mode (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{txcc}	GTXCLK cycle time in 1000 Mbps mode	7.9996	8	8.0004	ns	125 MHz ±50 PPM
	GTXCLK cycle time in 100 Mbps mode	36	40	44	ns	25 MHz ±50 PPM
	GTXCLK cycle time in 10 Mbps	360	400	440	ns	2.5 MHz ±50 PPM
$T_{\_suav}$	GTXD_[3:0] or GTXCTL data output to GREFCLK transition (at the CS8032/CS8033 EPON ONU)	-0.50	0	0.50	ns	Figure 38
Duty_R	GREFCLK duty cycle	40	50	55	%	—
Duty_G	GRXCLK, and GTXCLK duty cycle in 1000 Mbps mode	40	50	60	%	—
	GRXCLK and GTXCLK duty cycle in 10/100 Mbps mode	40	50	60	%	—
Tr / Tf	Rise / Fall Time (20-80%)	—	—	0.75	ns	—
T_hav	Clock transition to data valid (available hold time).	3.1	—	—	ns	

10.5.5.2 RMII Mode

The FE UNI interface and the GE UNI interface of the CS8032/CS8033 EPON ONU support RMII ([4] on page 86) protocol. This section specifies the AC electrical characteristics of the RMII reference clock (Figure 39 on page 74), receive (Figure 40 on page 75), and transmit (Figure 41 on page 75) signals. Table 41 on page 75 specifies various the timing parameters of the RMII interface.

Figure 39 RMII Reference Clock Timing

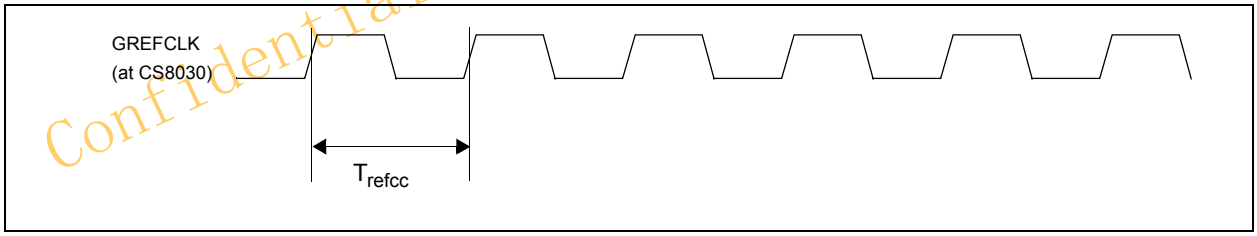


Figure 40 RMII Receive Timing

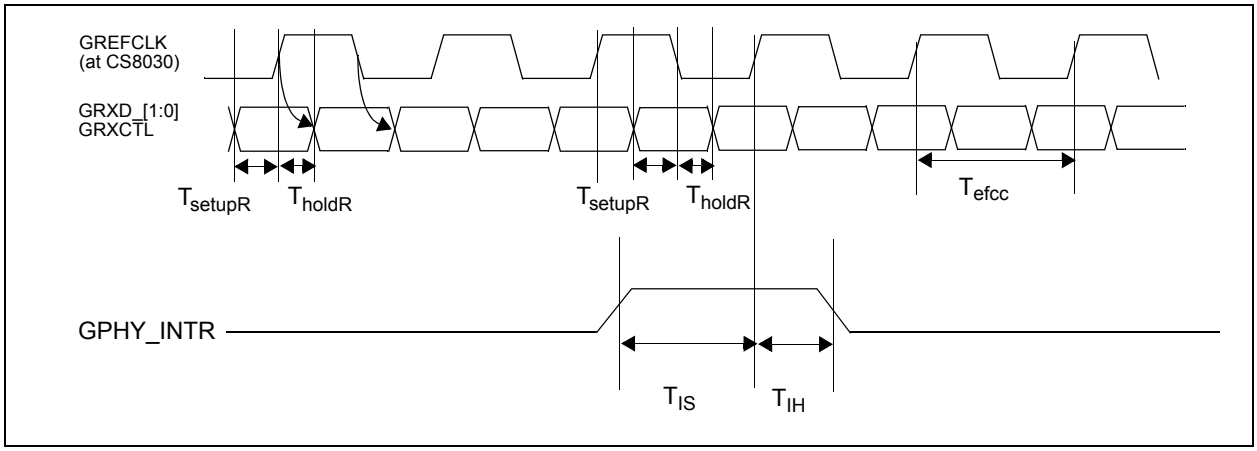


Figure 41 RMII Transmit Timing

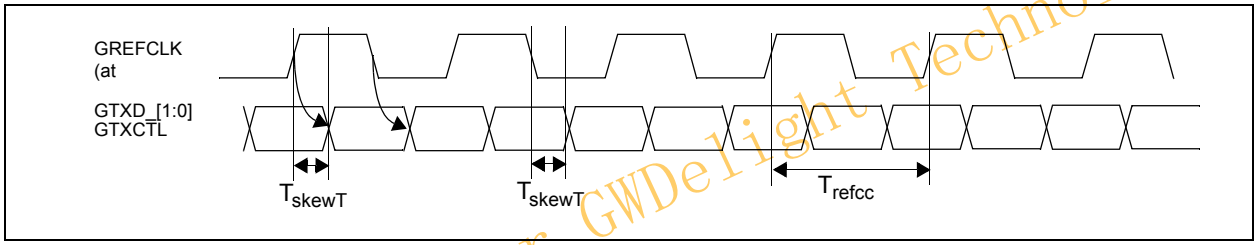


Table 41 RMII AC Characteristics

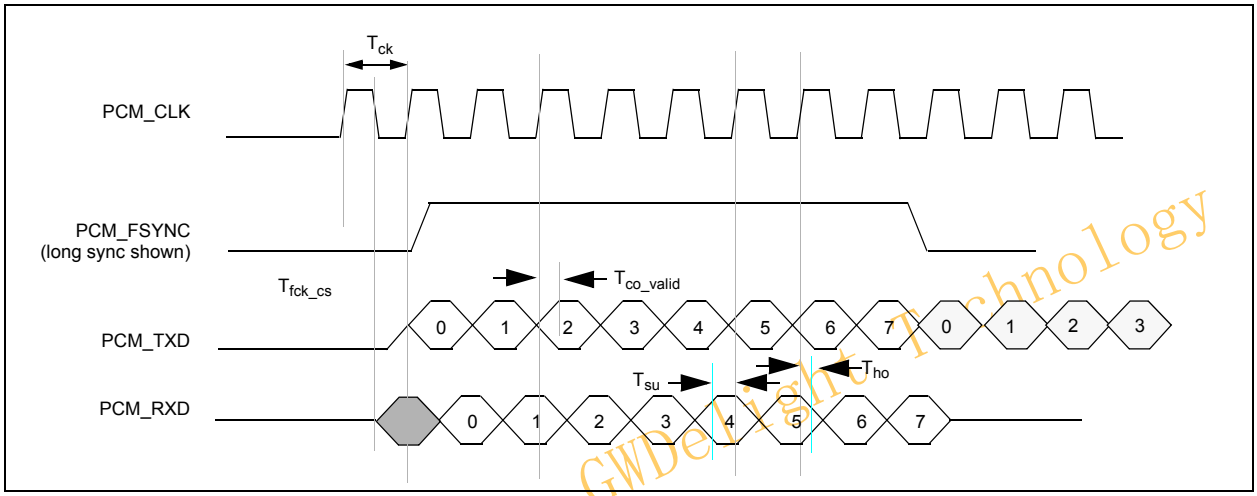
Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{refcc}	GREFCLK period	19.998	20	20.002	ns	50 MHz ±50 PPM (Figure 39)
Duty_R	GREFCLK duty cycle	45	50	55	%	—
T_{setupR}	GRXD_[1:0], GRXCTL Setup to GREFCLK rising edge	4	—	—	ns	Figure 40
T_{holdR}	GRXD_[1:0], GRXCTL hold from GREFCLK rising edge	2	—	—	ns	Figure 40
T_{skewT}	GTXD_[1:0] or GTXCTL data output to GREFCLK output Skew (at the CS8032/CS8033 EPON ONU)	-0.66	0	0.66	ns	Figure 41
Tr / Tf	rise/fall time	1	—	5	ns	0.8 V to 2.0 V level

10.5.6 PCM Interface

The PCM interface supports a standard TDM Highway interface to support VoIP connection to external SLIC/SLAC devices. The device operates with a serial clock of not more than 8.192 MHz. The serial interface speed is programmable and may be as low as 256 kHz.

The CS8032/CS8033 EPON ONU serial data is transferred on the rising edge of PCM_CLK. The interface protocol expects the SLAC device to transfer serial data on the falling edge of PCM_CLK. Figure 42 is the PCM interface timing diagram and Table 42 specifies the AC characteristics of the interface.

Figure 42 PCM Interface Timing Diagram



The timing requirements of the PCM interface are shown in Table 42.

Table 42 PCM Interface Requirements

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{ck}	External transfer clock cycle time	122	—	3900	ns	Period of the PCM_CLK reference clock signal is configured in the range of 256 kHz to 8.192 MHz by software running on the embedded ARM926EJ-S* Processor. The PCM_CLK reference clock is generated from the external 16.384 MHz crystal connected to the PCM_XIN and the PCM_XOUT pins.
T_{co_valid}	PCM_TXD valid time from rising edge of PCM_CLK	1	—	15	ns	—
T_{su}	PCM_RXD setup time to rising edge of PCM_CLK	15	—	—	ns	—
T_{ho}	PCM_RXD hold time from rising edge of PCM_PCLK	2	—	—	ns	—

10.5.7 MDC/MDIO Interface Timings

The MDC/MDIO interface is used for managing the GE and FE PHYs in a CS8032/CS8033 EPON ONU system. The interface is compliant with IEEE802.3 ([2] on page 86) Clause 28. Table 43 specifies the AC characteristics of the interface.

Table 43 MDIO Timing

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{co}	Output Data valid relative to rising edge of MDC	-10	—	+10	ns	Output data valid window
T_{su}	Input Data Setup	10	—	—	ns	Input setup relative to rising edge of MDC
T_{ho}	Input Data Hold	0	—	—	ns	Input hold relative to rising edge of MDC
T_{cyc}	MDC Clock cycle time	400	—	—	ns	—
T_{ck_pwh}	MDC Clock pulse width High	160	—	—	ns	—
T_{ck_pwl}	MDC Clock pulse width Low	160	—	1	ns	—

10.5.8 JTAG Interface Timings

Figure 43 JTAG Timing Diagram

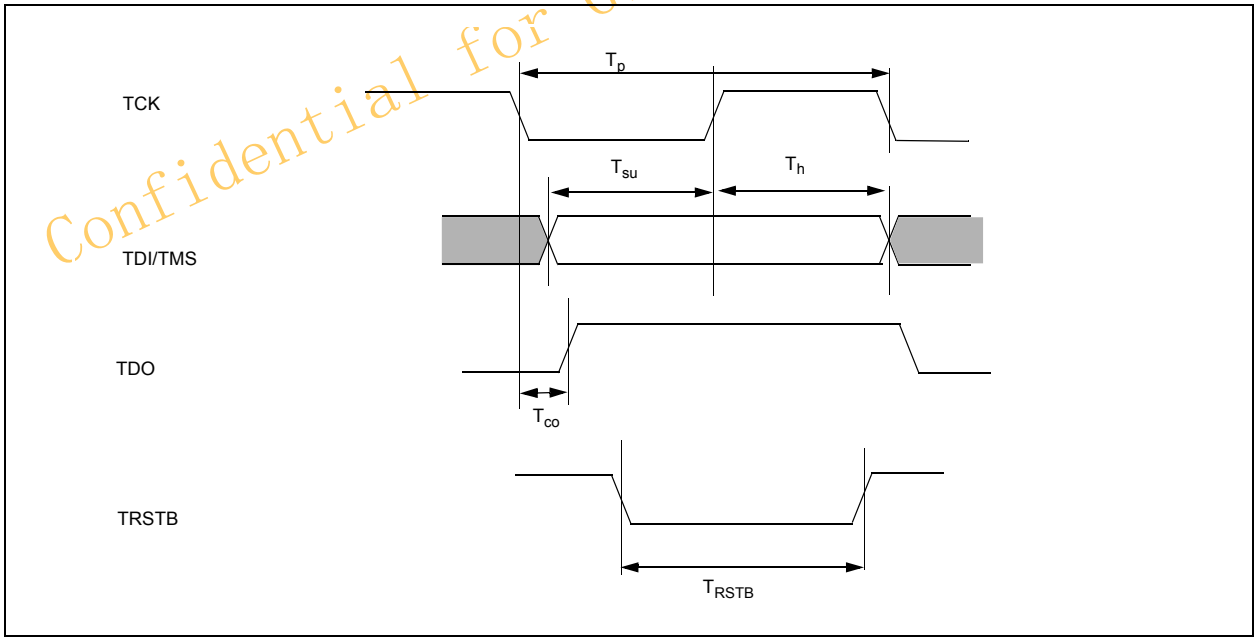


Table 44 JTAG Timing Requirements

Symbol	Parameter	Min	Typ	Max	Units
T_p	Serial Clock Period of TCK	100	—	—	ns
$T_{duty\text{-}cycle}$	Duty Cycle of TCK	40	—	60	%
T_{co}	TDO Clock to output	2	—	15	ns
T_{su}	TMS/TDI Setup	10	—	—	ns
T_h	TMS/TDI Hold Time	5	—	—	ns
T_{RSTB}	TRSTN Pulse Width	50	—	—	ns

10.5.9 RESETN Timing

Figure 44 RESETN Timing Diagram

Table 45 Miscellaneous Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{RSTP}	RESETN Pulse Width	1	—	—	ms

11.0 CS8032/CS8033 EPON ONU Ball List

Table 46 Ball List Sorted by Ball

Note: See Table 47, *Ball List Sorted by Signal Name*, on page 81 for the ball list sorted by signal name.

Ball	Signal Name
A1	SSP_CSN_2
A2	SSP_CSN_1
A3	SSP_RXD
A4	SSP_CLK
A5	PTP_PPS
A6	RMII_TXEN
A7	RMII_RXDV
A8	RMII_RXD_0
A9	RMII_RXD_1
A10	PCM_CLK
A11	PCM_RXD
A12	PCM_XOUT
A13	LPB_ADDR_04
A14	LPB_ADDR_09
A15	LPB_ADDR_06
B1	SSP_CSN_0
B2	SSP_TXD
B3	GPIO_00
B4	UART_TXD
B5	UART_RXD
B6	PTP_TOD
B7	RMII_TXD_0
B8	RMII_TXD_1
B9	RMII_REFCLK
B10	PCM_TXD
B11	PCM_XIN
B12	PCM_FSYNC
B13	LPB_ADDR_07
B14	LPB_ADDR_10
B15	LPB_ADDR_13
C1	GPIO_10
C2	GPIO_14
C3	LPB_ADDR_00
C4	LPB_ADDR_01
C5	LPB_ADDR_02
C6	LPB_ADDR_03
C7	LPB_ADDR_05
C8	LPB_ADDR_08
C9	LPB_ADDR_11
C10	LPB_ADDR_14
C11	LPB_ADDR_17
C12	LPB_ADDR_20
C13	LPB_ADDR_23
C14	LPB_ADDR_19
C15	LPB_ADDR_16
D1	GPIO_01
D2	GPIO_13
D3	BIWC
D4	VDD33
D5	GND1
D6	GND1
D7	VDD25A
D8	VDD25A
D9	GND1
D10	GND1
D11	VDD25A
D12	GND1
D13	LPB_ADDR_22
D14	LPB_ADDR_15
D15	LPB_ADDR_12
E1	GPIO_02
E2	GPIO_12
E3	BIWD
E4	VDD25A
E5	GND1
E6	GND1
E7	GND1
E8	GND1
E9	GND1
E10	GND1
E11	GND1
E12	VDD25A
E13	LPB_ADDR_24
E14	LPB_ADDR_21
E15	LPB_ADDR_18
F1	GPIO_15
F2	GPIO_11
F3	GPIO_08
F4	VDD25A
F5	GND1
F6	GND1
F7	VDD10A
F8	VDD10A
F9	VDD10A
F10	VDD10A
F11	GND1
F12	VDD25C
F13	LPB_ADDR_25
F14	LPB_XDATA_03
F15	LPB_XDATA_02
G1	GND1
G2	VDD25A
G3	GPIO_09
G4	VDD25A
G5	GND1
G6	GND1
G7	VDD10A
G8	VDD10A
G9	VDD10A
G10	VDD10A
G11	VDD25B
G12	VDD25C

G10	VDD10A
G11	VDD25B
G12	VDD25C

Ball	Signal Name
K4	VDD25A
K5	GND1
K6	VDD10A
K7	VDD10A
K8	VDD10A
K9	GND1
K10	GND1
K11	GND1
K12	TRSTN
K13	LPB_WEN
K14	LPB_XDATA_00
K15	LPB_XDATA_07
L1	GTXCTL
L2	GRXD_0
L3	GPIO_06
L4	TEST_MODE
L5	GND1
L6	GND1
L7	GND1
L8	GND1
L9	GND1
L10	THERMAL
L11	VDD25A
L12	VDD25A
L13	SDRAM_CSN
L14	LPB_XDATA_04
L15	LPB_XDATA_08
M1	GTXCLK
M2	GTXD_3
M3	GPIO_07
M4	VDD25A
M5	VDD25A
M6	GND
M7	VDD10B
M8	VDD10B
M9	NC
M10	GND1
M11	GND1
M12	VDD25A

Ball	Signal Name
M13	FLASH_CSN
M14	LPB_XDATA_05
M15	LPB_XDATA_09
N1	GTXD_2
N2	GTXD_1
N3	JTAG_MODE
N4	PLL_LOCK
N5	EXT_CLOCK_SEL
N6	VDD10B
N7	VDD10B
N8	VDD10B
N9	VDD10B
N10	VDD10B
N11	TDO
N12	TDI
N13	TMS
N14	LPB_XDATA_06
N15	LPB_OEN
P1	GTXD_0
P2	RESETN
P3	EXT_CLOCK
P4	AB_PLL_VDDA
P5	GND2
P6	ETX_N
P7	GND2
P8	ERX_N
P9	GND2
P10	CPLL_REFCLK_N
P11	ATST_REXT_VTOI
P12	TCK
P13	MDC
P14	CPD_DAT_EN_IN
P15	CPD_CLK_OUT
R1	GPHY_INTR
R2	ETX_BURST
R3	SYNC_CLKO
R4	AB_PLL_VSSA
R5	GND2
R6	ETX_P

Ball	Signal Name
R7	GND2
R8	ERX_P
R9	GND2
R10	CPLL_REFCLK_P
R11	REXT_PMC
R12	ERX_SIGLOSS
R13	MDIO
R14	CPD_CLK_FB_IN
R15	CPD_DAT_EN_OUT

Table 47 Ball List Sorted by Signal Name

Note: See Table 46, *Ball List Sorted by Ball*, on page 79 for the ball list sorted by ball.

Signal Name	Ball
ATST_REXT_VTOI	P11
REXT_PMC	R11
AB_PLL_VDDA	P4
AB_PLL_VSSA	R4
BIWC	D3
BIWD	E3
CPD_CLK_FB_IN	R14
CPD_CLK_OUT	P15
CPD_DAT_EN_IN	P14
CPD_DAT_EN_OUT	R15
CPLL_REFCLK_N	P10
CPLL_REFCLK_P	R10
ERX_N	P8
ERX_P	R8
ERX_SIGLOSS	R12
ETX_BURST	R2
ETX_N	P6
ETX_P	R6
EXT_CLOCK	P3
EXT_CLOCK_SEL	N5
FLASH_CSN	M13
GND	M6
GND1	D10
GND1	D12
GND1	D5

Signal Name	Ball
GND1	D6
GND1	D9
GND1	E10
GND1	E11
GND1	E5
GND1	E6
GND1	E7
GND1	E8
GND1	E9
GND1	F11
GND1	F5
GND1	F6
GND1	G1
GND1	G15
GND1	G5
GND1	G6
GND1	H12
GND1	H5
GND1	J12
GND1	J5
GND1	K10
GND1	K11
GND1	K5
GND1	K9
GND1	L5

Signal Name	Ball
GND1	L6
GND1	L7
GND1	L8
GND1	L9
GND1	M10
GND1	M11
GND2	P5
GND2	P7
GND2	P9
GND2	R5
GND2	R7
GND2	R9
GPHY_INTR	R1
GPIO_00	B3
GPIO_01	D1
GPIO_02	E1
GPIO_03	H3
GPIO_04	J3
GPIO_05	K3
GPIO_06	L3
GPIO_07	M3
GPIO_08	F3
GPIO_09	G3
GPIO_10	C1
GPIO_11	F2

Signal Name	Ball
GPIO_12	E2
GPIO_13	D2
GPIO_14	C2
GPIO_15	F1
GREFCLK	H1
GRXCLK	J1
GRXCTL	K1
GRXD_0	L2
GRXD_1	K2
GRXD_2	J2
GRXD_3	H2
GTXCLK	M1
GTXCTL	L1
GTXD_0	P1
GTXD_1	N2
GTXD_2	N1
GTXD_3	M2
JTAG_MODE	N3
LPB_ADDR_00	C3
LPB_ADDR_01	C4
LPB_ADDR_02	C5
LPB_ADDR_03	C6
LPB_ADDR_04	A13
LPB_ADDR_05	C7
LPB_ADDR_06	A15
LPB_ADDR_07	B13
LPB_ADDR_08	C8
LPB_ADDR_09	A14
LPB_ADDR_10	B14
LPB_ADDR_11	C9
LPB_ADDR_12	D15
LPB_ADDR_13	B15
LPB_ADDR_14	C10
LPB_ADDR_15	D14
LPB_ADDR_16	C15
LPB_ADDR_17	C11
LPB_ADDR_18	E15
LPB_ADDR_19	C14
LPB_ADDR_20	C12

Signal Name	Ball
LPB_ADDR_21	E14
LPB_ADDR_22	D13
LPB_ADDR_23	C13
LPB_ADDR_24	E13
LPB_ADDR_25	F13
LPB_OEN	N15
LPB_WEN	K13
LPB_XDATA_00	K14
LPB_XDATA_01	J14
LPB_XDATA_02	F15
LPB_XDATA_03	F14
LPB_XDATA_04	L14
LPB_XDATA_05	M14
LPB_XDATA_06	N14
LPB_XDATA_07	K15
LPB_XDATA_08	L15
LPB_XDATA_09	M15
LPB_XDATA_10	H14
LPB_XDATA_11	H15
LPB_XDATA_12	J15
LPB_XDATA_13	G13
LPB_XDATA_14	H13
LPB_XDATA_15	J13
MDC	P13
MDIO	R13
NC	M9
PCM_CLK	A10
PCM_FSYNC	B12
PCM_RXD	A11
PCM_TXD	B10
PCM_XIN	B11
PCM_XOUT	A12
PLL_LOCK	N4
PTP_PPS	A5
PTP_TOD	B6
RESETN	P2
RMII_REFCLK	B9
RMII_RXD_0	A8
RMII_RXD_1	A9

Signal Name	Ball
RMII_RXDV	A7
RMII_TXD_0	B7
RMII_TXD_1	B8
RMII_TXEN	A6
SDRAM_CSN	L13
SSP_CLK	A4
SSP_CSN_0	B1
SSP_CSN_1	A2
SSP_CSN_2	A1
SSP_RXD	A3
SSP_TXD	B2
SYNC_CLKO	R3
TCK	P12
TDI	N12
TDO	N11
TEST_MODE	L4
THERMAL	L10
TMS	N13
TRSTN	K12
UART_RXD	B5
UART_TXD	B4
VDD10A	F10
VDD10A	F7
VDD10A	F8
VDD10A	F9
VDD10A	G10
VDD10A	G7
VDD10A	G8
VDD10A	G9
VDD10A	H10
VDD10A	H6
VDD10A	H7
VDD10A	H8
VDD10A	H9
VDD10A	J10
VDD10A	J6
VDD10A	J7
VDD10A	J8
VDD10A	J9

Signal Name	Ball
VDD10A	K6
VDD10A	K7
VDD10A	K8
VDD10B	M7
VDD10B	M8
VDD10B	N10
VDD10B	N6
VDD10B	N7
VDD10B	N8
VDD10B	N9
VDD25A	D11
VDD25A	D7
VDD25A	D8
VDD25A	E12
VDD25A	E4
VDD25A	F4
VDD25A	G14
VDD25A	G2
VDD25A	G4
VDD25A	J4
VDD25A	K4
VDD25A	L11
VDD25A	L12
VDD25A	M12
VDD25A	M4
VDD25A	M5
VDD25B	G11
VDD25B	H11
VDD25B	J11
VDD25C	F12
VDD25C	G12
VDD25C	H4
VDD33	D4

12.0 CS8032/CS8033 EPON ONU Ball Map (Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1	SSP_CSN_2	SSP_CSN_0	GPIO_10	GPIO_01	GPIO_02	GPIO_15	GND1	GREFCLK	GRXCLK	GRXCTL	GTXCTL	GTXCLK	GTXD_2	GTXD_0	GPHY_INTR	1
2	SSP_CSN_1	SSP_TXD	GPIO_14	GPIO_13	GPIO_12	GPIO_11	VDD25A	GRXD_3	GRXD_2	GRXD_1	GRXD_0	GTXD_3	GTXD_1	RESETN	ETX_BURST	2
3	SSP_RXD	GPIO_00	LPB_ADDR_00	BIWC	BIWD	GPIO_08	GPIO_09	GPIO_03	GPIO_04	GPIO_05	GPIO_06	GPIO_07	JTAG_MODE	EXT_CLOCK	SYNC_CLKO	3
4	SSP_CLK	UART_TXD	LPB_ADDR_01	VDD33	VDD25A	VDD25A	VDD25A	VDD25C	VDD25A	VDD25A	TEST_MODE	VDD25A	PLL_LOCK	AB_PLL_VDDA	AB_PLL_VSSA	4
5	PTP_PPS	UART_RXD	LPB_ADDR_02	GND1	GND1	GND1	GND1	GND1	GND1	GND1	GND1	VDD25A	EXT_CLOCK_SEL	GND2	GND2	5
6	RMII_TXEN	PTP_TOD	LPB_ADDR_03	GND1	GND1	GND1	GND1	VDD10A	VDD10A	VDD10A	GND1	GND	VDD10B	ETX_N	ETX_P	6
7	RMII_RXDV	RMII_TXD_0	LPB_ADDR_05	VDD25A	GND1	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	GND1	VDD10B	VDD10B	GND2	GND2	7
8	RMII_RXD_0	RMII_TXD_1	LPB_ADDR_08	VDD25A	GND1	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	GND1	VDD10B	VDD10B	ERX_N	ERX_P	8
9	RMII_RXD_1	RMII_REFCLK	LPB_ADDR_11	GND1	GND1	VDD10A	VDD10A	VDD10A	VDD10A	GND1	GND1	NC	VDD10B	GND2	GND2	9
10	PCM_CLK	PCM_TXD	LPB_ADDR_14	GND1	GND1	VDD10A	VDD10A	VDD10A	VDD10A	GND1	THERMAL	GND1	VDD10B	CPLL_REFCLK_N	CPLL_REFCLK_P	10
11	PCM_RXD	PCM_XIN	LPB_ADDR_17	VDD25A	GND1	GND1	VDD25B	VDD25B	VDD25B	GND1	VDD25A	GND1	TDO	ATST_REXT_VTOI	REXT_PMC	11
12	PCM_XOUT	PCM_FSYNC	LPB_ADDR_20	GND1	VDD25A	VDD25C	VDD25C	GND1	GND1	TRSTN	VDD25A	VDD25A	TDI	TCK	ERX_SIGLOSS	12
13	LPB_ADDR_04	LPB_ADDR_07	LPB_ADDR_23	LPB_ADDR_22	LPB_ADDR_24	LPB_ADDR_25	LPB_XDATA_13	LPB_XDATA_14	LPB_XDATA_15	LPB_WEN	SDRAM_CSN	FLASH_CSN	TMS	MDC	MDIO	13
14	LPB_ADDR_09	LPB_ADDR_10	LPB_ADDR_19	LPB_ADDR_15	LPB_ADDR_21	LPB_XDATA_03	VDD25A	LPB_XDATA_10	LPB_XDATA_01	LPB_XDATA_00	LPB_XDATA_04	LPB_XDATA_05	LPB_XDATA_06	CPD_DAT_EN_IN	CPD_CLK_FB_IN	14
15	LPB_ADDR_06	LPB_ADDR_13	LPB_ADDR_16	LPB_ADDR_12	LPB_ADDR_18	LPB_XDATA_02	GND1	LPB_XDATA_11	LPB_XDATA_12	LPB_XDATA_07	LPB_XDATA_08	LPB_XDATA_09	LPB_OEN	CPD_CLK_OUT	CPD_DAT_EN_OUT	15
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

13.0 Terminology

FTTH	FIber to the Home
OLT	Optical Line Terminal
ONU	Optical Network Unit
iROS™	Cortina Systems® intelligent Real-time Operating System
UNI	User Network Interface
NNI	Network Node Interface
MAC	Media Access Control
PCS	PHYsical Coding Sublayer
FEC	Forward Error Correction
LLID	Logical Link Identifier
DPID	Destination Port Identifier
SPID	Source Port Identifier
OAM	Operation, Administration, and Maintenance
IVL	Independent VLAN Learning
ACL	Access Control List
DBA	Dynamic Bandwidth Allocation
DSCP	DiffServ Code Points
IGMP	Internet Group Multicast Protocol
MDU	Multi-dwelling Unit
MLD	Multicast Listener Discovery
PCM	Pulse Code Modulation
SFU	Single Family Unit
SiP	System-in-Package
SIP	Session Initiation Protocol
SVL	Shared VLAN Learning
VoIP	Voice over IP
SLAC	Subscriber Line Access Controller
SLIC	Subscriber Line Interface Controller

14.0 References

Please refer to the following:

[1] China Mobile: Specification on TD Wireless System High Precision Timing Synchronization Features, Functions and Timing Interface Technology

[2] IEEE802.3-2008

[3] Reduced Gigabit Media Independent Interface (RGMII) Version 2.0 (http://www.hp.com/rnd/pdfs/RGMIIv2_0_final_hp.pdf)

[4] RMII™ Specification Rev 1.2 (http://www.national.com/appinfo/networks/files/rmii_1_2.pdf)

[5] IEEE1588-2008

[6] IEEE802.1AS- Draft 7.0

[7] China Telecom's Technical Requirement of EPON Equipment v2.1 (December 2009)

[8] IEEE802.3az Draft 3.1

For additional product and ordering information:

www.cortina-systems.com