

# Zhao Xia

Electronics and Information Systems Department  
Ghent University  
Gent, Belgium

Office: Technologiepark 15  
Email: xia.zhao@ugent.be  
Homepage: <http://zhaoxiahust.github.io/>

## Education

Ph.D. Candidate in Electronics and Information Systems Department, Ghent University

M.S. Computer Science and Technology, National University of Defense Technology, 2014.

*GPA:* Top 2% All Core Courses are A.

*Dissertation:* “Parallel GPGPU Simulator and a Low-Cost NoC Design”.

*Supervisor:* Prof. Zhiying Wang, Ass.Prof. Sheng Ma

B.S. Computer Science and Technology, Huazhong University of Science and Technology, 2012.

*GPA:* Top 5%

## Research Interest

My research interests include GPGPU architecture in general, and multi-program execution and Network-on-Chip (NoC) design more in particular..

## Research Experience

Ghent University, System Performance Lab

Research Assistant, September 2015–present.

National University of Defense Technology, Computer Architecture Group

Research Assistant, September 2012– May 2015.

Huazhong University of Science and Technology, SCTS Lab

Research Assistant, September 2011–May 2012.

## Research

### *Conference Publications*

1. **Xia Zhao**, Zhiying Wang, Lieven Eeckhout. Classification-Driven Search for Effective SM Partitioning in GPU Multitasking. *32nd ACM International Conference on Supercomputing (ICS)*, 2018
2. Yuxi Liu, **Xia Zhao**, Magnus Jahre, Zhenlin Wang, Xiaolin Wang, Yingwei Luo, Lieven Eeckhout. Get Out of the Valley: Power-Efficient Address Mapping for GPUs. *45th International Symposium on Computer Architecture (ISCA)*, 2018.
3. Lu Wang, **Xia Zhao**, David Kaeli, Zhiying Wang, Lieven Eeckhout. Intra-Cluster Coalescing to Reduce GPU NoC Pressure. *32nd IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, 2018.
4. Yuxi Liu, **Xia Zhao**, Zhibin Yu, Zhenlin Wang, Xiaolin Wang, Yingwei Luo, Lieven Eeckhout. BACM: Barrier-Aware Cache Management for Irregular Memory-Intensive GPGPU Workloads. *35th IEEE International Conference on Computer Design (ICCD)*, 2017.

5. Yuxi Liu, **Xia Zhao**, Zhibin Yu, Zhenlin Wang, Xiaolin Wang, Yingwei Luo, Lieven Eeckhout. BACM: Barrier-Aware Cache Management for Irregular Memory-Intensive GPGPU Workloads. *26th IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT)*, 2017 (Poster).
6. Chen Li, Sheng Ma, Lu Wang, Zicong Wang, **Xia Zhao**, Yang Guo. DLL: A Dynamic Latency-Aware Load-Balancing Strategy in 2.5D NoC Architecture. *34th IEEE International Conference on Computer Design (ICCD)*, 2016.
7. **Xia Zhao**, Sheng Ma, Chen Li, Lieven Eeckhout, Zhiying Wang. (2016). A Heterogeneous Low-Cost and Low-Latency Ring-Chain Network for GPGPUs. *34th IEEE International Conference on Computer Design (ICCD)*, 2016.
8. **Xia Zhao**, Sheng Ma, Yuxi Liu, Lieven Eeckhout, Zhiying Wang. (2016). A Low-Cost Conflict-Free NoC for GPGPUs. *53rd Design Automation Conference (DAC)*, 2016 (HiPEAC Paper Award).
9. **Xia Zhao**, Li Shen, Xin Liu, Zhiying Wang. (2014). Parallelization of GPU Simulator on Multi-core Platforms. *Advanced Computer Architecture (ACA)*, 2014 (Best Student Paper Award).

### *Journal Publications*

10. **Xia Zhao**, Yuxi Liu, Almutaz Adileh, Lieven Eeckhout. LA-LLC: Inter-Core Locality-Aware Last-Level Cache To Exploit Many-to-Many Traffic in GPGPUs. *IEEE Computer Architecture Letters (CAL)*, 2017
11. **Xia Zhao**, Sheng Ma, Wei Chen and Zhiying Wang. Exploiting Parallelism in the Simulation of GPGPU Program. *Journal of shanghai Jiaotong University (Science)*, 2015

### Grants, Fellowships, & Awards

ACACES Summer School Grant, HiPEAC, 2017

HiPEAC Paper Award, HiPEAC, 2017

Special Research Fund, Ghent University, 2016

CSC scholarship, China Scholarship Council, 2015

Best Student Paper, Advanced Computer Architecture, 2014 (2/67)

National Second Award, National Postgraduate Mathematic Contest in Modeling, 2013

The Excellent Graduate, HuaZhong University of Science and Technology, 2012

National Encouragement scholarship, HuaZhong University of Science and Technology, 2012 (2%)

National Scholarship, HuaZhong University of Science and Technology, 2011 (1%)

Merit Student, HuaZhong University of Science and Technology, 2011

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