Genesys Logic, Inc.

GL850G

USB 2.0 Hub Controller

Datasheet

Revision 1.28
Dec. 21, 2016

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1.27	12/24/2013	Updated CH2 Features, p.10
1.28	12/21/2016	Modify 3.3 Pin Descriptions

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CHAPTER 1 GENERAL DESCRIPTION

GL850G is Genesys Logic's advanced version hub solutions which fully comply with Universal Serial Bus Specification Revision 2.0. GL850G inherits Genesys Logic's cutting edge technology on cost and power efficient serial interface design. GL850G has proven compatibility, lower power consumption figure and better cost structure above all USB2.0 hub solutions worldwide.

GL850G provides multiple advantages to simplify board level design that help achieve lowest BOM (Bill of Material) for system integrator. GL850G integrated both 5V to 3.3V and 3.3V to 1.8V voltage drop regulator into single chip, therefore no external LDO required. Also, GL850G's power enable pin supports both high-enable and low-enable power switch that provides better flexibility on component selection.

GL850G embeds an 8-bit RISC processor to manipulate the control/status registers and respond to the requests from USB host. Firmware of GL850G will control its general purpose I/O (GPIO) to access the external EEPROM and then respond to the host the customized PID and VID configured in the external EEPROM. Default settings in the internal mask ROM is responded to the host without having external EEPROM. GL850G is designed for customers with much flexibility. The more complicated settings such as PID, VID, and number of downstream ports settings are easily achieved by programming the external EEPROM (Ref. to Chapter 5).

Each downstream port of GL850G supports two-color (green/amber) status LEDs to indicate normal/abnormal status. GL850G also support both Individual and Gang modes (4 ports as a group) for power management. The GL850G is a full function solution which supports both Individual/Gang power management modes and the two-color (green/amber) status LEDs. Please refer the table in the end of this chapter for more detail. Number of downstream ports setting can be configured by IO setting in absence of EEPROM. (Ref. to Chapter 5)

To fully meet the cost/performance requirement, GL850G is a single TT hub solution for the cost requirement. Genesys Logic also provides GL852G for multiple TT hub solution to target on systems which require higher performance for full/low-speed devices, like docking station, embedded system … etc.. Please refer to GL852G datasheet for more detailed information.

*TT (transaction translator) is the main traffic control engine in an USB 2.0 hub to handle the unbalanced traffic speed between the upstream port and the downstream ports.

CHAPTER 2 FEATURES

- Compliant to USB Specification Revision 2.0
  - Support 4/3/2 downstream ports by I/O pin configuration
  - Upstream port supports both high-speed (HS) and full-speed (FS) traffic
  - Downstream ports support HS, FS, and low-speed (LS) traffic
  - 1 control pipe (endpoint 0, 64-byte data payload) and 1 interrupt pipe (endpoint 1, 1-byte data payload)
  - Backward compatible to *USB specification Revision 1.1*
- On-chip 8-bit micro-processor
  - RISC-like architecture
  - USB optimized instruction set
  - Performance: 6 MIPS @ 12MHz
  - With 64-byte RAM and 2K mask ROM
  - Support customized PID, VID by reading external EEPROM
  - Support downstream port configuration by reading external EEPROM
- Single Transaction Translator (STT)
  - Single TT shares the same TT control logics for all downstream port devices. This is the most cost effective solution for TT. Multiple TT provides individual TT control logics for each downstream port. This is a performance better choice for USB 2.0 hub. Please refer to GL852G datasheet for more detailed information.
- Integrate USB 2.0 transceiver
- Built-in upstream 1.5KΩ pull-up and downstream 15KΩ pull-down
- Embed serial resister for USB signals
- Conform to bus power requirements
- Automatic switching between self-powered and bus-powered modes
- Support compound-device (non-removable in downstream ports) by I/O pin configuration
- Configurable non-removable device support
- Built-in PLL supports external 12 MHz crystal / Oscillator clock input
- Built-in 5V to 3.3V regulator
- Low power consumption
- Improve output drivers with slew-rate control for EMI reduction
- Internal power-fail detection for ESD recovery
- ESD protection up to 4KV of HBM by MIL-STD-883H standard on all USB pins.
- Each downstream port supports two-color status indicator, with automatic and manual modes compliant to USB specification Revision 2.0 (Not available for SSOP 28 package)
- Support both individual and gang modes of power management and over-current detection for downstream ports (Individual mode is not supported by SSOP 28 package)
- Power enable pin supports both low/high-enabled power switches. (Power switch is not supported by GL850G-22 SSOP28 package)
- Optional 27/48 MHz Oscillator clock input (Not available for QFN28 / SSOP28 package)
- Number of Downstream port can be configured by GPIO without external EEPROM
- Available package type: 48 pin LQFP, 28 pin QFN and 28 pin SSOP (Full Function only available in 48 pin)
- Applications:
  - Stand-alone USB hub
  - PC motherboard USB hub, Docking of notebook
  - Gaming console

- LCD monitor hub
- Any compound device to support USB hub function

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

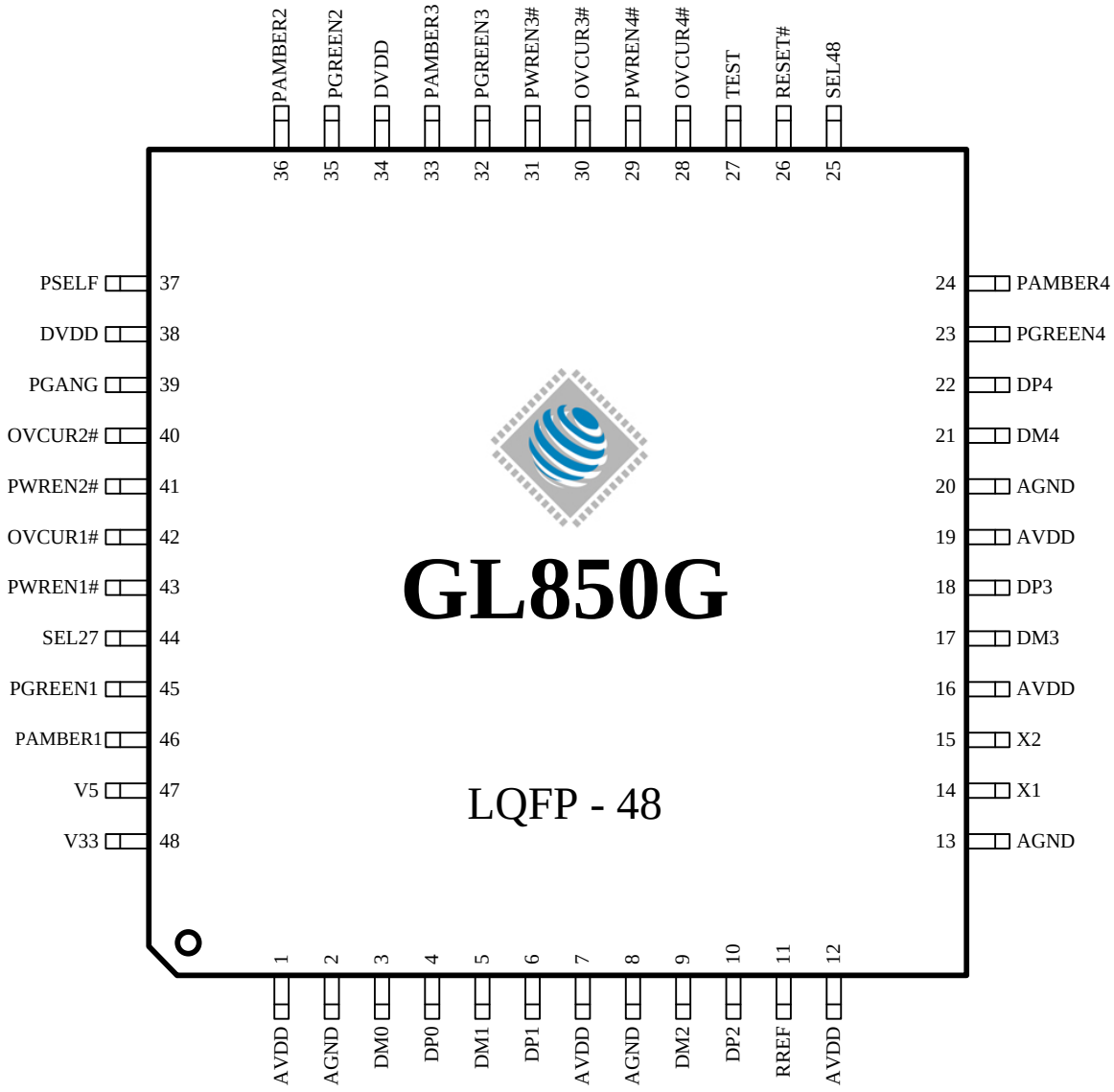


Figure 3.1 - GL850G LQFP 48 Pin Pinout Diagram

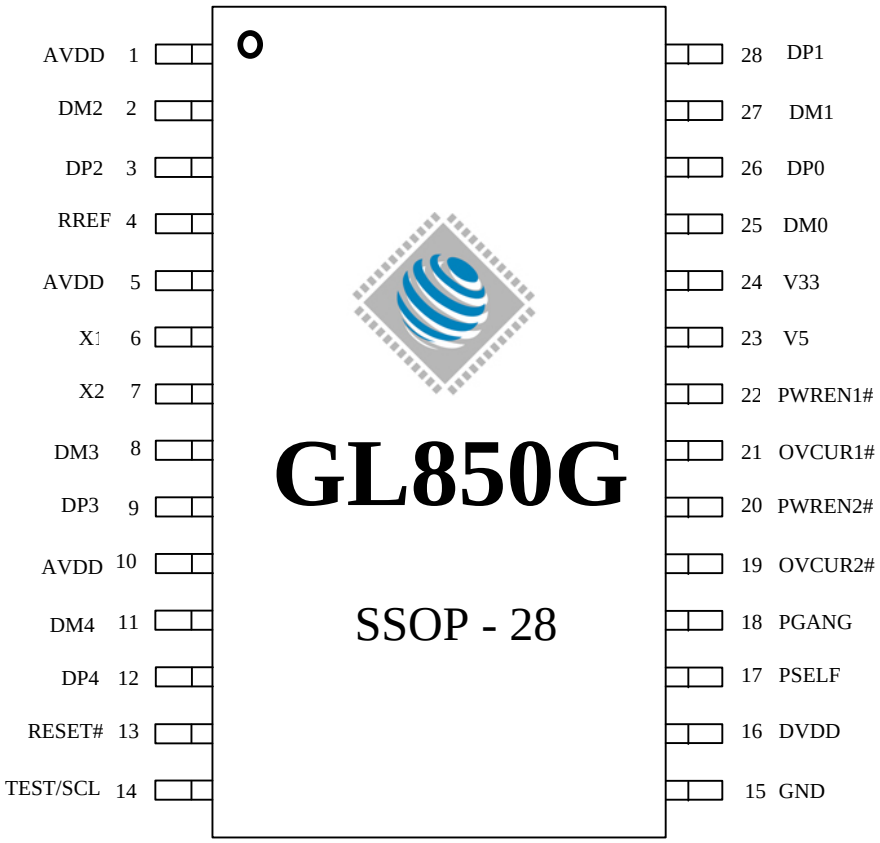


Figure 3.2 - GL850G SSOP 28 Pin Pinout Diagram

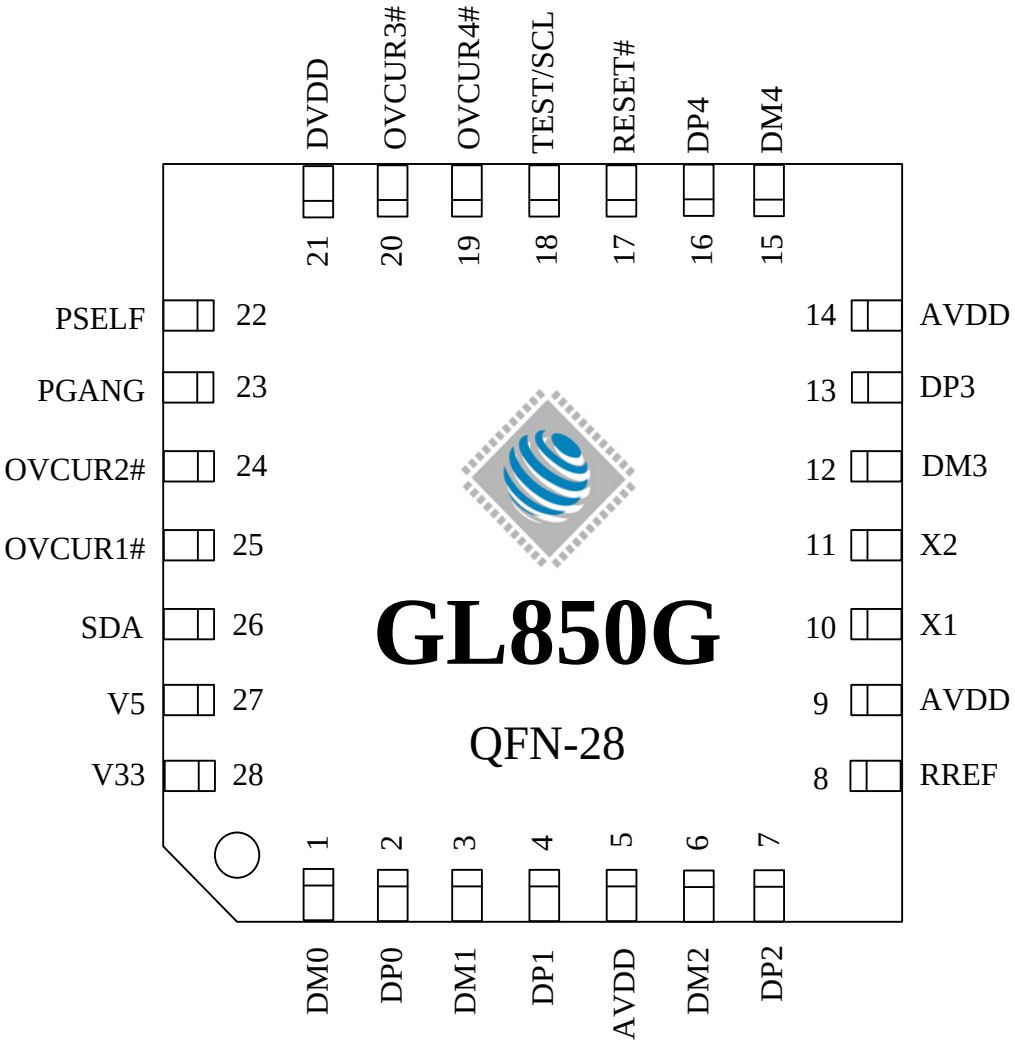


Figure 3.3 - GL850G QFN 28 Pin Pinout Diagram

3.2 Pin List

Table 3.1 - GL850G LQFP 48 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	AVDD	P	13	AGND	P	25	SEL48	I	37	PSELF	I_5V
2	AGND	P	14	X1	I	26	RESET#	I_5V	38	DVDD	P
3	DM0	B	15	X2	O	27	TEST	I	39	PGANG	B
4	DP0	B	16	AVDD	P	28	OVCUR4#	I_5V	40	OVCUR2#	I_5V
5	DM1	B	17	DM3	B	29	PWREN4#	O	41	PWREN2#	O
6	DP1	B	18	DP3	B	30	OVCUR3#	I_5V	42	OVCUR1#	I_5V
7	AVDD	P	19	AVDD	P	31	PWREN3#	O	43	PWREN1#	O
8	AGND	P	20	AGND	P	32	PGREEN3	O	44	SEL27	I
9	DM2	B	21	DM4	B	33	PAMBER3	O	45	PGREEN1	O
10	DP2	B	22	DP4	B	34	DVDD	P	46	PAMBER1	O
11	RREF	A	23	PGREEN4	O	35	PGREEN2	O	47	V5	P
12	AVDD	P	24	PAMBER4	O	36	PAMBER2	O	48	V33	P

Table 3.2 - GL850G SSOP 28 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	AVDD	P	8	DM3	B	15	GND	P	22	PWREN1#	O
2	DM2	B	9	DP3	B	16	DVDD	P	23	V5	P
3	DP2	B	10	AVDD	P	17	PSELF	I_5V	24	V33	P
4	RREF	A	11	DM4	B	18	PGANG	B	25	DM0	B
5	AVDD	P	12	DP4	B	19	OVCUR2#	I_5V	26	DP0	B
6	X1	I	13	RESET#	I_5V	20	PWREN2#*	O	27	DM1	B
7	X2	O	14	TEST/SCL	I/B	21	OVCUR1#*	I_5V	28	DP1	B

* Power switch is not supported in GL850G-22 version.

Table 3.3 - GL850G QFN 28 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DM0	B	8	RREF	A	15	DM4	B	22	PSELF	I_5V
2	DP0	B	9	AVDD	P	16	DP4	B	23	PGANG	B
3	DM1	B	10	X1	I	17	RESET#	I_5V	24	OVCUR2#	I_5V
4	DP1	B	11	X2	O	18	TEST/SCL	I/B	25	OVCUR1#	I_5V
5	AVDD	P	12	DM3	B	19	OVCUR4#	I_5V	26	SDA	B
6	DM2	B	13	DP3	B	20	OVCUR3#	I_5V	27	V5	P
7	DP2	B	14	AVDD	P	21	DVDD	P	28	V33	P

3.3 Pin Descriptions

Table 3.4 - Pin Descriptions

USB Interface					
Pin Name	**GL850G**			**I/O Type**	**Description**
	LQFP 48 Pin	**SSOP 28 Pin**	**QFN 28 Pin**		
DM0,DP0	3,4	25,26	1,2	B	USB signals for USPORT
DM1,DP1	5,6	27,28	3,4	B	USB signals for DSPORT1
DM2,DP2	9,10	2,3	6,7	B	USB signals for DSPORT2
DM3,DP3	17,18	8,9	12,13	B	USB signals for DSPORT3
DM4,DP4	21,22	11,12	15,16	B	USB signals for DSPORT4
RREF	11	4	8	A	A 680Ω resister must be connected between RREF and analog ground (AGND)

Note: USB signals must be carefully handled in PCB routing. For detailed information, please refer to **USB 2.0 Hub Design Guide**.

Hub Interface					
Pin Name	**GL850G**			**I/O Type**	**Description**
	LQFP 48 Pin	**SSOP 28 Pin**	**QFN 28 Pin**		
OVCUR1~4#	42,40, 30,28	21,19	25,24, 20,19	I_5V	Active low. Over current indicator for DSPORT1~4. *Over current flag On when OVCUR= low over 3ms. OVCUR1# is the only over current flag for GANG mode
PWREN1~4#	43,41, 31,29	22,20	--	O	Active low. Power enable output for DSPORT1~4 PWREN1# is the only power-enable output for GANG mode * Power switch is not supported in GL850G-22 version.
PGREEN1~4	45,35, 32,23	--	--	1,3,4:O 2:B (pd)	Green LED indicator for DSPORT1~4 *GREEN[1~2] are also used to access the external EEPROM For detailed information, please refer to Chapter 5
PAMBER1~4	46,36, 33,24	--	--	O (pd)	Amber LED indicator for DSPORT1~4 *Amber[1~2] are also used to access the external EEPROM For detailed information, please refer to Chapter 5
PSELF	37	17	22	I_5V	0: GL850G is bus-powered 1: GL850G is self-powered

PGANG	39	18	23	B	This pin is default put in input mode after power-on reset. Individual/gang mode is strapped during this period. After the strapping period, this pin will be set to output mode, and then output high for normal mode. When GL850G is suspended, this pin will output low. *For detailed explanation, please see Chapter 5 Gang input:1, output: 0@normal, 1@suspend Individual input:0, output: 1@normal, 0@suspend

Clock and Reset Interface					
Pin Name	GL850G			I/O Type	Description
	LQFP 48 Pin	SSOP 28 Pin	QFN 28 Pin		
X1	14	6	10	I	12MHz crystal clock input, or 12/27/48MHz clock input
X2	15	7	11	O	12MHz crystal clock output
RESET#	26	13	17	I_5V	Active low. External reset input, default pull high 10KΩ When RESET# = low, whole chip is reset to the initial state
SEL48/SEL27	25,44	--	--	I	SEL48/SEL27: 0 1: 48MHz OSC-in 1 0: 27MHz OSC-in 1 1: 12MHz X'tal/OSC-in

System Interface					
Pin Name	GL850G			I/O Type	Description
	LQFP 48 Pin	SSOP 28 Pin	QFN 28 Pin		
TEST/SCL	27	14	18	I (pd) B	TEST: 0: Normal operation. (Internal pull down) 1: Chip will be put in test mode. I2C:clock output pin (SSOP 28pin/QFN 28pin only)
SDA	--	--	26	B	I2C: data pin

Power / Ground					
Pin Name	GL850G			I/O Type	Description
	LQFP 48 Pin	SSOP 28 Pin	QFN 28 Pin		
AVDD	1,7,12, 16,19	1,5,10	5,9,14	P	3.3V analog power input for analog circuits

AGND	2,8,13, 20	--	--	P	Analog ground input for analog circuits
DVDD	34,38	16	21	P	3.3V digital power input for digital circuits
GND	--	15	--		Ground
V5	47	23	27	P	5V Power input. It need be NC if using external regulator
V33	48	24	28	P	5V-to-3.3V regulator Vout (LQFP48) 5V-to-3.3V regulator Vout & 3.3 input (SSOP28/QFN28) It can be NC or connect to 3.3V power if using external regulator (LQFP48 only)

Note: Analog circuits are quite sensitive to power and ground noise. PCB layout must take care the power routing and the ground plane. For detailed information, please refer to **USB 2.0 Hub Design Guide**.

Notation:

Type	**O**	Output
	I	Input
	I_5V	5V tolerant input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

CHAPTER 4 BLOCK DIAGRAM

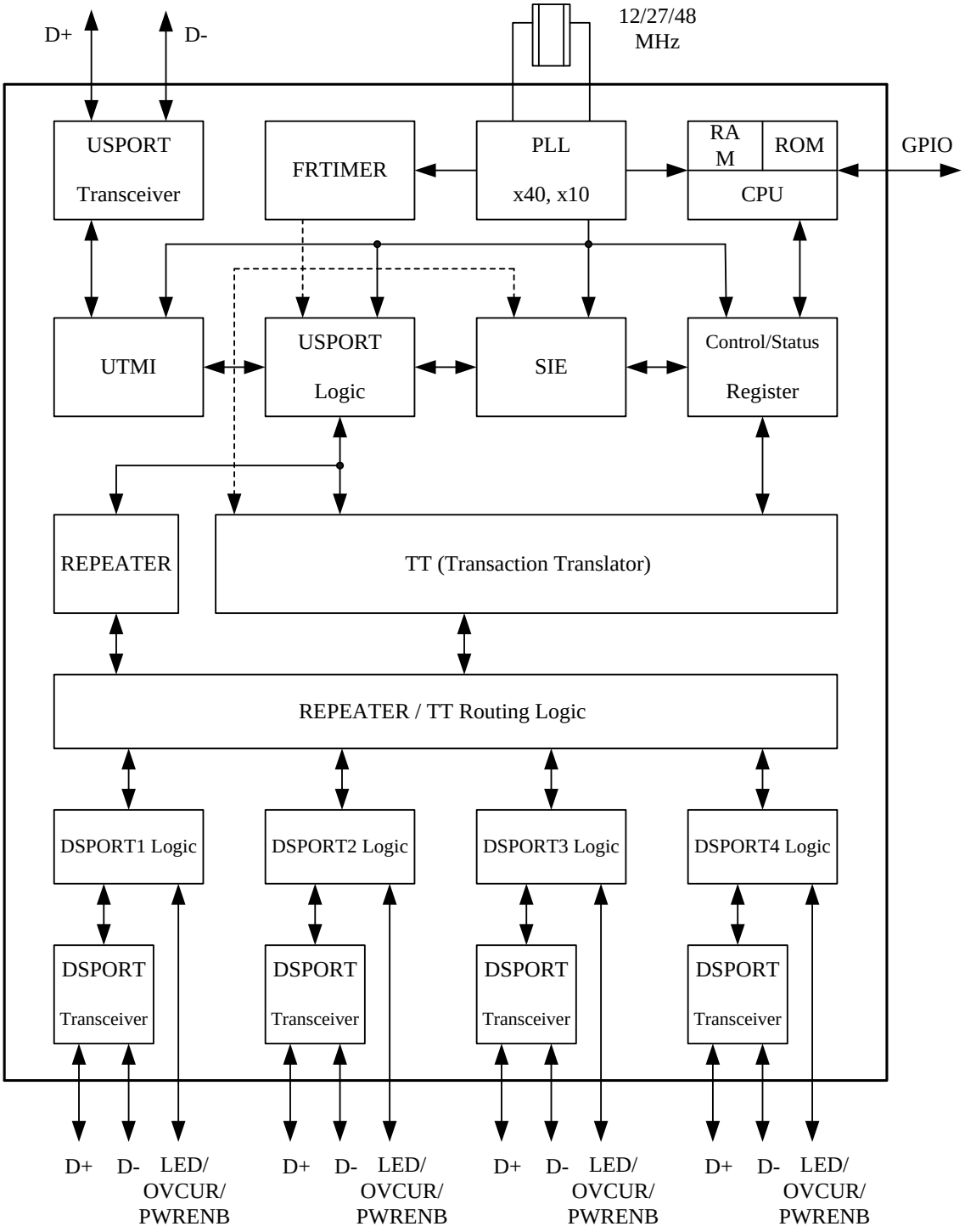


Figure 4.1 - GL850G Block Diagram (Single TT)

CHAPTER 5 FUNCTION DESCRIPTION

5.1 General Description

5.1.1 USPORT Transceiver

USPORT (upstream port) transceiver is the analog circuit that supports both full-speed and high-speed electrical characteristics defined in chapter 7 of *USB specification Revision 2.0*. USPORT transceiver will operate in full-speed electrical signaling when GL850G is plugged into a 1.1 host/hub. USPORT transceiver will operate in high-speed electrical signaling when GL850G is plugged into a 2.0 host/hub.

5.1.2 PLL (Phase Lock Loop)

GL850G contains a 40x PLL. PLL generates the clock sources for the whole chip. The generated clocks are proven quite accurate that help in generating high speed signal without jitter.

5.1.3 FRTIMER

This module implements hub (micro) frame timer. The (micro) frame timer is derived from the hub's local clock and is synchronized to the host (micro) frame period by the host generated Start of (micro) frame (SOF). FRTIMER keeps tracking the host's SOF such that GL850G is always safely synchronized to the host. The functionality of FRTIMER is described in section 11.2 of *USB Specification Revision 2.0*.

5.1.4 µC

µC is the micro-processor unit of GL850G. It is an 8-bit RISC processor with 2K ROM and 64 bytes RAM. It operates at 6MIPS of 12Mhz clock to decode the USB command issued from host and then prepares the data to respond to the host. In addition, µC can handle GPIO (general purpose I/O) settings and reading content of EEPROM to support high flexibility for customers of different configurations of hub. These configurations include self/bus power mode setting, individual/gang mode setting, downstream port number setting, device removable/non-removable setting, and PID/VID setting.

5.1.5 UTMI (USB 2.0 Transceiver Microcell Interface)

UTMI handles the low level USB protocol and signaling. It's designed based on the Intel's UTMI specification 1.01. The major functions of UTMI logic are to handle the data and clock recovery, NRZI encoding/decoding, Bit stuffing /de-stuffing, supporting USB 2.0 test modes, and serial/parallel conversion.

5.1.6 USPORT Logic

USPORT implements the upstream port logic defined in section 11.6 of *USB specification Revision 2.0*. It mainly manipulates traffics in the upstream direction. The main functions include the state machines of Receiver and Transmitter, interfaces between UTMI and SIE, and traffic control to/from the REPEATER and TT.

5.1.7 SIE (Serial Interface Engine)

SIE handles the USB protocol defined in chapter 8 of *USB specification Revision 2.0*. It co-works with Mc to play the role of the hub kernel. The main functions of SIE include the state machine of USB protocol flow, CRC check, PID error check, and timeout check. Unlike USB 1.1, bit stuffing/de-stuffing is implemented in UTMI, not in SIE.

5.1.8 Control/Status Register

Control/Status register is the interface register between hardware and firmware. This register contains the information necessary to control endpoint0 and endpoint1 pipelines. Through the firmware based architecture, GL850G possesses higher flexibility to control the USB protocol easily and correctly.

5.1.9 REPEATER

Repeater logic implements the control logic defined in section 11.4 and section 11.7 of *USB specification Revision 2.0*. REPEATER controls the traffic flow when upstream port and downstream port are signaling in the same speed. In addition, REPEATER will generate internal resume signal whenever a wakeup event is issued under the situation that hub is globally suspended.

5.1.10 TT (Transaction Translator)

TT implements the control logic defined in section 11.14 ~ 11.22 of *USB specification Revision 2.0*. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub. GL850G adopts the single TT architecture to provide the most cost effective solution. Single TT shares the same buffer control module for each downstream port. GL852G adopts multiple TT architecture to provide the most performance effective solution. Multiple TT provides control logics for each downstream port respectively. Please refer to GL852G datasheet for more detailed information.

5.1.11 REPEATER/TT Routing Logic

REPEATER and TT are the major traffic control machines in the USB 2.0 hub. Under situation that USPORT and DSPORT are signaling in the same speed, REPEATER/TT routing logic switches the traffic channel to the REPEATER. Under situation that USPORT is in the high speed signaling and DSPORT is in the full/low speed signaling, REPEATER/TT routing logic switches the traffic channel to the TT.

5.1.11.1 Connected to USB 1.1 Host/Hub

If an USB 2.0 hub is connected to the downstream port of an USB 1.1 host/hub, it will operate in USB 1.1 mode. For an USB 1.1 hub, both upstream direction traffic and downstream direction traffic are passing through REPEATER. That is, the REPEATER/TT routing logic will route the traffic channel to the REPEATER.

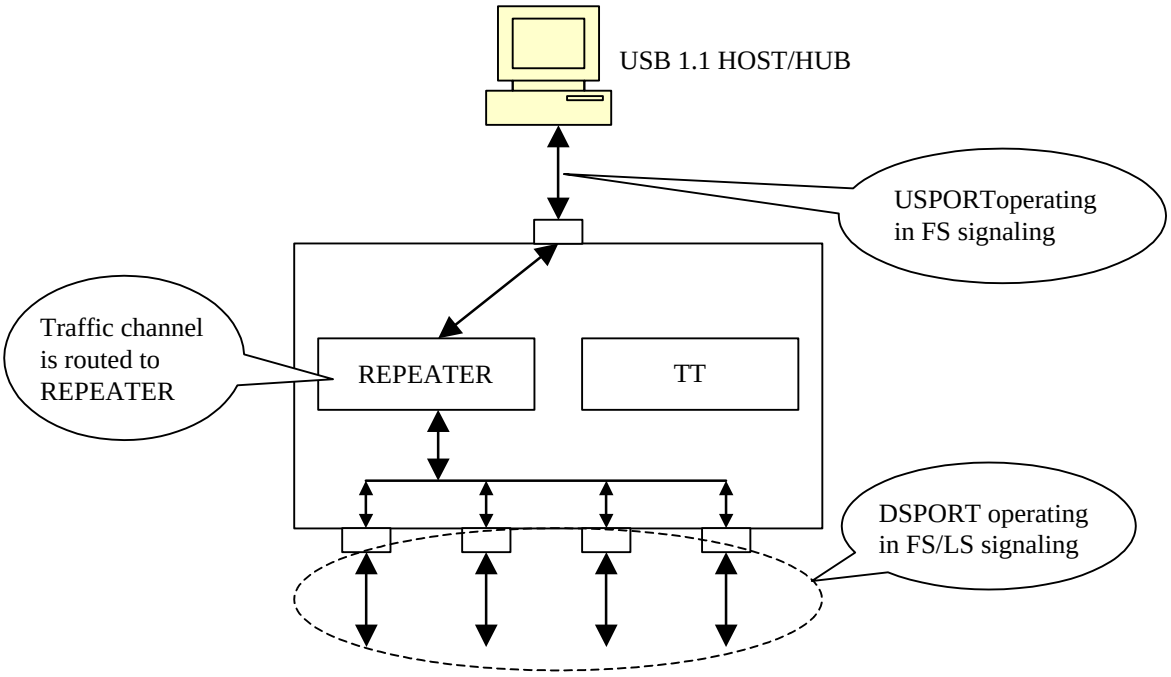


Figure 5.1 - Operating in USB 1.1 Scheme

5.1.11.2 Connected to USB 2.0 Host/Hub

If an USB 2.0 hub is connected to an USB 2.0 host/hub, it will operate in USB 2.0 mode. The upstream port signaling is in high speed with bandwidth of 480 Mbps under this environment. The traffic channel will then be routed to the REPEATER when the device connected to the downstream port is signaling also in high speed. On the other hand, the traffic channel will then be routed to TT when the device connected to the downstream port is signaling in full/low speed.

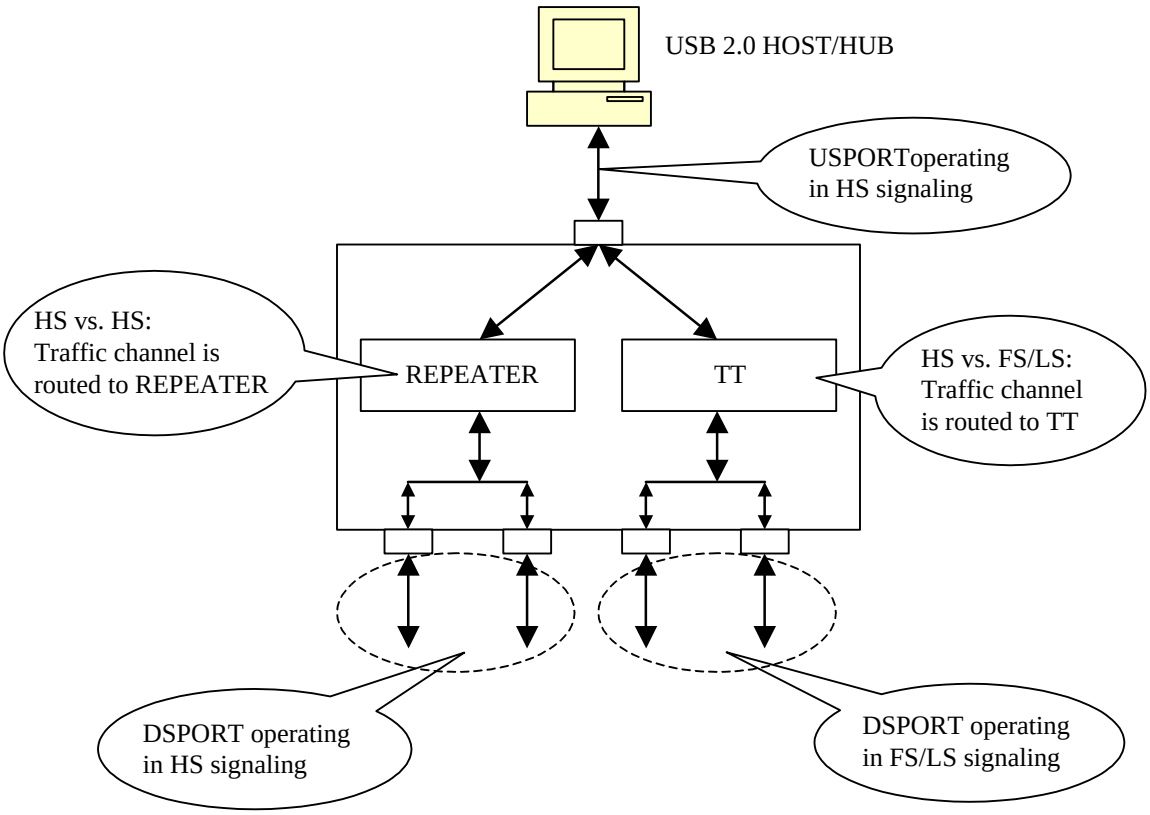


Figure 5.2 - Operating in USB 2.0 Scheme

5.1.12 DSPORT Logic

DSPORT (downstream port) logic implements the control logic defined in section 11.5 of *USB specification Revision 2.0*. It mainly manipulates the state machine, the connection/disconnection detection, over current detection and power enable control, and the status LED control of the downstream port. Besides, it also output the control signals to the DSPORT transceiver.

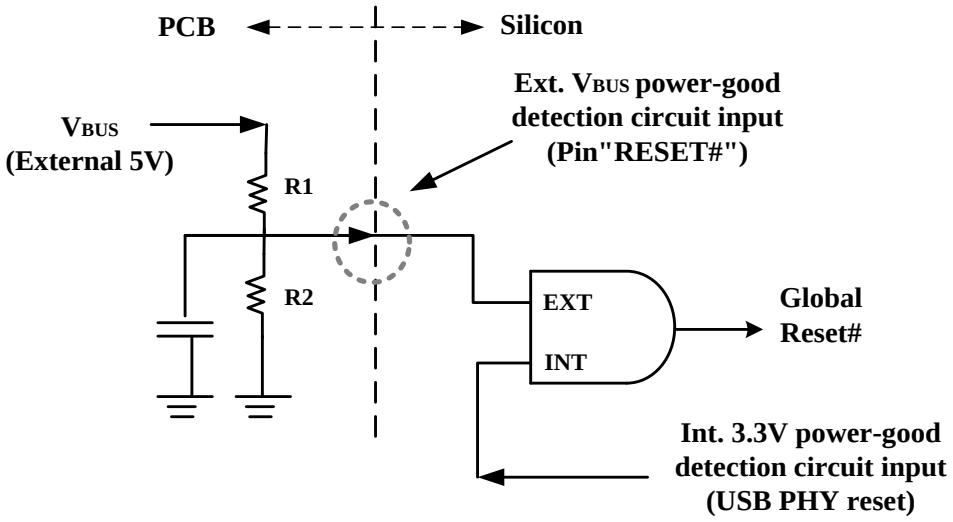
5.1.13 DSPORT Transceiver

DSPORT transceiver is the analog circuit that supports high-speed, full-speed, and low-speed electrical characteristics defined in chapter 7 of *USB specification Revision 2.0*. In addition, each DSPORT transceiver accurately controls its own squelch level to detect the detachment and attachment of devices.

5.2 Configuration and I/O Settings

5.2.1 RESET Setting

GL850G's power on reset can either be triggered by external reset or internal power good reset circuit. The external reset pin, RESETJ, is connected to upstream port Vbus (5V) to sense the USB plug / unplug or 5V voltage drop. The reset trigger voltage can be set by adjusting the value of resistor R1 and R2 (Suggested value refers to schematics) GL850G's internal reset is designed to monitor silicon's internal core power (3.3V) and initiate reset when unstable power event occurs. The power on sequence will start after the power good voltage has been met, and the reset will be released after approximately 2.7 uS after power good.



GL850G internally contains a power on reset circuit as depicted in the picture above

Figure 5.3 - Power on Reset Diagram

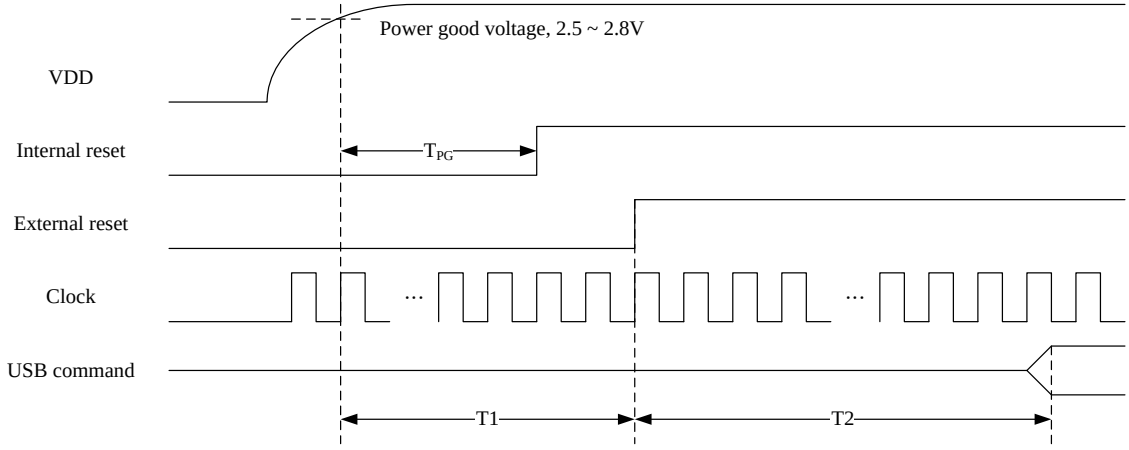


Figure 5.4 - Power on Sequence of GL850G

Table 5.1 - Reset Timing

Symbol	Parameter	Min.	Max.	Unit
T_{PG}	VDD power up to internal reset (power good) assert (12MHz)	-	2.7	µs
	VDD power up to internal reset (power good) assert (24MHz)	-	1.3	
	VDD power up to internal reset (power good) assert (27MHz)	-	1.2	
	VDD power up to internal reset (power good) assert (48MHz)	-	0.7	
T1	VDD power up to external reset (RESETJ) assert	3	-	µs
T2	RESET assert to respond USB command ready	70	-	ms

To fully control the reset process of GL850G, we suggest the reset time applied in the external reset circuit should longer than that of the internal reset circuit.

5.2.2 PGANG/SUSPND Setting

To save pin count, GL850G uses the same pin to decide individual/gang mode as well as to output the suspend flag. The individual/gang mode is decided within 20us after power on reset. Then, about 50ms later, this pin is changed to output mode. GL850G outputs the suspend flag once it is globally suspended. For individual mode, a pull low resister greater than 100KΩ should be placed. For gang mode, a pull high resister greater than 100KΩ should be placed. In figure 5.5, we also depict the suspend LED indicator schematics. It should be noticed that the polarity of LED must be followed, otherwise the suspend current will be over spec limitation (2.5mA).

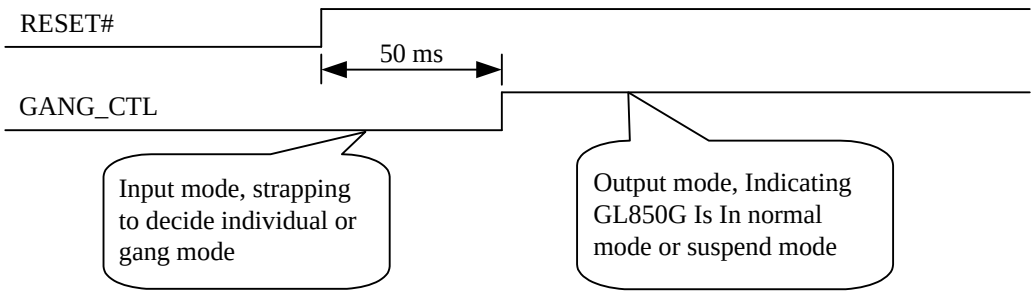


Figure 5.5 - Timing of PGANG/SUSPEND Strapping

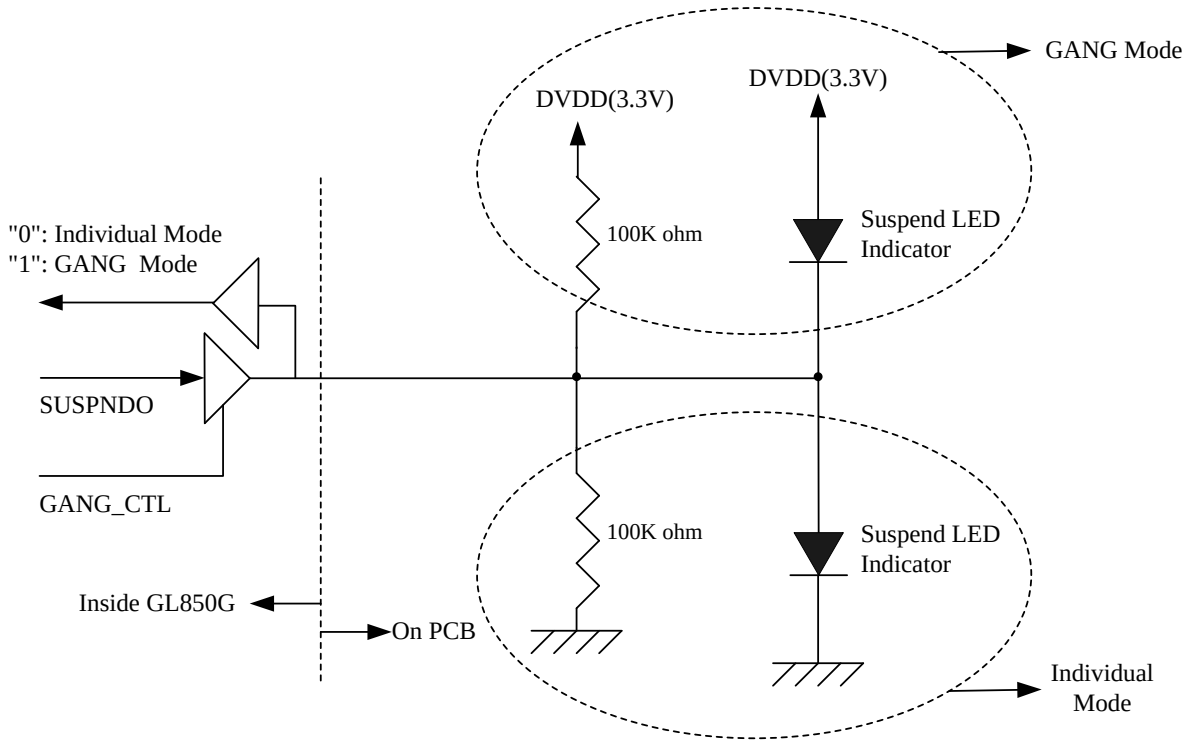


Figure 5.6 - Individual/GANG Mode Setting

5.2.3 SELF/BUS Power Setting

GL850G can operate under bus power and conform to the power consumption limitation completely (suspend current < 2.5 mA, normal operation current < 100 mA). By setting PSELF, GL850G can be configured as a bus-power or a self-power hub.

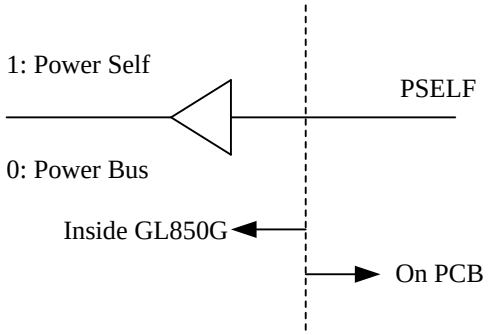


Figure 5.7 - SELF/BUS Power Setting

5.2.4 LED Connections

GL850G controls the LED lighting according to the flow defined in section 11.5.3 of *Universal Serial Bus Specification Revision2.0*. Both manual mode and Automatic mode are supported in GL850G. When GL850G is globally suspended, GL850G will turn off the LED to save power.

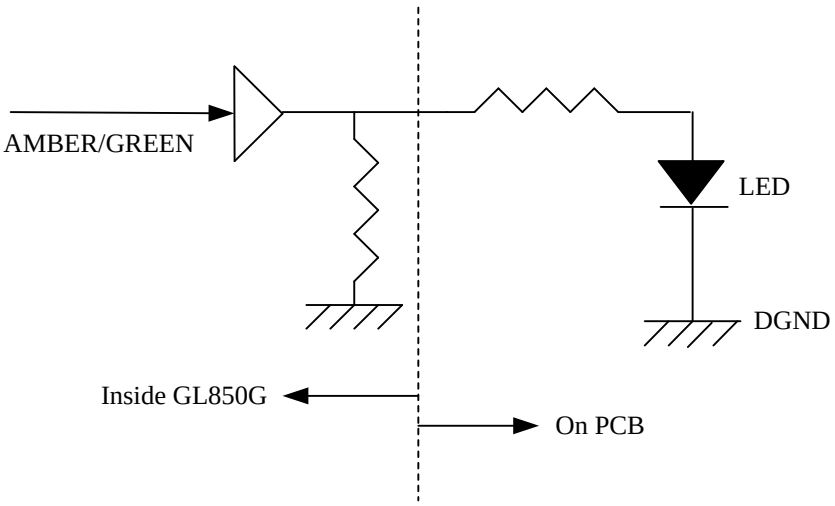


Figure 5.8 - LED Connection

5.2.5 EEPROM Setting

GL850G replies to host commands by the default settings in the internal ROM. GL850G also offers the ability to reply to the host according to the settings in the external EEPROM (LQFP48 supports 93C46 and QFN28/SSOP28 only supports 24C02). The detail setting information please refers to the **USB 2.0 Hub AP Note_EEPROM Info** document.

The schematics between GL850G and 93C46 are depicted in the following figures:

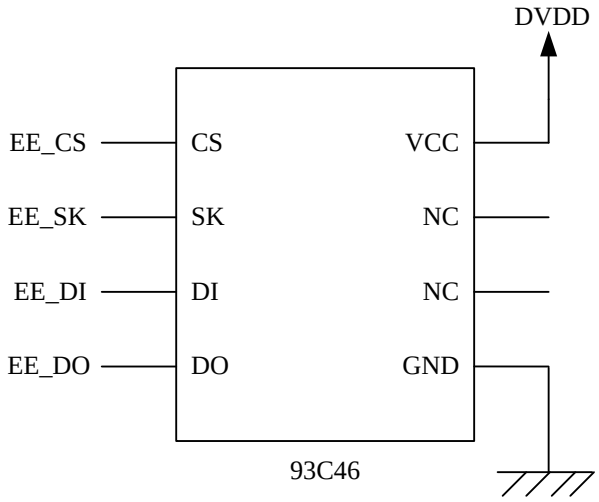


Figure 5.9 - Schematics between GL850G and 93C46

GL850G firstly verifies the check sum after power on reset. If the check sum is correct, GL850G will take the configuration of 93C46 as part of the descriptor contents. To prevent the content of 93C46 from being over-written, amber LED will be disabled when 93C46 exists.

5.2.6 Power Switch Enable Polarity (Only Available in LQFP48 Package)

Both low/high-enabled power switches are supported. It is determined by jumper setting, based on the state of pin AMBER2, as the following table:

Table 5.2 - Configuration by Power Switch Type

AMBER2	Power Switch Enable Polarity
0	Low-active
1	High-active

Note: When AMBER2=1, the external resistor of PWREN1~4 need pull down.

5.2.7 Port Number Configuration (Only Available in LQFP48 Package)

Number of downstream port can be configured as 2/3/4 ports by pin strapping in addition to EEPROM, based on the state of pin AMBER 3, AMBER 4, as the following table:

Table 5.3 - Port Number Configuration

AMBER3	AMBER 4	Port Number
1	0	2
0	1	3
0	0	4

5.2.8 Non-removable Port Configuration (Only Available in LQFP48 Package)

For compound application or embedded system, downstream ports that always connected inside the system can be set as non-removable based on the state of corresponding status LED, pin GREEN 1~4. If the pin is pull high in the initial stage (POR reset), the corresponding port will be set as non-removable.

5.2.9 Reference Clock Configuration (Only Available in LQFP48 Package)

GL850G can support optional 27/48MHz clock source, which is selectable through GPIO configurations. For some on-board design that 27/48MHz clock source is available, such as motherboard or Monitor built-in applications, system integrator can leverage this feature to further reduce BOM cost by removing external crystal.

Table 5.4 - Ref. Clock Configuration

SEL48	SEL27	Clock Source
0	1	48MHz OSC-in
1	0	27MHz OSC-in
1	1	12MHz X'tal/OSC-in

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Maximum Ratings

Table 6.1 - Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_5	5V Power Supply	-0.5	+6.0	V
V_{DD}	3.3V Power Supply	-0.5	+3.6	V
V_{IN}	Input Voltage for digital I/O pins	-0.5	+3.6	V
V_{INOD}	Open-drain input pins(Ovcur1~4#,Pself,Reset)	-0.5	+5.5	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	-0.5	+3.6	V
T_S	Storage Temperature under bias	-55	+100	^oC
F_{OSC}	Frequency	12 MHz ± 0.05%		

6.2 Operating Ranges

Table 6.2 - Operating Ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_5	5V Power Supply	4. 5	5.0	5.5	V
V_{DD}	3.3V Power Supply	3.0	3.3	3.6	V
V_{IN}	Input Voltage for digital I/O pins	-0.5	-	3.6	V
V_{INOD}	Open-drain input pins(Ovcur1~4#,Pself,Reset)	-0.5	-	5.0	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	0.5	-	3.6	V
T_A	Ambient Temperature	0	-	85	^oC
T_J	Absolute maximum junction temperature	0	-	125	^oC
θ_{JA}	Thermal Characteristics 48 LQFP	-	83.5	-	$^oC/W$
	Thermal Characteristics 28 SSOP	-	63.3	-	$^oC/W$
	Thermal Characteristics 28 QFN	-	34.5	-	$^oC/W$

6.3 DC Characteristics

Table 6.3 - DC Characteristics except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
P_D	Power Dissipation	150	-	300	mW
V_{IL}	LOW level input voltage	-	-	0.8	V
V_{IH}	HIGH level input voltage	2.0	-	-	V
V_{TLH}	LOW to HIGH threshold voltage	1.4	1.5	1.6	V
V_{THL}	HIGH to LOW threshold voltage	0.87	0.94	0.99	V
V_{OL}	LOW level output voltage when I_{OL}=8mA	-	-	0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4	-	-	V
R_{DN}	Pad internal pull down resister	29	59	135	KΩ
R_{UP}	Pad internal pull up resister	80	108	140	KΩ

Table 6.4 - DC Characteristics of USB Signals under FS/LS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	DP/DM FS static output LOW(R_L of 1.5K to 3.6V)	0	-	0.3	V
V_{OH}	DP/DM FS static output HIGH (R_L of 15K to GND)	2.8	-	3.6	V
V_{DI}	Differential input sensitivity	0.2	-	-	V
V_{CM}	Differential common mode range	0.8	-	2.5	V
V_{SE}	Single-ended receiver threshold	0.2	-	-	V
C_{IN}	Transceiver capacitance	-	-	20	Pf
I_{LO}	Hi-Z state data line leakage	-10	-	+10	μA
Z_{DRV}	Driver output resistance	28	-	44	Ω

Table 6.5 - DC Characteristics of USB Signals under HS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	DP/DM HS static output LOW(R_L of 1.5K to 3.6V)	-	-	0.1	V
C_{IN}	Transceiver capacitance	4	4.5	5	Pf
I_{LO}	Hi-Z state data line leakage	-5	0	+5	μA
Z_{DRV}	Driver output resistance for USB 2.0 HS	42	45	48	Ω

6.4 Power Consumption

Table 6.6 - DC Supply Current

Symbol	Condition			Current	Unit
	Active ports	Host	Device		
I_{SUSP}	Suspend			538	uA
I_{CC}	4	H*	H	52.4	mA
	3	H	H	47.8	mA
	2	H	H	43.2	mA
	1	H	H	38.6	mA
	USPORT Config.	H	N/A	33.8	mA

*H: High-Speed

Note:

Test result represents silicon level operating current, without considering additional power consumption contributed by external over-current protection circuit such as power switch or polyfuse.

6.5 AC Characteristics

GL850G LQFP48 package supports 93C46 EEPROM for customized VID/PID. GL850G QFN28 and SSOP28 package supports 24C02 type EEPROM. AC characteristics of these two types of EEPROM summarized as below figures and tables.

6.5.1 93C46 EEPROM IF

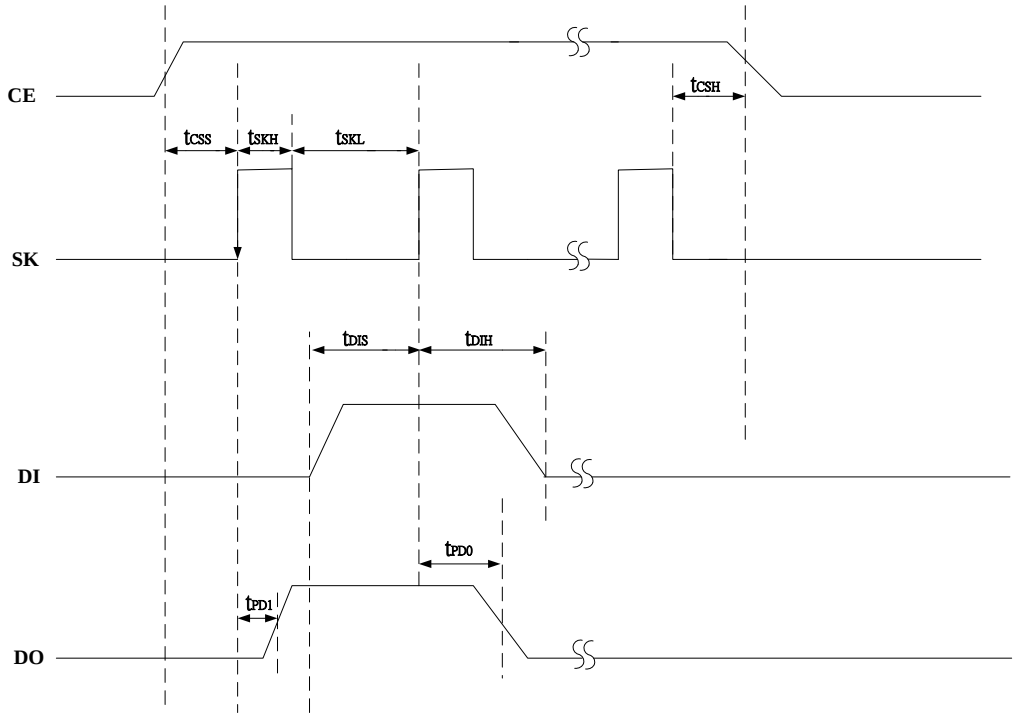
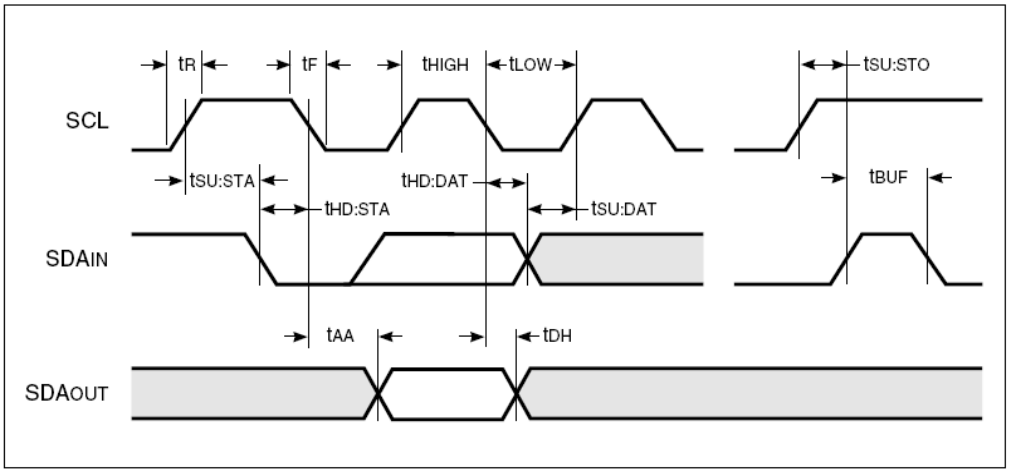


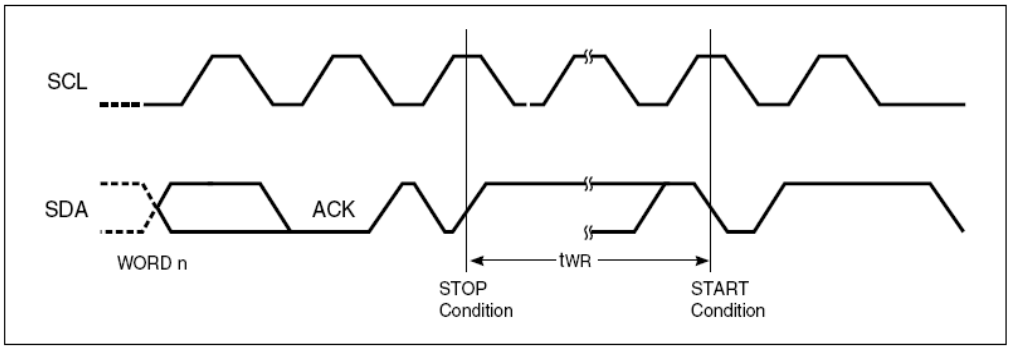
Table 6.7 - AC Characteristics of EEPROM Interface (93C46)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CSS}	CS Setup Time	3.0			us
t_{CSH}	CS Hold Time	3.0			
t_{SKH}	SK High Time	1.0			
t_{SKL}	SK Low Time	2.2			
t_{DIS}	DI Setup Time	1.8			
t_{DIH}	DI Hold Time	2.4			
t_{PD1}	Output Delay to “1”			1.8	
t_{PD0}	Output Delay to “0”			1.8	

6.5.2 24C02 EEPROM Interface



Bus Timing



Write Cycle Timing

Table 6.8 - AC Characteristics of EEPROM Interface (24C02)

Symbol	Parameter	Test Conditions	1.8V-5.5V Min.	1.8V-5.5V Max.	2.5V-5.5V Min.	2.5V-5.5V Max.	Unit
f_{SCL}	SCL Clock Frequency		0	100	0	400	KHz
T	Noise Suppression Time(1)		—	100	—	50	ns
t_{LOW}	Clock LOW Period		4.7	—	1.2	—	µs
t_{HIGH}	Clock HIGH Period		4	—	0.6	—	µs
t_{BUF}	Bus Free Time Before New Transmission(1)		4.7	—	1.2	—	µs
$t_{SU:STA}$	Start Condition Setup Time		4.7	—	0.6	—	µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7	—	0.6	—	µs
$t_{HD:STA}$	Start Condition Hold Time		4	—	0.6	—	µs
$t_{HD:STO}$	Stop Condition Hold Time		4	—	0.6	—	µs
$t_{SU:DAT}$	Data In Setup Time		200	—	100	—	ns
$t_{HD:DAT}$	Data In Hold Time		0	—	0	—	ns
t_{DH}	Data Out Hold Time	SCL LOW to SDA Data Out Change	100	—	50	—	ns
t_{AA}	Clock to Output	SCL LOW to SDA Data Out Valid	0.1	4.5	0.1	0.9	µs
t_R	SCL and SDA Rise Time(1)		—	1000	—	300	ns
t_F	SCL and SDA Fall Time(1)		—	300	—	300	ns
t_{WR}	Write Cycle Time		—	10	—	5	ms

Note:
1. This parameter is characterized but not 100% tested.

6.6 On-Chip Power Regulator

GL850G requires 3.3V source power for normal operation of internal core logic and USB physical layer (PHY). The integrated low-drop power regulator converts 5V power input from USB cable (Vbus) to 3.3V voltage for silicon power source. The 3.3V power output is guaranteed by an internal voltage reference circuit to prevent unstable 5V power compromise USB data integrity. The regulator's maximum current loading is 200mA, which provides enough tolerance for normal GL850G operation (below 100mA).

On-chip Power Regulator Features:

- 5V to 3.3V low-drop power regulator
- 200mA maximum output driving capability
- Provide stable 3.3V output when Vin = 4.4V~5.5V
- Max. suspend current:266uA; typical suspend current 187uA

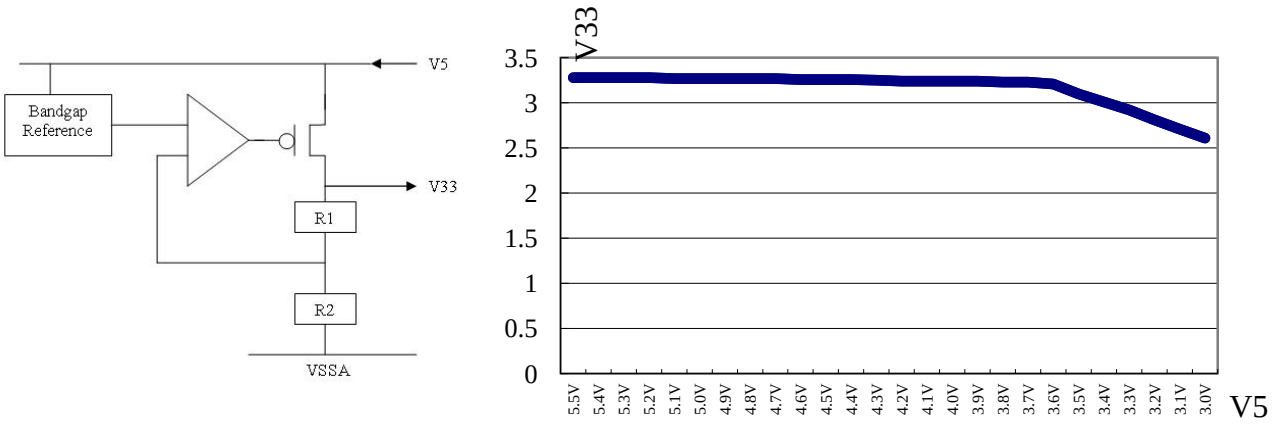
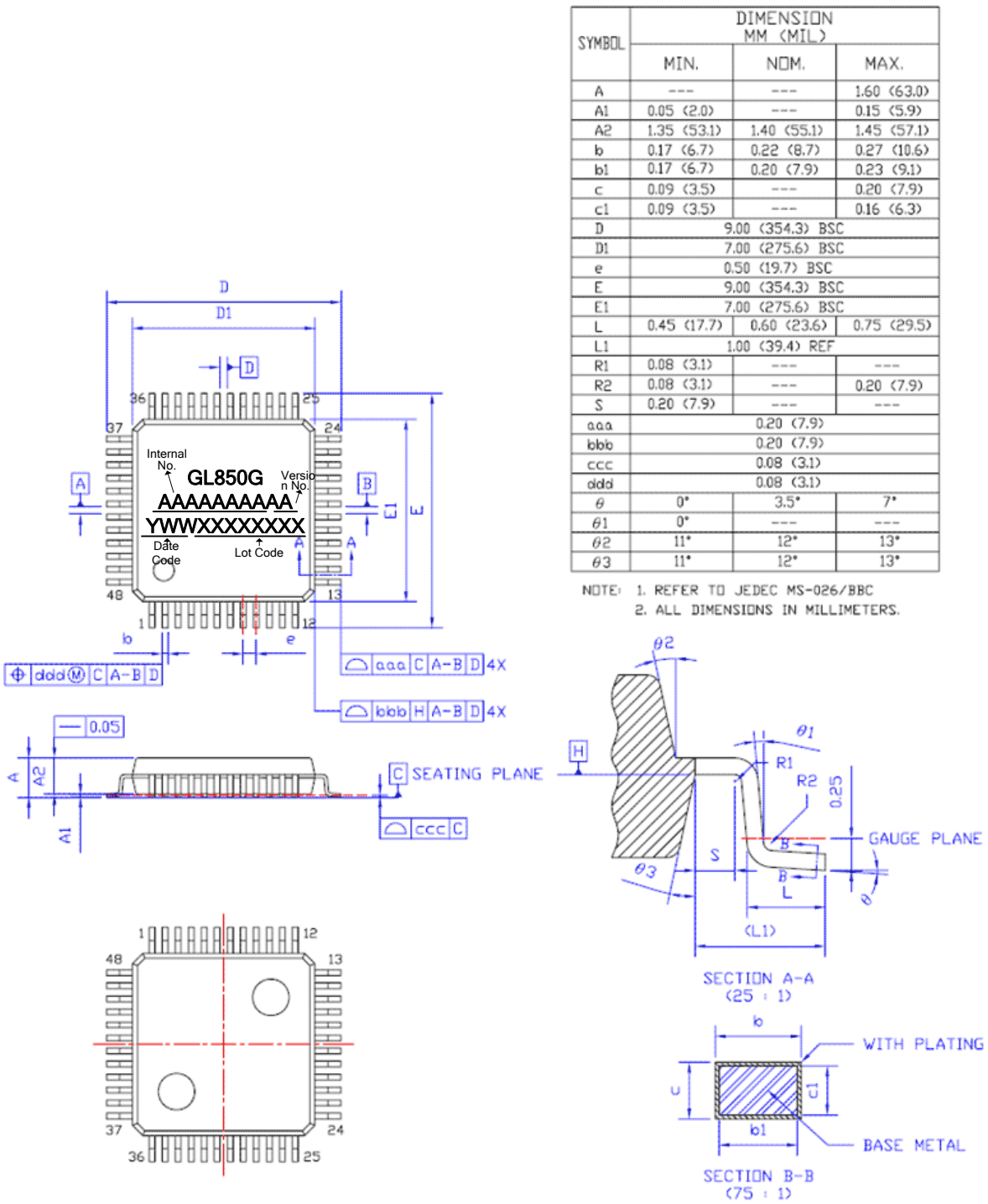


Figure 6.1 - Vin(V5) vs Vout(V33)*

*Note: Measured environment: Ambient temperature = 25℃ / Current Loading = 200mA

CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	1.60 (63.0)
A1	0.05 (2.0)	---	0.15 (5.9)
A2	1.35 (53.1)	1.40 (55.1)	1.45 (57.1)
b	0.17 (6.7)	0.22 (8.7)	0.27 (10.6)
b1	0.17 (6.7)	0.20 (7.9)	0.23 (9.1)
c	0.09 (3.5)	---	0.20 (7.9)
c1	0.09 (3.5)	---	0.16 (6.3)
D	9.00 (354.3) BSC		
D1	7.00 (275.6) BSC		
e	0.50 (19.7) BSC		
E	9.00 (354.3) BSC		
E1	7.00 (275.6) BSC		
L	0.45 (17.7)	0.60 (23.6)	0.75 (29.5)
L1	1.00 (39.4) REF		
R1	0.08 (3.1)	---	---
R2	0.08 (3.1)	---	0.20 (7.9)
S	0.20 (7.9)	---	---
aaa	0.20 (7.9)		
bbb	0.20 (7.9)		
ccc	0.08 (3.1)		
ddd	0.08 (3.1)		
θ	0°	3.5°	7°
θ1	0°	---	---
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTE: 1. REFER TO JEDEC MS-026/BBC
2. ALL DIMENSIONS IN MILLIMETERS.

Figure 7.1 - GL850G 48 Pin LQFP Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	2.00 (78.7)
A1	0.05 (2.0)	---	0.21 (8.3)
A2	1.65 (65.0)	1.75 (68.9)	1.85 (72.8)
b	0.22 (8.7)	---	0.38 (15.0)
b1	0.22 (8.7)	0.30 (11.8)	0.33 (13.0)
c	0.09 (3.5)	---	0.25 (9.8)
c1	0.09 (3.5)	---	0.21 (8.3)
D	10.20 (401.6) BSC		
e	0.65 (25.6) BSC		
E	7.80 (307.1) BSC		
E1	5.30 (208.7) BSC		
L	0.55 (21.7)	0.75 (29.5)	0.95 (37.4)
L1	1.25 (49.2) REF		
R1	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
R2	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
y	---	---	0.08 (3.1)
θ	0°	4°	8°
θ1	0°	---	---
θ2	7° TYP		
θ3	7° TYP		

NOTE: 1. REFER TO JEDEC MO-150
2. ALL DIMENSIONS IN MILLIMETERS.

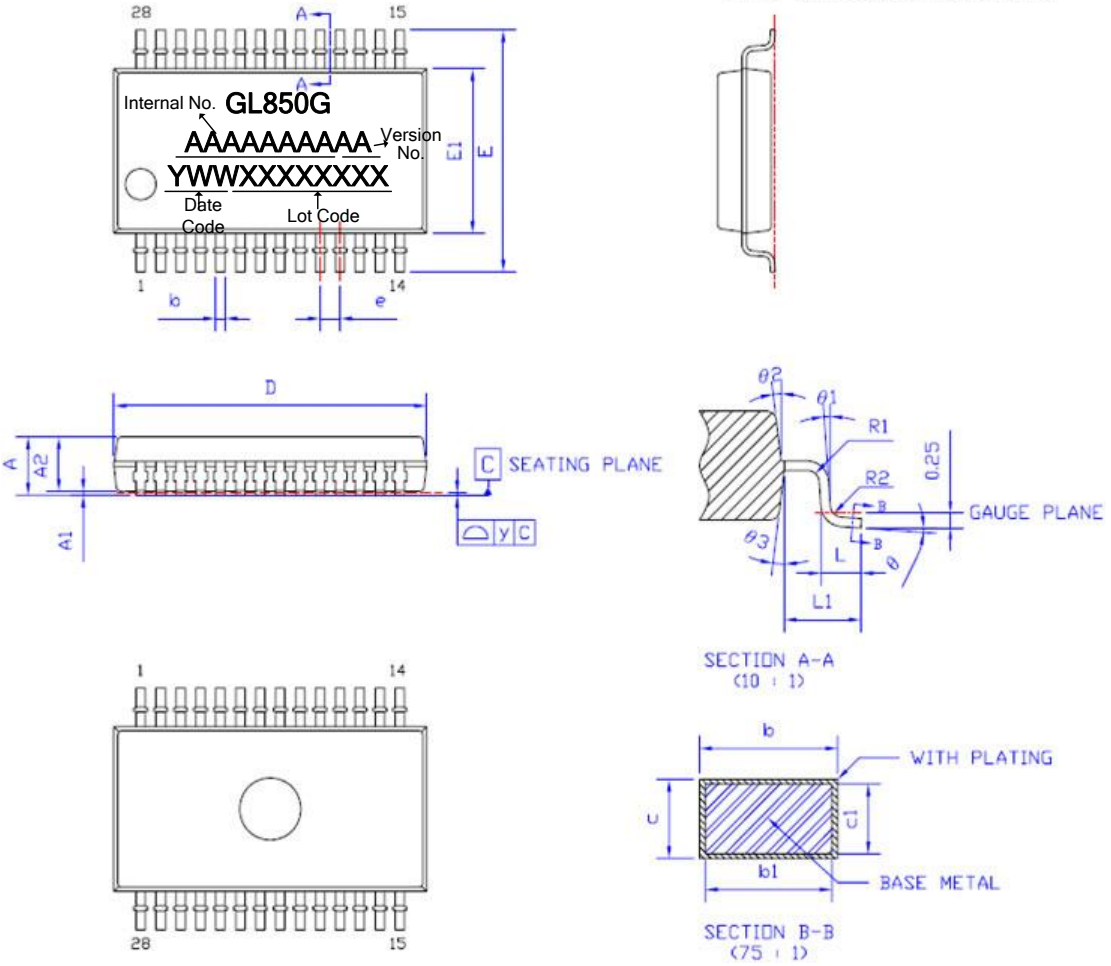
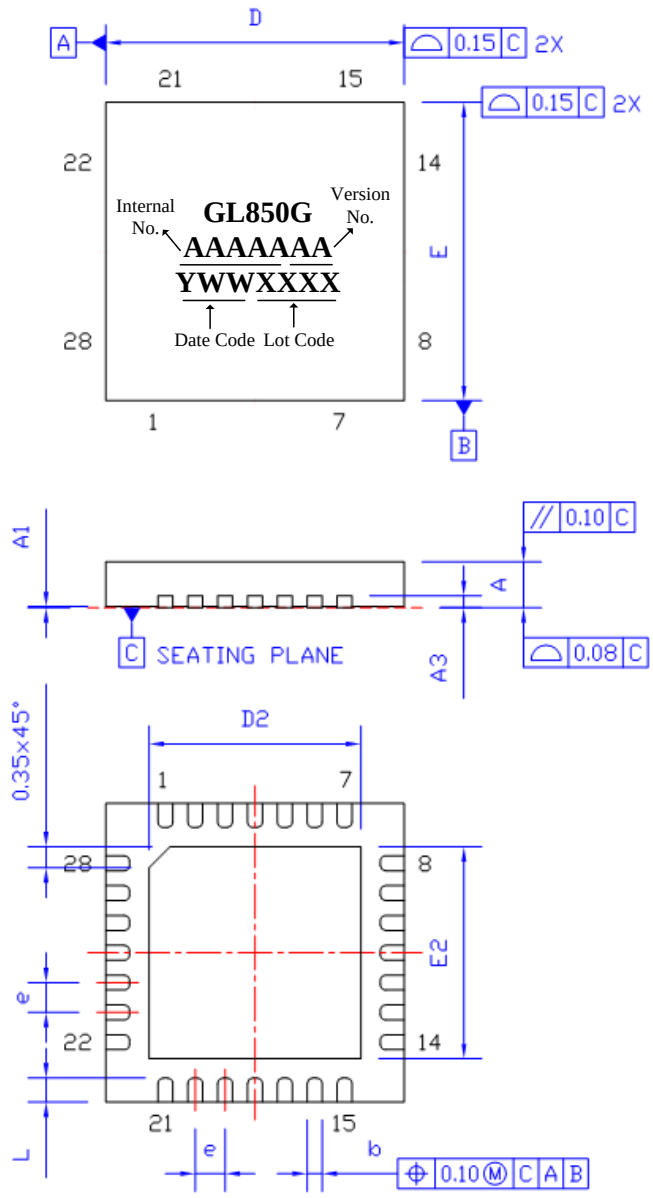


Figure 7.2 - GL850G 28 Pin SSOP Package



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.18 (7.1)	0.25 (9.8)	0.30 (11.8)
D	5.00 (196.9) BSC		
D2	3.40 (133.9)	3.55 (139.8)	3.70 (145.7)
E	5.00 (196.9) BSC		
E2	3.40 (133.9)	3.55 (139.8)	3.70 (145.7)
e	0.50 (19.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

Figure 7.3 - GL850G 28 Pin QFN Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Green/Wire Material	Version	Status
GL850G-MNYXX	LQFP 48	Green Package	XX	Available
GL850G-HHYXX	SSOP 28	Green Package	XX	Available
GL850G-OHYXX	QFN 28	Green Package	XX	Available

Note: The marking of "OHY" will not be shown on the IC due to QFN 28 package size limitation.