COSE222: Computer Architecture
Assignment #1

Due: Sep 27, 2020 (Sunday) 11:59pm on Blackboard

Solutions

Please answer for the questions. Write your student ID and name on the top of the document. Submit your homework with "**PDF**" format only. (You can easily generate the pdf files from Microsoft Word or HWP. You can also handwrite your answers to scan the handwritten documents with "**PDF**" format. You can use the document capture applications such as "Office Lens" for scanning your documents with your smartphones.)

The answer rules:
(1) You can write answers in both Korean and English.
(2) Please make your final answer numbers have two decimal places.
(3) Performance of A is improved by *NN* % compared to performance B if PerfA / PerfB = 1.*NN*.

1. Write the eight great ideas in computer architecture research mentioned during the class. [8]

Design for Moore's Law
Use abstraction to simplify design
Make the common case fast
Performance via parallelism
Performance via pipelining
Performance via prediction
Hierarchy of memories
Dependability via redundancy (for reliability)

2. **Student Y** stated that the performance of the ARM processor using 2 GHz clock exhibits higher performance than the x86 Pentium processor that runs with 1.5 GHz clock. Explain why the statement by **Student Y** is not always true. Please take a counter example in your answer. [5]

This statement is not always true because the execution time of computer systems are influenced by other factors such as instruction counts after compilation and CPI affected by microarctheicture.

For instance the instruction counts using an x86 compiler can be smaller.

3. Assume a color display using **8-bits** for each of primary colors (red, green, blue) per pixel and a frame size is 1920 × 1080.

(a) What is the minimum size in **bytes** of the frame buffer to store a single frame? [3]

1920 * 1080 pixels = 2,073,600 pixels → 2,073,600 * 3 = 6,220,800 bytes

(b) Assume that you are requested to design a display interface that can transfer 60 frames per second. Assuming a single frame has a 1920 x 1080 resolution of 8-bits R/G/B pixels, calculate the minimum

bandwidth of this display interface. Write your answer using MB/s. (1 KB = 1024 byte, 1 MB = 1024 KB) [3]

Total amount of data to be transferred per second is

6,220,800 bytes/frame * 60 frame/sec= 373,248,000 bytes/sec =355.96 MB/s

4. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has 2.4GHz clock rate and a CPI of 1.2. P2 has a 3.0GHz clock rate and CPI of 1.4. P3 has a 4.0GHz clock rate and has a CPI of 2.2.

(a) Which processor has the highest performance expressed in **instructions per second**? [6]

Performance of P1 (inst/sec) = $2.4 * 10^9/1.2 = 2.00 * 10^9$
Performance of P2 (inst/sec) = $3.0 * 10^9/1.4 = 2.14 * 10^9$
Performance of P3 (inst/sec) = $4.0 * 10^9 / 2.2 = 1.82 * 10^9$

P2 has the highest performance

(b) If the processors each execute a program in 10 seconds, find the **number of cycles** and the **number of instructions**. [6]

Cycles of P1 = $10 * 2.4 * 10^9 = 24 * 10^9$
Cycles of P2 = $10 * 3.0 * 10^9 = 30 * 10^9$
Cycles of P3 = $10 * 4.0 * 10^9 = 40 * 10^9$

# of instructions of P1 = $24 * 10^9 / 1.2 = 2.00 * 10^{10}$
# of instructions of P2 = $30 * 10^9 / 1.4 = 2.14 * 10^{10}$
# of instructions of P3 = $40 * 10^9 / 2.2 = 1.82 * 10^{10}$

5. Computer A can execute a C program 10 times in one second and Computer B can execute the same C program 20 times in one second. If the MIPS (million instructions per second) rate of Computer A is MIPS_A and MIPS rate of Computer B is MIPS_B, then an engineer concludes that MIPS_B = MIPS_A x 2. Under what conditions is this calculation correct? [5]

The assumption is correct only if the two machines have the same ISA and even with the same ISA they both use the same compiler.

6. Assume that for a certain program **compiler A** results in a dynamic instruction count of $1.1x10^9$ and has an execution time of 1.2 sec, while **compiler B** results in a dynamic instruction count of $1.5x10^9$ and an execution time of 1.7 sec.

(a) Find the average CPI for each program given that the processor has a clock cycle time of 1 ns. [6]

For the program compiled by compiler A:
Clock cycle count = $1.2x10^9$, therefore CPI = clock cycle count / instruction count = 1.09

For the program compiled by compiler B:
Clock cycle count = $1.7x10^9$, therefore CPI = clock cycle count / instruction count = 1.13

(b) Assume that the compiled programs run on two different processors **X** and **Y**. If the execution times on the two processors are the same, how much faster is the clock of the **processor Y** running **compiler**

B's code versus the clock of the **processor X** running **compiler A**'s code? Assume that the processors have the same microarchitecture deploying the same ISA. [5]

Considering execution time = # of instructions * CPI * clock cycle time,
therefore $1.1x10^9 * 1.09$ / frequency of X = $1.5x10^9 * 1.13$ / frequency of Y
frequency of Y / frequency of X = $(1.5x10^9 * 1.13) / (1.1x10^9 * 1.09) = 1.41$

Processor Y has 41% faster clock frequency.

(c) A new compiler is developed that uses only $6.0x10^8$ instructions and has average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor? [6]

Comparing to compiler A:
$(1.1x10^9 * 1.09) / (0.6x10^9 * 1.1) = 1.82$ 82% speedup

Comparing to compiler B:
$(1.5x10^9 * 1.13) / (0.6x10^9 * 1.1) = 2.57$ 2.57 times speedup

7. Consider two different implementations of **the same instruction set architecture**. The instructions can be divided into four classes according to their CPI (classes A, B, C, and D). Consider the following two processors and an application.

P1: Clock frequency = 2.0GHz, CPIs for each instruction class = 1, 2, 3, 3

P2: Clock frequency = 3.0GHz, CPIs for each instruction class = 2, 2, 2, 2

Application:
Instruction count = $1.0x10^6$,
fractions by instruction classes: class A = 20%, class B = 10%, class C = 40%, class D = 30%

(a) Which processor is faster: P1 or P2? [5]

Class A: $2 * 10^5$ inst, Class B: $1 * 10^5$ inst, Class C: $4 * 10^5$ inst, Class D = $3 * 10^5$ inst
Execution time = Clock counts / clock frequency
Execution time of P1 = $(1*2 + 2*1 + 3*4 + 3*3) * 10^5 / 2.0 * 10^9 = 12.5 * 10^{-4}$ sec
Execution time of P2 = $(2*2 + 2*1 + 2*4 + 2*3) * 10^5 / 3.0 * 10^9 = 6.67 * 10^{-4}$ sec
P2 is faster!!

(b) What is the global CPI for each implementation? [6]

CPI = Total clock counts / total # of instructions
CPI of P1 = $(1*2 + 2*1 + 3*4 + 3*3) * 10^5 / 10^6 = 2.5$
CPI of P2 = $(2*2 + 2*1 + 2*4 + 2*3) * 10^5 / 10^6 = 2.0$

(c) Figure out the clock cycles required in both cases. [4]

Clock cycles of P1 = $(1*2 + 2*1 + 3*4 + 3*3) * 10^5 = 25 * 10^5$
Clock cycles of P1 = $(2*2 + 2*1 + 2*4 + 2*3) * 10^5 = 20 * 10^5$

8. An enhancement is proposed to a computer (called the **baseline**). The enhancement merges some commonly occurring instructions into a single instruction. But this enhancement increases the clock cycle time by 20% for all instructions. Assume that 80% of the instructions in the baseline computer are merged into just 40%. (That means 2 instructions are merged into one instruction.) Furthermore,

assume that in the baseline machine the CPI (clock per instruction) of the instructions that **cannot** be merged is **50%** higher than the CPI of the instructions that **can** be merged. What is the speedup of the enhanced computer over the baseline? [15]

For the baseline machine, the execution time of instructions is 1.1aT

fused instructions: (0.8) * a * T = 0.8aT
non-fused instructions: (0.2) * 1.5a * T = 0.3aT
, where a is a CPI of fused instructions and T is a clock period

For the enhanced machine, the execution time of instructions is 0.84aT

fused instructions: (0.4) * a * 1.2T = 0.48aT
non-fused instructions: (0.2) * 1.5a * 1.2T = 0.36aT

Therefore, speedup = 1.1aT / 0.84aT = 1.3095 Speed-up = 30.95%

Baseline: 0.2 *1.5 + .8 = 1.1
Enhanced: 0.2 *1.2 *1.5 + 0.4 * 1.2 = 0.84 ; Speedup = 1.1/0.84 = 30.95%.

9. Let us assume that 40% of instructions in a certain program can be parallelized. Note that if 100% of instructions is parallelizable, the execution time of this application will be half if running on a dual-core processor.

(a) What are the performance improvements of this application when running on dual-core (2 cores), quad-core (4 cores), and octa-core (8 cores) processors, respectively. Assume that the baseline machine for comparison is a single-core system. [6]

Let us assume the execution time on the single-core processor is A. The execution time of each case is,
For dual-core processor, (0.6 + 0.4/2)A = 0.80A, Speedup = 1/0.8 = 1.25, Performance improvement = 25%
For quad-core processor, (0.6 + 0.4/4)A = 0.70A, Speedup = 1/0.7 = 1.43, Performance improvement = 43%
For octa-core processor, (0.6 + 0.4/8)A = 0.65A, Speedup = 1/0.65 = 1.54, Performance improvement = 54%

(b) Assuming the dynamic power consumption of the single-core processor is P, what are the power consumption of the dual-core, quad-core, and octa-core processors, respectively? Use the equation learned during the class and ignore the activity factor. [6]

P=CV2f. Only the capacity load increases when multi-core processors are deployed.
For dual-core, power consumption = 2P
For quad-core, power consumption = 4P
For octa-core, power consumption = 8P

(c) Energy (=power x time) is the appropriate metric that considers both performance and cost. Namely we can recognize the total of consumed power that is required for executing applications by using energy. Calculate the energy consumption of single-core, dual-core, quad-core, and octa-core processors respectively using A (execution time) and P (power consumption) of the single-core processor. Figure out the best configuration considering the only energy consumption. [8]

For single-core, energy = AP
For dual-core, energy = 0.8A * 2P = 1.6AP

For quad-core, energy = 0.7A * 4P = 2.8AP
For octa-core, energy = 0.65A * 8P = 5.2AP

The single-core processor is the best configuration only considering the energy consumption.

10. Assume a program requires the execution of $50x10^6$ FP instructions, $110x10^6$ INT instructions, $80x10^6$ load/store instructions, and $16x10^6$ branch instructions. The CPI for each type of instruction (FP, INT, load/store, and branch types) is 1, 1, 4, and 2, respectively. Assume that the processor has a 2GHz clock rate.

(a) By how much must we improve the CPI of FP instructions if we want the program to run two times faster? [6]

Execution time = Total clock count / clock frequency
Execution time before improvement = $(50*1 + 110*1 + 80*4 + 16*2) * 10^6 / 2*10^9 = 256*10^{-3}$ sec
Let us assume the improved CPI of FP is X, then
$(50*X + 110*1 + 80*4 + 16*2) * 10^6 / 2*10^9 = 256*10^{-3} / 2$
25X + 231 = 128, No positive number for X, so IT IS IMPOSSIBLE!!!!

(b) By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 40% and the CPI of load/store and branch instructions is reduced by 30%? [6]

Execution time after improvement = $(50*0.6 + 110*0.6 + 80*2.8 + 16*1.4) * 10^6 / 2*10^9 = 171.2 * 10^{-3}$ sec, Performance is improved by 49.5%