Building Blocks of a Flip-Chip Integrated Superconducting Quantum Processor

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Abstract. We have integrated single and coupled superconducting transmon qubits into flip-chip modules. Each module consists of two chips — one quantum chip and one control chip — that are bump-bonded together. We demonstrate time-averaged coherence times exceeding 90 µs, single-qubit gate fidelities exceeding 99.9%, and two-qubit gate fidelities above 98.6%. We also present device design methods and discuss the sensitivity of device parameters to variation in interchip spacing. Notably, the additional flip-chip fabrication steps do not degrade the qubit performance compared to our baseline state-of-the-art in single-chip, planar circuits. This integration technique can be extended to the realisation of quantum processors accommodating hundreds of qubits in one module as it offers adequate input/output wiring access to all qubits and couplers.

1. Introduction

The realisation of superconducting quantum processors with arrays of increasing numbers of qubits faces several interesting engineering and physics challenges [1, 2, 3]. From the hardware perspective, scaled-up circuit designs and fabrication processes must not degrade the device performance, which otherwise would adversely affect the fidelity of quantum algorithms. This already becomes non-trivial at the scale of dozens of interconnected qubits, which requires intricate routing of the input/output microwave circuitry.

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In conventional devices fabricated on a single chip, one approach to routing signal lines is to implement signal crossovers using superconducting air-bridges [4, 5, 6]. Furthermore, to minimise signal crosstalk, transmission lines can be enclosed in elongated 'tunnels', which connect the ground planes on either side of the lines [4]. While feasible in small-scale circuits, these techniques alone seem insufficient for scaling up further. Monolithic integration, featuring buried multi-layer superconducting wiring, is an appealing solution [7]; however, this technology has not been demonstrated in coexistence with high-performance superconducting qubits.

Two other scalable 3D-integration approaches are multi-chip (flip-chip or interposer chip) circuits and out-of-plane wiring [8, 9, 1, 2, 10, 11, 12, 13, 14, 15, 16]. Both approaches have the advantage that the chip hosting the quantum circuitry can be fabricated separately, with minimal extra processing that risks degrading qubit performance.

Multi-chip implementations [8, 9, 1, 2, 10, 11, 12] typically separate the quantum and the input/output wiring circuitry onto different chips. These chips are then connected to each other in a multi-chip module by flip-chip bump-bonding techniques. This enables flexible signal routing from the perimeter of the wiring chip to the capacitive, inductive, or galvanic point of contact with the quantum chip. Combined with superconducting through-silicon-via technology for grounding and signal routing [17], this technique would enable higher-density wiring with connections from the entire back plane of the wiring chip, rather than solely from the perimeter.

Out-of-plane wiring implementations eliminate the need for multiple chips, but instead deploy, e.g., spring-loaded [13, 14, 15] or coaxial [16] pins that approach the chip perpendicularly. Such implementations yield direct access to components within the two-dimensional qubit array, obviating the need of routing from the edges of the chip.

In this paper, we demonstrate superconducting quantum devices in a scalable architecture by integrating them into a flip-chip module comprised of two silicon chips, which we denote as the control (C) chip and the quantum (Q) chip, see fig. 1(a-c). The device consists of fixed-frequency aluminium transmon qubits and a flux-tunable parametric coupler on the Q-chip. These components are capacitively and inductively coupled to the control lines (XY and Z, respectively) and qubit-readout resonators located on the C-chip. The attained qubit performance is near the state of the art for flip-chip devices. We characterise single-qubit and two-qubit (CZ) gates with average fidelities of 99.97% and 98.66%, respectively. The measured average T_1 relaxation time in single-qubit devices is as high as $110 \,\mu s$, which, notably, is not degraded compared to our baseline single-chip devices [18, 19, 20] and comparable to state-of-the-art 3D-integrated devices reported by other groups [9, 1, 2, 21, 22, 23, 11, 3]. Moreover, we discuss device parameter sensitivities due to variations in the interchip spacing.

2. Design and Simulation Workflow

The design process of the devices in this work typically begins by determining the target parameters at the Hamiltonian level (qubit and coupler $|0\rangle$ -to- $|1\rangle$ transition frequencies f_{01} ,

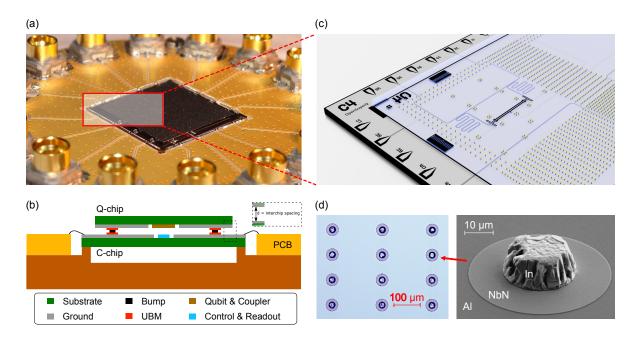


Figure 1. Flip-chip module. (a) Photograph of a flip-chip module within the centre cut-out of a printed circuit board (PCB), mounted in a microwave package (lid not shown). (b) Simplified cross-sectional illustration of the flip-chip module (not to scale). The quantum chip (Q-chip) hosts qubits and couplers, i.e., any elements containing Josephson junctions. The control chip (C-chip) hosts the input/output wiring, i.e., control lines (XY and Z), readout resonators, and readout feedlines. The two chips are separated by arrays of bumps that provide galvanic connection and mechanical support. The module is mounted into a copper sample box with a recess below the chip, and the C-chip is wire-bonded to the PCB. (c) Illustrated 3D model of the flip-chip module with the substrate of the Q-chip rendered transparent. (d) Images of the the bump layer (In), the under-bump metallisation layer (NbN), and the wiring layer (Al) prior to bonding. Bumps have the same layout on both chips. The image on the left (right) side was taken using an optical (a scanning electron) microscope.

anharmonicities α , readout frequencies f_r , coupling rates g, Purcell-decay limit T_p , etc.). These target parameters are chosen to be similar to those of our standard single-chip devices [19]. This comparison enables us to benchmark flip-chip device performances, and also validate the accuracy of the device simulation and fabrication processes.

Next, we employ ANSYS—a finite element electromagnetic simulation software suite—to find the right geometry that corresponds to the target parameters [24]. Specifically, the ANSYS HFSS Eigenmode solver is used to predict resonator frequencies, while the ANSYS Maxwell Electrostatic solver is used to determine capacitance values between the various elements. In the simulation software, the model consists of two silicon (Si) chips that are facing each other, similar to the model shown in fig. 1(b). The chips are separated by the interchip spacing d. The metallic layer of each chip is represented by a planar sheet (zero thickness) located directly on the surface of each chip. The sheet is then given the appropriate boundary condition (for Eigenmode simulations) or excitation mode (for Electrostatic simulations). We typically aim for a convergence criterion below 0.5% for both solvers (see Section 2 of the Supplementary Materials for more details).

In practice, variations in the interchip spacing d introduced by the flip-chip bonding process leads to deviations from the target device parameters. To understand the extent to which these would affect the device parameters, we first build a simulation model with a target interchip spacing (here $d_{\text{target}} = 8 \, \mu\text{m}$). Next, two additional simulations are performed for $d = d_{\text{target}} \pm 1 \, \mu\text{m}$, i.e., 7 and 9 μm . This leads to a range of device parameters that can be compared with the target parameters. In addition, this enables us to anticipate changes in device parameters — caused by variations in d — that can lead to degraded device performance. For instance, the increase in the coupling strength between a qubit and its readout resonator when $d < d_{\text{target}}$ may lead to a Purcell-limited qubit T_1 . In such a case, we will target lower coupling strength at $d_{\text{target}} = 8 \, \mu\text{m}$ so that the qubit is not Purcell-limited for a smaller d (at least when $d > 7 \, \mu\text{m}$). Section 5.2 will discuss in more details the sensitivity of various parameters to variations in d.

3. Fabrication

The device fabrication is based on our standard qubit process at Chalmers (150 nm-thick aluminium [Al] on 280 µm-thick high-resistivity intrinsic Si) [18, 19]. The quantum (Q) and control (C) chips are connected together into a module by bump-bonding a pattern of compressible pillars of superconducting indium (In). This provides mechanical interchip separation and galvanic connection to their respective ground planes. Indium has been shown to be compatible with superconducting qubit fabrication processes [8, 25]. An under-bump-metallisation (UBM) layer of superconducting NbN separates the Al film and In pillars. The UBM is meant to act as a diffusion barrier that prevents the formation of an Al–In intermetallic state [26] and to protect the Al film from corrosion during bump fabrication. The bumps and UBM are shown in fig. 1(d).

At Chalmers, we fabricated two 2-inch wafers, one containing four C-chips (14.3 mm \times 14.3 mm) and the other containing four Q-chips (12 mm \times 12 mm). First, an Al film was deposited on both wafers by e-beam evaporation. Second, the UBM pads were deposited in a process comprised of sputtering of a 50 nm-thick NbN film on patterned resists followed by liftoff. Thereafter, the wiring layer was etched out of the Al film. As a final step, the Josephson junctions (JJs) were fabricated on the Q-wafer [18].

At VTT, In pillars on both wafers were formed by evaporation of a thick film $(8 \,\mu\text{m})$ on optically-patterned single-layer resist with a sidewall profile optimised for liftoff. After liftoff and dicing, individual chips were bonded into modules by compression at room temperature, creating superconducting electrical contacts between the chips without degrading the Al tunnel junctions and electrodes.

Again at Chalmers, the flip-chip modules were wire-bonded with Al wire to a printed circuit board (PCB) within an engineered, connectorised microwave package initially designed at ETH (see photograph in fig. 1[a] and cross-section illustration in fig. 1[b]).

4. Device Characterisation

4.1. Interchip Spacing, Chip Tilt, and Transition Temperatures

In this section, we report on the statistical analysis of the interchip spacing and chip tilt achieved in our flip-chip modules, and the superconducting transition temperatures of the materials comprising the flip-chip stack.

Deviations from the targeted interchip spacing d_{target} or non-zero tilt between the nominally parallel chip surfaces can occur due to slight variations in the bump-bonding process between different runs. We characterise these deviations non-destructively at VTT, using a scanning electron microscope, by measuring the distance z_i between the two surfaces at each of the four corners of the flip-chip module. The interchip spacing d at the centre of each module is inferred from the average of these four values, i.e., $d = (\sum_{i=1}^4 z_i)/4$. The chip tilt Δd is defined as the largest difference between z_i of any two corners, i.e., $\Delta d = \max(|z_i - z_j|)$ for $i \neq j$. The chip tilt angle $\Delta \theta$ is defined as the largest tilt angle measured between any two corners. Measurements of 17 flip-chip modules yield the following sample means and standard deviations: $d = (7.8 \pm 0.8) \,\mu\text{m}$, $\Delta d = (1.7 \pm 1.0) \,\mu\text{m}$, and $\Delta \theta = (126 \pm 76) \,\mu\text{rad}$. We refer the reader to Section 3.1 of the Supplementary Materials for more details.

Non-superconducting materials and interfaces in the flip-chip connections is a potential source of non-negligible Joule heating, especially when used for delivering inter-chip flux bias currents, which can be in the range of milliamperes. Using four-point probe measurements, we characterise the resistance of a daisy chain of 1200 bonded bump pairs, where each unit of the daisy chain consists of a planar interconnecting segment of Al and a pair of bonded In bumps with NbN UBM layers. In order to determine the superconducting transition temperatures T_c of the In bumps, we also characterise a separate daisy chain structure that omits Al and has NbN in the interconnecting planar segments. The T_c of NbN, In, and Al are observed near 12 K, 3.3 K, and 1.2 K respectively, indicating that all part of the stack are superconducting at millikelvin temperatures. Below approximately 1.2 K, we observe no resistance above the noise floor of the measurement system, which sets an upper bound of $\leq 50 \,\mathrm{n}\Omega$ per daisy chain unit. This measurement-setup-limited upper bound is comparable to the values reported in other works [8, 25]. Refer to Section 3.2 of the Supplementary Materials for the plots of temperature-dependent resistance values for the different material stacks and more details about the measurement apparatus.

4.2. Control Elements and Gate Fidelities

In this section, we demonstrate the high-fidelity single-qubit and two-qubit gates driven by the control elements on the C-chip. Figure 2(a) illustrates a flip-chip device containing two fixed-frequency transmon qubits and a frequency-tunable coupler on the Q-chip. They face the control elements (XY1, XY2, Z), readout resonators (readout 1, readout 2), and a feedthrough transmission line on the C-chip. The XY-line (or charge-line) is an open-ended coplanar-waveguide transmission line, capacitively coupled to the qubit (see the leftmost inset of fig. 2[a]) and is used for driving qubit-state transitions. The Z-line (or flux-line) is a shorted

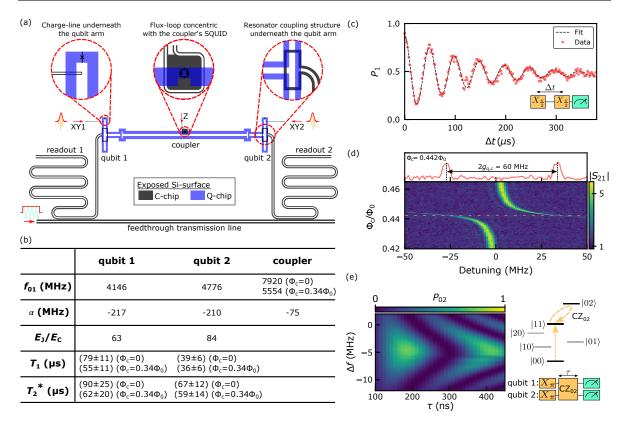


Figure 2. Two-qubit flip-chip device. (a) Illustration of two fixed-frequency transmon qubits and one frequency-tunable coupler, located on the Q-chip, and control lines (charge- or XYline, flux- or Z-line), $\lambda/4$ readout resonators, and a feedthrough transmission line, located on the C-chip. The shaded area corresponds to the exposed silicon surface on each chip. The left inset shows the charge-lines (C-chip), opposite the qubit arm (Q-chip). The middle inset shows the flux-loop (C-chip), concentric with the superconducting quantum interference device (SQUID) loop of the coupler (Q-chip). The right inset shows the open-ended part of the readout resonator (C-chip), opposite the qubit (Q-chip). (b) Summary of device parameters (all were inferred from measurements except the anharmonicity α of the coupler). See Table 8 of the Supplementary Materials for more details. (c) Oscillation in the excited-state population of qubit 1, obtained by applying a Ramsey pulse sequence with 20 kHz detuning, via XY1. (d) Avoided level crossing observed in the frequency spectroscopy of qubit 2 as the coupler is brought into resonance via the current applied to the Z-line. (e) Change in the population of state $|02\rangle$ vs modulation frequency detuning (Δf) and duration of the parametric modulation pulse (τ) . On the right, the energy diagram illustrates the CZ₀₂ transition and the gate sequence implemented in this experiment. The frequency detuning (Δf) is the difference between modulation frequency and resonant frequency of the |11>-to-|02> transition, i.e., $f_{\text{CZ}_{02}} = f_{01}(\text{q2}) - f_{01}(\text{q1}) + \alpha(\text{q2}).$

loop, concentric with the coupler's superconducting quantum interference device (SQUID) axis (see the middle inset of fig. 2[a]), and is used to provide static and alternating magnetic flux to parametrically modulate the coupler and drive two-qubit gates. The readout elements are quarter-wavelength ($\lambda/4$) transmission-line resonators that are capacitively coupled to the qubits (see the rightmost inset of fig. 2[a]) and are also coupled to a feedthrough transmission line for multiplexed readout. The table in fig. 2(b) contains a basic summary of the device parameters. More details can be found in Section 4 of the Supplementary Materials.

We first demonstrate the functionality of the XY-line for coherent driving of the qubit. Figure 2(c) shows an oscillation in the first excited state population (P_1) of qubit 1 when a 20 kHz detuned Ramsey pulse sequence is applied via XY1 [27].

Next, we turn our attention to the Z-line. By varying the direct current (DC) applied to the line, we change the magnetic flux Φ_c threading the SQUID loop, which, in turn, changes the resonant frequency of the coupler $(f_c = f_{c0} \sqrt{|\cos(\pi \Phi_c/\Phi_0)|})$, where f_{c0} is the zero-bias coupler frequency, $\Phi_0 = h/2e$ is the flux quantum, h is the Planck constant, and e is the electron charge). When the coupler is tuned into resonance with the qubit, the two systems hybridise. This results in an avoided level crossing in the frequency spectroscopy data as shown in fig. 2(d) for qubit 2, yielding the coupler–qubit coupling strength for qubit 2, $g_{q2,c} \sim 30 \, \text{MHz}$. Similarly for qubit 1, $g_{q1,c} \sim 27 \, \text{MHz}$.

We focus on one of the two-qubit gates natively available in our coupled system—the controlled-Z (CZ) gate—which implements a π phase shift on the joint qubit state $|q_1q_2\rangle = |11\rangle$ and leaves the other computational states unchanged. The CZ gate is implemented by parametric modulation of the coupler frequency via the Z-line [28, 29]. It brings the state on a round trip from $|11\rangle$ to $|02\rangle$ and back (referred to as the CZ₀₂ transition in the energy diagram of fig. 2(e)).

We bias the SQUID of the coupler at a non-zero flux offset (here, $\Phi_c = 0.34\Phi_0$), prepare both qubits simultaneously in the $|11\rangle$ -state (via XY1, XY2), apply a pulsed, alternating-current (AC) modulation to the Z-line, and measure the joint probability of the $|02\rangle$ -state (see the pulse sequence in fig. 2[e]). By varying both modulation frequency and CZ-pulse duration, we observe the expected oscillation in the population of the $|02\rangle$ -state as shown in fig. 2(e).

A common way to benchmark the performance of single-qubit and two-qubit gates is by performing randomised benchmarking (RB) experiments [30]. Reference RB experiments consist of the application of random Clifford sequences of varying lengths m to the qubits which have been prepared in an initial state (typically the ground state), followed by an inverting gate to create an overall identity operation (see fig. 3[c]). Each Clifford is a combination of several physical gates from our gate set. The decay constant of the measured sequence fidelity versus m provides an estimate of the average gate error [31, 32].

Our single-qubit gate is implemented by applying a 20 ns pulse with a cosine envelope, and is calibrated to maximise population transfer while minimising phase error [33, 34, 35]. Figure 3(a) shows results from single-qubit reference RB experiments performed simultaneously on both qubits. From this data, the average physical gate error of qubit 1 is $r_{1Q}(q1) = (2.20 \pm 0.02) \times 10^{-4}$, and of qubit 2 is $r_{1Q}(q2) = (4.28 \pm 0.06) \times 10^{-4}$, where the uncertainty represents the standard error of the fit. Furthermore, averaging the

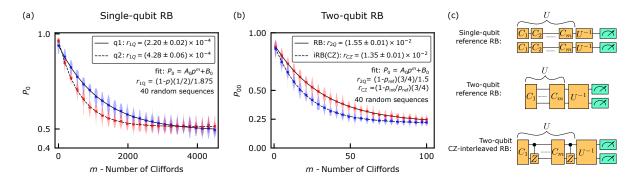


Figure 3. Characterisation of quantum gates for the two-qubit flip-chip device shown in fig. 2. (a) Single-qubit reference randomised benchmarking (RB) performed simultaneously on both qubits. Single-qubit gates are 20 ns wide pulses with a cosine envelope. The average physical gate errors on both qubits are below $r_{1Q} \approx 5 \times 10^{-4}$, equivalent to an average fidelity above $\mathcal{F}_{1Q} \approx 99.95\%$. The single-qubit interleaved RB results can be found in Table 9 of the Supplementary Materials. (b) Two-qubit reference and interleaved RB results for a 295 nswide CZ-gate with a flat-top cosine envelope and virtual-Z gates (see main text for more details). The tunable coupler is biased at $\Phi = 0.34 \, \Phi_0$. The average error of the CZ-gate in this measurement run is $r_{CZ} \approx 1.35 \times 10^{-2}$, equivalent to a CZ gate fidelity of $\mathcal{F}_{CZ} \approx 98.65\%$. (c) Gate sequences for the reference and interleaved RB experiments.

gate errors obtained from repeating single-qubit reference RB measurements over the course of 8 hours, without any additional gate recalibration in between, reveals similar results, $\bar{r}_{1Q}(q1) = (2.3 \pm 0.1) \times 10^{-4}$ for qubit 1 and $\bar{r}_{1Q}(q2) = (4.2 \pm 0.1) \times 10^{-4}$ for qubit 2, where the uncertainty is from the standard deviation of the spread (see fig. S4 in Section 4 of the Supplementary Materials). In terms of average physical gate fidelities, the 8-hour average values are $\overline{\mathcal{F}}_{q1,meas} = 1 - \bar{r}_{1Q}(q1) = (99.977 \pm 0.001)\%$ for qubit 1 and $\overline{\mathcal{F}}_{q2,meas} = 1 - \bar{r}_{1Q}(q2) = (99.958 \pm 0.001)\%$ for qubit 2.

The CZ gate consists of a 295 ns flat-top pulse with a cosine-shaped rise and fall profile, complemented by virtual Z-rotations to both qubits. The latter serves to correct for additional dispersive shifts to both qubits introduced by the coupler during modulation [36]. Figure 3(b) shows the result from implementing a reference two-qubit RB experiment reaching an average physical gate error of $r_{2Q} = (1.55 \pm 0.01) \times 10^{-2}$. As this reference RB sequence contains a mixture of single-qubit and CZ gates, a variant sequence is performed by interleaving each random Clifford with a CZ gate (see fig. 3[c] for the pulse sequence). The interleaved RB experiment can provide an estimate of the error per CZ gate, which in the case of fig. 3(b) is $r_{CZ} = (1.35 \pm 0.01) \times 10^{-2}$. Similarly, the average CZ error is characterised over the course of 10 hours. Without any gate-recalibration in-between, we obtain an average CZ error of $\overline{r}_{CZ} = (1.34 \pm 0.08) \times 10^{-2}$ or equivalently a CZ fidelity of $\overline{\mathcal{F}}_{CZ,meas} = 1 - \overline{r}_{CZ} = (98.66 \pm 0.08)\%$ (see fig. S4 in Section 4 of the Supplementary Materials).

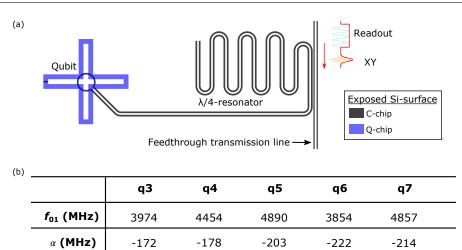
4.3. Coherence Times

Another common benchmark is the qubit coherence times, which, in the absence of other errors, set a bound on the device performance. In this section, we investigate whether the

 $E_{\rm J}/E_{\rm C}$

 T_1 (µs)

 T_2^* (µs)



100

 (98 ± 24)

 (133 ± 43)

87

 (89 ± 25)

 (100 ± 27)

Figure 4. Single-qubit coherence times in a flip-chip environment. (a) Illustration of
a fixed-frequency Xmon on the Q-chip, coupled capacitively to a $\lambda/4$ -resonator on the C-
chip. The drive (XY) and the readout pulses are coupled to the resonator via the feedthrough
transmission line. (b) Summary of the measured parameters. The coherence times were
obtained by interleaving measurements of T_1 and T_2^* repeatedly over a 48-hour period. The
table contains the mean and standard deviation of the data spread. Data were obtained from
two separate flip-chip modules. Histogram and time series of T_1 and T_2^* for each qubit can be
found in fig. S6 of the Supplementary Materials.

93

 (95 ± 31)

 (132 ± 42)

54

 (110 ± 16)

 (72 ± 24)

85

 (96 ± 29)

 (125 ± 37)

coherence time is substantially affected by the presence of another Si chip in close proximity and by the additional flip-chip fabrication process.

The table in fig. 2(b) summarises the coherence times of the two-qubit flip-chip device (shown in fig. 2[a]) obtained by interleaving measurements of relaxation times T_1 and Ramsey free-induction decay times T_2^* simultaneously on both qubits, and repeatedly over a 36-hour period. In this device, qubits 1 and 2 exhibit average $T_1 = 79 \,\mu s$ and 39 μs , respectively (at $\Phi_c/\Phi_0 = 0$). Simple estimations of the limit imposed by decays via the readout resonator and the XY-line show that both qubits in this flip-chip module are indeed Purcell-decay limited, with qubit 2 being penalised more for having stronger coupling and smaller frequency detuning from its readout resonator (see discussion in Section 4.3 of the Supplementary Materials).

To further investigate the level of qubit coherence that can be achieved in the flip-chip fabrication process outlined in Section 3, we characterised the coherence times of single-qubit flip-chip devices in a configuration shown in fig. 4(a). In this simplified design, the 'Xmon' [37] qubit-state control and readout are both performed via the feedthrough transmission line that is coupled to the $\lambda/4$ -resonator, i.e., without a separate XY-line. Basic parameters of the five single-qubit flip-chip Xmons characterised in this work are summarised in the table in fig. 4(b), with most exhibiting average values of T_1 and T_2^* above 90 μ s. In contrast to

the qubits in fig. 2(b), a simple estimation of the T_1 -limit due to relaxation via the readout resonator shows that these qubits are not yet Purcell-decay limited by the coupling to the $\lambda/4$ -resonator ($T_p > 160 \,\mu$ s, see Section 5 of the Supplementary Materials).

5. Discussion

5.1. Gate Fidelities and Coherence Times

Our demonstrated average gate fidelities in flip-chip are comparable to those obtained in single-chip devices [19] and those reported by other groups in flip-chip modules [2, 1, 9, 12, 38]. In particular, the short gate duration in Ref. [1] enabled a CZ fidelity of almost 99.6% in one qubit pair (fig. S17 in its Supplementary Materials), in a scheme that relies on having frequency-tunable qubits. The coherence-time limit to the gate fidelities in our case is estimated to be $\mathcal{F}_{1Q,inc} \sim 99.98\%$ and $\mathcal{F}_{CZ,inc} \sim 99.34\%$ according to Ref. [39] (see Section 6 of the Supplementary Materials). This indicates that the measured average single-qubit gate fidelity ($\overline{\mathcal{F}}_{1Q,meas} = (\overline{\mathcal{F}}_{q1,meas} + \overline{\mathcal{F}}_{q2,meas})/2 \sim 99.97\%$) and the average CZ gate fidelity ($\overline{\mathcal{F}}_{CZ,meas} = 98.66\%$) are still limited by both coherent and incoherent errors, with the single-qubit gate fidelities being closer to coherence-limited. Measures to improve the gate fidelities include decreasing the CZ gate duration, device redesign, and deploying more involved gate optimisation strategies [36].

Most of the single-qubit flip-chip devices in this work exhibit average $T_1 > 90 \,\mu s$ with average $T_2^* > T_1$, which is not degraded compared to our previously reported single-chip qubit coherence times for similar device geometry [18, 20]. Analysis of the participation ratio simulation results (Section 7 of the Supplementary Material) shows that the metallic layer of the second chip does cause a redistribution of electric energy from the substrate to the vacuum space in-between the chips while leaving that within the thin oxide interfaces largely unchanged. Therefore, we do not expect higher losses in flip-chip for the device geometry we use, provided that the additional fabrication steps do not add significant lossy materials nor residues. This explains the similarity between the high coherence results in flip-chip and single-chip devices. Our coherence times also compare favourably to values reported for flip-chip devices by other groups [40, 9, 21, 2, 1, 11, 12].

Further work aiming to improve qubit coherence times in general will include device design and process development, in particular to reduce the loss contribution of dielectrics. Recently, transmons made of tantalum showed promisingly long T_1 as high as $\sim 500 \,\mu s$ in planar, single chips [41, 42]. we note that Ref. [11] reported on T_1 degradation of a "floating" transmon design from $\sim 160 \,\mu s$ in the single-chip case down to $\sim 60 \,\mu s$ in the flip-chip case (see Table II & III in Appendix A of Ref. [11]), highlighting the difficulty of developing fabrication processes and designs compatible with preserved coherence.

In a scaled-up quantum processor consisting of a two-dimensional array of interconnected qubits, multiple signal lines would be routed close together on the C-chip and would also pass directly below the couplers on the Q-chip. Understanding the extent to which this would induce signal crosstalk and influence the device parameters by added capacitance,

inductance, and dielectric loss participation is a matter of ongoing investigation.

5.2. Parameter Sensitivity

The ability to design and manufacture quantum processors according to the desired specification is of paramount importance in view of the resources required to fabricate and characterise them. One challenge with flip-chip integrated devices is that the interchip spacing d plays an important role in determining the device parameters. The statistics taken for a small number of modules in Section 4.1 yield the following values for interchip spacing $d = (7.8 \pm 0.8) \,\mu\text{m}$ and chip tilt $\Delta d = (1.7 \pm 1.0) \,\mu\text{m}$. This justifies the design strategy described in Section 2 (design for $d_{\text{target}} = 8 \,\mu\text{m}$, and examine parameter changes at $d = d_{\text{target}} \pm 1 \,\mu\text{m}$), which partially allows us to include design margins toward deviations in device parameters due to module-to-module variations in d and non-parallel chips (tilt, i.e., $\Delta d > 0$) within each module.

To quantify the parameter sensitivity of the flip-chip device, we consider as an example the parameter variation in the two-qubit flip-chip device of fig. 2(a) due to a deviation of d by 1 μ m from its target value. For larger deviations, see Section 4.3 of the Supplementary Material.

According to our electromagnetic simulations, a 1 μ m variation in d results in a 2.6% variation in the qubit self-capacitance. This is in contrast to single-chip qubits, whose charging energy is determined entirely by lithography, with negligible variations. Such variations have implications for the achievable qubit-frequency precision; this is particularly important for multi-qubit processors with fixed-frequency qubits, for which the frequency allocation for neighbouring qubits has to be carefully designed to minimise crosstalk. Adding the variation due to Josephson-junction resistance variations in our current process [20], the estimated qubit-frequency variation for a 4 GHz transmon qubit becomes 4.1% (see Section 8 of the Supplementary Materials).

Other quantities are more strongly dependent on d, such as the coupling capacitance between XY-line and qubit or between readout resonator and qubit: our simulations indicate a 12% change for a 1 μ m variation in d. This, in turn, affects the readout condition and the Purcell-decay limit imposed on the qubit. However, these couplings can be designed with a safe margin to anticipate variations induced during flip-chip bonding, as briefly described in Section 2.

Likewise, to perform frequency-division multiplexed readout without crosstalk, resonators sharing the same feedthrough transmission line must be sufficiently separated in frequency. Module-to-module variations in d result in off-target resonant frequencies: in the absence of chip tilt ($\Delta d=0$), the frequencies are shifted in the same direction, but in the presence of tilt they are shifted in opposite directions and may come too close. For the coplanar-waveguide resonators in fig. 2(a), our electromagnetic simulations indicate that a 1 μ m variation in d results in a 2% variation of the resonant frequency (120 MHz for a 6 GHz resonator). The frequencies must be allocated with this clearance in mind to ensure that frequency collisions between resonators due to chip tilt can be avoided.

Looking ahead, at least two possible improvements can be made to decrease the parameter sensitivity due to variations in d. The first is to implement hard-stop spacers to better control the resulting interchip spacing and tilt [21]. Another solution is to revise the device designs: for instance, a qubit facing a bare Si surface on the C-chip has a smaller relative contribution to its capacitance from the ground plane of the C-chip than one facing a superconducting ground plane, resulting in lower sensitivity to variations in d.

5.3. Chip Deformation

The chip can also be deformed during bonding. Such deformation would result in a non-linearly varying chip separation across the module, which, if not understood properly, could adversely affect our ability to accurately target specific device parameters in a large quantum processor. Unfortunately, such deformation cannot be reliably deduced solely from the measurement of chip separation on each corner of the module. A more thorough investigation would require a full imaging of the chip surface before and after bonding. A parallel investigation track would be to compare measured device parameters to simulation and infer the local separation between the two chips at the device location.

5.4. Choice of Target Interchip Spacing

Two considerations guided our choice of target interchip spacing, $d_{\text{target}} = 8 \, \mu\text{m}$. Larger values of d_{target} result in device parameters that are less sensitive to deviations in d (as shown in Section 4.3 of the Supplementary Material). On the other hand, the lithography and deposition of indium bumps becomes impractical for $d_{\text{target}} > 8 \, \mu\text{m}$. Therefore, we aimed for a target value of $8 \, \mu\text{m}$.

6. Conclusion

We have demonstrated the basic building blocks of a flip-chip integrated quantum processor and achieved transmon coherence times and quantum gate fidelities approaching the best flip-chip device performances reported in literature [2, 1, 12]. A comparison of coherence times with those from in-house-fabricated single-chip devices indicates that the qubits are not degraded by the additional flip-chip fabrication steps at this level of performance. The pristine flip-chip environment demonstrated in this work is therefore ready to be used for the investigation and implementation of multi-qubit processors.

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8. Data Availability Statement

The data that supports the findings of this study are available upon reasonable request from the authors.

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SUPPLEMENTARY MATERIALS for

"Building Blocks of a Flip-Chip Integrated Superconducting Quantum Processor"

1. Device Hamiltonian

In this section, we establish the notation for parameters (closely following Ref. [43]) referred to in the rest of this supplementary material and the main text.

The Hamiltonian of a single transmon qubit \mathcal{H}_q is

$$\mathcal{H}_{q} = 4E_{C}\hat{n}^{2} - E_{J}\cos\hat{\phi},\tag{S1}$$

where \hat{n} and $\hat{\phi}$ are the charge number and phase operators, $E_{\rm C}=e^2/2C_{\rm q}$ is the charging energy, $E_{\rm J}=hI_{\rm c}/(4\pi e)$ is the Josephson energy, and $I_{\rm c}$ is the junction critical current.

Expanding the $\cos \hat{\phi}$ term up to the second order $\hat{\phi}^2$, we obtain the Hamiltonian of a quantum harmonic oscillator $\mathcal{H}_0 = hf\hat{a}^{\dagger}\hat{a}$, where

$$\hat{\phi} = \left(\frac{2E_{\rm C}}{E_{\rm J}}\right)^{1/4} \left(\hat{a}^{\dagger} + \hat{a}\right), \qquad \hat{n} = \frac{i}{2} \left(\frac{E_{\rm J}}{2E_{\rm C}}\right)^{1/4} \left(\hat{a}^{\dagger} - \hat{a}\right), \qquad [\hat{a}, \hat{a}^{\dagger}] = 1, \tag{S2}$$

and f is the frequency. If we also retain the fourth-order diagonal term, which is sufficient for the purpose of establishing the notation in this text, then

$$\frac{\mathcal{H}_{q}}{h} \approx f_{01}\hat{a}^{\dagger}\hat{a} + \frac{\alpha}{2}\hat{a}^{\dagger}\hat{a}^{\dagger}\hat{a}\hat{a}, \tag{S3}$$

where f_{01} is the transition frequency between the ground state $|0\rangle$ and the first excited state $|1\rangle$, and $\alpha = f_{12} - f_{01}$ is the qubit anharmonicity.

The Hamiltonian of a qubit coupled to its readout resonator (a harmonic oscillator with annihilation and creation operators b and b^{\dagger} such that $[\hat{b}, \hat{b}^{\dagger}] = 1$) is

$$\frac{\mathcal{H}_{q,r}}{h} = \frac{\mathcal{H}_{q}}{h} + f_r \hat{b}^{\dagger} \hat{b} + g_{q,r} \left(\hat{a}^{\dagger} + \hat{a} \right) \left(\hat{b}^{\dagger} + \hat{b} \right), \tag{S4}$$

where $g_{q,r}$ is the coupling strength between the qubit and the resonator. This Hamiltonian describes the coupled qubit-resonator system shown in fig. 2 of the main text.

For a coupled two-qubit system such as the one shown in fig. 2 of the main text, the Hamiltonian is

$$\frac{\mathcal{H}_{q,r,c}}{h} = \sum_{i=1,2} \frac{\mathcal{H}_{q_i,r_i}}{h} + \frac{\mathcal{H}_c}{h} + \sum_{i=1,2} g_{q_i,c} \left(\hat{a}_{q_i}^{\dagger} + \hat{a}_{q_i} \right) \left(\hat{a}_c^{\dagger} + \hat{a}_c \right), \tag{S5}$$

where \mathcal{H}_c is written in the form of eq. (S3) for the coupler, and $g_{q_i,c}$ is the coupling strength between qubit i and the coupler.

2. Various Aspects of Device Parameter Simulation

This section outlines several aspects of device simulation performed for the devices presented in this work. It complements the discussion presented in Section 2 of the main text.

2.1. Resonator Frequency

The resonance frequency of the resonator is simulated using the ANSYS HFSS Eigenmode solver. The substrate dielectric constant is set to 11.7. We typically aim for a convergence criterion in the form of *Maximum Delta Frequency Per Pass* below 0.5 %.

2.2. Resonator Coupling Quality Factor

The coupling quality factor Q_c of the resonator to the transmission line is simulated using the ANSYS HFSS Driven Modal solver with an initial mesh generated by the ANSYS HFSS Eigenmode solver [44].

In the simulation model, the resonator is coupled to the transmission line. Each end of the transmission line is connected to the ground plane via a rectangular sheet. In the Eigenmode solver, the sheet is assigned the *lumped RLC impedance* boundary condition; the resistance is set to 50Ω , and the other two elements (capacitance and inductance) are set to *None*. In the Driven Modal solver, the same rectangular sheet is instead assigned the *Lumped Port* excitation (50Ω impedance). Both ground planes and transmission lines are set to have the *perfect E* boundary condition.

The main simulation is run using the Driven Modal solver, where we use the *Broadband Adaptive Solutions* option with a $\pm 100\,\mathrm{MHz}$ frequency range centred around the expected resonance frequency (*Iterative Solver* with *Mixed Order* basis functions). The frequency sweep type is *Fast*, and we make sure that the frequency step is smaller than the expected resonance linewidth.

The Driven Modal solution setup is configured to use an initial mesh generated by the Eigenmode solver (*Import Mesh* option). We require the Eigenmode solver to solve for at least two modes, one for the resonator and another one for the feedline. As only a rough initial mesh is required, we typically set the maximum number of passes in Eigenmode solver to be 10 (with a convergence criterion in the form of *Maximum Delta Frequency Per Pass* of 1%). Apart from this, we do not impose additional mesh refinement in the solver. For the

Driven Modal solver, we typically aim for a convergence criterion in the form of *Maximum Delta S* of 0.02.

It should be noted that it is possible to run the Driven Modal solver without importing an initial mesh from the Eigenmode solver. But we frequently find that the Driven Modal solver, when run alone, cannot catch the resonance of the resonator especially when the coupling between the resonator and the feedline becomes weaker.

After the Driven Modal simulation is completed, the S_{21} parameter between the two ports of the feedline is fitted using the circle fit technique [45], which returns the internal quality factor Q_i (above 10^7 as the dielectric loss tangent of the substrate was set to be 10^{-7}), and the coupling quality factor Q_c . The decay rate of the resonator to the transmission line, κ_r , is calculated as $\kappa_r = 2\pi f_r/Q_c$.

The simulated resonance frequency f_r and the coupling quality factor Q_c are summarised in Table S1 (for the two-qubit flip-chip device) and Table S2 (for the single-qubit flip-chip devices).

Parameter	Res. 1	Res. 2
$Q_{ m c,sim}$	12723	12086
$f_{\rm r,sim}\left({ m GHz}\right)$	6.107	6.285
$\kappa_{\rm r,sim}/2\pi({ m MHz})$	0.48	0.52
f _{r,meas} (GHz)	6.210	6.370
$\kappa_{\rm r,meas}/2\pi({ m MHz})$	0.63	0.76

Table S1. Two-qubit flip-chip device—simulated and measured resonator Q_c , f_r , and κ_r . The interchip spacing is set to 6.9 μ m. $f_{r,meas}$ and $\kappa_{r,meas}$ are measured values from Table S8.

Parameter	Res. 3	Res. 4	Res. 5	Res. 6	Res. 7
$Q_{ m c,sim}$	16347	13712	16415	15703	16471
$f_{ m r,sim}\left(m GHz ight)$	5.807	6.292	6.813	5.824	6.812
$\kappa_{\rm r,sim}/2\pi({ m MHz})$	0.36	0.38	0.42	0.37	0.41
f _{r,meas} (GHz)	5.727	6.185	6.691	5.887	6.720
$\kappa_{\rm r,meas}/2\pi({ m MHz})$	0.23	0.19	0.49	0.25	0.37

Table S2. Single-qubit flip-chip device—simulated and measured resonator Q_c , f_r , and κ_r . The interchip spacing is set to 7.1 μ m. $f_{r,meas}$ and $\kappa_{r,meas}$ are measured values from Table S10.

2.3. Coupling Strength g

The coupling strengths of qubit—resonator $g_{q,r}$ and qubit—coupler $g_{q,c}$ are calculated using the capacitance values obtained from ANSYS Maxwell Electrostatics [44].

Each metallic layer in the design environment is considered as one electrode of a capacitor. The capacitance matrix has diagonal terms that represent self capacitances and off-diagonal terms that represent coupling capacitance between different objects. The self capacitance of the transmon is used to determine its charging energy $E_{\rm c}$. For the devices presented in this work, we typically aim for an energy error convergence criterion below

0.5 %. Tables S3 and S4 show the simulated capacitance matrix elements for the two-qubit and single-qubit flip-chip devices.

Parameter	q1	q2	coupler
$C_{q,self}$ (fF)	97.48	98.50	271.14
$C_{r,self}^*$ (fF)	590.78	574.23	
$C_{q,r}$ (fF)	8.37	8.37	
$C_{q,c}$ (fF)	2.38	2.38	
$C_{q,XY}$ (fF)	0.108	0.108	

Table S3. Two-qubit flip-chip device—simulated capacitance matrix elements. Interchip spacing is set to $6.9 \mu m$.

Parameter	q3	q4	q5	q6	q7
$C_{q,self}(fF)$	127	114.99	103.09	99.53	97.54
$C_{r,self}^*(fF)$	616.55	566.22	533.76	606.56	533.44
$C_{q,r}(fF)$	10.3	8.29	6.89	7.76	6.45

Table S4. Single-qubit devices—simulated capacitance matrix elements. The interchip spacing is set to 7.1 um.

The coupling capacitances of the qubit–coupler system $C_{q,c}$ and qubit–resonator system $C_{q,r}$ can be used to calculate the coupling coefficients $g_{q,c}$ and $g_{q,r}$, respectively. The coupling strength between two resonators is calculated with the aid of the following equation [46],

$$g_{1,2} = \frac{\sqrt{f_1 f_2}}{2} \frac{C_{1,2}}{\sqrt{C_{1,\text{self}} C_{2,\text{self}}}},$$
 (S6)

where the indices 1 and 2 represent either the qubit, coupler, or resonator. f_1 and f_2 are the individual resonant frequency of the coupled systems, and $C_{1,2}$ is the coupling capacitance. Note that, for the resonator's capacitance, we use $C_{r,self}^* = C_{r,self} \cdot 2/\pi$, where $C_{r,self}$ is its self-capacitance obtained from the Maxwell solver. The factor $2/\pi$ is to account for the fact that the simulation model assumes a constant voltage throughout the structure, while the actual resonator is a $\lambda/4$ resonator with a non-homogeneous field distribution.

Table S5 contains the calculated coupling strengths between qubit and resonator and coupler in the two-qubit flip-chip device. Table S6 contains those for the single-qubit devices.

Parameter	q1	q2
g _{q,r,sim} (MHz)	90	97
$g_{q,r,meas}$ (MHz)	95	115
g _{q,c,sim} (MHz)	31	34
$g_{q,c,meas}$ (MHz)	27	30

Table S5. Two-qubit device—simulated values of coupling strengths. The interchip spacing is set to 6.9 um. $g_{q,r,meas}$ and $g_{q,c,meas}$ are measured values from Table S8.

Parameter	q3	q4	q5	q6	q7
$g_{q,r,sim}$ (MHz)	86	83	82	74	79
g _{q,r,meas} (MHz)	85	84	79	80	81

Table S6. Single-qubit devices—simulated values of coupling strengths. The interchip spacing is set to 7.1 um. $g_{q,r,meas}$ are measured values from Table S10.

The coupling capacitance between the qubit and XY-line is also simulated by the Electrostatic solver, from which the quality factor of the coupling between the qubit and the XY-line $Q_c(XY)$ can be extracted,

$$Q_{c}(XY) = \frac{C_{q,self}}{\omega_{01}C_{qXY}^{2}R_{e}},$$
(S7)

where $\omega_{01} = 2\pi f_{01}$ is the angular frequency of the qubit and $R_{\rm e}$ is the resistance of external load. In our case, $R_{\rm e} = 50\,\Omega$ is assumed to be the characteristic impedance of XY-line.

2.4. Purcell-decay Limited Lifetime T_p

The Purcell lifetime due to decay via the readout resonator, i.e., T_p (read), is given by Ref. [47] as

$$\frac{1}{T_{\rm p}({\rm read})} = \kappa_{\rm r} \left(\frac{g_{\rm q,r}}{\Delta_{\rm q,r}}\right)^2,\tag{S8}$$

where κ_r is the decay rate of the resonator to the transmission line, $g_{q,r}$ is the coupling rate between the qubit and the resonator, and $\Delta_{q,r} = f_{01} - f_r$ is the qubit–readout detuning.

The Purcell lifetime due to decay via the XY-line, i.e., $T_p(XY)$, is given by Ref. [46] as

$$\frac{1}{T_{\rm p}({\rm XY})} = \frac{\omega_{01}}{Q_{\rm c}({\rm XY})} = \frac{R_{\rm e}(\omega_{01}C_{\rm q,XY})^2}{C_{\rm q,self}},$$
 (S9)

where $R_{\rm e}$ is the resistance of the external load (assumed to be 50 Ω), ω_{01} is the angular frequency of the qubit $|0\rangle$ -to- $|1\rangle$ transition, $C_{\rm q,XY}$ is the capacitive coupling between the XY-line and the qubit, and $C_{\rm q,self}=e^2/2E_{\rm c}$ is the qubit self-capacitance.

We take the combined Purcell decay rate as the sum of both rates: $1/T_p(\text{read} + XY) = 1/T_p(\text{read}) + 1/T_p(XY)$.

3. Measurements of Interchip Spacing, Chip Tilt, and Transition Temperatures

3.1. Interchip Spacing and Chip Tilt

Figure S1 shows the four corners of a flip-chip module labelled as: north east (NE), north west (NW), south east (SE), and south west (SW). The characterisation of each flip-chip module was performed by measuring the distance z_i between the two surfaces of the chips at each of these four corners. The distance measurements were performed non-destructively using a scanning electron microscope.

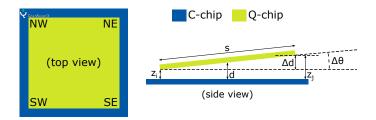


Figure S1. Simplified illustration of the flip-chip module.

The interchip spacing d, defined as the distance between the surfaces of the two chips at the centre of each module, is inferred from mean distance across the four corners. The chip tilt Δd is defined as the largest difference of z_i between any two corners, i.e., $\Delta d = \max(|z_i - z_j|)$ for $i \neq j$. This includes the tilt along the edges (NW-NE, NE-SE, SE-SW, SW-NW) and the diagonals (NW-SE, NE-SW). Furthermore, a tilt angle can be defined for each pair of corners, i.e., $\theta_{ij} = |z_i - z_j|/s$, where $s = 12 \, \text{mm}$ (16.97 mm) if the considered tilt is along the edge (the diagonal) of the module. The chip tilt angle $\Delta \theta$ is then defined as the largest tilt angle measured between any two corners, i.e., $\Delta \theta = \max_{ij} \theta_{ij}$.

Table S7 contains a summary of the measured distances z_i of the four corners of each flipchip module. There were 8 fabrication runs, producing 23 flip-chip modules in total. We only take into account measurements that were obtained using a scanning electron microscope (SEM). Therefore, we exclude the first generation FC1 as the distances were characterised using an optical microscope. We also exclude the fifth generation FC4a as the modules were not bonded with the proper tool. As a result, only 17 flip-chip modules are included in our statistical analysis of the interchip spacing and chip tilt.

From these data, we infer the following mean and standard deviation values: $d = (7.8 \pm 0.8) \, \mu \text{m}$, $\Delta d = (1.7 \pm 1.0) \, \mu \text{m}$, and $\Delta \theta = (126 \pm 76) \, \mu \text{rad}$.

Note that the different flip-chip modules listed in Table S7 were meant to investigate various device designs and flip-chip fabrication steps. Starting from the investigation of basic devices like resonators, we gradually built more complex circuitry as we integrated new learning from each experiment. Modules from FC4a onwards focus primarily on the investigation of single- and multi-qubit devices. The coherence and fidelity results shown in this work are from FC4b and FC5.

3.2. Transition Temperatures of the Flip-Chip Connections

We characterise the resistance of a daisy chain of bonded bump pairs constituting the flip-chip material stack employed in this work. The resistance is estimated via conventional lock-in amplified 4-wire voltage sensing under current bias ($f = 18 \, \text{Hz}$). The cryogenic setup for this measurement is based on a cryofree Helium-3 sorption fridge (Oxford Instruments Heliox). The temperature of the sample space is slowly swept at a rate of 0.1 K/min and measured by a pair of RuO₂ and Cernox thermometers, both recently (2021) calibrated against a primary thermometer (Al-based Coulomb blockade) in the 1.6 K - 30 K temperature range.

Figure S2 shows the resistance per bump as a function of temperature on three

#	Module		z (μm)			d	Δd	$\Delta \theta$	Remarks			
#	Module	SE	NE	SW	NW	(µm)	(µm)	(µrad)	Kemarks			
FC1	CQ1	8.5	7.8	8	8.5	8.2	0.7	58				
	CQ2	8.3	8.0	8.0	7.0	7.8	1.3	83	optical			
	C3,Q3			n	ot bonde	ed			microscope			
	CQ4	8.0	6.3	7.5	7.0	7.2	1.7	141				
FC2	CQ1	7.77	7.81	8.44	8.48	8.13	0.71	56				
	CQ2	8.05	8.28	7.89	8.12	8.09	0.39	23	CEM			
	C3,Q3			n	ot bonde	ed			SEM			
	CQ4	8.55	8.75	7.81	8.01	8.28	0.94	62				
FC3a	CQ1	7.43	7.66	8.83	9.06	8.25	1.63	117				
	CQ2	11.33	9.22	9.14	7.03	9.18	4.3	253	CEM			
	C3,Q3			n	ot bonde	ed			SEM			
	CQ4	8.88	9.14	9.31	9.57	9.23	0.69	41				
FC3b	CQ1	8.62	8.35	7.65	7.38	8.00	1.24	81				
	CQ2	7.29	8.36	7.61	8.58	7.94	1.29	89	arr.			
	C3,Q3		1	n	ot bonde	ed			SEM			
	CQ4	7.22	6.88	8.05	7.71	7.47	1.17	69				
FC4a	CQ1	9.29	9.49	14.30	10.90	11.00	5.01	418				
	CQ2	10.30	9.49	11.13	10.78	10.40	1.64	108	SEM,			
	C3,Q3		not bonded									
	CQ4	12.77	10.54	12.19	11.02	11.60	2.23	186				
FC4b	C1,Q1			n	ot bonde	ed						
	CQ2	5.1	5.6	7.3	7.1	6.3	2.2	183	CEM			
	C3,Q3			n	ot bonde	ed			SEM			
	CQ4	7.5	6.3	7.4	6.3	6.9	1.2	100				
FC5	C1,Q1			n	ot bonde	ed						
	CQ2	8.9	5.6	7.7	6.3	7.1	3.3	275	CEM			
	CQ3	8.3	7.4	6.5	6.3	7.1	2.0	150	SEM			
	C4,Q4	not bonded										
FC6	CQ1	7.9	6.4	7.6	7.0	7.2	1.5	125				
	CQ2	8.7	8.0	8.7	6.3	7.3	2.4	200	CEM			
	CQ3	9.8	8.0	9.8	7.1	8.0	2.7	225	SEM			
	CQ4	8.2	7.0	8.2	7.7	8.4	1.2	100				

Table S7. Data of the distance at each of the four corners of each flip-chip module. SEM: scanning electron microscope.

temperature ranges corresponding to the superconducting transition regions of Al, In, and NbN. The data were obtained from the measurement of two different material stacks: Al/NbN/In and NbN/In.

For the Al/NbN/In stack, the trace was measured from a daisy-chain structure containing N=1200 bumps under current excitation $I_{\rm exc}$ of 20 μ A rms. Superconducting transitions $T_{\rm c}$ of the NbN structures are well visible in the 11-12 K temperature range (see fig. S2(a)), whereas analogous In bump features are not readily visible (not shown in fig. S2) due to their negligible resistance compared to the normal-state resistance of the Al strip (as high as $30 \, {\rm m}\Omega$ at $1.3 \, {\rm K}$). The latter turns superconducting below $\sim 1.2 \, {\rm K}$ (fig. S2(b)), with measured resistance reaching nonzero level of $45 \, {\rm n}\Omega$ per bump corresponding to common-mode pickup

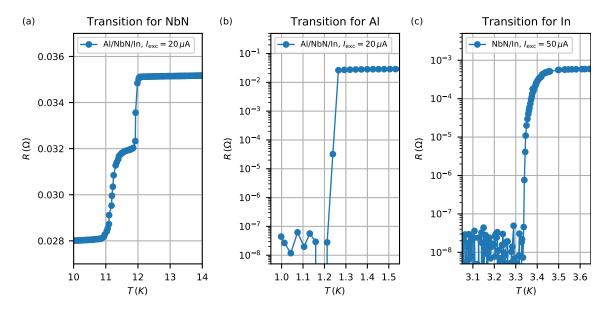


Figure S2. Resistance measurements of the flip-chip connection. The temperature range on the horizontal axes focus on the superconducting transition regions of NbN (a), Al (b), and In (c). The displayed resistance value corresponds to the resistance per bump or daisy chain unit. The vertical scales of (a) is linear, (b) and (c) are logarithmic. The data for (a) and (b) are obtained from measurements of the same Al/NbN/In material stack, while (c) is obtained from a separate NbN/In material stack.

of the voltage preamplifier (NF corporation LI-75A: -130 dB CMRR at the frequency of interest against 175Ω resistance to measurement common in our setup). The measurement uncertainty below 1.2 K provides an upper bound to the resistance of the Al/NbN/In stack to be approximately $50 n\Omega$ per bump or daisy chain unit.

For the NbN/In stack, the trace was measured from a daisy-chain structure containing N=1920 bumps under $I_{\rm exc}$ of $50\,\mu\rm A$ rms, resulting in measurement uncertainty of approximately $20\,\rm n\Omega$ per bump (below $\sim 3.3\,\rm K$). In this case, $T_{\rm c}$ of the In bumps is well visible at $\sim 3.35\,\rm K$ (with normal-state resistance $0.6\,\rm m\Omega$ per unit) due to the absence of any lower $T_{\rm c}$ superconducting components (see fig. S2(c)). Notably, an improved bonding setup with $5\,\Omega$ resistance to measurement common allows for a CMRR limit <n Ω per bump, well below the measurement uncertainty.

4. Two-Qubit Flip-Chip Device

4.1. Device Parameters

Table S8 summarises parameters of the two-qubit flip-chip device shown in fig. 2(a) of the main text. Of particular interest is the estimated Purcell-decay limit to the qubit lifetime due to relaxation via the readout resonator and the XY-line, i.e., $T_p(\text{read}+XY)$, see Section 2.4 for more detail. The limit due to the readout resonator, $T_p(\text{read})$, is calculated from measured parameters. The value of the XY coupling capacitance, required to calculate the corresponding Purcell-decay limit, $T_p(XY)$, is obtained from a simulation using the measured

Parameter	q1	q2	coupler
f ₀₁ (MHz)	4146	4776	$7920 (\Phi_{c} = 0)$ $5554 (\Phi_{c} = 0.34 \Phi_{0})$
α (MHz)	-217	-210	-75
$E_{ m J}/E_{ m C}$	63	84	
$E_{\rm C}/h({ m MHz})$	194	192	
f _r (MHz)	6210	6370	
$\kappa_{\rm r}/2\pi({ m MHz})$	0.63	0.76	
g _{q,c} (MHz)	27	30	
g _{q,r} (MHz)	95	115	
$T_1 (\mu s) (\Phi_c = 0)$	(79 ± 11)	(39 ± 6)	
$T_1 (\mu s) (\Phi_c = 0.34 \Phi_0)$	(55 ± 11)	(36 ± 6)	
$T_2^* (\mu s) (\Phi_c = 0)$	(90 ± 25)	(67 ± 12)	
$T_2^* (\mu s) (\Phi_c = 0.34 \Phi_0)$	(62 ± 20)	(59 ± 14)	
$T_{\rm p}(\mu {\rm s})({\rm XY})$	248	187	
$T_{\rm p}$ (µs)(read)	119	40	
$T_{\rm p}$ (µs)(read+XY)	80	33	
$d (\mu m)/\Delta d (\mu m)$		6.9/1.2	·

Table S8. Device parameters for the two-qubit flip-chip device shown in fig. 2(a) of the main text. Except for the coupler's anharmonicity (obtained from simulation), all values are either measured or inferred from measurement data. f_{01} , α , and f_{r} are the frequencies corresponding to the qubit $|0\rangle$ -to- $|1\rangle$ transition, anharmonicity, and the readout resonator frequency. E_{I} and E_{C} are the Josephson and charging energies inferred from the measured f_{01} and α . $\kappa_{r}/2\pi$ is the decay rate of the resonator to the transmission line estimated from the full-width at half-maximum of the readout resonator absorption tone. $g_{q,c}$ is the qubit—coupler coupling strength (see fig. 2[d] of the main text), and $g_{q,r}$ is the qubit—resonator coupling strength inferred from the shift of the resonator frequency from low to high measurement power ('punch-out' measurement, see Ref. [48]). $T_{p}(XY/\text{read})$ is the estimated Purcell-decay limited lifetime of the qubit due to relaxation via the XY-line/readout resonator, see text for more details. Values for T_{1} and T_{2}^{*} are the average and standard deviation of the statistics obtained over a certain period of time (17 hours for the data taken at $\Phi_{c} = 0$, and 36 hours for that at $\Phi_{c} = 0.34 \, \Phi_{0}$). d and Δd are, respectively, the average interchip spacing and chip tilt of the flip-chip module.

average interchip spacing of 6.9 μ m. While this can only provide an estimate, the calculated Purcell limit due to both readout and XY elements is close to the maximum measured T_1 values of both qubits.

The measured values of T_1 and T_2^* are lower when the coupler is biased at $\Phi_c = 0.34 \, \Phi_0$, i.e., when the coupler frequency is closer to the qubit frequencies, and where it is also more susceptible to magnetic-flux noise, compared to at $\Phi_c = 0$. This suggests non-negligible qubit relaxation and dephasing dynamics due to the coupler, an issue currently under investigation.

Figure S3 shows the time-series and histograms of the fluctuations of both T_1 and T_2^* values. The numbers for T_1 and T_2^* quoted in Table S8 correspond to the average and standard deviation of these values.

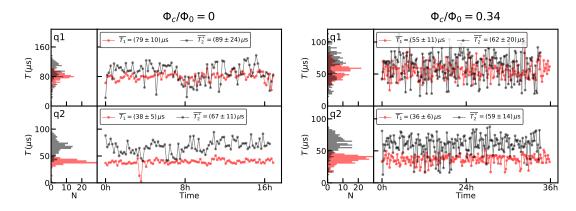


Figure S3. Temporal fluctuations of T_1 **and** T_2^* of qubits 1 and 2 in fig. 2 of the main text.

	Ref.	I	X_{π}	$-X_{\pi}$	$X_{\pi/2}$	$-X_{\pi/2}$	Y_{π}	$-Y_{\pi}$	$Y_{\pi/2}$	$-Y_{\pi/2}$
$\bar{r}_{q1}(\times 10^{-4})$	1.8	1.6	2.3	2.4	1.9	2.8	4.5	3.4	2.9	2.8
$\bar{r}_{q2}(\times 10^{-4})$	5.1	3.0	4.6	5.9	4.6	6.4	8.6	5.4	4.5	5.3

Table S9. Average error rates of single-qubit gates of qubits in fig. 2(a) of the main text estimated via interleaved RB.

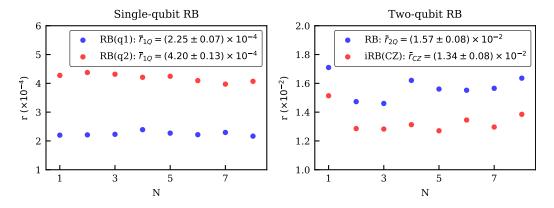


Figure S4. Error rates r for single-qubit (a) and two-qubit (b) gates obtained by randomised benchmarking with 40 random sequences repeated over 8 hours and 10 hours, respectively. Data for reference RB (\bar{r}_{1Q} , \bar{r}_{2Q}) are average physical gate errors. Numbers quoted in the legend are mean and standard deviation values.

4.2. Randomised Benchmarking Results

In addition to the reference single-qubit RB results shown in fig. 3(a) of the main text, Table S9 lists the individual single-qubit gate errors extracted from interleaved RB experiments. Figure S4 shows the fluctuations of the error rates extracted from the RB experiments over 8 hours (single-qubit RB) and 10 hours (two-qubit RB) without any further gate calibrations in between.

4.3. Change in Device Parameters for Off-Target d

Figure S5 shows the change in simulated parameters of the two-qubit flip-chip device for larger deviation of interchip spacing from the target design value ($d_{\text{target}} = 8 \,\mu\text{m}$). The purpose

is to give the reader an idea of how the various parameters behave under such circumstances.

Apart from the interchip spacing value d, the rest of the device geometries are fixed. The value of $E_{\rm J}$ for each qubit is determined from the measured qubit frequency and anharmonicity values for this device. We carried out the electromagnetic simulation using the ANSYS software suite, and calculated the device parameters using the techniques outlined in Section 2 of this Supplementary Material.

First, we note that the qubit-XY coupling capacitance $C_{q,XY}$ increases with decreasing d, similar to the increase in the capacitance of a parallel-plate capacitor when the plates are nearer to each other. The reasoning for the qubit self-capacitance $C_{q,self}$ is more subtle, as there are contributions from both Q-chip (ground plane) and C-chip (ground plane, resonator, XY). In our case, there is a substantial increase in the C-chip contribution as both chips are brought closer together, which leads to the behaviour shown in fig. S5.

The opposing trends between the qubit and resonator frequencies are more interesting. For the qubit, its inductive energy is dominated by the junction Josephson energy E_J , which, in our case, is a fixed value. As the chips are brought closer, the increase in $C_{q,self}$ leads to lower charging energy E_C , and consequently lower f_{01} . Similarly, the resonator capacitance C_r increases with decreasing d. Crucially though, the inductive energy of the resonator, which is a transmission line device, is stored in its geometric inductance L_r . In a flip-chip environment, L_r becomes *smaller* with decreasing d, and the overall effect is such that the resonator frequency $(f_r = 1/(2\pi\sqrt{L_r}C_r))$ increases with decreasing d.

The behaviour of the Purcell limits $[T_p(XY), T_p(read)]$ as a function of d are mainly determined by the interplay between the various parameters described in eqs. (S9), and (S8). As a result, they could behave differently for different parameter combinations. This difference is clearly visible in comparing the response of the combined Purcell limit $T_p(read + XY)$ between qubit 1 and qubit 2 as shown in fig. S5.

Finally, we note that even if we achieved an on-target interchip spacing, qubit 2 is Purcell-limited to $\approx 37 \,\mu s$. As discussed previously, this is due to a smaller-than-expected qubit-resonator detuning $|\Delta_{q,r}|$ caused by an off-target junction size in this fabrication run.

5. Single-Qubit Flip-Chip Device

5.1. Device Parameters

Table S10 summarises the parameters of the single-qubit flip-chip devices discussed in Section 4.3 of the main text. Here, the measured T_1 values are similar to what we regularly achieve in single-chip devices (and T_1 is not limited by Purcell decay). Figure S6 shows the histogram and the time-series of T_1 and T_2^* from each single-qubit device.

6. Coherence-time limits for gate fidelities

To find the coherence-time limits for the gate fidelities discussed in Section 5.1 of the main text, we use the results derived in Ref. [49]. There, it is shown that, to first order in the ratio

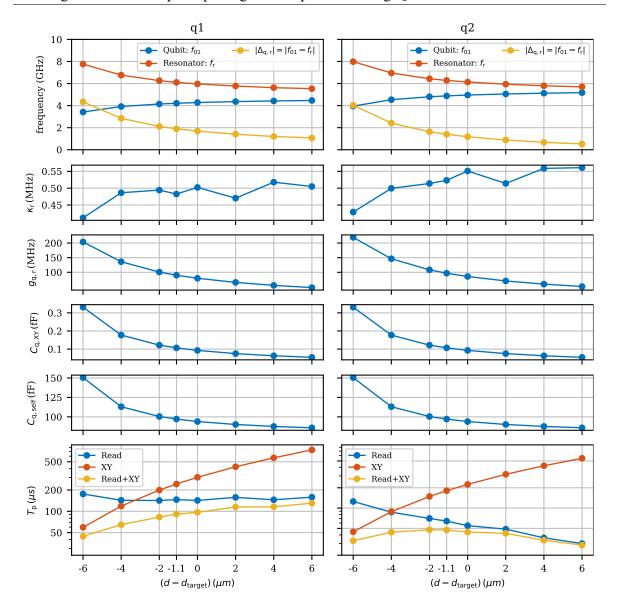


Figure S5. Effect of off-target interchip spacing on the device parameters of the two-qubit flip-chip device shown in fig. 2(a) of the main text. Plots in the same row (column) share the same y-axis (x-axis). Here $d_{\text{target}} = 8 \, \mu \text{m}$ is the target value for interchip spacing used during the design process. The mark for $d - d_{\text{target}} = -1.1 \, \mu \text{m}$ corresponds to the actual value of interchip spacing achieved for this device (i.e., $d = 6.9 \, \mu \text{m}$).

 τ/T of the gate time τ and the time-scale T of the dissipation, the average gate fidelity for an N-qubit gate affected by relaxation and dephasing is

$$\mathcal{F}_{N,\text{inc}} = 1 - \frac{d\tau}{2(d+1)} \sum_{k=1}^{N} \left(\frac{1}{T_1^{(k)}} + \frac{1}{T_{\varphi}^{(k)}} \right), \tag{S10}$$

where $d=2^N$ is the dimension of the Hilbert space for the N qubits, T_1^k is the relaxation time of qubit k, and T_{φ}^k is the pure dephasing time of qubit k. Note that this expression is the same for all N-qubit gates, as long as their dynamics are restricted to the computational subspace.

Using eq. (S10) and $1/T_2^* = 1/2T_1 + 1/T_{\varphi}$, we have that the single-qubit (N = 1) gate

Parameter	q3	q4	q5	q6	q 7
f_{01} (MHz)	3974	4454	4890	3854	4887
α (MHz)	-172	-178	-203	-222	-214
$E_{ m J}/E_{ m C}$	87	100	93	54	85
$E_{\rm C}/h({ m MHz})$	157	164	186	196	195
f _r (MHz)	5727	6185	6691	5887	6720
$\kappa_{\rm r}/2\pi({\rm MHz})$	0.23	0.19	0.49	0.25	0.37
g _{q,r} (MHz)	85	84	79	80	81
T_1 (µs)	(89 ± 25)	(98 ± 24)	(95 ± 31)	(110 ± 16)	(96 ± 29)
T_2^* (µs)	(100 ± 27)	(133 ± 43)	(132 ± 42)	(72 ± 24)	(125 ± 37)
$T_{\rm p}$ (µs)(read)	294	356	169	411	220
$d (\mu m)/\Delta d (\mu m)$		7.1/3.3	7.1/2	.0	

Table S10. Parameters for the single-qubit flip-chip devices discussed in Section 4.3 of the main text. A description of each parameter can be found in the caption of Table S8.

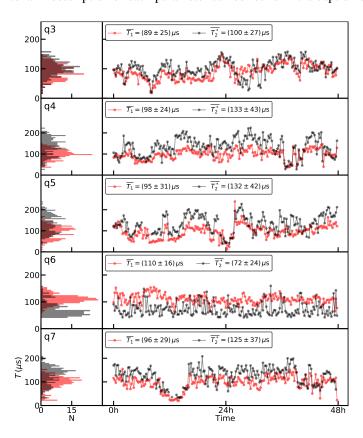


Figure S6. Temporal fluctuation of T_1 **and** T_2^* from the single-qubit devices in Table S10.

fidelity is given by

$$\mathcal{F}_{1Q,\text{inc}} = 1 - \frac{\tau_{1Q}}{3} \left(\frac{1}{2T_1} + \frac{1}{T_2^*} \right)$$
 (S11)

and the two-qubit (N = 2) gate fidelity is

$$\mathcal{F}_{2Q,inc} = 1 - \frac{2\tau_{2Q}}{5} \left(\frac{1}{2T_1^{(q1)}} + \frac{1}{T_2^{*(q1)}} + \frac{1}{2T_1^{(q2)}} + \frac{1}{T_2^{*(q2)}} \right).$$
 (S12)

Since the CZ gate as implemented here has the system temporarily leaving the computational subspace when the initial state is $|11\rangle$, this expression will be slightly modified [50]. However, the difference in the impact of decoherence on $|11\rangle$ and $|02\rangle$ is not large, so eq. (S12) remains a good approximation.

Inserting the gate time $\tau_{1Q}=20\,\mathrm{ns}$ and the average values for T_1 and T_2^* at $\Phi_c=0.34\,\Phi_0$ for qubits 1 and 2 from Table S8 in eq. (S11) yields that the coherence-time limit for single-qubit gates was $\mathcal{F}_{q1,\mathrm{inc}}\sim 99.983\%$ for qubit 1 and $\mathcal{F}_{q2,\mathrm{inc}}\sim 99.979\%$ for qubit 2. From this, we calculated the time-coherence limit to single-qubit gate fidelity quoted in the main text, i.e., $\mathcal{F}_{1Q,\mathrm{inc}}=(\mathcal{F}_{q1,\mathrm{inc}}+\mathcal{F}_{q2,\mathrm{inc}})/2\sim 99.98\,\%$. Similarly, inserting the gate time $\tau_{2Q}=295\,\mathrm{ns}$ and these coherence times in eq. (S12) yields that the coherence-time limit for two-qubit gates was $\mathcal{F}_{2Q,\mathrm{inc}}\sim 99.34\%$.

7. Participation Ratio Simulation

This section focuses on the simulated participation ratio p_i of the different domains of a coplanar-waveguide (CPW) cross-section in the single-chip and flip-chip situations. We show that, for the typical CPW geometry, interchip spacing d, and lossy dielectric parameters used in this work, there is no expected degradation in the resulting Q-factor. By extending the analysis to small values of d, the p_i -value of one of the lossy interfaces is increased substantially, leading to an equivalent Q-factor that would become even worse than the equivalent single-chip Q-factor.

The participation ratio p_i of domain Ω_i is defined as the fraction of its electric energy w_i and the total electric energy w of the whole domain [51, 52, 53, 54, 55, 56], i.e.,

$$p_i = \frac{w_i}{w}, \qquad w_i = \int_{\Omega_i} \epsilon_{\mathbf{r}}(\Omega_i) \left| \vec{E}(\vec{r}) \right|^2 d\vec{r}, \qquad w = \sum_i w_i,$$
 (S13)

where $\epsilon_{\rm r}(\Omega_i)$ is the relative permittivity of domain Ω_i . Together with the loss-tangent value $\tan \delta_i$ for each domain, they can be used to calculate the equivalent Q-factor,

$$\frac{1}{Q} = \sum_{i} p_i \tan \delta_i. \tag{S14}$$

The E-field of the CPW cross-section is simulated using ANSYS 2D Extractor. The modelled domains are: (1) the Si chip(s) (or Substrate), (2) the Al films for the signal line and the ground plane (or Metal), (3) the lossy dielectric interfaces (Metal-Air/MA, Substrate-Air/SA, and Substrate-Metal/SM), and (4) the rest is designated as the Air, as shown in fig. S7(b). The Metal domain is set as a perfect electric conductor and assigned as either the "Signal Line" or the "Reference Ground". The "Solve Options" setting for each of conductor is "Solve on Boundary". The initial seed mesh setting is as follows: (1) a 10 μ m maximum element length for a rectangular area enclosing the CPW section (the size is $1.5a \times a$, where a = (w + 2g), and w, g are respectively the width of the signal line, and the CPW signal-ground gap distance), (2) a 10 nm maximum element length for each $2 \times 2\mu$ m² rectangular

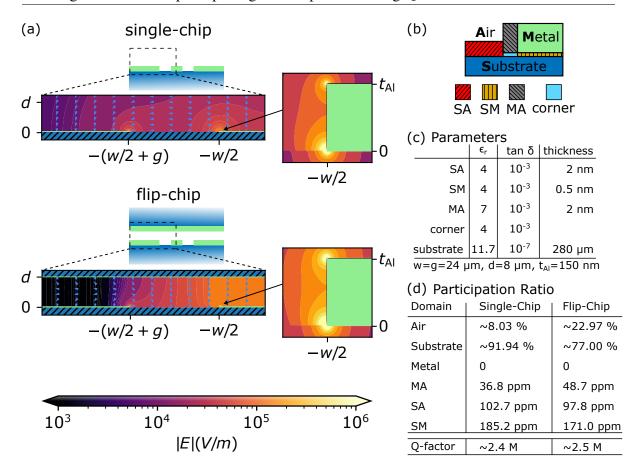


Figure S7. Comparing simulated E-field distribution in single-chip and flip-chip geometries. (a) Contour plots of the electrical field magnitude for the same CPW geometry in both single-chip and flip-chip environment. The color map is in logarithmic scale. The arrow indicates the direction of the E-field. (b) Designation of the various domains for the participation ratio simulation. (c) Parameters used in the simulation. (d) Calculated participation ratio of the different domains for both single-chip and flip-chip CPW geometries.

area enclosing the four relevant corners of the CPW structure. The solution frequency is 5 GHz, and the "CG Parameter Convergence" error is 0.1%.

The geometry and/or dielectric parameters of each domain are listed in fig. S7(c). The Air domain is considered lossless. The dielectric thicknesses and permittivity ϵ_r are our current best guess based on the information we have on our processes. The latter is not an issue for the purpose of our discussion as we are interested in the change of the p_i values going from the single-chip case (a bare CPW) to the flip-chip case (same CPW geometry, with an additional metal layer at a distance of $d = 8 \mu m$). Similarly, as long as the same $\tan \delta_i$ values are used in the comparison of single-chip vs flip-chip, then it does not affect the conclusion since they are only scaling factors, see eq. (S14).

Figure S7(a) shows the plots of the E-field magnitude in both single-chip and flip-chip situations. The additional ground plane on the top of the CPW structure redistributes the electric energy so that it appears more concentrated in the region between both chips. The table of p_i in fig. S7(d) clearly shows that a larger portion of the energy is now in the Air

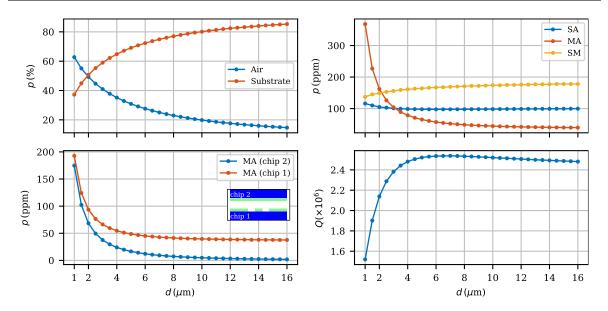


Figure S8. Simulation of participation ratio (p) of the different domains and overall quality factor (Q) for different interchip spacing (d) of a CPW geometry in a flip-chip environment. Apart from d, the rest of the parameters are identical to those used in fig. S7.

domain. Crucially, there is redistribution in the p_i of each lossy interface. Notably the MA contribution increases while both SM and SA contributions decrease. Note that the energy contribution from the domain labelled "corner" in fig. S7(b) is divided equally between the MA and the SM domains.

Using eq. (S14), the calculated Q-factor increased by $\sim 4\%$, going from the single-chip and flip-chip case. This shows that the addition of another chip in close proximity does not necessarily lead to performance degradation, provided that the additional flip-chip fabrication steps do not add more lossy layers to the MA and the SA domains. Note that the $\sim 4\%$ increase in Q-factor corresponds to $\sim 4 \,\mu s$ increase in equivalent T_1 for a 5 GHz-qubit, which could be hard to discern in view of the much larger fluctuation in the qubit T_1 ($\sim 20 - 30 \,\mu s$, see fig. S6) typically attributed to the presence of TLS impurities.

To further illustrate the impact of the additional chip on the p_i values, we ran the simulation for different values of d, from 1 μ m to 16 μ m. The results are shown in fig. S8. As d decreases, the Air p_i increases while the Substrate p_i decreases to the point that it is possible to obtain equal energy in the Air and in the Substrate (see $d=2~\mu$ m). As this happens, the contribution from the MA region also increases substantially and eventually becomes the most dominant interface for d below $\sim 2~\mu$ m. Analysing the contributions from both chips separately for large d (say $d=8~\mu$ m), the MA interface on the additional chip (labelled as chip 2 in fig. S8) contributes about 15 % to the overall MA participation ratio. However, this portion increases as the chips come closer to the point that it is similar to the contribution from chip 1 at $d\sim 1~\mu$ m. The substantial increase in contribution from the MA region for very small d leads to the degradation of Q-factor.

A drawback of this simulation is the fact that it is not based on the complete 3D model,

which would require more computational power and memory. It is possible that the 3D model would yield similar results as the transmon shape we use consist of multiple arms of CPW-like structure. Notwitstanding this issue, the Q-factor for the flip-chip case is $\sim 4\%$ higher than in the single-chip case, which is perhaps an indication of further opportunities to tune the qubit geometry for an optimised Q-factor. Given a pre-determined value of d (which is fixed by the fabrication capability), could there be a "sweet spot" for the combination of w and g that would yield an optimised Q-factor? Do the conclusions here hold if we remove the metal layer from the additional chip, thereby allowing the E-field from the device to penetrate into it? Would the 3D model simulation yield similar results as the 2D model? These are interesting problems that could be addressed in future works.

8. Sensitivity of Qubit Frequencies due to Fluctuations in $E_{\rm C}$ and $E_{\rm J}$

We describe the manner in which we arrive at a variation of \sim 4.1 % in qubit frequencies, when taking account variations in $E_{\rm J}$ and $E_{\rm C}$ (see Section 5.2 of the main text).

For a transmon qubit, the $|0\rangle$ -to- $|1\rangle$ transition frequency is by Ref. [47] as

$$hf_{01} = \sqrt{8E_{\rm J}E_{\rm C}} - E_{\rm C}.$$
 (S15)

The charging energy depends on the qubit self-capacitance, i.e., $E_{\rm C}=e^2/(2C)$, and the Josephson energy depends on the junction critical current $(I_{\rm c})$ or equivalently the junction normal-state resistance $R_{\rm N}$, i.e., $E_{\rm J}=hI_{\rm c}/(4\pi e)$ and $I_{\rm c}R_{\rm N}=\pi\Delta/(2e)$, where Δ is the aluminium gap parameter.

Consider a transmon qubit with $f_{01} = 4$ GHz, $E_{\rm C}/h = 200$ MHz, and $E_{\rm J}/h = 11000$ MHz. For the qubit design shown in fig. 2(a) of the main text, a variation in the interchip spacing of 1 μ m leads to a ~2.6 % relative change in $E_{\rm C}$.

A Josephson energy of $E_{\rm J}/h=11000\,{\rm MHz}$ requires a normal-state resistance $R_{\rm N}\sim12500\,\Omega$, which in our case, is equivalent to a junction area of $A\sim0.022\,\mu{\rm m}^2$. This translates to a variation of $\sim5.5\,\%$ in the normal-state resistance $R_{\rm N}$ or equivalently $\sim5.5\,\%$ in $E_{\rm J}$, according to fig. 4(e) of Ref. [57].

These two sources of variations are then propagated to f_{01} according to the following equation:

$$df_{01} = \frac{\partial f_{01}}{\partial E_{C}} dE_{C} + \frac{\partial f_{01}}{\partial E_{J}} dE_{J}$$

$$= \left(\frac{1}{2} \sqrt{\frac{8E_{J}}{E_{C}}} - 1\right) dE_{C} + \left(\frac{1}{2} \sqrt{\frac{8E_{C}}{E_{J}}}\right) dE_{J}$$

$$\frac{df_{01}}{f_{01}} = \left(\frac{1}{2} \sqrt{\frac{8E_{J}}{E_{C}}} - 1\right) \frac{E_{C}}{f_{01}} \left(\frac{dE_{C}}{E_{C}}\right) + \left(\frac{1}{2} \sqrt{\frac{8E_{C}}{E_{J}}}\right) \frac{E_{J}}{f_{01}} \left(\frac{dE_{J}}{E_{J}}\right).$$
(S16)

This results in $df_{01}/f_{01} \sim 4.1$ % for the stated f_{01} , $E_{\rm C}$, $E_{\rm J}$, and assuming $dE_{\rm C}/E_{\rm C} \sim 2.6$ % and $dE_{\rm J}/E_{\rm J} \sim 5.5$ %. We note in particular that the quoted $dE_{\rm J}/E_{\rm J}$ is related to the actual standard deviation while $dE_{\rm C}/E_{\rm C}$ is estimated from the simulation, as such the variation in frequency df_{01}/f_{01} should be regarded as an order of magnitude estimation.

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