An 84dB-SNDR Low-OSR 4th-order Noise-Shaping SAR with an FIA-Assisted EF-CRFF Structure and Noise-Mitigated Push-Pull Buffer-in-Loop Technique

Tzuhan Wang*, **Xie Tian***, Zhe Liu, Shaolan Li

**Equally Contributed Credits*

Georgia Institute of Technology
Atlanta, Georgia

Self Introduction

- **National Taiwan University, Taipei**
  - B.S. degree in 2016
  - M.S. degree in 2018
- **Georgia Institute of Technology, Atlanta GA**
  - PH.D. student since 2019
- **Research interests**
  - Analog and mixed-signal circuit
  - Energy efficient ADC design

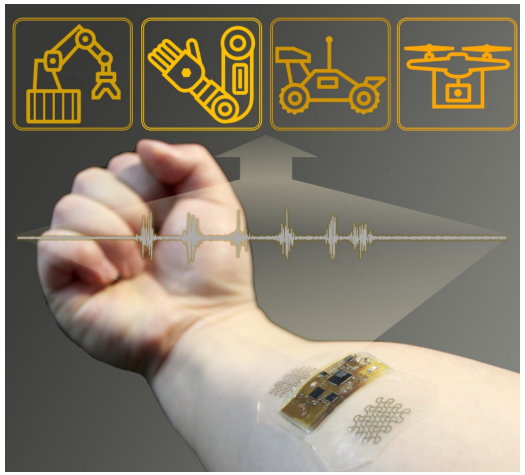
Tzuhan Wang

Outline

- Existing challenges of NS-SAR
- Proposed EF-CRFF structure for NS-SAR
- Proposed noise-cancelling buffer for NS-SAR
- Measurements results
- Conclusion

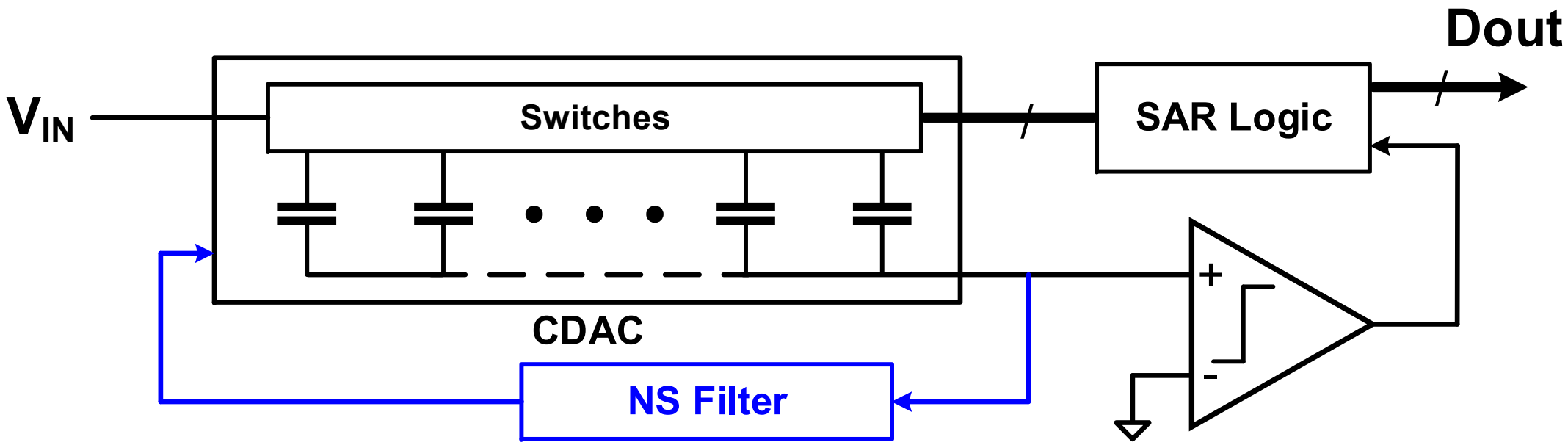
ADC Trend for Emerging Applications

- **Need from applications**
  - Internet of things
  - Healthcare/biomedical
  - Autonomous vehicles
- **Our design target**
  - SNDR > 80dB
  - FoMs > 180dB



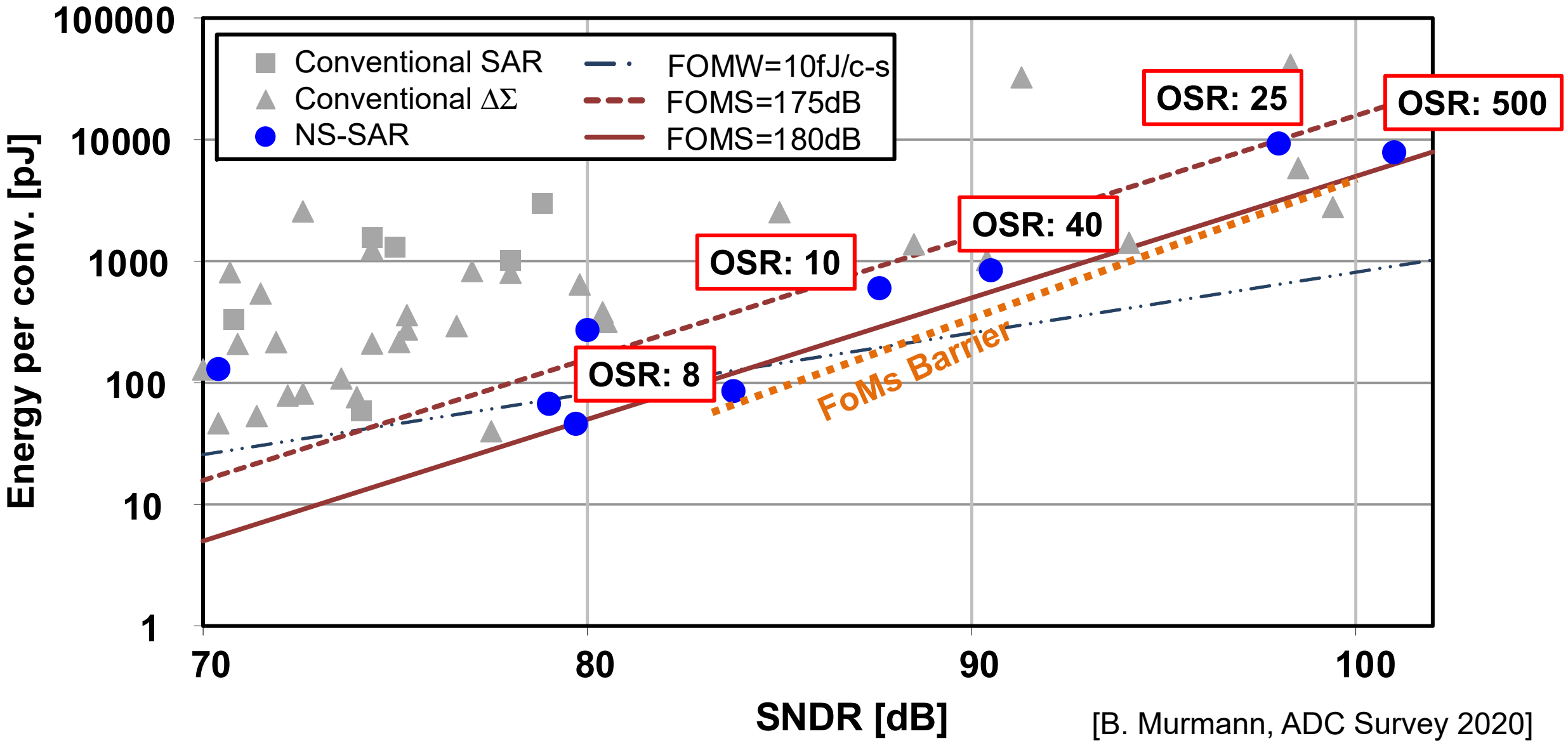
Less power more performance

Noise-Shaping (NS) SAR ADC



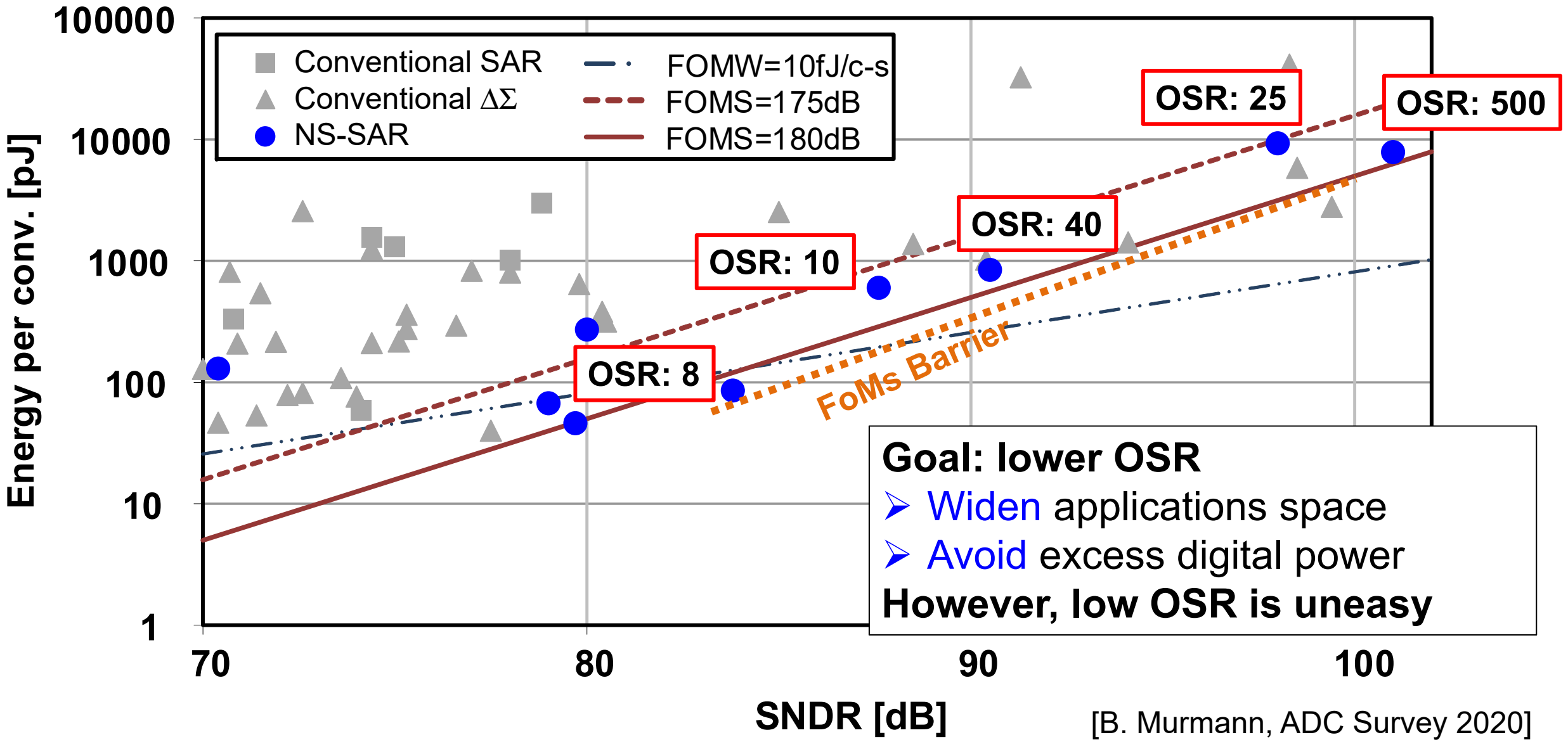
- **SAR + ΔΣ → combines NS with SAR**
  - SAR conversion → V_{RES} to NS filter → filter result feedback
  - Relaxed filter design vs. ΔΣ
  - High-resolution with mild OSR

Recent NSSAR Survey



[B. Murmann, ADC Survey 2020]

Recent NSSAR Survey

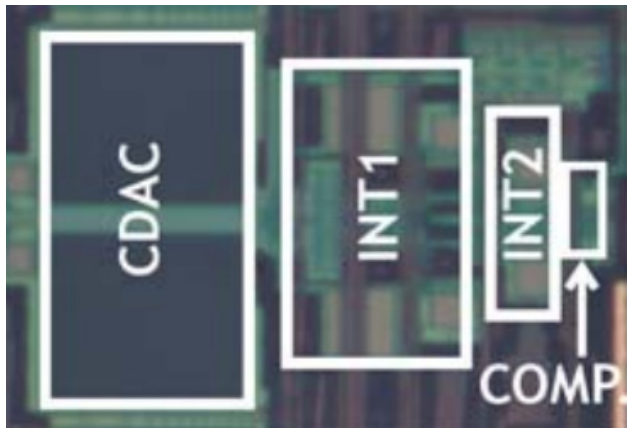


[B. Murmann, ADC Survey 2020]

Limitations of NSSAR ADC

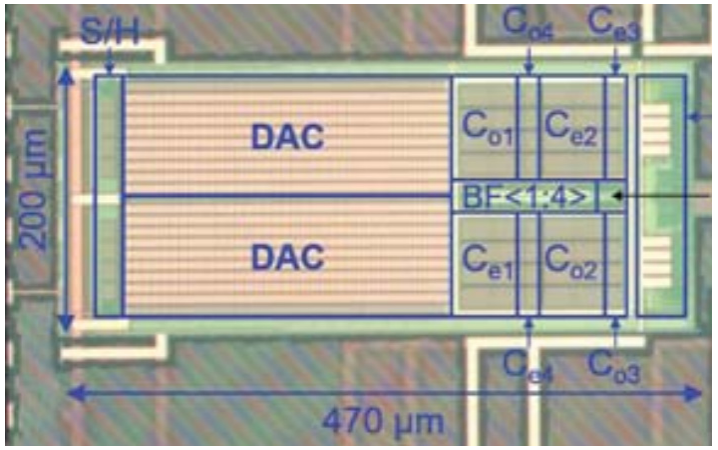
- **Recent mild OSR NSSAR ADC**

[Tang, *ISSCC* 20]



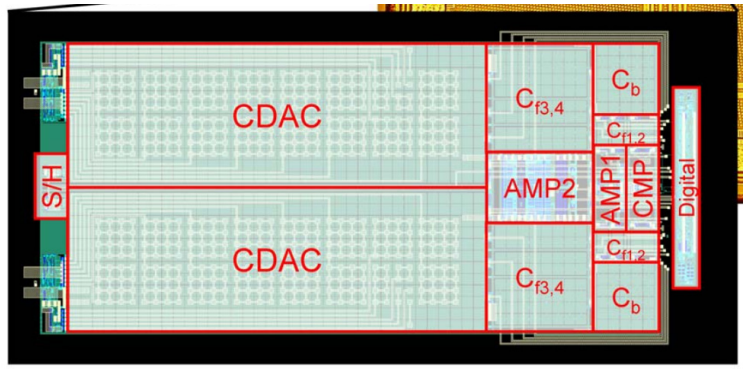
84dB SNDR, **OSR =8**
C_{IN} = 4pF

[Liu, *ISSCC* 21]



93dB SNDR, **OSR =10**
C_{IN} = 32pF

[Jie, *ISSCC* 20]



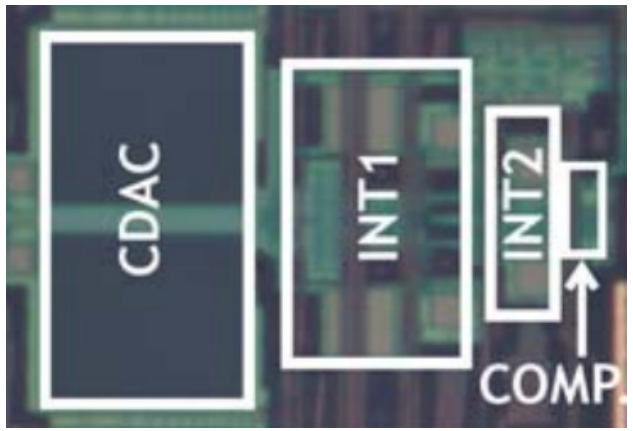
87dB SNDR, **OSR =10**
C_{IN} = 15.4pF

- **The need to achieve low OSR**
  - **Higher order NS required**
    - → Complex NS filter↑ ☹
    - → Trade off power & noise ↑ ☹
- **High cost to achieve low noise**
  - **Large CDAC: to lower kT/C noise**
    - → Area & power ↑ ☹
    - → Input driver complexity ↑ ☹

Limitations of NSSAR ADC

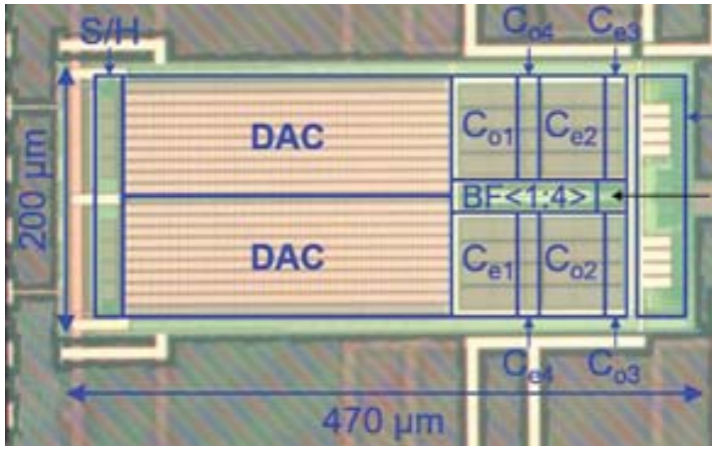
- **Recent mild OSR NSSAR ADC**

[Tang, *ISSCC* 20]



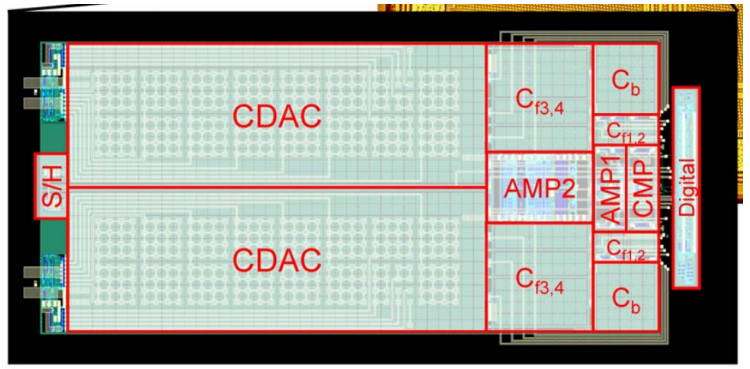
84dB SNDR, **OSR =8**
C_{IN} = 4pF

[Liu, *ISSCC* 21]



93dB SNDR, **OSR =10**
C_{IN} = 32pF

[Jie, *ISSCC* 20]



87dB SNDR, **OSR =10**

- **The need to achieve low OSR**
  - **Higher order NS required**
    - → Complex NS filter↑ ☹
    - → Trade off power & noise ↑ ☹
  - **Goal: Surpass kT/C noise barrier**
    - ➢ Less power & Less area
  - **Goal: Relax input driver requirement**
    - ➢ Easier to drive
    - → Area & power ↑ ☹
    - → Input driver complexity ↑ ☹

Solutions

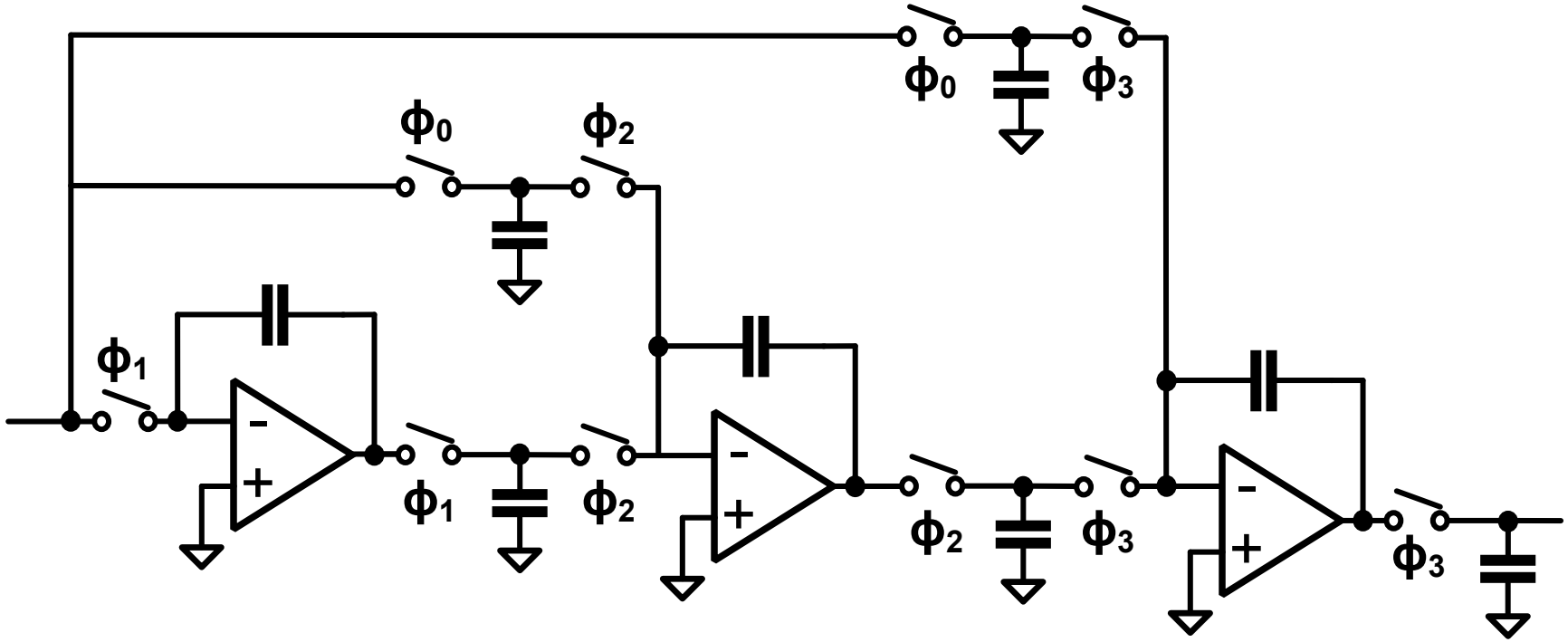
- **Bottleneck1: energy efficient high-order NS**
  - –Hybrid EF-CRFF structure
    - Open loop D-Amp assisted integration
- **Bottleneck2: low noise & input driver relaxation**
  - –Buffer-embedded NSSAR
    - Inherent noise cancellation

Outline

- Existing challenges of NS-SAR
- **Proposed EF-CRFF structure for NS-SAR**
- Proposed noise-cancelling buffer for NS-SAR
- Measurements results
- Conclusion

Prior Arts 1: High-Order CIFF NS

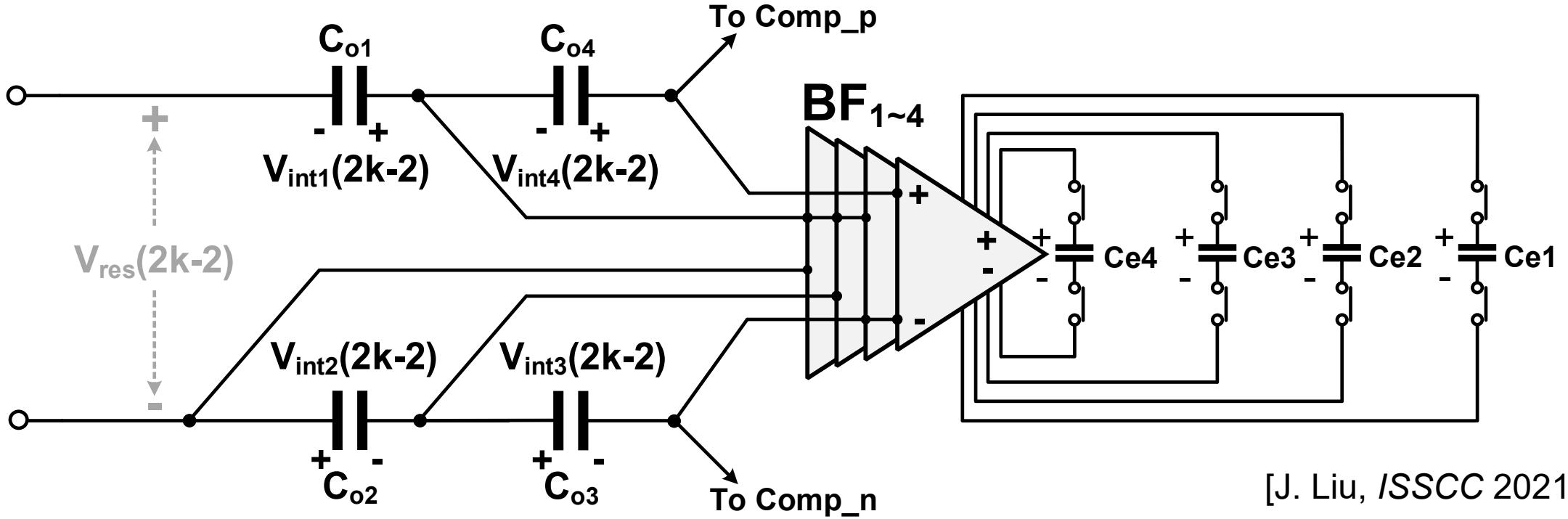
- 3rd order integrator
- Closed loop OTA: stable & sharp NTF ☺
- High-gain static amp: power & scaling unfriendly ☹



[K. Obata, *VLSI* 2016]

Prior Arts 2: Cap. Stacking Integrator

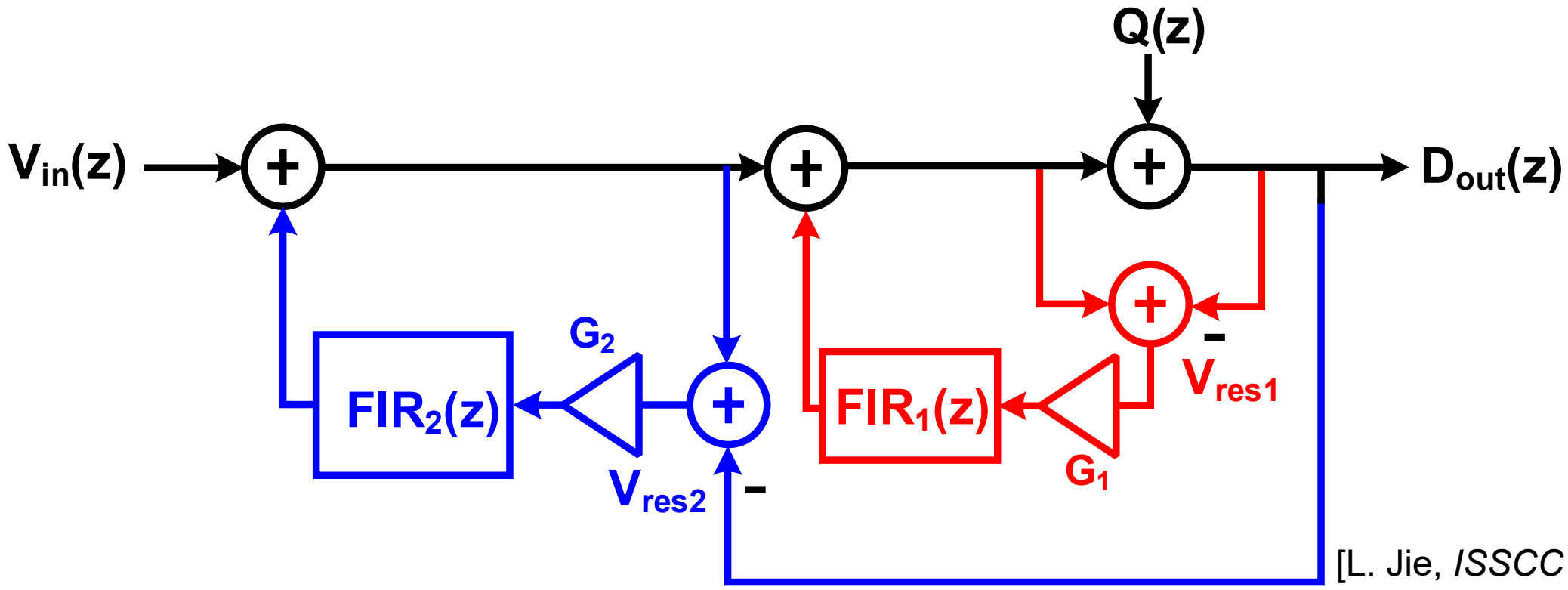
- Buffer + caps. : PVT robustness ☺
- Nearly perfect integration: sharp high-order NTF ☺
- Static power buffer: energy efficiency ☹
- Lack NTF optimization: low OSR unsuitable ☹



[J. Liu, *ISSCC* 2021]

Prior Arts 3: Nested EF Structure

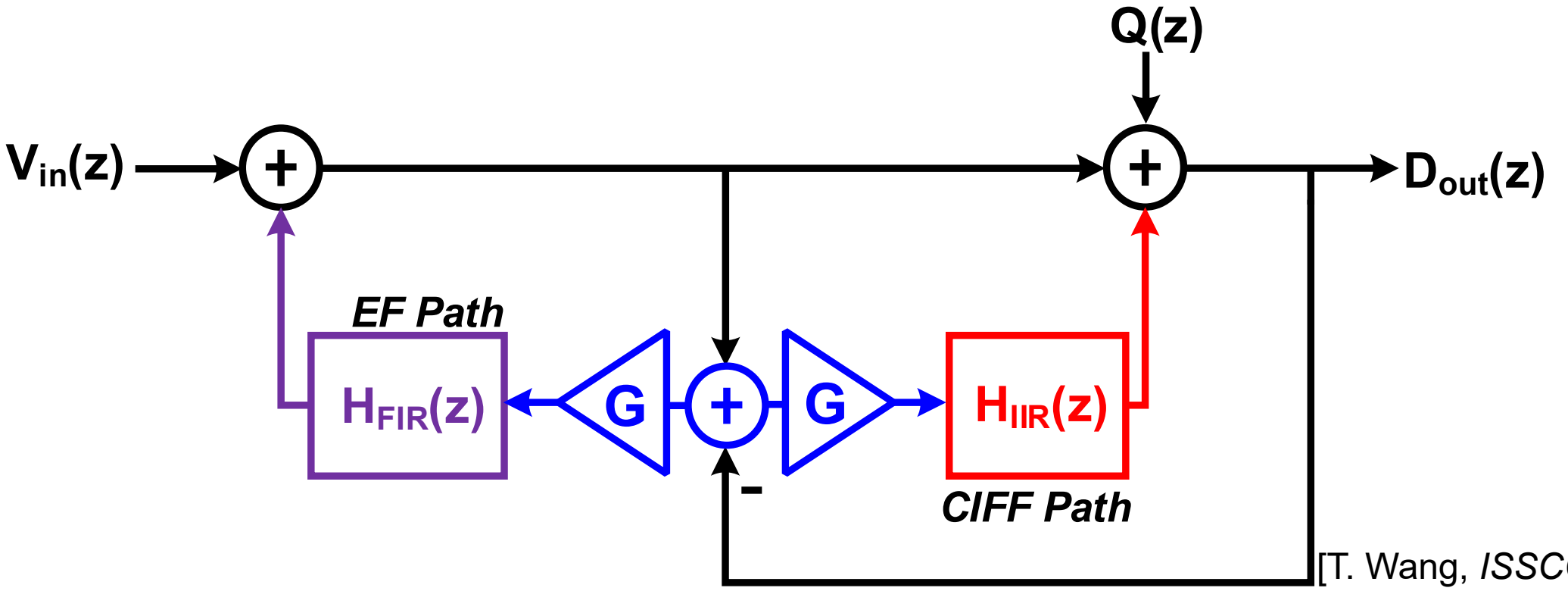
- **EF structure: V_{res} extract → FIR filter** [S. Li, *ISSCC* 2018]
- **High-order NTF, low complexity** ☺
- **SQNR fluctuation: 2 amp affect zeros** ☹



[L. Jie, *ISSCC* 2020]

Prior Arts 4: EF-CIFF Structure

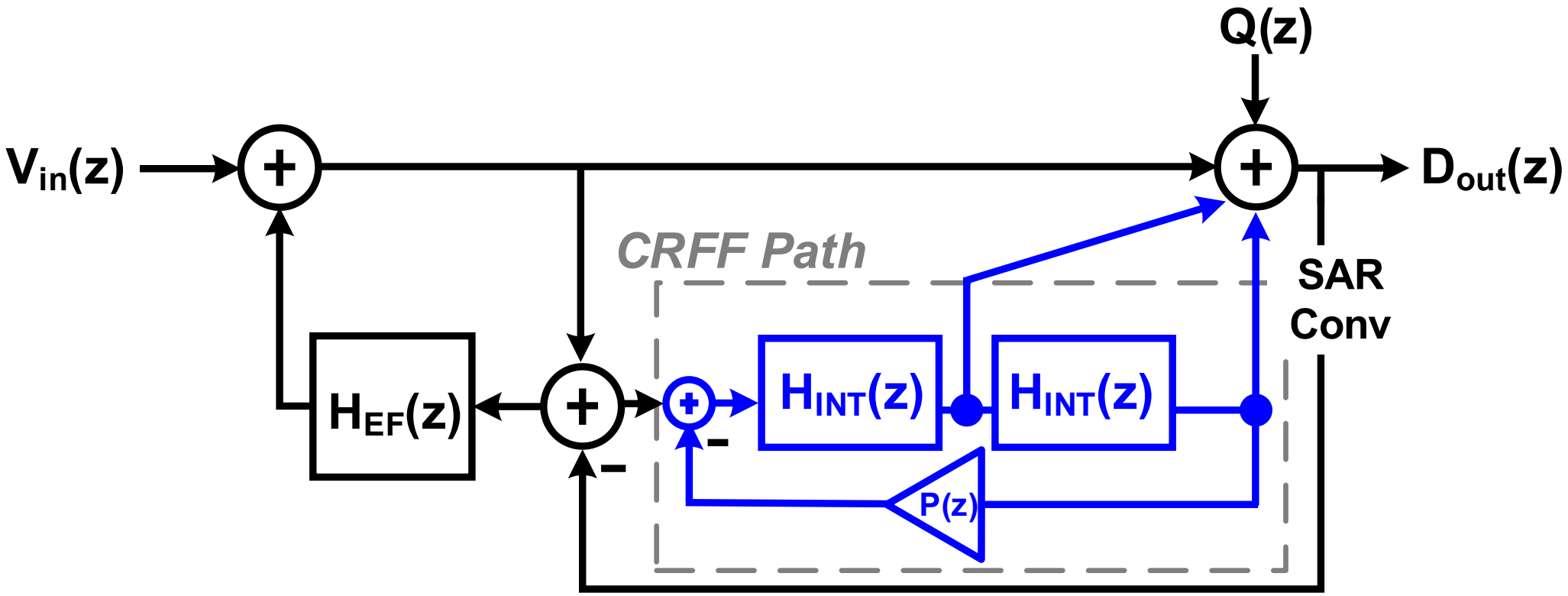
- Hybrid structure: single amp ☺
- PVT robustness against EF-EF ☺
- Limited NS order: 1st stage CIFF only ☹



[T. Wang, *ISSCC* 2021]

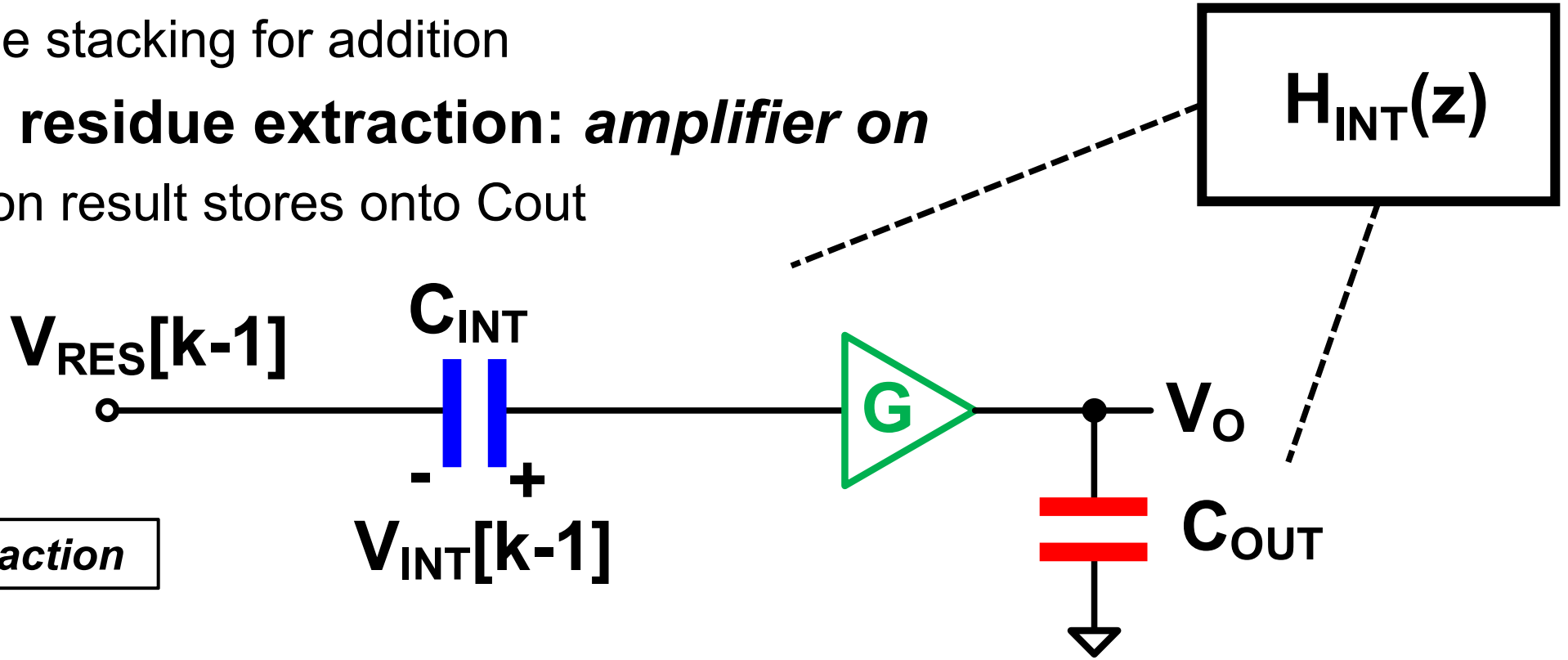
Low OSR Approach: CRFF Integrator

- **Cascade resonator feedforward (CRFF) approach:**
  - Complex zeros → optimized NTF → low OSR suitable
  - Key: energy efficient integration implementation



Proposed Integrator – Basic Model (1)

- **Integration in DT system: addition**
  - Voltage stacking for addition
- **During residue extraction: *amplifier on***
  - Addition result stores onto Cout

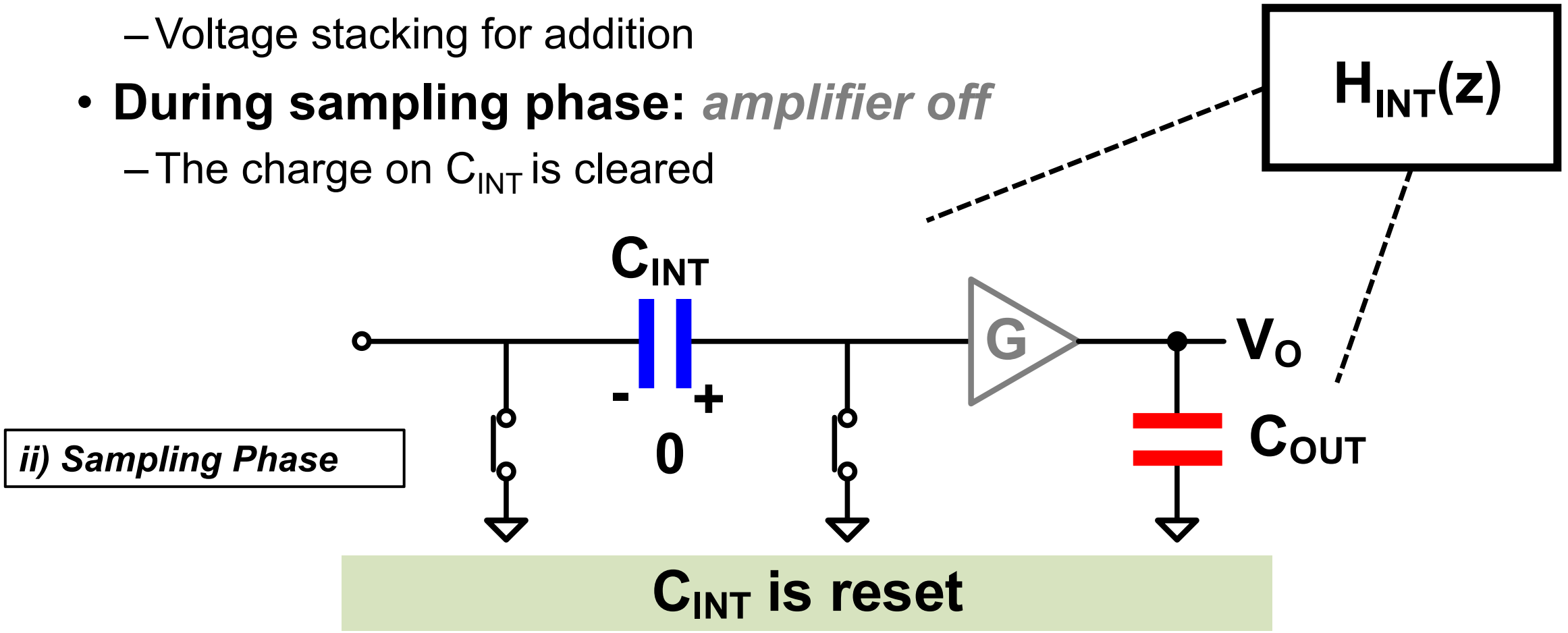


i) Residue Extraction

$$V_O = G\cdot(V_{RES}[k-1] + V_{INT}[k-1])$$

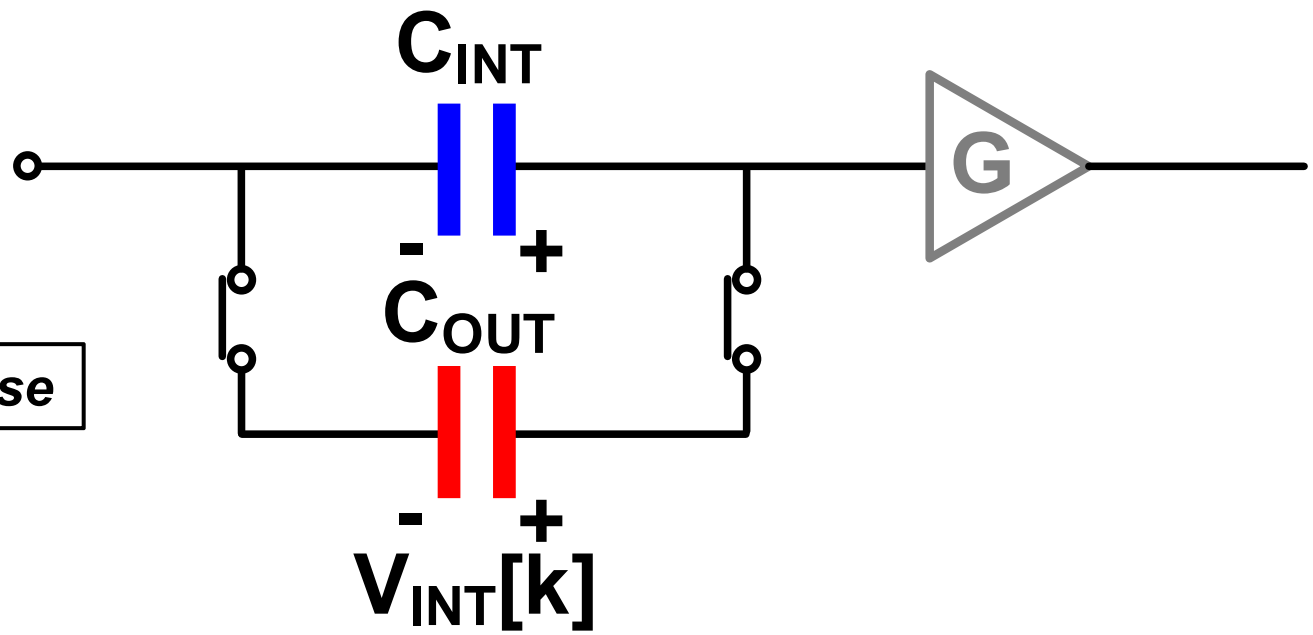
Proposed Integrator – Basic Model (2)

- **Integration in DT system: addition**
  - Voltage stacking for addition
- **During sampling phase:** ***amplifier off***
  - The charge on C_{INT} is cleared



Proposed Integrator – Basic Model (3)

- **Integration in DT system: addition**
  - Voltage stacking for addition
- **During conversion phase:** ***amplifier off***
  - Through charge sharing, integration is completed



$$H_{INT}(z)$$

$$H(Z) = \frac{1}{1 - Z^{-1}}$$

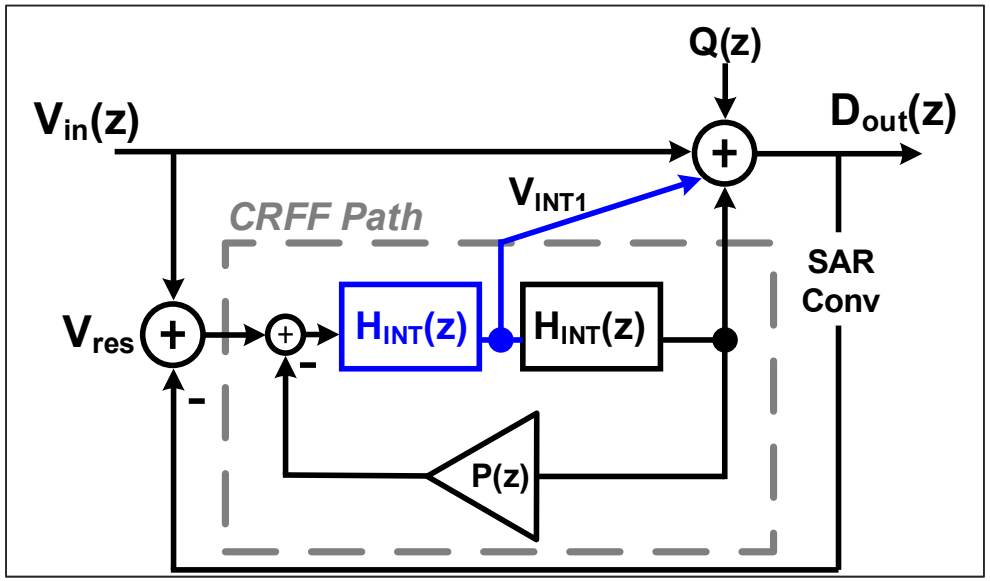
$G = 1/K = C_{INT}/C_{total}$

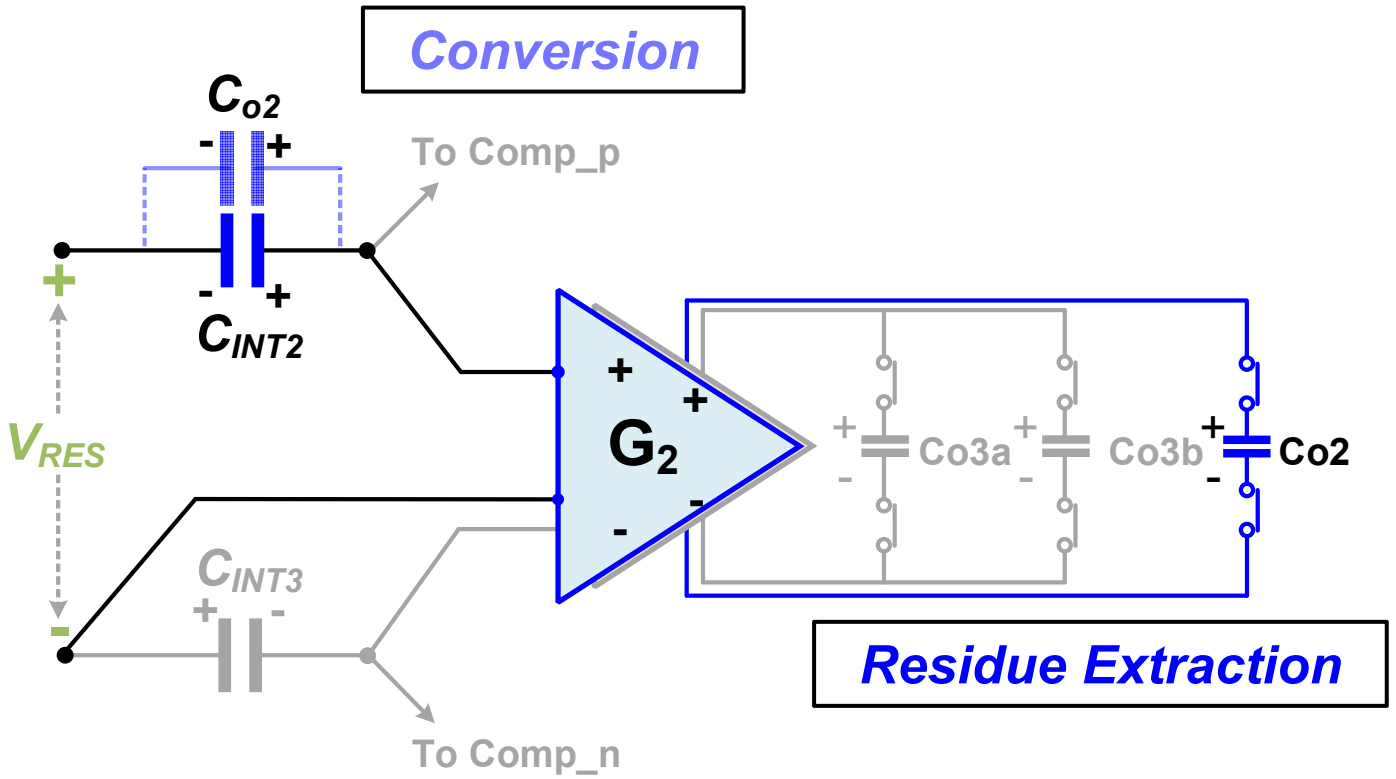
iii) Conversion Phase

$$V_{INT}[k] = G/K \cdot (V_{RES}[k-1] + V_{INT}[k-1])$$

Proposed Integrator – Basic Model (4)

- 1st and 2nd integrations performs simultaneously
- 1st - integration

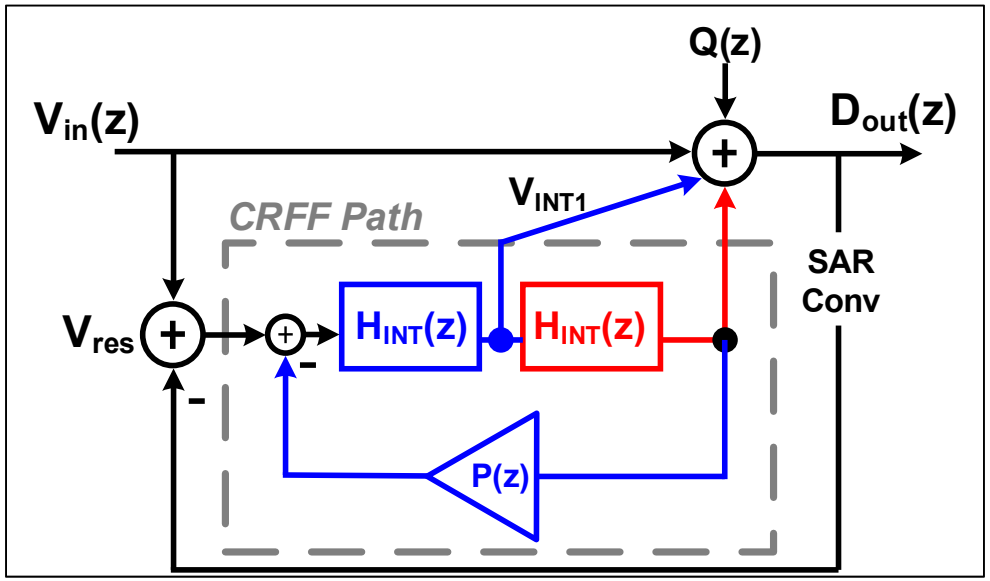


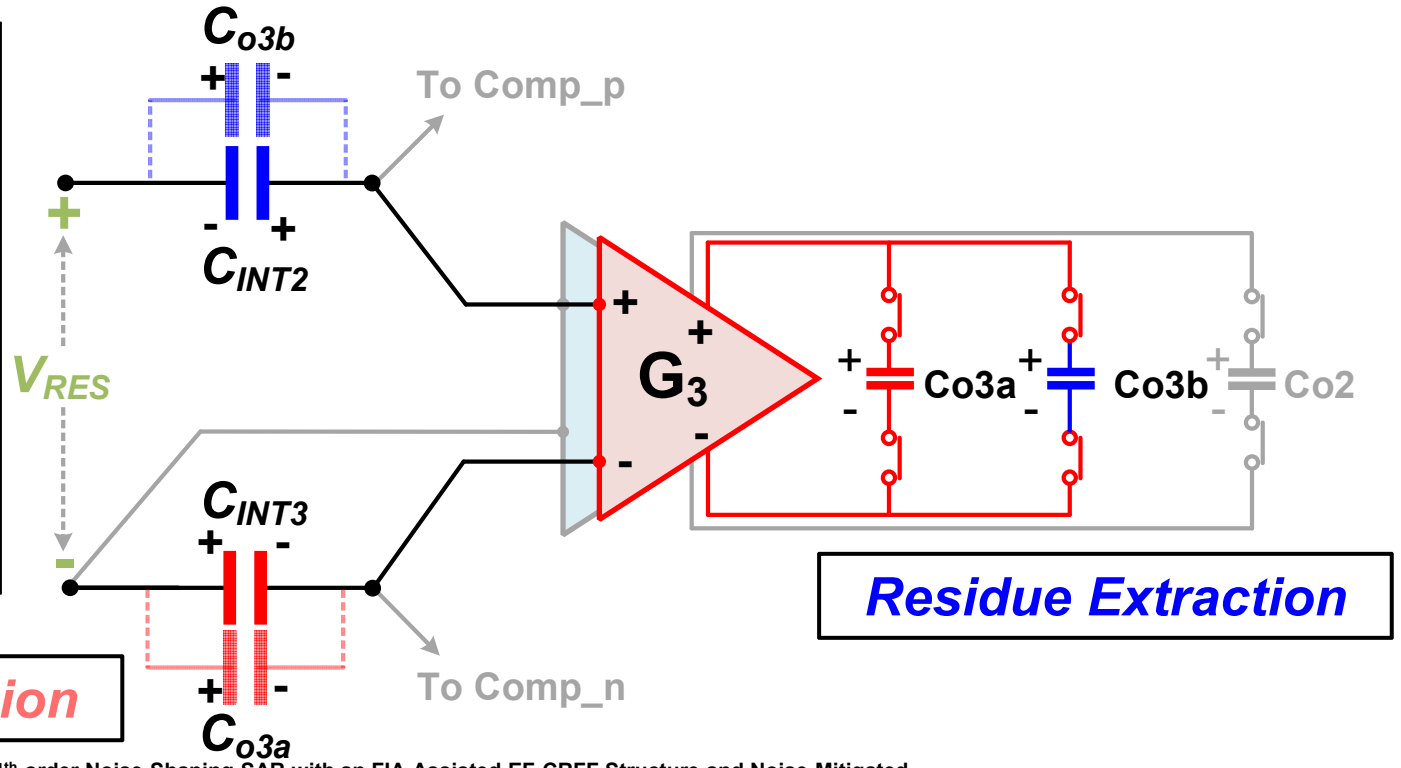


Proposed Integrator – Basic Model (5)

- 1st and 2nd integrations performs simultaneously
- 2nd - integration: CRFF → notch → optimized NTF
- Optimized NTF → low OSR ☺

$$V_{INT}[k]=G/K_1\cdot(V_{INT1}[k-1]+V_{RES}[k-1]) -G/K_2\cdot(V_{INT2}[k-1])$$



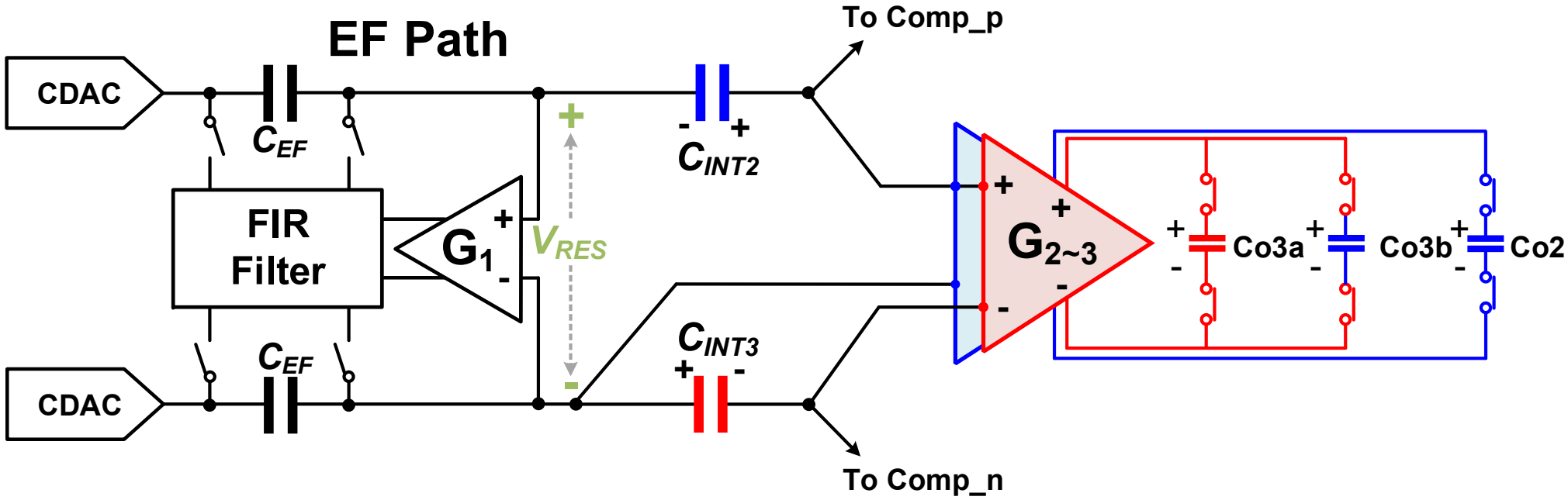


Residue Extraction

Conversion

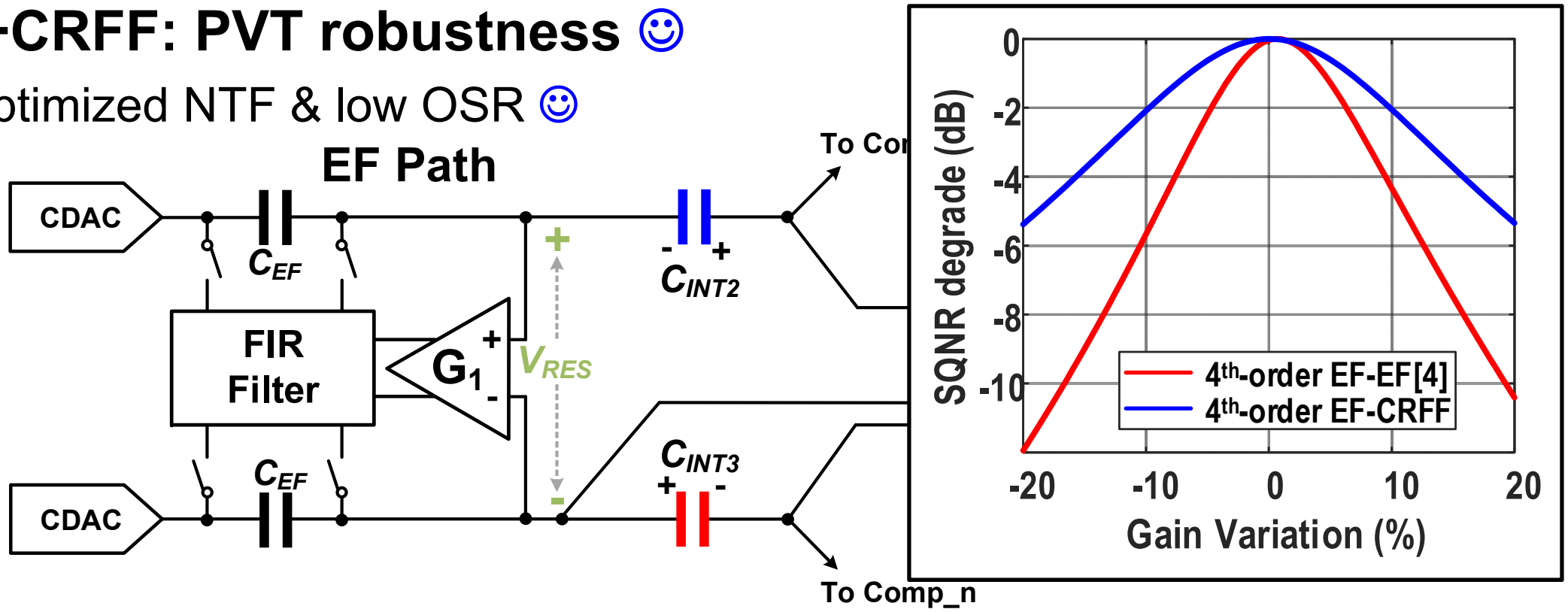
Proposed EF-CRFF Structure

- **Proposed integration**
  - Avoid ping-pong switching cap☺
  - Low input-referred noise ☺
- **EF+CRFF:**
  - Optimized NTF & low OSR ☺
- **Amp. fires only at V_{RES} ext.**
  - Fully dynamic operation ☺
  - Good energy efficiency ☺



Proposed EF-CRFF Structure

- **Proposed integration**
  - Avoid ping-pong switching cap☺
  - Low input-referred noise ☺
- **EF+CRFF: PVT robustness** ☺
  - Optimized NTF & low OSR ☺
- **Amp. fires only at V_{RES} ext.**
  - Fully dynamic operation ☺
  - Good energy efficiency ☺

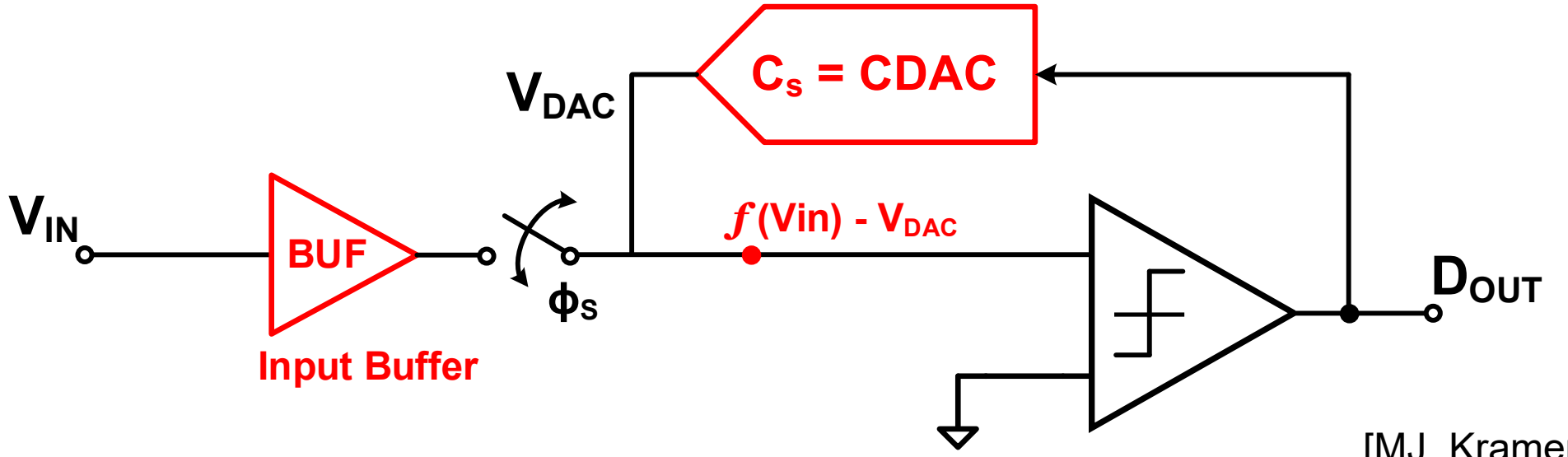


Outline

- Existing challenges of NS-SAR
- Proposed EF-CRFF structure for NS-SAR
- **Proposed noise-cancelling buffer for NS-SAR**
- Measurements results
- Conclusion

Prior Art: Conventional SAR

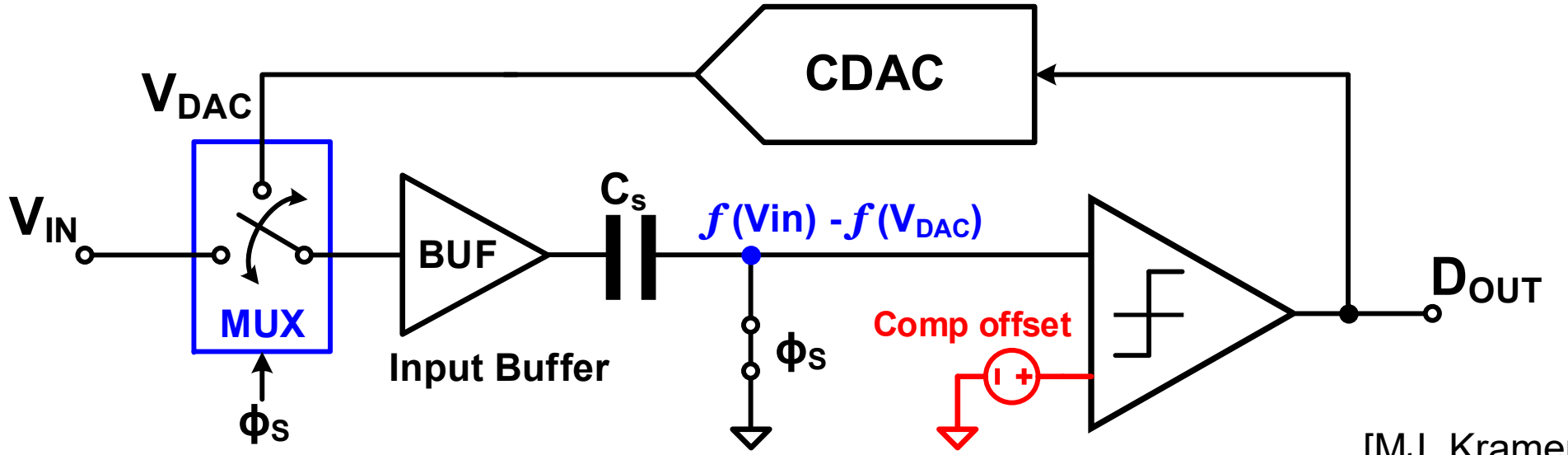
- **V_{IN} passed buffer while V_{DAC} does not**
  - V_{IN} is affected by buffer nonlinearity
- **Input buffer: linear → hard buffer design ☹**



[MJ. Kramer, *ISSCC* 2015]

Prior Art: Buffer-in-Loop (BIL) SAR

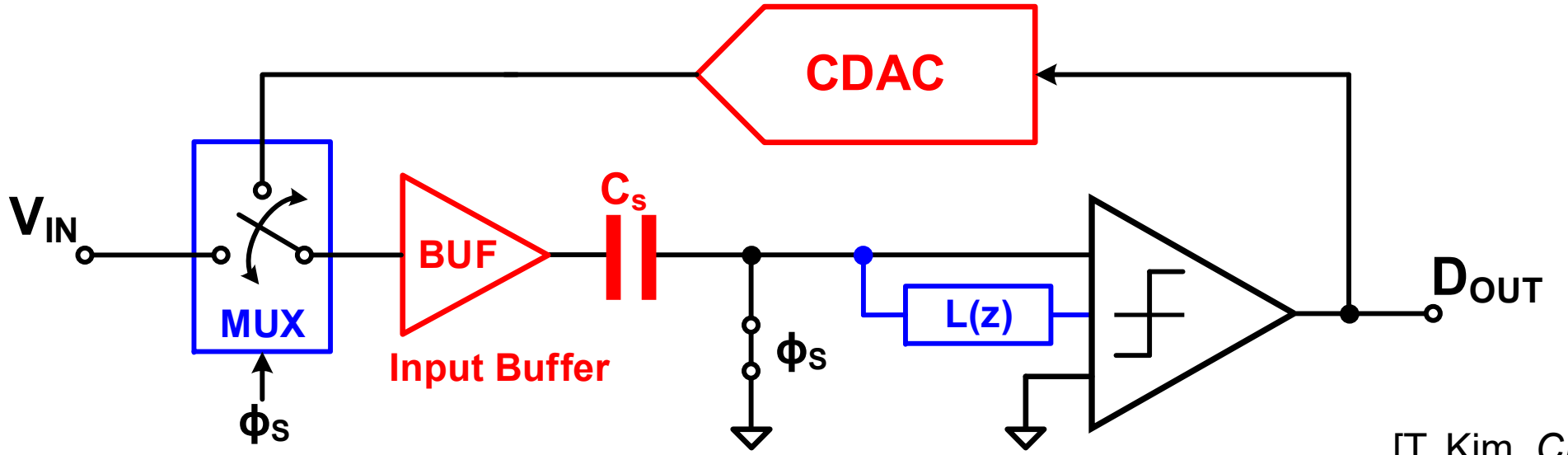
- Buffer embedded → linearity enhanced ☺
- Separated CDAC & Cs → devoid CDAC kT/C noise ☺
- Comparator offset → disturb linearity compensation ☹



[MJ. Kramer, *ISSCC* 2015]

Prior Art: Buffer-in-Loop (BIL) NS-SAR

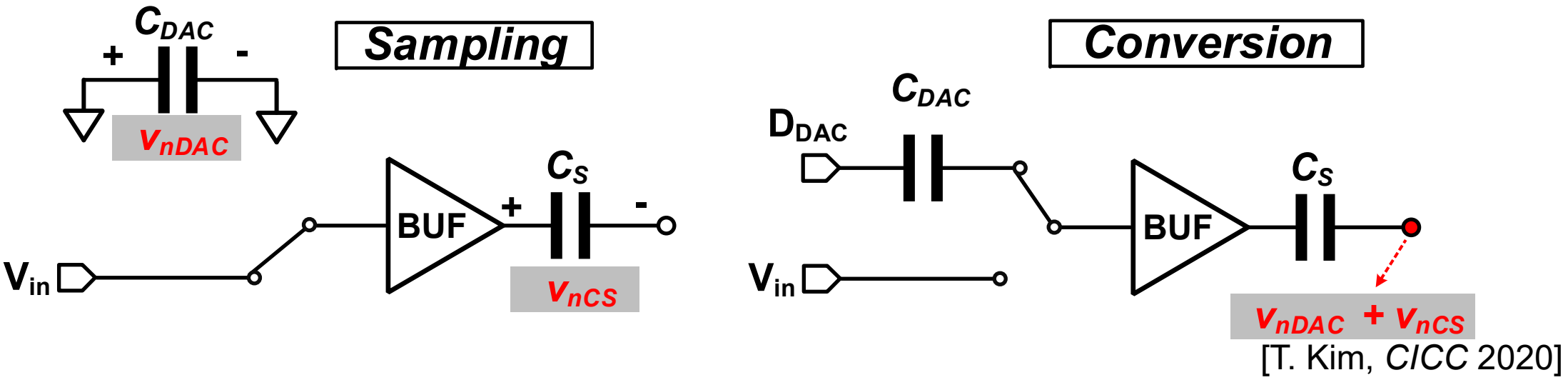
- Buffer embedded → linearity enhanced ☺
- Separated CDAC & Cs → devoid CDAC kT/C noise ☺
- Noise shaping included → devoid comp offset ☺



[T. Kim, *CICC* 2020]

Prior Art: Buffer-in-Loop (BIL) NS-SAR

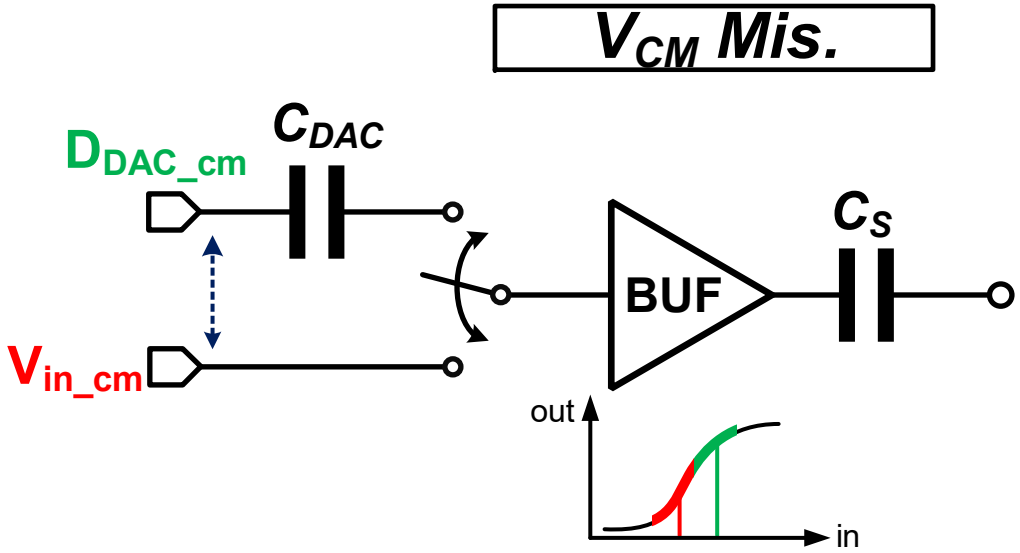
- Conversion phase: Cs sampling noise + CDAC reset noise ☹
- Residue extraction: additional buffer noise ☹
- V_{CM} mismatch: buffer nonlinearity leaks ☹

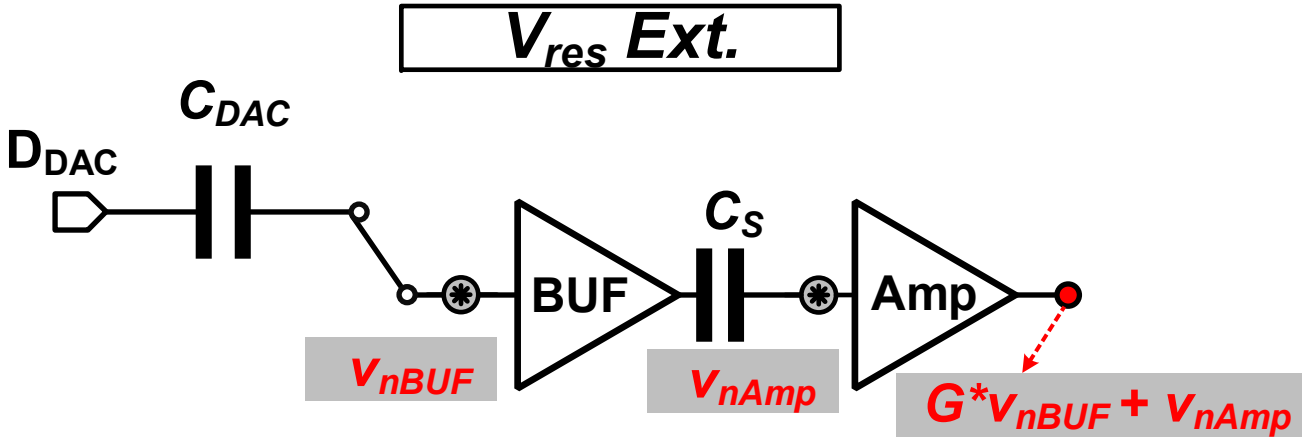


[T. Kim, *CICC* 2020]

Prior Art: Buffer-in-Loop (BIL) NS-SAR

- Conversion phase: Cs sampling noise + CDAC reset noise ☹
- Residue extraction: additional buffer noise ☹
- V_{CM} mismatch: buffer nonlinearity leaks ☹





[T. Kim, *CICC* 2020]

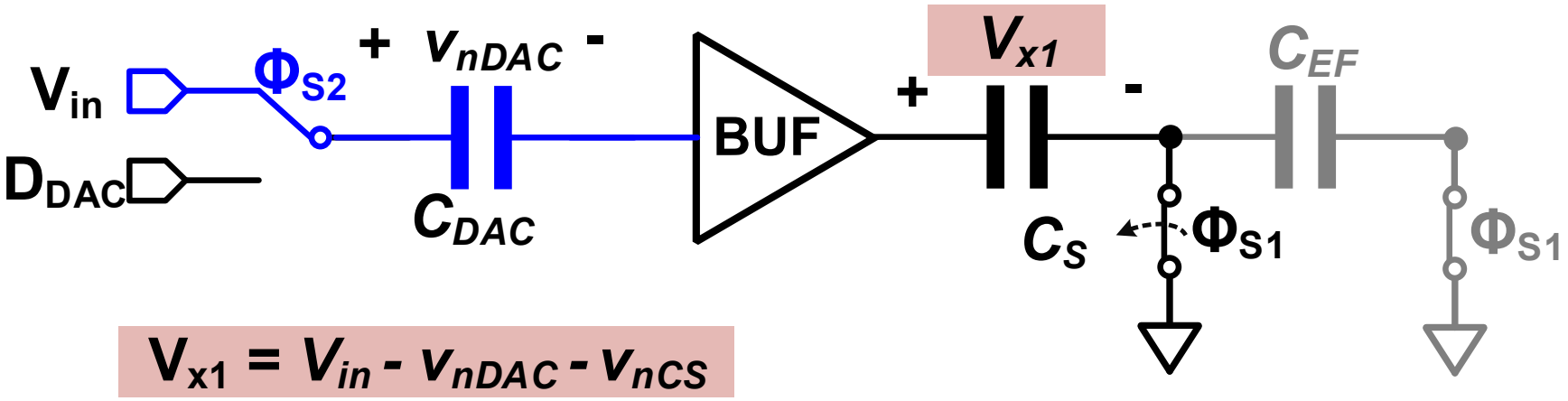
Prior Art: Buffer-in-Loop (BIL) NS-SAR

- Conversion phase: Cs sampling noise + CDAC reset noise ☹
- Residue extraction: additional buffer noise ☹
- V_{CM} mismatch: buffer nonlinearity leaks ☹
- *Can these issues be mitigated in BIL NSSAR? Yes*

Our solution:
Noise mitigated switching + PPSF + FIA

Proposed BIL with CDAC Noise Cancellation

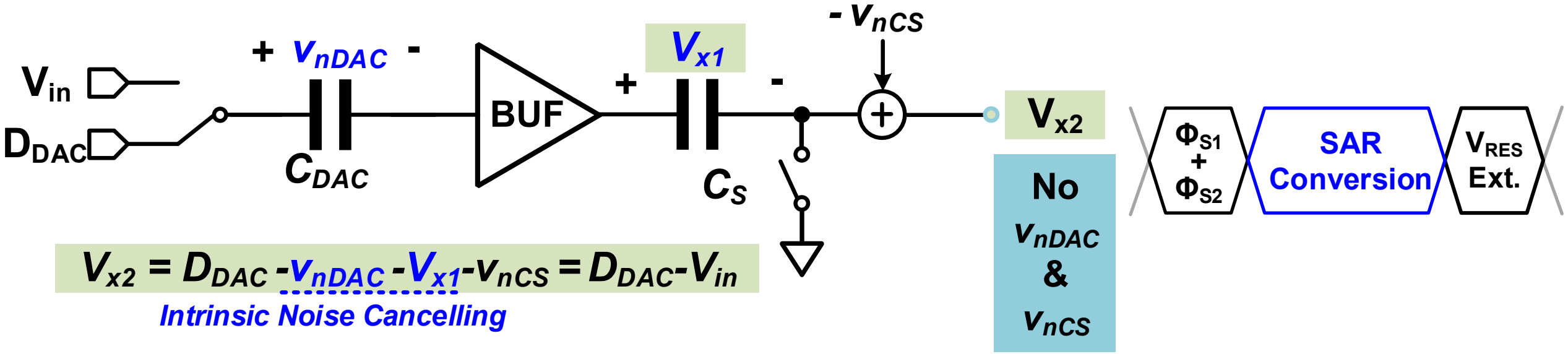
- Series noise cancellation after buffer
- At Φ_{S1} . → the $-V_{nDAC}$ is kept on Cs
- At Φ_{S2} . → the $-V_{nCs}$ is kept on Cs



$$V_{x1} = V_{in} - v_{nDAC} - v_{nCS}$$

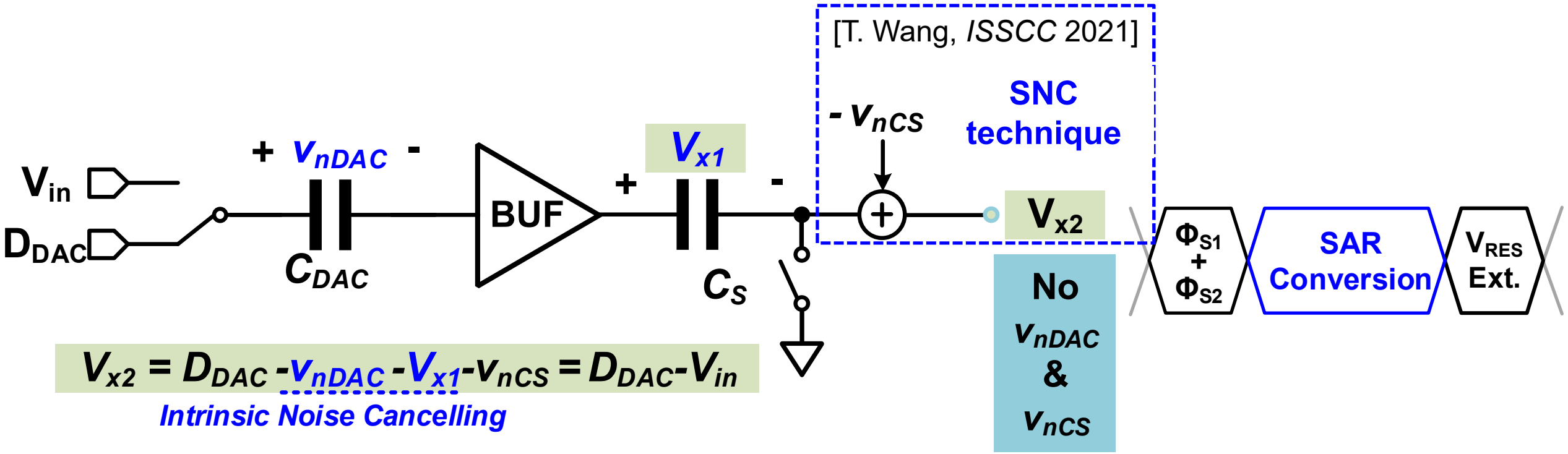
Proposed BIL with CDAC Noise Cancellation

- Series noise cancellation **after buffer**
- At conv. → V_{nDAC} transferred to Cs, V_{nDAC} **is cancelled**
- CDAC & Cs in series → V_{CM} mismatch ↓



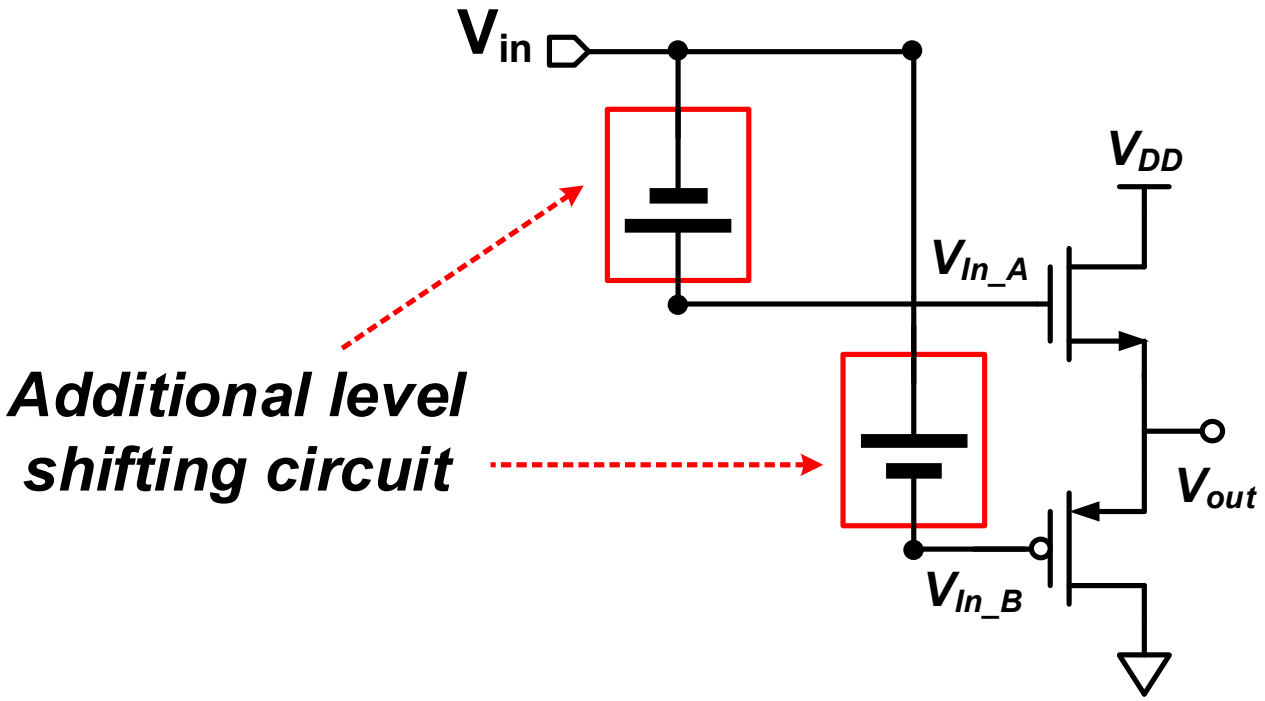
Proposed BIL with CDAC Noise Cancellation

- Series kT/C cancellation **after buffer**
- EF reused SNC is applied → V_{nCs} **is cancelled**
- Reduced kT/C noise → Cs size ↓ **& buffer relaxation**



Push-Pull Source Follower (PPSF)

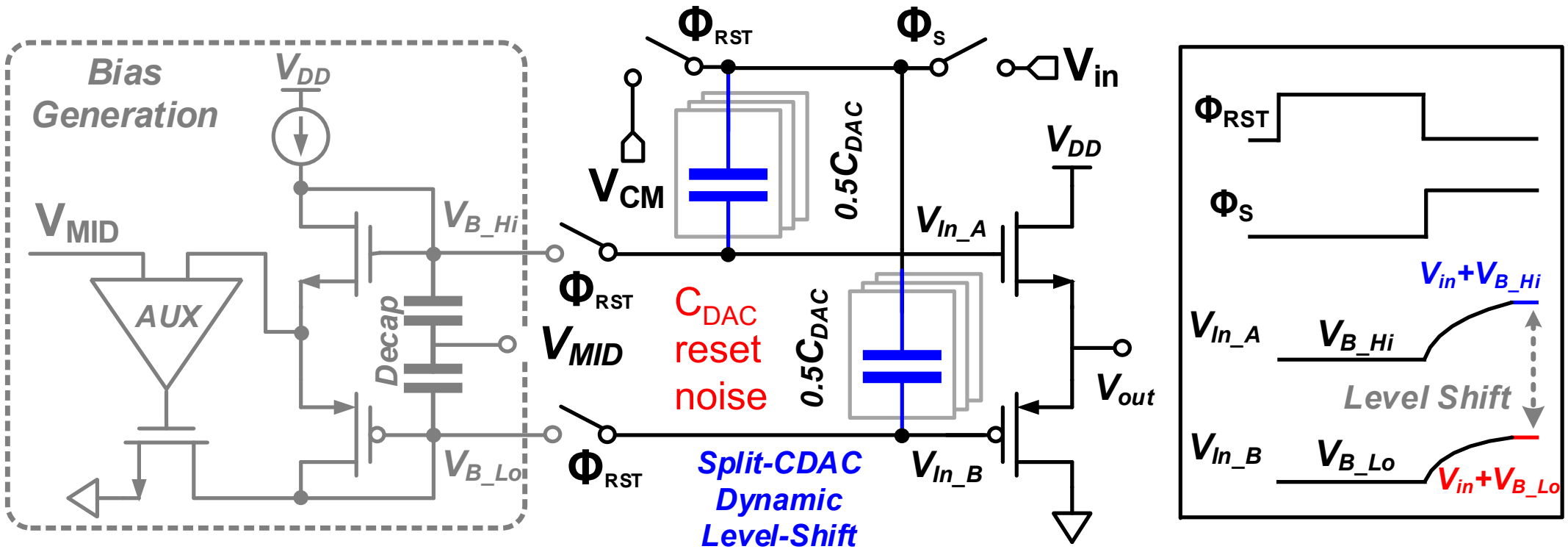
- PPSF → gm/id ↑→ lower noise ☺
- Excellent linearity → input V_{CM} mismatch sensitivity ↓
- Drawback: level shifting (LS) circuit ☹ → capacitive LS 😐



[MJ. Seo, *JSSC* 2020]

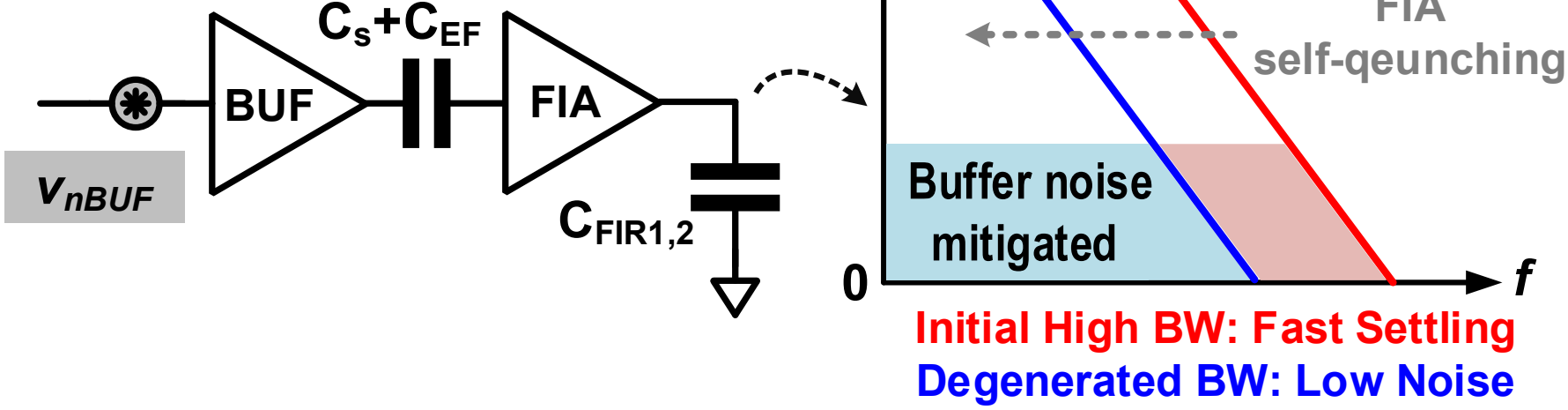
Push-Pull Source Follower (PPSF)

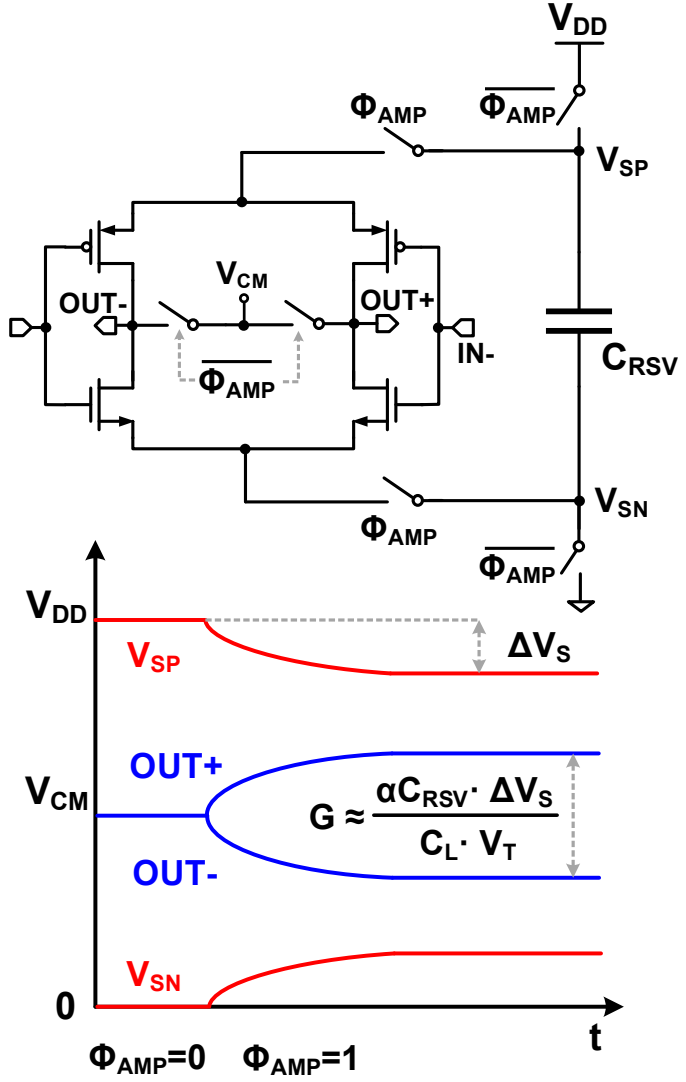
- Proposed PPSF → hardware reuse
- Area penalty free → split CDAC → complexity ↓ ☺
- Noise penalty free → noise cancellation assisted ☺



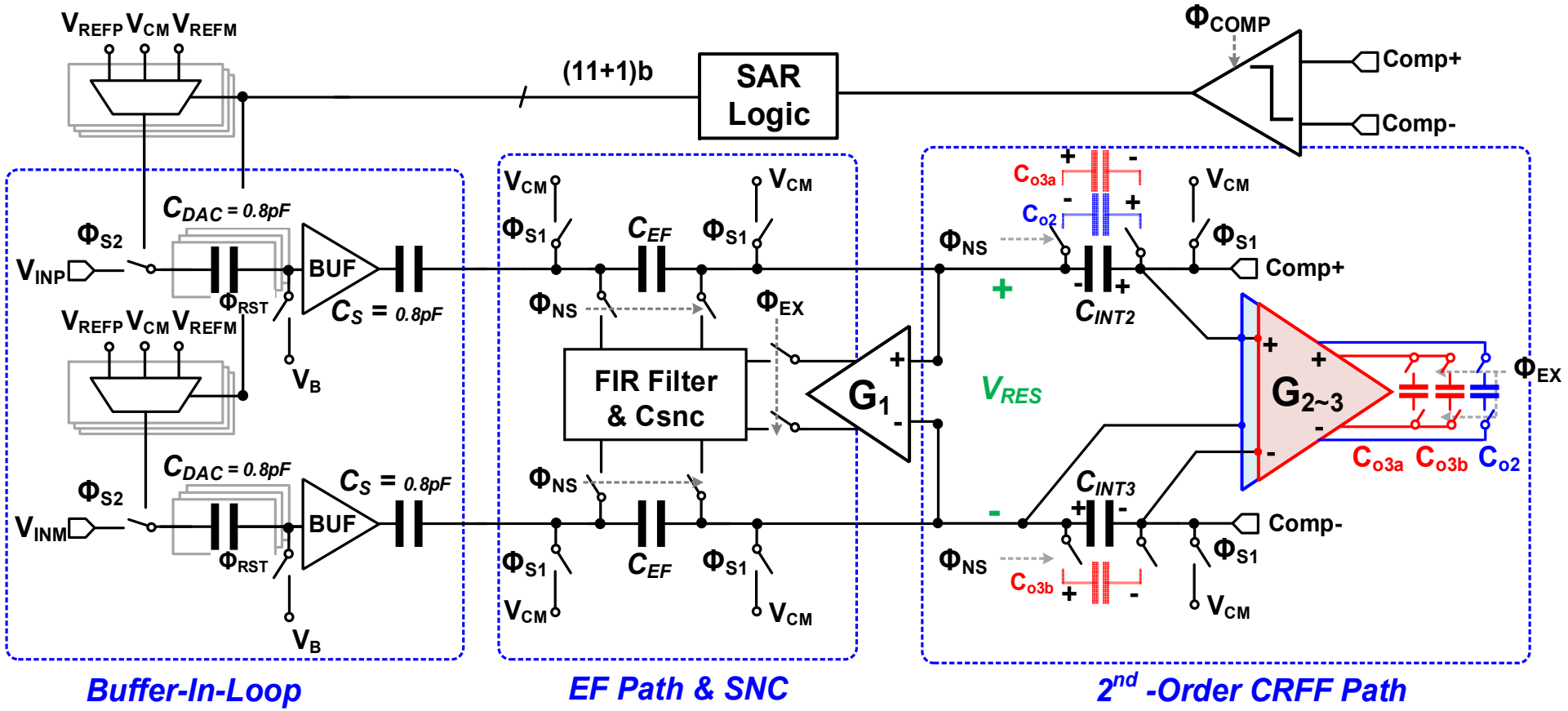
FIA Assisted Buffer Noise Reduction

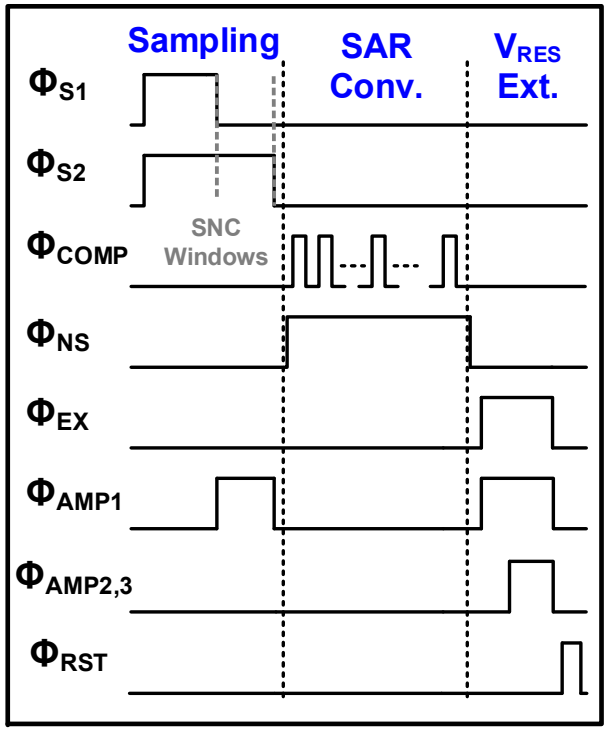
- Open loop floating inverter amplifier
- Self quenched→ amplification BW shrinks
- Inherently suppresses the PPSF noise ☺





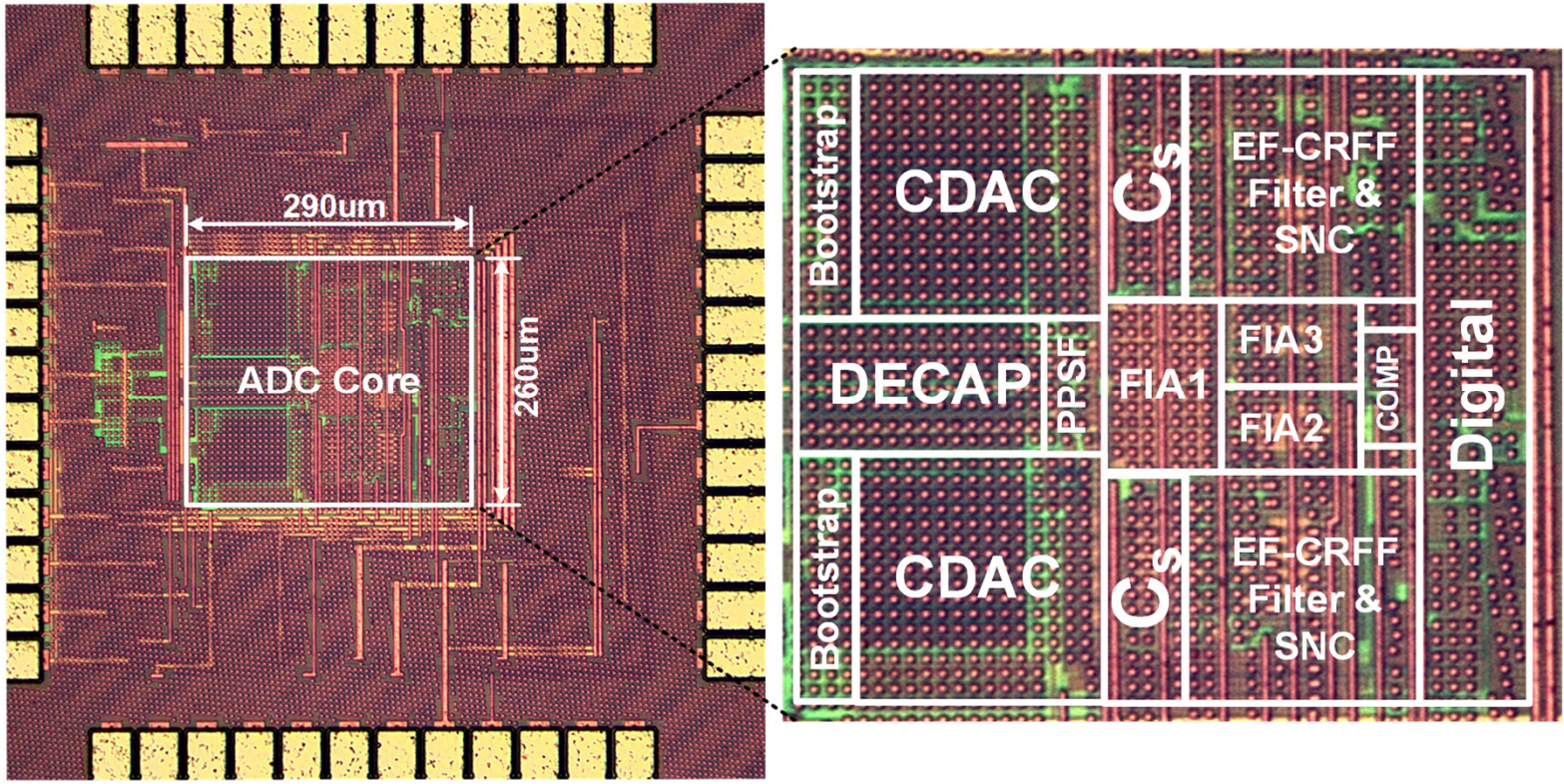
Overall Implementation





Chip Micrograph

- 65nm CMOS
- Total Area: 0.075mm^2
- Supply: 1.2V/2V
- Fs: 5 MHz
- OSR: 5
- BW: 500kHz

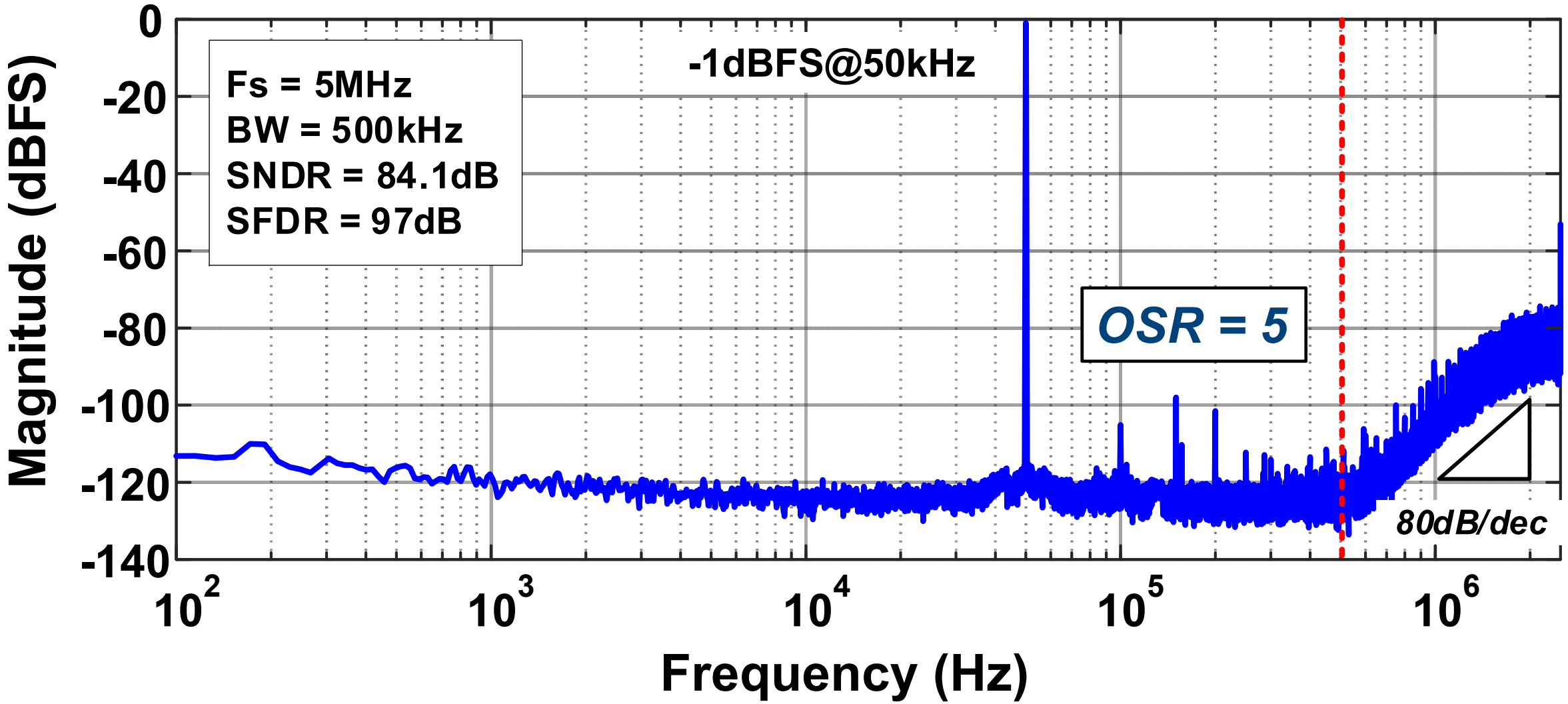


1. CDAC and Cs area can be limited
2. PPSF area overhead is very small

Outline

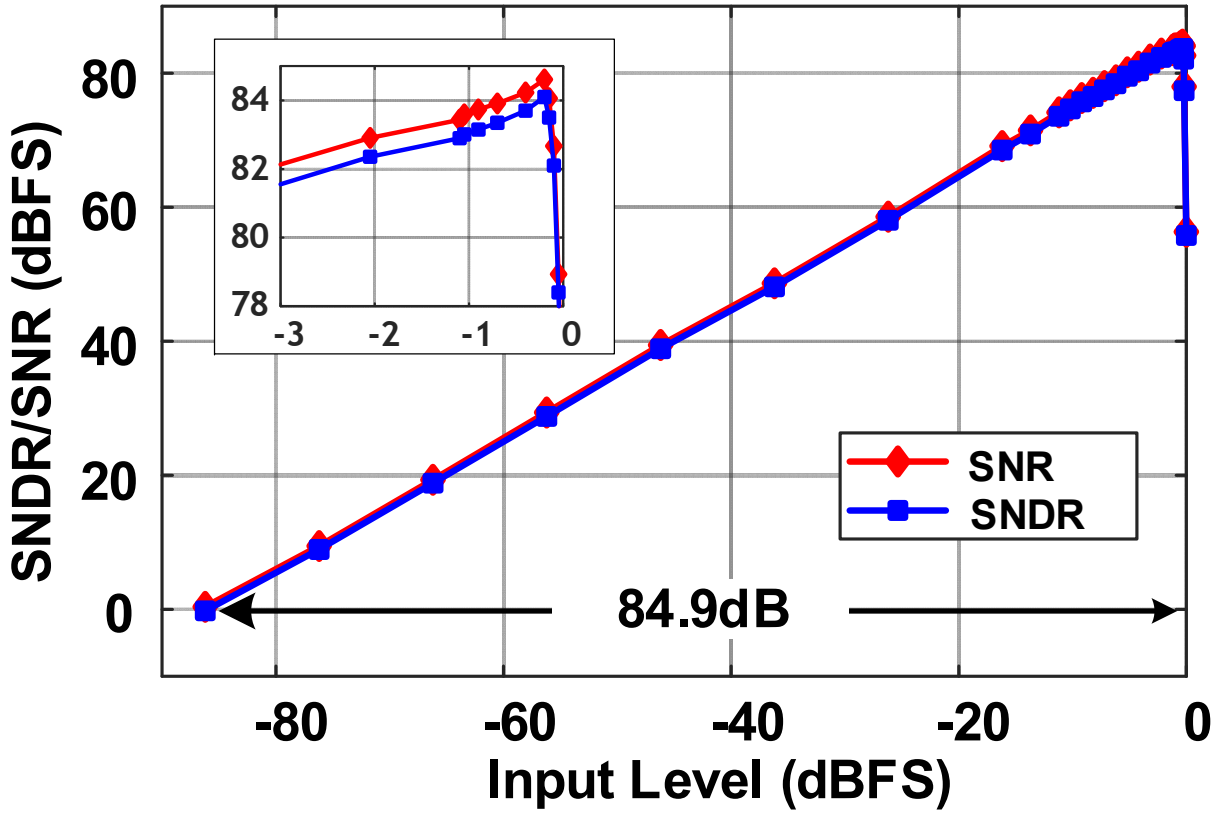
- Existing challenges of NS-SAR
- Proposed EF-CRFF structure for NS-SAR
- Proposed noise-cancelling buffer for NS-SAR
- **Measurements results**
- Conclusion

Measured Spectrum

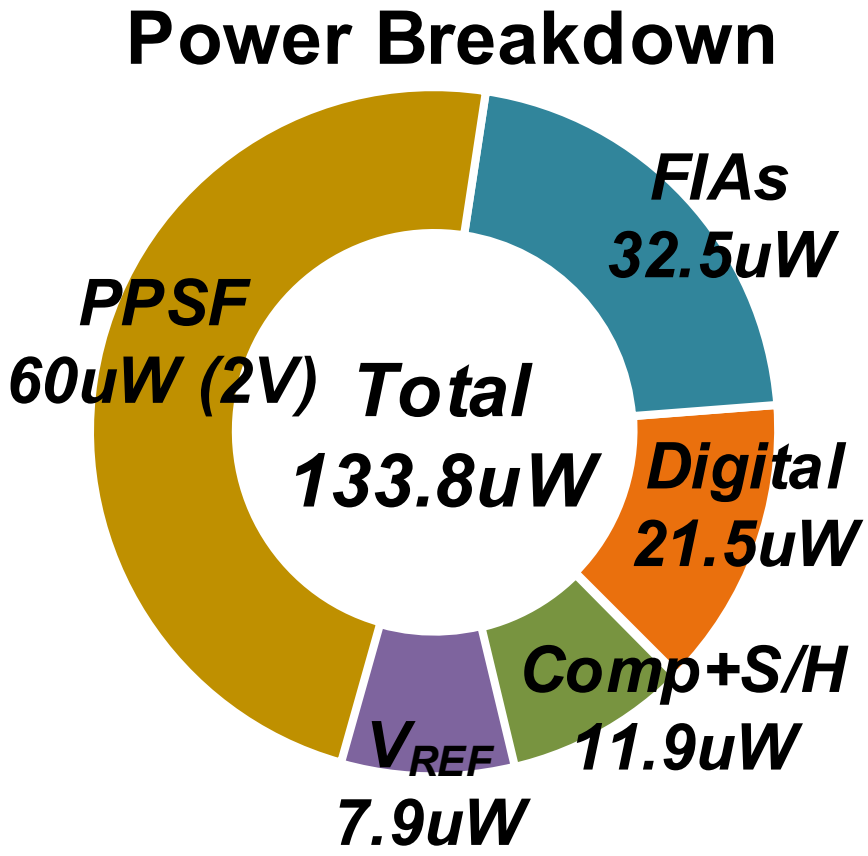


Measured DR & Power Breakdown

- **Measured DR:**
  - 84.9 dB

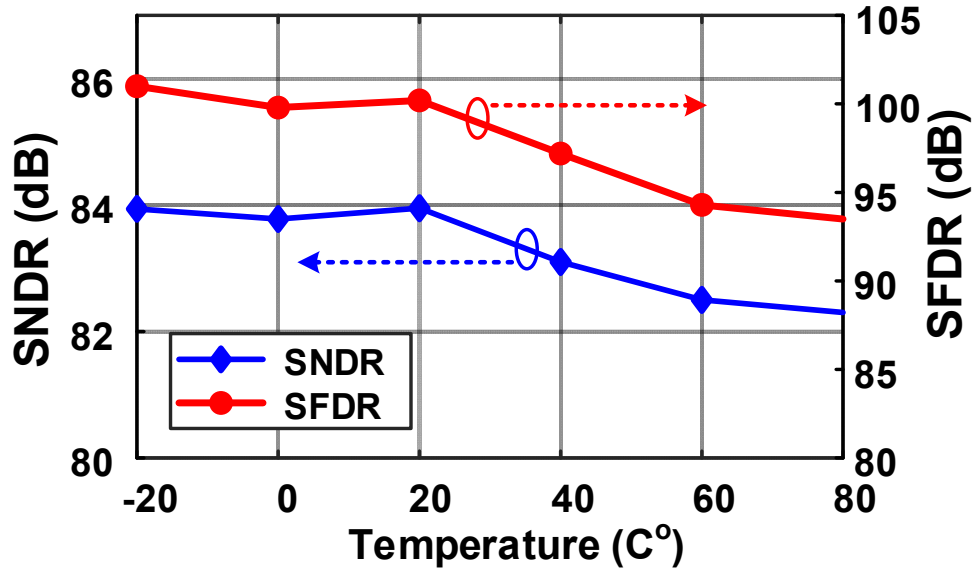


- **Power**
  - With Buffer: 133.8uW @ 5MS/s
  - Buffer power < 50%

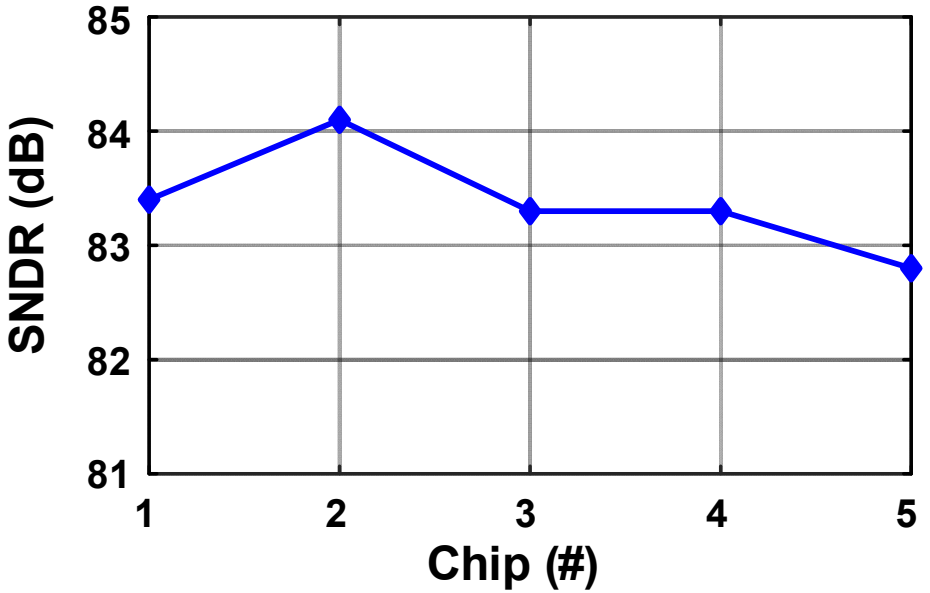


Measured Temp and Chip Variations

- **Temp: -20°C ~ 80°C**
  - SNDR within 1.5dB
  - SFDR within 6dB

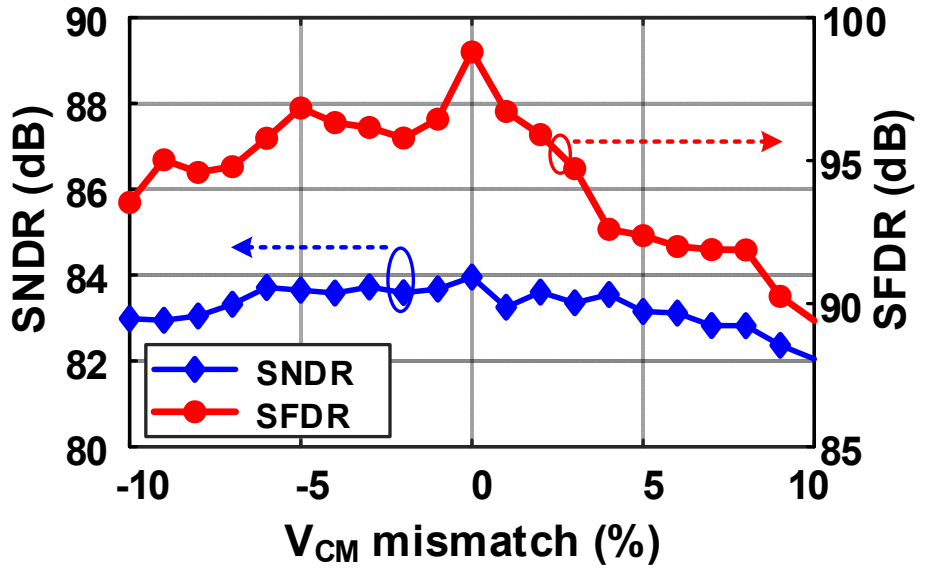


- **Measured 5 chips variation**
  - SNDR within 1dB

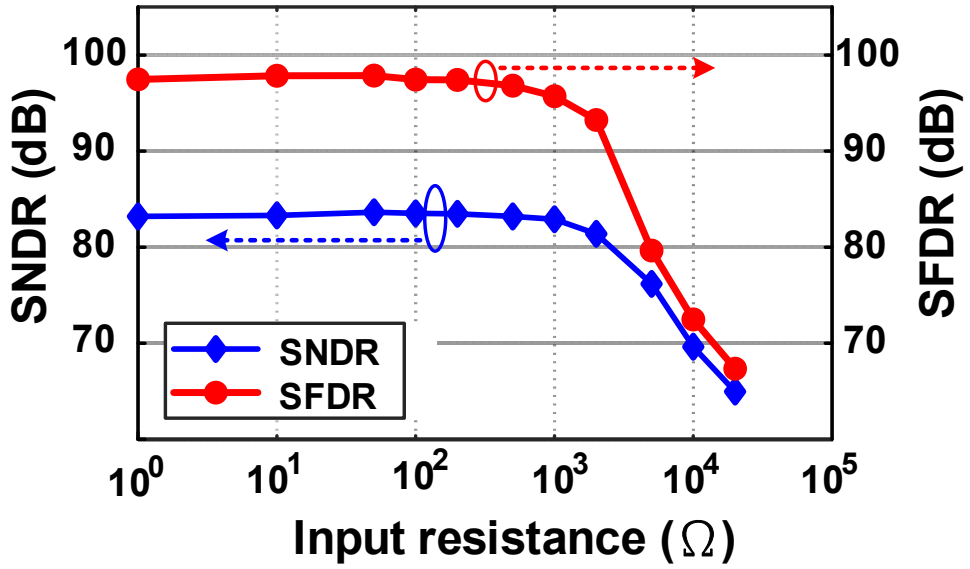


Measured V_{CM} mismatch and input resis. Variations

- **V_{CM} mismatch: -10% ~ 10%**
  - Varying input signal V_{CM}
  - SNDR above 82dB



- **Input Resistance: 1Ω ~ 25KΩ**
  - SNDR above 83dB at 1kΩ



Performance Summary

Specifications	ISSCC 20 Tang	ISSCC 20 Lu	ISSCC 21 Wang	ISSCC 21 Liu	CICC 19 Kim	This work	
						w/o BUF	W BUF
Process [nm]	40	28	65	40	65	**65**	
Architecture	CIFF	EF-EF	EF-CIFF	CIFF	CIFF	**EF-CRFF**	
NS Order	2	4	3	4	2	**4**	
Fully Dynamic NS	✓	✗	✓	✗	✓	✓	
kT/C Noise Suppressed	✗	✗	✓	✗	✗	✓	
Input Buffered	✗	✗	✗	✗	✓	✓	
Buffer Type	-	-	-	-	Source Follower	**PPSF**	
Supply [V]	0.8/1.1	1	1.1	1.1	0.9/2.1	**1.2/2**	

Performance Summary

Specifications	ISSCC 20 Tang	ISSCC 20 Lu	ISSCC 21 Wang	ISSCC 21 Liu	CICC 19 Kim	This work	
						w/o BUF	w BUF
C_{IN} Diff [pF]	4	15.36	0.8	32	0.8@/2.3##	**0.8@/0.8##**	
Power [uW]	107	120	119	340	870#	**73.8**	**133.8**
Fs [Ms/s]	10	2	10	5	80	**5**	
BW [kHz]	625	100	625	250	2000	**500**	
OSR	8	10	8	10	40	**5**	
SNDR [dB]	83.8	87.6	84.8	93.3	73.8	**84.1**	
FoMs1* [dB]	181.5	176.8	182.0	182.0	167.4#	**182.4**	**180.0**
FoMw [dB]**	6.8	30.8	6.6	18.1	54.3#	**5.6**	**10.0**

**FoMs1 = SNDR+1*log10(BW/Power) **FoMs2 = DR+1*log10(BW/Power) # With Buffer Power Included @Sampling Cap ##CDAC*

Conclusion

- **Low OSR barrier**
  - Higher order implementation and kT/C barrier and driver relaxation
- **Proposed EF-CRFF structure**
  - Achieve 4th order of noise shaping at low loss
  - Fully dynamic operation thus power efficient
- **Proposed noise cancellation buffer scheme**
  - Leverage series connection with CDAC, buffer and Cs.
  - Inherently cancels the CDAC reset noise
- **>13b ENOB (OSR =5) relaxing the input driving**

Thanks for your attention!