

ZHENGQI, GAO

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EDUCATION

Massachusetts Institute of Technology

Cambridge, USA

Ph.D. in Electrical Engineering and Computer Science

Sep 2021 – Jun 2026 (Expected)

- GPA: 5.00/5.00 (Rank: NA); worked with Prof. Duane S. Boning
- Research interests: design automation for photonic integrated circuits and machine learning

Fudan University

Shanghai, China

M.S. in Microelectronics and Solid State Electronics

Sep 2018 – Jun 2021

- GPA: 3.82/4.00 (Rank: NA); worked with Prof. Jun Tao and Prof. Xin Li (Duke Univ.)
- Research interests: electronic design automation (EDA), and machine learning

B.E. in Microelectronic Science and Engineering

Sep 2014 – Jun 2018

- GPA: 3.84/4.00 (Rank: 4/71); selected to Elite Engineering Program (top 5%)
- Relevant coursework: Mathematical Analysis, Probability, Mathematical Statistics and Stochastic Process, Signal and System, Data Structure and Algorithm Design, Design of Analog Integrated Circuits

PUBLICATIONS

1. Z. Xue*, **Z. Gao***, S. Ren*, and H. Zhao, “The Modality Focusing Hypothesis: On the Blink of Multimodal Knowledge Distillation,” *Arxiv Preprint*, 2022. [PDF] (* indicates equal contribution)
2. **Z. Gao**, Z. Zhang and D. S. Boning, “Automatic Design of a Broadband Directional Coupler via Bayesian Optimization,” *Conference on Lasers and Electro-Optics (CLEO)*, 2022.
3. **Z. Gao**, S. Ren, Z. Xue, and H. Zhao, “Training-Free Robust Multimodal Learning via Sample-Wise Jacobian Regularization,” *Arxiv Preprint*, 2022. [PDF]
4. S. Ren, H. Wang, **Z. Gao**, S. He, A. Yuille, Y. Zhou and C. Xie, “A Simple Data Mixing Prior for Improving Self-Supervised Learning,” *IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR)*, Jun. 2022. [PDF]
5. S. Ren, **Z. Gao**, T. Hua, Z. Xue, Y. Tian, S. He and H. Zhao, “Co-Advise: Cross Inductive Bias Distillation,” *IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR)*, Jun. 2022. [PDF]
6. Z. Xue, S. Ren, **Z. Gao** and H. Zhao, “Multimodal Knowledge Expansion,” *IEEE International Conference on Computer Vision (ICCV)*, Oct. 2021. [PDF]
7. **Z. Gao** and R. Rohrer, “Efficient Non-Monte-Carlo Yield Estimation,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*. [PDF]
8. **Z. Gao**, J. Tao, Y. Su, D. Zhou, X. Zeng and X. Li, “Fast Statistical Analysis of Rare Failure Events with Truncated Normal Distribution in High-Dimensional Variation Space,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*. [PDF]
9. **Z. Gao**, Z. Chen, J. Tao, Y. Sun, D. Zhou, and X. Zeng, “Bayesian Inference on Introduced General Region: An Efficient Parametric Yield Estimation Method for Integrated Circuits,” *ACM/IEEE Asia and South Pacific Design Automation Conference (ASPDAC)*, Jan. 2021. [PDF]
10. **Z. Gao**, J. Tao, D. Zhou, X. Zeng and X. Li, “Efficient Rare Failure Analysis over Multiple Corners via Correlated Bayesian Inference,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Oct. 2020. [PDF] [Code]
11. **Z. Gao**, J. Tao, D. Zhou and X. Zeng, “Efficient Parametric Yield Estimation over Multiple Process Corners via Bayesian Inference Based on Bernoulli Distribution,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Oct. 2020. [PDF] [Code]
12. J. Shi, **Z. Gao**, J. Tao, Y. Su, D. Zhou and X. Zeng, “Multi-Corner Parametric Yield Estimation via Bayesian Inference on Bernoulli Distribution with Conjugate Prior,” *IEEE International Symposium on Circuits and Systems (ISCAS)*, Oct. 2020. [PDF]
13. Y. Li, X. Zeng, **Z. Gao**, L. Lin, J. Tao, J. Han, X. Cheng, M. Tahoori and X. Zeng, “Exploring A Bayesian Optimization Framework Compatible with Digital Standard Flow for Soft-Error-Tolerant Circuit,” *IEEE/ACM*

- Design Automation Conference (DAC)*, Jul. 2020. [\[PDF\]](#)
14. **Z. Gao**, J. Tao, Y. Su, D. Zhou and X. Zeng, "Projection Based Active Gaussian Process Regression for Pareto Front Modeling," *Arxiv Preprint*. [\[PDF\]](#)
 15. **Z. Gao**, J. Tao, F. Yang, Y. Su, D. Zhou and X. Zeng, "Efficient Performance Trade-Off Modeling for Analog Circuit Based on Bayesian Neural Network," *IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, Nov. 2019. [\[PDF\]](#)
 16. J. Tao, **Z. Gao**, D. Zhou and X. Zeng, "Efficient Statistical Analysis for Correlated Rare Failure Events," *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Nov. 2018. [\[PDF\]](#)

RESEARCH EXPERIENCE

Massachusetts Institute of Technology	Cambridge, USA
<i>Research Assistant to Prof. Duane S. Boning</i>	Sep 2021 – Jun 2026 (expected)
<ul style="list-style-type: none"> Investigated neural network uncertainty quantification on regression problem Researched on automatic light processing functions synthesis on programmable photonics Optimized silicon photonic devices via Bayesian optimization 	
Shanghai Qizhi Institute	Shanghai, China
<i>Research Assistant to Prof. Hang Zhao</i>	Mar 2021 – Jun 2021
<ul style="list-style-type: none"> Exploited multimodal learning under knowledge distillation Developed a method to address adversarial attack by utilizing the multimodal data 	
Southern Methodist University	Remotely
<i>Research Assistant to Prof. Ron Rohrer</i>	May 2020 – Sep 2021
<ul style="list-style-type: none"> Built a power grid DC simulator for the electromigration problem Analyzed parametric yield based on the adjoint method 	
Fudan University (State Key Laboratory of ASIC & System)	Shanghai, China
<i>Research Assistant to Prof. Jun Tao (in collaboration with Prof. Xin Li)</i>	Sep 2016 – Jul 2021
<ul style="list-style-type: none"> Exploited a graph neural network for graph similarity tasks Improved post-silicon yield estimation with the domain adaptation technique Estimated multi-corner failure rate and yield with Bayesian inference Modeled performance trade-off of analog circuits based on a Bayesian neural network Optimized a time variant analog filter by hierarchical clustering (bachelor thesis) Developed an SRAM failure-rate estimation tool in collaboration with Prof. Xuan Zhang (WUSTL) [see here] 	

TEACHING AND INTERNSHIPS

Fudan University (FDU) and Duke Kunshan University (DKU)	China
<i>Teaching Assistant</i>	Sep 2019 – Mar 2020
<ul style="list-style-type: none"> Performed TA duties for Design of Analog Integrated Circuits at FDU (instructor: Prof. Jun Xu) and Introduction to Programming & Data Structure at DKU (instructor: Prof. Dennis Quan [Duke Univ.]) 	
Baidu Inc.	Shanghai, China
<i>Quality Assurance (QA) Engineering Intern</i>	Jun 2017 – Sep 2017
<ul style="list-style-type: none"> Measured the robustness of programs and took charge of the FEEDS project 	

SELECTED AWARDS AND HONORS

Outstanding Graduates of Shanghai (top 5%)	2021
National Scholarship, Fudan University (top 1%)	2020
Rising Star of Academic, Fudan University (awarded to 11 graduate students majoring in Sci. & Engi.)	2020
Pacemaker to Merit Student, Fudan University (awarded to 15 graduate students)	2019
First Prize Scholarship, Fudan University (top 5%)	2019
National Gold Award, China "Internet+" College Student Innovation & Entrepreneur Competition (top 5%)	2018
National 2 nd Prize, China Post-Graduate Mathematical Contest in Modeling (top 15%)	2018
Outstanding Undergraduates of Shanghai (top 5%)	2018
Meritorious Winner, American Mathematical Contest in Modeling (top 13%)	2017
Top 11%, 2017 IEEE Xtreme Global Programming Competition (out of 3,350 teams worldwide)	2017
First Prize Scholarship, Fudan University (top 5%)	2015, 2016, 2017

- National 2nd prize, China Mathematical Contest in Modeling (top 15%)

2016

REPRESENTATIVE PROJECTS

PRML Solution Manual (GitHub 700+ Stars)

Shanghai, China

An Original Solution Manual for Pattern Recognition and Machine Learning (PRML)

Sep 2017 – Present

- Solved nearly all exercises in *PRML* [[see here](#)]
- Communicated with people globally via email, helping them solve problems relevant to *PRML*

Auto-Grading System

Kunshan, China

An Auto-Grading System Developed at DKU

Jan 2020 – Mar 2020

- Led a small TA group to peruse the source code of Submittity
- Developed a fully automatic grading system based on Submittity

“Dr. Stanley’s House” (Puzzle Video Game) Written in Haskell

Shanghai, China

Final Project for Introduction to Functional Programming: From C/C++ to Haskell

Sep 2018 – Jan 2019

- Implemented the game with a complete plot via Haskell [[see here](#)]
- Organized the program structure, sorted the logic, and set the schedule as the team leader
- Exploited Haskell libraries (e.g., SDL2, SDL2-ttf, and SDL2-mixer) to add music and animation

ADDITIONAL INFORMATION

Computer and Language Skills

- **Programming languages & Software:** C/C++, MATLAB, Python, Linux, Java, Haskell, HSPICE, SPECTRE
- **Languages:** Mandarin Chinese (native), English (proficient)

PROFESSIONAL SERVICES

- **Independent reviewer:** ICCAD, IEEE TCAD, etc.,