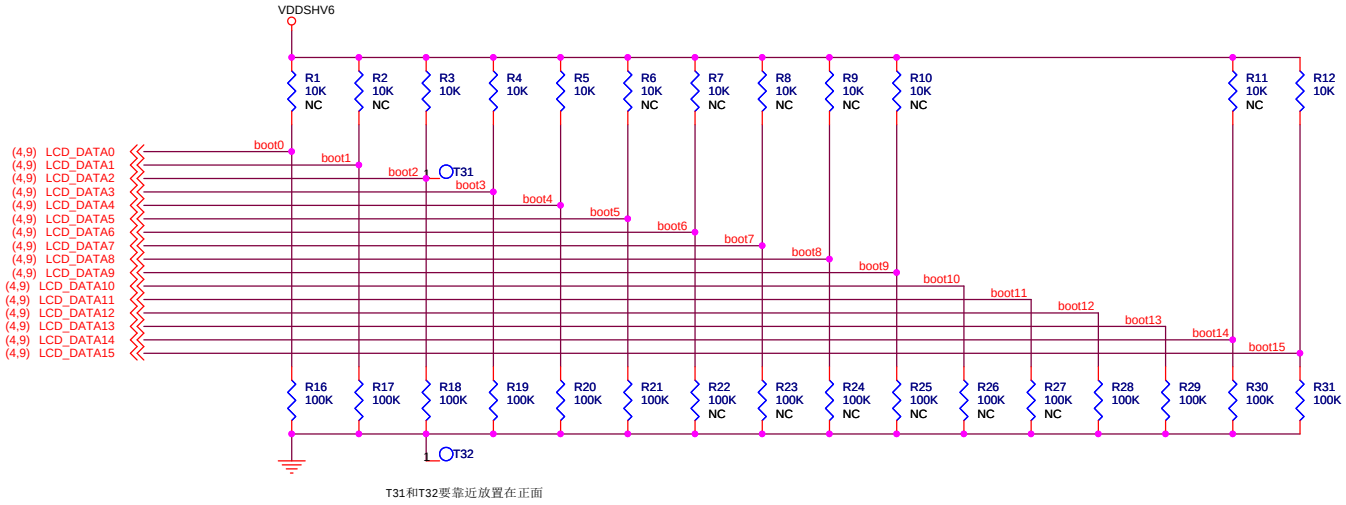
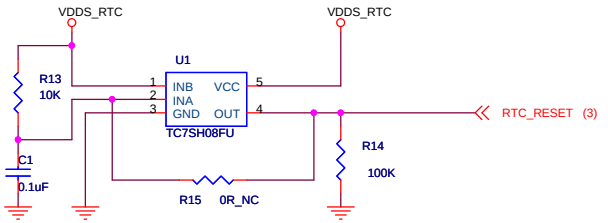
BOOT[0...15]: 0011 10XX XXXX 0001b
BOOT[4...0]: 11100b boot seq:MMC1->MMC0->UART0->USB0
BOOT[5]: 0b CLKOUT1=disable
BOOT[15,14]: 10b 25MHz

BOOT

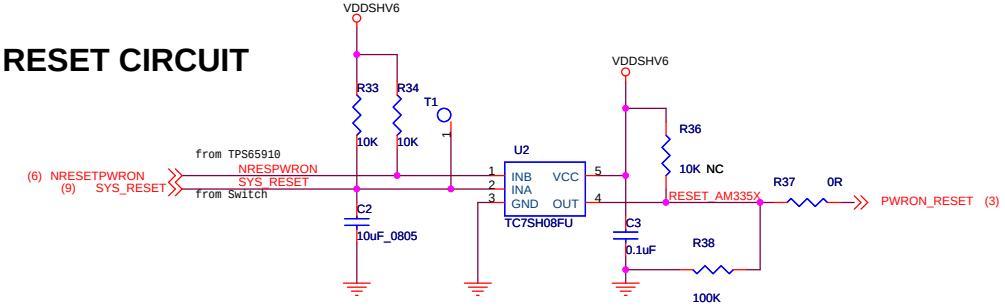


T31和T32要靠近放置在正面

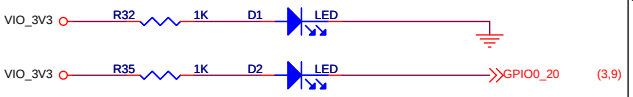
RTC RESET



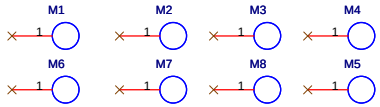
HW RESET CIRCUIT



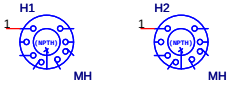
Power LED



HOLE & MARK

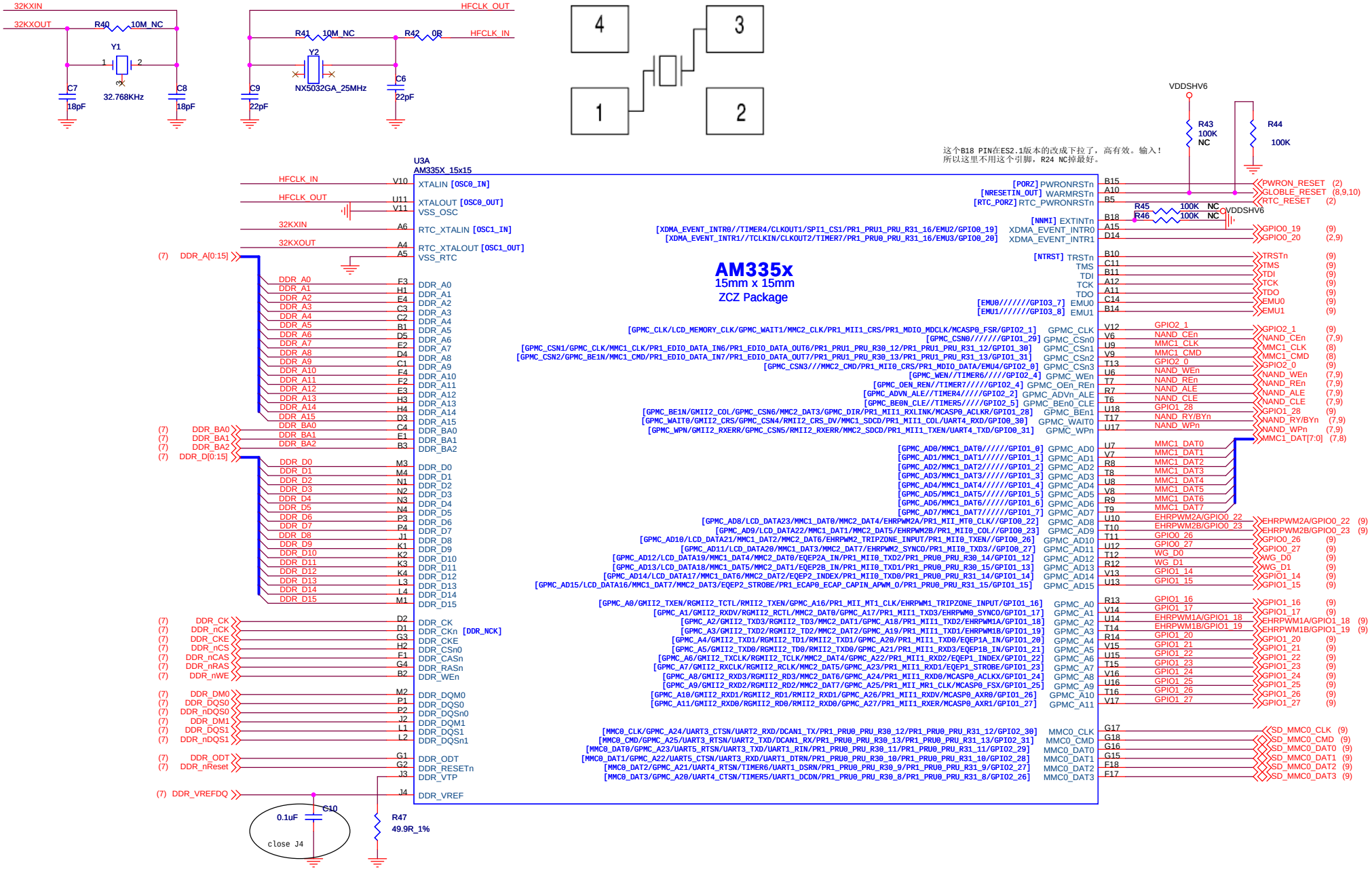


底板对核心板输入VBAT和VIO_3V3



这两个孔是内径2.7mm，外径6.5mm；

Design	<design>	CM335n	
Review	<review>	Title BOOT/RTC/RESET	
Authorize	<authorize>	Size A3	Doc Name CM335X 141101 / Ver. V1.0
Standardize	<standardize>	Date Monday, November 17, 2014	Sheet 2 of 10



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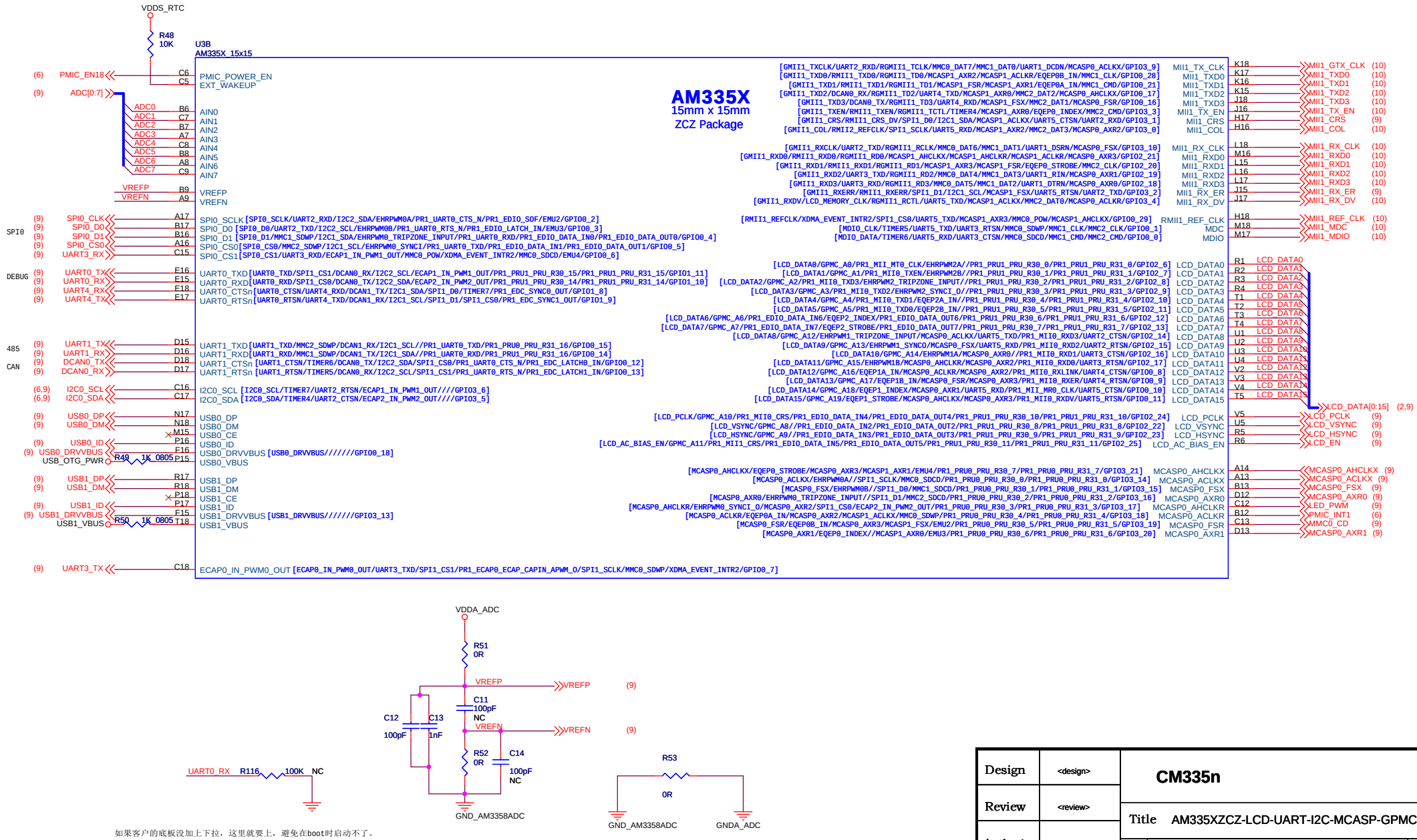
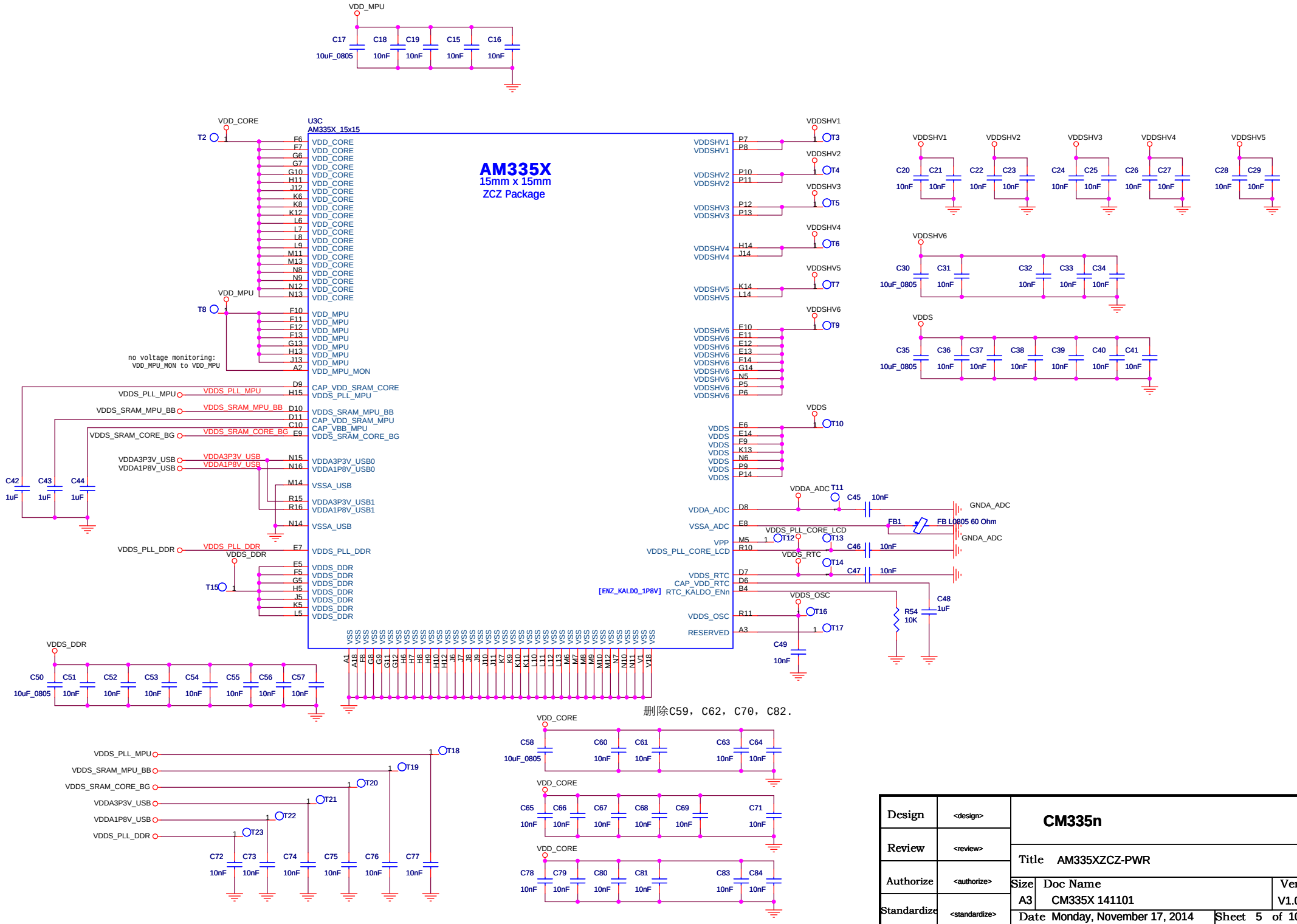
Review	<review>	Title AM335XZCZ-DDR-NAND-IF	
Authorize	<authorize>	Size A3	Doc Name CM335X 141101 Ver. V1.0
Standardize	<standardize>	Date Monday, November 17, 2014	Sheet 3 of 10



Design	<design>	CM335n	
Review	<review>	Title	AM335XZCZ-LCD-UART-I2C-MCASP-GPMC
Authorize	<authorize>	Size: A3	Doc Name: CM335X 141101 — Ver.: V1.0
Standardize	<standardize>	Date: Monday, November 17, 2014	Sheet 4 of 10



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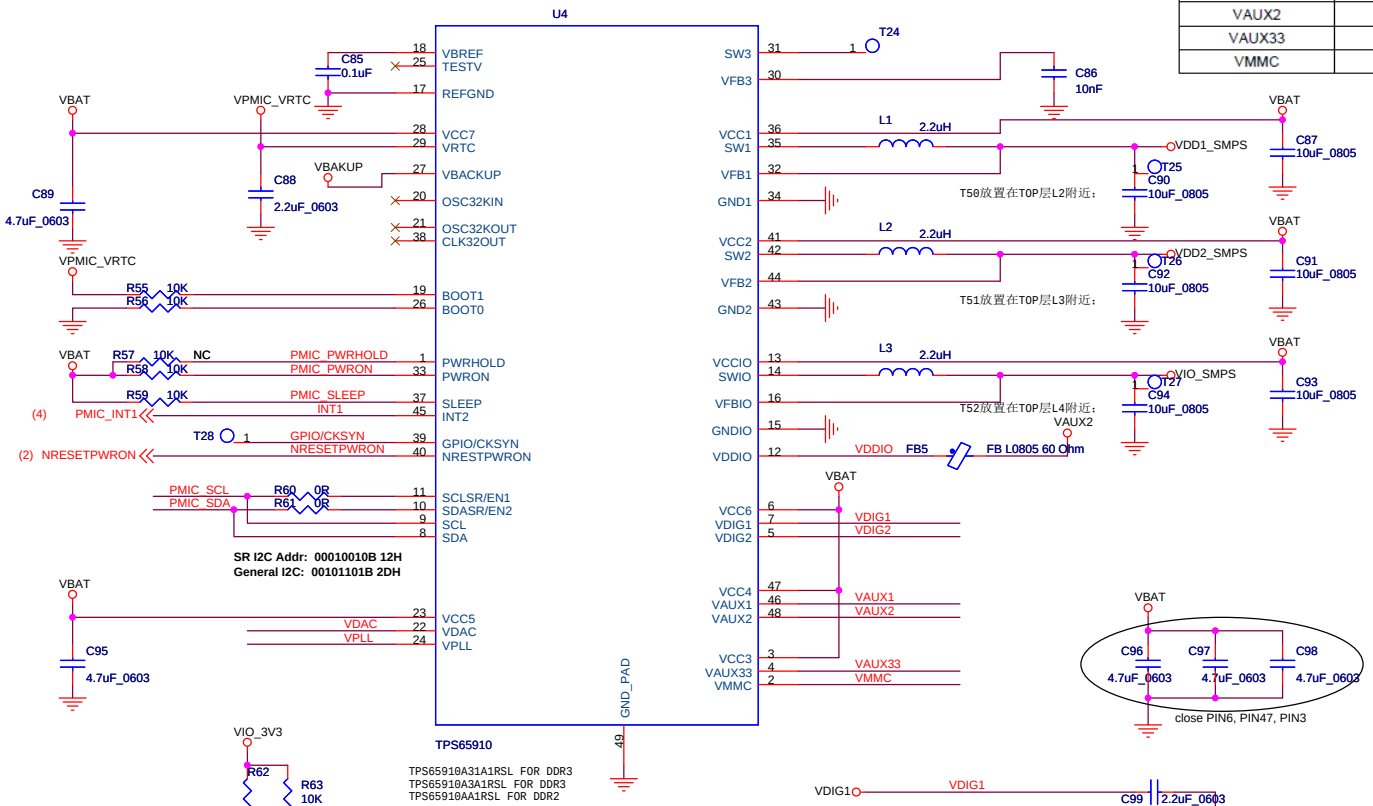
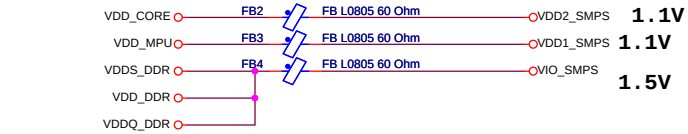
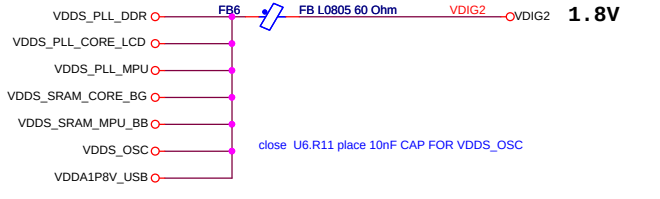
Authorize	<authorize>	Size A3	Doc Name CM335X 141101 Ver. V1.0
Standardize	<standardize>	Date Monday, November 17, 2014	Sheet 5 of 10

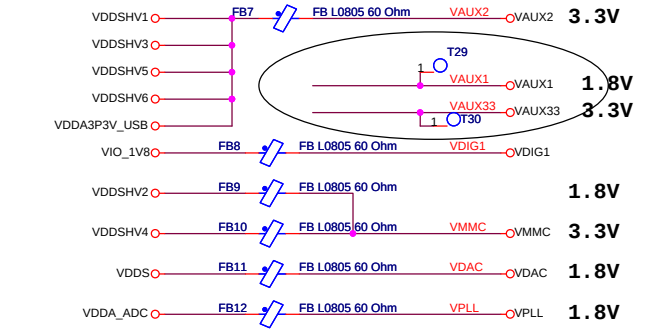
RESOURCE	TYPE	VOLTAGES	POWER
VIO	SMPS	1.5 V / 1.8 V / 2.5 V / 3.3 V	1000 mA
VDD1	SMPS	0.6 ... 1.5 in 12.5-mV steps Programmable multiplication factor: x2, x3	1500 mA
VDD2	SMPS	0.6 ... 1.5 in 12.5-mV steps Programmable multiplication factor: x2, x3	1500 mA
VDD3	SMPS	5 V	100 mA
VDIG1	LDO	1.2 V, 1.5 V, 1.8 V, 2.7 V	300 mA
VDIG2	LDO	1 V, 1.1 V, 1.2 V, 1.8 V	300 mA
VPLL	LDO	1.0 V, 1.1 V, 1.8 V, 2.5 V	50 mA
VDAC	LDO	1.8 V, 2.6 V, 2.8 V, 2.85 V	150 mA
VAUX1	LDO	1.8 V, 2.5 V, 2.8 V, 2.85 V	300 mA
VAUX2	LDO	1.8 V, 2.8 V, 2.9 V, 3.3 V	150 mA
VAUX33	LDO	1.8 V, 2.0 V, 2.8 V, 3.3 V	150 mA
VMMC	LDO	1.8 V, 2.8 V, 3.0 V, 3.3 V	300 mA

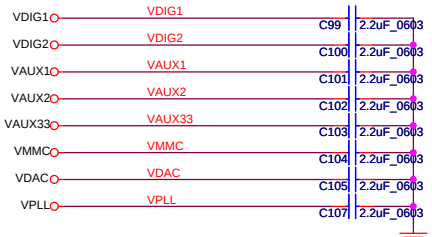


WARNNING:
PLS FIRST SETTING VIO_SMPS to 1.5V FOR DDR POWER.

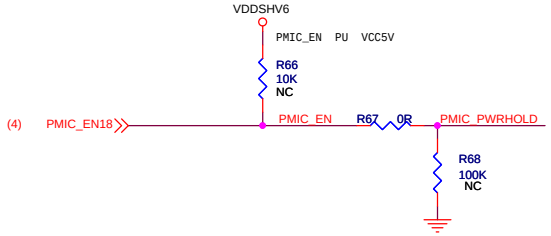




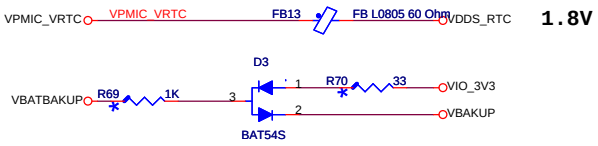




VIO18 change

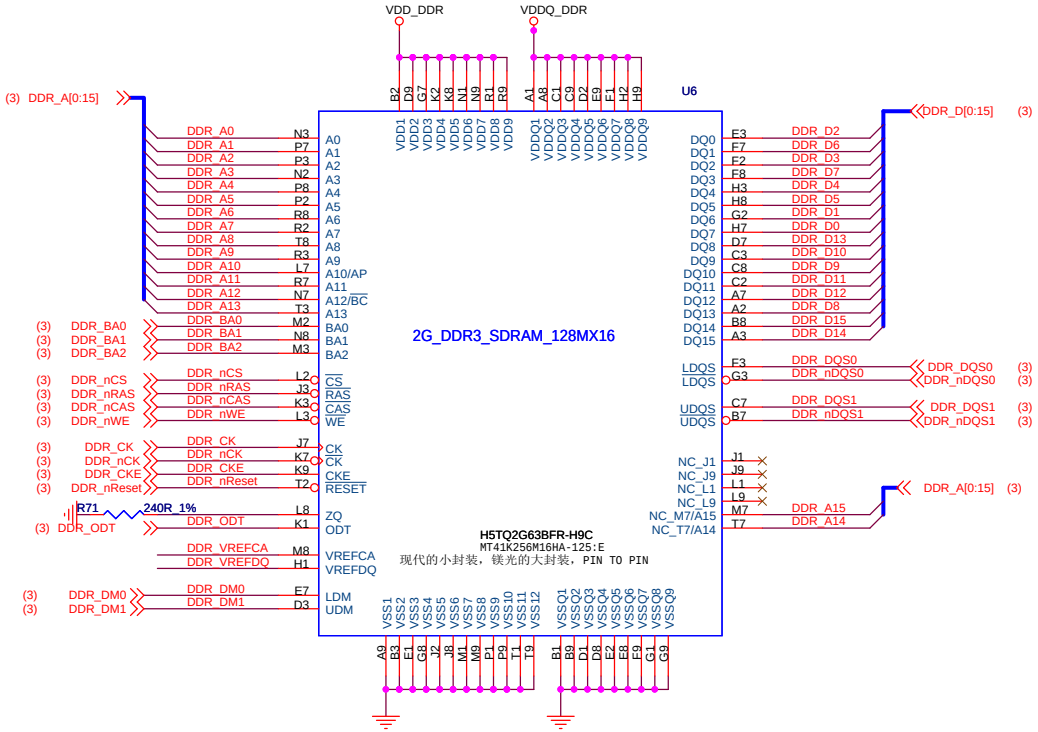


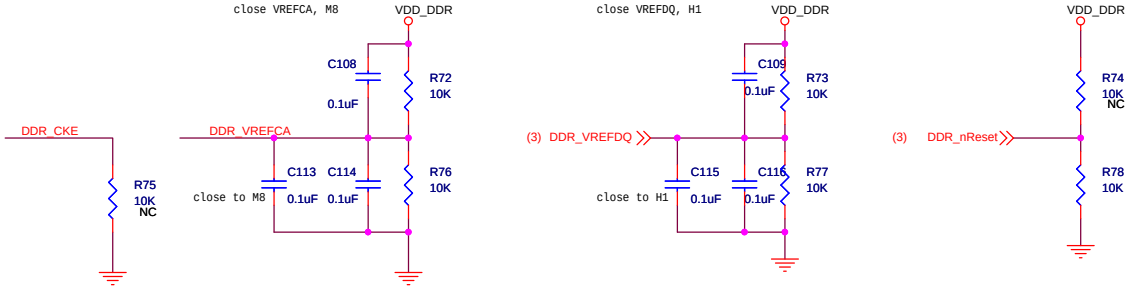
这里是个错误设计，是靠2G07的漏电流过去打开PMIC_PWRHOLD。
解法一：去掉U5，R66，R67，焊接R68，R57，100K；
解法二：去掉U5，R66，U5的3，4脚连接起来；

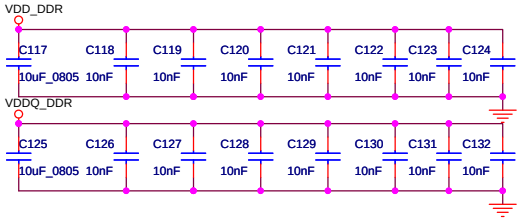


Design	<design>	CM335n	
Review	<review>	Title PMIC/RTC	
Authorize	<authorize>	Size A3	Doc Name CM335X 141101 Ver. V1.0
Standardize	<standardize>	Date Monday, November 17, 2014	Sheet 6 of 10

DDR3

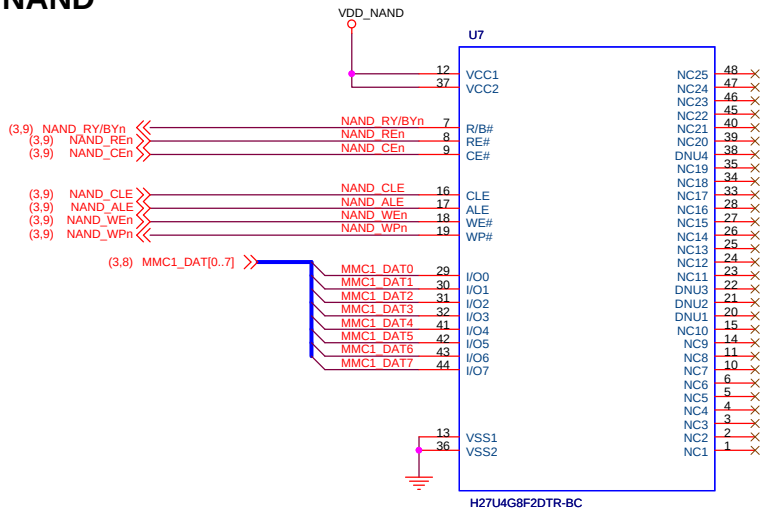






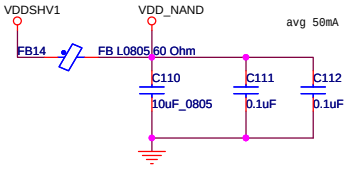
if space careless, serial resisters recommended(22R) on data[0..7]

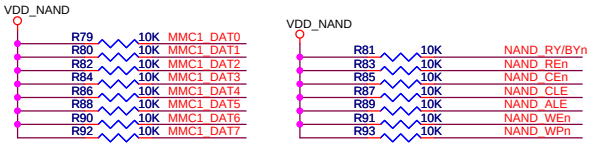
NAND



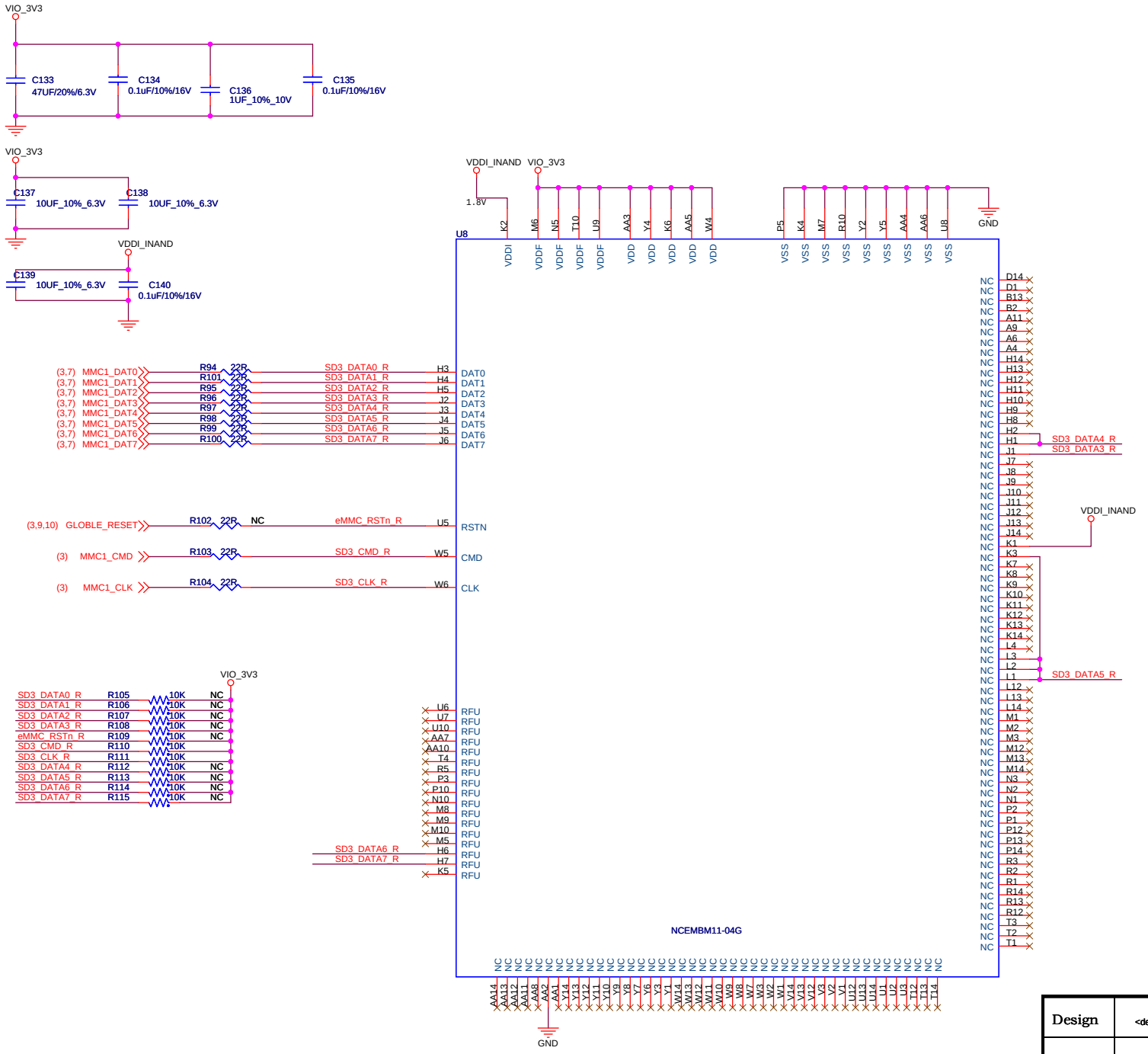
查查是否和三星的K9F1G08U0D是否PIN TO PIN；是否有4G08 SLC的？

与EMMC是双layout的，二者取其一。





Design	<design>	CM335n	
Review	<review>	Title DDR3/NAND	
Authorize	<authorize>	Size A3	Doc Name CM335X 141101 Ver. V1.0
Standardize	<standardize>	Date Monday, November 17, 2014	Sheet 7 of 10



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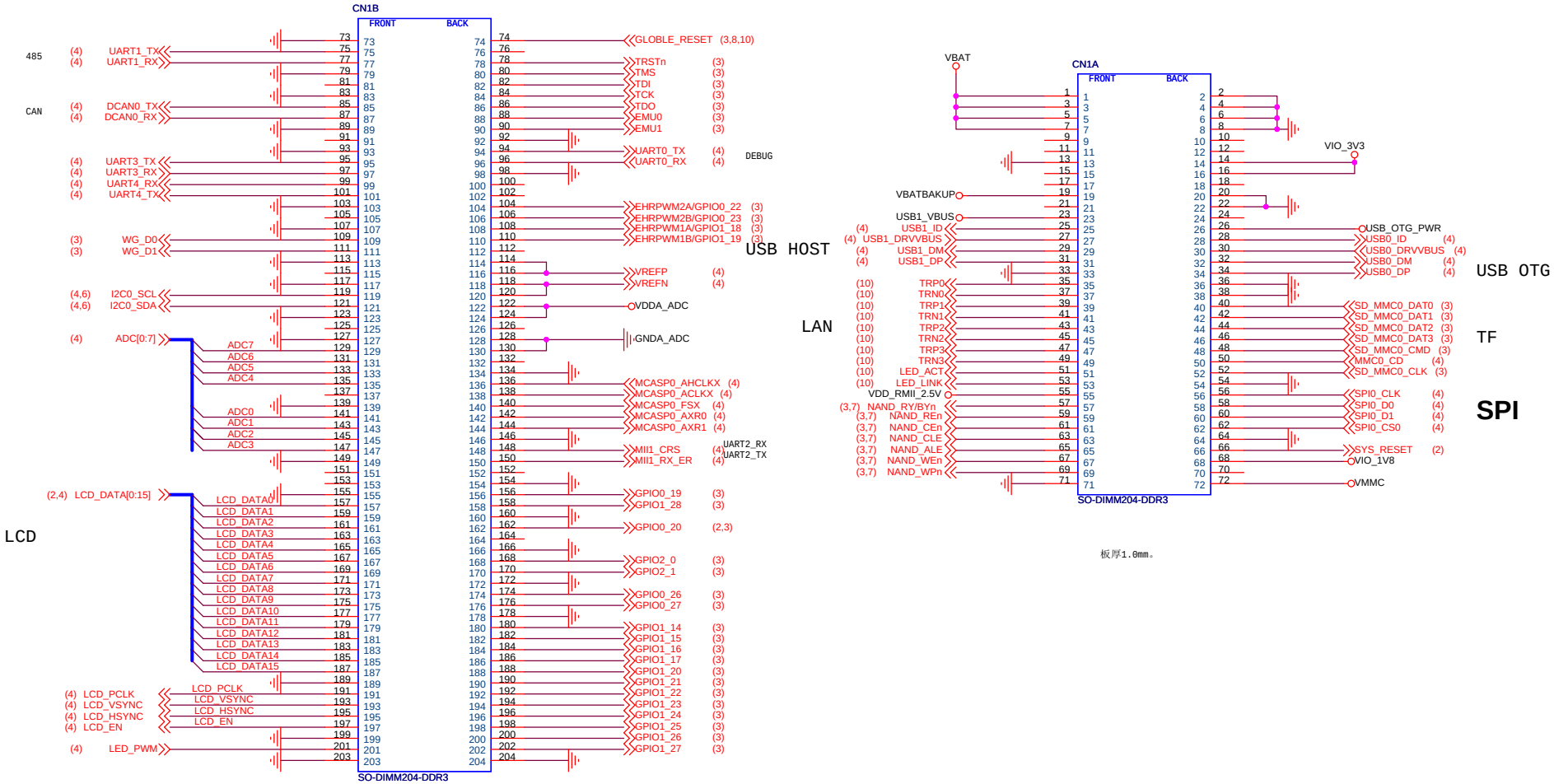
Review	<review>	Title eMMC	
Authorize	<authorize>	Size A3	Doc Name CM335X 141101 / Ver. V1.0
Standardize	<standardize>	Date Monday, November 17, 2014	Sheet 8 of 10



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Review	<review>	Title GOLD FIGERS	
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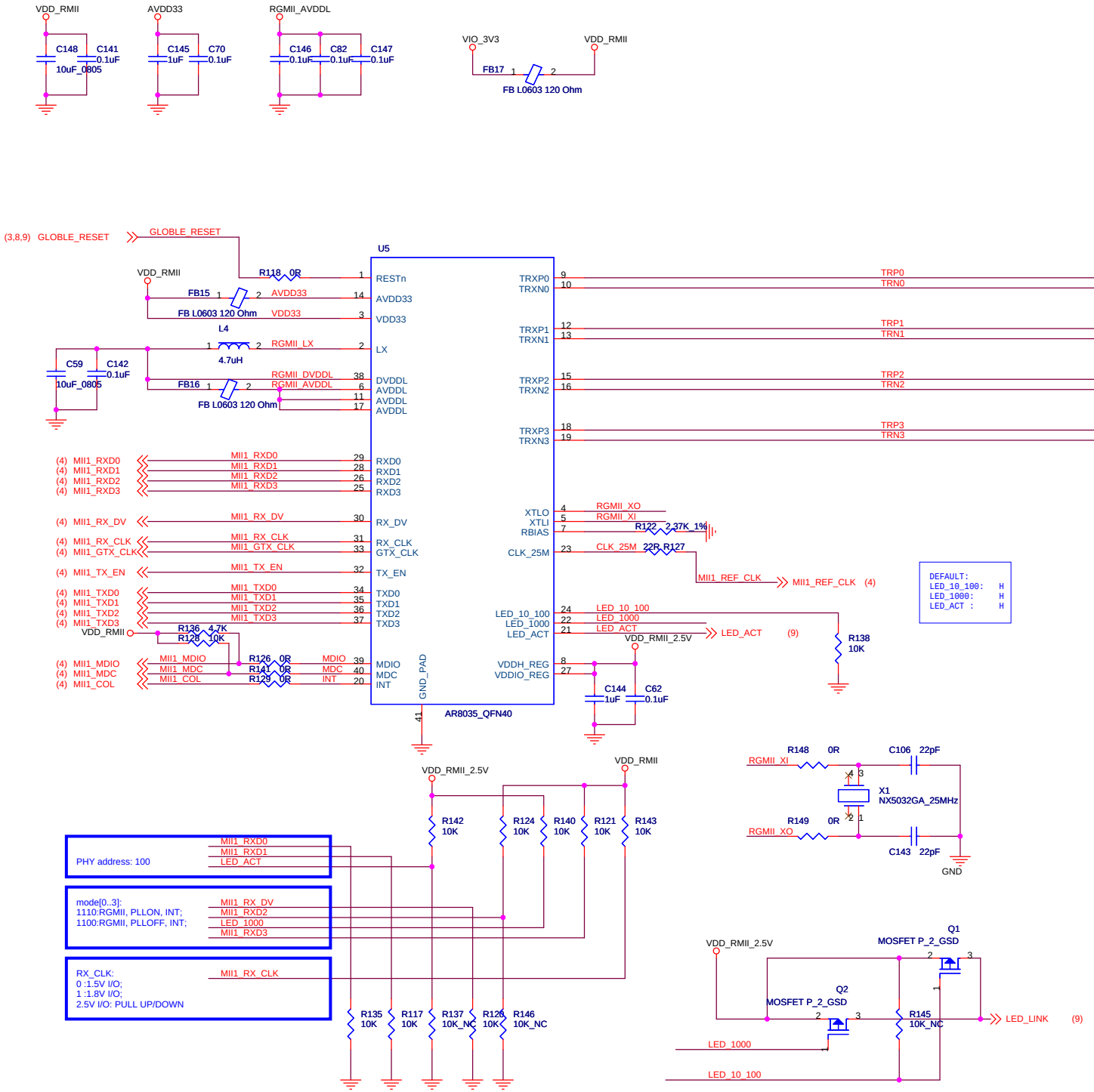
Standardize	<standardize>	Date Monday, November 17, 2014	Sheet 9 of 10



3.6 Power Pin Consumption

Table 3-12. **Power Pin Characteristic**

Symbol	Voltage Range	Current
AVDDL	1.1V ±5%	50.8 mA
DVDDL	1.1V ±5%	113.7 mA
AVDD33	3.3V ±5%	63.8 mA
VDDIO_REG	Connect VDDH_REG 2.5V	20.9 mA

NOTE: Data for components selection and layout guide

PHY Pin	PHY Core Config Signal	Description	Default Internal Weak Pull-up/Pull-down
RXD0	PHYADDRESS0	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00"	0
RXD1	PHYADDRESS1		0
LED_ACT	PHYADDRESS2		1
RX_DV	MODE0	mode select bit 0	0
RXD2	MODE1	mode select bit 1	0
LED_1000	MODE2	mode select bit 2	1
RXD3	MODE3	mode select bit 3	0
RX_CLK	1.8V/1.5V	Select the RGMII/RMII I/O voltage level 1: 1.8V I/O 0: 1.5V I/O	0

NOTE: 0=Pull-down, 1=Pull-up

NOTE: Power on strapping pins are latched during power-up reset or warm hardware reset.

NOTE: Some MAC devices input pins may drive high/low during power-up or reset. So PHY power on strapping status may be affected by the MAC side. In this case an external 10kΩ pull-down or pull-high resistor is needed to ensure a stable expected status.

NOTE: When using 2.5V RGMII I/O voltage level, RX_CLK can be pull-up or pull-down.

MODE[3:0]	Description
1100	RGMII, PLLOFF, INT;
1110	RGMII, PLLON, INT;
Others	Reserved

Design	<design>	CM335n	
Review	<review>	Title GIGA LAN	
Authorize	<authorize>	Size A3	Doc Name CM335X 141101 Ver. V1.0
Standardize	<standardize>	Date Monday, November 17, 2014	Sheet 10 of 10