AD-DAC-FMC-ADP
Quick Start Guide

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Getting Started with the AD-DAC-FMC-ADP Adapter Board

INTRODUCTION

The ADC-DAC-FMC-ADP adapter board allows any of Analog Devices' DPG2-compatiable High-Speed DAC Evaluation Boards to be used on a Xilinx® evaluation board with a FMC connector. The adapter board uses the Low Pin Count (LPC) version of the FMC connector, so it can be used on either LPC or HPC hosts (such as the ML605 or SP605).

A list of DPG2-compatiable evaluation boards can be found at http://www.analog.com/dpg

The schematic and layout are included in the following pages of this document. In addition, example UCF files for both the ML605 and SP605 are included as a starting point.

CLOCKING

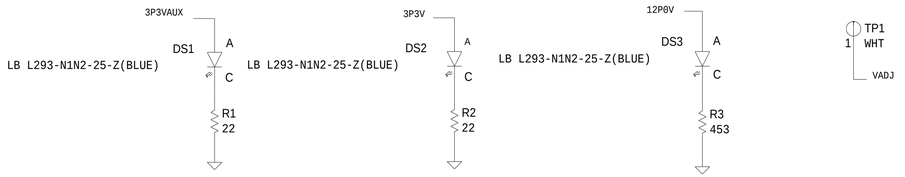
Every DPG2-compatiable evaluation board provides two LVDS clocks to the host. These two clocks are always identical in both frequency and phase. On DACs using an LVDS interface, the host is then expected to output two LVDS clocks that are phase aligned to the data. It is very important that these clocks be generated the same way as the data, so that any delays inside the FPGA are matched. Therefore, this clock should be considered another data bit with a fixed "10101" pattern.

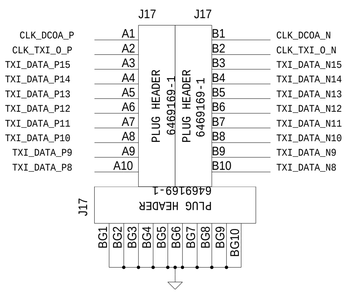
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

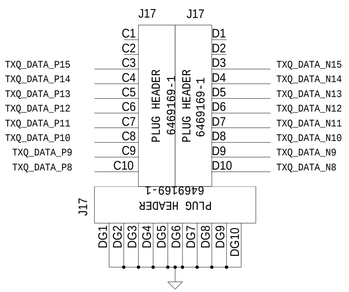
One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113 ©2010 Analog Devices, Inc. All rights reserved.

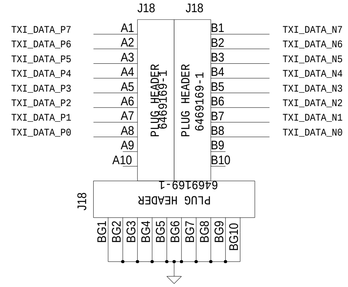
DPG2 CONNECTOR

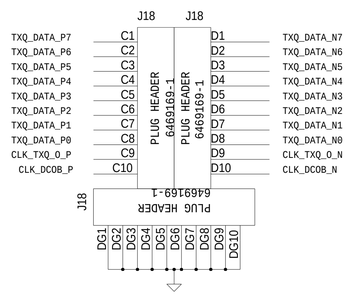
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	FIRST REVISION (PREVIOUS BOARD WAS HPC VERSION, WHICH THIS REPLACES)	7/2010	
B	TIE TDI AND TDO TOGETHER	3-30-12	J.C.
C	ADDED EEPROM	3-07-13	J.C.

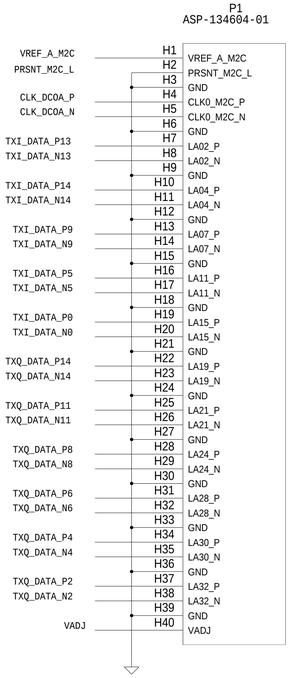


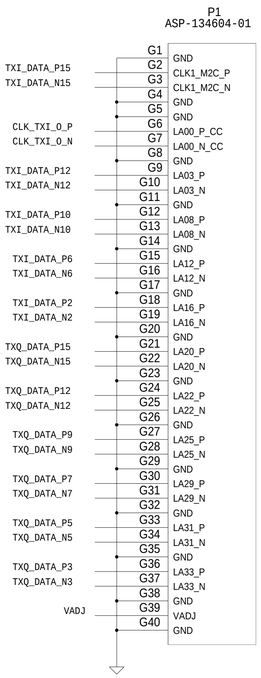


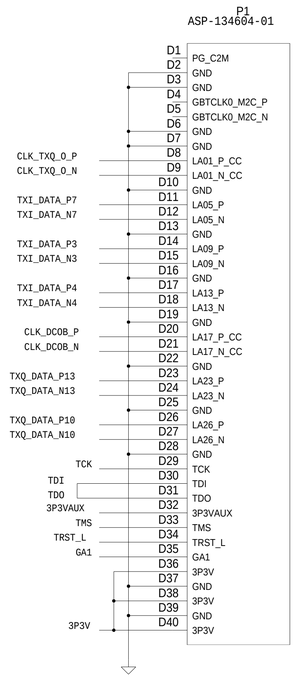


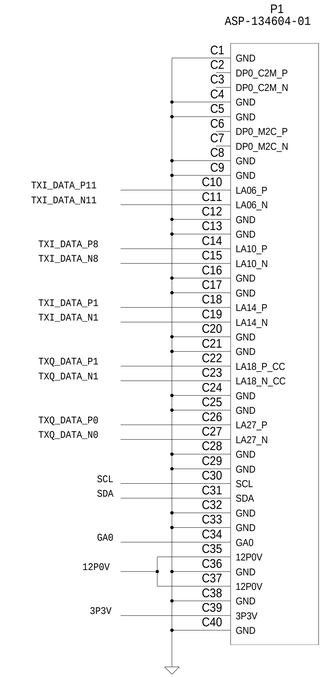




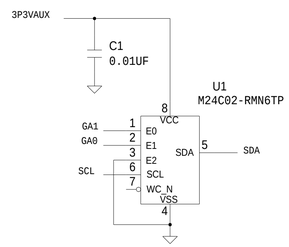








"C" ROW CLOSEST TO BOARD EDGE



SILKSCREEN NOTES:

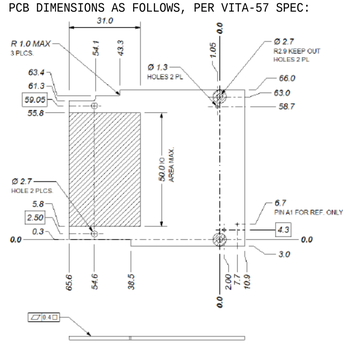
SAP PART NUMBER: AD-DAC-FMC-ADP
PART NUMBER AND PCB REVISION (BELOW) TO BE ON TOP SILKSCREEN

LAYOUT NOTES:

ALL LINES MATCHED LENGTH (MATCHING MORE CRITICAL THAN LINE LENGTH)
PAIRS WITHIN TXI____, TXQ____, CAN BE MOVED TO EASE ROUTING

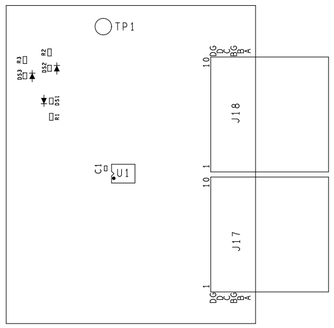
PCB NOTES:

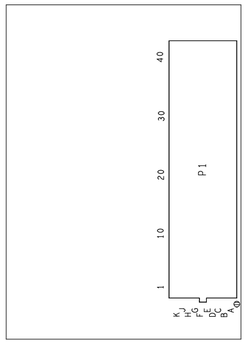
PCB DIMENSIONS AS FOLLOWS, PER VITA-57 SPEC:



ANALOG DEVICES	SCHEMATIC	
	DPG2 LPC ADAPTER BRD AD-DAC-FMC-ADP -	
THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.	DESIGN VIEW -	DRAWING NO. HSC 10033 — REV C
	PTD ENGINEER J COUTERMARSH	SIZE D — SCALE - — SHEET 2 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	16AUG10	J.C.
B	TIE TDO AND TDI TOGETHER	30MAR12	J.C.
C	ADDED EEPROM	13MAR13	J.C.



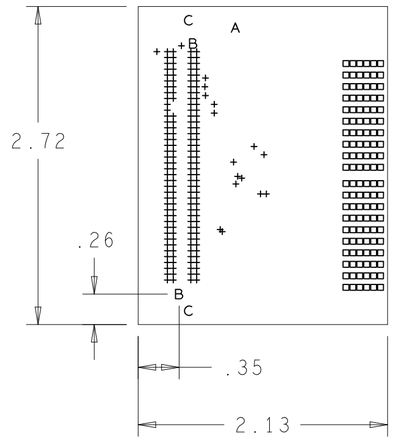


PRIMARY SIDE

SECONDARY SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX +-.010 +-1/32 +/- 2 .XXX +-.005	ASSEMBLY		ANALOG DEVICES HSC DIVISION 804 WOBURN STREET WILMINGTON, MA 01887
	APPROVAL	DATE	TITLE: VITA57 TO DPGA ADAPTER BOARD (AD-DAC-FMC-ADP)
MATERIAL	DRAWN BY W.D.B.	16AUG10	
	DESIGNED		
	CHECKED		
FINISH	APPROVED		SIZE: C; FSCM NO: ; DRAWING NUMBER: HSC 10033; REV: C
	MFG ENGINEER		
DO NOT SCALE DWG			SCALE 1/1; SHEET 1 OF 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	16AUG10	J.C.
B	TIE TDO AND TDI TOGETHER	30MAR12	J.C.
C	ADDED EEPROM	13MAR13	J.C.



PRIMARY SIDE

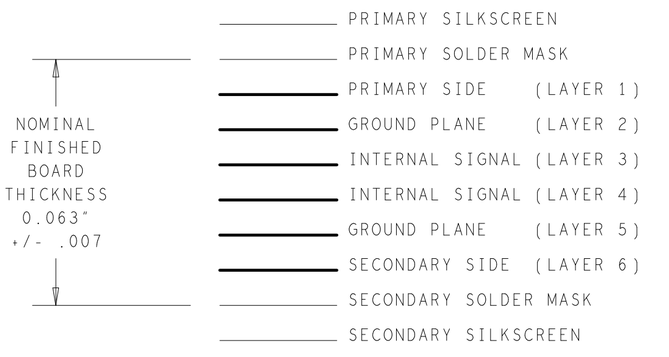
NOTES:

MATERIALS: FR-4, IN ACCORDANCE WITH IPC-L-130 (LATEST REV.). GLASS FABRIC BASE, EPOXY RESIN, FIRE RESISTANT.
BONDING AGENT: PREIMPREGNATED B STAGE EPOXY GLASS CLOTH IN ACCORDANCE WITH IPC-L-109 (LATEST REV.).
CLADDING: EXTERNAL LAYERS 1/4 OZ. COPPER, OVERPLATE TO 1 OZ. INTERNAL PLANE LAYERS 2 OZ. COPPER.
SOLDER MASK: SHALL BE BLUE LIQUID PHOTOIMAGABLE (LPI) APPLIED ON BOTH SIDES OVER BARE COPPER AND SHALL MEET IPC-SM-840 (LATEST REV.) CLASS 3.
SILK SCREEN: SHALL BE PERMANENT NON-CONDUCTIVE EPOXY INK, COLOR WHITE.
U.L. RATING: 94VO MINIMUM.

FABRICATION:

1. REFER TO IPC-6010 SERIES (LATEST REV.), CLASS 2 FOR FABRICATION UNLESS OTHERWISE SPECIFIED.
2. UNDIMENSIONED HOLES TO BE LOCATED WITHIN +/-.005 OF THEIR TRUE POSITION WITH RESPECT TO ARTWORK.
3. PLATED HOLE WALL THICKNESS SHALL NOT BE LESS THAN .001 INCH MINIMUM AVERAGE, WITH NO READING LESS THAN .0008 BY CROSS SECTION.
4. HOLE DIAMETERS APPLY AFTER PLATING.
5. FINISHED CONDUCTOR WIDTHS SHALL NOT BE REDUCED FROM THE NOMINAL, INDICATED ON THE MASTER PATTERN, BY MORE THAN THE CONDUCTOR THICKNESS.
6. MINIMUM DESIGN LINE WIDTH IS .008 INCH.
7. MINIMUM DESIGN SPACING IS .005 INCH.
8. BOARD/PANEL MUST MEET IPC-A-600 (LATEST REV.) CLASS 2 FOR FLATNESS.
9. MFGR. TO LEGIBLY ETCH OR STAMP/SCREEN WITH PERMANENT NON-CONDUCTIVE INK ON SECONDARY SIDE IN A CLEAR AREA UNLESS OTHERWISE INDICATED;
   A. U.L. CODE
   B. DATE CODE (STAMP)
   C. FLAMMABILITY RATING
   D. MFGR. LOGO
   E. SUCCESSFUL ELECTRICAL BOARD TEST.
10. NON-FUNCTIONAL PADS MAY BE REMOVED FROM INNER SIGNAL LAYERS AT MFGR. DISCRETION.
11. IF PAD SIZES PROVIDED ARE NOT LARGE ENOUGH TO MAINTAIN ANNULAR RING REQUIREMENT, MFGR. MAY TEAR DROP PADS TO MAINTAIN ANNULAR RING AT PAD TO CIRCUIT INTERFACE ONLY AND MUST INSURE ELECTRICAL INTEGRITY.
12. REPAIRS PER IPC-R-700 ARE ALLOWED.
13. MODIFICATIONS TO THE ARTWORK, OTHER THAN THOSE DESCRIBED ON THE FABRICATION DRAWING, ARE NOT ALLOWED WITHOUT WRITTEN AUTHORIZATION.
14. FINISH: SURFACES SHALL HAVE ENIG FINISH PLATED WITH 2-6 MICROINCHES OF IMMERSION GOLD OVER 100-200 MICROINCHES OF ELECTROLESS NICKEL.

6 LAYER STACKUP



DIFFERENTIAL IMPEDANCE = 100 OHMS +/- 10%
ARTWORK LINE WIDTH FOR IMPEDANCE CONTROLLED LINES = 0.005"

HOLE TOLERANCE

UNLESS SPECIFIED
PLATED: +/- .003
NON PLATED: +/- .001

FINISHED HOLES IN MILS ALL UNITS ARE IN MILS				
FIGURE	SIZE	PLATED	QTY	TOLERANCE/NOTES
+	10.0	PLATED	175	
□	24.0	PLATED	120	
A	63.0	PLATED	1	
B	50.0	NON-PLATED	2	
C	105.0	NON-PLATED	2	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX +-.010 .XXX +-.005 FRACTIONS +-1/32 ANGLES +/- 2

NCDRILL

APPROVAL	DATE
DRAWN BY W.D.B.	16AUG10
DESIGNED	
CHECKED	
APPROVED	
MFG ENGINEER	

MATERIAL

FINISH

DO NOT SCALE DWG

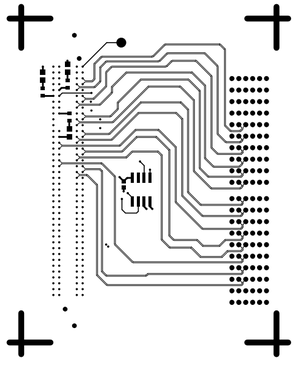
ANALOG DEVICES
HSC DIVISION
804 WOBURN STREET
WILMINGTON, MA 01887

TITLE: VITA57 TO DPGA ADAPTER BOARD (AD-DAC-FMC-ADP)

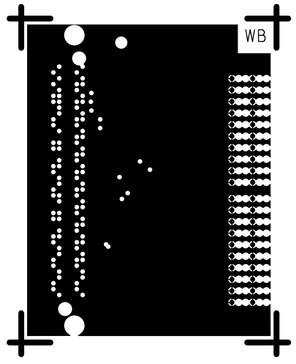
SIZE	FSCM NO	DRAWING NUMBER	REV
C		HSC 10033	C

SCALE 1/1 SHEET 1 OF 1

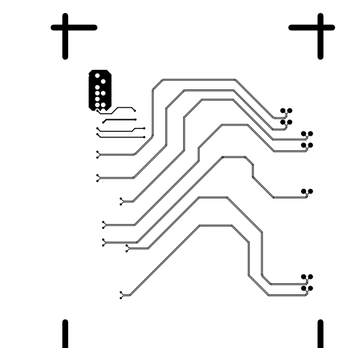
L1 PRIMARY
VITA57-DPG2 ADAPTER BRD
HSC 10033
REV C



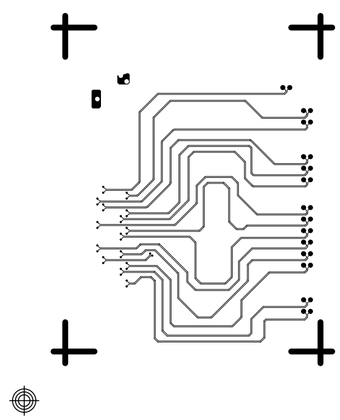
L2_GROUND
VITA57-DPG2 ADAPTER BRD
HSC 10033
REV C



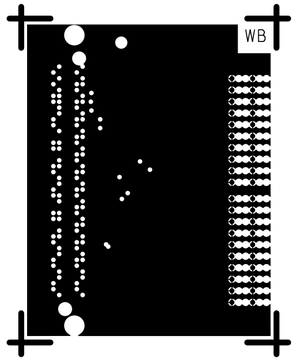
L3_SIGNAL
VITA57-DPG2 ADAPTER BRD
HSC 10033
REV C



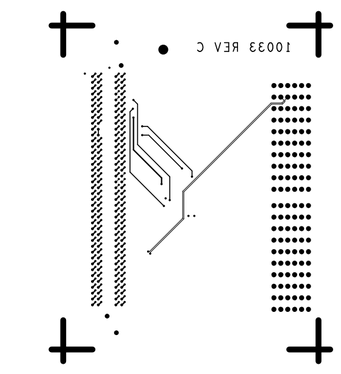
L4_SIGNAL
VITA57-DPG2 ADAPTER BRD
HSC 10033
REV C



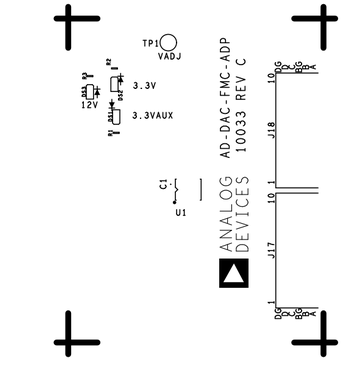
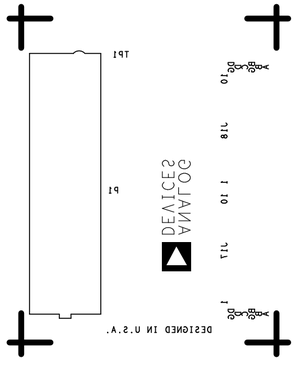
L5_GROUND
VITA57-DPG2 ADAPTER BRD
HSC 10033
REV C



L6 SECONDARY
VITA57-DPG2 ADAPTER BRD
HSC 10033
REV C



SILKSCREEN PRIMARY
VITA57-DPG2 ADAPTER BRD
HSC 10033
REV C



SILKSCREEN SECONDARY
VITA57-DPG2 ADAPTER BRD
HSC 10033
REV C