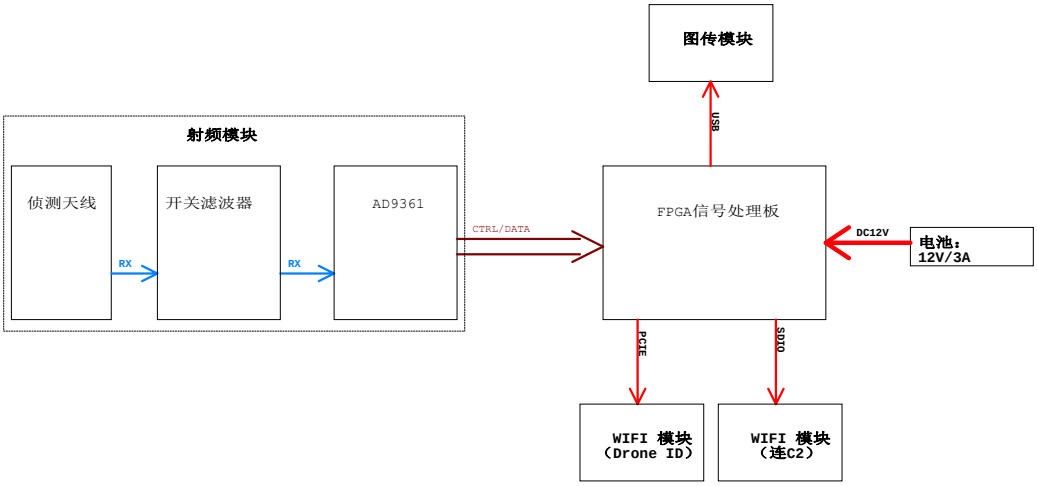
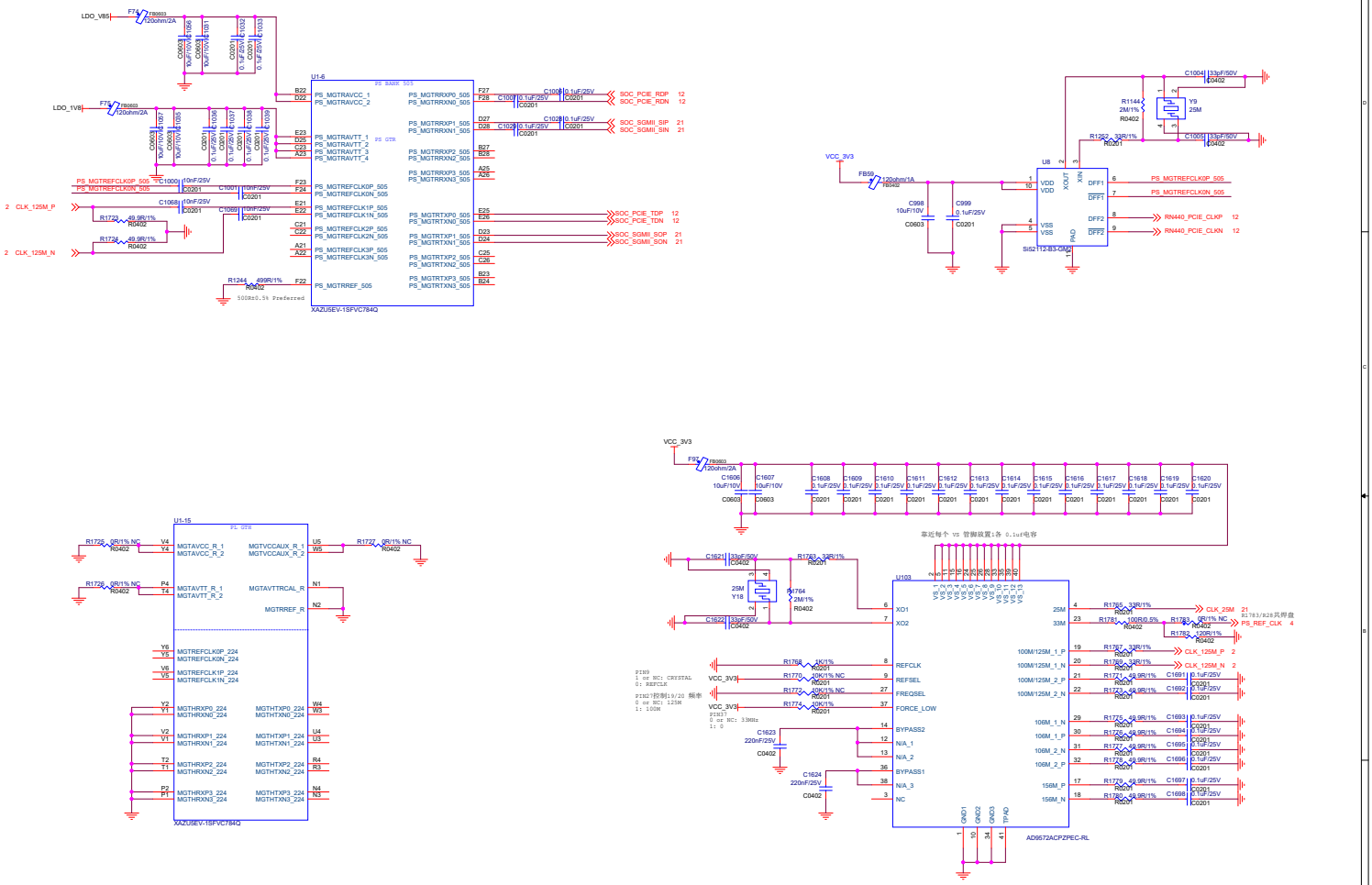
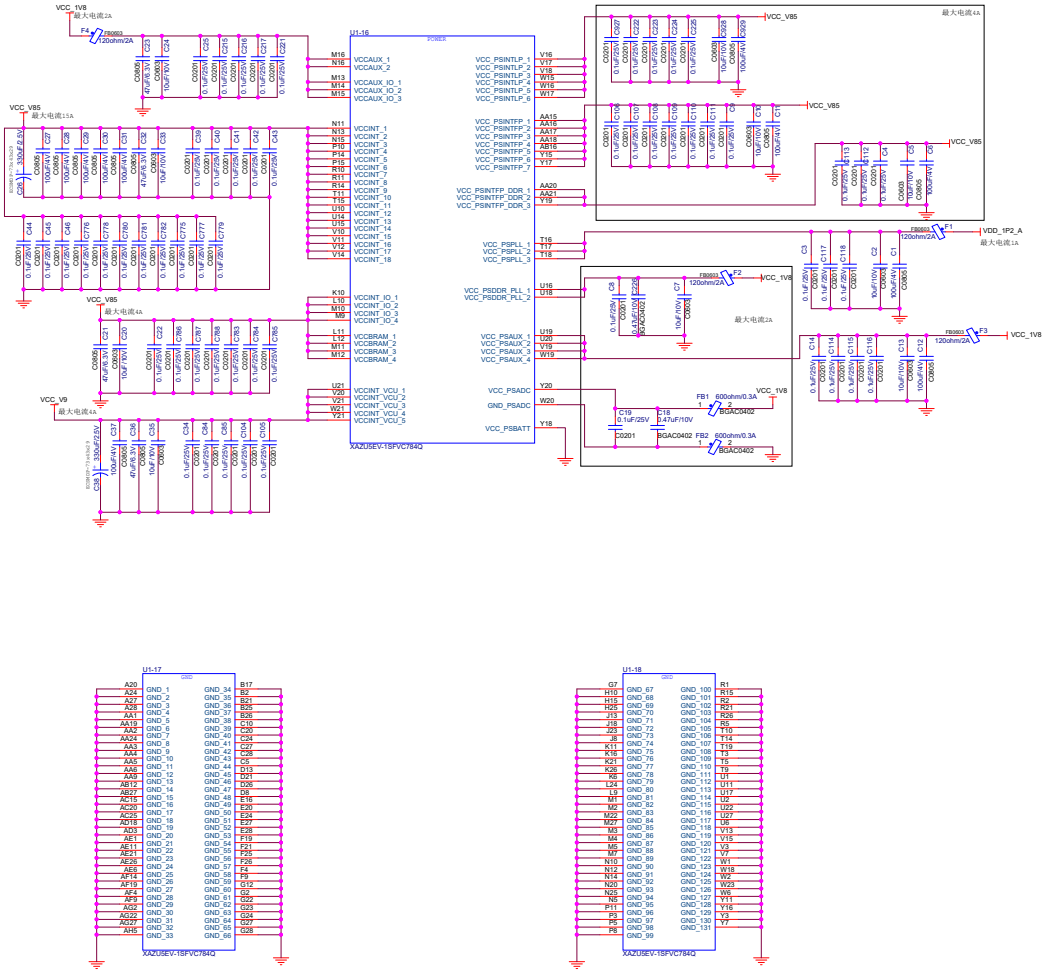


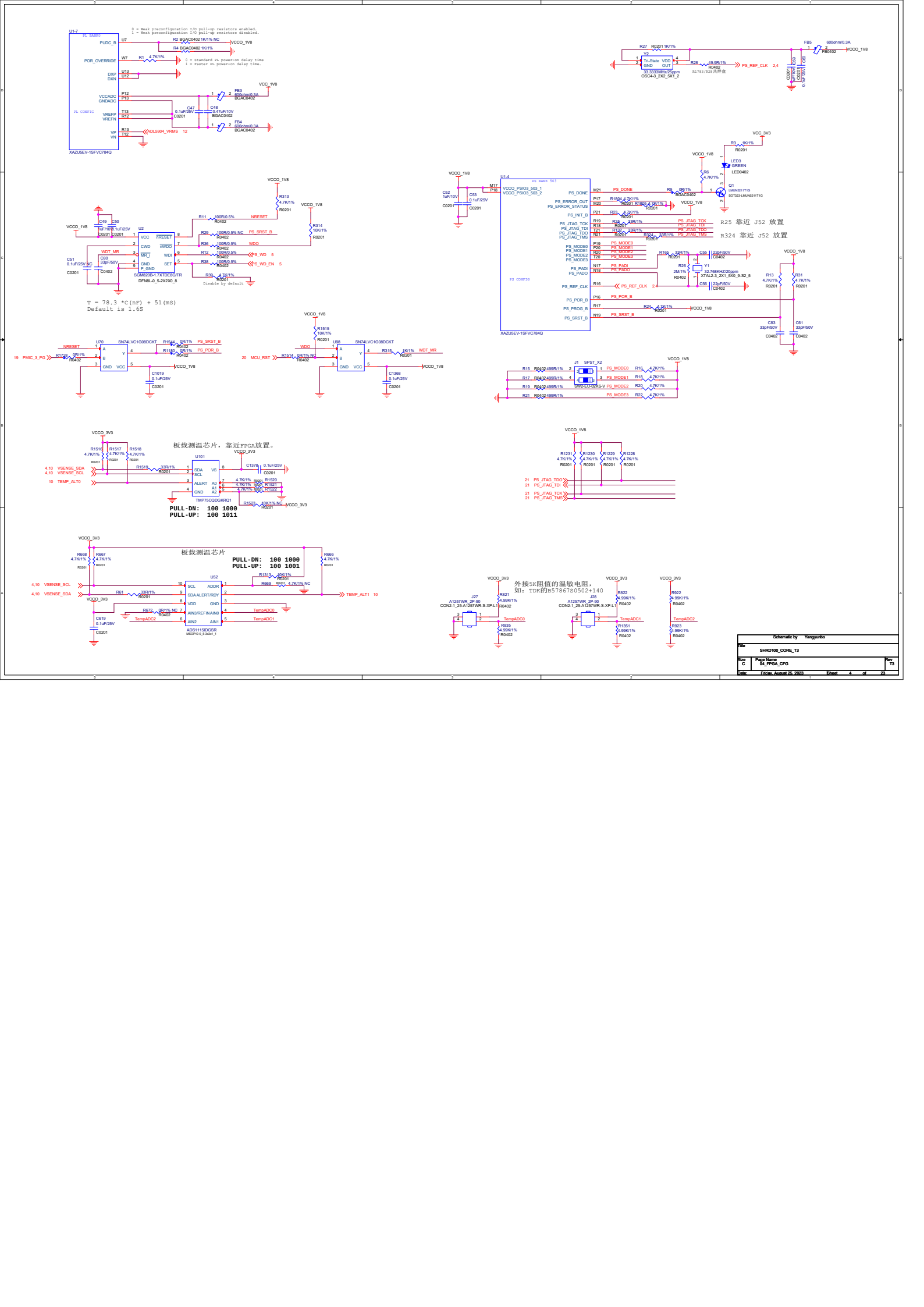
Schematic by	Yangyunbo	
Title	SHRD100_CORE_T3	
Size: C	Page Name: 01_System block	Rev: T3
Date: Friday, August 25, 2023	Sheet 1 of 23	

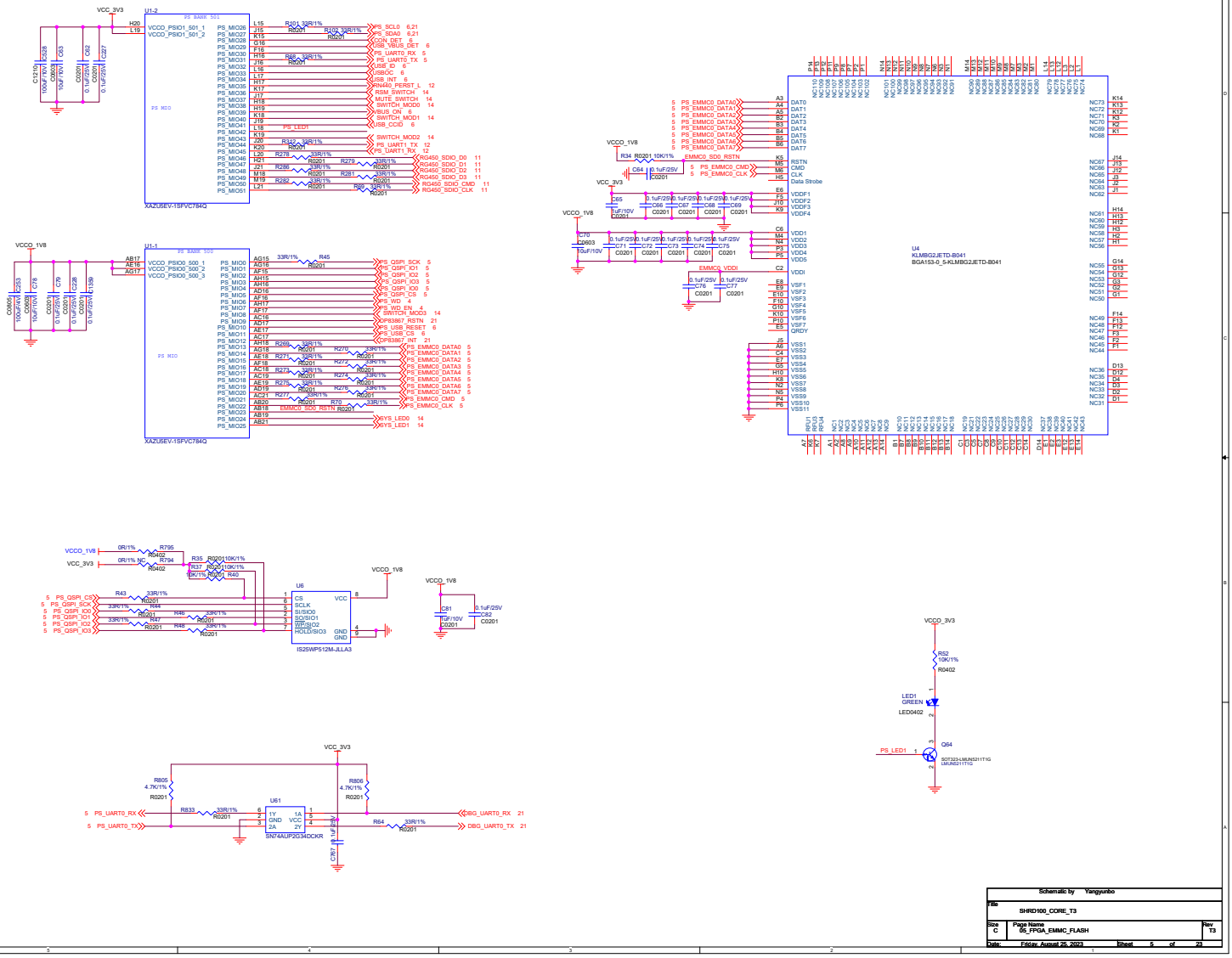


Schematic by	Yangyunbo		
Title	SHRD100_CORE_T3		
Size C	Page Name 02_FPGA_GTR		Rev T3
Date: Friday, August 25, 2023	Sheet 2	of 23	

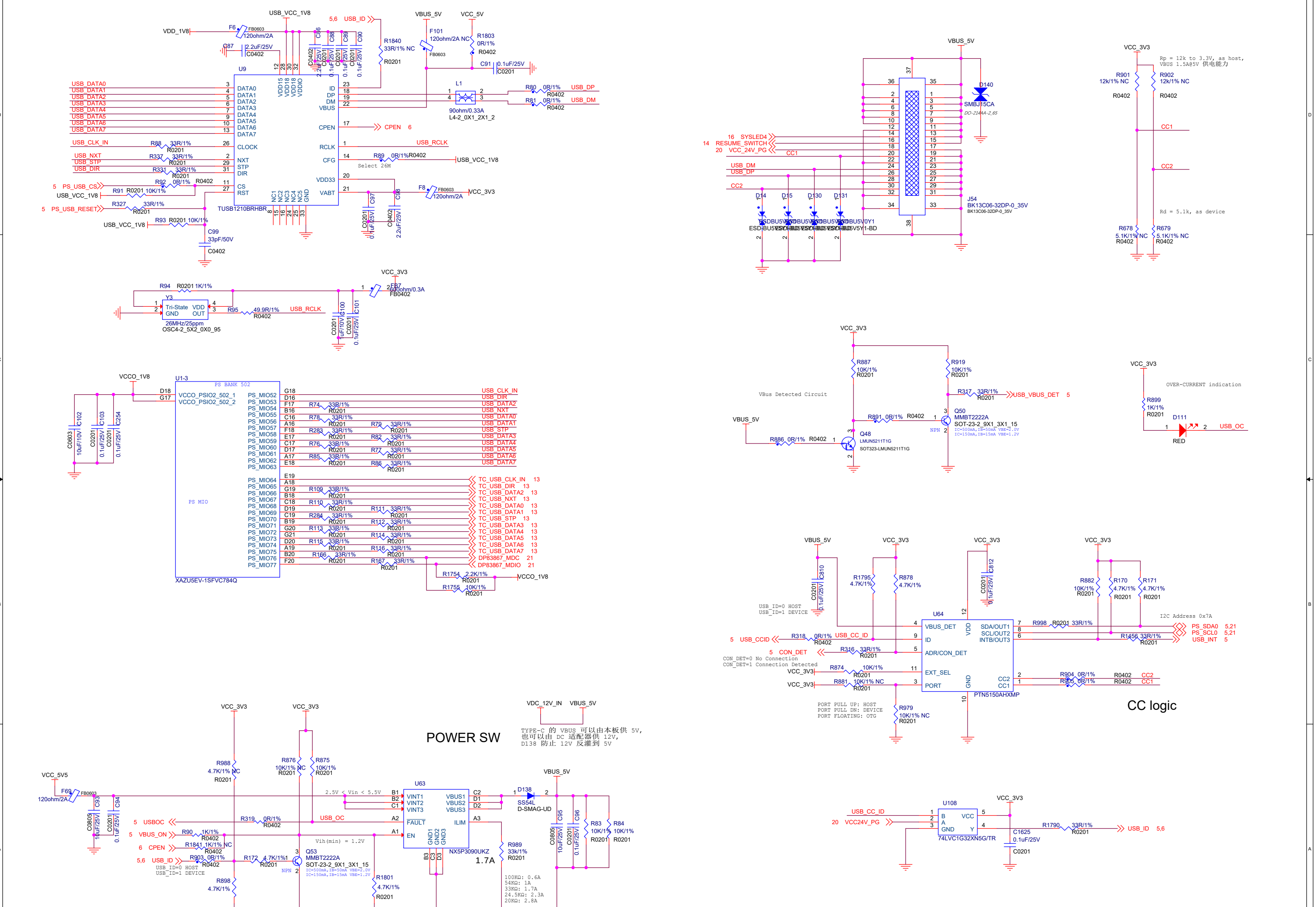


Schematic by	Yangyunbo		
Title	SHRD100_CORE_T3		
Size C	Page Name 03_FPGA_POWER		Rev T3
Date: Friday, August 25, 2023	Sheet 3	of 23	

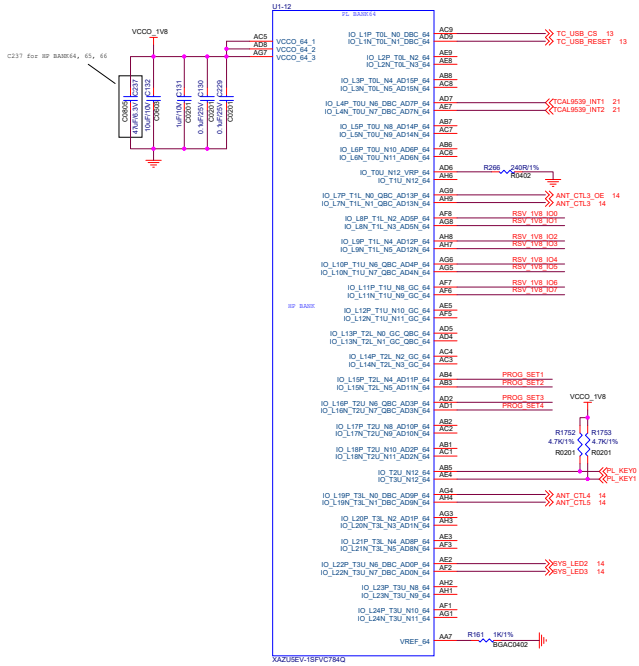

U1-7
PL BANK0
PUDC_B
POR_OVERRIDE
DXP
DXN
VCCADC
GNDADC
PL CONFIG
VREFP
VREFN
VP
VN
XAZU5EV-1SFVC784Q
0 = Weak preconfiguration I/O pull-up resistors enabled.
1 = Weak preconfiguration I/O pull-up resistors disabled.
0 = Standard PL power-on delay time
1 = Faster PL power-on delay time.
VCCO_1V8
VCC_1V8
ADL5904_VRMS
R27 R0201 1K/1%
Y2
Tri-State VDD
GND OUT
33.3333MHz/25ppm
OSC4-3_2X2_5X1_2
R28 49.9R/1%
R0402
PS_REF_CLK
FB5 600ohm/0.3A
FB0402
VCCO_3V3
R3 1K/1%
R0201
LED3
GREEN
LED0402
Q1
LMUN5211T1G
SOT323-LMUN5211T1G
R6 4.7K/1%
BGAC0402
U2
VCC
CWD
MR
GND
nRESET
nWDO
WDI
SET
P_GND
SGM826B-1.7XTDE8G/TR
DFN8L-0_5-2X2X0_8
R313 4.7K/1%
R314 10K/1%
R11 100R/0.5% NC
R29 100R/0.5% NC
R36 100R/0.5%
R12 100R/0.5%
R38 100R/0.5%
R39 4.7K/1%
Disable by default
PS_SRST_B
WDO
PS_WD
PS_WD_EN
NRESET
WDT_MR
T = 78.3 *C(nF) + 51(mS)
Default is 1.6S
U1-4
PS BANK 503
PS CONFIG
XAZU5EV-1SFVC784Q
PS_DONE
PS_ERROR_OUT
PS_ERROR_STATUS
PS_INIT_B
PS_JTAG_TCK
PS_JTAG_TDI
PS_JTAG_TDO
PS_JTAG_TMS
PS_MODE0
PS_MODE1
PS_MODE2
PS_MODE3
PS_PADI
PS_PADO
PS_REF_CLK
PS_POR_B
PS_PROG_B
PS_SRST_B
R25 靠近 J52 放置
R324 靠近 J52 放置
Y1
32.768KHZ/20ppm
XTAL2-3_2X1_5X0_9-S2_5
U70
SN74LVC1G08DCKT
U98
R1544 0R/1%
R1545 0R/1%
R1728 0R/1%
R1514 0R/1% NC
R315 1K/1%
C1019 0.1uF/25V
C1368 0.1uF/25V
J1 SPST_X2
SW2-EU-02KS-V
R15 R0402 499R/1%
R17 R0402 499R/1%
R19 R0402 499R/1%
R21 R0402 499R/1%
R16 4.7K/1%
R18 4.7K/1%
R20 4.7K/1%
R22 4.7K/1%
板载测温芯片，靠近FPGA放置。
U101
TMP75CQDGKRQ1
R1519 33R/1%
R1520 4.7K/1%
R1521 4.7K/1%
R1522 4.7K/1%
R1523 10K/1% NC
C1378 0.1uF/25V
PULL-DN: 100 1000
PULL-UP: 100 1011
R1231 4.7K/1%
R1230 4.7K/1%
R1229 4.7K/1%
R1228 4.7K/1%
板载测温芯片
U52
ADS1115IDGSR
MSOP10-0_53dxH_1
R61 33R/1%
R672 0R/1% NC
R1313 10K/1%
R669 4.7K/1% NC
R666 4.7K/1%
R668 4.7K/1%
R667 4.7K/1%
C619 0.1uF/25V
PULL-DN: 100 1000
PULL-UP: 100 1001
外接5K阻值的温敏电阻，
如：TDK的B57867S0502+140
J27
A1257WR-2P-90
CON2-1_25-A1257WR-S-XP-L1
J28
R821 4.99K/1%
R835 4.99K/1%
R822 4.99K/1%
R1351 4.99K/1%
R922 4.99K/1%
R923 4.99K/1%
TempADC0
TempADC1
TempADC2
Schematic by Yangyunbo
Title
SHRD100_CORE_T3
Size C
Page Name 04_FPGA_CFG
Rev T3
Date: Friday, August 25, 2023
Sheet 4 of 23

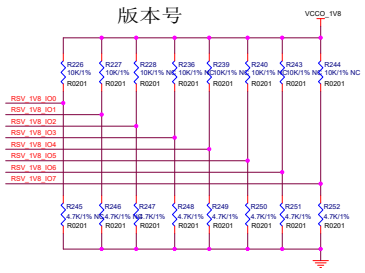


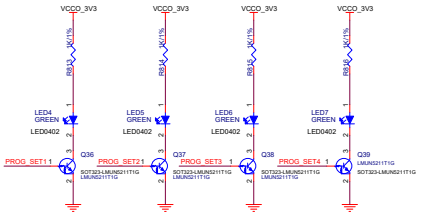
Schematic by	Yangyunbo
Title	SHRD100_CORE_T3
Size	C
Page Name	05_FPGA_EMMC_FLASH
Rev	T3
Date:	Friday, August 25, 2023
Sheet	5 of 23



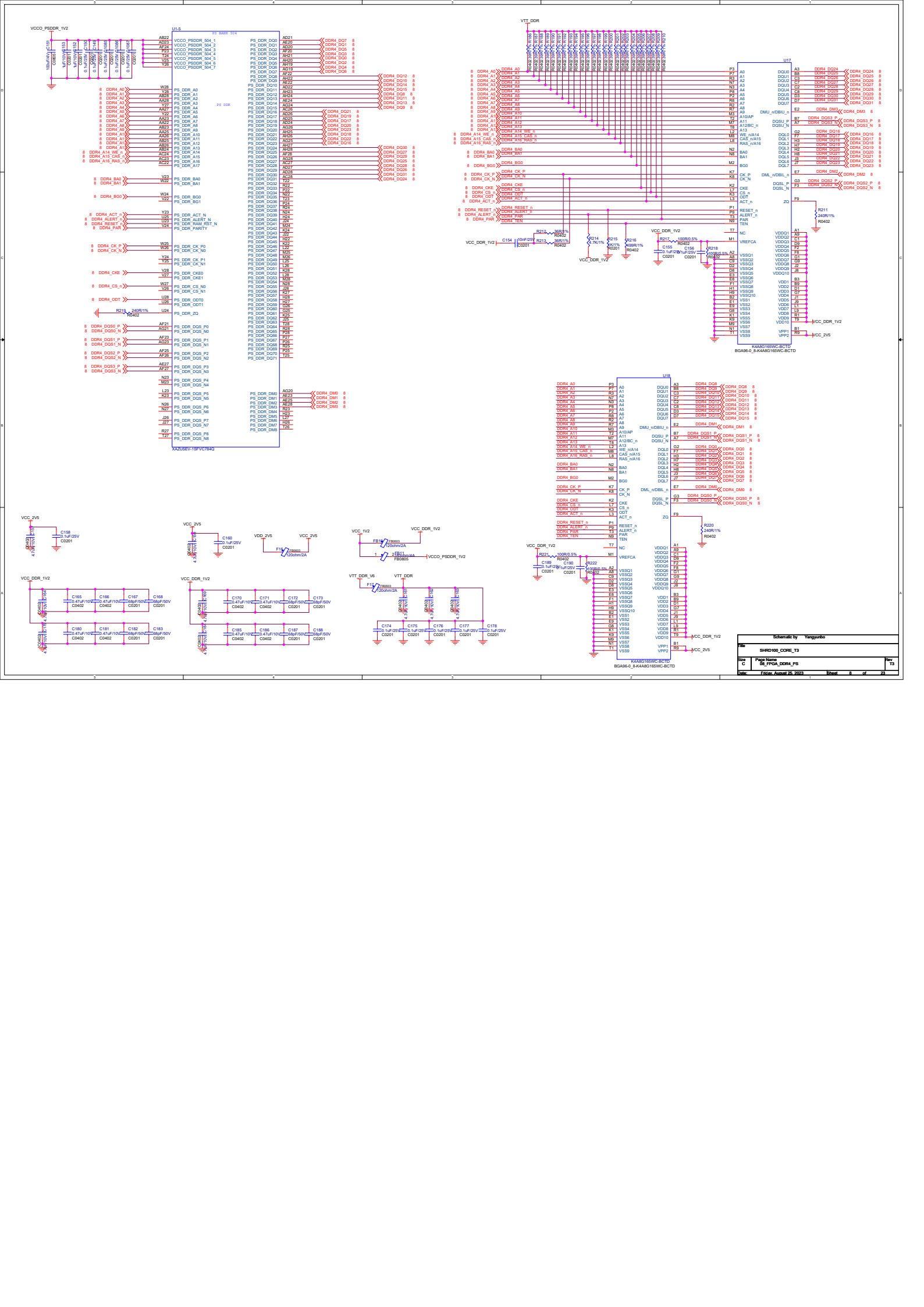
Schematic by	Yangyunbo		
Title	SHRD100_CORE_T3		
Size C	Page Name 06_FPGA_USB		Rev T3
Date: Friday, August 25, 2023	Sheet 6 of 23		







Schematic by	Yangyunbo		
Title	SHRD100_CORE_T3		
Size C	Page Name 07_FPGA_BANK64		Rev T3
Date: Friday, August 25, 2023	Sheet 7	of 23	


VCCO_PSDDR_1V2
U1-5
PS BANK 504
XAZU5EV-1SFVC784Q
VTT_DDR
U17
U18
K4A8G165WC-BCTD
BGA96-0_8-K4A8G165WC-BCTD
VCC_DDR_1V2
VCC_2V5
VCC_1V2
VTT_DDR_V6
VDD_2V5
VCCO_PSDDR_1V2
Schematic by Yangyunbo
SHRD100_CORE_T3
Page Name 06_FPGA_DDR4_PS
Rev T3
Friday, August 25, 2023
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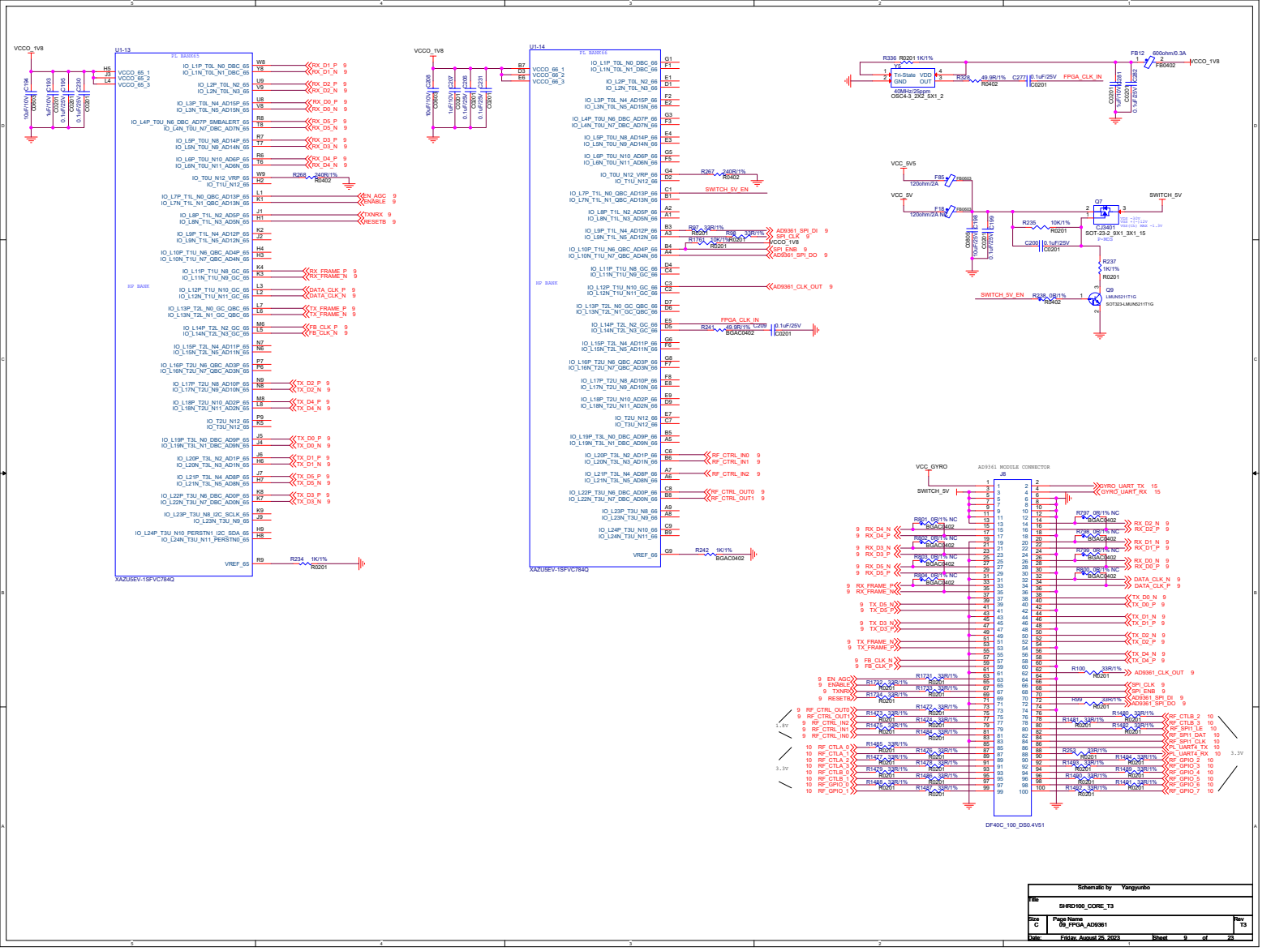
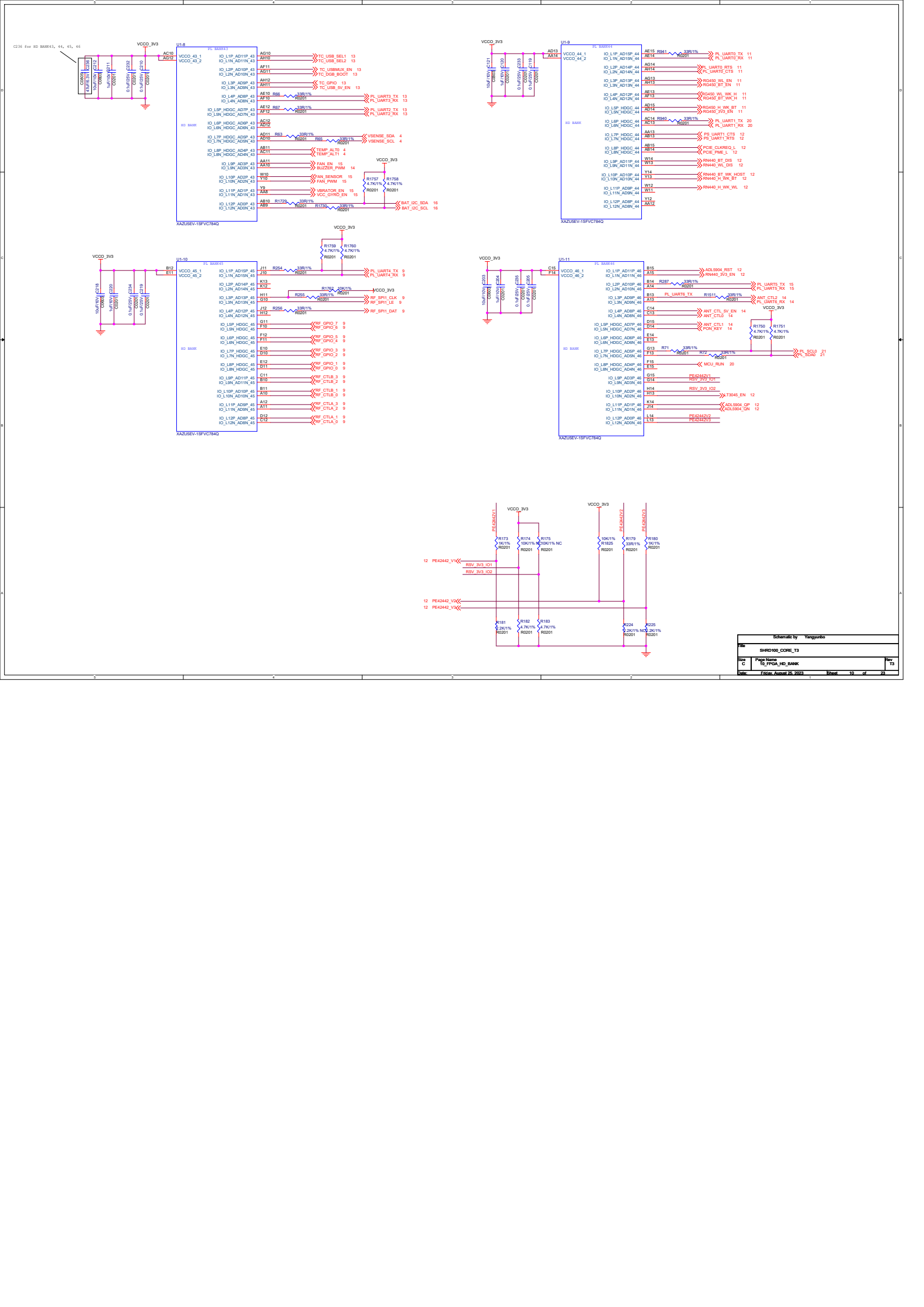


Schematic by	Yangyunbo		
Title	SHRD100_CORE_T3		
Size	Page Name		Rev
C	09_FPGA_AD9361		T3
Date:	Friday, August 25, 2023	Sheet 9 of 23	


C236 for HD BANK43, 44, 45, 46
VCCO_3V3
U1-8
PL BANK43
XAZU5EV-1SFVC784Q
HD BANK
U1-9
PL BANK44
U1-10
PL BANK45
U1-11
PL BANK46
PE42442V1
PE42442V2
PE42442V3
Schematic by Yangyunbo
SHRD100_CORE_T3
Size C
Page Name T0_FPGA_HD_BANK
Rev T3
Date: Friday, August 25, 2023
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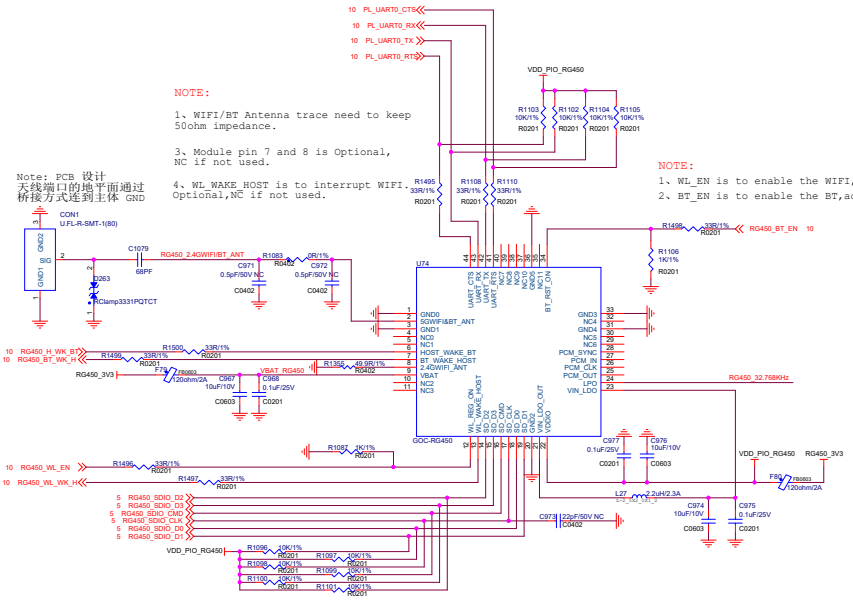
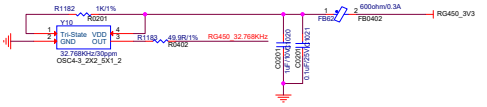


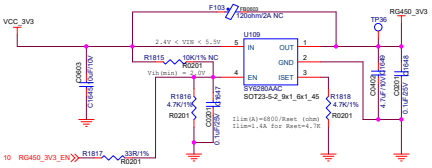
UART Connection between Module and Host.

Host	Module
UART_TX	UART_RX
UART_RX	UART_TX
UART_CTS	UART_RTS
UART_RTS	UART_CTS

PCM Connection between Module and Host.

Host	Module
PCM_CLK	PCM_CLK
PCM_SYNC	PCM_SYNC
PCM_IN	PCM_OUT
PCM_OUT	PCM_IN





SDIO NOTE:

1、Trace total length < 4000mils, and six signals trace length difference <300mils.
2、Add damping resistor.
3、SDIO signals do not allow crossed over and overlapped.
4、CLK signals should keep well ground.
5、The less changing the PCB layer the better.

Power and LPO Note:

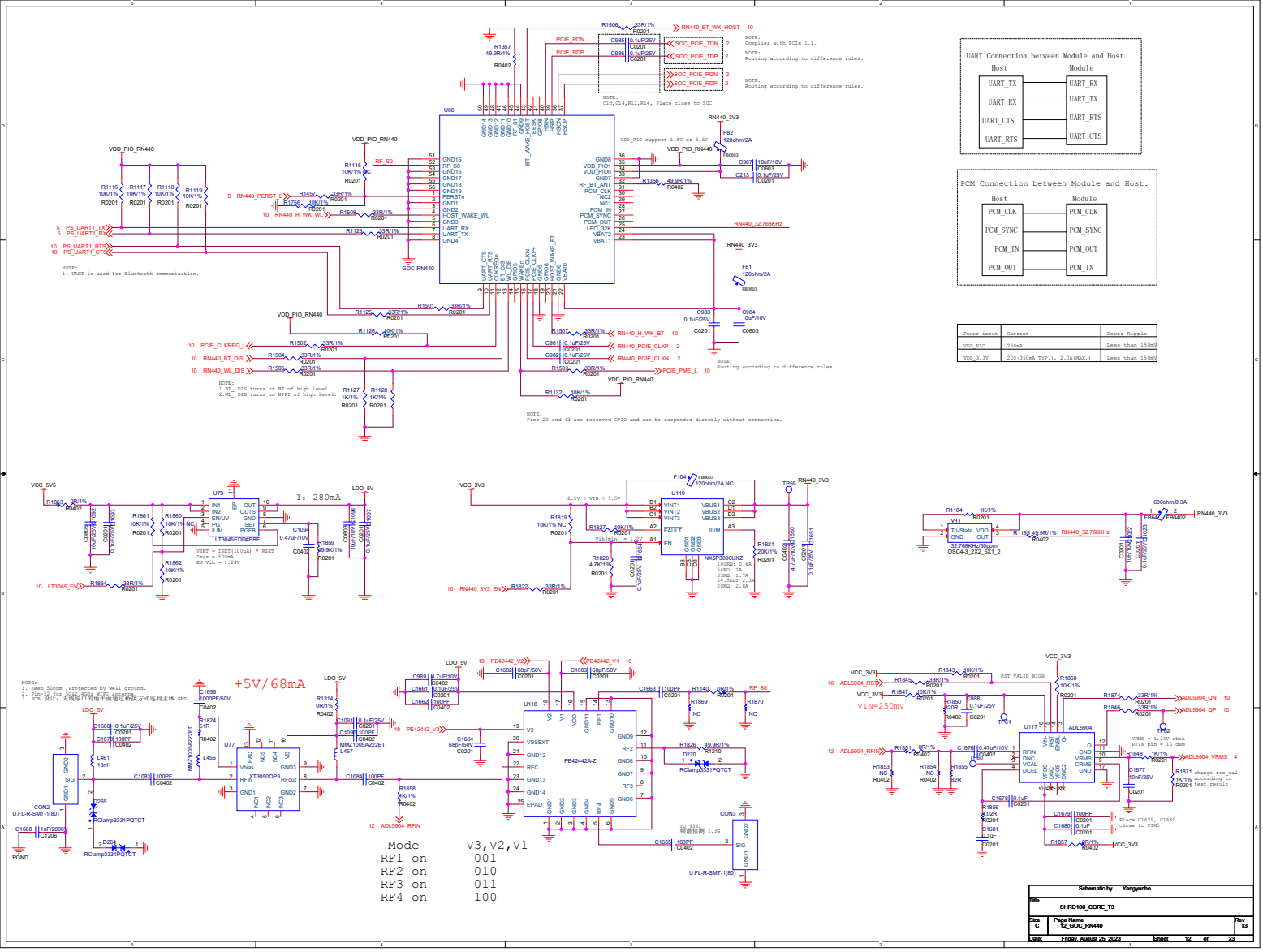
1.This module requires two sets of power supply VDD_3.3V and VDD_PIO. Independent power supply is recommended.The power ripple is less than 80 mV. Current for power supply :

Power input	Current	Power Ripple
VDD_PIO	150mA	Less than 80mV
VDD_3.3V	200-350mA(TYP.);700mA(MAX.)	Less than 80mV

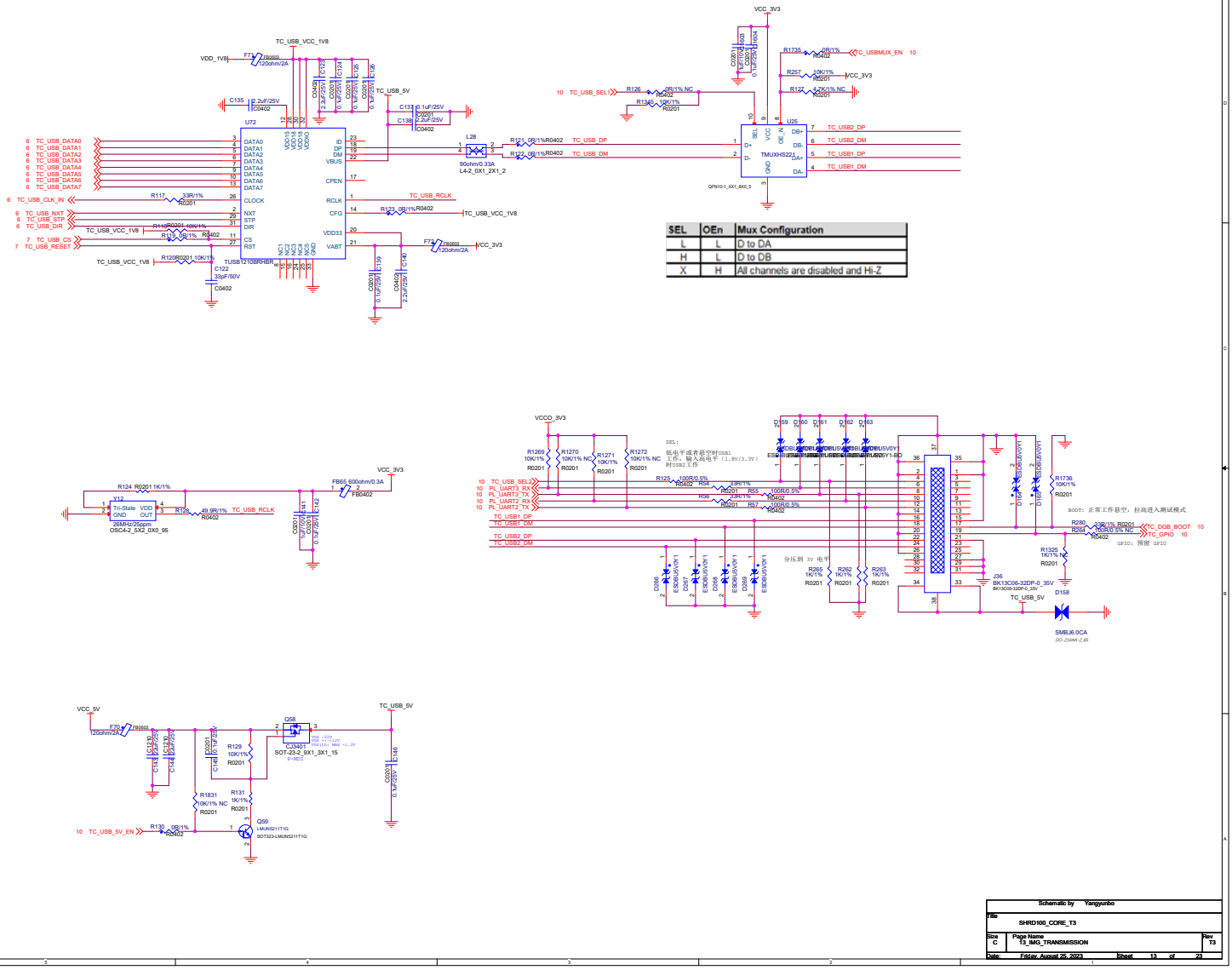
2、VDD_PIO support 1.8V or 3.3V.It mainly depends on the voltage supported by I/O on host side.

3、EXT_LPO(32.768KHz) is Optional,NC if not used.

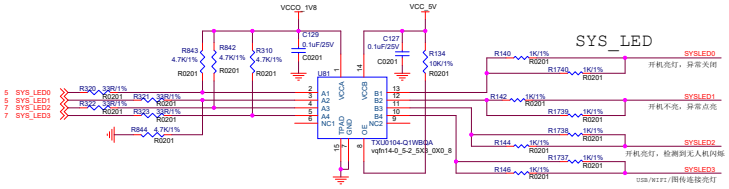
Schematic by	Yangyunbo		
Title	SHRD100_CORE_T3		
Size C	Page Name T1_GOC-RG450		Rev T3
Date:	Friday, August 25, 2023	Sheet 11 of	23

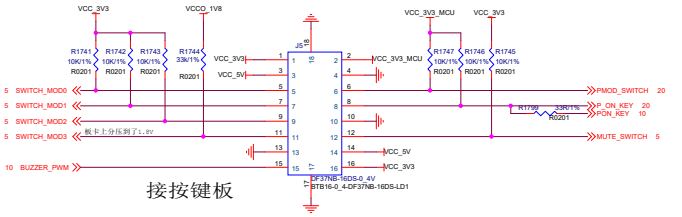


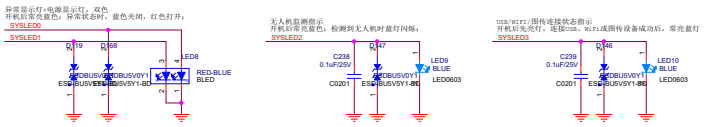
Schematic by	Yangyunbo
Title	SHRD100_CORE_T3
Size	C
Page Name	T2_GOC_RN440
Rev	T3
Date:	Friday, August 25, 2023
Sheet	12 of 23

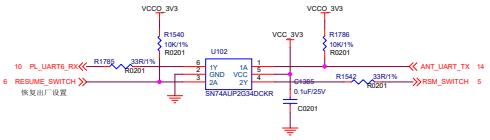


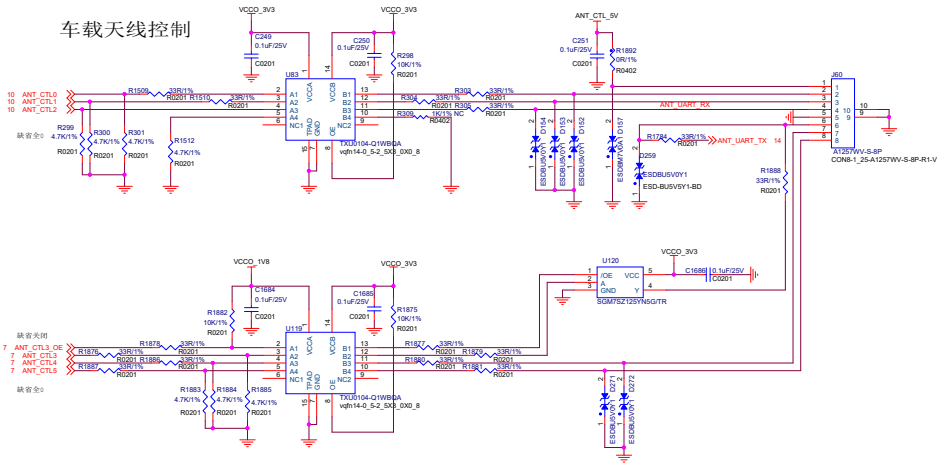
Schematic by	Yangyunbo		
Title	SHRD100_CORE_T3		
Size C	Page Name T3_IMG_TRANSMISSION		Rev T3
Date: Friday, August 25, 2023	Sheet 13	of 23	

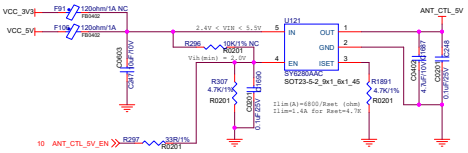






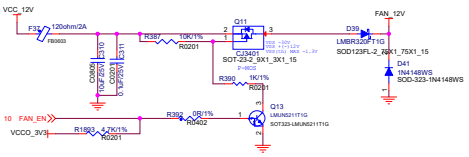




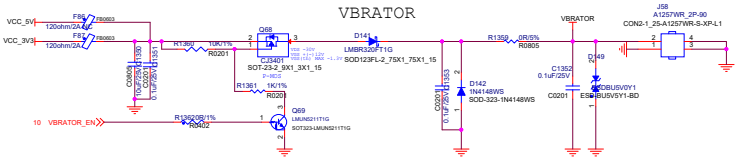


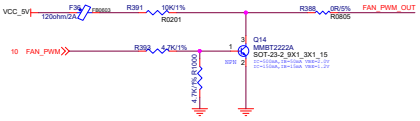
Schematic by	Yangyunbo		
Title	SHRD100_CORE_T3		
Size C	Page Name T4_USR_INTERFACE		Rev T3
Date:	Friday, August 25, 2023	Sheet 14 of 23	

FAN

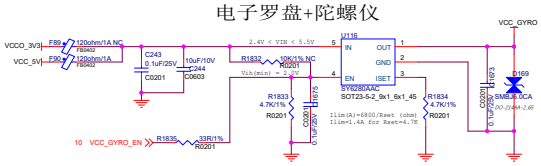


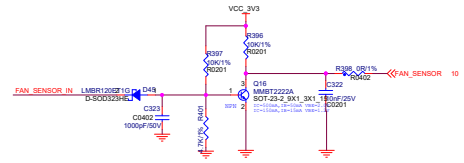
VBRATOR

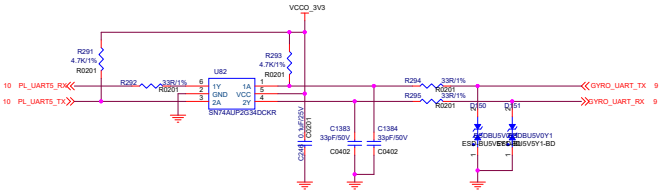


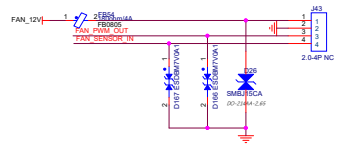


电子罗盘+陀螺仪

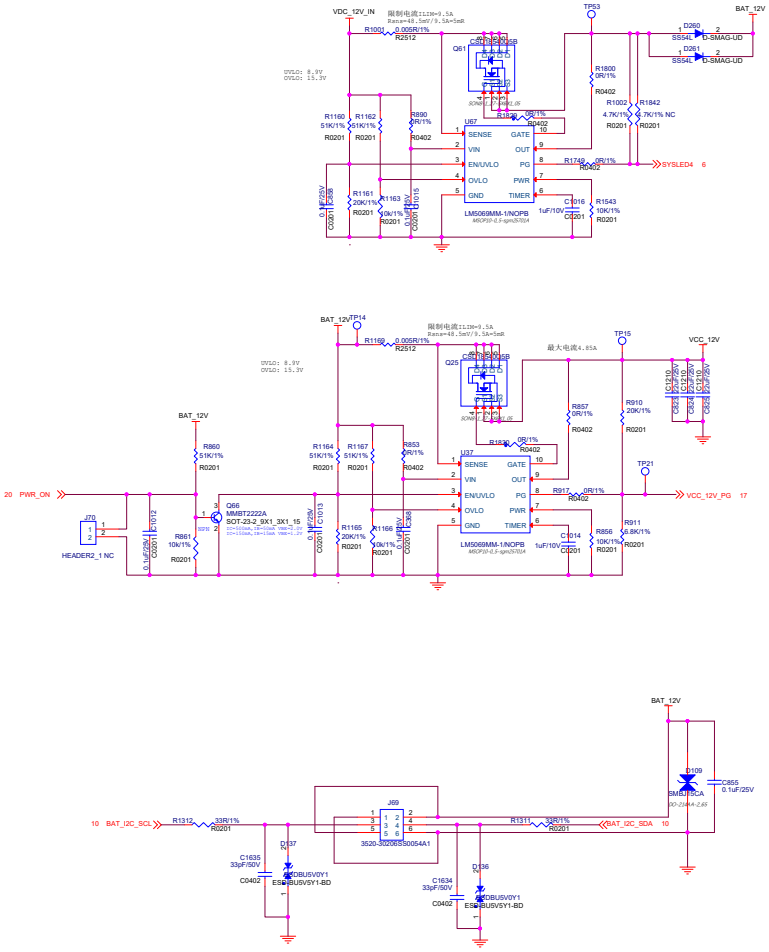




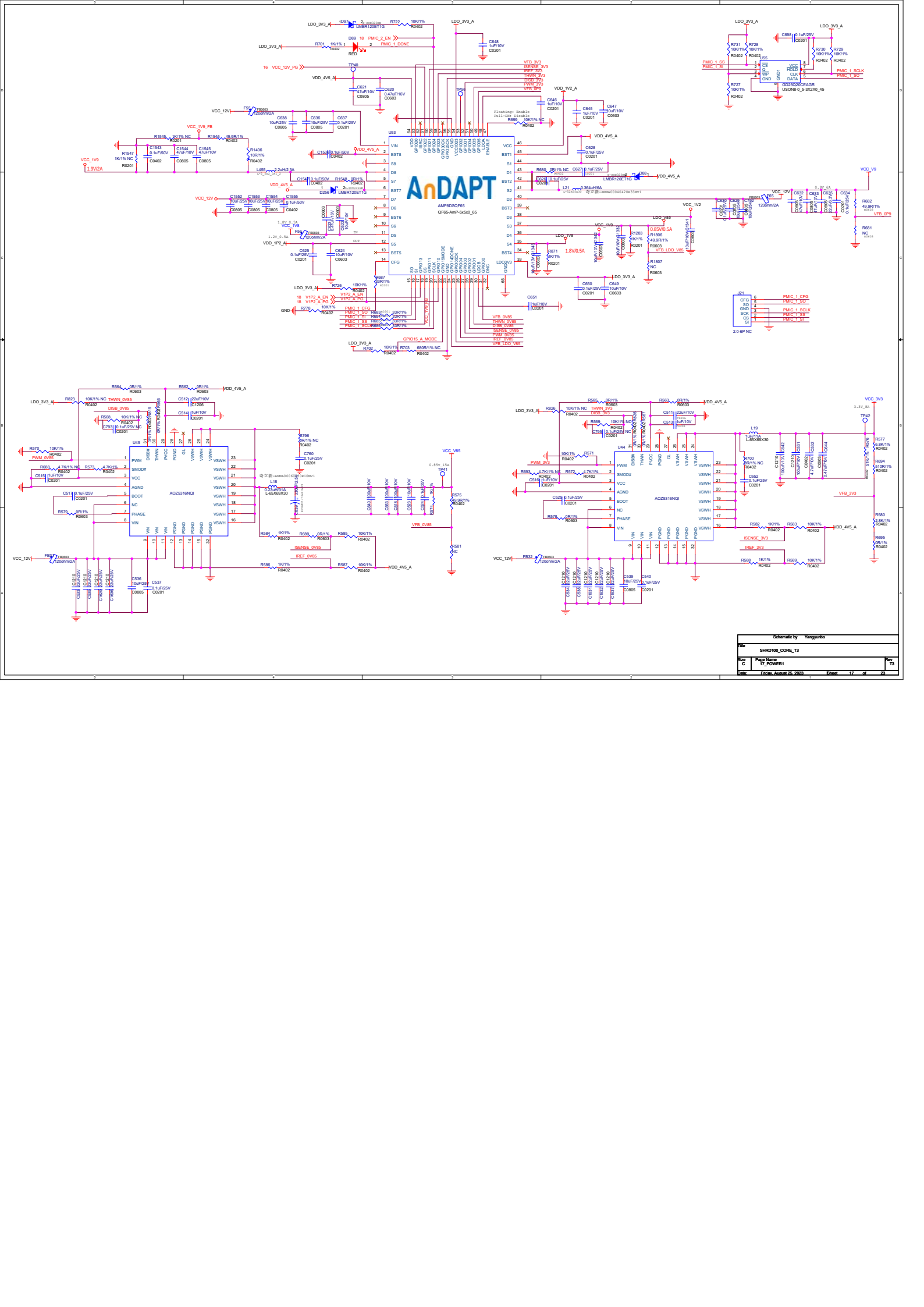




Schematic by	Yangyunbo	
Title	SHRD100_CORE_T3	
Size C	Page Name 15_FAN_GYRO	Rev T3
Date: Friday, August 25, 2023	Sheet 15 of 23	



Schematic by	Yangyunbo	
Title	SHRD100_CORE_T3	
Size C	Page Name 16_PWR_IN	Rev T3
Date: Friday, August 25, 2023	Sheet 16 of 23	


AnDAPT
AMP8DSGF65
QF65-AmP-5x5x0_65
LDO_3V3_A
VDD_4V5_A
VDD_1V2_A
VCC_12V
VCC_1V9
VCC_1V2
VCC_1V8
VCC_3V3
VCC_VB5
VDD_1P2_A
LDO_1V8
LDO_1V85
0.85V/0.5A
1.8V/0.5A
1.9V/2A
AOZ5316NQI
LMBR120ET1G
PMIC_1_SS
PMIC_1_SI
PMIC_1_SCLK
PMIC_1_SO
PMIC_1_CFG
VFB_LDO_V85
VFB_0V85
VFB_3V3
VFB_0P9
ISENSE_0V85
ISENSE_3V3
IREF_0V85
IREF_3V3
GPIO15_A_MODE
V1P2_A_EN
V1P2_A_PG
DISB_0V85
DISB_3V3
THWN_0V85
THWN_3V3
PWM_0V85
PWM_3V3
2.0-6P NC
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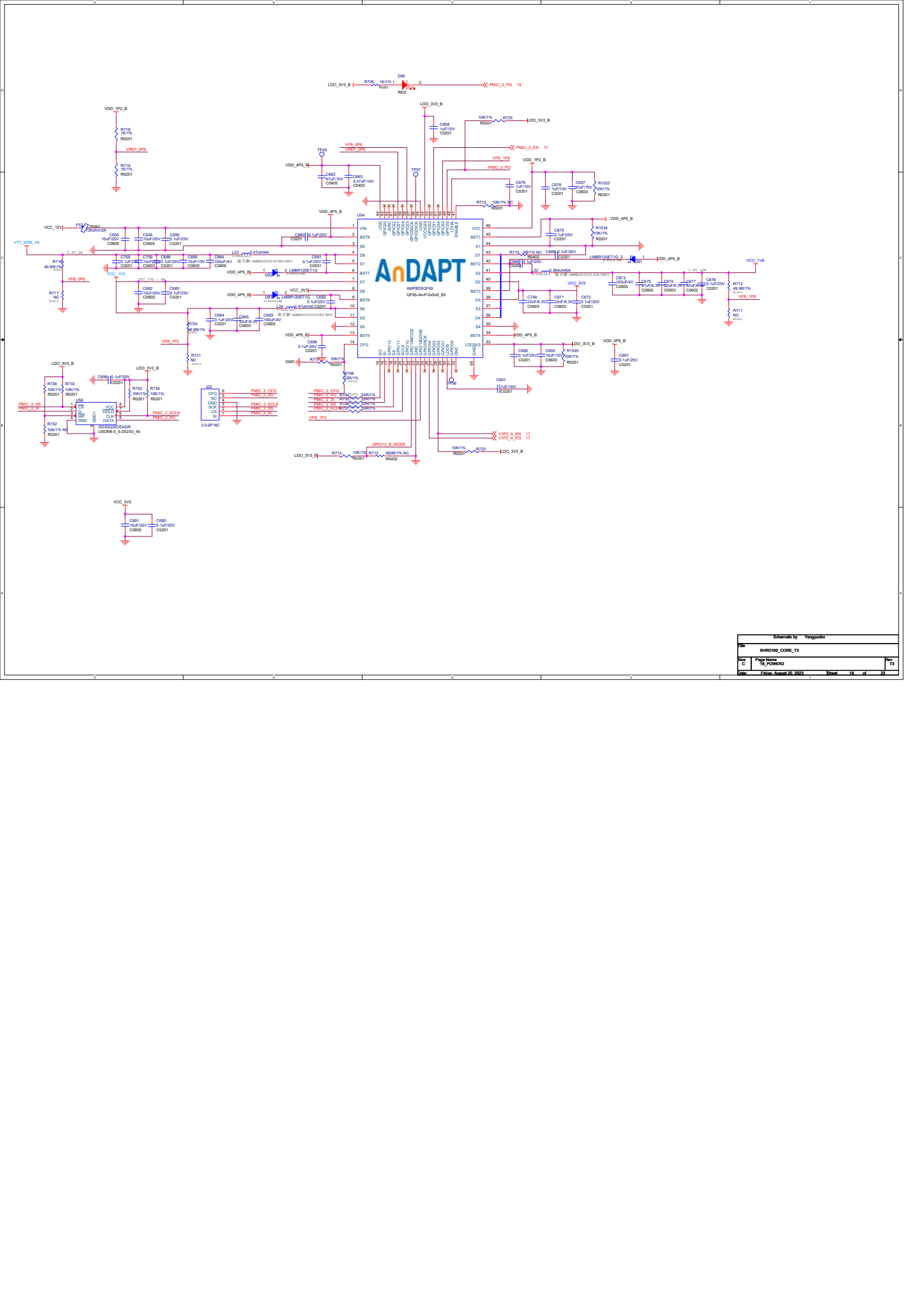
AnDAPT
AMP8DSQF65
QF65-AmP-5x5x0_65
LDO_3V3_B
VDD_1P2_B
VDD_4P5_B
VCC_3V3
VCC_1V8
VCC_12V
VTT_DDR_V6
VFB_0P6
VREF_0P6
VFB_1P8
VFB_1P2
PMIC_2_PG
PMIC_2_EN
PMIC_2_SS
PMIC_2_SI
PMIC_2_SCLK
PMIC_2_SO
PMIC_2_CFG
GPIO15_B_MODE
V1P2_A_EN
V1P2_A_PG
LMBR120ET1G
GD25Q20CEAGR
USON8-0_5-3X2X0_45
2.0-6P NC
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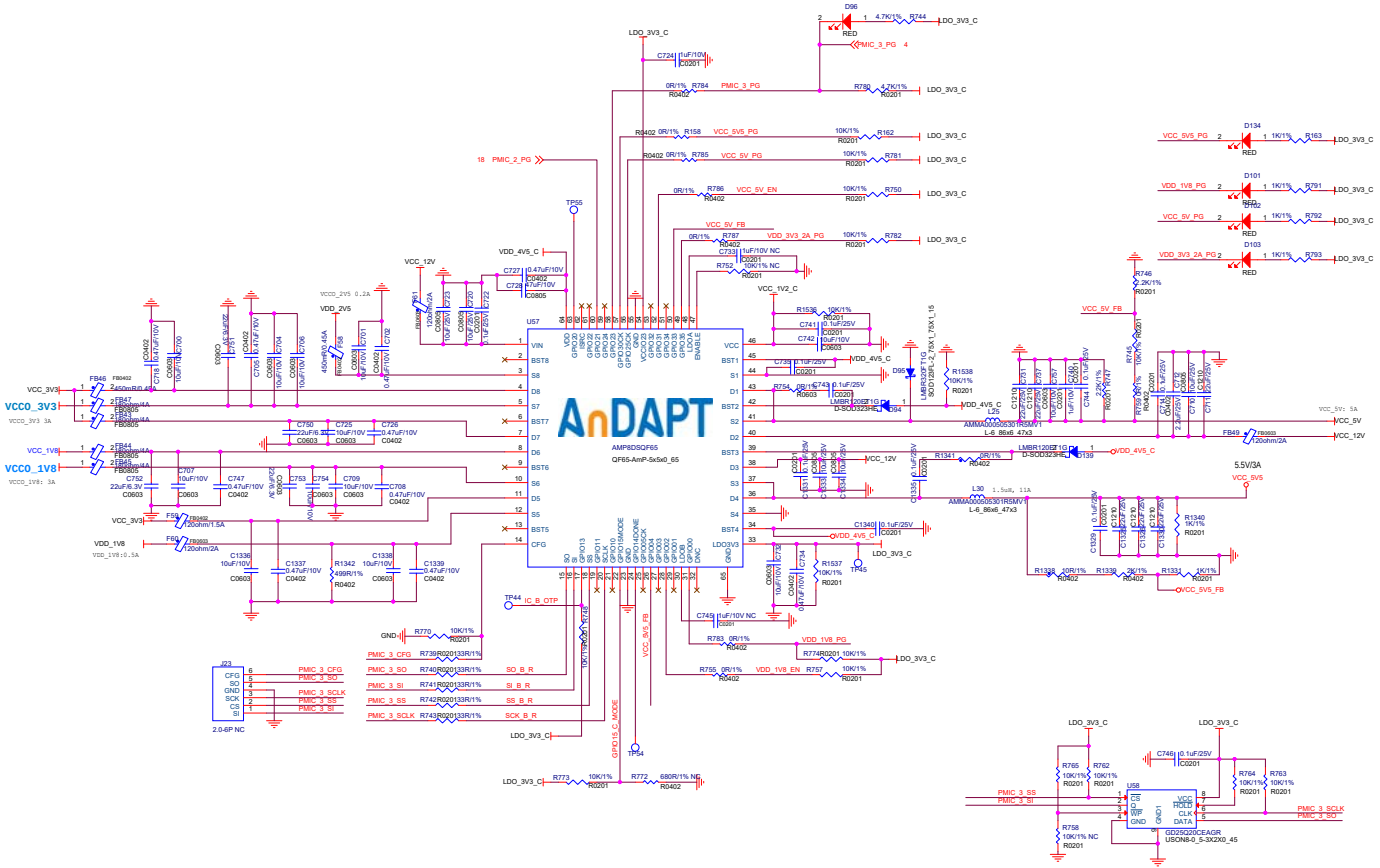

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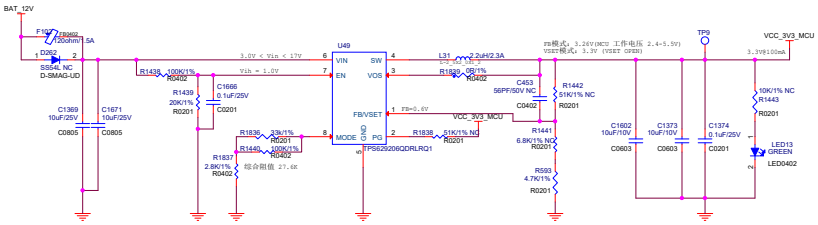
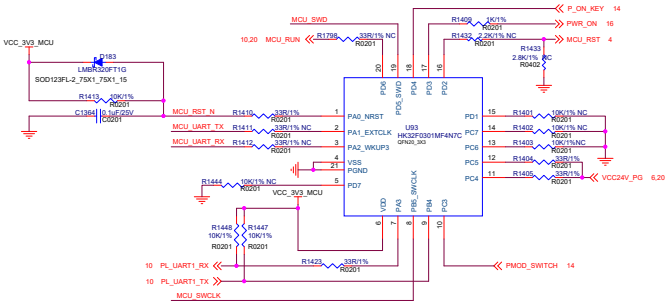
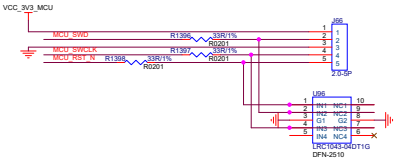
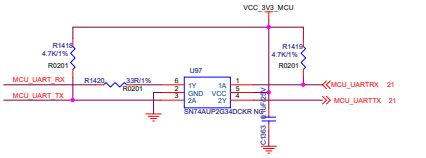


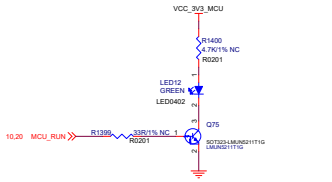
Table 8-1. Smart-CONFIG Setting Table

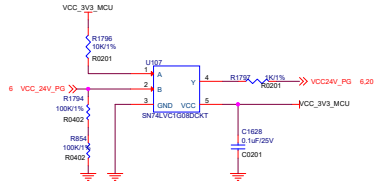
#	M ODE/S-CONF Level Or Resistor Value [Ω] (1)	FB/VSET Pin	F_{sw} (MHz)	Output Discharge	Mode (Auto Or Forced PWM)	Dynamic Mode Change
	Setting Options by Level					
1	GND	external FB	up to 2.5(2)	yes	Auto PFM/PWM with AEE	Active
2	HIGH (> 1.8 V)	external FB	2.5	yes	Forced PWM	
	Setting Options by Resistor					
3	7.50 k	external FB	up to 2.5(2)	no	Auto PFM/PWM with AEE	not active
4	9.31 k	external FB	2.5	no	Forced PWM	
5	11.50 k	external FB	1	yes	Auto PFM/PWM	
6	14.30 k	external FB	1	yes	Forced PWM	
7	17.80 k	external FB	1	no	Auto PFM/PWM	
8	22.10 k	external FB	1	no	Forced PWM	
9	27.40 k	VSET	up to 2.5(2)	yes	Auto PFM/PWM with AEE	
10	34.00 k	VSET	2.5	yes	Forced PWM	
11	42.20 k	VSET	up to 2.5(2)	no	Auto PFM/PWM with AEE	
12	52.30 k	VSET	2.5	no	Forced PWM	
13	64.90 k	VSET	1	yes	Auto PFM/PWM	
14	80.60 k	VSET	1	yes	Forced PWM	
15	100.00 k	VSET	1	no	Auto PFM/PWM	
16	124.00 k	VSET	1	no	Forced PWM	











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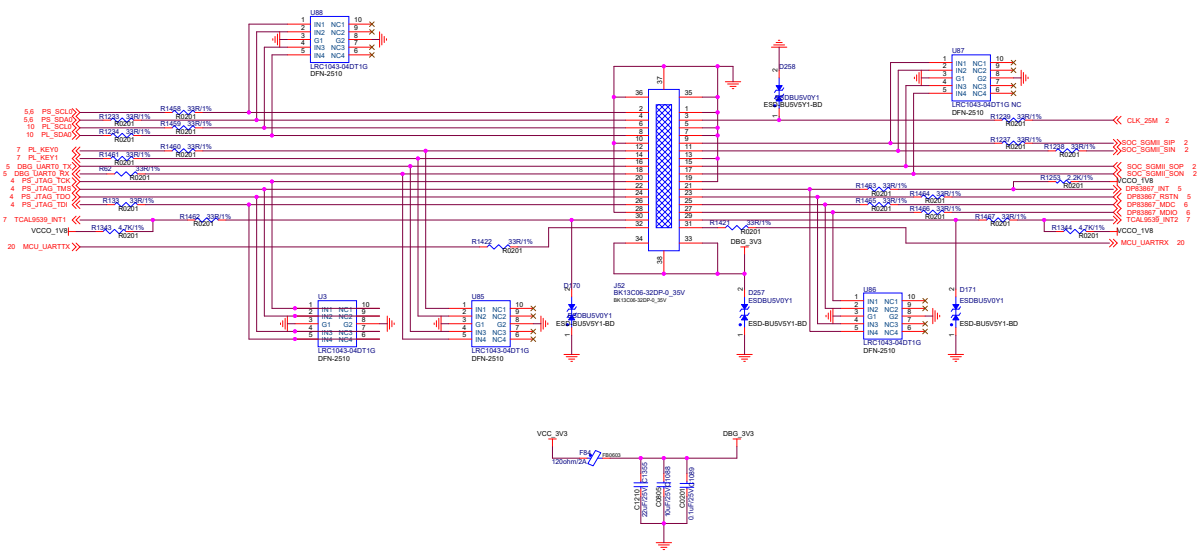

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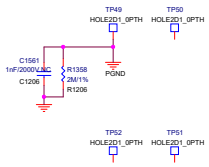
板上的螺钉通孔，
内直径2.1mm。



SMD 线夹

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本版在 SHRD100_CORE_T2 基础上，主要修改点如下：
1、外部天线端口分出 1 路到射频模块，用于频谱侦测；
2、保留一个螺钉孔接保护地；
3、增加射频保护电路；
4、修正 T2 版本的 BUG：DC 电源与BAT电源之间增加防反灌二极管等；

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