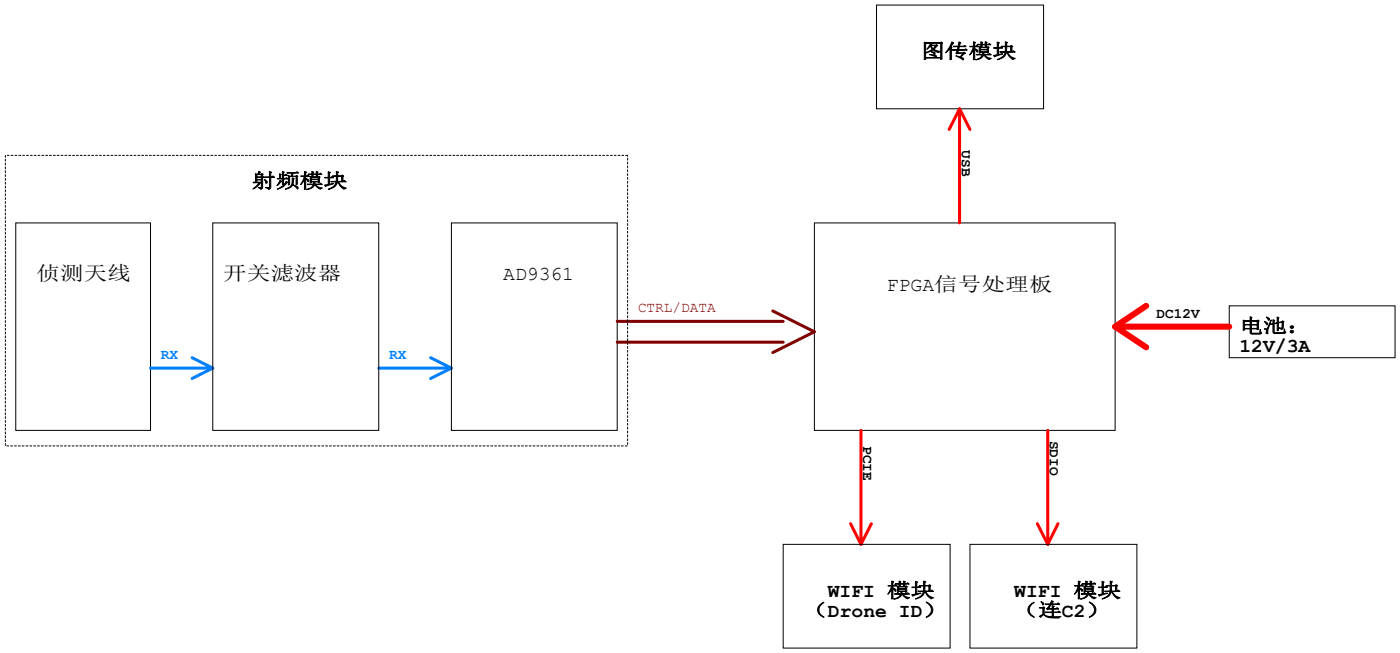
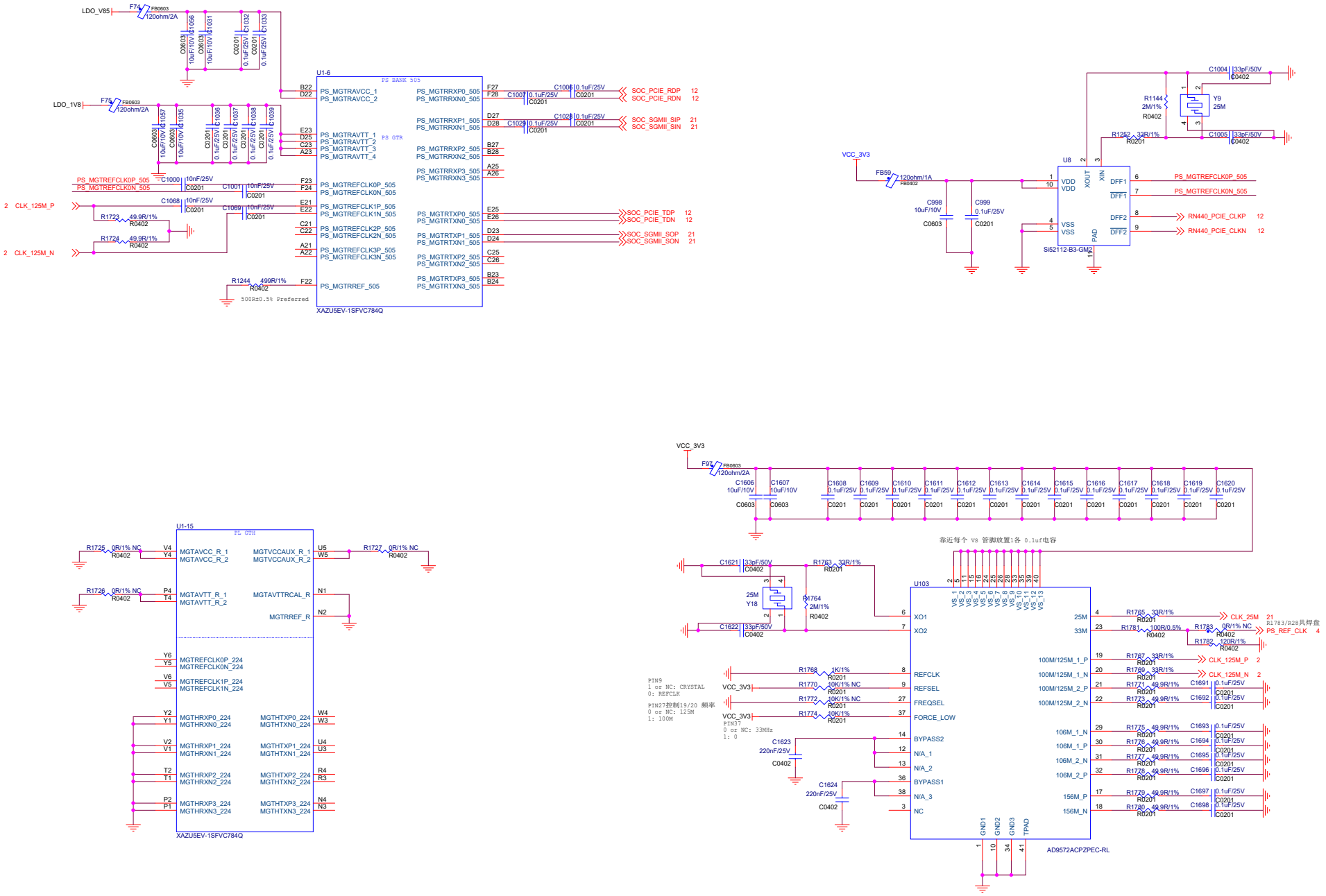
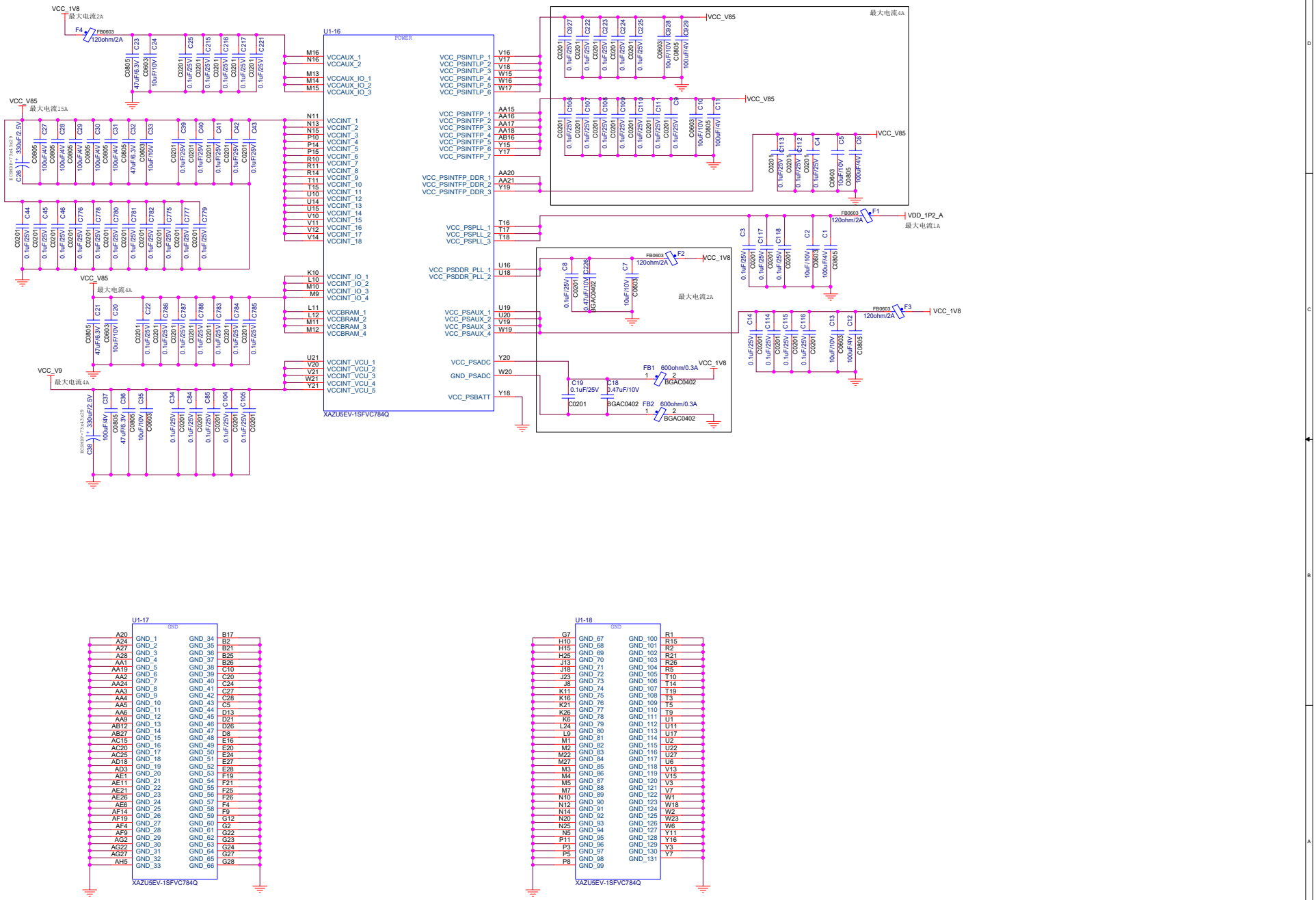
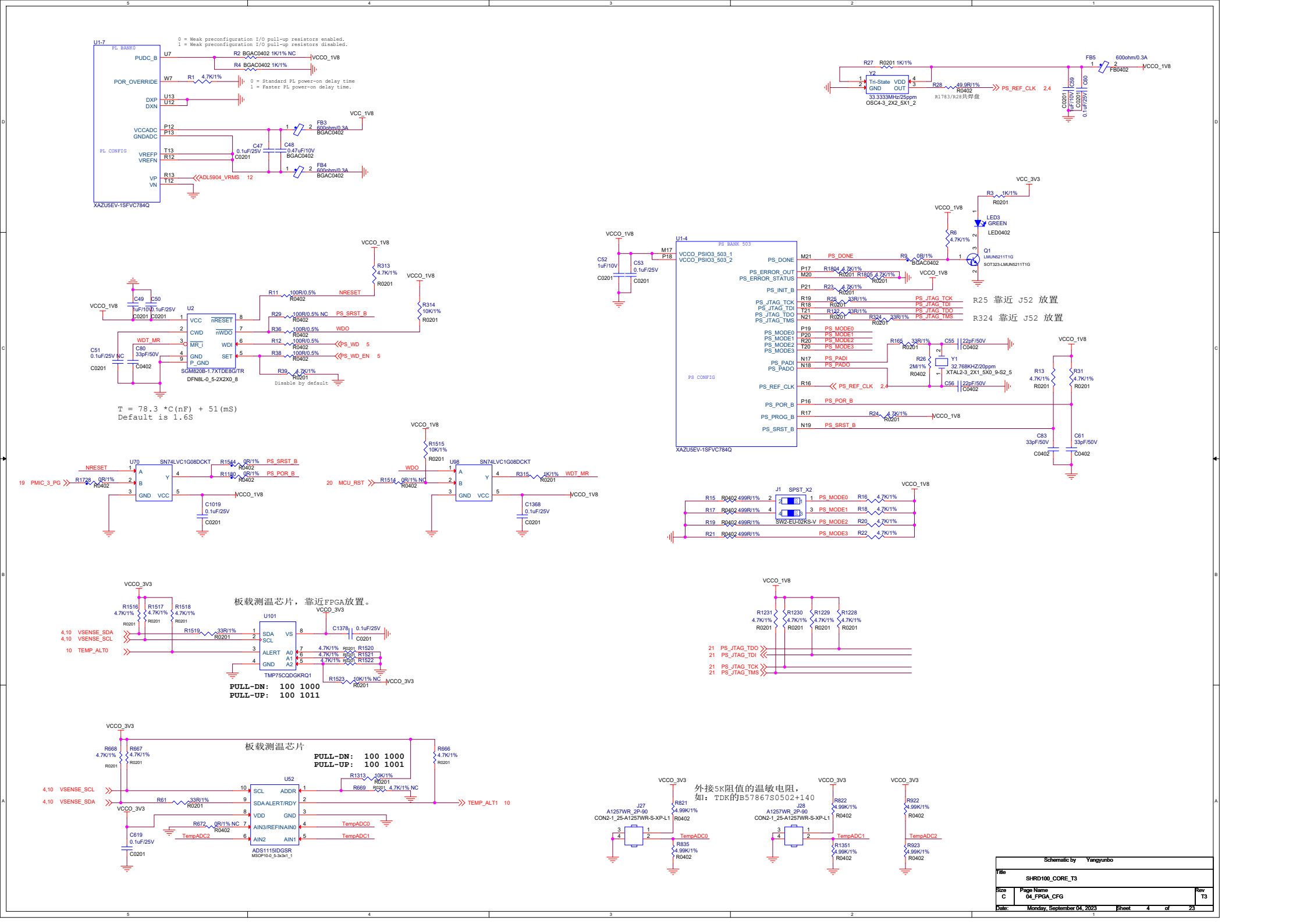


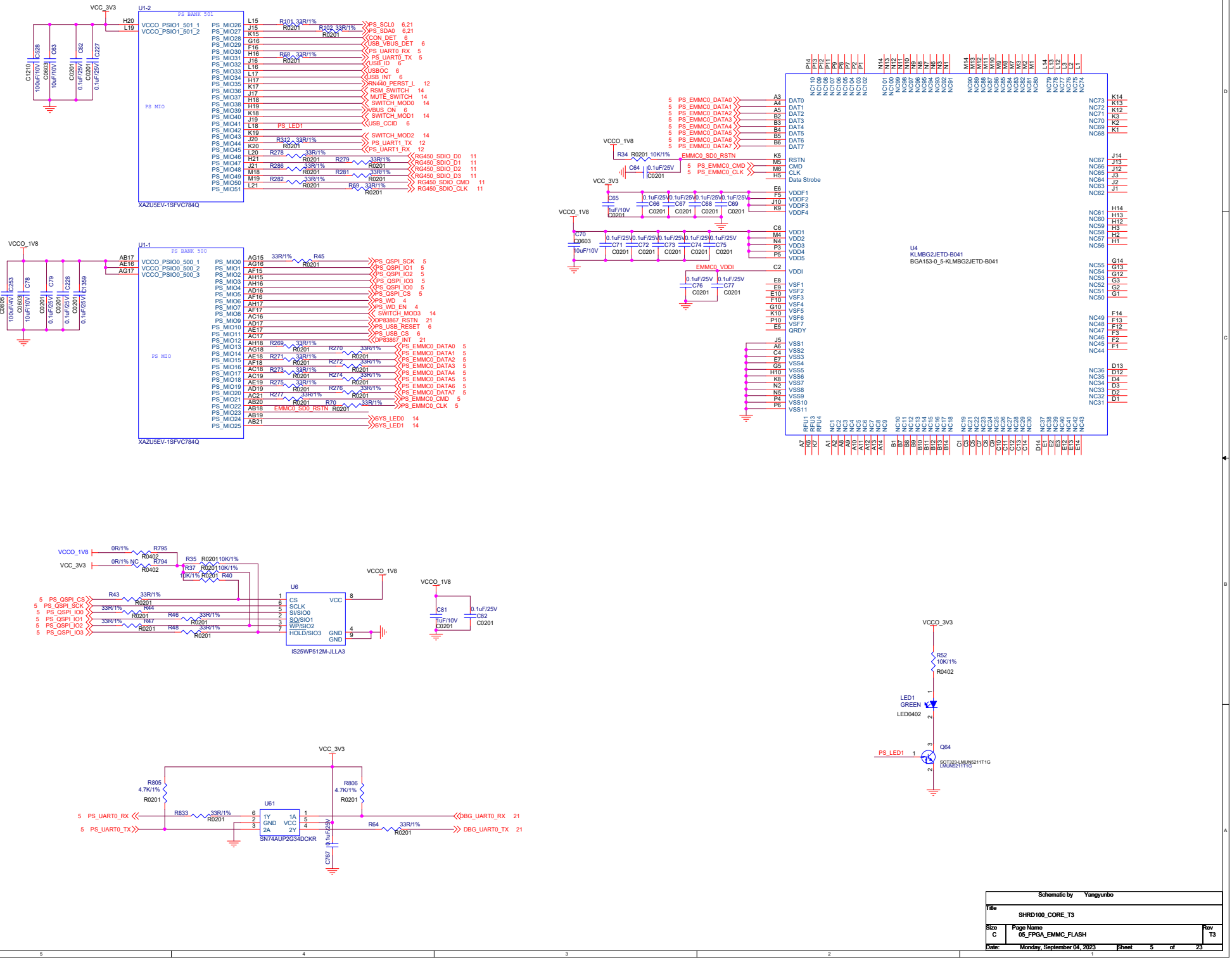
Schematic by	Yangyunbo	
Title	SHRD100_CORE_T3	
Size: C	Page Name: 01_System block	Rev: T3
Date: Monday, September 04, 2023	Sheet 1 of 23	


LDO_V85
LDO_1V8
U1-6
PS BANK 505
PS GTR
XAZU5EV-1SFVC784Q
VCC_3V3
U8
Si52112-B3-GM2
U1-15
PL GTH
U103
AD9572ACPZPEC-RL
靠近每个 VS 管脚放置1各 0.1uf电容
Schematic by Yangyunbo
Title
SHRD100_CORE_T3
Size C
Page Name 02_FPGA_GTR
Rev T3
Date: Monday, September 04, 2023
Sheet 2 of 23



Schematic by	Yangyunbo		
Title	SHRD100_CORE_T3		
Size C	Page Name 03_FPGA_POWER		Rev T3
Date: Monday, September 04, 2023	Sheet 3	of 23	


U1-7
PL BANK0
0 = Weak preconfiguration I/O pull-up resistors enabled.
1 = Weak preconfiguration I/O pull-up resistors disabled.
PUDC_B
POR_OVERRIDE
0 = Standard PL power-on delay time
1 = Faster PL power-on delay time.
DXP
DXN
VCCADC
GNDADC
PL CONFIG
VREFP
VREFN
VP
VN
XAZU5EV-1SFVC784Q
VCC_1V8
VCCO_1V8
VCCO_3V3
U2
SGM820B-1.7XTDE8G/TR
DFN8L-0_5-2X2X0_8
T = 78.3 *C(nF) + 51(mS)
Default is 1.6S
U70
SN74LVC1G08DCKT
U98
SN74LVC1G08DCKT
U1-4
PS BANK 503
PS CONFIG
XAZU5EV-1SFVC784Q
J1
SPST_X2
SW2-EU-02KS-V
Y1
XTAL2-3_2X1_5X0_9-S2_5
Y2
OSC4-3_2X2_5X1_2
33.3333MHz/25ppm
R1783/R28共焊盘
LED3
GREEN
LED0402
Q1
LMUN5211T1G
SOT323-LMUN5211T1G
R25 靠近 J52 放置
R324 靠近 J52 放置
板载测温芯片，靠近FPGA放置。
U101
TMP75CQDGKRQ1
PULL-DN: 100 1000
PULL-UP: 100 1011
板载测温芯片
U52
ADS1115IDGSR
MSOP10-0_5-3x3x1_1
外接5K阻值的温敏电阻，
如：TDK的B57867S0502+140
J27
J28
A1257WR_2P-90
CON2-1_25-A1257WR-S-XP-L1
Schematic by Yangyunbo
Title
SHRD100_CORE_T3
Size C
Page Name 04_FPGA_CFG
Rev T3
Date: Monday, September 04, 2023
Sheet 4 of 23


U1-2
PS BANK 501
XAZU5EV-1SFVC784Q
U1-1
PS BANK 500
XAZU5EV-1SFVC784Q
U4
KLMBG2JETD-B041
BGA153-0_5-KLMBG2JETD-B041
U6
IS25WP512M-JLLA3
U61
SN74AUP2G34DCKR
Schematic by Yangyunbo
Title
SHRD100_CORE_T3
Size C
Page Name 05_FPGA_EMMC_FLASH
Rev T3
Date: Monday, September 04, 2023
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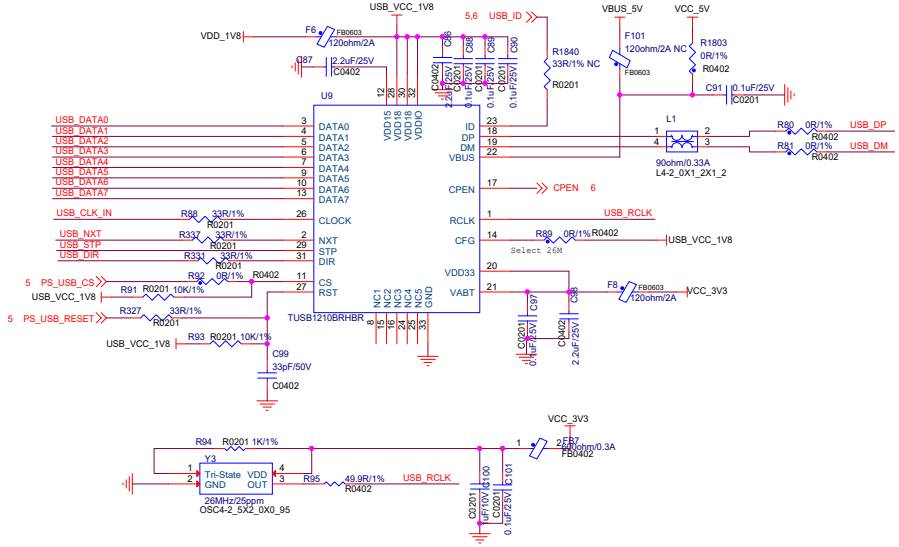
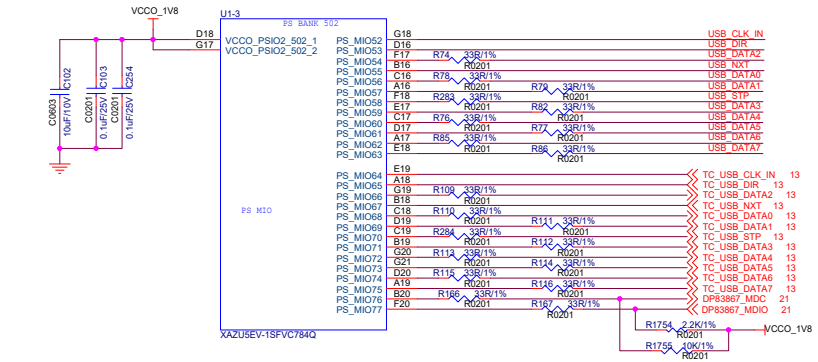
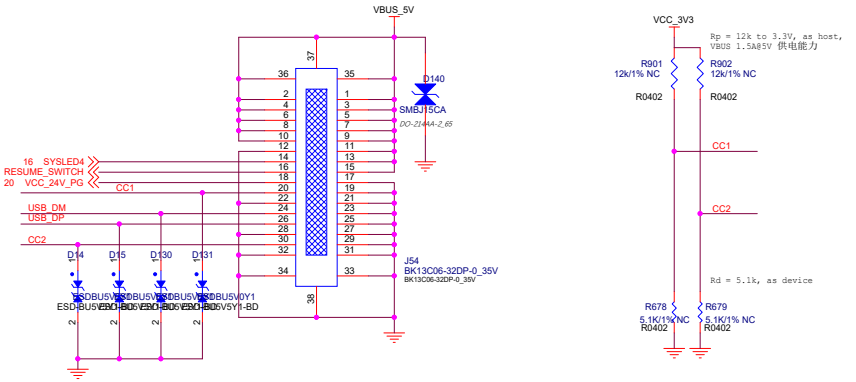
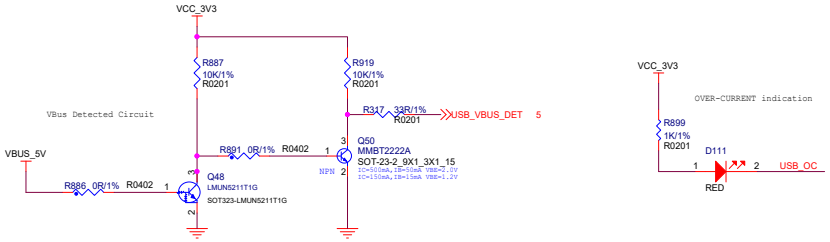
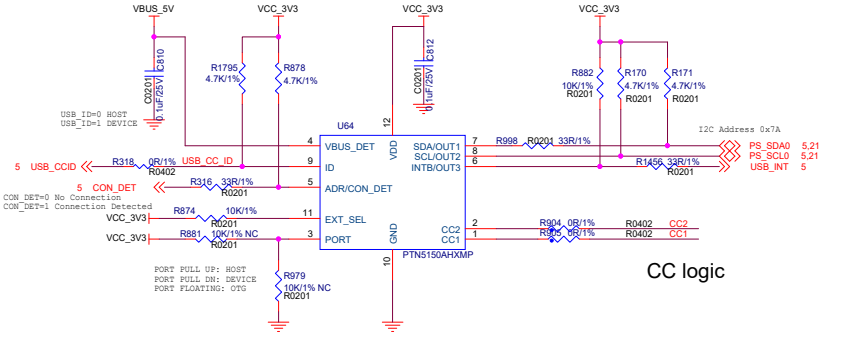


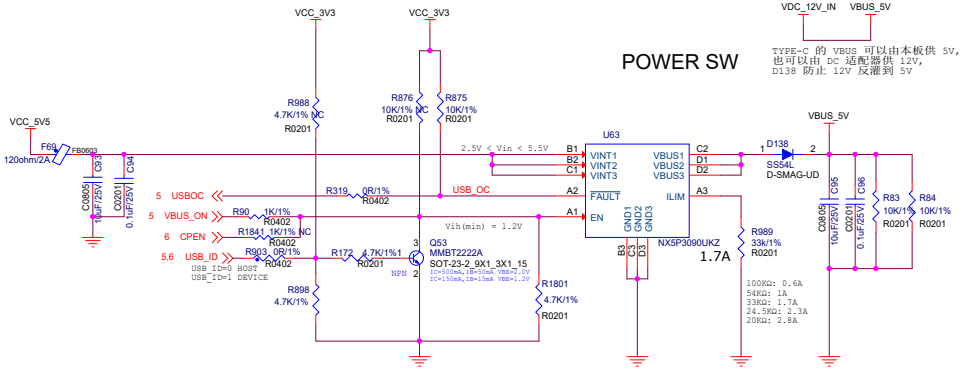




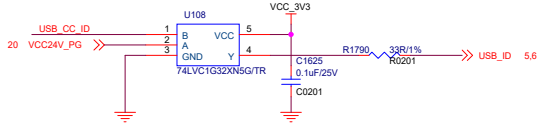




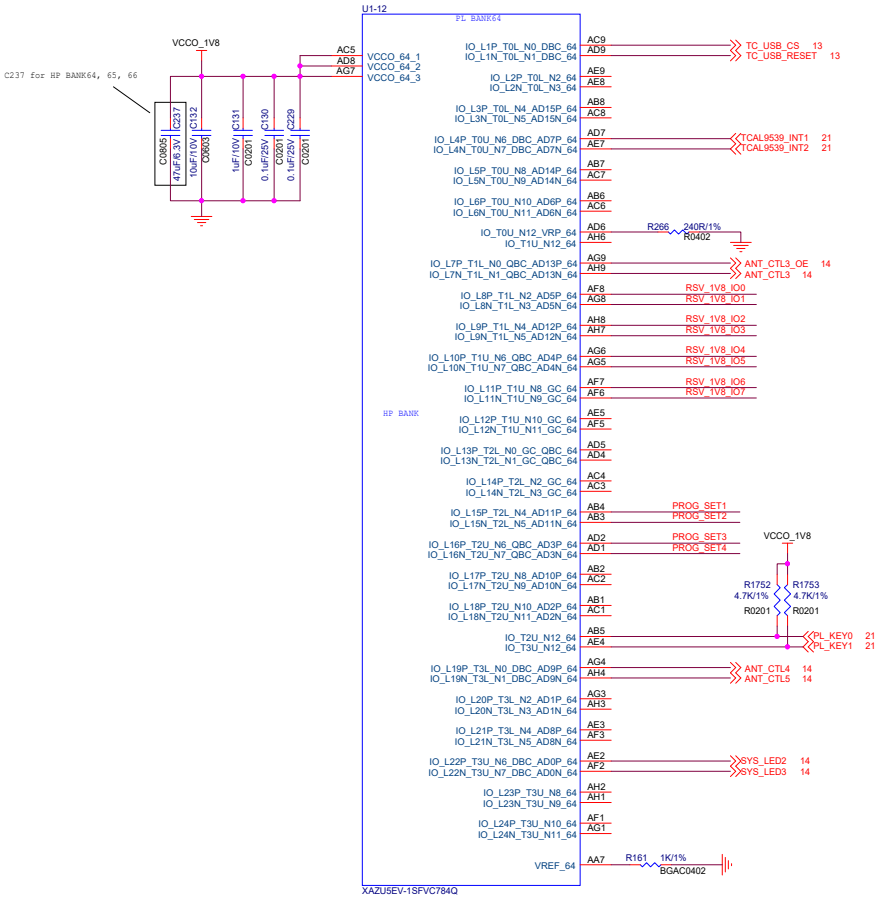
CC logic

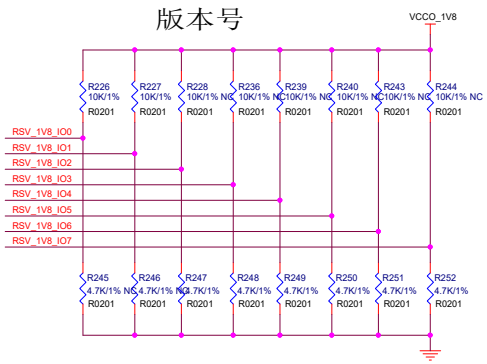


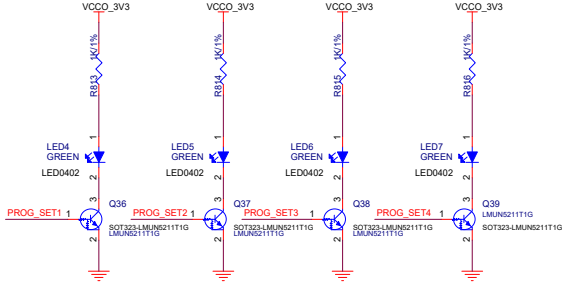
POWER SW



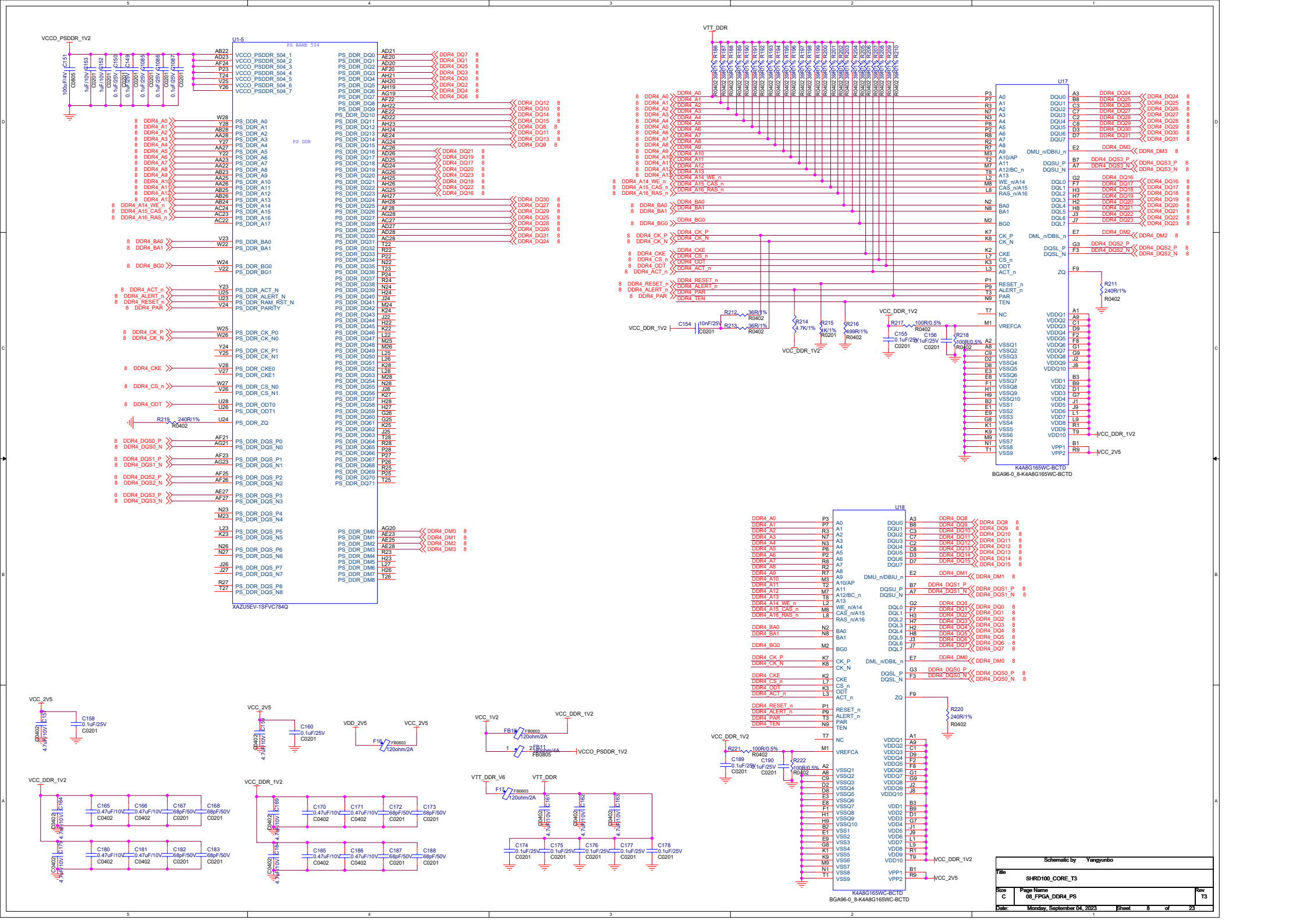
Schematic by	Yangyunbo	
Title	SHRD100_CORE_T3	
Size C	Page Name 06_FPGA_USB	Rev T3
Date: Monday, September 04, 2023	Sheet 6 of 23	







Schematic by	Yangyunbo	
Title	SHRD100_CORE_T3	
Size C	Page Name 07_FPGA_BANK64	Rev T3
Date: Monday, September 04, 2023	Sheet 7 of 23	


VCCO_PSDDR_1V2
U1-5
PS BANK 504
PS DDR
XAZU5EV-1SFVC784Q
VTT_DDR
U17
K4A8G165WC-BCTD
BGA96-0_8-K4A8G165WC-BCTD
U18
K4A8G165WC-BCTD
BGA96-0_8-K4A8G165WC-BCTD
VCC_DDR_1V2
VCC_2V5
VDD_2V5
VTT_DDR_V6
Schematic by Yangyunbo
Title
SHRD100_CORE_T3
Size C
Page Name 08_FPGA_DDR4_PS
Rev T3
Date: Monday, September 04, 2023
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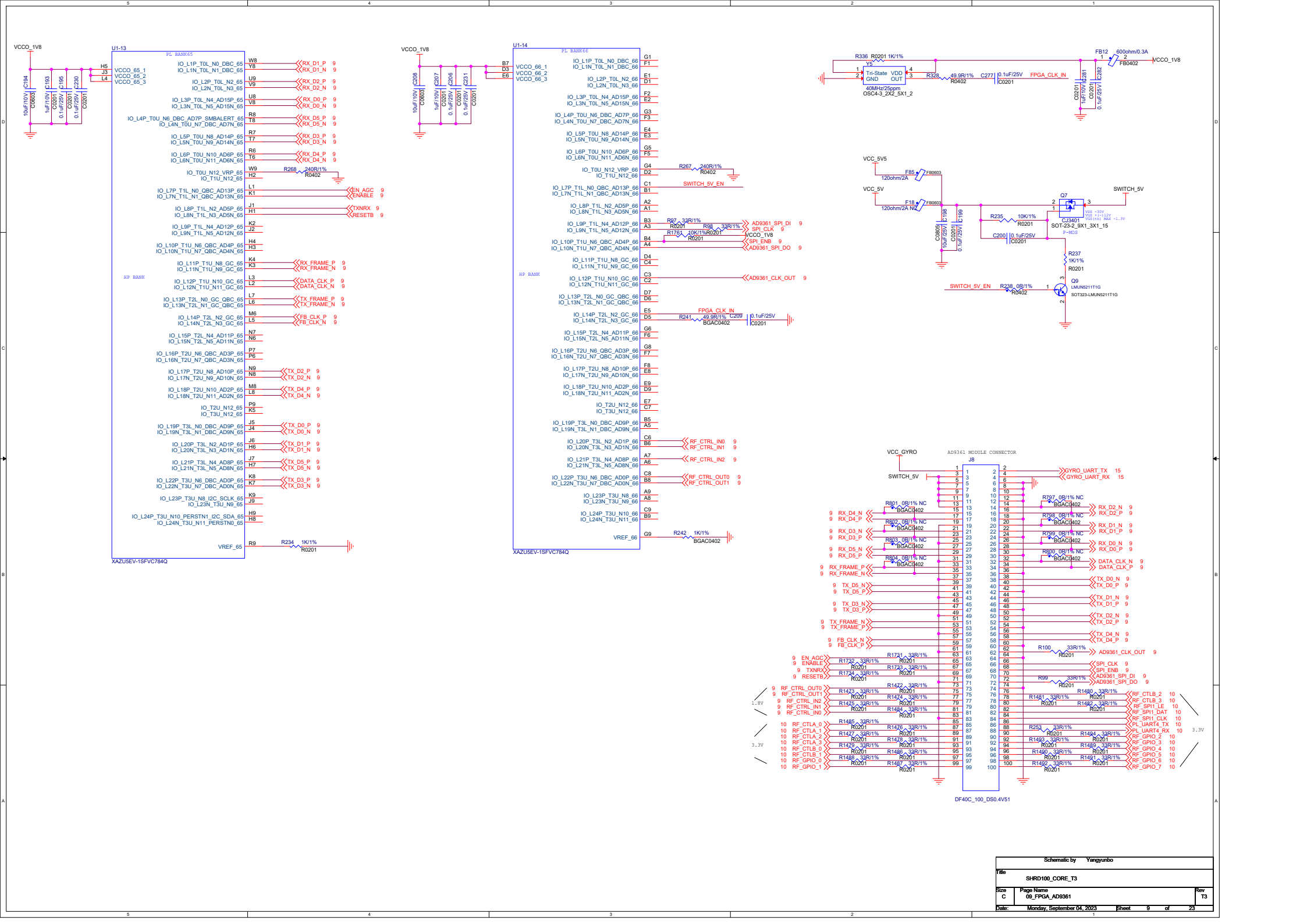

Schematic by	Yangyunbo
Title	SHRD100_CORE_T3
Size	C
Page Name	09_FPGA_AD9361
Rev	T3
Date:	Monday, September 04, 2023
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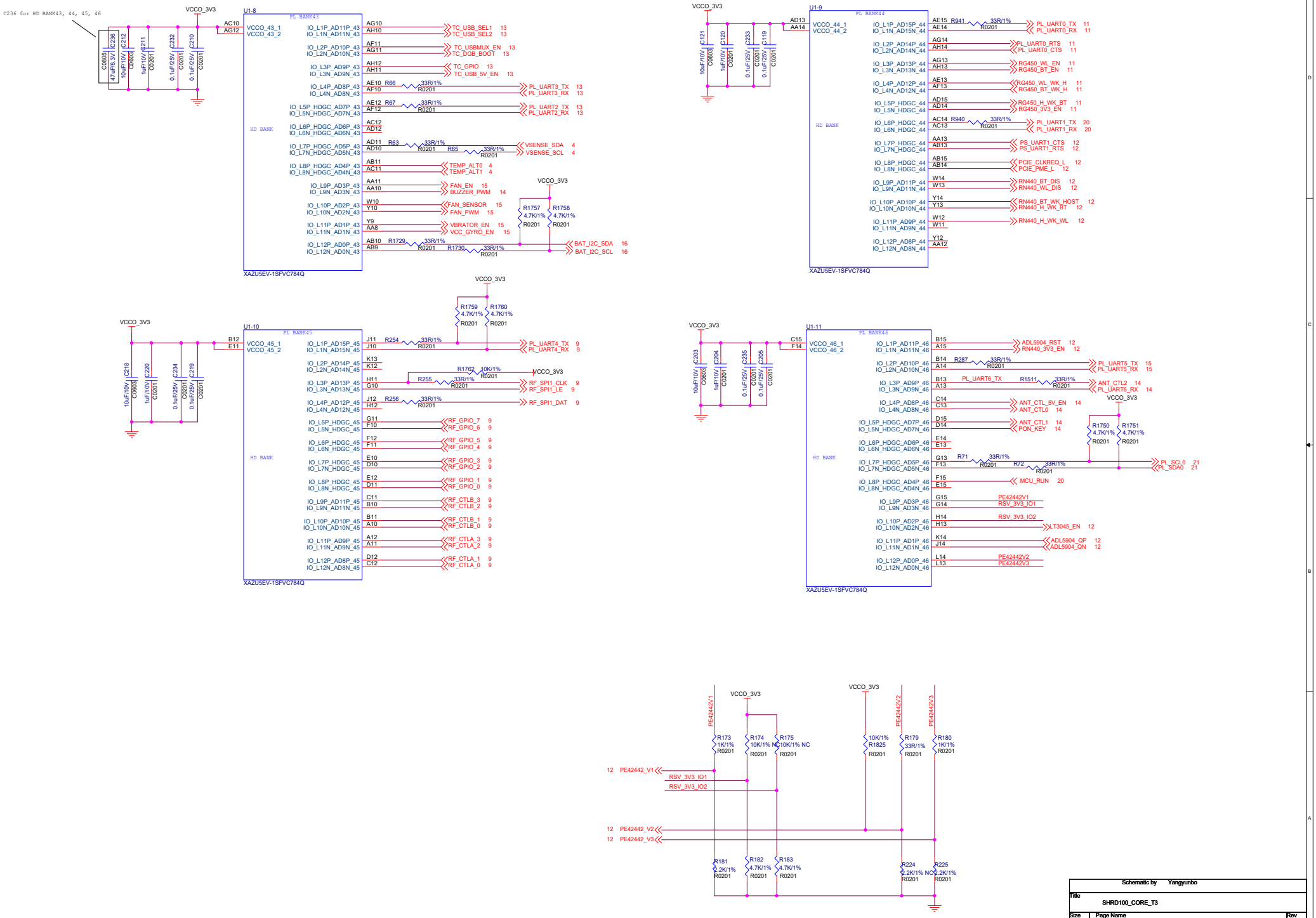
C236 for HD BANK43, 44, 45, 46
VCCO_3V3
U1-8
PL BANK43
HD BANK
XAZU5EV-1SFVC784Q
U1-9
PL BANK44
XAZU5EV-1SFVC784Q
U1-10
PL BANK45
XAZU5EV-1SFVC784Q
U1-11
PL BANK46
XAZU5EV-1SFVC784Q
PE42442V1
PE42442V2
PE42442V3
RSV_3V3_IO1
RSV_3V3_IO2
Schematic by Yangyunbo
Title SHRD100_CORE_T3
Size C
Page Name 10_FPGA_HD_BANK
Rev T3
Date: Monday, September 04, 2023
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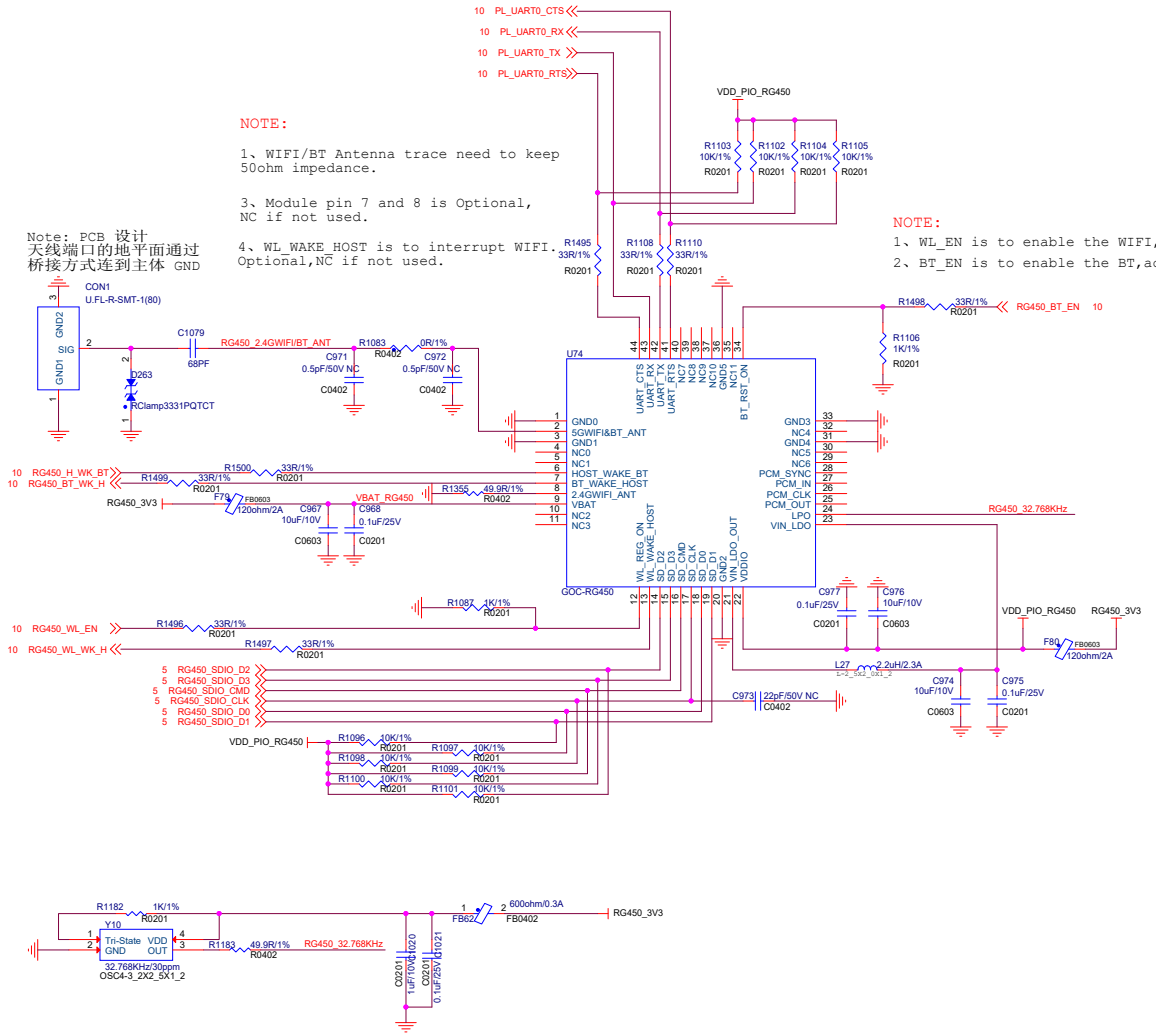
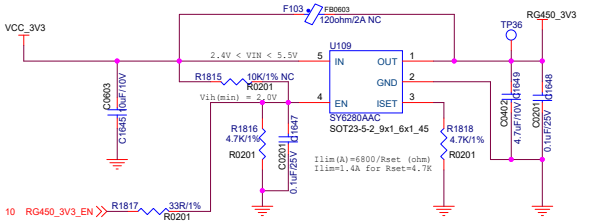


UART Connection between Module and Host.

Host	Module
UART_TX	UART_RX
UART_RX	UART_TX
UART_CTS	UART_RTS
UART_RTS	UART_CTS

PCM Connection between Module and Host.

Host	Module
PCM_CLK	PCM_CLK
PCM_SYNC	PCM_SYNC
PCM_IN	PCM_OUT
PCM_OUT	PCM_IN



SDIO NOTE:

1、Trace total length < 4000mils, and six signals trace length difference <300mils.
2、Add damping resistor.
3、SDIO signals do not allow crossed over and overlapped.
4、CLK signals should keep well ground.
5、The less changing the PCB layer the better.

Power and LPO Note:

1.This module requires two sets of power supply VDD_3.3V and VDD_PIO. Independent power supply is recommended.The power ripple is less than 80 mV. Current for power supply :

Power input	Current	Power Ripple
VDD_PIO	150mA	Less than 80mV
VDD_3.3V	200-350mA(TYP.);700mA(MAX.)	Less than 80mV

2、VDD_PIO support 1.8V or 3.3V.It mainly depends on the voltage supported by I/O on host side.

3、EXT_LPO(32.768KHz) is Optional,NC if not used.

Schematic by	Yangyunbo		
Title	SHRD100_CORE_T3		
Size C	Page Name 11_GOC-RG450		Rev T3
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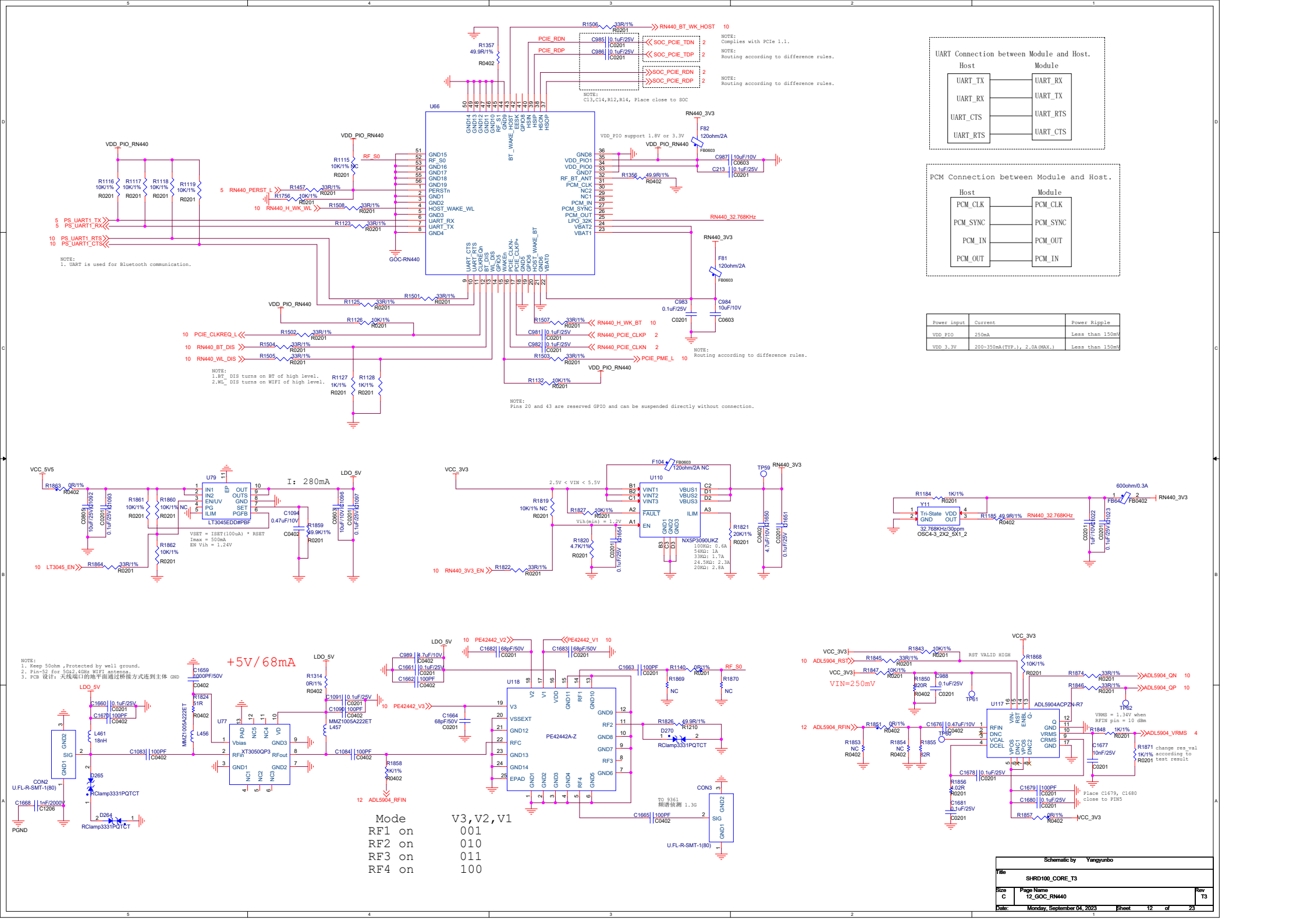

Power input	Current	Power Ripple
VDD_PIO	250mA	Less than 150mV
VDD_3.3V	200-350mA(TYP.), 2.0A(MAX.)	Less than 150mV

Schematic by	Yangyunbo
Title	SHRD100_CORE_T3
Size	C
Page Name	12_GOC_RN440
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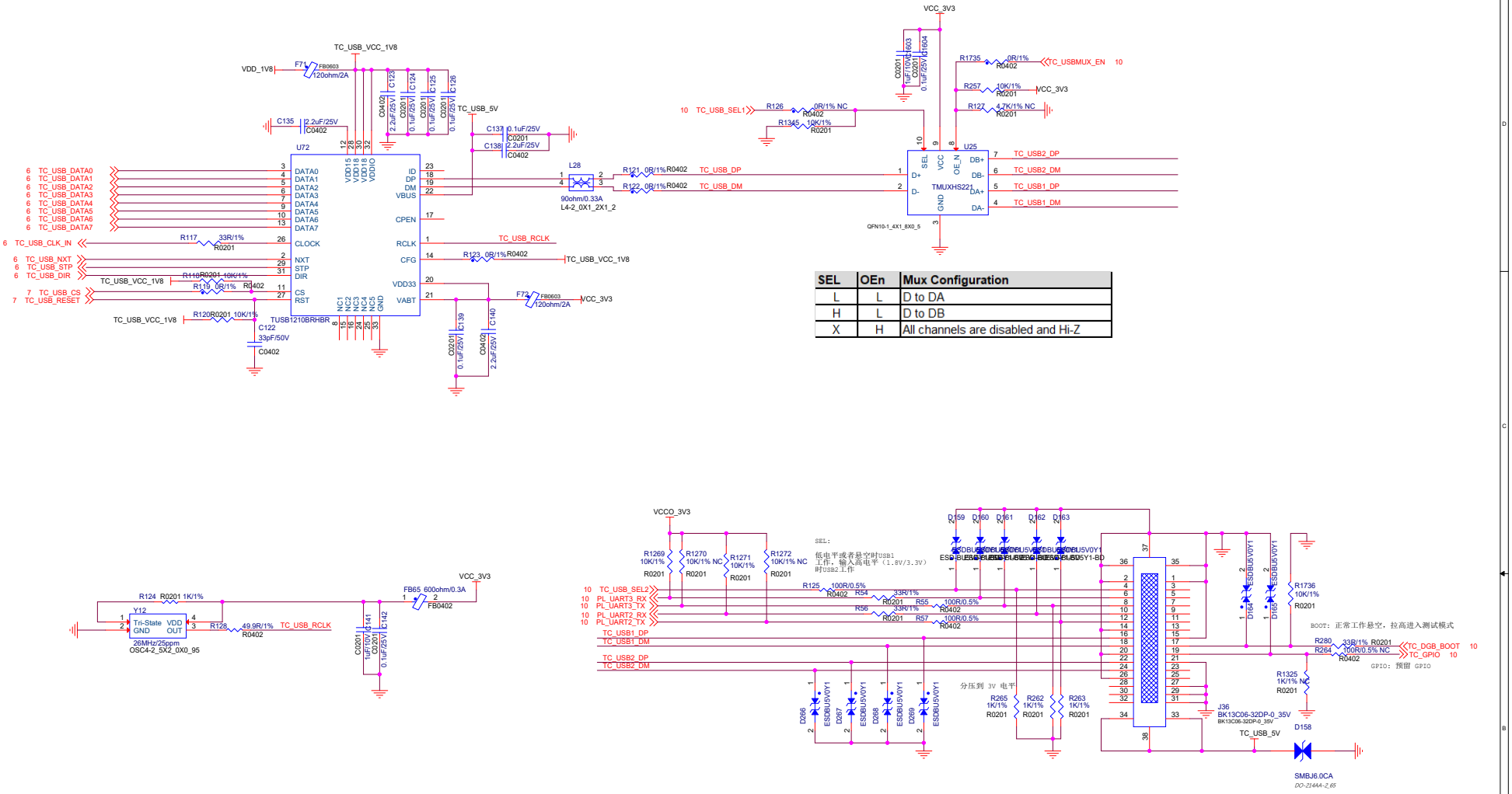
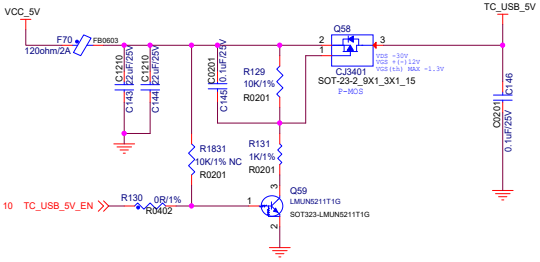
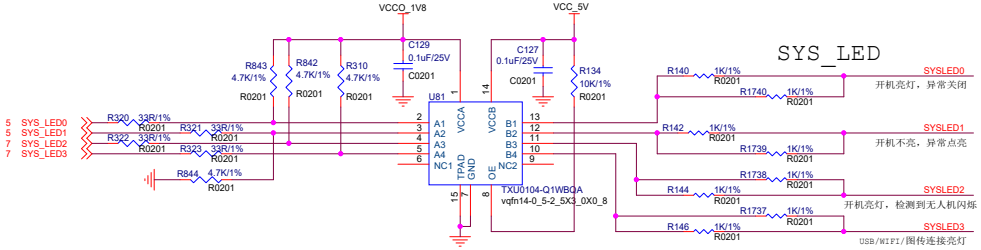
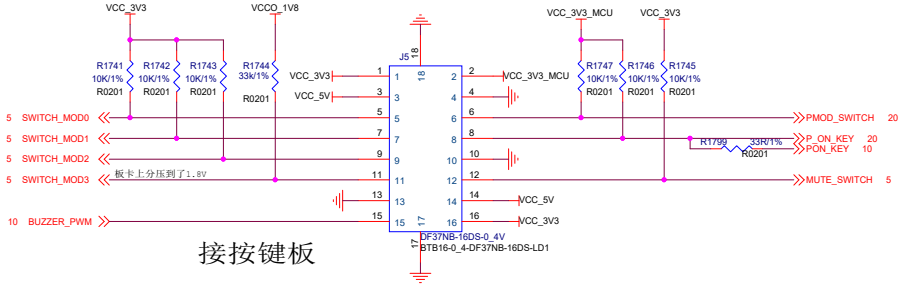


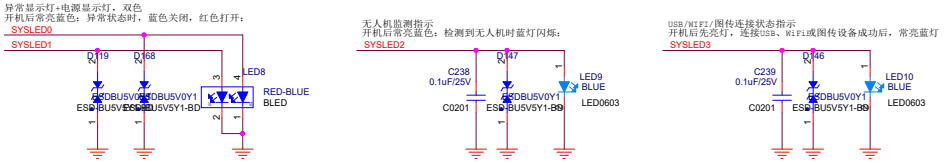
SEL	OEn	Mux Configuration
L	L	D to DA
H	L	D to DB
X	H	All channels are disabled and Hi-Z

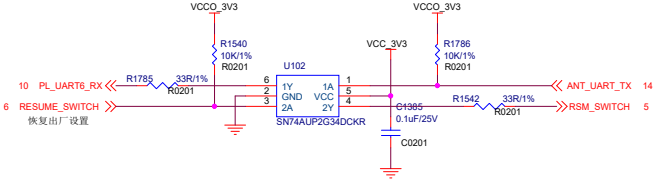


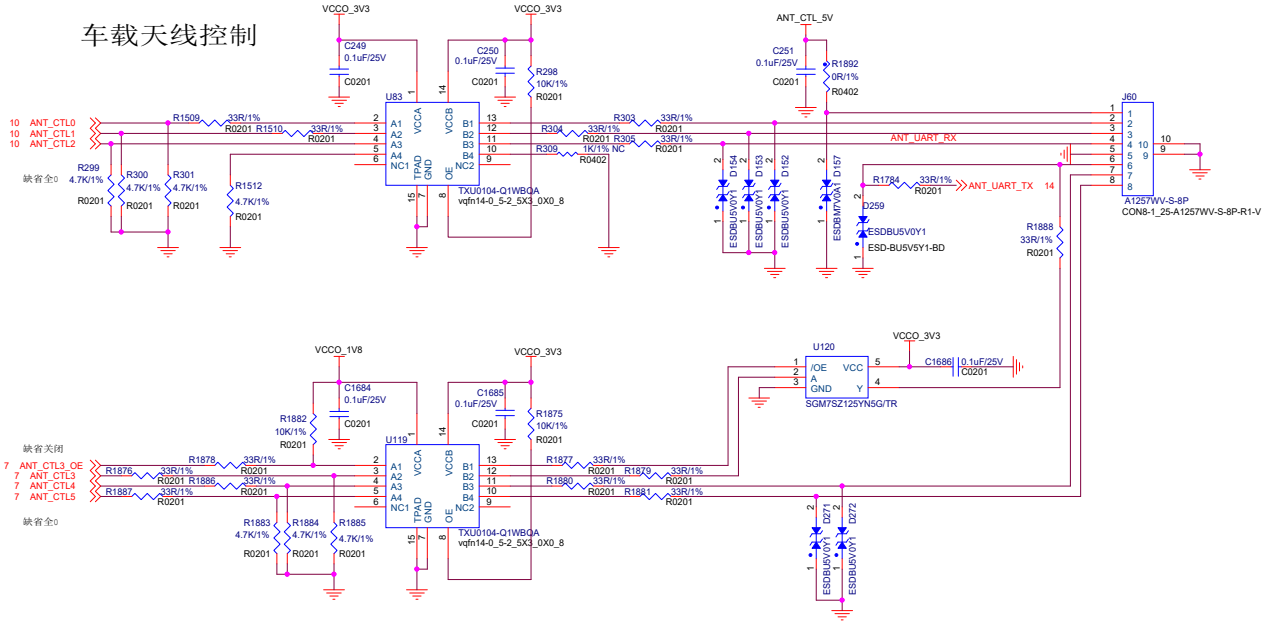
Schematic by	Yangyunbo		
Title	SHRD100_CORE_T3		
Size C	Page Name 13_IMG_TRANSMISSION		Rev T3
Date:	Monday, September 04, 2023	Sheet 13 of 23	

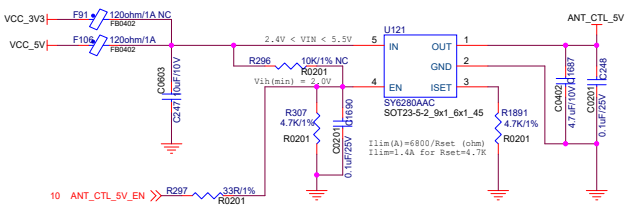












Schematic by	Yangyunbo	
Title	SHRD100_CORE_T3	
Size C	Page Name 14_USR_INTERFACE	Rev T3
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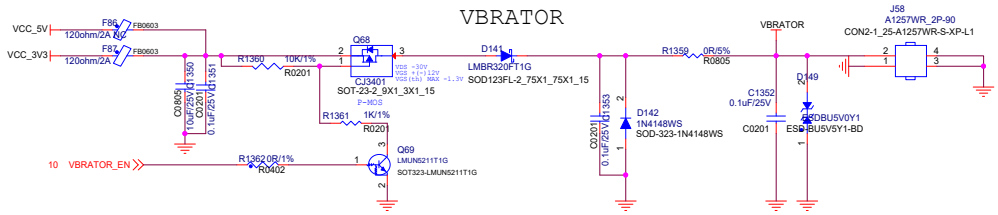
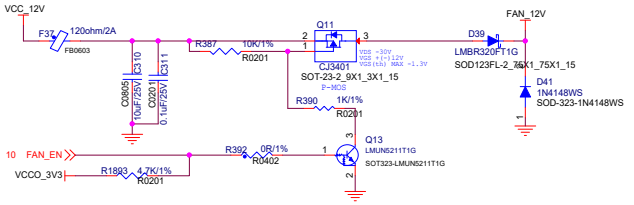
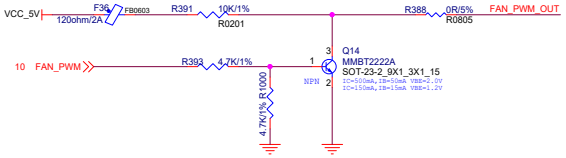
VBRATOR

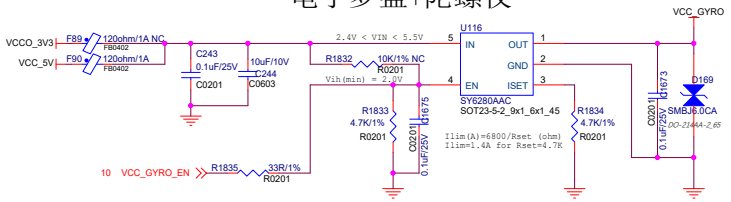


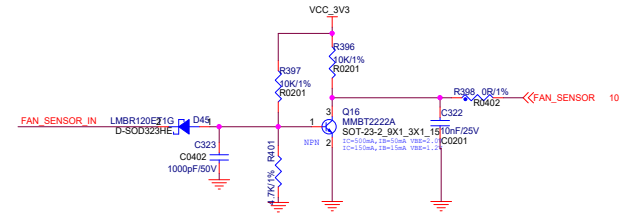
FAN

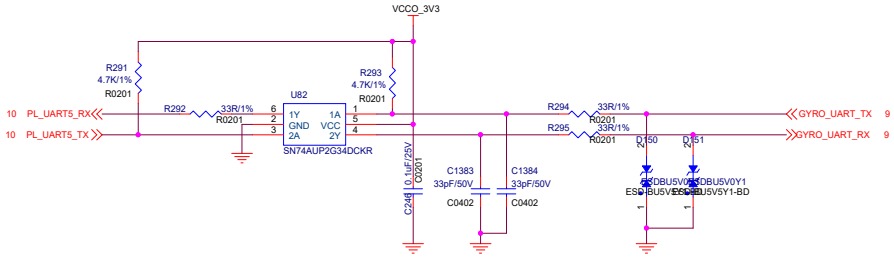


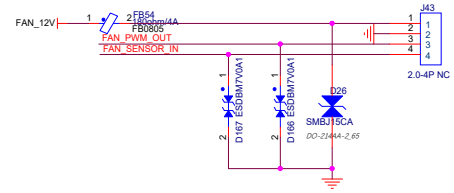


电子罗盘+陀螺仪

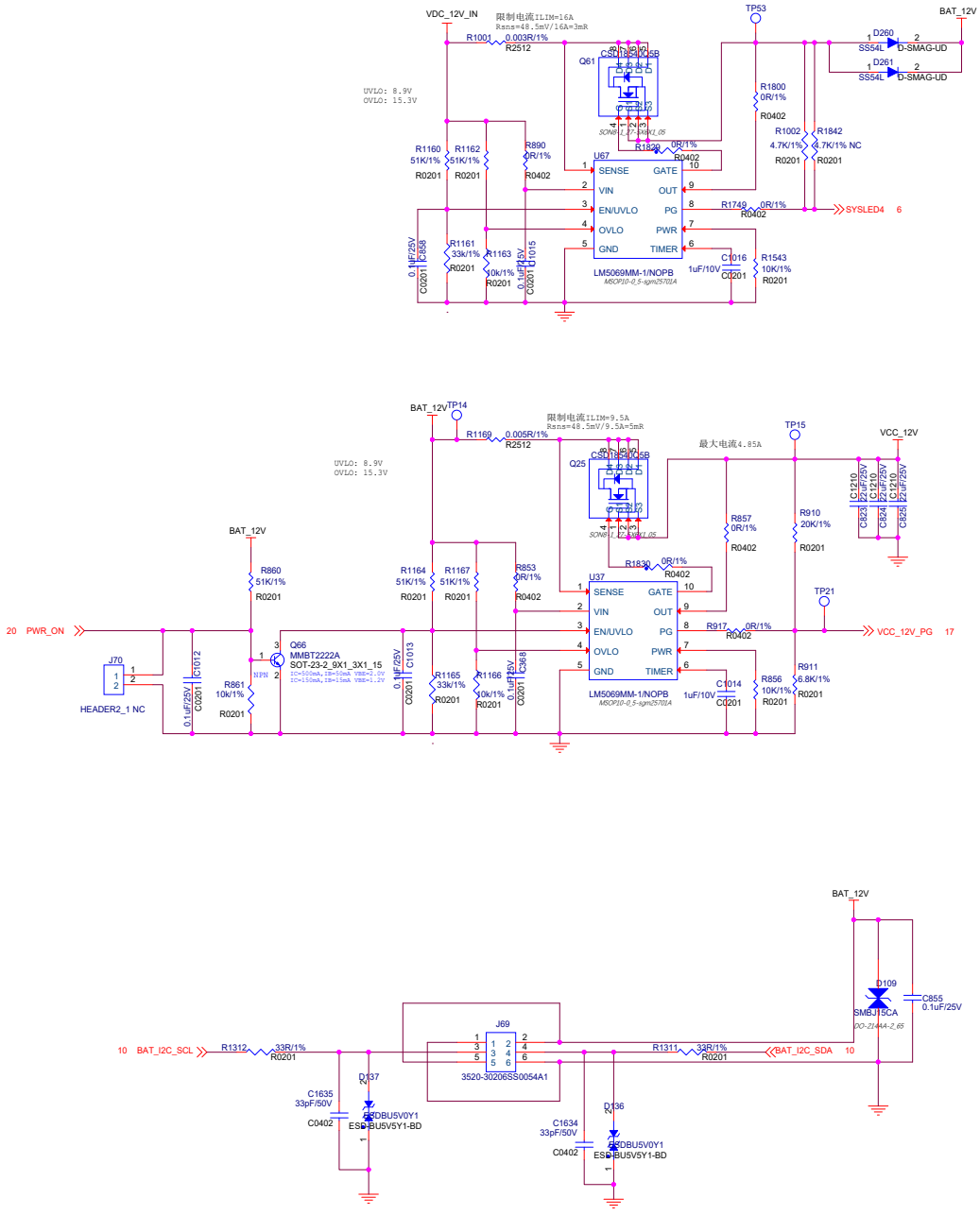




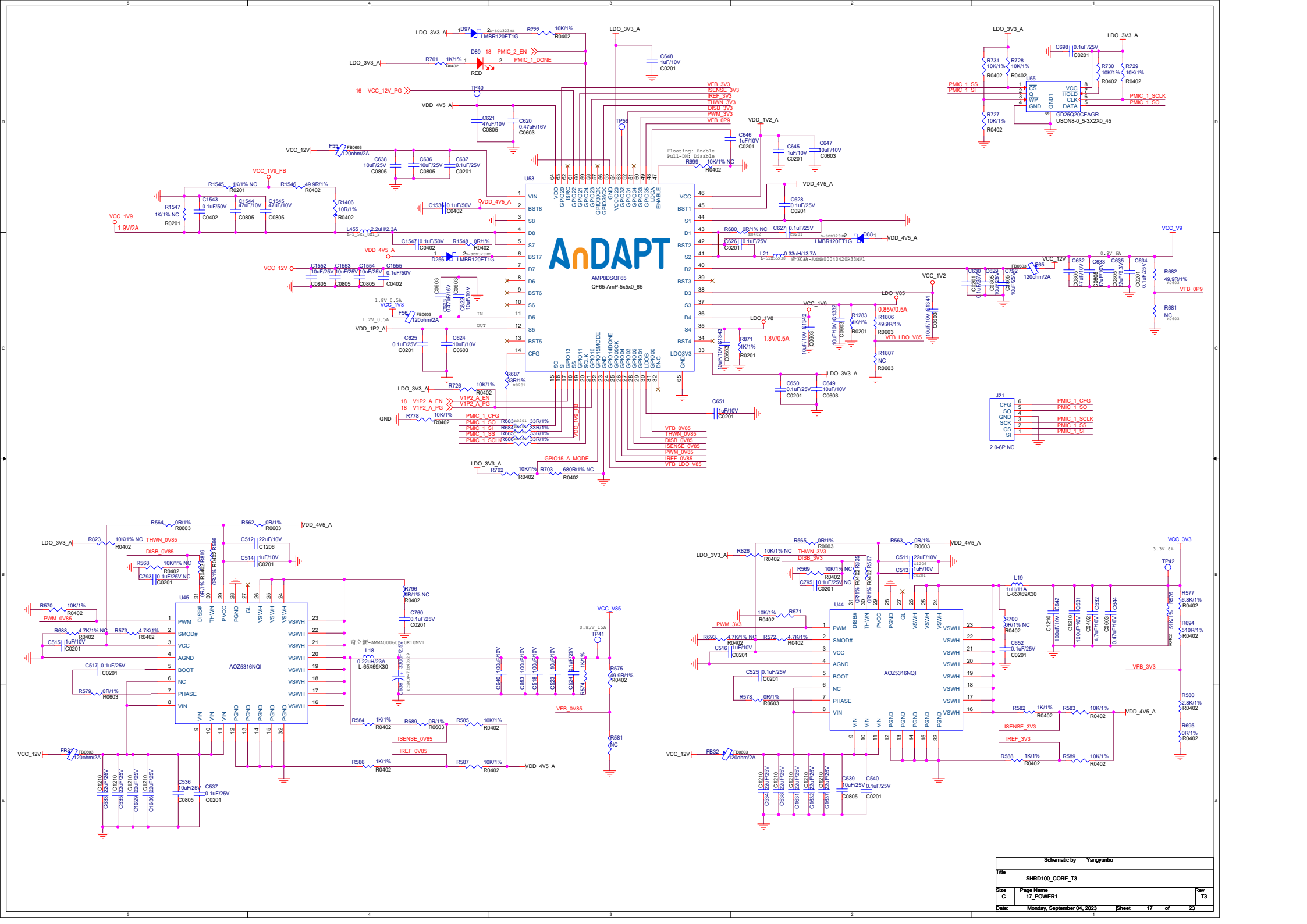




Schematic by	Yangyunbo	
Title	SHRD100_CORE_T3	
Size C	Page Name 15_FAN_GYRO	Rev T3
Date: Monday, September 04, 2023	Sheet 15 of 23	



Schematic by	Yangyunbo	
Title	SHRD100_CORE_T3	
Size C	Page Name 16_PWR_IN	Rev T3
Date: Monday, September 04, 2023	Sheet 16 of 23	


AnDAPT
AMP8DSQF65
QF65-AmP-5x5x0_65
U53
U45
AOZ5316NQI
U44
AOZ5316NQI
U55
GD25Q20CEAGR
USON8-0_5-3X2X0_45
J21
2.0-6P NC
LDO_3V3_A
VDD_4V5_A
VDD_1V2_A
VCC_1V2
VCC_1V9
VCC_12V
VCC_V9
VCC_V85
VCC_3V3
VDD_1P2_A
VCC_1V8
VFB_3V3
VFB_0V9
VFB_0V85
PMIC_1_SS
PMIC_1_SI
PMIC_1_SCLK
PMIC_1_SO
PMIC_1_CFG
THWN_3V3
DISB_3V3
PWM_3V3
ISENSE_3V3
IREF_3V3
THWN_0V85
DISB_0V85
PWM_0V85
ISENSE_0V85
IREF_0V85
VFB_LDO_V85
V1P2_A_EN
V1P2_A_PG
PMIC_1_EN
PMIC_1_DONE
GPIO15_A_MODE
VCC_12V_PG
LMBR120ET1G
奇立新-AMMA00040420R33MV1
奇立新-AMMA00060520R10MV1
0.85V/0.5A
1.8V/0.5A
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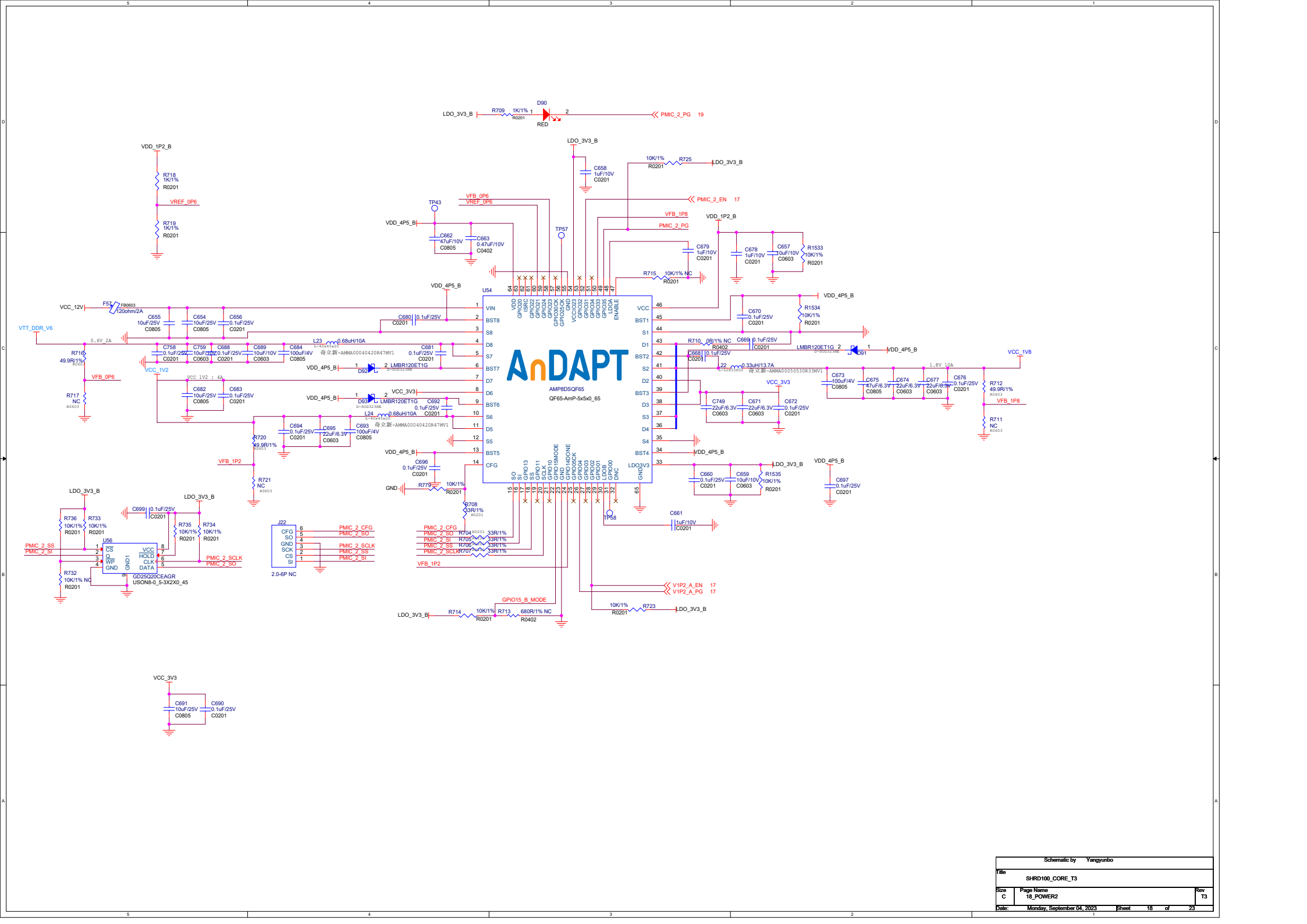

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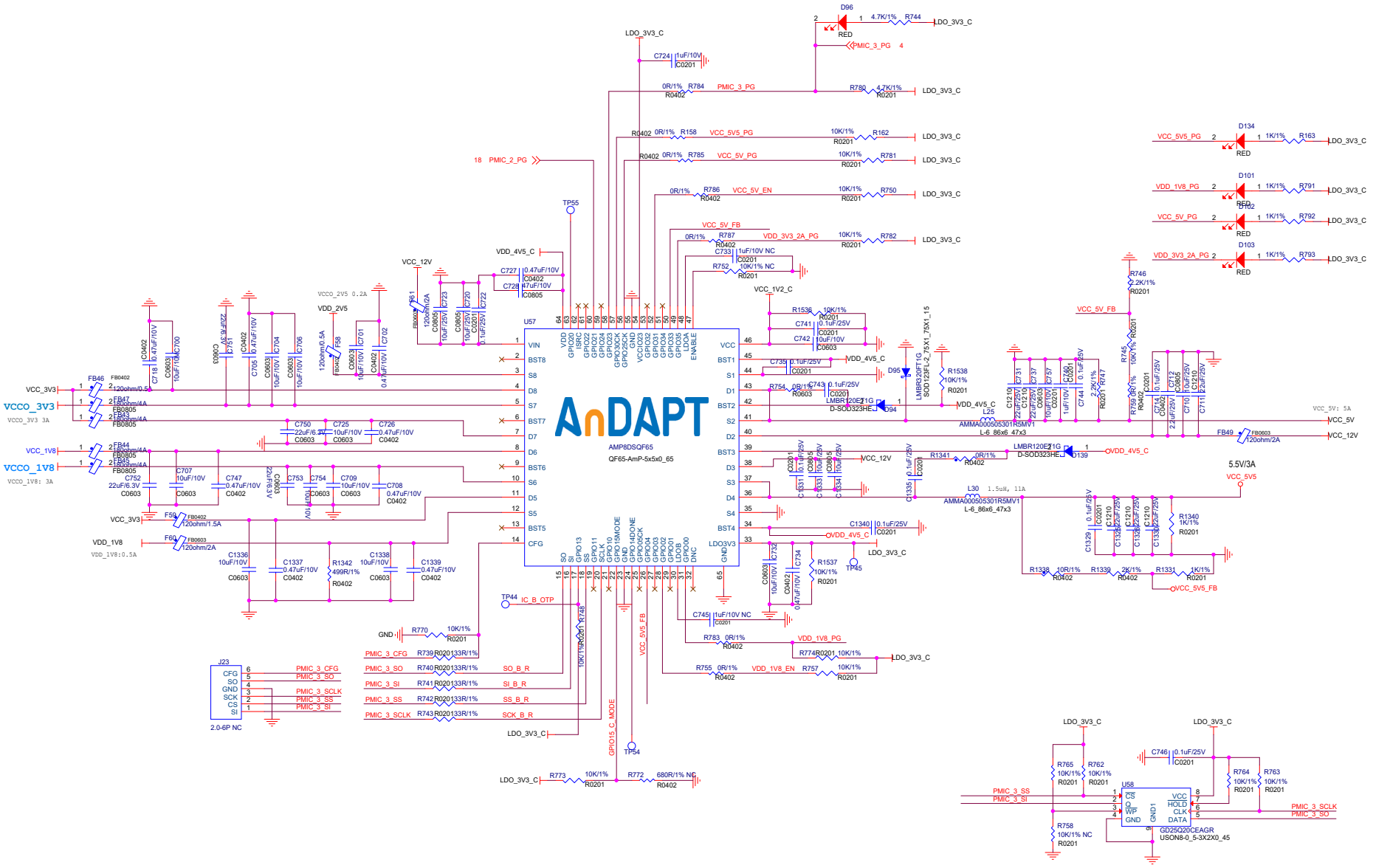

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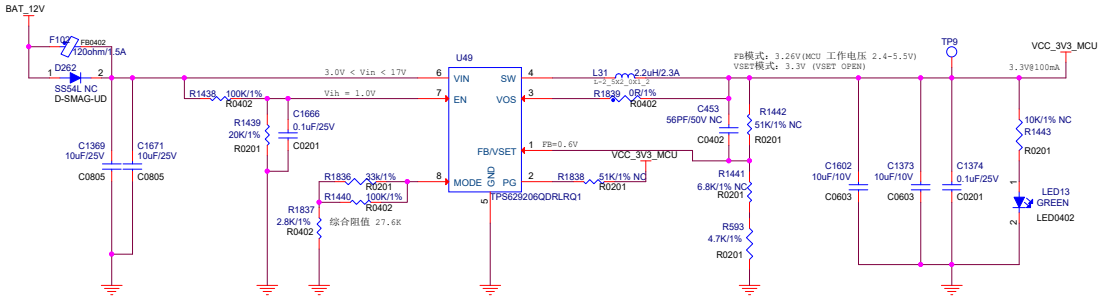
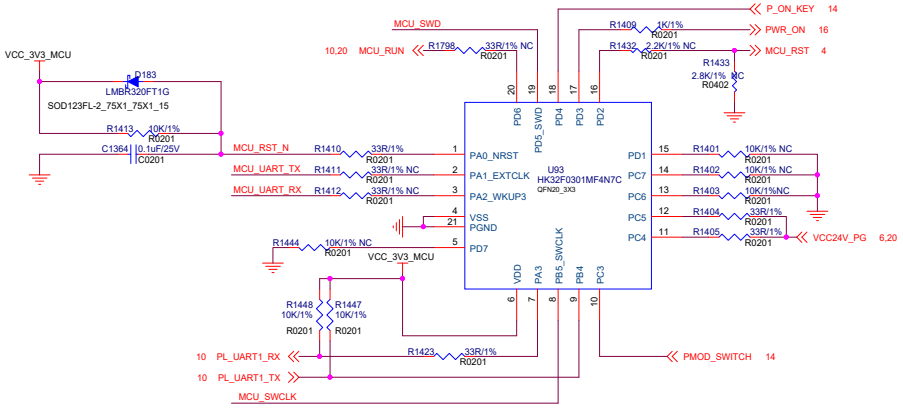
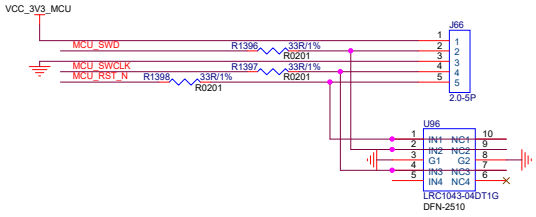
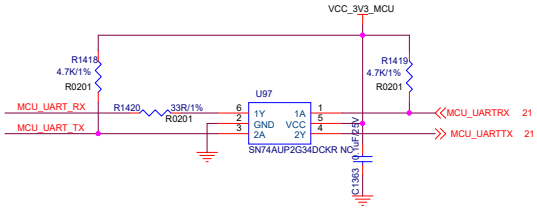


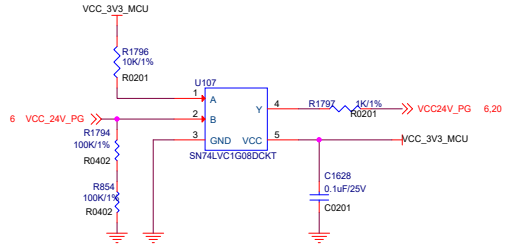
Table 8-1. Smart-CONFIG Setting Table

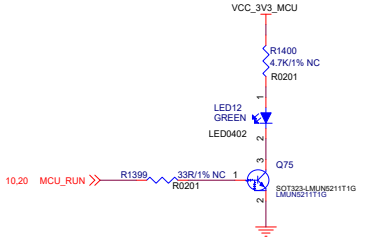
#	M ODE/S-CONF Level Or Resistor Value [Ω] (1)	FB/VSET Pin	F_{SW} (MHz)	Output Discharge	Mode (Auto Or Forced PWM)	Dynamic Mode Change
	Setting Options by Level					
1	GND	external FB	up to 2.5(2)	yes	Auto PFM/PWM with AEE	Active
2	HIGH (> 1.8 V)	external FB	2.5	yes	Forced PWM	
	Setting Options by Resistor					
3	7.50 k	external FB	up to 2.5(2)	no	Auto PFM/PWM with AEE	not active
4	9.31 k	external FB	2.5	no	Forced PWM	
5	11.50 k	external FB	1	yes	Auto PFM/PWM	
6	14.30 k	external FB	1	yes	Forced PWM	
7	17.80 k	external FB	1	no	Auto PFM/PWM	
8	22.10 k	external FB	1	no	Forced PWM	
9	27.40 k	VSET	up to 2.5(2)	yes	Auto PFM/PWM with AEE	
10	34.00 k	VSET	2.5	yes	Forced PWM	
11	42.20 k	VSET	up to 2.5(2)	no	Auto PFM/PWM with AEE	
12	52.30 k	VSET	2.5	no	Forced PWM	
13	64.90 k	VSET	1	yes	Auto PFM/PWM	
14	80.60 k	VSET	1	yes	Forced PWM	
15	100.00 k	VSET	1	no	Auto PFM/PWM	
16	124.00 k	VSET	1	no	Forced PWM	











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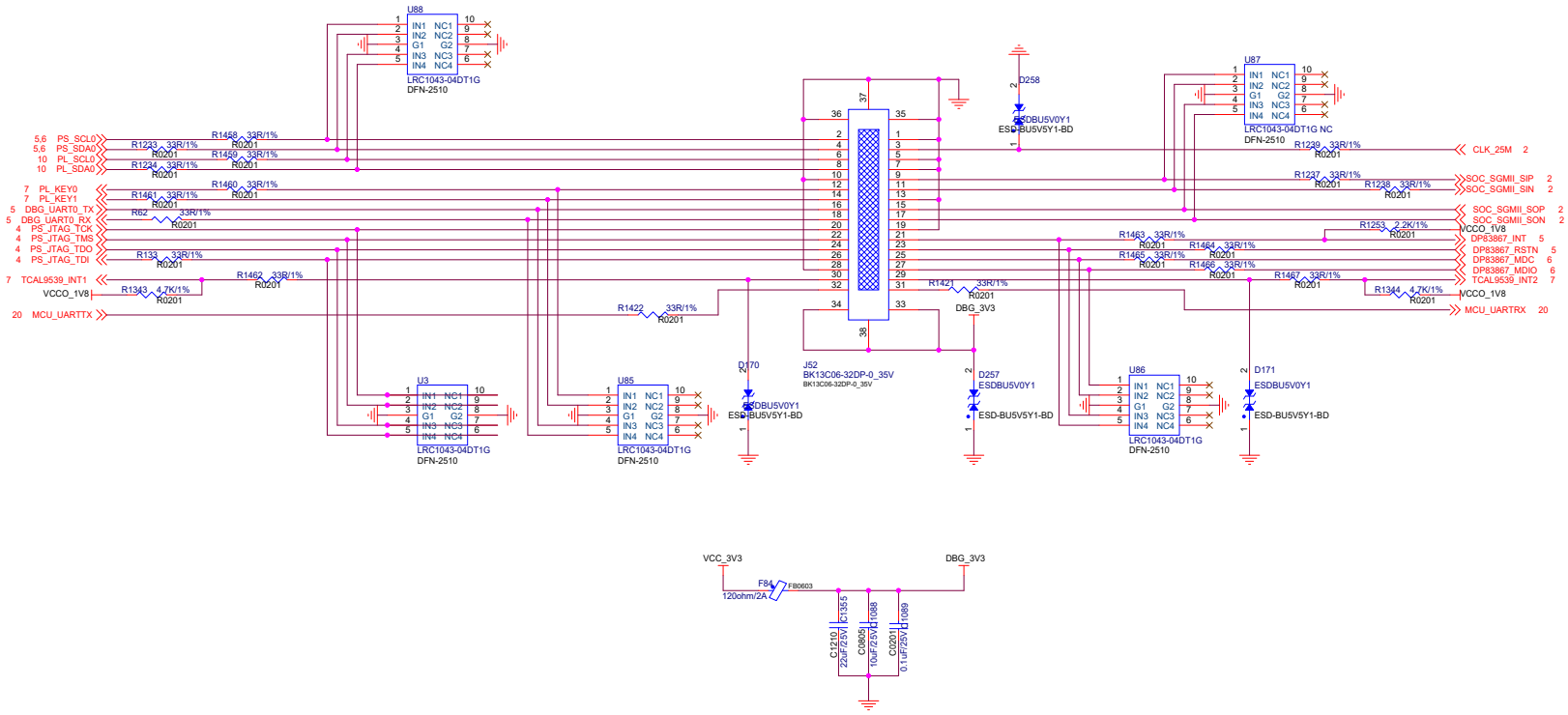

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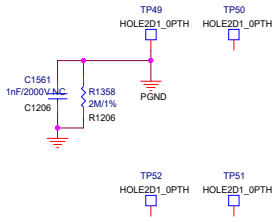
板上的螺钉通孔，
内直径2.1mm。



SMD 线夹

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本版在 SHRD100 CORE T2 基础上，主要修改点如下：
1、外部天线端口分出一1 路到射频模块，用于频谱侦测；
2、保留一个螺钉孔接保护地；
3、增加射频保护电路；
4、修正 T2 版本的 BUG：DC 电源与BAT电源之间增加防反灌二极管等；

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