Zhengxiong Li

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EDUCATION

Wuhan University Wuhan, China
Bachelor of Engineering, Hongyi Honor College 09/2020 - 06/2024

- **Major:** Microelectronics Science and Engineering
- **Cumulative GPA:** 3.79/4.00
- **Honors & Awards:**
  2022 First Prize in China Undergraduate Mathematical Contest in Modeling
  2023&2022&2021 Wuhan University Outstanding Student Scholarship

PATENT & PAPER

- Hu, M., **Li, Z.,** Jiang, X*. (2023). *A Resource-efficient FIR Filter Design Based on an RAG Improved Algorithm.* In Proceedings of the 2023 5th International Conference on Circuits and Systems (ICCS) (Poster and Oral Presentation by **Li, Z**), Huzhou, China. Retrieved from https://ieeexplore.ieee.org/document/10367312
- **Li, Z.**, et al. (2021). *Laser directional energy deposition area calculation method of full convolution neural network*. Application CN202110307051.9A events. 2021-06-15 Publication of CN112967266A. Retrieved from https://patents.google.com/patent/CN112967266A/en?oq=CN112967266A
- **Li, Z.**, et al. (2021). *Laser directional energy deposition sputtering counting method of full convolution neural network*. Application CN202110307531.5A events. 2021-06-15 Publication of CN112967267A. Retrieved from https://patents.google.com/patent/CN112967267A/en?oq=CN112967267A

RESEARCH EXPERIENCE

Development of an FPGA-Based Automatic Calibration System for RFIC Wuhan, China
Independent Undergraduate Researcher; Supervisor: Prof. Xianyang Jiang *05/2022 – 04/2023*

- Designed a pair of SPI protocol communication interfaces to enable data transmission among the PC, FPGA board, and target chip to be calibrated.
- Employed the DDS method to develop a system generating periodically vibrating waveforms with high stability.
- Developed a series of FIR filters and verified their efficacy using Matlab while integrating various decimation modules to filter the digital data acquired from ADC for precise signal processing.
- Conducted simulation and debugging procedures for FPGA and PCB boards, leading to their successful deployment.

FPGA/GPU-Based Numerical Solvers for Sustainable Energy System Simulation Edmonton, Canada
Lab's Name: RTX-Lab (Real Time Experiment Laboratory)[1], University of Alberta
Research Intern; Mitacs Internship; Supervisor: Prof. Venkata Dinavahi, IEEE fellow *06/2023 - 09/2023*

- Developed a high-performance solution for real-time simulation of electrical systems, ensuring the hardware's ability to predict the next 1us' situation within a strict time frame, such as 100ns or shorter.
- Trained GRU and LSTM models for Synchronous Machine and Induction Machine modeling.
- Implemented the pre-trained model on Xilinx Data Center Acceleration Card (U250), aiming to achieve real-time or faster than real-time simulation for the entire electrical system.

Multi-Scale Spatial Registration Method for Whole-Slide Pathology Images Wuhan, China
Undergraduate Researcher; Supervisor: Prof. Cheng Lei *03/2023 - Present*

- Reviewed existing literature on pathology image analysis and identified limitations in current methods such as SIFT, KAZE, AKAZE, and BRISK.
- Developed an algorithm based on the concept of multi-scale spatial space for efficient extraction of image features; overcame challenges posed by rotation, missing parts, and color differences in whole-slide pathology image analysis.
- Successfully achieved image registration based on the extracted features and achieved a high level of accuracy.

Image Segmentation and Classification in Metallic Additive Manufacturing Wuhan, China

[1] Official Website of RTX-Lab is available at: http://www.ece.ualberta.ca/~dinavahi/RTX_index.htm

Researcher Leader *10/2020 - 06/2021*

- Applied FCN neural network for semantic segmentation of captured images, enabling accurate measurement of the area of molten pool sections and the counts of sputtering sections in metallic additive manufacturing.

ACADEMIC EXPERIENCE

RISC-V CPU Implementation on FPGA Wuhan, China

Core Member *08/2022 - Present*

- Designed a five-stage pipeline CPU and achieved basic operations such as XOR, AND, and algorithm calculation.
- Designed bypass and stall structure to solve data hazard while data are required before it is written back into registers.

FPGA-Based Ultra-High-Speed Panoramic Camera Image Stitching Project Wuhan, China

Core Member *04/2023 - 06/2023*

- Improved the performance of existing software algorithm and transformed it into hardware description language.
- Implemented the improved algorithm on a Xilinx FPGA development board, to achieve high resolution and high frame rate for panoramic camera image stitching.
- Collaborated with a diverse team, including fellow students from the laboratory, engineers from the company, and students from Huazhong University of Science and Technology.

Self-Localizing Robotic Arm Wuhan, China

Core Member *02/2022 - 05/2023*

- Conducted software algorithm development to enable the robotic arm's self-localization in a confined environment.
- Identified random errors in data transmission of sensor data between the Arduino boards, which were caused by electromagnetic interference.
- Switched from IIC protocol to SPI protocol to provide a more reliable communication protocol for data transmission.

LEADERSHIP EXPERIENCE

Deputy President at Chinese Flute Club *9/2021 - Present*

- Coordinated various large-scale events, such as Club Recruitment and Anniversary Concert, attracting participation of over 500 students and faculty members; achieved the honorary title of "Top 10 Clubs" at Wuhan University.

Teaching Assistant of Digital Logic Circuit Laboratory Experiment Course *07/2022 - 09/ 2022*

- Conducted seminars, collected technical documents, graded them, and contributed to curriculum design.
- Successfully recruited exceptional students to the laboratory through targeted outreach efforts.

Coordinator of COVID-19 Relief Volunteer Group in Shijiazhuang *12/2020 - 02/ 2021*

- Assisted in the organization of multiple rounds of nucleic acid amplification testing and distribution of essential living supplies to residents.

OTHER INFORMATION

- **Programming:** Verilog for hardware description, Python for data analysis and automatic script, Matlab for module verification and automatic script, C & C++ for high-level hardware description
- **Laboratory Techniques:** Vitis, Vivado, Quartus, Modelsim, FPGA hardware debug, FPGA software development
- **Software:** Vitis, Vivado, Quartus, Modelsim, Latex, Markdown, Microsoft Office
- **Languages:** Mandarin (Native), English (Fluent), Japanese (Basic)