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Guilei Wang

# Investigation on SiGe Selective Epitaxy for Source and Drain Engineering in 22 nm CMOS Technology Node and Beyond



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Guilei Wang

# Investigation on SiGe Selective Epitaxy for Source and Drain Engineering in 22 nm CMOS Technology Node and Beyond

Doctoral Thesis accepted by  
Chinese Academy of Sciences, Beijing, China



Springer

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# **Supervisors' Foreword**

After five decades, CMOS has been constantly downscaled following the technology road map, and by crossing to sub-10-nm node, we further approach to the end of road map in few years. During this period of time, the IC manufacturer has solved many problems and technical problems, and today's transistor structure is totally different than original one manufactured in the Bell Labs. The most important key points for improving the transistor performance are strain engineering, new high-k & metal gate, junction formations, and transition from 2D to 3D structure. By considering these designs, the carrier mobility increased significantly, and short-channel effect could be decreased in the ultra-small transistor sizes.

Many efforts have been spent to introduce new processing, specially the selective deposition of SiGe layers in the source/drain regions. The SiGe material has been used as stressor material to create uniaxial strain in the channel. One major problem for such design is pattern dependency of the growth where the profile of SiGe layer varies due to the variation of the chip layout.

This thesis presents research in field of microelectronics which carried out during four years in Chinese Academy of Science in Institute of Microelectronics. This work presents integration, growth, and strain engineering of SiGe in source/drain in 22- and 16-nm node CMOS. The transistor processing has been paid attention, the steps such as in situ and ex situ cleaning of recess in S/D regions and surface of the Si fins have been studied, and their impact on the shape of the recess in S/D and Si fins and quality of SiGe epitaxy have been investigated. This research provides valuable information about how to measure strain by XRD and TEM techniques. Another focus has been spent on establishing a kinetic model to predict the layer profile of SiGe and the pattern dependency behavior of the growth. The quality of research is excellent, and it contains very important scientific content; many parts of work have been even awarded in important conferences (EMRS).

Beijing, China  
May 2019

Prof. Henry H. Radamson  
Prof. Chao Zhao

# Abstract

As CMOS technology is continuously downscaled for decades, the traditional 2D transistor design has ended in 22-nm technology node, and 3D transistors were invented to control the short-channel effect, parasitic resistances, and capacitances. Different methods have been also proposed to engineer the strain in the channel region and boost the channel mobility. During these technology developments, selective epitaxial growth (SEG) method has been used to deposit SiGe as stressor material in source and drain (S/D) region to induce uniaxial strain in channel region. This thesis is in the field of nanoelectronics and presents device processing and epitaxy modeling. It presents the key parameters of high-quality SiGe selective epitaxial growth with a focus on its pattern dependency behavior and the key integration issues in the transistor structures. The main research outcome of this thesis is as follows:

- (1) It is found that *in situ* cleaning has large impact on dopant diffusion and to shape of the S/D recess as well as the Si fins. For 22-nm planar devices, pre-baking at 800 °C is applicable, whereas pre-baking at lower temperature as 780–800 °C is necessary to remove native oxide but to avoid any damage to Si fins which is essential for high-quality SiGe SEG. The S/D Si loss at high pre-baking temperature is attributed to HCl etching because of residual Cl atoms in H<sub>2</sub> atmosphere. At lower pre-baking pressure, the morphology change occurs, and this is caused by the migration of Si atoms originating from the thermal mismatch between SiO<sub>2</sub> and Si.
- (2) The *ex situ* cleaning has also important role on the SiGe epitaxial layer. It is observed that rinsing time in diluted buffer oxide etch (DBOE) and the amount of HCl affect SiGe SEG significantly. These two parameters need to be optimized in order to avoid mushroom-like growth on both dummy gate and Si<sub>3</sub>N<sub>4</sub> isolation spacers.
- (3) Selective growth Si<sub>1-x</sub>Ge<sub>x</sub> ( $0.25 \leq x \leq 0.35$ ) with boron concentration of  $1-3 \times 10^{20} \text{ cm}^{-3}$  was investigated and optimized for S/D regions of 22-nm node planar transistors and 14-nm node FinFETs. A three-layer structure of Si<sub>1-x</sub>Ge<sub>x</sub> was designed in S/D areas. A strain-relaxed buffer (SRB) layer as

bottom layer, the middle layer with high Ge content ( $\text{Si}_{0.65}\text{Ge}_{0.35}$  or  $\text{Si}_{0.60}\text{Ge}_{0.40}$ ), was intended as stressor material to fill the recess and a cap layer with low Ge content ( $\text{Si}_{0.75}\text{Ge}_{0.25}$  or  $\text{Si}_{0.80}\text{Ge}_{0.20}$ ) as a sacrificial material for the Ni-silicidation process. The purpose of the cap layer was to avoid strain reduction in the channel region when the layer is consumed. The characteristics of transistors were measured, and the results were explained in terms of growth conditions.

- (4) A kinetic gas model was developed to evaluate the pattern dependency of the SiGe SEG process and to predict the layer profile within transistor arrays in a chip and over different locations on a wafer. The input parameters include growth temperature, partial pressures of reactant gases, and chip layout. By using this model, the number of test wafers for epitaxy experiments can be decreased significantly when the chips are located with a distance from the edge of the 200-mm wafer. SiGe layers with poor epi-quality were obtained when the coverage of exposed Si of the chip was below 1%. In such chips, high Ge content with layer thicknesses above the critical thickness was observed. When the epitaxy process parameters can be predicted by the model for a desired epi-profile in an advanced chip design, fast and cost-effective process development can be achieved in the mass production.

**Keywords** CMOS • Planar transistors • FinFET • Strain • SiGe • Selective epitaxial growth • RPCVD • Pattern dependency

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As time flies, my time of doctoral study is drawing to a close in the twinkling of an eye. I still remember that I felt in tension when I just passed my Ph.D. entrance examination many years ago, but for now I still feel uneasy at the end of my Ph.D. study. This kind of nervous mood is like holding a newborn baby, happy and bewildered. I once went astray on the way of learning, and I was not the “Outstanding Student” in everyone’s eyes. I am so grateful that I could continue my study after leaving the college for many years. Hereby, I would like to extend my most sincere gratitude to all the teachers, classmates, relatives, friends, and colleagues who have cared, supported, and helped me.

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May 2016

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# Abbreviations

AFM	Atomic force microscopy
APCVD	Atmospheric pressure chemical vapor deposition
APM	$\text{NH}_4\text{OH} + \text{H}_2\text{O}_2 + \text{H}_2\text{O}$
$\text{B}_2\text{H}_6$	Diborane
C	Carbon
CESL	Contact etch stop layer
CMOS	Complementary metal-oxide semiconductor
CMP	Chemical-mechanical polishing
CVD	Chemical vapor deposition
DBOE	Diluted buffer oxide etch
DFM	Design for manufacturability
DG	Double gate
DHF	Diluted hydrofluoric acid
DIBL	Drain-induced barrier lowering
DSL	Dual stress liner
DTMAH	Diluted tetramethylammonium hydroxide
EBL	Electron beam lithography
EDX	Energy-dispersive X-ray detector
EOT	Equivalent oxide thickness
ESD	Electrostatic discharge
FIB	Focused ion beam
FinFET	Fin field-effect transistor
FWHM	Full-width half-maximum
Ge	Germanium
$\text{GeH}_4$	Germane
HARP	High-aspect-ratio process
HBT	Heterojunction bipolar transistor
HCI	Hot-carrier injection effect
HH	Heavy-hole
HKMG	High-k metal gate

HOI	Heterostructure on insulator
HRRLM	High-resolution reciprocal lattice mapping
HRTEM	High-resolution transmission electron microscopy
HRXRD	High-resolution X-ray diffraction
IC	Integrated circuit
LD <sub>D</sub>	Lightly doped drain
LH	Light-hole
LPCVD	Low-pressure chemical vapor deposition
LPE	Liquid-phase epitaxy
MBE	Molecular beam epitaxy
MFC	Mass flow controller
MGIS	Metal gate-induced strain
MOS	Metal-oxide semiconductor
NMOS	N-type metal-oxide semiconductor
NSEG	Non-selective epitaxial growth
PMOS	P-type metal-oxide semiconductor
R&D	Research and Development
RMS	Root mean square
RPCVD	Reduced pressure chemical vapor deposition
S/D	Source/Drain
SCE	Short-channel effect
SEG	Selective epitaxial growth
Si	Silicon
SiC	Si <sub>1-y</sub> C <sub>y</sub> Silicon carbon alloy
SiGe	Si <sub>1-x</sub> Ge <sub>x</sub> Silicon germanium alloy
SiH <sub>2</sub> Cl <sub>2</sub>	Dichlorosilane, DCS
SiH <sub>4</sub>	Silane
SIMS	Secondary ion mass spectrometry
SMT	Stress memorization technique
SOI	Silicon on insulator
SPE	Solid-phase epitaxy
SPM	H <sub>2</sub> SO <sub>4</sub> + H <sub>2</sub> O <sub>2</sub>
SRB	Strain-relaxed buffer
SSDOI	Strained silicon directly on insulator
SSL <sub>S</sub>	Singapore synchrotron light source
SSRF	Shanghai synchrotron radiation facility
STI	Shallow trench isolation
TCAD	Technology computer-aided design
TEM	Transmission electron microscopy
TFET	Tunnel field-effect transistor
UHVCVD	Ultra-high vacuum chemical vapor deposition
VPE	Vapor-phase epitaxy
XRD	X-ray diffraction

# Chapter 1

## Introduction



Currently, we are living in the modern time and era of information technology. As the foundation of information industry, the development of integrate circuit (IC) is inseparable from our daily life. The emergence of new electronic applications are commonly in used smart phones, computers, drones, and unmanned vehicle which is all attributed to great advances and innovations of IC technology. The development history of IC in recent decades is not only the result of the combination of technology promotion and market demand, but also the history of the transformation of technological innovation into productivity [1]. In addition, the progressive development of integrated circuit has always been considered as the key to promote the development of information technology, and the technology node and production scale. Therefore, the level of IC development are important metrics for evaluating the overall national strength and level of economic growth.

### 1.1 Development Status and Challenges of Integrated Circuit

On December 16, 1947, the first transistor was invented at Bell Laboratories by William Shockley, John Bardeen and Walter Brattain. This was perhaps the most important electronics event of the 20th century, as it later made possible the integrated circuit and microprocessor that are the basis of modern electronics [2]. On September 12, 1958, Jack Kilby of Texas Instruments built the first monolithic integrated circuit using germanium mesa. Although the proposed IC comprises just one transistor, it still marks the arrival of IC era for the world. In 1960, the first planar integrated circuit is fabricated at Fairchild Semiconductor in the United States. Later in 1963, Frank Wanlass of the Fairchild R&D Laboratory showed that logic circuits combining p-channel and n-channel MOS transistors in a complementary symmetry circuit configuration CMOS, which has still been used today owing to its superior performance. In 1965, Gorden Moore proposed the famous “Moore’s Law”, which is

the observation that the number of transistors per unit area the degree of integration would double every 18 months. In each technology generation, transistor dimension is scaled by 30% (0.7x) and the chip performance is doubled [3]. In 1968, Intel was founded by Robert Noyce, Gorden Moore, and Andrew Grove, indicating the start of large-scale commercialization of LSI CMOS technology.

In the past decades, semiconductor technology has developed continuously in accordance with the device scaling theory proposed by Dennard et al. [4, 5], which has stimulated the increment of integration scale and improvement of performance for integrated circuit. With the development of CMOS IC technology over the past decade, it gradually becomes difficult to improve IC performance just through continuous scaling-down of device dimensions. Some of the fabrications techniques that have been used for a long time become hard to maintain the scaling-down trend. Thus, new process modules, new materials, and new device structures should be developed in time to overcome these upcoming challenges and to continue Moore's Law. Figure 1.1 shows the key technology roadmap for CMOS integrated circuit.

The last 20 years have seen an aggressive scaling-down of silicon CMOS technology from 1  $\mu\text{m}$  planar structure to advanced 20 nm 3D FinFETs. Especially, when entering the 45 nm technology node and below, the reduction of the physical gate

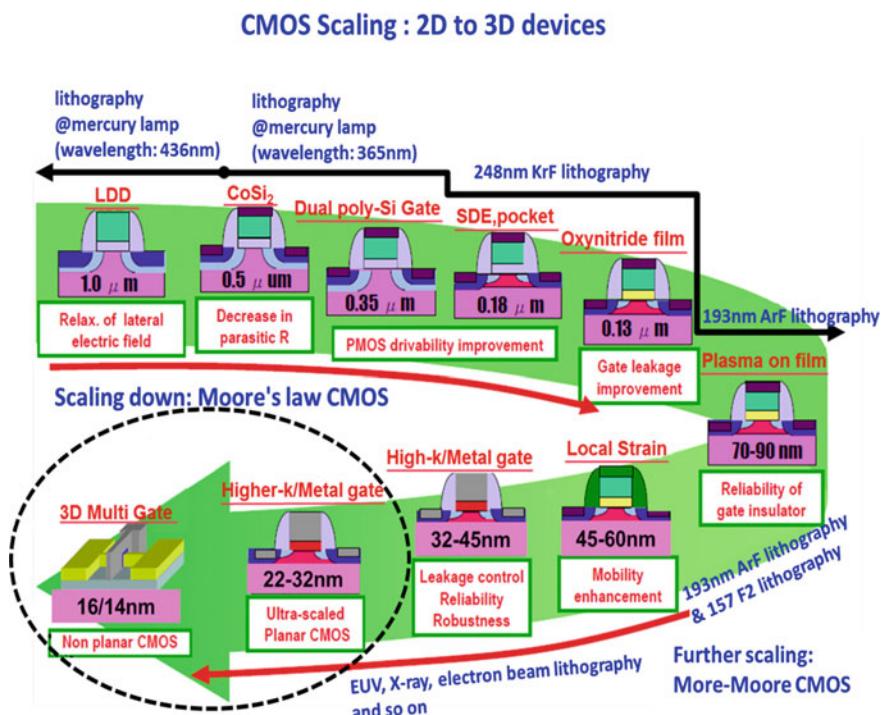


Fig. 1.1 Key technology roadmap for CMOS integrated circuit

length brings more technical challenges to nanoscale CMOS devices [6, 7]. The main technical challenges are listed as follows:

1. Gate electrode: The polysilicon depletion effect (PDE) induced by the traditional polysilicon gate results in an increase of equivalent gate oxide thickness, reduced gate control and occurrence of short channel effects (SCE) particularly in small-size MOSFETs. Therefore, traditional polysilicon can't meet the requirements of gate control for small-size MOSFETs.
2. Gate dielectric: As the device size continues shrinking, the gate oxide thickness needs to be continuously thinned down to improve short channel effects immunity and gate controllability. However, using ultra-thin gate oxide exponentially increases the tunneling leakage current, followed by increasing of power consumption. Thus, the device reliability issues become more prominent. The distributed defects and traps in interfacial oxide cause significant interfacial and Coulomb's scattering, resulting in serious degradation of carrier mobility.
3. Channel/substrate: the reduction of gate length leads to serious short channel effects, drain-induced barrier lowering (DIBL), deterioration of the sub-threshold characteristics, etc. Due to the existence of parasitic effects, device drive current no longer increases linearly. Hence, carrier mobility of the channel needs to be further improved to boost device performance.
4. Source/drain (S/D) regions: In order to enhance the channel carrier mobility, strain engineering by selective epitaxial growth of heterojunction materials in S/D regions has been widely employed to induce uniaxial strain in channel region and to boost carrier mobility. Besides, parasitic S/D series resistance is difficult to scale down proportionally with the shrinkage of device size, which becomes a more important contributor to the total resistance of a transistor and inevitably impacts the drive current. Thus, suitable silicide processes corresponding to different S/D materials should be implemented to reduce the parasitic resistance.

In an effort to overcome the above-mentioned technical challenges, new technologies have been employed into each product generation to continue the trend of Moore's Law. For example, strained silicon technology has been utilized to improve the current drive capability of transistors through enhancing the carrier mobility of channel. To mitigate the impact of S/D parasitic series resistance and capacitance on device performance, Schottky-barrier silicide S/D has been proposed to replace the ion-implanted S/D in conventional CMOS process. In order to improve the short channel effects, ultra-shallow and halo implantation techniques are applied in S/D regions [8]. And in order to restrain hot-carrier injection effect (HCI), lightly-doped-drain (LDD) implantation and other techniques are also suggested [9].

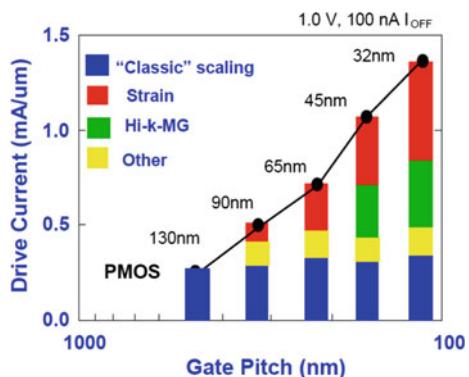
Later, dozens of new semiconductor materials are introduced to resolve the process problems and improve the performance of the device. In 2007, Intel introduced high- $\kappa$  dielectric and metal gate in 45 nm planar technology node to reduce the device's equivalent oxide thickness (EOT) and to enhance gate control capability [10]. In 2009, Intel unveiled the second generation of HKMG process in its 32 nm technology node, for the purpose of further EOT scaling and device performance improvement [11]. When CMOS process enters 10 nm node and below, new channel materials

with higher carrier mobility than silicon, such as Ge, III-V compounds and so on, are likely to be introduced to further promote the development of CMOS integrated circuit technology [12].

With respect to novel device structures, several new types of MOSFETs have been reported, such as silicon on insulator (SOI) MOS devices [13–15], planar double-gate (DG) MOSFETs [16], fin field-effect transistor (FinFETs) [17],  $\Omega$  gate and multi-gate MOSFETs [18], tunnel field-effect transistor (TFET) [19] and so on. Among these new device structures, the 22 nm FinFET product proposed by Intel in 2011 is the most attractive one. FinFET devices differ from planar structure counterparts by the three-dimensional Fin structure, which leads to further improvement of device performance and integration density of IC [20]. In 2013, Intel developed FinFET technology to 16 nm node [21], and optimized the Fin structure through further reduction of Fin pitch to increase integration density. At present, research and development (R&D) of Intel's 10 nm technology is in progress.

In brief, the development of CMOS IC technology and the extension of Moore's Law are inseparable from the breakthrough of new process modules, new materials and new device structures. In each technology node, technical schemes always follow the previous technology roadmap with minor changes. If technical changes are too significant, mass production would become more challenging and the manufacturing cost would rise simultaneously. Thus, industries always give priority to technology solutions adapted for large-scale production instead of those with major changes. For example, strained silicon technology is one of the technical solutions suitable for large-scale production [22]. As shown in Fig. 1.2, strain has had tremendous impact in advancing the transistor scaling roadmap for generations after the 130 nm node (90, 65, 45, 32 nm) [23]. One way to carry out strain engineering in the transistor structure is using SiGe alloy as stressor material in S/D areas. Epitaxial growth of SiGe in S/D can generate compressive strain in PMOS channel region which can enhance hole mobility, leading to performance enhancement of CMOS transistors. Integration of highly strained SiGe in S/D presents excellent compatibility with current CMOS technology and plays an increasingly important role in advanced manufacturing processes.

**Fig. 1.2** Importance of strain in modern CMOS scaling [23]



## 1.2 Major Research Works in This Thesis

In this paper, integration of strained SiGe in S/D for 22 nm planar and 16 nm FinFET devices has been systematically investigated to meet the requirements of the “National S&T Major Project 02”. This research focuses on selective epitaxial growth of high-quality strained SiGe thin films and its process integration and industrial-relevant applications. The research content in the work is closely relevant to practical issues in industry. The major research works are listed as follows:

1. Epitaxial growth of high-quality, defect-free strained SiGe thin films on an 8-inch process platform using reduced pressure chemical vapor deposition (RPCVD) and its process optimization for high epitaxial quality. Key factors that affects the high-quality selective epitaxial growth of SiGe films are analyzed to promote the applications of strained SiGe technology.
2. Key technical issues for selective epitaxial growth of SiGe film on S/D are studied. The research contents include the influence of cleaning process prior to epitaxy and prebake during epitaxial growth on the surface morphology of SiGe film in S/D.
3. The influence of the DBOE rinse time and the amount of HCl vapor on the selectivity of SiGe epitaxial growth are studied.
4. Electrical characteristics for 22 nm planar and 16 nm FinFET devices with SiGe S/D are systematically analyzed. High-resolution X-ray diffraction (HRXRD) detection technique and Technology Computer Aided Design (TCAD) simulations are performed to analyze strain variation during SiGe epitaxial growth on S/D. During the source-drain epitaxial process, SiGe films with several Ge concentration gradients are experimentally grown as the strained S/D.
5. The reaction kinetics and growth mechanisms of SiGe selective epitaxy are studied. Meanwhile, the microscopic and macroscopic effects of the pattern density during selective epitaxial growth are explained in detail. By studying the diffusion kinetics of the reaction gas and the established calculation model, the causes for the dissimilarity of the properties of selective epitaxial grown SiGe films in different regions are also explained. The results of the calculation model are verified by the film growth rate and Ge composition distribution obtained from experimental test. This could establish a design for manufacturability (DFM) reference for SiGe selective epitaxial growth integration and layout design to resolve some practical issues for the application of SiGe technology.

## 1.3 Thesis Organization

According to the main research contents, the chapters in this thesis are arranged as follows:

This chapter presents the background of the thesis, the significance of the work, the main research contents and the organization of the thesis.

Chapter 2 presents the development and classifications of strained silicon technology, mechanisms of carrier mobility enhancement via strained silicon technology and main strain engineering techniques.

Chapter 3 focuses on epitaxial growth of high-quality SiGe films on S/D regions. The mechanisms of selective epitaxial growth of thin films are studied, and key process parameters affecting the growth of high quality SiGe films are also discussed.

In Chap. 4, the influence of cleaning process prior to epitaxy and pre-baking during epitaxial growth are systematically studied. In order to introduce the maximum stress on channel, SiGe film in S/D regions is sequentially grown in the sequence of buffer layer, core layer and sacrificial layer. The distribution and variation of strain during SiGe epitaxial growth on S/D were studied by HRXRD test technology and TCAD simulations. Integration of strained SiGe in S/D for 22 nm planar and 16 nm FinFET devices and electrical characterization have been performed and discussed.

In Chap. 5, based on the reaction kinetics and growth mechanism of SiGe selective epitaxy, a calculation model is established to study the influence of microscopic and macroscopic effects of the pattern density on the epitaxy results during the selective epitaxy process. And the theoretical calculation model is also verified through the test results of HRXRD and EDX.

In Chap. 6, key contributions of this research are summarized and future prospects for the applications of SiGe selective epitaxy technology are offered.

## 1.4 Summary

In this chapter, the development history of integrated circuits is briefly reviewed, and a series of CMOS scaling challenges as well as the corresponding technical solutions carried out in large-scale manufacturing are illustrated. Strained silicon technology adopted in 90 nm technology node is one of the key technologies for device driving capability improvement. Among the family of strained silicon technologies, SiGe source/drain is compatible with the CMOS process, and it plays an increasingly important role in advanced manufacturing processes. Therefore, this thesis focuses on the source/drain engineering. Finally, the main research work and the thesis organization are given.

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# Chapter 2

## Strained Silicon Technology



### 2.1 Introduction

With transistor dimension shrinking into nanoscale regime as described in the previous chapter, conventional gate oxide thickness has been scaled near the thickness limit of 1 nm. This scaling trend brings issues about power consumption, transistor density and off-leakage current, together with carrier mobility degradation. Furthermore, the continuous scaling-down of device dimensions and further performance enhancement are facing more and more severe challenges. Therefore, to overcome these challenges occurred during technology development, various technical solutions can be implemented to improve device performance. One of the important and simple technical solutions is strained silicon technology. For device driving capability improvement, strained silicon technology is applied to enhance the carrier mobility on channel to compensate the mobility degradation caused by the scaling-down of device dimensions [1–4].

In 2002, Intel unveiled its microprocessors using strained silicon technology at the 90 nm process node [5]. This is the first process in the industry to implement strained silicon in production. Since then, each process node has adopted different strained silicon technologies to improve device performance. For example, since 65 nm technology node, semiconductor industry has applied strained silicon technology into CMOS production [5], including strained SiGe on source/drain and silicon nitride capping layer. In addition, metal gate-induced strain is introduced in 45 nm process node [6]. Among the current approaches for transistor performance improvement, the mobility enhancement via strained silicon technology has had tremendous impact in device performance enhancement and has become one of the important techniques to extend Moore's Law [7].

## 2.2 Physics of Strained Silicon Technology

As we all know, the relationship between the drive current and the mobility of MOS-FETs is shown in the following equation [8]:

$$I_D = \frac{W\mu_{eff}C_{ox}}{2L}(V_G - V_T)^2 = \frac{W\mu_{eff}K_{ox}\epsilon_0}{2L}(V_G - V_T)^2$$

where  $I_D$  is the drive current,  $W$  is the channel gate width,  $L$  is the channel gate length,  $\mu_{eff}$  is the effective carrier mobility,  $C_{ox}$  is the gate oxide capacitance per unit area,  $V_G$  is the gate voltage and  $V_T$  is the threshold voltage. With the down-scaling of CMOS transistors, especially the aggressive shrinkage of channel length, channel doping concentration is increased to suppress the source-drain punch-through and short-channel effect. However, this results in the degradation of  $\mu_{eff}$  and threshold voltage roll-up. Therefore, in order to further enhance device performance, strained silicon technology, which can induce additional strain in channel region, should be performed to increase carrier mobility. This approach could compensate the mobility degradation due to several contributing factors, such as significant Coulomb's scattering which is originated from high channel doping concentration, and increased effective gate electric field and enhanced interface scattering caused by the down-scaling of gate dielectrics [1, 2, 4].

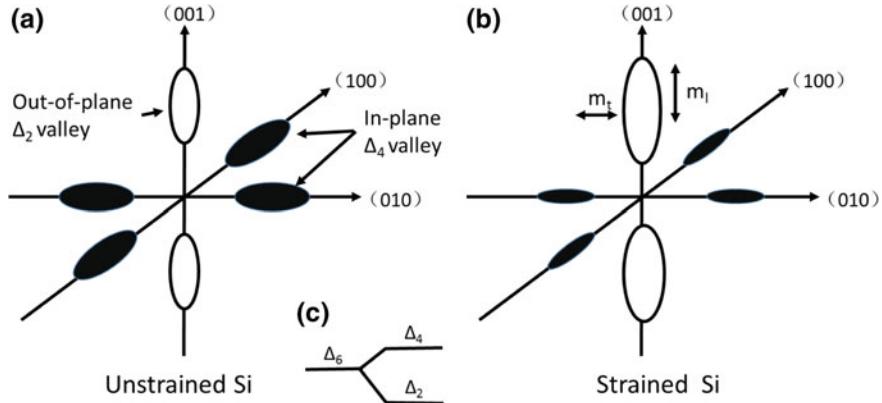
Based on the study of the impact of strain on carrier mobility [9–11], the carrier mobility can be expressed by Eq. (2.2):

$$\mu = \frac{q\tau}{m^*} \quad (2.2)$$

where  $q$  is the electron charge,  $1/\tau$  is the scattering rate and  $m^*$  is the conductivity effective mass. Strain enhances the mobility by reducing the conductivity effective mass and/or the scattering rate. For electrons, both mass and scattering changes are generally accepted as important for mobility enhancement [12]. However, for holes, mainly the mass change due to band warping and repopulation plays a significant role in (<1 GPa) stress level since strain induces smaller valence band splitting compared to the conduction band [13].

### 2.2.1 Effect of Strain on Electron Mobility

For electron transport in bulk Si at room temperature, the conduction band is comprised of six degenerate valleys, as shown in Fig. 2.1a. These valleys are of equal energy, as shown by  $\Delta_6$  in Fig. 2.1c. The degeneracy reflects the cubic symmetry of the Si lattice. The effective mass for any direction is the reciprocal of the curvature of the electron energy function in that direction. Consequently, the effective mass of each ellipsoid is anisotropic, with the transverse mass (perpendicular to the axis)



**Fig. 2.1** Electron conduction band valleys for **a** relaxed silicon, **b** strained silicon with biaxial tensile strain. **c** Energy level at the bottom of the six conduction band valleys. Application of advantageous strain splits the energy level as shown, removing the degeneracy (i.e., the equivalence in energy) between the  $\Delta_2$  and  $\Delta_4$  valleys

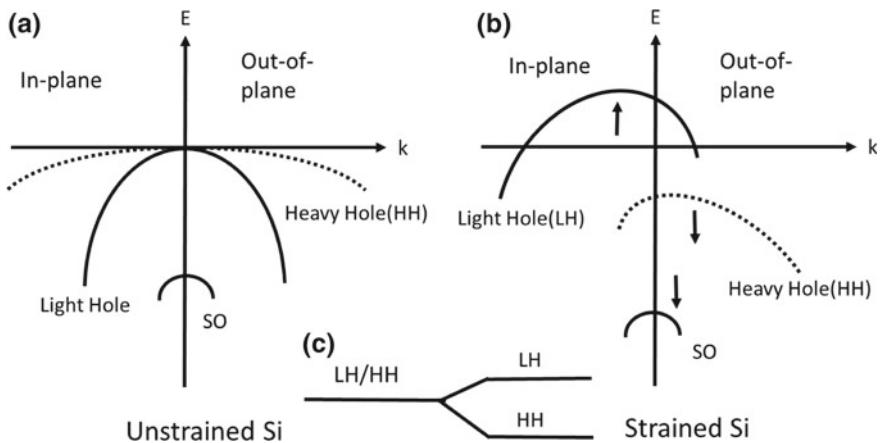
given by  $m_t = 0.19 m_o$  being significantly smaller than the longitudinal mass (parallel to the axis) given by  $m_l = 0.98 m_o$ , where  $m_o$  is the free electron mass [14]. For unstressed bulk Si, the total electron conductivity mass,  $m^*$ , is obtained by adding the contributions of the six degenerate valleys and is given by

$$m^* = \left[ \frac{1}{6} \left( \frac{2}{m_l} + \frac{4}{m_t} \right) \right]^{-1}$$

For MOSFETs on a (001) wafer, advantageous strain removes the degeneracy between the four in-plane valleys ( $\Delta_4$ ) and the two out-of-plane valleys ( $\Delta_2$ ) by splitting them in energy, as shown in Fig. 2.1b. The lower energy of the  $\Delta_2$  valleys means that they are preferentially occupied by electrons. The electron mobility partly improves via a reduced in-plane and increased out-of-plane  $m^*$  due to the favorable mass of the  $\Delta_2$  valleys, which results in more electrons with an in-plane transverse effective mass ( $m_t = 0.19 m_o$ ) and out-of-plane longitudinal mass ( $m_l = 0.98 m_o$ ). For a given strain, quantifying the effective mass reduction and comparing it to the enhanced mobility reveals that mass reduction alone explains only part of the mobility enhancement [15]. Hence, electron scattering must also be reduced due to the conduction valleys splitting into two sets of energy levels, which lowers the rate of intervalley phonon scattering between the  $\Delta_2$  and  $\Delta_4$  valleys [16].

### 2.2.2 Effect of Strain on Hole Mobility

For holes, the valence-band structure of Si is more complex than the conduction-band.



**Fig. 2.2** The hole valence band structure for **a** relaxed silicon and **b** strained silicon with biaxial tensile strain. **c** Splitting of holes under stress

For unstrained Si at room temperature, holes occupy three bands, including heavy-hole (HH) and light-hole (LH) bands, as well as a spin-orbit energy band lower than the  $\Gamma$  point. LH and HH bands are anisotropic and non-parabolically distributed on both sides of E-axis, as shown in Fig. 2.2a.

With the application of strain, the degenerate light and heavy hole bands split. The energy of the light hole band increases, forming the upper valence band, while the energy of heavy hole band decreases, forming the lower valence band. Besides, the energy of spin-orbit band also decreases [9], as shown in Fig. 2.2b, c. In addition to the valence band splitting induced by strain, the shape of the constant-energy surface of the valence band is changed, forming a warped valence band, and the effective masses of the holes along different directions exhibit high anisotropy and redistribute in reciprocal ("k") space. In this case, the effective mass of the holes along in-plane channel direction is mainly contributed by light holes, and the heavy holes are mainly redistributed in the crystal faces perpendicular to the channel. Therefore, the main reason for the increase of hole mobility is the decrease of in-plane hole effective mass induced by applied stain and the decrease of intervalley scattering rate [17]. Note that the contribution on band splitting in comparison to band warping in the hole mobility enhancement at low stress level (<1 GPa) is negligible, due to the higher Si phonon energy (60 meV). Hole intervalley scattering is not significantly reduced for stress less than 1 GPa since the band splitting is less than the optical phonon energy. Thus, for holes, only mass change due to band warping and repopulation plays a significant role at today's manufacturable (<1 GPa) stress level since strain induced valence band splitting is smaller than that for the conduction band. In conclusion, the reduction of the effective mass of holes is more dependent on the valence band warping rather than valence band splitting [11]. The valence band warping induced by applied strain plays a crucial role in the improvement of hole mobility. During the implementation of strain technology, specific strain techniques applied to PMOS

devices, which can induce compressive strain parallel to the channel direction, is effective to improve hole mobility. For instance, integration of highly strained SiGe in source/drain is quite effective for the performance enhancement of PMOS devices.

### 2.2.3 *Effect of Strain Direction on Mobility Improvement*

For NMOS and PMOS devices, different types of strain for carrier mobility enhancement should be applied along in-plane channel direction, since the strain applied along different directions has different effects on channel mobility improvement. For NMOS devices, the carriers are electrons, and the applied strain leads to the splitting of silicon energy valley which can populate the distribution of electrons in  $\Delta_2$  valley. Many types of stress increase the electron mobility via increased population in the  $\Delta_2$  valley; in-plane biaxial and uniaxial tensile and out-of-plane uniaxial compressive stress are some examples. Table 2.1 summarizes the types of strain that enhance carrier mobility along all directions of MOSFETs [18].

The number of “+” in the table indicates that strain applied in the corresponding direction is more effective to improve carrier mobility. If the opposite strain is applied in the same direction, carrier mobility enhancement can't be obtained, and it will degrade the mobility. In addition, it can be seen from the table that the effect of strain on mobility improvement along different directions is also different, and the difference is obvious. The compressive stain perpendicular to the channel plane and the tensile strain parallel to the in-plane channel direction can effectively enhance electron mobility, whereas the compressive strain parallel to the channel direction is more effective in increasing hole mobility.

Therefore, application of strained silicon technology can enhance the hole mobility, which is beneficial for the mobility match between electron and hole, thereby further optimizing the size ratio between NMOS and PMOS devices in CMOS circuits and improving the CMOS performance.

**Table 2.1** Types of strain required for carrier mobility enhancement

Direction of strain change	NMOS	PMOS
Plane parallel to channel direction (longitudinal)	Tensile strain (+++)	Compressive strain (++++)
Plane perpendicular to channel direction (transverse)	Tensile strain (++)	Tensile strain (+++)
Perpendicular to channel plane (out-of-plane)	Compressive strain (++++)	Tensile strain (+)

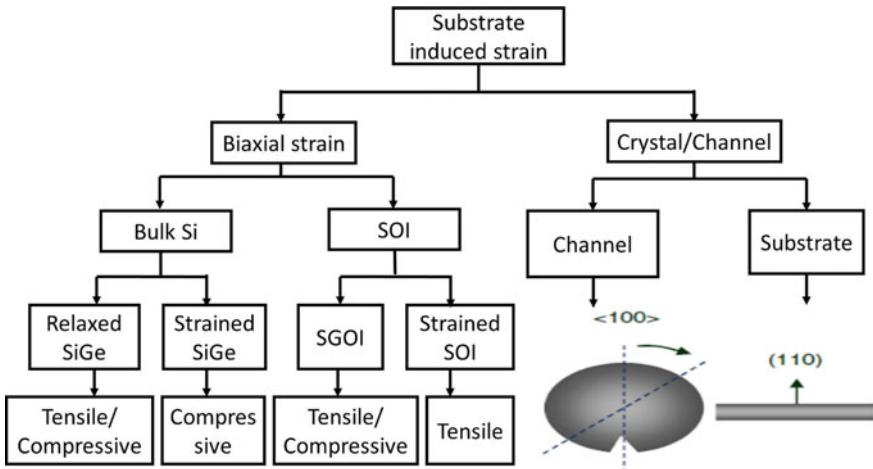
## 2.3 Classification of Strain Techniques

There are various approaches to introduce strain into the channel of MOSFETs, which can be realized by different substrates and different process techniques. According to the area where strain is introduced, strain techniques can be classified into two categories, including global strain and local strain. Substrate-induced strain is one type of global strain technique. Besides, strain techniques can be categorized according to the direction where strain is applied, including biaxial strain and uniaxial strain. Process-induced strain engineer technology is one of the main strain techniques for integrated circuit manufacturing. The type of applied external strain can be categorized into tensile and compressive strain. Different types of external strain should be applied in accordance with the strain enhancement mechanism in the channel region for NMOS and PMOS devices.

### 2.3.1 Substrate-Induced Strain

The substrate-induced strain is a technique form a uniform strained layer over the entire substrate. The strain technique used earlier in CMOS integration is to epitaxially grow a SiGe ‘buffer layer’ with a certain Ge composition on top of the silicon substrate as the strain relaxed buffer (SRB) [10, 19, 20]. Then a thin layer of strained silicon is grown on top of the SRB SiGe film. In order to improve the surface roughness, the surface of the SRB layer is treated with chemical mechanical polishing (CMP) [21]. Due to the larger lattice constant than silicon, the silicon layer grown in the top is subject to undergo biaxial tensile strain. Rim et al. [20] reported that the carrier concentration in the top grown silicon layer varies with different Ge compositions of SiGe film. For the SRB layer and the fully strained epitaxial silicon film, the biaxial tensile strain in the silicon channel also increases as the Ge composition increases in SRB layer, and the electron mobility is enhanced accordingly. When the Ge composition reaches 28% in the SRB, a 110% enhancement in the electron mobility is observed in the strained Si. However, the hole mobility is more complicated than that of electron. When the Ge composition is <13%, no significant improvement is observed in the hole mobility. Meanwhile for the Ge composition in range of 28 and 35%, the hole mobility can be significantly improved. The Ge component can be increased up to 45%. However, the increase ratio of hole mobility rapidly decreases as the effective electrical field is strengthened.

Another type of global strain technique combined with SOI technology is to implement different strained and high mobility materials on-insulator substrates (XOI) [22], including strained silicon directly on insulator (SSDOI) and heterostructure on insulator (HOI). The formation of such a strained substrate is generally realized by bonding technology. This occurs when an insulating layer (for example, a  $\text{SiO}_2$  film) is grown on a wafer substrate, and a thin layer of strained material is epitaxially grown on another wafer. Then the two wafers are bonded together and the strained layer



**Fig. 2.3** Classification of substrate-induced strain techniques

on insulator is finally formed by backside thinning or the delamination method. In order to eliminate the impact of the fully relaxed buffer layer in the SSDOI structure, epitaxial growth of strained SiGe layer on the basis of this buffer layer can be much more compatible with CMOS processes [23, 24].

Carrier mobility enhancement can also be realized by implementation of substrates with specific crystalline orientations. An optimum device technology for performance improvement would consist of NMOS lying in the (100) plane with high electron mobility and PMOS lying in the (110) plane with high hole mobility [25, 26]. During the integration of CMOS device on silicon wafers with a (100) surface orientation, the transistor layout of PMOS can be designed using (110) surface orientation on the wafer. Therefore, the carrier mobility of the NMOS and PMOS devices is enhanced simultaneously, which facilitates CMOS integration. Figure 2.3 shows classification of substrate-induced strain techniques.

### 2.3.2 Process-Induced Strain

Process-induced strain is the main method for strain engineering in modern sub 90 nm CMOS integration. Different processes can be utilized to generate appropriate strains for NMOS and PMOS devices to enhance carrier mobility. Key process-induced strain techniques are illustrated as follows:

- (1) **Stress memorization technique (SMT):** SMT was first proposed by Ota et al. at IBM [27]. The main process of SMT is to deposit a  $\text{Si}_x\text{N}_y$  capping layer with high tensile strain on top of the polysilicon gate of NMOS device with gate length of ~55 nm. Afterwards, an annealing step which can transfer strain

from the capping layer to the channel is performed to enhance the electron mobility for device performance improvement. During the annealing process, the polysilicon gate tends to recrystallize and the  $\text{Si}_x\text{Ny}$  tensile stressor on top of the gate tends to shrink, which can produce tensile strain along the channel direction and thus enhance the electron mobility [28–30]. The strain magnitude for SMT mainly depends on the dose of pre-amorphization implantation (PAI) for polysilicon, the thickness of the capping film as the stressor and variation of strain before and after annealing process [29, 31, 32].

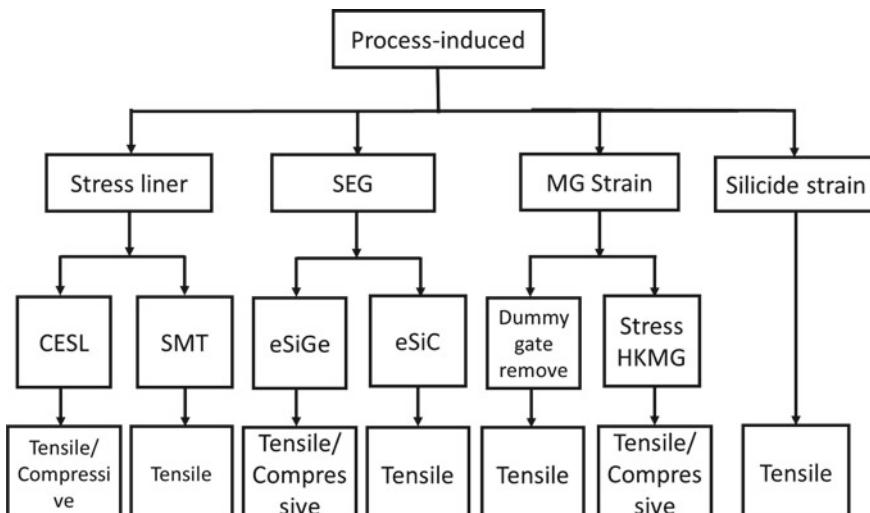
- (2) **Dual stress liner (DSL):** DSL process is the further development of contact etch stop layer (CESL) strain engineering technology. Ito et al. once studied the mechanism of CESL strain technique [33, 34], and thereafter IBM has successfully fabricated devices with the integration of DSL process in the 45 nm technology nodes [35]. For short channel devices, a CESL film on top of the gate electrode with residual tensile strain produces tensile strain parallel to the channel direction and exerts a compressive strain in vertical to the channel plane, therefore a net gain in electron mobility is achieved for NMOS devices. On the contrary, a CESL film covering the gate electrode with residual compressive strain produces a compressive stress parallel to the channel direction which is beneficial for PMOS device carrier enhancement. Therefore, the implementation of tensile silicon nitride liner for NMOS and compressive silicon nitride liner for PMOS can improve CMOS device performance during process integration [35]. The magnitude of mobility enhancement resulted from DSL is a function of: the growth conditions of silicon nitride film with high stress level and its thickness, as well as the gate height and the transistor spacer width [36–38]. Lately, some reports have integrated diamond-like carbon (DLC) film with extremely high stress level of (>6 GPa) instead of silicon nitride film for PMOS devices, which can also improve device performance efficiently [39].
- (3) **Strain engineering on S/D regions:** The S/D strain engineering is realized by epitaxial growth of heterostructures in S/D regions of the device which can induce uniaxial strain to the channel. At sub-90-nm nodes, selective epitaxial growth of SiGe films was used to fill the S/D-recessed regions to create uniaxial compressive strain in the channel region, which improves the hole mobility [5]. SiGe has a larger lattice constant than silicon. Thus, the lattice mismatch between SiGe and Si, which has a squeezing effect on the channel, produces the compressive strain in PMOS devices. While for NMOS device, selective epitaxial growth of SiC films in S/D was used. SiC has a smaller lattice constant than silicon. Thus, the lattice mismatch between SiC and Si produces a tensile strain in the channel, which improves the mobility of electrons [40].
- (4) **Silicidation in S/D induced strain:** The formation of silicide also induces tensile strain parallel to the channel direction. The magnitude of the induced strain depends on several factors, such as the type of silicide, silicide film thickness and process conditions etc. [41, 42].
- (5) **Shallow trench isolation (STI):** Filling the STI gap for small-sized MOSFETs with e.g.  $\text{SiO}_2$ , can also induce local biaxial compressive strain to the channel.

The SiO<sub>2</sub> filler with high coefficient of thermal expansion tends to expand horizontally, inducing local biaxial compressive strain to the channel.

- (6) **Metal gate induced strain (MGIS):** Metal gate induced strain can only take effect during process integration of small-sized MOSFETs, especially for the gate-last process integration. After dummy gate removal, deposition of highly strained HKMG material in the gate trench is performed to induce proper stress to the channel [43–45].

The above-mentioned methods which can induce strain in device channel are all local strain techniques. Normally, it is necessary to consider the magnitude of device performance improvement for the chosen technique as well as its feasibility for process integration, when selecting the strain engineering technique. And to ensure device performance enhancement, more than one strain engineering techniques are usually selected simultaneously. In addition, different strain engineering techniques should be implemented for NMOS and PMOS devices respectively. The strain engineering techniques that are currently used in mass production include embedded SiGe in S/D or silicon nitride capping layer with compressive strain for PMOS, as well as silicon nitride capping layer with tensile strain for NMOS and metal gate induced strain. However, embedded SiC in S/D for NMOS is still under development and can't be applied for mass production. Embedded SiGe in S/D has been widely used to improve PMOS performance. Various process-induced strain techniques and the corresponding induced strain parallel to the channel direction are summarized in Fig. 2.4.

Among the group of process-induced strain techniques, embedded SiGe in S/D for PMOS devices has received particularly attention due to its good compatibility



**Fig. 2.4** Classification of process-induced strain techniques

with traditional silicon-based processes, low cost, significant effect on device performance improvement, and wide applications. The application of embedded SiGe in S/D for PMOS is not only beneficial for hole mobility enhancement, but also excellent for the improvement of device transconductance and drive current, as well as the reduction of series resistance ( $R_{SD}$ ), channel resistance, electro-static discharge (ESD), etc. Moreover, integration of strained SiGe film can also efficiently improve device performance for some other devices with sophisticated structures, such as UT-SOI, MuGFET, FinFET, etc., and nanoscale devices at sub-22 nm nodes. SiGe strain engineering has been considered as one of the key technologies for advanced CMOS integration. Therefore, it is worthwhile to carry out the necessary research on SiGe strain engineering technology.

## 2.4 Summary

This chapter first claims the important role that strained silicon technology has played in CMOS integration. Strained silicon technology is one of the key technologies to continue the trend of “Moore’s Law”. Strain engineering for silicon in transistors is discussed in depth. The mechanisms of carrier mobility enhancement by virtue of strain engineering are explained in detail. Various strain engineering methods in silicon as well as the relevant research and application status are also summarized. Finally, the process-induced strain techniques for CMOS integration are introduced. Embedded SiGe in S/D for PMOS devices is a typical process-induced strain technique and has been widely used in mass production owing to its low cost, significant effect on device performance improvement and good compatibility with traditional silicon-based processes. Thus, we mainly studied the integration of SiGe on S/D regions in the following chapters.

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# Chapter 3

## Epitaxial Growth of SiGe Thin Films



This chapter introduces the research about SiGe growth as well as kinetic mechanism and different growth methods with a focus on reduced pressure chemical vapor deposition (RPCVD) technology. The selective epitaxial growth of high quality strained SiGe films has been studied in detail, and key factors affecting the epitaxial quality and strain for epitaxial grown films has been investigated.

### 3.1 Introduction

In the 1950s, research on SiGe thin films was already reported [1]. In 1957, H. Kroemer proposed the application of SiGe thin films in heterojunction bipolar transistors [2]. In the beginning, it was difficult to grow high-quality SiGe thin films due to large lattice mismatch between Si and Ge atoms, therefore the subject for SiGe thin films was remained in the status of theoretical research and different experimental attempt. In 1975, high quality SiGe films with fully strain and low defect density was deposited by using molecular beam epitaxy (MBE) [3]. In 1986, IBM's applied ultra-high vacuum chemical vapor deposition (UHVCVD) technique and successfully fabricated SiGe heterojunction bipolar transistor (HBT) [4]. With the rise of strained silicon technology since 2000, ASM (Advanced Semiconductor Materials) and Applied Materials (AMAT) have released their reduced chemical vapor deposition (RPCVD) technology for thin film growth, respectively, and thereafter selective epitaxial growth of SiGe thin film for mass production of integrated circuits was realized.

### 3.1.1 SiGe Crystal Structure and Strain

Both Si and Ge are group-IV elements in the periodic table, and they have four valence electrons located in the outermost atomic layer. The atoms in Si or Ge single-crystal with diamond lattice structure are bonded together via covalent bonds. The lattice constants for Si and Ge single-crystals are 5.431 Å and 5.658 Å, respectively. When a fraction of Ge,  $x$  is alloyed with Si to form  $\text{Si}_{1-x}\text{Ge}_x$  crystal at room temperature, the lattice constant of the  $\text{Si}_{1-x}\text{Ge}_x$  crystal can be determined from Eq. 3.1 according to Vegard's law [5]:

$$a_{\text{Si}}(x) = a_{\text{Si}}(1 - x) + a_{\text{Ge}} \cdot x = 5.431 + 0.227x \left(\text{\AA}\right) \quad (3.1)$$

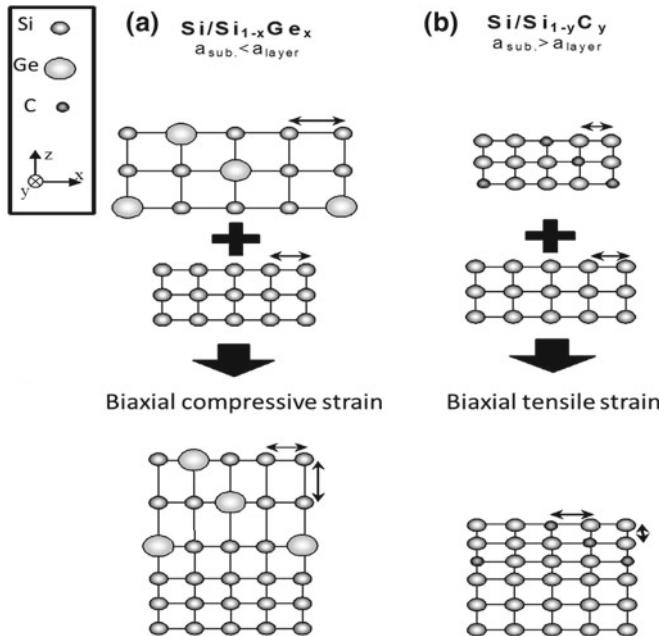
The lattice mismatch between Si and Ge is about 4.2% at room temperature [6], and the total lattice mismatch ( $f$ ) between  $\text{Si}_{1-x}\text{Ge}_x$  crystal and Si can be expressed by the following linear relationship:

$$f = (a_{\text{SiGe}} - a_{\text{Si}})/a_{\text{Si}} = 0.042x \quad (3.2)$$

Equation 3.1 shows the mismatch ratio between  $\text{Si}_{1-x}\text{Ge}_x$  crystal and Si substrate is proportional to the Ge content. If the Ge content is in moderate level, the lattice mismatch in the heterogeneous film induces stress when the SiGe film is epitaxially grown on Si in Fig. 3.1a. Since the Ge has a larger lattice constant than Si, biaxial compressive strain is generated on the plane of the SiGe film. While C has smaller lattice than Si then SiC film epitaxial grown on the Si substrate, it produces biaxial tensile strain.

However, when the Ge content increases to relatively high, the lattice mismatch between the  $\text{Si}_{1-x}\text{Ge}_x$  layer and the Si substrate is increased and finally is relaxed. When the induced strain relaxes, the dislocation density is increased.

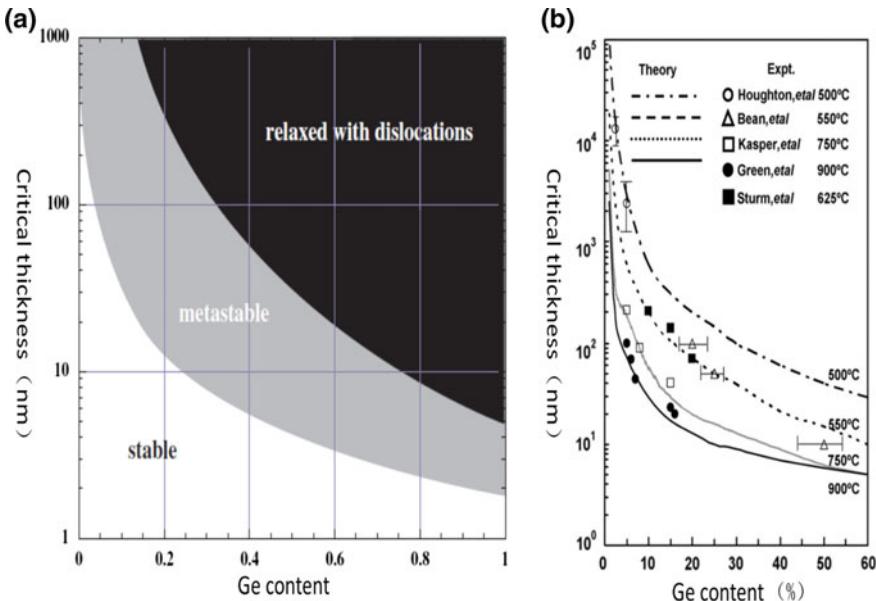
The  $\text{Si}_{1-x}\text{Ge}_x$  film grown on Si substrate is pseudo-morphic. The tetragonal distortion in the film growth direction destroys the cubic symmetry of the crystal, which leads to a split in the valence band energies and the degenerates also the conduction band. The tetragonal crystal is in a metastable state and has the tendency of elastic deformation. Previously, MBE method demonstrated the  $\text{Si}_{1-x}\text{Ge}_x$  films are grown in three-dimensional islands at high growth temperatures. Thus, the surface of the obtained  $\text{Si}_{1-x}\text{Ge}_x$  film is rough and undulate. Meanwhile, when the  $\text{Si}_{1-x}\text{Ge}_x$  film is grown under low temperature, the kinetics of stress release and crystal structure destruction will be inhibited. The key parameter for kinetic inhibition is the precise control of Ge content. Therefore, the growth of SiGe/Si heterojunction structure with high Ge content and smooth surface depends strongly on the growth temperature, which effectively promote the two-dimensional (2D) growth and suppresses the formation of three-dimensional (3D) islands.



**Fig. 3.1** Different strain types for **a** SiGe and **b** SiC films epitaxial grown on Si

### 3.1.2 Critical Thickness

The thickness and Ge content of SiGe thin films are two important factors to be considered. The epitaxial growth of SiGe film with a certain Ge content is not susceptible to influence the silicon substrate because of the relatively large silicon thickness. However, the initially grown SiGe film which is close to the SiGe/Si interface shows pseudo-morphic to adapt to the lattice constant of silicon substrate. When the thickness of the SiGe film exceeds a critical value, the strain energy accumulated within SiGe becomes too large to maintain the local lattice equilibrium for SiGe and Si atoms. Therefore, the strain will be released, forming the misfit dislocation. The atom arrangement on both sides of the SiGe/Si heterojunction interfaces will be dislocated, and the SiGe film becomes relaxed and the strain are decreased. The value of the film thickness is called “critical thickness” [7]. Dislocations occurred in SiGe films after strain relaxation (see Fig. 3.3b). With the increment of Ge content and growth temperature, the “critical thickness” of SiGe film decreases accordingly [8, 9]. Figure 3.2a shows the relation between the critical thickness of SiGe film epitaxially grown on Si and its Ge content given by Matthews and Blakeslee [10] and three different states during the strain process are also schematically shown. Figure 3.2b especially illustrates the impact of epitaxial growth temperature on the critical thickness of SiGe film [11, 12].

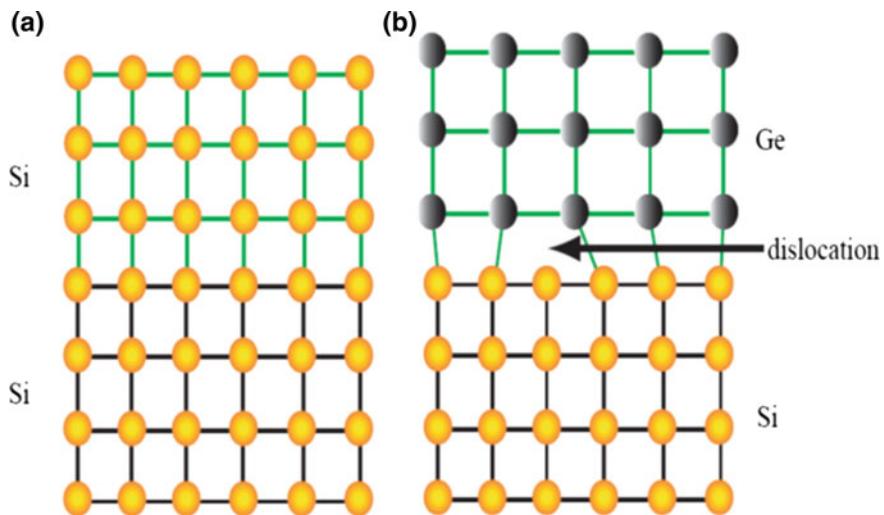


**Fig. 3.2** Impact of **a** Ge content and **b** epitaxial growth temperature on critical thickness of SiGe growth on Si [10–12]

### 3.1.3 Epitaxy and Its Main Growth Techniques

Epitaxy is the growth of a thin single crystal film known as the epitaxial layer on a single crystal substrate by introducing necessary sources for synthesis reaction. According to the types of materials for epitaxial layer compared to the substrate material the epitaxy can be classified in two major categories: homoepitaxy, which means that the epitaxial material is the same as the substrate material (see Fig. 3.3a); the other case is called heteroepitaxy, which means that the epitaxial material is different from the substrate material, such as the growth of Ge or III–V materials on silicon substrate (see Fig. 3.3b). It should be noted that heteroepitaxy has been widely employed in mass production of integrated circuits.

At present, the main SiGe epitaxial growth techniques can be classified into two categories: MBE and CVD. MBE is an advanced technique for crystalline thin films growth. During the reaction process, the required particles are obtained by thermal evaporation or electron beam excitation treatment for the precursor molecules. Then the obtained particles are accumulated onto a substrate with suitably heat treatment for epitaxial growth. MBE can realize ultra-thin SiGe film growth under low temperature. However, MBE equipment is normally designed for monolithic wafer-scale processing, which requires high vacuum and exhibits lower output. Besides, MBE equipment is expensive, and its cost for maintenance and precursor supplement are also unacceptable for mass production. Therefore, MBE technology is not suitable for

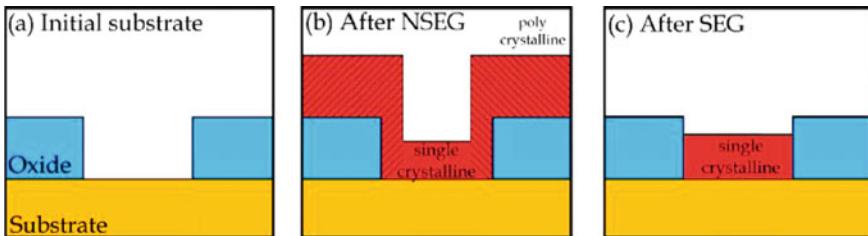


**Fig. 3.3** Schematic structures for **a** homoepitaxy and **b** heteroepitaxy

large-scale manufacturing applications. The epitaxial growth of SiGe material under low temperature along the whole process flow can be realized by CVD technique, which can also avoid the deformation of the substrate pattern during the surface cleaning process. Among the feasible CVD techniques, ultra-high vacuum CVD (UHVCVD) requires the equipment to maintain high vacuum and low growth temperature. The epitaxial growth rate for UHVCVD is still very slow. Thus, UHVCVD is preferable for the epitaxial growth of ultra-thin films. While for RPCVD, it has the capability for mass production, and the relevant process equipment is simple and easy for maintenance. Therefore, selective epitaxial growth of SiGe film by RPCVD is suitable mass production of integrated circuits.

In addition, according to the manner in which atoms are transferred to the substrate, epitaxial growth can be classified into three types, including vapor phase epitaxy (VPE), liquid phase epitaxy (LPE), and solid phase epitaxy (SPE). Liquid phase epitaxy and solid phase epitaxy are just suitable for the preparation of substrates, but not suitable for device integration. Vapor phase epitaxy technology is mature and can control the film thickness, impurity concentration and crystal integrity, so it keeps on playing an important role in silicon process.

According to the pressure control and vacuum level during CVD gas-phase reaction, vapor phase epitaxy can be classified into: (1) atmospheric pressure chemical vapor deposition (APCVD); (2) reduced pressure chemical vapor deposition (RPCVD) at reaction pressures of a few Torr; (3) low pressure chemical vapor deposition (LPCVD) at reaction pressures of a few mTorr and below; (4) ultra-high vacuum chemical vapor deposition (UHVCVD) with tight pressure control and high vacuum level.



**Fig. 3.4** **a** Starting surface for epitaxial growth. Schematic structures of **b** non-selective epitaxy and **c** selective epitaxy

### 3.1.4 Non-selective Epitaxy and Selective Epitaxy

The growth regions for SiGe films on a single crystal substrate are some opening windows (see Fig. 3.4a), which are previously defined by dielectric masks (e.g., SiO<sub>2</sub> or SiN). Then the epitaxial grown films are formed on both the single crystal substrates and the dielectric layers (see Fig. 3.4b). This epitaxy approach is called non-selective epitaxy growth (NSEG). The obtained SiGe films by NSEG are classified into two types: one is single crystal SiGe film grown in the single crystal substrate, and the other is polycrystalline SiGe grown on the surface of the dielectric films (e.g., SiO<sub>2</sub> and SiN). For selective epitaxy (SEG), etching gas (HCl) is introduced during epitaxial growth. By adjusting the ratio between HCl and other reaction gases, the etching rate of HCl on the deposited polycrystalline SiGe film is greater than that on the single crystal SiGe film. Then the selective epitaxy growth of the single crystal SiGe is completed, as shown in Fig. 3.4c. Selective epitaxy is mainly implemented in SiGe source/drain strain engineering for integrated circuits.

## 3.2 SiGe Selective Epitaxy Using RPCVD Technology

### 3.2.1 RPCVD Equipment

RPCVD is the most commonly used technology for Si and SiGe epitaxial growth in current industrial production. There are two kinds of equipment provided by two manufacturers majoring in selective epitaxy technique for integrated circuit fabrication, including AMAT's reduced pressure chemical vapor phase epitaxy equipment and ASM's single-chip reduced pressure epitaxy equipment. Both companies have introduced their own equipment with different design features and merits for Si/SiGe selective epitaxy. Anyhow, the equipment provided by the two companies for 300 mm wafers is more advantageous than counterparts for 200 mm wafers. With the integration of pre-treatment processes prior to epitaxy for AMAT's equipment, the remaining natural oxide on the wafer surface can be removed under low temperature, which

can effectively reduce the thermal budget during device integration. Compared with AMAT's equipment, the chambers of ASM's equipment are available for epitaxy over a wider temperature range, which can provide some flexibility for research purpose. With the consideration of the research purpose and the experimental conditions of our laboratory, we selected ASM E2000 plus for the research work of SiGe film growth.

The ASM E2000 plus RPCVD equipment is a specific equipment for selective epitaxial growth of SiGe films for industrial fabrication on 200 mm wafers. The air pressure of the chamber is precisely controlled by a dry pump group. The whole equipment consists of a load-lock chamber, a buffer chamber and a process chamber for epitaxy. The wafer passes through the load-lock chamber and the buffer chamber to the process chamber. There are two sets of heated quartz halogen lamps located in the upper and lower sides of the process chamber. A graphite base for wafer placement is located at the center of the process chamber. The reaction gas enters the process chamber from the front side and is discharged from the back side. The equipment uses the design of an independent reaction chamber design and a single-wafer processing system, which is compatible with 4–6 in. wafer. In the process chamber, the reaction gas enters the process chamber in laminar flow to ensure uniformity of the reaction for epitaxial growth. The equipment can also realize *in situ* high-gradient-doping level. The residual gas after the epitaxy is collected by the exhaust gas treatment equipment and discharged to the factory for centralized processing.

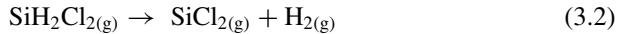
The pressure and temperature control of the process chamber should be quite precise, because the temperature determines the adhesion coefficient of the reaction gas and the pressure determines the growth rate of SiGe film. During the film growth process, the wafer is fixed on a susceptor in a quartz chamber, and is heated by the radiation from halogen lamps above and below the process chamber, so we can rapidly rise and reduce the temperature in the range between 400 and 1200 °C. The temperature in the chamber is monitored by four thermocouples in real-time. The flow rate of the precursor gas and the carrier gas is controlled by a series of massflow controller. The process control valve (PCV) can also control the gas pressure in the process chamber to control the gas flow rate during the entire epitaxial growth process, thereby adjusting the growth rate of SiGe film.

### ***3.2.2 Epitaxial Growth of SiGe Films***

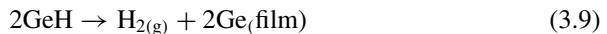
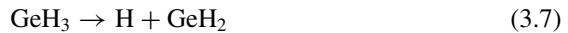
During the epitaxial process of SiGe thin films, the precursors corresponding to Si are SiH<sub>4</sub>, Si<sub>2</sub>H<sub>6</sub>, SiH<sub>2</sub>Cl<sub>2</sub> (DCS), SiHCl<sub>3</sub> and SiCl<sub>4</sub>; and the precursors corresponding to Ge are GeH<sub>4</sub> and Ge<sub>2</sub>H<sub>6</sub>, which are diluted by H<sub>2</sub> to a certain concentration. If p-type or n-type *in situ* doping is required, the dopants that can be utilized are B<sub>2</sub>H<sub>6</sub> and PH<sub>3</sub> (AsH<sub>3</sub>) diluted in H<sub>2</sub>. The selectivity of SiGe selective epitaxial growth is mainly achieved by the utilization of HCl gas, which is introduced as a cleaning gas for the quartz chamber by cleaning up the film accumulated on the chamber surface. The dilute protective gas, such as N<sub>2</sub> and H<sub>2</sub>, is required throughout the entire reaction

process. To avoid oxygen contamination induced by water vapor which can affect the quality of the SiGe film, the HCl, N<sub>2</sub> and H<sub>2</sub> used in the reaction process must undergo a purifier before entering the chamber.

Since the integration of SiGe in source/drain is performed by a selective epitaxy process. The precursor corresponding to Si is SiH<sub>2</sub>Cl<sub>2</sub> (DCS), and the precursor corresponding to Ge is 10% GeH<sub>4</sub> mixed with H<sub>2</sub>. The selective etchant is HCl vapor, and H<sub>2</sub> is used as a diluent gas during the high-temperature reaction. The chemical equations for the reactions occurred during the epitaxy process are listed as follows:



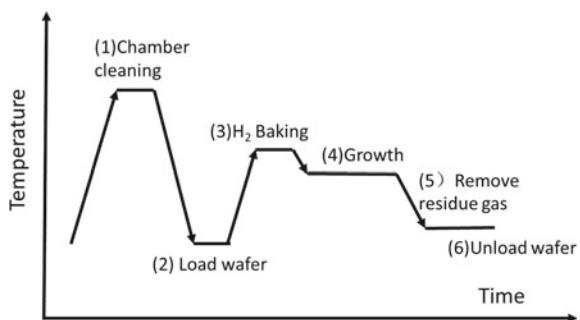
The chemical equations for the reaction of GeH<sub>4</sub> during epitaxy are listed as follows:



H<sub>2</sub> is a very important gas during the reaction process. It is utilized as the surfactant to ensure the flatness of the epitaxial layers. Besides, H<sub>2</sub> can also reduce the surface free energy and change the diffusion of the atoms at the surface and step, thereby improving the quality of epitaxial grown film. In addition, under low temperature, the growth rate is limited by the desorption rate of H atoms, which can also affect the SiGe epitaxial growth rate. The desorption rate of H atoms affects the decomposition of DCS and GeH<sub>4</sub>. Epitaxial growth can only be achieved when DCS and GeH<sub>4</sub> are decomposed.

In our experiments, the substrate was first cleaned to remove possible organic contamination and particles. The standard cleaning process for the integrated circuit are following: At first, the SPM was used for 10 min at 120 °C to remove the organic

**Fig. 3.5** Schematic diagram of the SiGe epitaxy process



contamination on the surface of the silicon wafer. After being rinsed in the deionized water for 5 min, the wafer was rinsed in APM solution for 10 min to remove the surface particles. After being rinsed in the deionized water for another 5 min, the wafer was rinsed with HF solution (100:1) for 60 s, dried up and then quickly loaded into the processing chamber for epitaxial growth. Finally, an oxide layer without metal ions and organic impurities is formed on the surface of the silicon wafer after an HF rinse. This oxide layer should to be removed in situ in the process chamber before epitaxial growth of single crystal SiGe on the surface of silicon substrate. The main processes in the chamber are listed as follows:

- (1) Cleaning the process chamber by H<sub>2</sub> and HCl (For low pressure epitaxy, high vacuum is required);
- (2) Transferring the wafer into the process chamber after the wafer cleaning by removing organic contamination and surface particles;
- (3) Heating up the wafer to the baking temperature to remove the surface oxide (The baking temperature is dependent on the type of substrate);
- (4) Lowering the temperature to the epitaxial growth temperature and introducing the precursor gases for Si, Ge and dopant for the growth of desired films;
- (5) Blowing away the excess reaction gases and by-products by introducing H<sub>2</sub>;
- (6) Removing the silicon wafer after the cooling-down process;
- (7) The key process steps in the process chamber are shown in Fig. 3.5.

### 3.3 Characterization of SiGe Films

In this section, we mainly studied the parameters of the epitaxial grown SiGe films, such as film thickness, crystal quality, Ge content and distribution, strain relaxation and surface roughness. The relevant characterization methods are X-ray diffraction (XRD), secondary ion mass spectrometry (SIMS), transmission electron microscope (TEM) and atomic force microscope (AFM). Based on these methods, the quality and strain of the SiGe film are analyzed and the optimal conditions for selective epitaxial growth are determined.

### 3.3.1 Analysis of SiGe/Si Interface

Among the various current-used techniques, SIMS is the most sensitive one for surface analysis. The test accuracy of SIMS is relatively high, enabling accurate measurement of target elements and their profile. SIMS is often carried out in SiGe epitaxy processes to determine the composition and dopant concentration. SIMS can also test and analyze the contents of C and O elements at the SiGe/Si interface which can be related to film quality.

The basic principle of SIMS is illustrated. The test sample is placed in an ultra-high vacuum atmosphere and the surface of the sample is bombarded with high-energy ion beam. Some of the ions which are bombarded by the high-energy ions and escape from the surface of the sample. These ions are defined as secondary ions. The mass of the generated secondary ions is then measured and analyzed by mass spectrometry, and the composition of the sample is obtained correspondingly. The SIMS test can measure the total concentration of atoms, but can't distinguish the distribution of interstitial atoms and substitutional ones. Therefore, the strain and defects in the SiGe films can't be characterized.

Two epitaxial SiGe samples (named as A and B) were prepared in two different chambers for SIMS characterization. As shown in Fig. 3.6, C and O impurity atoms were found to be presented at the SiGe/Si interface and inside SiGe film, and the concentrations for C and O atoms exceeded the standard value (less than  $1 \times 10^{18}$  atoms/cm $^3$ ). The concentration of O in the SiGe/Si interface and the inside films is higher than that of C. This test results show that the epitaxial grown SiGe film was seriously contaminated by O, which affects the film quality.

The SIMS analysis of sample B shows that the concentrations of C and O impurity atoms presented at SiGe/Si interface and inside SiGe film is remarkably lower. In particular, the concentration of O in SiGe film is  $1 \times 10^{17}$  atoms/cm $^3$ , which is lower

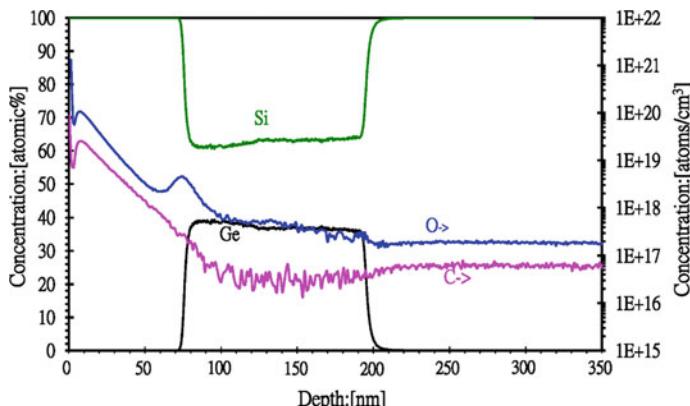
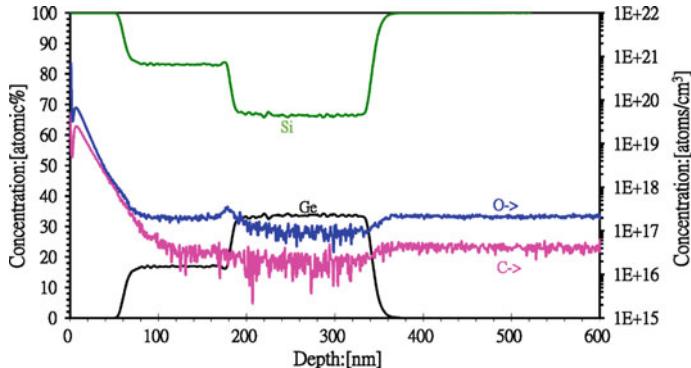


Fig. 3.6 SIMS profile of different elements in sample A



**Fig. 3.7** SIMS profile of different elements in sample B

than silicon substrate. The results indicate that the SiGe film is not contaminated by oxygen, and the film quality is better than sample A (Fig. 3.7).

The SIMS results show that the difference between A and B samples mainly is O contamination on the surface of sample A during the epitaxy process. The O contamination is caused by incomplete cleaning step of wafer surface. Therefore, the epitaxial growth of sample B was successful after a long time of influx, extraction and pre-flow of gases. In order to effectively suppress the influence of oxygen or water vapor during the growth of SiGe films and to ensure the film quality, HCl, H<sub>2</sub> and N<sub>2</sub> gases should be purified before entering the process chamber.

### 3.3.2 HRXRD Analysis of SiGe Films

X-ray diffraction (XRD) is the most important characterization method of strain in SiGe films. The thickness, composition, crystal quality (defects), strain/relaxation (mismatch) and doping of SiGe strained films can be obtained by XRD. For high quality SiGe multilayer film, the resolution of XRD for strain analysis is  $10^{-5}$  and the depth resolution is 0.1 nm. While for single-layer epitaxial SiGe film, the minimum thickness that can be analyzed is about 10 nm [13].

XRD instrument consists of X-ray tube with Cu target, quadruple crystal monochromator, slits, double crystal analyzer, and detector. The basic principle of XRD can be expressed in Bragg's Law (3.10):

$$2d \sin(\theta) = n\lambda \quad (3.10)$$

Here  $d$  is the distance between the parallel crystal planes,  $\lambda$  is the wavelength of the ray, and  $\theta$  is the angle between the incident beam and the crystal surface.

The main characteristic parameters of SiGe films can be measured by X-ray scanning of the crystal plane of the samples in the following two ways:

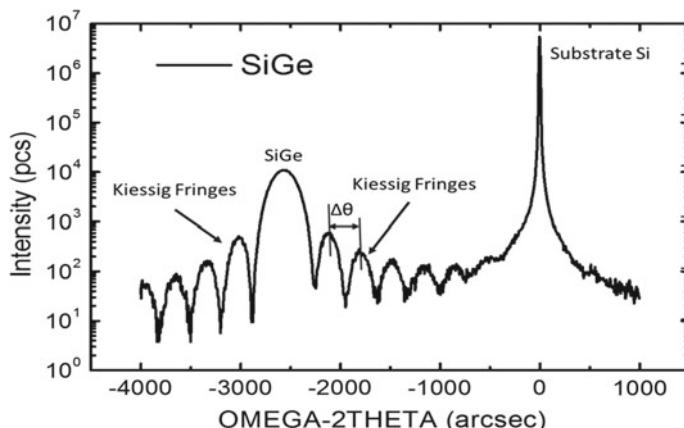
(1) Rocking curve measurement in (004) symmetry plane:

During XRD analysis, X-ray with an incidence angle  $\omega$  and a fixed  $2\theta$  scans different orientations of the crystal planes with fixed spacing. Meanwhile,  $\omega$ - $2\theta$  scan with a fixed scanning rate ratio can detect different orientations of the specific crystal planes. The spectra obtained by the  $\omega$ - $2\theta$  scan are called rocking curves (RCs). As shown in Fig. 3.8, the  $\omega$ - $2\theta$  scan of the intrinsic SiGe film grown by selective epitaxy produces two distinct peaks. One peak representing SiGe is located on the left, and the other representing Si substrate is located on the right.

The composition of SiGe thin films can be determined from the split angle between the SiGe and Si substrate peak in the XRD spectra. Because of the internal reflection at SiGe/Si interfaces, X-rays can cause interference in the epitaxial layer. This interference produces interference sub-peaks (Kiessig Frings) on both sides of the SiGe peak. The quality of the epitaxial SiGe interface can be indirectly characterized by the number of interference sub-peaks. The existence of dislocations and stacking faults caused by strain relaxation will affect the quality of SiGe films, and the number of interference sub-peaks on both sides of SiGe peak decreases in the corresponding XRD scanning curves. If the film is completely relaxed, there will be no obvious interference peaks. By measuring the distance between two adjacent sub-peaks, the film thickness ( $t$ ) of the strained SiGe film can be calculated by the following Eq. (3.11):

$$2\Delta\theta \cos(\theta) * t = \lambda \quad (3.11)$$

The analysis of XRD spectra shows that the SiGe film is strained. Besides, the film thickness is 61 nm, and the composition of Ge is 28%. There are clear interference sub-peaks on both sides of SiGe peak, and the epitaxial grown films have good interface quality.



**Fig. 3.8** Rocking curve of strained SiGe by XRD scanning in (004) plane

(2) Measurement of reciprocal lattice mapping in (113) asymmetric plane:

High resolution reciprocal lattice mapping (HRRLM) can be obtained by  $\omega$ - $2\theta$  scan with the incidence angle  $\omega$  in the range of  $\pm\Delta\omega$ . Reflections of HRRLM in (113) asymmetric surface is sensitive to defects in the films, and even a small number of defects can be characterized. Thus, HRRLM is suitable for strain and defect analysis in the applications of integrated circuits with SiGe devices. In HRRLM spectra, the position of epitaxial SiGe peaks relative to Si substrate peaks reveals the state of strain relaxation, and the defect density in the films can be obtained by analyzing the Full-Width-Half-Maximum (FWHM) of the peaks. The data obtained from the scanning spectra can be used to calculate the lattice mismatch along the vertical and parallel directions. The following two formulas can be used for the relevant calculations [14, 15]:

$$f_{\perp} = \frac{\sin \theta_s \cos(\omega_s - \theta_s)}{\sin \theta_l \cos(\omega_l - \theta_l)} - 1 \quad (3.12)$$

$$f_{\parallel} = \frac{\sin \theta_s \sin(\omega_s - \theta_s)}{\sin \theta_l \sin(\omega_l - \theta_l)} - 1 \quad (3.13)$$

The s and l in the formula represent the substrate and epitaxial layer, respectively.  $\perp$  and  $\parallel$  stand for the directions perpendicular and parallel to the growth direction. The lattice mismatch f can be expressed in Formula (3.14):

$$f = (f_{\perp} - f_{\parallel}) \frac{1 - \nu}{1 + \nu} + f_{\perp} \quad (3.14)$$

The  $\nu$  (0.278 for SiGe) in the formula is Poisson's ratio of SiGe in Si system [16]. HRRLM characterization of strain variation in SiGe thin films during process integration will be discussed in detail in the following chapters about SiGe device integration.

In summary, XRD detection of SiGe samples has the advantages of non-destructive and fast method with high measurement accuracy to be widely used to monitor Ge content and internal strain of strained SiGe films. However, the XRD technique for characterizing SiGe epitaxial films still has also some drawbacks. The diffraction peak position of the epitaxial SiGe film is limited by both Ge content and strain in the films. Once the thickness of the SiGe film exceeds the critical thickness, an accurate film information can't be obtained.

### 3.3.3 Surface Roughness of Strained SiGe Films

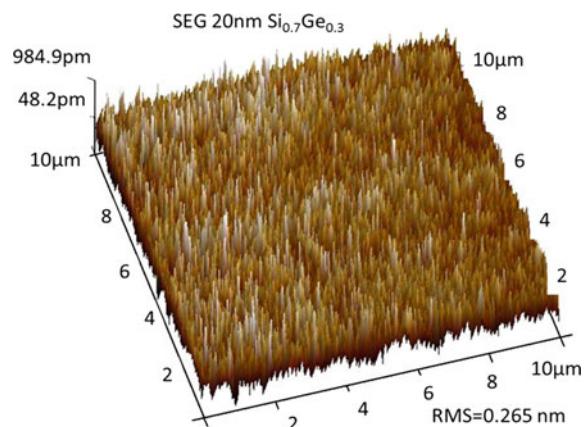
The SiGe film is affected by different processes and the surface properties vary greatly. Excessive growth temperatures produce three-dimensional island morphology and strain relaxation, resulting in rough surfaces for the epitaxial grown SiGe

film. If the growth temperature is too low, it is prone to generate defects or even amorphous morphology in the epitaxial films. The choice of epitaxial substrate and the method of pre-treatment, as well as the use of selective gases in the process, etc., will result in variation of surface quality. Therefore, there are many uneven peaks and valleys with very small amplitude and very close distance on the surface of SiGe thin film. As an attribute of surface fluctuation, surface roughness of thin film is the deviation between the surface of the film and the standard plane within a small value range. For epitaxial SiGe films, it is quite important to control the surface roughness because the actual device fabrication starts from thin-layer surface contact, and the surface characteristics are directly related to subsequent process integration and circuit performance. Therefore, surface roughness is also an important parameter to characterize the quality of SiGe crystals.

Atomic Force Microscopy (AFM) is an important test method for characterizing and analyzing the surface properties of strained epitaxial SiGe films. It can provide a reference for optimizing the process conditions. AFM is a kind of scanning microscope (SPM). By scanning the surface of the sample, three-dimensional image the sample surface can be obtained, and the analysis of surface structure, roughness, flatness, and defects can be performed. The main principle of AFM is to use a sharp and extremely thin tip to interact with the surface of the sample. The movement of the tip is monitored by reflecting the laser beam from the back of the cantilever to the photosensitive detector. A slight change of the cantilever will change the position of the beam monitored by the detector, and the position change of the reflected beam is then converted into a longitudinal movement of the tip.

In this research, Bruker's Dimension Icon AFM instrument is used. The working mode is light tapping, and the scanning range is  $10 \mu\text{m} \times 10 \mu\text{m}$  for surface analysis of the prepared sample. The results of the surface roughness analysis of SiGe films prepared by selective epitaxial growth (SEG) are shown in Fig. 3.9. In the film preparation, the temperature for selective epitaxy was  $650^\circ\text{C}$  and the reaction pressure was 20 Torr. The SiGe film was epitaxially grown on Si with a Ge content of 30%

**Fig. 3.9** Surface roughness analysis of selective epitaxial SiGe thin films

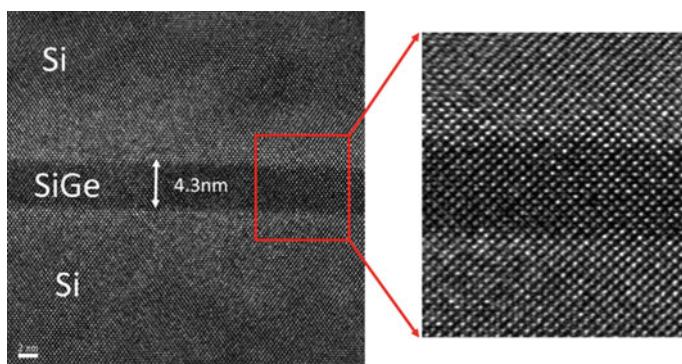


and a thickness of 20 nm. The surface roughness which is expressed in root mean square (RMS) for the sample is 0.265 nm by AFM analysis. The surface roughness of the films grown by selective epitaxy is very small, and the surface properties of the films are good. Thus, epitaxial grown films with high quality are obtained.

### 3.3.4 TEM Analysis of SiGe Films

Through the TEM analysis of epitaxial SiGe films, the microscopic observation and composition analysis of the films can be realized. TEM can be used not only to observe the lattice structure of SiGe and Si, but also to analyze the composition of elements in the films by energy dispersive X-ray detector (EDX). The basic principle of TEM is that the accelerated and aggregated electron beams are projected onto a very thin sample, and the electrons collide with the atoms in the sample to change the direction and produce scattering. Due to variations of sample thickness, lattice arrangement, density, etc., different shading images appear, and the signals are processed to form pictures on the display screen. TEM equipment structure mainly consists of four parts: electron source, electromagnetic lens system, sample holder and imaging system [17]. Typically, TEM has a resolution of 0.1 nm and a magnification of about a million times, and it can be used to observe very thin and tiny structures. Samples are processed and prepared before TEM imaging. Sample preparation is quite important for TEM imaging because electron transmission requires the sample to be “transparent” to electrons, that is, the sample can penetrate electrons. For SiGe, the thickness of the sample is required to be tens of nanometers or even a few nanometers, and sample preparation is performed by Focused Ion Beam (FIB) [18].

Figure 3.10 shows the TEM image of the epitaxial strained SiGe film. The Ge component is 28%, and the growth temperature is 650 °C. The interface between



**Fig. 3.10** TEM analysis of strained SiGe film

SiGe and Si is quite clear from the TEM image, and the lattices of SiGe and Si are perfectly matched, indicating that good quality of the epitaxial SiGe film.

### 3.4 Main Factors Affecting the Growth and Strain of SiGe Films

During selective epitaxial growth, it is necessary to select suitable process conditions to prepare a high-quality strained SiGe film, thereby meeting the requirements of device integration. This section mainly analyzes and discusses the main factors affecting the quality of SiGe selective growth and the film strain laying the foundation for integration applications.

#### 3.4.1 Experimental Process of SiGe Growth

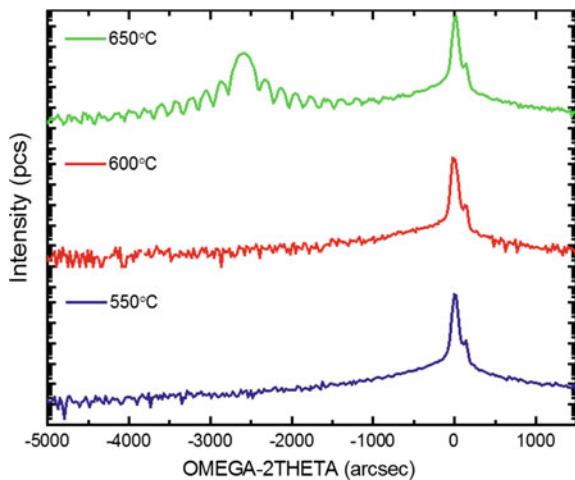
In the experiments on this work, RPCVD epitaxial equipment was used to selectively grow SiGe thin films under different process conditions, including the reaction temperature, total pressure, HCl gas consumption and different dopants. The Ge components in strained SiGe films were analyzed by XRD and the concentration of dopants was calibrated by SIMS.

#### 3.4.2 Influence of Reaction Temperature on the Strain of SiGe Films

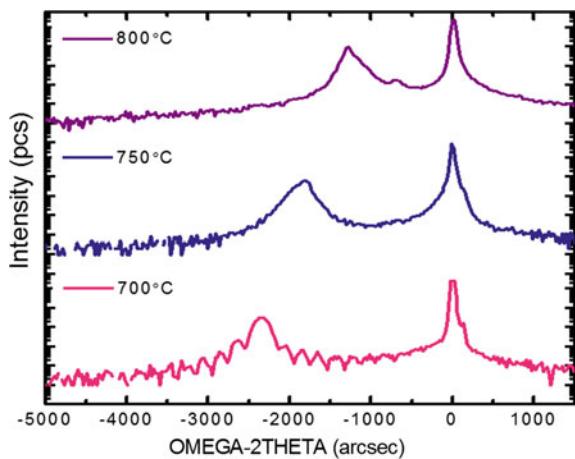
The selective epitaxial growth of SiGe film is sensitive to the reaction temperature, and the effect of HCl on the growth of SiGe films is different at low and high temperatures. In order to study the effect of different reaction temperatures on the selective epitaxial growth of SiGe, the same reaction gas flow rate and chamber pressure were set, and the SiGe films selectively grown at different reaction temperatures were analyzed by XRD. As shown in Figs. 3.11 and 3.12, no SiGe peak appeared in the XRD spectrum when the reaction temperature is 550 °C. This is because DCS is difficult to decompose at 550 °C. Moreover, HCl in the chamber inhibits the decomposition of DCS, which increases the difficulty of DCS decomposition. Therefore, SiGe films are hardly to be grown under such circumstance.

When the temperature rises to 600 °C, there is still no obvious SiGe peak in the XRD spectrum. When the temperature rises to 650 °C or 700 °C, the main peak of SiGe appears in XRD spectrums, and many obvious small interference peaks appear at both sides of SiGe peak, indicating the strain state and high-quality interface of the films. The SiGe growth rate under reaction temperature above 650 °C is higher than

**Fig. 3.11** XRD spectrums of SiGe films grown at 550, 600 and 650 °C



**Fig. 3.12** XRD spectrums of SiGe films grown at 700, 750 and 800 °C



that under reaction temperature below 600 °C. The strained Ge content in the film gradually decreases for temperatures above 700 °C. When the reaction temperature continues to rise above 750 °C, the interference peaks on both sides of the SiGe main peaks disappear. With the increase of reaction temperature, the position of SiGe peak comes closer to the Si substrate peak and the strained Ge composition continue to decrease. This is because the critical strain thickness for SiGe thin film with 20% Ge is only about 10 nm when the reaction temperature rises to 750 °C [9]. Rapid growth will make the thickness of the film quickly exceed the critical thickness. The strain in the film relaxes rapidly and the strained Ge composition measured by XRD also decreases.

**Table 3.1** Parameters for SiGe selective epitaxy processes under different temperatures

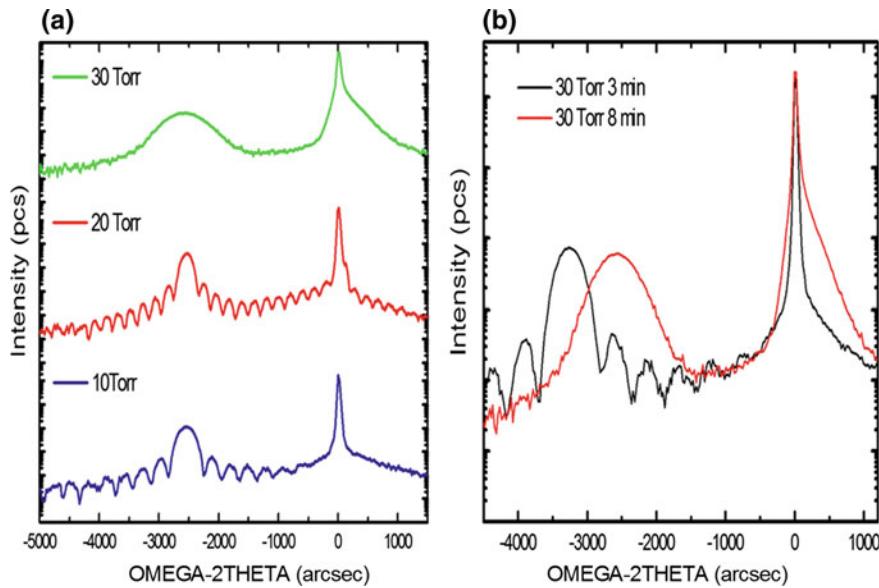
Temperature (°C)	SiGe thickness (nm)	Growth time (min)	Growth rate (nm/min)	Ge composition (%) measured by XRD
650	92	10	9.4	28.2
700	94	3	31	25.4
750	220	3	73	20.1
800	270	2	135	13.7

Because SiGe thin films can hardly grow at temperatures below 600 °C and there are no SiGe peaks in the corresponding XRD spectrums, the relevant process parameters are not listed in Table 3.1. According to the data in Table 3.1, it can be found that setting epitaxial growth temperature above 650 °C can lead to gradually increase of the deposition rate of SiGe, along with the decrease of strained Ge composition decreases and increase of defects in the films. This is because the growth rate depends on the concentrations and types of the reaction gases at high temperature. In addition, DCS and GeH<sub>4</sub> react rapidly to form SiGe, even if HCl etching is enhanced. At low temperature, the reaction rate depends on the decomposition rate of DCS. With the decrease of temperature, the decomposition of DCS becomes more difficult and the growth rate is relatively slow. Therefore, the experimental results show that the preferable reaction temperature for selective epitaxial growth of SiGe is between 650 and 700 °C. In order to retain high strain for SiGe film, the preferred reaction temperature is 650 °C. Meanwhile, the thickness of SiGe film for source/drain integration applications in CMOS devices is below 60 nm, which is less than the thickness of SiGe film in Table 3.1, so the density of defects will be much less.

### 3.4.3 Influence of Reaction Pressure on the Growth of SiGe Thin Films

The most direct effect of reaction pressure on the selective epitaxial growth of SiGe films is the growth rate. Selecting suitable reaction pressure is conducive to controlling the growth rate of SiGe film. To further investigate the effect of reaction pressure on the growth of SiGe films, the pressures in the process chamber were set as 10, 20 and 30 Torr, respectively, while keeping the same reaction temperature (650 °C) and other reaction conditions. From the XRD spectrums in Fig. 3.13a, it can be found that the thickness of SiGe film increases with the increase of pressure.

When the pressure is 30 Torr, the growth rate of SiGe is too fast and the thickness of SiGe film is too thick, resulting in strain relaxation beyond the critical thickness, so the interference peaks have been disappeared. When the growth time of SiGe is reduced from 8 to 3 min, the interference peaks appear again in Fig. 3.13b. In Table 3.2, the parameters for SiGe growth under different growth pressures and growth time are



**Fig. 3.13** **a** XRD spectrums for SiGe films grown under different pressure levels (10, 20 and 30 Torr), **b** and different growth time (3 min/8 min, 30 Torr)

**Table 3.2** Effect of different pressures on the growth of SiGe thin films

Pressure (Torr)	SiGe thickness (nm)	Growth time (min)	Growth rate (nm/min)	Ge composition (%) measured by XRD
10	64	8	8	27.2
20	94	10	9.4	28.2
30	110	8	13.8	27.8
30	42	3	14	34.9

summarized. Therefore, to control the growth rate of selective epitaxy and to meet the requirements of practical application, 20 Torr is selected as the total pressure in the chamber for selective epitaxial growth of SiGe.

#### 3.4.4 Influence of HCl Gas on the Growth of SiGe Films

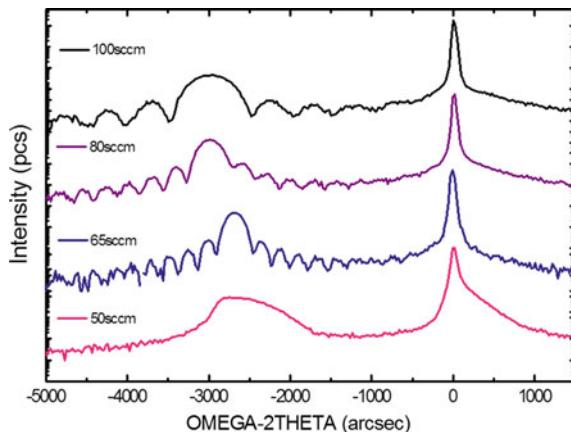
HCl gas is an etchant gas which is used to maintain the selectivity during SiGe epitaxial growth. In order to study the influence of HCl on the selectivity of SiGe films, the flow rate of HCl was set as 50, 65, 80 and 100 sccm, while other reaction conditions (growth temperature of 650 °C and total pressure of 20 Torr) remained

**Table 3.3** Effect of different HCl flow rates on the growth of SiGe films

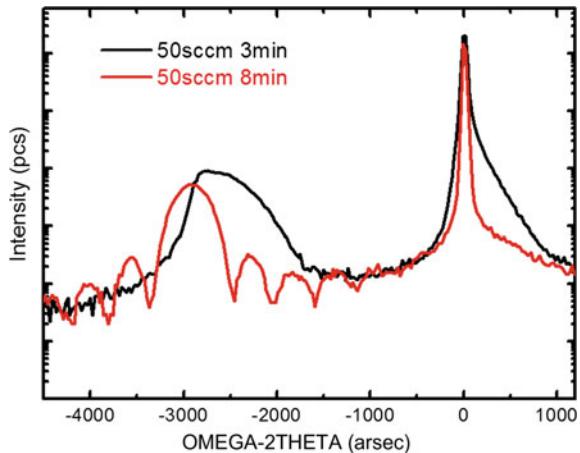
HCl flow rates (sccm)	SiGe thickness (nm)	Growth time (min)	Growth rate(nm/min)	Ge composition (%) measured by XRD
50	115	8	14.3	27
50	43	3	14.3	31.1
65	83	8	9.4	28.2
80	67	8	8.4	32
100	38	8	4.8	32.6

unchanged, (see Table 3.3). By increasing of HCl flow rate, the peak position of SiGe shifts to the left (see Fig. 3.14) and the Ge content is increased. Besides, the growth rate of the films decreases accordingly. This is due to the etching rate increases with the increase of HCl partial pressure, and the growth rate decreases accordingly. However, the etching rate of silicon by HCl is higher than that of Ge under the same conditions, therefore the Ge content in SiGe films increases accordingly (Fig. 3.15).

When the flow rate is 50 sccm, the growth of SiGe film is very fast, and the thickness of SiGe film exceeds the critical thickness rapidly, causing the interference peaks are vanished in the XRD spectrum. When the growth time is decreased from 8 to 3 min, the interference peaks are appeared again in the XRD spectrum. Therefore, appropriate HCl partial pressure and large critical thickness threshold should be considered for practical applications. The effect of HCl flow rate and growth time on the growth of SiGe films is summarized in Table 3.3. In addition, the consumption of HCl has a great influence on the selectivity for SiGe epitaxy on source/drain regions, which will be explicitly discussed in the next chapter.

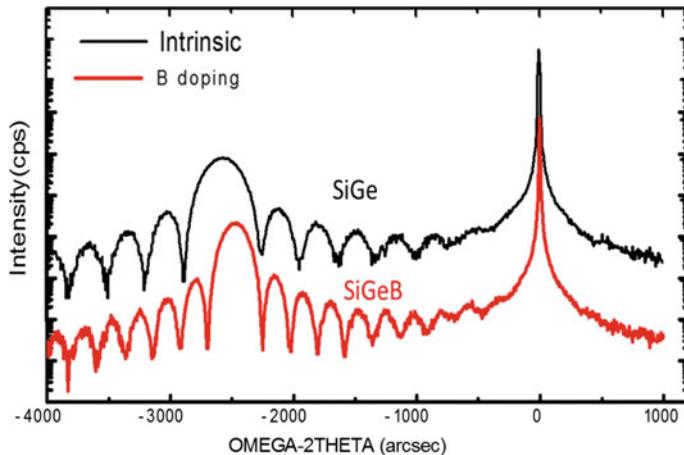
**Fig. 3.14** XRD spectrums of SiGe films grown at different HCl flow rates

**Fig. 3.15** XRD spectrums of SiGe films grown at different growth time (3 min/8 min, 50 sccm HCl)



### 3.4.5 Influence of Doping Concentration on the Strain of SiGe Films

During the epitaxy process of SiGe thin films, diluted  $\text{B}_2\text{H}_6$  in  $\text{H}_2$  is used for P-type in situ doping. The so-called in situ doping is that impurity atoms, such as boron, are doped into SiGe films during the epitaxial growth. Since the boron atoms are already in substitutional sites, subsequent thermal annealing process is not necessary. However, boron doping would reduce the lattice constant of SiGe and the amount of strain in SiGe films. This phenomenon here is called as “strain compensation effect” [19–21]. Additionally, when the boron doping concentration is too large, the SiGe film would be polycrystalline or amorphous [19]. When boron doping concentration is  $1 \times 10^{20}$  atoms/cm<sup>3</sup>, the strain compensation in SiGe films is minor. When the doping concentration is higher than  $4 \times 10^{20}$  atoms/cm<sup>3</sup>, the strain relaxation will be 33% [9]. To study the effect of doping concentration on the strain of SiGe films, the intrinsic SiGe thin films and boron-doped SiGe counterparts were scanned and analyzed by XRD. The doping concentration of boron in SiGe film was calculated by the SiGe peak shift [22, 23], along with the change of lattice constant of SiGe film after in situ boron doping [24, 25]. Figure 3.16 shows the two XRD rocking curves for SiGe and SiGe:B, respectively. After in situ boron doping, SiGe peak shifts to the right side, which is close to the Si peak. Here, the apparent Ge content for SiGe:B film is 26.3% and the corresponding film thickness is 85 nm, while the original Ge in intrinsic SiGe film before doping is 27.6% and the corresponding thickness is 61 nm. After in situ doping, Ge content is reduced by 1.3%, and the film growth rate is also increased. The calculated results show that the doping concentration of boron in SiGe film is  $8 \times 10^{19}$  atoms/cm<sup>3</sup>. In this time, the condition for  $\text{B}_2\text{H}_6$  gas flow is 2slm for DIL, 120 sccm for Source and 120 sccm for INJ in epi recipe. Here, DIL is the flow of  $\text{H}_2$  for dilution, Source is the flow from supply gas bottle INJ is the flow for gas that enters the process chamber.

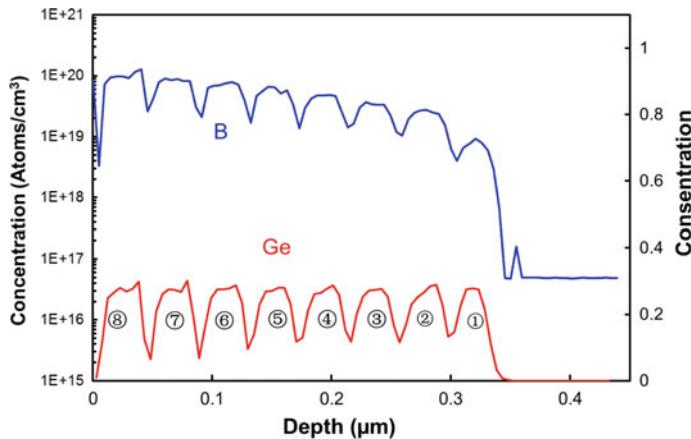


**Fig. 3.16** Effect of boron doping on the strain of SiGe film

The doping concentration of boron in SiGe depends on the dilution ratio of dopant gas  $\text{B}_2\text{H}_6$  in  $\text{H}_2$  and the setting of flow rate. The effect of the  $\text{B}_2\text{H}_6$  gas flow rate on the Ge content was studied by XRD and the results were summarized in Table 3.4. The results show that the Ge content doesn't change substantially when the doping source concentration is very low. This proves that the doping concentration of boron is low and can't be estimated by the method mentioned in the previous section. When the concentration of doping source increases to 1%, Ge composition shows a significant change, as shown in Fig. 3.16. In order to meet the requirements of the applications in transistor source/drain regions, the SIMS (see Fig. 3.17) can accurately calibrate the doping concentration in SiGe film at different flow rates of  $\text{B}_2\text{H}_6$ , where the boron doping concentration can be verified by XRD in the meantime. 1%  $\text{B}_2\text{H}_6$  in  $\text{H}_2$  was used for the growth of test sample in Fig. 3.17. Nine types of flow rate setting for  $\text{B}_2\text{H}_6$  are given in Table 3.5. The SIMS results show that the boron doping concentration

**Table 3.4** Effect of dilution ratio of  $\text{B}_2\text{H}_6$  in  $\text{H}_2$  on Ge composition and doping

$\text{B}_2\text{H}_6$ type	$\text{B}_2\text{H}_6$ flow rate			Ge composition (%)	Doping concentration ( $\text{atoms}/\text{cm}^3$ )
	DIL (slm)	Source (sccm)	INJ (sccm)		
Intrinsic	0	0	0	27.6	—
50 ppm in $\text{H}_2$	2	120	120	27.5	Unable to calculate
50 ppm in $\text{H}_2$	2	160	160	27.5	Unable to calculate
50 ppm in $\text{H}_2$	0.5	195	195	27.4	Unable to calculate
1% in $\text{H}_2$	2	120	120	26.3	$6 \times 10^{19}$



**Fig. 3.17** SIMS results of Boron concentration and Ge content in SiGe films at different  $\text{B}_2\text{H}_6$  gas flow rates

**Table 3.5** Different flow settings for  $\text{B}_2\text{H}_6$

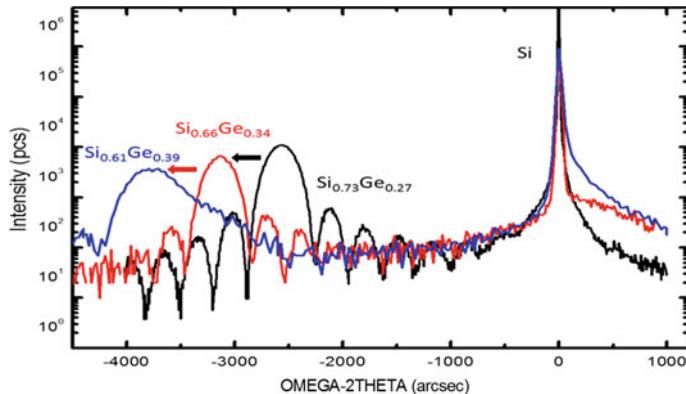
$\text{B}_2\text{H}_6$ flow rate	①	②	③	④	⑤	⑥	⑦	⑧
DIL (slm)	10	2	2	2	2	2	2	2
Source (sccm)	20	60	80	100	120	140	160	180
INJ (sccm)	10	60	80	100	120	140	160	180

increases with the increase of the flow rate. However, the Ge composition measured by SIMS doesn't change too much, so it can't be used to characterize the variation of strain composition in SiGe thin films.

The SIMS result is consistent with the result of XRD estimation. Therefore, in practical mass production, we can quickly estimate the boron doping concentration of in situ boron-doped SiGe samples by XRD scanning analysis instead of SIMS analysis to save cost and improve operation efficiency.

### 3.4.6 Effect of Ge Content on the Strain of SiGe Films

Based on the above experiments, it was found that there are many factors affecting the Ge composition during selective epitaxial growth of SiGe films. In addition to the influence of reaction temperature, total pressure, and HCl and doping partial pressure,  $\text{GeH}_4$  partial pressure can also influence the Ge content. With the increase of the partial pressure of  $\text{GeH}_4$ , the Ge content is increased. However, excessive increase of Ge content is not feasible for practical device applications. The quality of the SiGe film and the strain applied to device channel should be considered simultaneously. As the Ge content increases under the same reaction conditions, the critical thickness



**Fig. 3.18** Effect of Ge content on the strain of SiGe thin films

of SiGe film becomes smaller. If the film thickness exceeds the critical thickness, the interfacial defects of the film would increase and extend into the SiGe film, leading to the increase of dislocations and stacking defects, along with the degradation of strain effect with embedded SiGe in source/drain.

Figure 3.18 shows the XRD results for three types of SiGe films grown at 650 °C with total pressure of 20 Torr. With the increase of Ge content, the SiGe peak position in the spectrum begins to shift to the left. When the Ge content reaches 39%, the interference peaks on both sides of the SiGe peak disappear, indicating that the interfacial defects of SiGe/Si is increased and strain relaxation has been occurred. Therefore, to fabricate SiGe thin films with high Ge content and high strain, it is necessary to lower the growth temperature or change other process conditions to increase the critical thickness threshold, thus maintaining the strain of the films. In more practical way, suitable growth conditions and appropriate Ge composition for SiGe thin films should be selected according to the specific requirements of device applications, and the influence of the preparation process on the quality and strain of the films should be minimized.

### 3.5 Summary

In this chapter, the main fabrication techniques of SiGe thin films are introduced, especially the growth mechanism and experimental equipment of selective epitaxy of SiGe thin films by RPCVD. The SiGe thin films grown by selective epitaxy under different growth conditions were characterized and analyzed. Key factors affecting the growth quality and strain of SiGe films were analyzed and discussed. The epitaxial growth of SiGe films on Si substrate was optimized, and the relevant conditions for process optimization include:

- (1) The temperature range for reaction process should be between 650 and 700 °C. The growth temperature determines the growth rate and Ge content of SiGe. If the growth temperature is too high, the critical thickness threshold of the film is very small, and the strain of the film is easily relaxed, resulting in defect generation. If the temperature is too low, the Si precursor, DCS is not easy to decompose. Thus, the growth rate is very low, and defects are generated easily in the film. This is unsuitable for mass production applications.
- (2) Working pressure should be between 10 and 20 Torr. The change of total pressure can regulate the growth rate of SiGe. Excessive pressure is not conducive to the control of growth rate and the removal the by-products during reactions. This would affect the quality of the film.
- (3) HCl partial pressure should be between 50 and 65 sccm. With the increase of HCl consumption, the growth rate of SiGe films decreases and the Ge components increase. The consumption of HCl can be mainly used for the selectivity of the epitaxial grown film during device integration. The detailed information will be discussed in the following chapters.
- (4) Moderate boron doping concentration of  $1 \times 10^{20}$  atoms/cm<sup>3</sup> to  $3 \times 10^{20}$  atoms/cm<sup>3</sup>. The boron doping concentration in in situ doped epitaxial SiGe films can be estimated by XRD technique. This is beneficial for on-line monitoring of SiGe epitaxy process.
- (5) Suitable Ge content should be between 27 and 35%. Ideally, the larger the Ge component is, the greater the film strain will be. However, if the Ge content is excessively increased in practical application, the thickness of the films will exceed the critical thickness rapidly, resulting in strain relaxation and generation of defects. Therefore, in combination with practical production applications, it is necessary to choose the temperature as low as possible (650 °C) or other process conditions to increase the critical thickness threshold. In addition, in practical applications, Ge content is also affected by pattern density during selective epitaxy. The Ge composition of film grown on the patterned substrate would differ from the composition of film grown on bulk silicon wafer. More information will be given in the following chapters.

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# Chapter 4

## SiGe S/D Integration and Device Verification

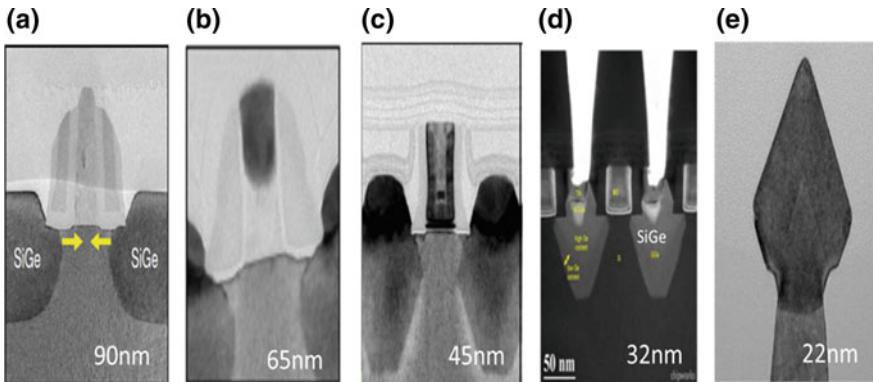


### 4.1 Introduction

SiGe S/D strain engineering is one of the key processes in the advanced manufacturing technology of integrated circuits. In each technology node in sub 90 nm technology generations, strain has been used to improve the channel mobility of PMOS devices. In this chapter, integration of SiGe selective epitaxy in S/D of 22 nm planar transistors and 16 nm FinFET have been studied. The strain distribution by SiGe in S/D regions is analyzed. Finally, the electrical measurements of 22 nm planar transistors and 16 nm FinFET devices with integrated SiGe S/D are presented.

#### 4.1.1 Development of SiGe S/D Strain Technology

As the world leader in large-scale integrated circuit manufacturing technology, Intel released the new Pentium IV processor with strained silicon technology produced in 90 nm process in 2003, with a maximum operating frequency of 3.4 GHz [1]. The NMOS used a high tensile stress SiN film of CESL. This was the first time to apply SiGe strain technology on PMOS S/D while the Ge composition in SiGe is 17% [2]. In 2004, Intel and Toshiba introduced strained silicon technology for the 65 nm process where the second-generation SiGe S/D strain technology was presented to improve the performance of the PMOS [3]. In order to obtain a large strain amount, the geometry of the S/D epitaxial region was adjusted. And the Ge component was increased to 23%, which significantly increased the channel strain by more than 60% [4]. At the same time, the NMOS device adopted a high tensile stress SiN film covering layer, so that the channel strain was more than 80%, and the current driving capability was improved by 20% [5]. In 2007, Intel adopted the HKMG back gate process integration solution in the 45 nm process, and the SiGe S/D strain



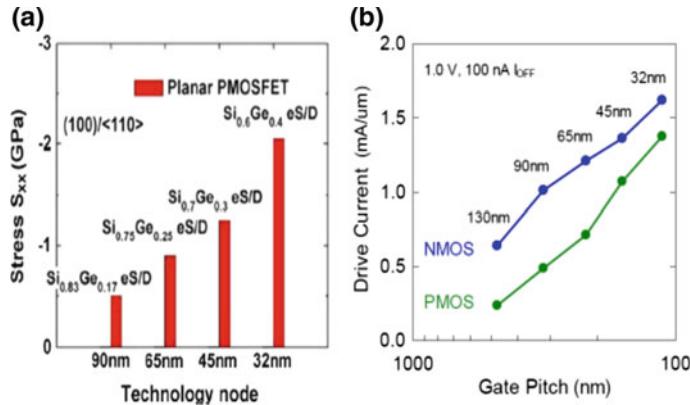
**Fig. 4.1** Development of SiGe S/D strain technology for each technology node of Intel [2, 3, 5, 7, 8]

technology also developed. The shape of the S/D recess changes from a circular shape to a sharper “ $\Sigma$ ” shape where SiGe could be placed closer to the channel, and the Ge composition is increased to about 30%. The PMOS device combined with SiGe S/D strain technology and HKMG integration increased the drive current by 51% in 65 nm technology generation [6]. In 2009, Intel’s 32 nm process [7] maintained the SiGe strain technology in 45 nm node but continued to use the improved S/D and post metal gate process. The performance was improved compared to 45 nm. In 2011, Intel did not introduce the 22 nm technology of planar technology, but they adopted the three-dimensional FinFET transistor technology. The S/D region of the FinFET PMOS device still used SiGe strain technology, but the film growth changed from planar process to 3D process, while the Ge component in the film was increased to more than 40% [8]. Figure 4.1 is a summary of the variation of the SiGe S/D strain technology used by Intel in sub-90 nm technology generation.

#### 4.1.2 Summary of SiGe S/D Technology

From the development history of the SiGe S/D strain technology in large-scale integrated circuit manufacturing (Fig. 4.1), it can be seen that the SiGe S/D are mainly used to introduce the compressive strain parallel to the channel direction in the channel plane of the PMOS device, which can improve the device performance. The main technical features are summarized as follows:

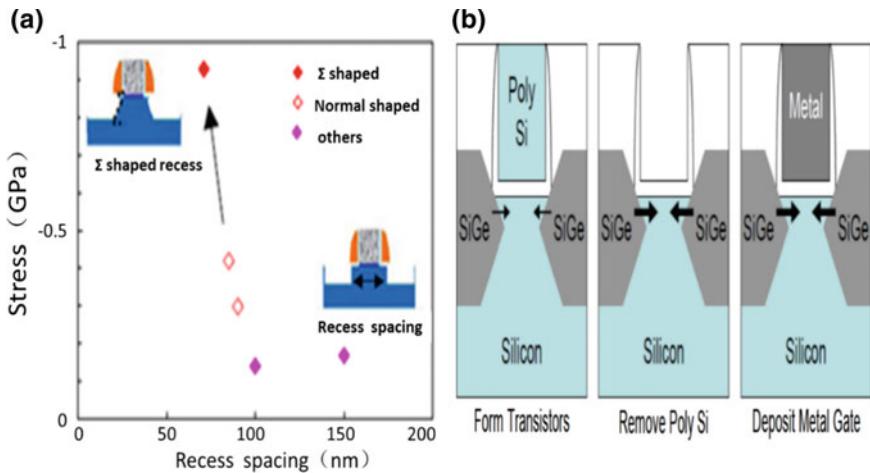
- (1) In the SiGe S/D process, the Ge composition in the SiGe film increases as the device size decreases. Figure 4.2a shows the effect of the Ge composition in SiGe S/D on the strain in various Intel technology generations [9]. The Ge composition increased from 18% in 90 nm to about 40% in 32 nm, and the compressive



**Fig. 4.2** The influence of **a** the Ge component in SiGe S/D on the increase of the strain and **b** the increase of the drive current in various Intel technology generations [9]

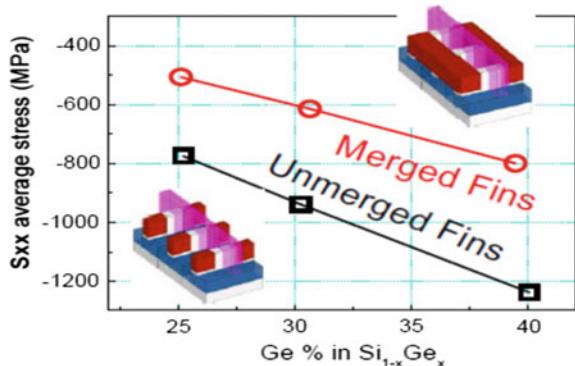
stress generated on the channel increased from 0.5 to 2 GPa. Figure 4.2b summarizes the contribution of the SiGe S/D strain technique to the drive current of each technology node in PMOS. As discussed in the previous section, increasing the Ge composition would reduce the critical thickness of the SiGe film. Therefore, the SiGe process should be optimized and adjusted while increasing the Ge composition to reduce the strain relaxation and defect generation caused by the increase of the Ge composition.

- (2) In the SiGe S/D process technology roadmap, the recess profile of the S/D epitaxial region changes significantly. It changes from the original Round Shape to a “ $\Sigma$ ” type which is closer to channel and can act directly on the channel, as shown in Fig. 4.1c. Figure 4.3 is a schematic diagram of the relationship between strain and morphology of the SiGe S/D [10, 11], which shows that the S/D of the “ $\Sigma$ ”-type structure will increase the channel strain. This design can be combined with the HKMG back gate integrated process [6], the mobility of the channel carriers will be further improved as well as the device performance.
- (3) In the 3D FinFET technology, the SiGe S/D process has changed greatly in size and morphology. The S/D changes from the recess of the planar device to the Si-Fin of the 3D device. In addition to increasing the Ge composition, changing the structural design of the Si-Fin can also increase the strain on the channel [12]. The design of the structure without the connection of the ends of the Si-Fin introduces a larger channel strain than the connected one, as shown in Fig. 4.4. In addition, the SiGe stressor in S/D in FinFET technology can increase the contact area of S/D, reducing the S/D contact resistance [13], and improves the drive current.



**Fig. 4.3** **a** Relationship between strain and morphology of SiGe S/D [11], **b** effect of SiGe S/D strain back gate integration on channel strain [6]

**Fig. 4.4** Effect of Si-Fin shape on SiGe S/D strain in FINFETs [13]



#### 4.1.3 Challenges of SiGe S/D Technology

SiGe S/D strain integration becomes more and more difficult as the transistor size shrinks. The main technical challenges are:

- (1) When the Ge composition in the SiGe S/D is within a certain range, the induced strain in the channel increases as the composition increases. However, as the composition continues to increase, and the film strain is released when the thickness is reached to a critical thickness. Although this critical thickness is above published data above bulk SiGe but the depth of recess and the thickness of the grown layer have to be carefully considered. Therefore, it is a very challenging task to obtain a high range of Ge components while maintaining the strain on the channel in the SiGe S/D strain engineering.

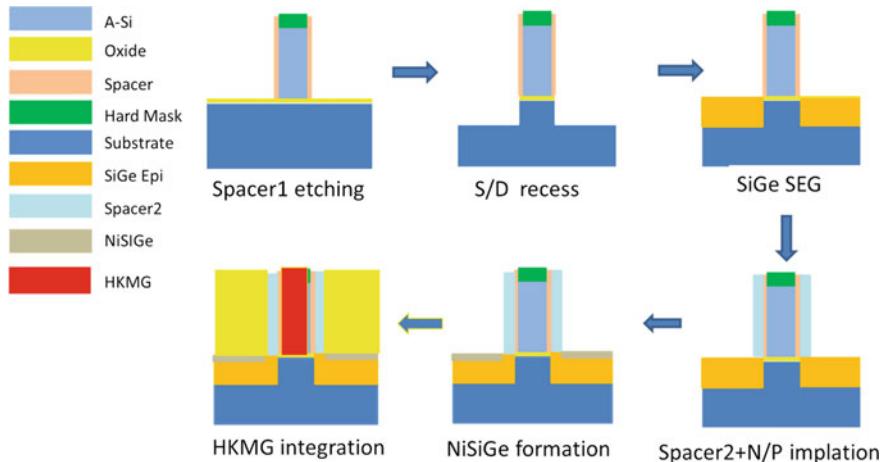
- (2) Selective epitaxial growth of SiGe in nanoscaled S/D areas of the transistors is different from growth on bare silicon wafer (bulk growth). This difference originates from surface quality of recess in S/D regions in planar transistors and the morphology (shape and roughness) of Si Fins in FINFETs.
- (3) Growth of SiGe S/D is vanrunable to presence of natural oxide and residuals after other process steps. As an example, SiN sidewall of the small size transistors and the hard mask oxide at the top of the dummy gate are thin for the “HF-Last” process, the removal of the natural oxide layer is a delicate task since to the hard mask oxide on the SiN sidewall and the top of the dummy gate should not be over-etched. Therefore, to create a high-quality interface before epitaxy is another challenge for SiGe S/D integration.
- (4) The pattern density has both microscopic and macroscopic effect on the SiGe selective epitaxy. This occurs when the silicon exposure areas vary in different regions of the chip and this affects the efficiency of pre-bake removal of the native oxide layer, SiGe growth rate, and Ge composition distribution during epitaxial processes. The variation of patten density affects the performance of devices in different regions of the chip. In this case, how to reduce the impact of pattern density effect on process and device performance is also a process challenge.

## 4.2 Integration of SiGe in S/D in 22 nm Planar MOSFETs

This section mainly discusses the SiGe S/D process integration and device fabrication of 22 nm planar devices, and studies the special S/D epitaxial formation methods.

### 4.2.1 *Device Integration Process, Experiment Details*

In this section, the process of 22 nm node planar PMOS transistors with embedded SiGe in S/D regions. The transistors are fabricated on 8 in. wafers. The etched Si trenches are formed and filled with  $\text{SiO}_2$  to obtain the shallow trench isolation (STI) for the transistors, and ion implantation is performed to define the well and device channel. Then, gate oxide and amorphous silicon are deposited on the device region, where amorphous silicon is used as a replacement gate in device integration (Dummy Gate), and would be removed during subsequent HKMG gate process integration. The sidewall 1 (Spacer 1) is formed after etching the covered SiN layer, and the subsequent process flow is as shown in Fig. 4.5. After device S/D etching, SiGe selective epitaxial growth is performed under low temperature, and B in situ doping is simultaneously performed. NiSiGe process integration is performed after the Spacer 2 process is formed, that is, after Ni is sputtered on the surface of SiGe, NiSiGe having a low ohmic contact resistance is formed by annealing at 300 and 450 °C for



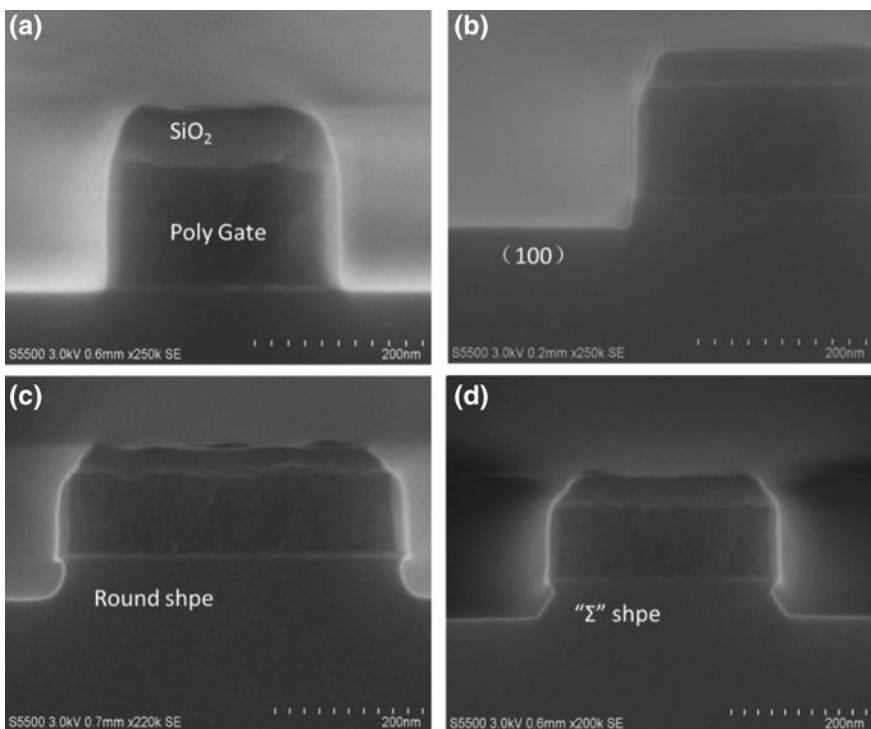
**Fig. 4.5** Schematic of the embedded S/D GeSi process integrated in 22 nm node MOSFETs

30 s in N<sub>2</sub> atmosphere. In the 22 nm planar process, HKMG back gate integration is also a critical process module. The dummy gate and the gate oxide layer are removed before depositing HK. HK is a 20 Å HfO<sub>2</sub> grown by Atomic layer deposition (ALD) technology, and TiN, Ti, TiN and W are sequentially deposited as PMOS metal gate structure layer after HfO<sub>2</sub>. After the alloy annealing of the device at 425 °C, the front end of the entire device is completed (without integrated interconnection), and the fabricated device can be measured for electrical performance. When fabricating a CMOS device, the NMOS region is masked with silicon oxide. After the PMOS SiGe S/D process is integrated, the silicon oxide masked on the NMOS is removed.

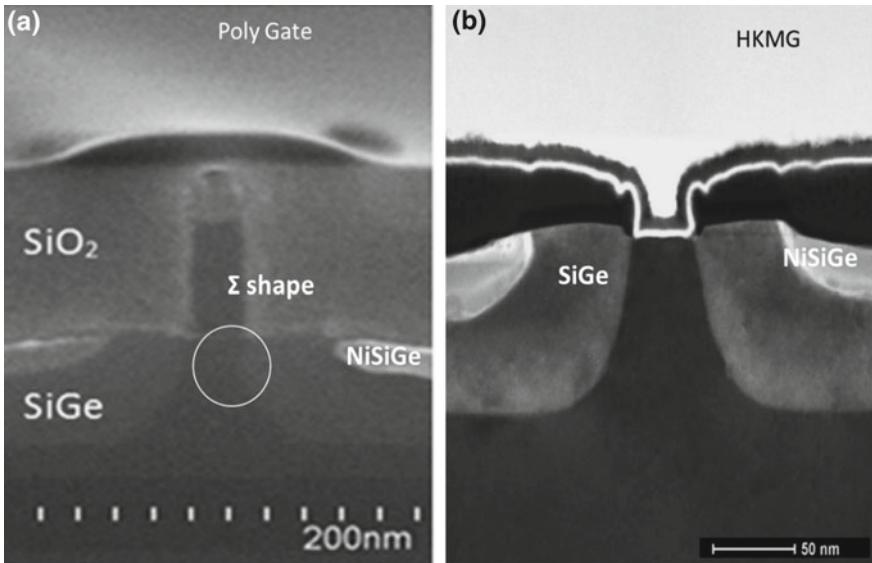
#### 4.2.2 S/D “Σ” Formation

The induced strain on the channel region by the selectively grown SiGe layers in the S/D regions can be affected by device geometries. The geometry of the device typically includes the width of the device, the length of the channel, the distance from the gate to the STI, and the thickness of the sidewalls. In general, SiGe in S/D regions of small size transistors produces more strain on the channel region than the large devices. In addition, the selective epitaxial process conditions of SiGe have a great influence on the S/D induced channel strain. The specific effects are following: the depth of the S/D regions, the recess morphology and the composition of Ge in the film. In order to induce strain effectively to the channel in a planar transistor process, the S/D profile is designed to be “Σ” shape, and the “sharp angle” formed by etching the S/D near the channel. This makes it easier for the selectively epitaxially grown SiGe to act more directly on the channel strain, maximizing the SiGe S/D strain.

The formation of a “ $\Sigma$ ” shape recess in the S/D regions is a complicated process, and it is necessary to control the depth, the surface roughness and the etching crystal orientation of the recess during etching the Si S/D to reduce the influence on the selective epitaxy process. Figure 4.6 are SEM images of the different stages of the S/D “ $\Sigma$ ” recess process. The process starts with a polycrystalline gate with  $\text{SiO}_2$  (see Fig. 4.6a). Later, dry (plasma) etching is used in a two-step process. At first, an anisotropic etch is performed to form Si trench with a certain depth along the (100) crystal orientation, which maintains the crystal orientation of the sidewall silicon approximation (110) (see Fig. 4.6b), and defines the depth of the S/D recesses. Subsequently in the same etch process, an isotropic etching is performed. The (100) and the approximate (110) crystal orientations in the Si trench are simultaneously etched and extended into the plane of the channel. This isotropic etching is important, and more lateral channel etching causes the S/D to be closer to the center of the channel. Finally, the sample is placed in a 2.37% Diluted Tetramethylammonium Hydroxide, tetramethylammonium hydroxide (DTMAH) alkaline solution diluted with deionized water at room temperature ( $23^\circ\text{C}$ ) to selectively etch the Si recess and to form “ $\Sigma$ ” shape (see Fig. 4.6d).



**Fig. 4.6** SEM image of the process flow of S/D “ $\Sigma$ ” morphology



**Fig. 4.7** Cross-sectional view of a 22 nm planar transistor integrated with SiGe S/D. **a** Multi-gate device with “ $\Sigma$ ” morphology [14]. **b** The transistor with integrated HKMG and NiSiGe contacts [15]

#### 4.2.3 S/D SiGe Selective Epitaxial Growth

For the epitaxial growth, the sample has to be pre-baked at 900 °C for 5 min to remove the surface of the natural oxide layer, and the SiGe S/D process is optimized to integrate SiGe S/D 22 nm PMOS devices (see Fig. 4.7) [14]. Both the S/D regions of these devices in the figure use Ni silicide as the contact. In Fig. 4.7a, the 22 nm MOSFET uses a polysilicon gate and the gate dielectric is thermo oxide. The 22 nm device in Fig. 4.7b uses the HKMG gate-last process integration scheme [15]. The quality of selectively grown SiGe films fulfills the requirements for high performance transistor.

### 4.3 Integration of SiGe S/D in 16 nm FinFET Device

#### 4.3.1 Device Preparation and Experimental Details

The Si FinFET includes many new process steps compared to the 22 nm planar process, and the entire device fabrication process is more complex. As shown in the process flow diagram of the 16 nm FinFET device in Fig. 4.8, Sidewall Transfer Lithography (STL) [16] is used to form Si Fins with a tip width of 20 nm and a height

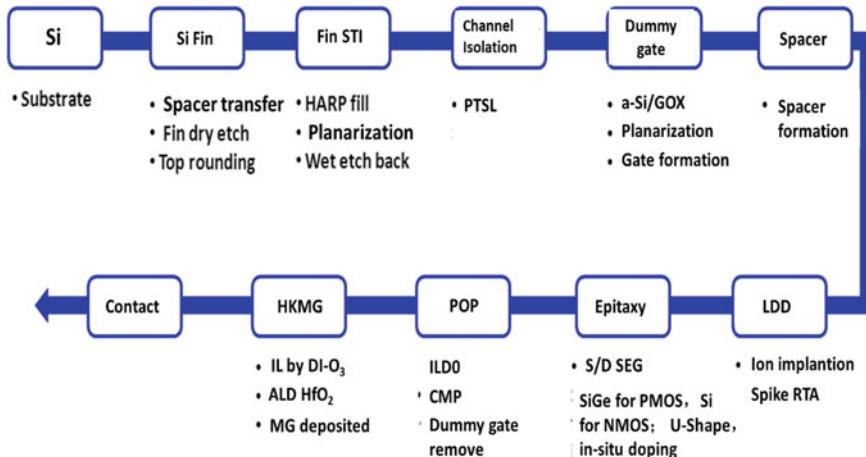
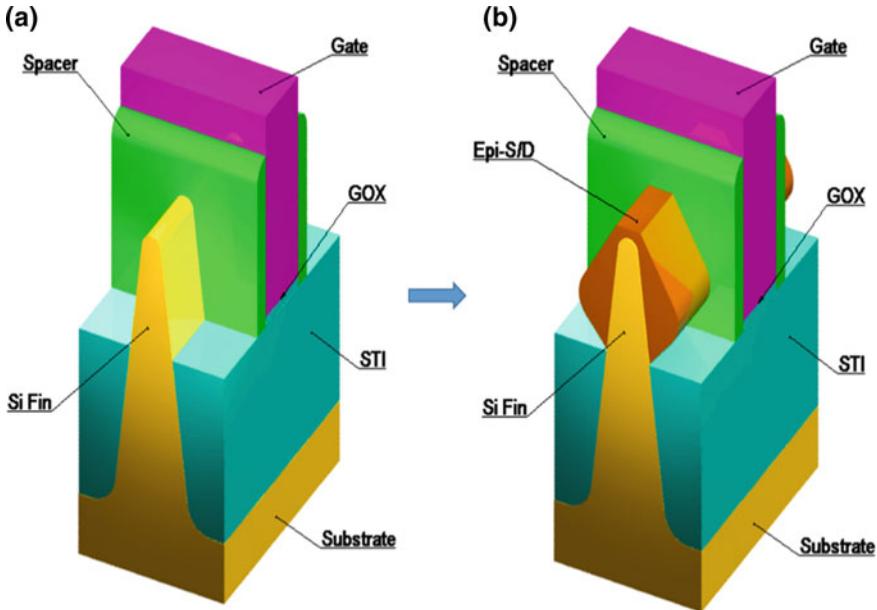


Fig. 4.8 Schematic diagram of the process flow in a bulk Si FinFET device

of 110 nm. The specific process of STL is as follows: at first, a stack of SiN, SiO<sub>2</sub> and amorphous silicon are deposited on the surface of the silicon substrate. After lithography defines the pattern size, etching is performed, and a SiN film with good conformal coverage is deposited on the amorphous silicon after etching to form a sidewall spacer, and after removing the amorphous silicon, the silicon substrate is anisotropically etched to form a trapezoidal Fins by using the SiN sidewall as a hard mask. The residual SiN is removed in a hot solution of phosphoric acid (H<sub>3</sub>PO<sub>4</sub>) and diluted hydrofluoric acid (DHF). A thin oxide layer is formed on the surface of the Fins by rapid thermal processing, and removed it to repair damage and reduce roughness of the surface of the Si Fins due to plasma etching. Subsequent Fin's STI process module uses a High-Aspect-Ratio Process (HAR) to deposit 2000 Å silicon dioxide for shallow trench isolation (STI). After the planarization process, a certain thickness of silicon oxide is removed by DHF to expose the top end of the Si Fins. The shape of the false grid line is defined by means of Electron Beam Lithography (EBL). Silicon nitride is deposited on both sides of the dummy gate to form sidewall spacers, and selective epitaxial growth of the S/D regions is performed after the implantation is activated. PMOS selective epitaxial SiGe, NMOS selective epitaxial Si. After the dummy gate is flattened and removed, the HKMG module is formed to perform electrical test analysis of the device.

#### 4.3.2 Selective Epitaxial Growth of SiGe/Si in 16 nm FinFET Devices

The three-dimensional device integration is more difficult than the planar device for the selective epitaxy of PMOS S/D SiGe and NMOS S/D Si. Selective epitaxial

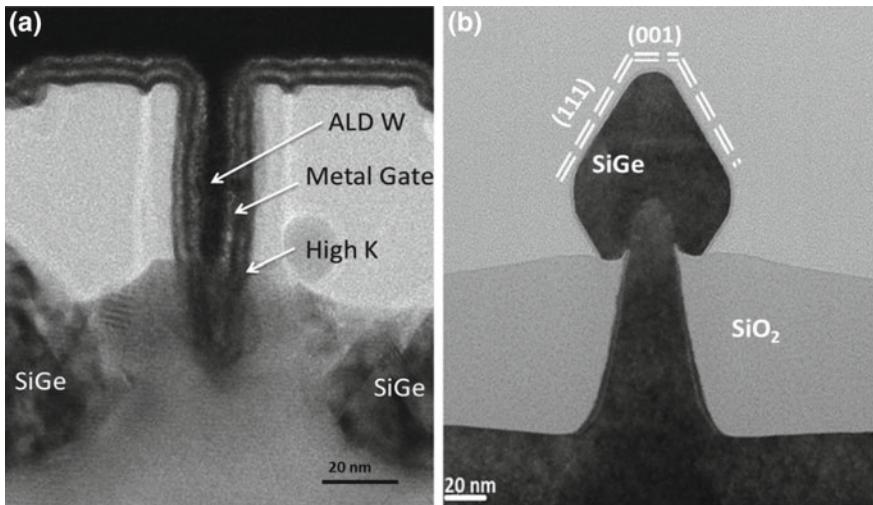


**Fig. 4.9** Schematic drawings of integrated S/D epitaxial growth of a 16 nm FinFET device

growth should not consider only the selectivity towards the dielectric layer (Spacer SiN and hard mask (HM), STI SiO<sub>2</sub>), but also the retention of the film strain in the growth of different crystal orientations of Si Fins. After the SiGe selective epitaxy is completed, the shape of the deposited SiGe is diamond like, which is symmetric along the center of the Si Fins, as shown in the diagram in Fig. 4.9b. On the other hand, if the S/D contact is directly integrated on the tip of small size Si Fins tip, the contact resistance is large, which affects the driving current of the FinFET. The epitaxy of SiGe in S/D regions can increase the S/D area and significantly reduces the S/D contact resistance, and improves transistor performance.

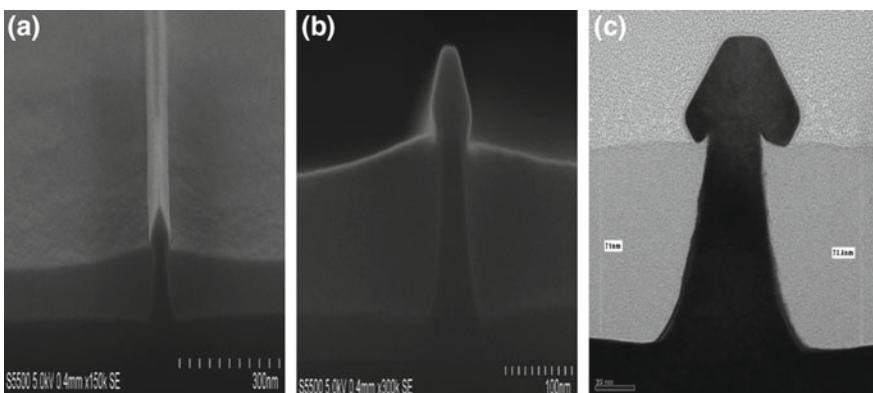
Figure 4.10a, b show the fabricated 16 nm FinFET PMOS device gate with integrated SiGe S/D [17, 18]. The TEM results show that the selective epitaxial growth of high quality SiGe is uniformly distributed symmetrically on both sides of Fin. The S/D regions contain different crystal facets: The top (100) and the side (111), which is due to the difference in the growth rate of SiGe on different crystal faces, but eventually merging to form a diamond shape. In addition, compared with Intel's 22 nm FinFET PMOS device SiGe S/D profile (as shown in Fig. 4.1e), it is found that its Fin tip is damaged sharply. The loss of Si Fin is small and the morphology remains good in the epitaxial process of this experiment.

For NMOS FinFET, Si is selectively grown to raise S/D regions which is very different from SiGe. Moreover, in order to balance the selectivity and growth rate of the epitaxial process, a higher growth temperature than SiGe epitaxy is required.



**Fig. 4.10** FinFET PMOS device with SiGe S/D. **a** Gate profile TEM [17], **b** SiGe S/D profile TEM [18]

The SiGe selective epitaxy is completed at 650 °C, and the selective epitaxial temperature of Si is at least 750 °C. Figure 4.11 is a picture of a selective epitaxial process with integrated Si. Since the selective epitaxy of Si is performed at a higher temperature and the etching effect of HCl on Si is remarkable, the S/D morphology is not as uniform as PMOS SiGe. The epitaxial Si on Si is homoepitaxial, so the interface between Si-Fin and selective epitaxial Si is not clearly distinguishable in TEM (Fig. 4.11c).



**Fig. 4.11** SEM images from FinFET NMOS with integrated Si in S/D regions. **a** Front view, **b** profile SEM, **c** profile TEM

## 4.4 Selective Epitaxial Process of SiGe for 22 and 16 nm MOSFETs

This section focuses on the key issues in the integration of selective epitaxy of SiGe S/D in 22 nm planar and 16 nm FinFET devices. These key issues mainly include interface cleaning before epitaxy, S/D morphology during epitaxy, growth quality, strain relaxation and selectivity. These issues are very important for the SiGe S/D integration and transistor performance. Therefore, the effects of selective epitaxy on SiGe S/D integration will be discussed in detail in this section.

### 4.4.1 *The Influence of Ex-situ Cleaning on SiGe Epitaxy*

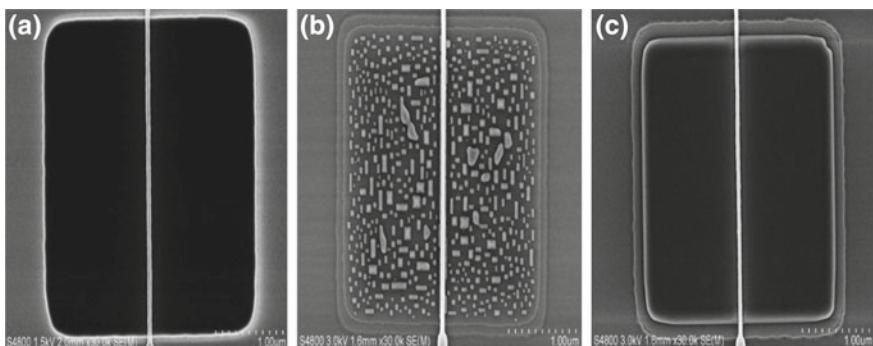
During the device process, the substrate wafer is pre-cleaned prior to selective epitaxial growth of the SiGe film. The purpose of the cleaning is to remove the photoresist residue present on the surface, the polymer produced by the etching, and the particles generated in the plasma etching chamber. The removal of these impurities requires an effective cleaning method. The common method used in the IC manufacturing industry is to use the RCA standard cleaning method, which was first initiated in 1965 by Kern and Puotinen et al. at the RCA laboratory in N.J. Princeton [19].

The cleaning process of the exposed surface of the patterned wafer is much more complicated than the bare silicon. The cleaning process needs not only to remove the undesired materials from the exposed surfaces, but also takes into consideration the effect of the cleaning solution on the loss of the dielectric film and the damage to the lines in the pattern. The main process steps of pre-epitaxial cleaning used in this experiment are following:

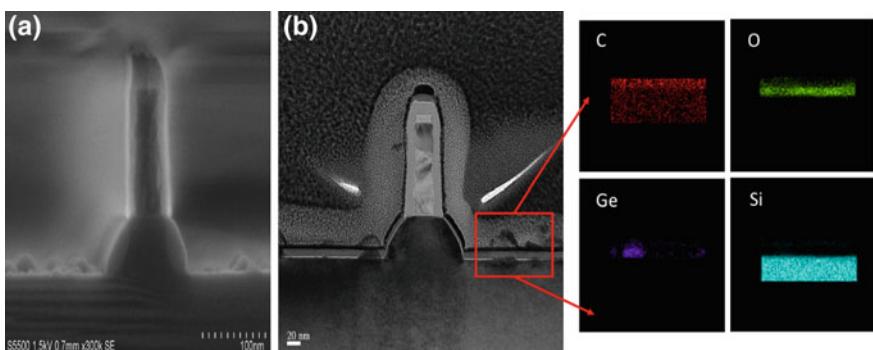
- (1) At First, SPM (mixed solution of  $H_2SO_4$  and  $H_2O_2$ ) is used for cleaning: SPM has a high oxidation capacity at 120 °C. The metal can be oxidized and dissolved in the cleaning liquid to oxidize the organic matter to form  $CO_2$  and  $H_2O$ . Cleaning the silicon wafer with SPM removes heavy organic and different metal contamination on the surface of the wafer, but the organic contamination is particularly difficult to remove since the organic material is carbonized.
- (2) At second, APM ( $NH_4OH/H_2O_2/H_2O$ ) is used: it is also an SC1 solution. Because of  $H_2O_2$ , a layer of natural oxide film is formed on the surface of silicon wafer. Since the natural oxide layer on the surface of the wafer then Si surface of wafer is corroded by  $NH_4OH$ , resulting the particles fall into the cleaning liquid, thereby achieving the purpose of removing surface particles.
- (3) Finally, DHF (diluted HF acid) solution: DHF can remove the natural oxide film on the silicon surface, while DHF suppresses the formation of the oxide film. When cleaning with DHF, the surface silicon is hardly corroded when the natural oxide film is etched away. However, the corrosion process should pay attention to the control of corrosion concentration and corrosion time. When the cleaning is completed, the natural oxide layer of the silicon surface is removed,

and the side wall SiN, hard mask SiO<sub>2</sub> and STI SiO<sub>2</sub> should not be excessively lost in the pattern. After the DHF cleaning is completed, it is necessary to put the sample in the load-locks as soon as possible in order to avoid the formation of more natural oxide layers and other contamination on the silicon surface during the sample transfer process. The process of removing the native oxide layer by HF solution cleaning before this epitaxy is also called as “HF-last”.

In the actual device SiGe epitaxy, the recess in S/D is subjected to a three-step cleaning (Fig. 4.12a) [15]. If the Si area is not completely cleaned then only discontinuous island like growth occurs, as shown in Fig. 4.12b [15]. Further TEM EDX analysis of the sample revealed that the C content of the Si surface is high (as shown in (b) of Fig. 4.13), and the Ge content is very low. The organic material agglomerates on the surface of the sample since they are not completely removed. It has been shown that these organic contaminations may come from the formed polymers



**Fig. 4.12** **a** SEM top view before epitaxial cleaning, **b** SEM top view of poor SiGe growth quality after epitaxial cleaning and **c** SEM top view of good SiGe growth quality after epitaxial cleaning [15]



**Fig. 4.13** **a** SEM cross-section of poor SiGe growth quality and **b** TEM cross-section and element EDX mapping analysis of poor SiGe growth quality [15]

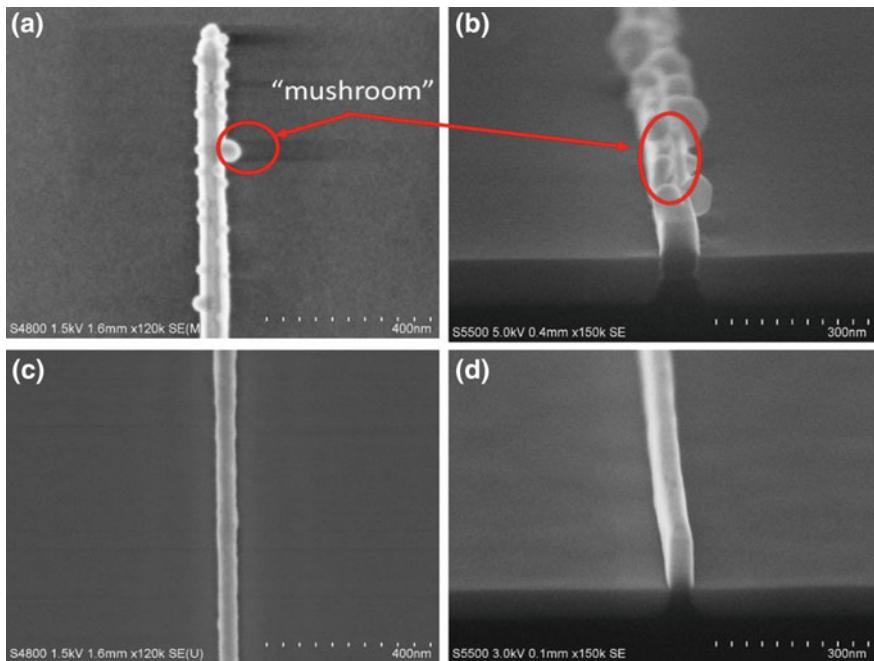
during the dry plasma. Figure 4.12c shows a successful epitaxy after a good surface cleaning [15].

The cleaning process is improved by dipping the sample in a 100:1 HF solution for 10–30 s before standard cleaning. The use of HF to destroy the Si–O bond in the polymer during the etching of the silicon trench reduces the adhesion between the polymer and the silicon substrate, which facilitates the removal of the organic polymer [20–22]. After the improvement, the quality of the selectively epitaxially grown SiGe film is very stable, as shown in (c) of Fig. 4.12.

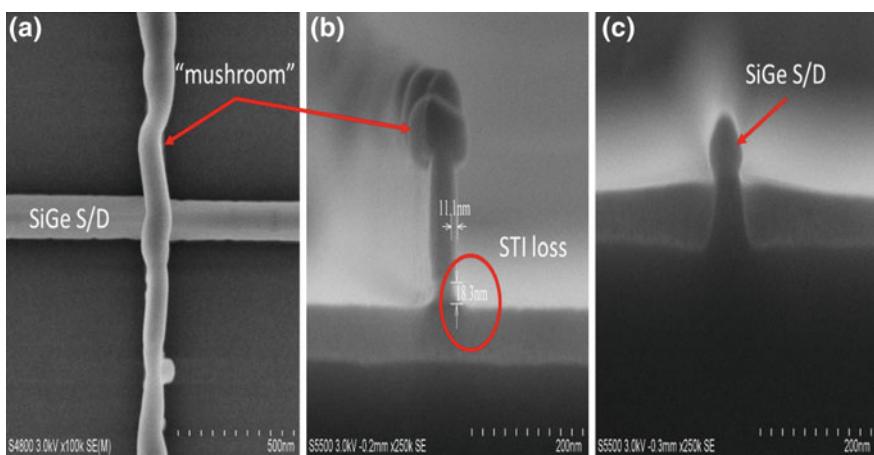
In addition, in order to enhance the removal ability of the natural oxide layer and selectivity etch of the SiN sidewalls during the “HF-last” cleaning process, a diluted BOE (Diluted Buffer Oxide Etcher, DBOE) solution is used in the cleaning experiments. The 7:1 BOE solution and deionized water are diluted in a volume ratio of 1:20 to achieve a chemical oxidation rate of about 0.5 nm/min. The diluted BOE solution effectively removes the native oxide layer on the Si surface, and the added ammonium fluoride acts as a buffer to avoid excessive consumption of fluoride ions to maintain a stable etch rate.

The removal of Si surface oxide layer by HF leaves hydrogen terminated surface, which effectively blocks the oxygen atmosphere in the isolated air [23, 24]. Since the polarity difference between the F and Si atoms is relatively large, the Si–F bond has a strong polarity. When the F atom reaches the surface, it can affect the Si–Si bond polarization of the surface, and the polarized Si–Si bond is easier to react with HF to form SiFx [25]. At the same time, the surface Si–Si bond will be replaced by a stable Si–H bond. Once the H bond is formed on the surface of the sample Si, it can suppress the rapid growth of the surface natural oxide layer, but it is more difficult to form Si–H bonds on the surface of the patterned substrate silicon than the bare silicon wafer. Therefore, in the process of removing the natural oxide layer by using the DBOE solution, when the HM and the STI SiO<sub>2</sub> are not excessively corroded, the DBOE etching time has to be prolonged as much as possible, to promote H bonding on the Si surface. If DBOE excessive etching is performed, HM SiO<sub>2</sub> at both ends of the dummy gate will be partially etched away. An extra care is required that dummy gate will not exposed during selective epitaxy and form “mushroom shape” undesired deposition. After a long period of HF dip, Fig. 4.14a, b show the “SiGe mushroom” during the selective epitaxial growth of SiGe in the 22 nm planar PMOS device integrated sample. In the 16 nm FinFET PMOS device integration, not only the “SiGe mushroom” at the top of the gate will occur, but also too much SiO<sub>2</sub> will be lost in the STI region (Fig. 4.15b), causing excessive leakage current of the device. Therefore, the key to DBOE corrosion is to remove the natural oxide layer on the surface while choosing a moderate corrosion time.

Therefore, after optimization of the cleaning process before epitaxy, the cleaning process steps for the SiGe S/D epitaxy are summarized as following: pre-treatment with 100:1 hydrofluoric acid solution, followed by SPM and APM step cleaning, and finally “HF-last” process uses DBOE solution cleaning. According to the thickness of HM SiO<sub>2</sub> and the loss of STI SiO<sub>2</sub>, the appropriate etching time (about 60 s) is selected, and the sample is controlled to be in the epitaxial equipment after the DBOE solution is cleaned and dried for less than 10 min.



**Fig. 4.14** SEM images of 22 nm PMOS gate with HF over-etching and SiGe epitaxial growth, **a** top view, **b** gate cross-sectional SEM image and HF moderately etched SiGe epitaxial growth, **c** top view and **d** gate cross-section SEM image



**Fig. 4.15** SEM images of FinFET PMOS fin after HF acid over-etching and SiGe epitaxial growth **a** top-view, **b** gate cross-section and **c** S/D cross-section

#### 4.4.2 The Influence of Pre-baking Process on SiGe Integration in S/D

The surface of Si etched by DBOE solution has a thin natural oxide layer (Native Oxide). This oxide layer must be removed before epitaxial film growth, which is the most critical criteria for the epitaxial film growth process. The process of removing the natural oxide layer or residual impurities on the silicon surface at a high temperature in the epitaxial process is generally referred to as pre-baking, also called epitaxial in situ cleaning. The main principle of pre-baking to remove the natural oxide layer is to reduce the oxygen concentration in a high-temperature H<sub>2</sub> reducing atmosphere to expose the Si surface for epitaxial growth of the single crystal material. The reactions occurring during the high temperature pre-baking process are as shown in Eqs. (4.1) and (4.2):

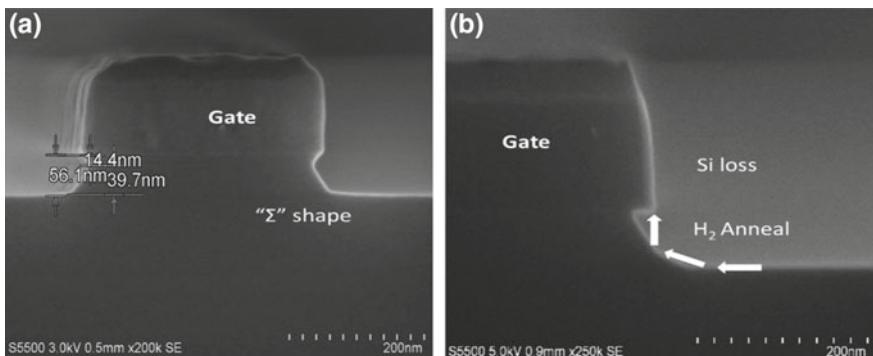


The above reaction mainly occurs in the reduction reaction, the reducing agent displaces the oxygen in the SiO<sub>2</sub>, and the more the reduction reaction occurs as the temperature rises. Pre-baking is performed at different temperatures for bare silicon wafers compared to patterned substrates. The bare silicon wafers are processed at 1050 °C for 2 min in H<sub>2</sub> atmosphere to completely remove the natural oxide layer on the silicon surface. The patterned substrates require lower temperature in pre-baking due to the thermal budget constraints of the device integration. In particular, when the sub 22 nm small size is reached, the transistors need less thermal process in order to protect the implant doping and S/D morphology before epitaxy. In order to further study the influence of the pre-baking process on the morphology of the S/D recess and Fins shape, a series of experiments are performed on the 22 nm planar and 16 nm FinFET device. In general, the effect of the pre-baking process on S/D morphology change and the removal of natural oxide layer can be examined by SEM or TEM techniques.

##### 4.4.2.1 Effect of Pre-baking Process

The test samples with “Σ” shape recess are baked at different temperatures, in order to determine the thermal stability of the shape. Figure 4.16a shows a test sample with the “Σ” shape recess, and (b) is a SEM of the cross section of the sample after baking at 900 °C for 3 min under normal pressure. The results show that the “Σ” shape disappeared in the sample baked at 900 °C under normal pressure, and the Si under the gate oxide is obviously lost.

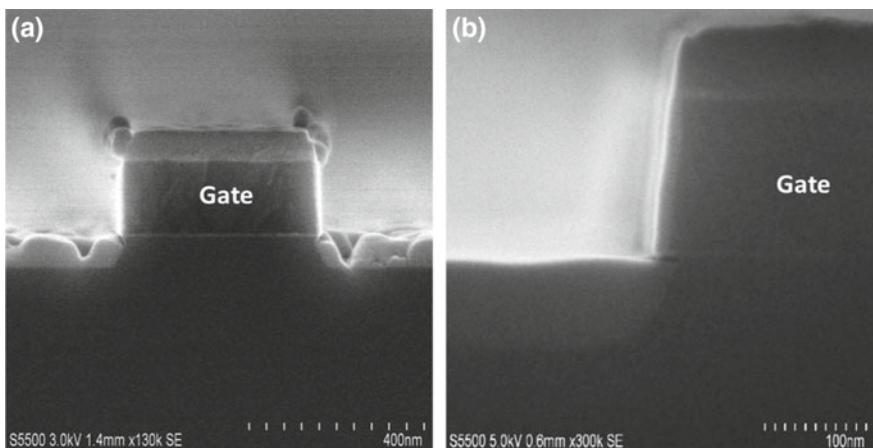
In order to further confirm whether the growth quality of SiGe has been affected, a structure sample with a “Σ” shape recess is selected to directly enter the chamber



**Fig. 4.16** Cross section images of a test sample with “ $\Sigma$ ” shape recess **a** as formed and **b** same sample as previous but baked at 900 °C for 3 min under atmospheric pressure

after cleaning, and the SiGe film is selectively epitaxially grown at 650 °C without baking, as shown in Fig. 4.17a. The other test sample is selectively epitaxially grown after baking at 900 °C for 3 min, as shown in Fig. 4.17b. As a result, it is found that the “ $\Sigma$ ” shape of the recess which is not baked at a high temperature has been maintained, but since the natural oxide layer on the Si surface is not removed, the quality of the grown SiGe film is poor. The high temperature baked sample showed a loss of Si, and the shape of the “ $\Sigma$ ” damaged due to the thermal treatment.

There are two main reasons for the above results. One reason may refer to presence of Cl-based residues on the surface of the film. The Cl will etch the surface Si at high temperature, and the etching effect will be more obvious with the increase of temperature, as shown in Fig. 4.17b. Another reason is that the potential surface energy of



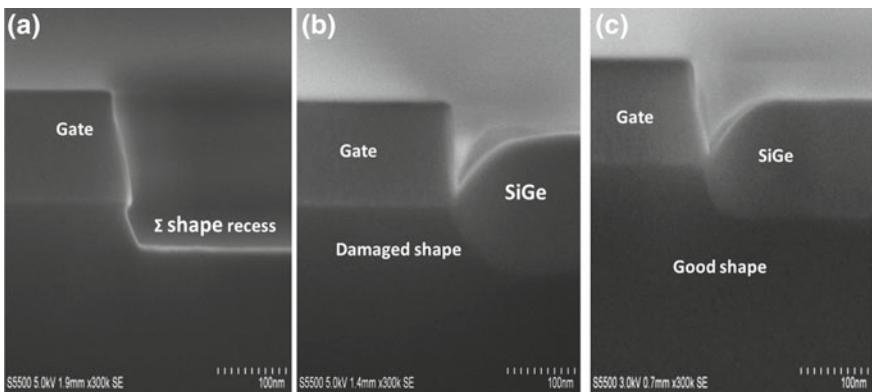
**Fig. 4.17** Cross section images of a test sample with “ $\Sigma$ ” recess **a** as formed without baking after SiGe growth and **b** the same sample but baking at 900 °C under atmospheric pressure for 3 min

the S/D recess formed by plasma etching is larger, and the thermal expansion coefficient of Si is larger than that of silicon oxide. When H<sub>2</sub> acts at high temperature, the surface is under action of silicon migration [26] changing the surface morphology. The silicon atoms on the surface migrate to the lower potential energy, which is opposite to the H<sub>2</sub> gas flow direction (as shown in Fig. 4.17b). The phenomenon of silicon migration is more pronounced at low pressure. The loss of S/D Si in the small size transistors has a great influence on the geometry of the channel, and the effect of the pre-designed channel strain enhancement is also weakened. Therefore, it is necessary to select a suitable pre-baking process in device integration.

Therefore, the atmospheric pressure is maintained and the baking temperature is continuously lowered to investigate the effect of the baking process on the S/D morphology and the film growth quality. It is found that when the temperature is lowered to 825 °C, the “Σ” morphology will be slightly deformed. The “Σ” morphology can be preserved at 800 °C, while the SiGe film can grow well (Fig. 4.18c). However, the morphology of SiGe can be affected when the baking temperature is lower than 800 °C, since the natural oxide layer is not removed. The experimental results are summarized in Table 4.1.

The Si loss at 800 °C baking for 3–7 min is almost 4 and 6 nm at 825 °C in S/D of 22 nm planar transistors.

For smaller transistors such as 16 nm FinFETs, the pre-baking process becomes more critical and important. If the Fin geometry and bulk doping concentration of



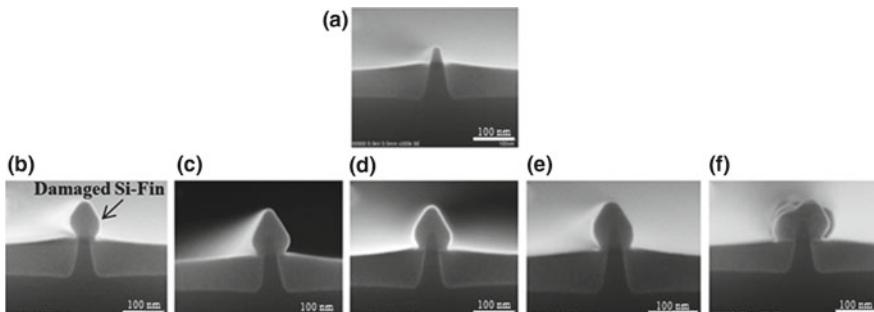
**Fig. 4.18** Effect of pre-baking temperature on S/D morphology. **a** “Σ” recess before baking, and recess after SiGe epitaxy when the thermal treatment was **b** 825 °C, **c** 800 °C

**Table 4.1** The quality of recess shape and epitaxial layer for different pre-cleaning temperatures. H<sub>2</sub> = 20 slm, pre-baking time = 7 min [14]

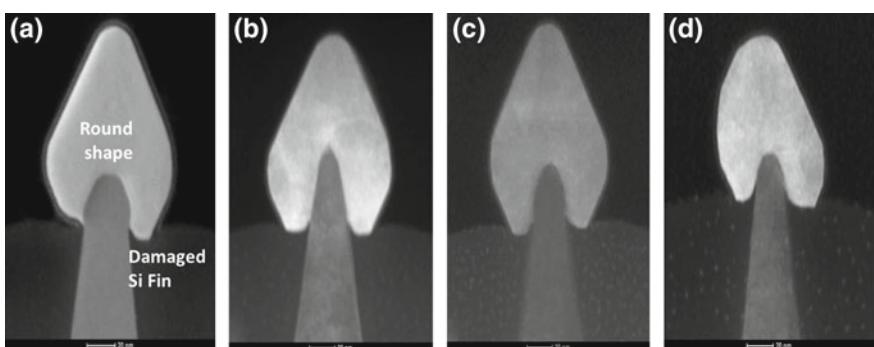
Temperature (°C)	700	750	800	825	850	900
Σ-shape recess	Preserved	Preserved	Preserved	Preserved	Failed	Failed
SiGe growth quality	Failed	Failed	Good	Good	Good	Good

the design is affected during the thermal treatment, it will affect the  $V_T$  and carrier distribution of the FinFET device [27]. Therefore, test samples are prepared for a series of different baking temperatures before the FinFET device is integrated. In these experiments, the samples are baked at different temperatures from 740 to 825 °C for 7 min (as shown in Fig. 4.19) [18]. The first micrograph shows a processed Si Fin without any epitaxial layer as reference sample (see Fig. 4.19a). The shape of the Si Fins in this sample is intact without any deformation. When the baking temperature is set at 825 °C, the interface between the top of the Si Fin and the SiGe interface can not be distinguished in SEM. It is speculated that the morphology of the top of the Si Fins has been destroyed. Further analysis has been performed by TEM in Fig. 4.20.

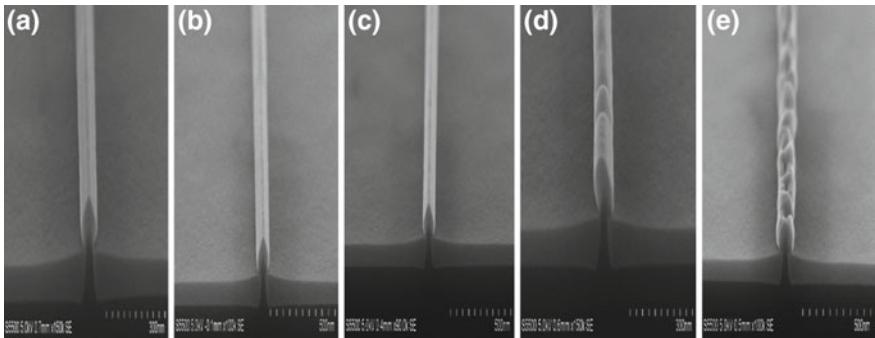
It can be clearly observed that the Si Fin has been damaged at 825 °C baking temperature (see Fig. 4.20a), and the Si loss and the Si migration to STI oxide in both directions cause the size change of Fin, but the epitaxial quality of the SiGe film is good. When the baking temperature is 800 °C and below, the interface between



**Fig. 4.19** SEM cross-section micrographs of the Si Fins with different pre-baking temperatures as follows: **a** as formed with no pre-baking, **b** at 825 °C, **c** 800 °C, **d** 780 °C, **e** 760 °C and **f** 740 °C [18]



**Fig. 4.20** TEM analysis of pre-baking temperature on Fin morphology. **a** 825 °C, **b** 800 °C, **c** 780 °C, **d** 760 °C [28]



**Fig. 4.21** Surface morphology of Fin at different pre-baking temperatures. **a** 825 °C, **b** 800 °C, **c** 780 °C, **d** 760 °C, **d** 740 °C

**Table 4.2** The effect of baking temperature on Fin morphology and SiGe growth quality [18]

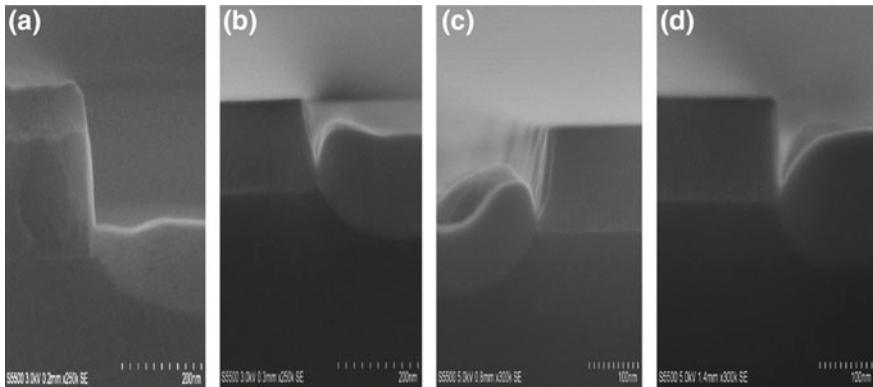
Temperature (°C)	740	760	780	800	825
Si Fin morphology	Preserved	Preserved	Preserved	Slightly deformed	Disappeared
SiGe growth quality	Poor	Poor	Good	Good	Good

Si Fin and epitaxial SiGe can be clearly observed, and the top morphology of Si Fin is maintained. However, when the baking temperature is lowered to 760 and 740 °C, the epitaxial SiGe shape is no longer symmetric along the Fin (Fig. 4.21e, f), and the quality of the epitaxy is deteriorated. This is mainly due to the presence of natural oxide layer on the surface of Si Fin which cannot be removed when the baking temperature is low.

The effect of baking temperature on Fin morphology and SiGe growth quality is summarized in Table 4.2. Similar with 22 nm planar devices, the morphology of Fin is obviously deformed as the baking temperature increases, and it can be maintained at low temperature baking, but the SiGe epitaxial quality is poor. The preferred baking temperature for 16 nm FinFET devices when integrated under atmospheric pressure is 780–800 °C, which is slightly lower than that of a 22 nm planar device. The main reason is that the exposed Si area is different in S/D regions in these transistors, which affects the gas flow when the surface is exposed to H<sub>2</sub> baking.

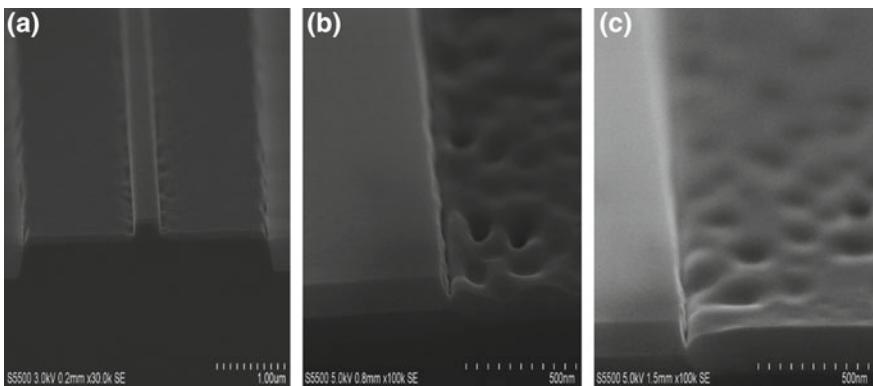
#### 4.4.2.2 Effect of Chamber Pressure on Pre-baking Process

The pre-baking process is carried out in H<sub>2</sub> in atmospheric pressure, meanwhile, the S/D morphology in low pressure baking is very different. In Fig. 4.22, the chamber pressure during baking is lowered to 10 Torr, and the sample with the “Σ” structure is baked at 800–900 °C for 7 min, respectively, and the conditions for selective epitaxial growth of SiGe are consistent.



**Fig. 4.22** Effect of different pre-baking temperature on S/D morphology at 10 Torr pressure. **a** 900 °C, **b** 850 °C, **c** 825 °C, **d** 800 °C

The experimental results show that the “ $\Sigma$ ” morphology of the baked samples at reduced pressure of 10 Torr is damaged or destroyed. The migration of silicon on the surface at reduced pressures is more significant than that under atmospheric pressure causing great changes in the morphology. At the same time, the quality of SiGe layers after baking in reduced pressure is worse than that under atmospheric pressure. The surface of the sample is uneven and rough, especially at baking temperatures of 820 and 800 °C (see Fig. 4.23b, c). The SiGe growth quality is improved at 900 °C baked samples. The main reason for this phenomenon is that when the pressure of the chamber is reduced, the H<sub>2</sub> flow rate is increased and the heat transport of the silicon surface is fast taken away, where the heat of the substrate is quickly compensated to the surface of the silicon, which accelerates the migration of silicon. Because the H<sub>2</sub> flow rate is increased, the residual Cl in the chamber will be quickly taken away, so

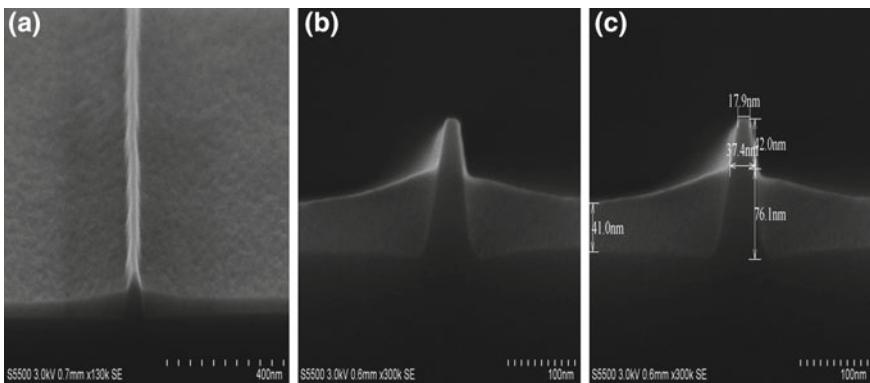


**Fig. 4.23** Epitaxial growth of SiGe after different pre-baking temperatures under 10 Torr pressure. **a** 900 °C, **b** 825 °C, **c** 800 °C

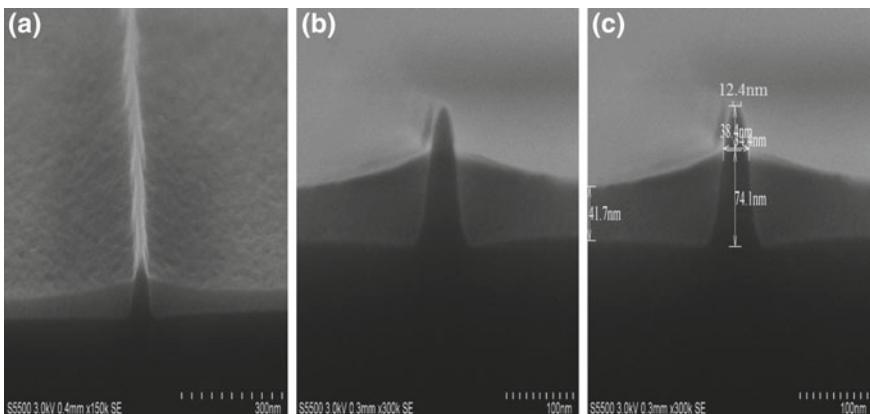
the phenomenon of Si etching is not obvious. However, the fast flowing H<sub>2</sub> and the natural oxide layer are not correlated, and the natural oxide layer of the surface is not sufficiently reduced, therefore, the overall SiGe growth quality is not satisfactory.

Pre-baking of 16 nm FinFET devices under reduced pressures has a greater impact on the morphology of Si Fins. In order to accurately evaluate the impact of pressure on the morphology and size change of Si Fins a series of samples with the same Fin structure and size are tested at 800 °C for different baking pressures. Figure 4.24a–c show the SEM images of the Fin morphology of the FinFET sample prior to epitaxy. The shape of Fin is unchanged in Fig. 4.24b. The top of Fin has an angle at both ends. The measurement of the size of the top Fin is 17.9 nm, as shown in Fig. 4.24c.

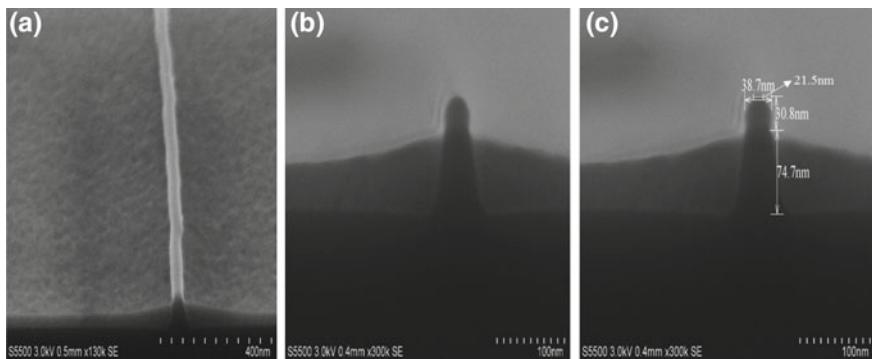
Figure 4.25a–c show SEM images of the Si Fin morphology in FinFET sam-



**Fig. 4.24** SEM images from samples with Fins before pre-baking. **a** In front view, **b** in cross-section, **c** the data of dimensions



**Fig. 4.25** Surface morphology of Fin baked under 800 °C atmospheric pressure. **a** Front view SEM, **b** SEM section, **c** SEM of measured size



**Fig. 4.26** Surface morphology of Si Fin baked at 800 °C under 20 Torr. **a** Front view, **b** cross-section, **c** measured data of dimensions

ples after pre-baking. The corners at the top of Fin disappear and become smooth (Fig. 4.25b), and the tip of Si Fins becomes sharper and smaller, only 12.4 nm is remained in Fig. 4.25c.

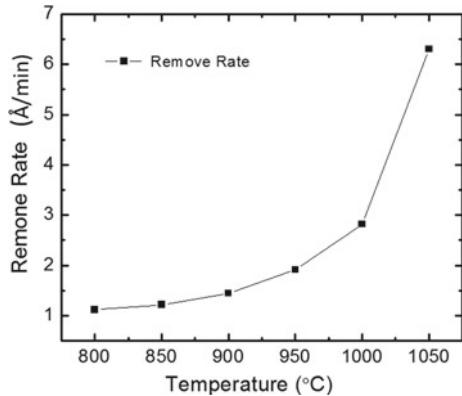
When the sample is pre-baked at a low pressure, the height of Fin became short and the surface morphology is greatly changed. As shown in Fig. 4.26b, the tip of Si Fin becomes very smooth. Comparing with Fig. 4.25a, the surface roughness of the entire Si Fin is remarkably improved in Fig. 4.26a. In addition, the Fin tip size is 21.5 nm in Fig. 4.26c, which is larger than that before baking and under normal pressure, and the width of the Fin is also slightly larger.

The effect of pressure on the surface morphology and dimensional changes of Si Fins after the pre-baking process is summarized in Table 4.3. Baking at atmospheric pressure causes Si loss and size reduction at the top of Si Fin. The main reason is that the residual Cl groups in the chamber play a major role in Si etching. The top end of Si Fin becomes smooth and large in size when are baked under reduced pressure, mainly because Si migration on Fin surface plays a major role under these conditions.

**Table 4.3** The effect of baking pressure on the morphology and dimensional changes of Si Fins

Pressure (Torr)	Before baking	760	20
Si Fin morphology	Steep with angle	Steep and sharp	Short and round smooth
Size of the top end (nm)	17.4	12.4	21.5

**Fig. 4.27** Rate of  $\text{SiO}_2$  removal baked at different temperature conditions



#### 4.4.2.3 Effect of Baking Time

The pre-baking process is carried out under certain temperature and pressure conditions, and a longer baking time is better for removal of the natural oxide layer. However, considering the influence of the S/D morphology, it is necessary to select an appropriate time to remove the surface natural oxide layer without destroying the S/D morphology. Figure 4.27 shows the rate at which  $\text{SiO}_2$  is removed at different baking temperatures at atmospheric pressure. It is calculated by measuring the change in film thickness before and after baking of  $\text{SiO}_2$  substrate. The experimental results show that the removal rate of  $\text{SiO}_2$  increases significantly with the increase of baking temperature. Therefore, the epitaxial pre-baking temperature on the bare silicon wafer is usually set to 1050 °C, and the natural oxide layer on the surface can be removed in 2 min. At 800 °C low temperature, it needs to be baked for at least 7 min to reach the same rate under 1050 °C for 1 min. For patterned substrates with different media, the removal of the native oxide layer is complicated, and the effect of the substrate pattern density effect is also considered. However, as the baking temperature rises, the effect of decreasing the baking time to achieve the same removal effect does not change.

#### 4.4.2.4 Effect of Other Factors on the Pre-baking Process

Adding different gas components to different pre-baking processes can result in different topographical changes in the sample. For example, in strain silicon device integration applications, in order to introduce strain into the channel, HCl gas is added during the pre-baking process. In this case, a certain thickness of Si is etched to form recess, then selectively epitaxially grow SiGe and Si [29, 30] to form strained recess for the channel region. In addition, in order to further reduce the pre-baking temperature during epitaxy and improve the removal efficiency of the natural oxide

layer, several reports have demonstrated that a mixture of  $\text{GeH}_4$  and  $\text{HCl}$  can be used in the pre-baking process to grow high quality SiGe at 600 °C [31].

In addition, when the silicon wafer is loaded into the reaction chamber, the temperature is set at a low temperature (less than 500 °C) to prevent the silicon from re-oxidizing with the water vapor in the air attached to the surface at a high temperature. The resulting oxide layer is more difficult to remove during baking [32, 33].

There are also equipments manufactured to integrate pre-processing steps to the epitaxy equipment. In situ cleaning is accomplished by plasma argon [34], hydrogen [35], and reaction with plasma  $\text{NF}_3$  and  $\text{NH}_3$  at low temperatures to excite  $\text{NH}_4\text{F}$  or  $\text{NH}_4\text{F}\text{-HF}$  molecules to remove surface natural oxide layers (Siconi Pre Clean) [36]. The wafer is then transferred into the epitaxial chamber, and further reducing the pre-baking temperature process to meet the requirements of full low temperature epitaxial growth.

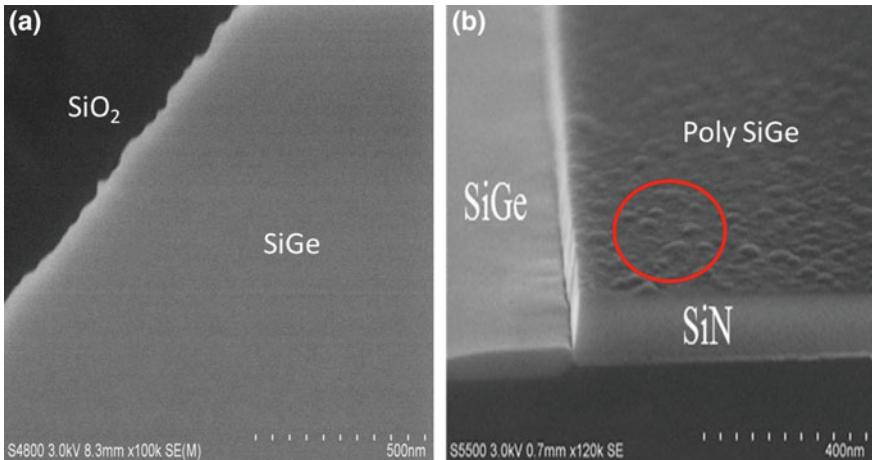
#### 4.4.3 SiGe S/D Epitaxial Selectivity

When the 22 nm planar and the 16 nm FinFET S/D device are integrated, selective epitaxial growth is required in the S/D regions, that is, there is no growth on the surface of  $\text{SiO}_2$  and  $\text{SiN}$  when the single crystal SiGe film is grown on Si. Selectivity is a key process parameter in the selective epitaxy process. The selectivity directly affects the performance of transistor.

When SiGe is epitaxially grown on the surface of different types of substrates, the nucleation rate of the grown grains is different, and there is a “difference time”. The “nucleation time” of the crystal grains on different substrates is in the order of  $\text{Si} < \text{SiN} < \text{SiO}_2$ , and nucleation growth is started only after the “nucleation time” is exceeded. In order to achieve selective epitaxial growth, sufficient Cl must be added to the reaction to inhibit nucleation of the masking layer surface at the beginning of the reaction. Moreover, the HCl introduced in the reaction can etch away the SiGe agglomerates formed on the surface of  $\text{SiO}_2$  and  $\text{SiN}$ . In order to maintain high selectivity in the SiGe epitaxial process, selective growth of SiGe is carried out at a low temperature and low pressure using a suitable gas ratio of DCS,  $\text{GeH}_4$  and HCl.

In Fig. 4.28, Si is exposed by lithography and etching on  $\text{SiO}_2$  and  $\text{SiN}$  substrates respectively, and the same SiGe selective epitaxial growth menu ( $T = 650$  °C,  $P = 20$  Torr,  $\text{HCl} = 50$  sccm) is used for epitaxial growth. As a result, there is no polycrystalline SiGe agglomerate growth on the surface of  $\text{SiO}_2$ , as shown in Fig. 4.28a; and there are many crystal SiGe agglomerates on the surface of  $\text{SiN}$ , as shown in Fig. 4.28b. The results show that the high selectivity of  $\text{SiN}$  surface under the same epitaxial conditions needs more HCl gas than that on the surface of  $\text{SiO}_2$ , because SiGe film has a fast nucleation rate on  $\text{SiN}$  surface and easy to grow polycrystalline SiGe.

The difference in nucleation rate of SiGe on different substrate surfaces depends mainly on the strength of the nucleation effect of the reactive groups adsorbed on the

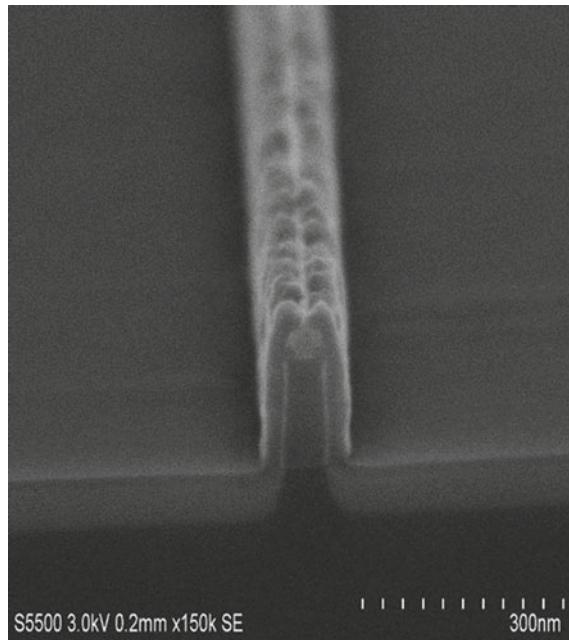


**Fig. 4.28** Selective epitaxy of SiGe in different media. **a** SiO<sub>2</sub> and **b** SiN

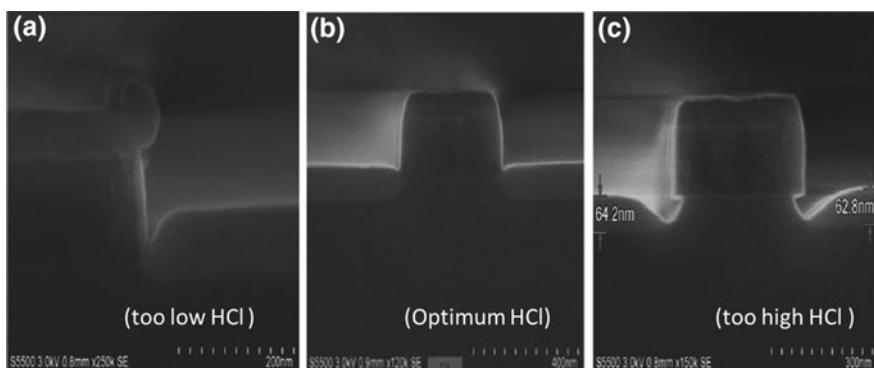
surface, and whether the other reactive atoms can be stably adsorbed on the surface of the substrate depends on whether the size of the initial nucleation reaches the critical nucleation size [37]. The critical size of nucleation is proportional to the surface tension coefficient of the film. The surface tension coefficient of the three films is: Si < SiN < SiO<sub>2</sub>. Therefore, the critical nucleation size on the Si surface is the smallest and it's the easiest to grow SiGe, while the critical nucleation size on the SiO<sub>2</sub> surface is the largest, and the SiGe nucleation on the surface is the slowest.

In device integration, selectivity of the growth is primarily regulated by the amount of reactant gas HCl. If there is no HCl, SiGe is epitaxially grown on the surface of SiO<sub>2</sub> and sidewall SiN, and the S/D are connected to the gate to cause short-circuit failure of the transistor, as shown in Fig. 4.29. To investigate the effect of HCl on selectivity, three samples are selectively epitaxially grown with different HCl flow rates and the sample cross sections are observed [14]. The epitaxial selectivity of SiGe in Fig. 4.30a is not very good. The ‘‘mushroom’’ (polycrystalline SiGe) on the sidewall of the gate is not removed, and polycrystalline SiGe agglomerates exist on the SiN sidewall. When the HCl flow rate is increased to 85 sccm, the selectivity is good in Fig. 4.30c. But the SiGe growth rate at the edge (111) and (110) crystal orientation of the S/D Si is completely suppressed, and the S/D area is not completely filled. Therefore, when the flow rate of HCl is 65 sccm, the selectivity can be satisfied, and the growth rate of SiGe can also meet the application requirements, as shown in Fig. 4.30c.

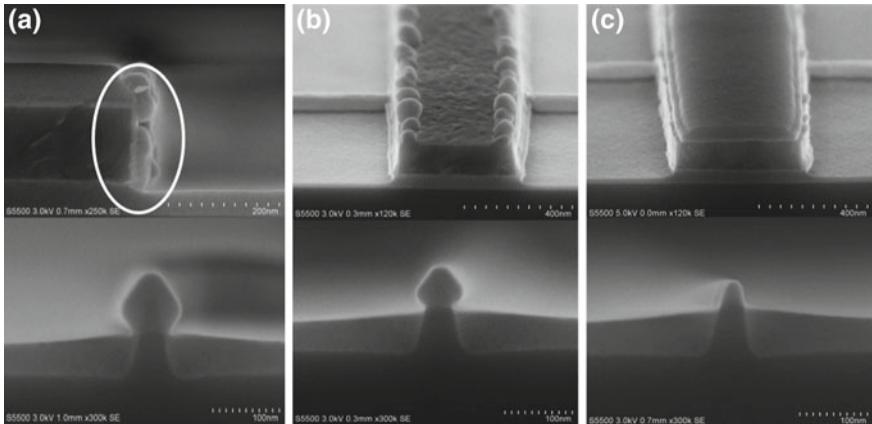
In similar, the selectivity of SiGe epitaxy in 16 nm FinFETs has been studied. But the SiGe epitaxial morphology, the residual ‘‘mushroom’’ at the top of the gate and are different with that of the planar device when the amount of HCl is different [17]. Figure 4.31 shows the effect of different amounts of HCl on the epitaxial integration of SiGe S/D of FinFET devices. It can be clearly obvious in Fig. 4.31a that the growth of polycrystalline SiGe is on the top side of the gate and the HM junction, as



**Fig. 4.29** Cross-section SEM image of selective epitaxial SiGe S/D without HCl



**Fig. 4.30** Cross-sectional SEM micrographs of the gate and S/D regions after the SiGe growth when HCl partial pressure is **a** 50 mtorr, **b** 65 mtorr and **c** 80 mtorr [14]



**Fig. 4.31** Cross-sectional SEM micrographs of S/D regions in a FINFET after the SiGe growth when HCl flow is **a** 50 sccm, **b** 60 sccm, and **c** 70 sccm [17]

well as the SiN sidewall, while the SiGe epitaxy is normal on Fin. The large flow of HCl can control the growth of SiGe in the SiN sidewall area. However, the exposed portion of the dummy gate still has a “mushroom” due to the overetching, but the growth of the SiGe film on the (111) surface of Fin is completely suppressed (as shown in Fig. 4.30c) [17]. Therefore, it is necessary to select a suitable amount of HCl, and consider the selectivity and growth rate of the epitaxy. A small amount of “mushroom” at the top of the gate is removed by the chemical mechanical polishing (CMP) process during HKMG integration and does not have much effect on the device.

The above research results show that the main factors affecting the selectivity of SiGe S/D integration selective epitaxy are following:

- (1) The amount of HCl: The amount of HCl is the key parameter affecting the selectivity. In the epitaxial process, it is necessary to select a suitable amount of HCl to maintain high quality growth of SiGe while ensuring high selectivity to  $\text{SiO}_2$  and SiN films.
- (2) “HF-last” post-processing time: When the etching time is too long, the dummy gate is exposed. And the polycrystalline SiGe can be easily grown, which increases the difficulty of selectivity.
- (3) Difference in substrate pattern density: Because the surface area of Si,  $\text{SiO}_2$  and SiN in the layout of the 22 nm planar and 16 nm FinFET device is different, the amount of HCl required in the selective epitaxy process and the “mushroom” production is not the same. The specific analysis should be combined with the actual graphics density, and the related content will be explained in the next chapter.

## 4.5 Strain Analysis of Integrated SiGe S/D in Nano Scaled Transistors

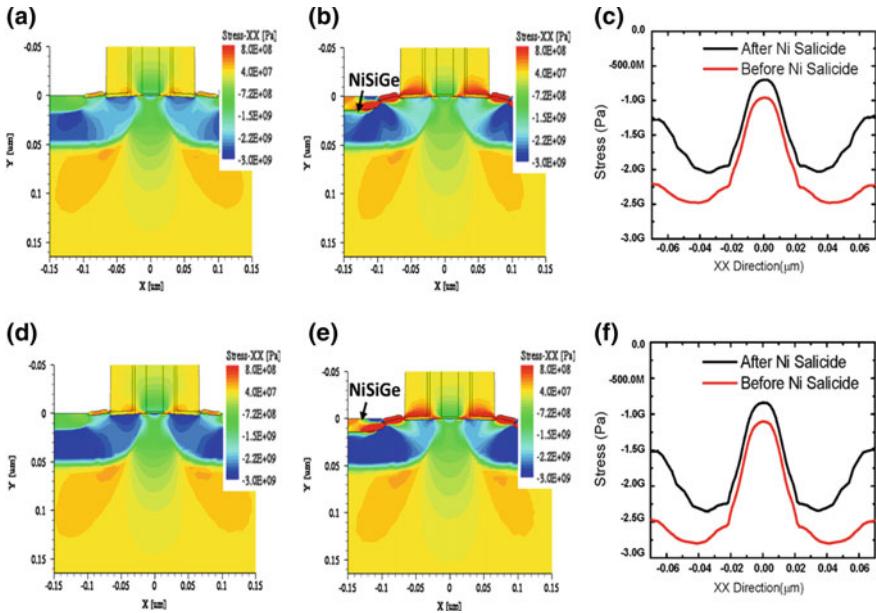
In the SiGe S/D integration process, the channel strain produced by the S/D is affected by the composition of the Ge in the epitaxial SiGe, the thickness of the film, and the subsequent integrated process. Generally, the strain generated by the SiGe S/D regions can be estimated by TCAD software simulation. The Ge composition of the SiGe in S/D regions and the strain of the film are analyzed by HRXRD which is a non-destructive method.

### 4.5.1 TCAD Simulation of Strain in Integrated SiGe S/D Transistors

This simulation study on integrated SiGe devices is based on Synopsys' TCAD (Technology Computer Aided Design) software, Sentaurus, an advanced IC process simulation software that develops and optimizes silicon-based semiconductor process technology to address current as well as process technologies development. The software is equipped with models that include individual process modules, including default parameters for data calibration from equipment vendors, and a simulated environment for predictive simulation of nanoscale CMOS processes.

In the entire SiGe S/D integration, maintaining the process and performance consistency on the silicon wafer is of great importance in chip manufacturing. In general, uniformity of etching, SiGe epitaxial quality, and metal silicide formation in the process are the most important issues for device performance. In transistor design, the carrier mobility in the channel region is one of the most important parameters, and the magnitude of the strain in the channel region directly determines the size of the parameter. The compressive strain at the channel of the PMOS device is mainly introduced by the SiGe S/D. In order to obtain high carrier mobility, it is necessary to integrate a higher Ge composition SiGe strained layer. In addition, the formation of the Ni silicon germanide process in the S/D regions may cause strain relief. This is mainly due to the consumption of Si atoms and pushing out Ge atoms during the silicidation of Ni, resulting in strain relaxation. Therefore, it is very necessary to use the simulation program to understand the strain distribution initially from SiGe epitaxy and then variation of strain in the integration process, which helps to carefully design the SiGe S/D film structure.

Figure 4.32a-f show the results of strain simulation analysis of SiGe S/D with different Ge components in a 22 nm planar PMOS device before and after NiSiGe formation. The simulation results show that the strain generated after epitaxial SiGe is uniformly distributed in the channel region, and the channel strain generated by the Ge composition of 0.35 and 0.4 is 1.0 GPa and 1.3 GPa, respectively. A  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layer on the top of the SiGe S/D region is designed in these transistors as a sacrificial

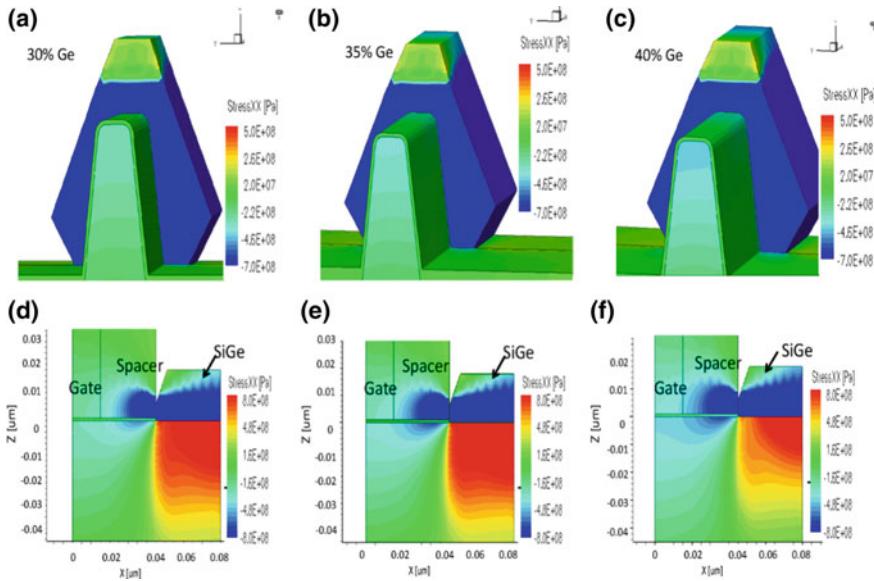


**Fig. 4.32** Strain simulation of SiGe in S/D regions with different Ge contents in 22 nm planar transistor before and after NiSiGe formation: **a**  $\text{Si}_{0.65}\text{Ge}_{0.35}$  as grown layer, **b** NiSiGe formation of previous sample, **c** channel stress distribution and **d**  $\text{Si}_{0.6}\text{Ge}_{0.4}$  as grown layer, **e** NiSiGe formation of previous sample and **f** channel stress distribution [38]

layer, but still partial strain release occurs during NiSiGe formation, and the channel strain is reduced to 0.6 and 0.8 GPa after the process [38].

In a subsequent integrated process, the PMOS device can continue to enhance the strain of the channel by using high-stress SiN cap layer. The results of these simulations can be used to optimize SiGe integration processes such as Ge composition selection, channel strain and S/D SiGe film design, NiSiGe formation temperature and thickness, etc. These parameters directly affect strain relaxation. TCAD simulation can also predict the relationship between strain relaxation and the thickness of the formed NiSiGe layer, so it is necessary to control the self-aligned silicidation process to maintain the strain in the channel region.

When 16 nm FinFET SiGe S/D are integrated, the strain in channel has been generated by SiGe in S/D is not as large as that of planar devices. The 16 nm FinFET device in this paper does not have any integrated silicidation process, therefore, in order to further study the influence of different Ge components in the S/D, and the effect of the pattern density effect on the Ge composition distribution during the selective epitaxy, strain simulation results were applied (see in Fig. 4.33a–f). The results show that after epitaxial SiGe on Si-Fin, the strain is uniformly introduced into the channel region, and the strain on the channel increases as the Ge composition increases. When the Ge compositions are  $x = 0.3, 0.35$ , and  $0.4$ , the channel strain is about 0.4 GPa, 0.6 GPa, and 0.8 GPa, respectively. The simulation results of channel strain generated



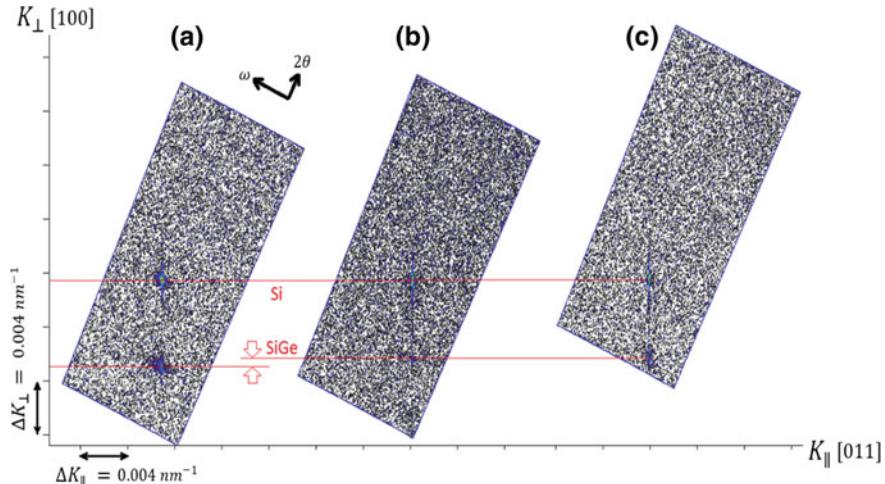
**Fig. 4.33** Simulation analysis of SiGe strain in S/D for different Ge components in 16 nm FinFET devices: **a, d**  $\text{Si}_{0.7}\text{Ge}_{0.3}$ , **b, e**  $\text{Si}_{0.65}\text{Ge}_{0.35}$ , **c, f**  $\text{Si}_{0.6}\text{Ge}_{0.4}$  [17]

by different Ge components can provide a basis for the subsequent study to analyze the effects of pattern density effects in selective epitaxy.

#### 4.5.2 HRXRD Analysis of Strain of Integrated SiGe S/D Devices

In the previous chapter, XRD is a fast and non-destructive method for studying strain in SiGe films. Therefore, we performed high-resolution X-ray diffractometry (HRXRD) on the 22 nm planar and 16 nm FinFET device with SiGe in S/D process to analyze the Ge composition distribution and the strain changes during integration process in different regions of the SiGe film on the wafer. The results of the test are used to simulate and contrast curves in the Takagi-Taupin equation to obtain highly accurate experimental data analysis [39].

In the 22 nm planar transistor structure, the samples are analyzed by HRXRD in different process steps. In order to accurately analyze the defects and strain of the epitaxial SiGe film, asymmetrical (113) reflection is used to generate high-resolution reciprocal space graphics (High-resolution reciprocal lattice mapping or HRRLM). The horizontal lattice mismatch ( $f_{\parallel}$ ) and the vertical lattice mismatch ( $f_{\perp}$ ) of the SiGe film epitaxial growth, and the effect of the Ni silicide formation process on the strain of the SiGe film can be analyzed from the HRRLM. The HRRLM analysis is

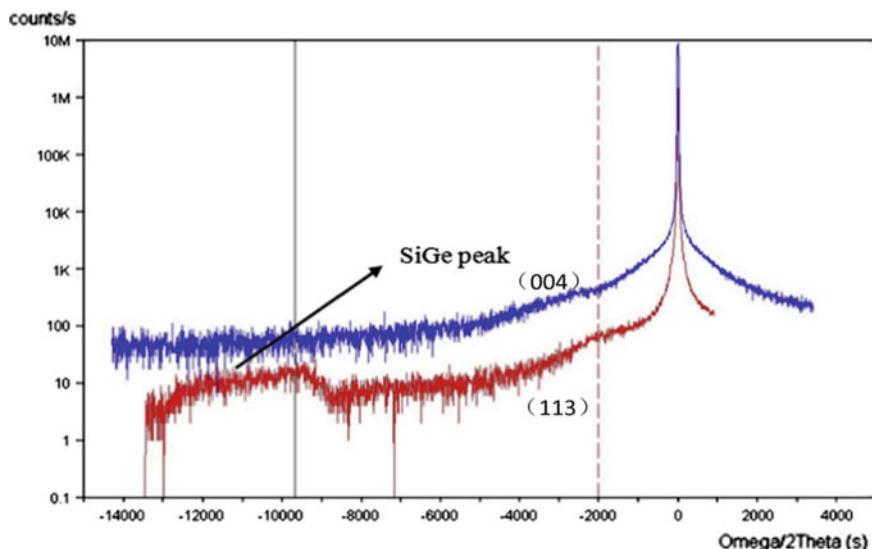


**Fig. 4.34** HRLRM of 22 nm planar device SiGe S/D film. **a** Intrinsic SiGe, **b** B-doped SiGe, **c** previous sample with a cap layer low-content SiGe layer to form NiSiGe [14]

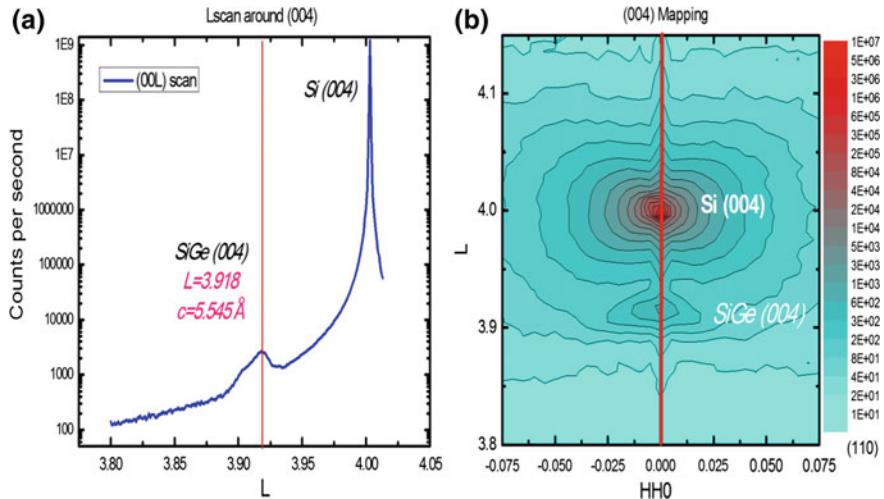
performed on the three samples in Fig. 4.34 [14]. Figure 4.34a is an intrinsic SiGe film without doping selective epitaxy. SiGe peak has a broadening in  $\omega$ -direction and the peak has an asymmetric feature with Si peak in  $K_{\parallel}$ -direction. This is an indication of strain relaxation of the SiGe layer. This was expected since the layer thickness (220 nm) exceeds the critical thickness for  $\text{Si}_{0.65}\text{Ge}_{0.35}$ . The  $f_{\perp}$  and  $f_{\parallel}$  values are obtained as 19,370 and 885 ppm, respectively, which result in ~8% strain relaxation. This asymmetric feature of SiGe layer is not observed for the B-doped sample in Fig. 4.34b (as well as in Fig. 4.34c). The SiGe layer is shifted towards Si substrate due to strain compensation caused by boron atoms in SiGe matrix [40]. This shift is estimated to be 1500 ppm which corresponds to a substitutional boron concentration of  $1.8 \times 10^{20} \text{ cm}^{-3}$  [39, 40]. It is emphasized here that this value may differ from atomic boron concentration which can be provided by secondary ion mass spectrometer (SIMS) technique. Due to small size of openings there is no possibility to perform such analysis for these SiGe layers. The measured  $f_{\perp}$  and  $f_{\parallel}$  values for this sample are 17,870 and 30 ppm, respectively, which indicate fully strained SiGe layers. Finally, in Fig. 4.34c, a SiGe layer with low Ge content ( $x$  about 0.2–0.25) is added as a strain sacrificial layer to the sample in (b) in order to reduce the influence of the Ni silicide formation process on the S/D SiGe strain. The stability of the NiSiGe silicide is poor when the Ge composition is higher than 30% [41]. The results of the comparison of (b) and (c) show that the peaks of Si and SiGe do not drift and no new characteristic peaks appear, which indicates that the low concentration SiGe layer is consumed by NiSiGe without affecting the strain core layer of the lower layer ( $\text{Si}_{0.65}\text{Ge}_{0.35}$ ). The design of such a SiGe strain core layer and the strain sacrificial layer facilitates the process integration of the NiSiGe and maintains the strain of the S/D without large drawback during the process.

In the 16 nm FinFET device structure to characterize the epitaxial SiGe film grown on Si Fins by HRXRD is not an easy task. This is due to small size of the SiGe layers. In addition, the area of the X-ray beam spot of the ordinary XRD tool is large, and the  $\text{SiO}_2$  at both ends of the Fin is also an interference for the test. In order to improve the sensitivity of XRD to the defect and strain of epitaxial SiGe film on the Fins, rocking curves were performed at (113), instead of (004) reflection. The incident beam angle for (113) reflection is as low as  $2.6^\circ$  compared to  $34.1^\circ$  for (004). In addition, a typical scan of  $2^\circ$  in (113) reflection makes a grazing angle where many chips can be covered by X-ray beam and contribute to XRD signal. As a result, the SiGe peak is intense enough at (113) reflection and can be analyzed to estimate the strain amount. At the same time, the Si-Fin dense region is selected as the XRD scanning region to enhance the test effect. The (004) scan illustrates a peak with very low intensity whereas (113) RCs have peaks with sufficient intensity for strain measurement in Fig. 4.35, and this peak is broadened which is a sign of strain distribution of SiGe layers [18]. This is due to either the strain relaxation over different facet planes or variation of Ge content over the regions of the chip as a result of pattern dependency.

The FinFET structure characterization of strain and Ge content are carried out by HR-XRD at facilities in Singapore Synchrotron Light Source (SSLS) and Shanghai Synchrotron Radiation Facility (SSRF). The area of the XRD beam spot is  $2 \text{ mm}^2$ , which can effectively improve the intensity during scanning. Figure 4.36a, b show the XRD curve and HRRLM using a symmetry (004) scan. The peak position of SiGe in Fig. 4.36a can be clearly detected. The peak position of SiGe layer and the



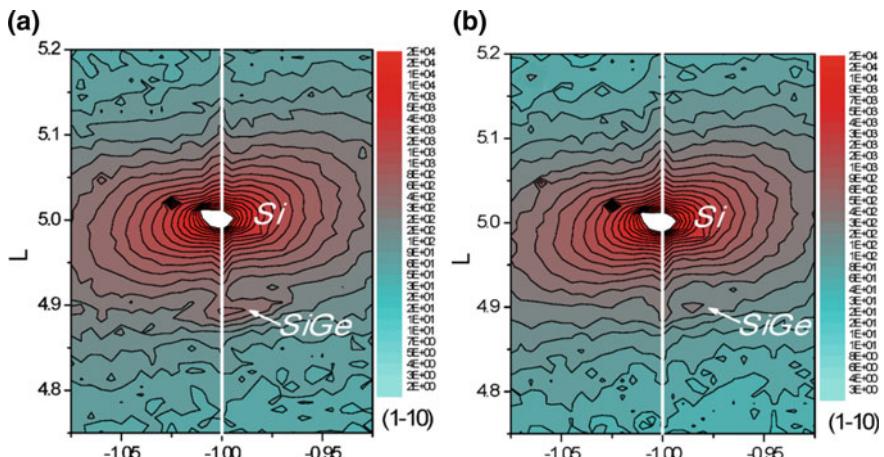
**Fig. 4.35** HRXRD rocking curves measured at (004) and (113) reflections (blue- and red-colored scan, respectively) from arrays of Si fins over a test chip [18]



**Fig. 4.36** XRD analysis of SiGe in 16 nm FinFET device structure. **a** (004) scan curve and **b** (004) HRLLM

peak of Si Fins in HRLLM are symmetric along a line in Fig. 4.36b, and there is no offset indicating that SiGe layers are strained.

In order to detect defects and the Ge composition in the SiGe layers, the samples are scanned by asymmetric ( $\bar{1}15$ ), at the center and edge areas of the wafer to verify whether the distribution of Ge is uniform. The SiGe peak positions of these two regions in Fig. 4.37 are offset from the peak position of Si, indicating that the SiGe in both regions has partial strain relaxation. The SiGe relaxation in the edge region is



**Fig. 4.37** HR-RSMs around ( $\bar{1}15$ ) from arrays of Si-fins located at **a** the center and **b** the edge of 200 mm wafer, respectively [17]

larger than that in the central region. The composition of Ge in the center is 35% and the edge area is 40% (as shown in Fig. 4.37a), mainly because the Si Fin arrangement in the edge region is sparse and covered with more oxide layer [17].

In summary, we can simulate the strain variation of SiGe layers due to processing by using the simulation tool. The simulation results help us to improve the integration process and to maintain the strain of the SiGe film during the process integration process. The XRD technology is also a non-destructive tool for quick measurements of SiGe film strain and Ge composition in nano scaled transistor structures. In particular, Synchrotron facilities can be applied to study the strain in 16 nm node technology.

## 4.6 TEM Analysis of Integrated SiGe S/D Devices

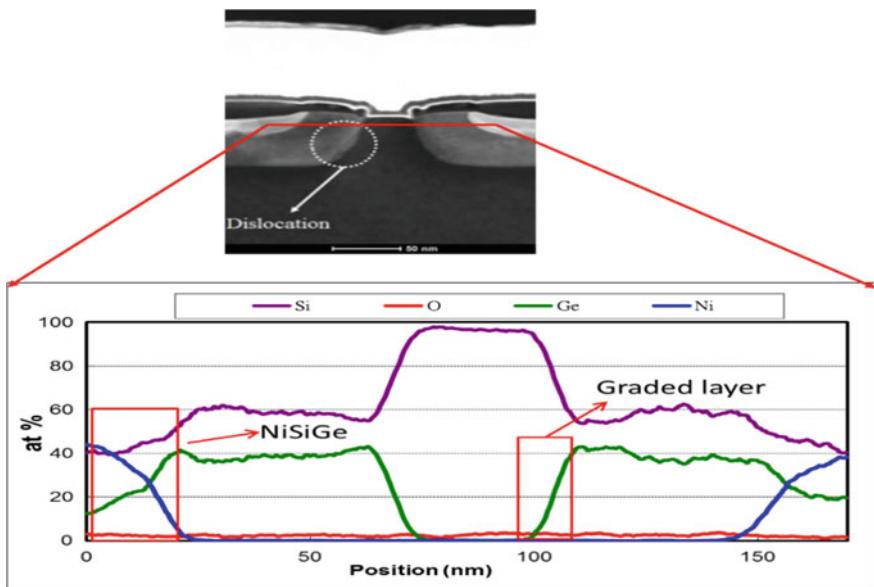
The thickness of the epitaxial SiGe and NiSiGe film layers, the defect density of the film and the quality at the epitaxial interface can be accurately analyzed by TEM. EDX analysis can measure the distribution of Ge in the film and the oxygen content at the interface. The EDX test is realized by analyzing the X-ray wavelength and intensity of the element characteristic emitted by the sample, determining the element contained in the sample according to the wavelength, as well as the relative content of the element in the film according to the intensity.

### 4.6.1 TEM Analysis of SiGe S/D in 22 nm Planar Devices

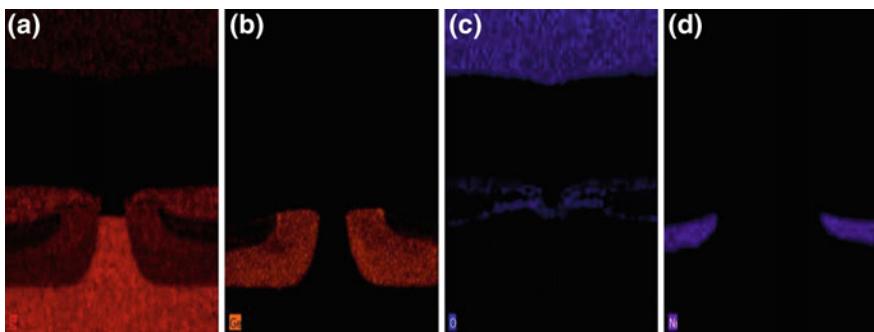
Figure 4.38 demonstrates a TEM analysis of the SiGe S/D and a component analysis of the EDX line scan of a 22 nm planar transistor.

The defects in the SiGe film can be observed from the TEM image. The EDX line scan of the S/D regions (horizontal red line in the TEM image) shows that the strained SiGe buffer layer is initially grown according to the pre-design, and the Ge content is graded from 0 to 0.35–0.4, then a constant content of 0.4 is grown as a strained core layer. The uppermost layer is a strained layer with Ge content of 20% as a sacrificial layer for the formation of NiSiGe.

In order to further analyze the content of O and the distribution of other elements at the interface between SiGe and Si during epitaxy, EDX analysis is performed on the above samples. As shown in Fig. 4.39c, the interface between Si and SiGe S/D regions does not have a signal of O, indicating that the surface natural oxide layer has been removed by the pre-baking process. Ge in (b) is uniformly distributed in the SiGe film. The NiSiGe in (d) consumes SiGe cap layer with low Ge content and does not affect the strained core layer [18].



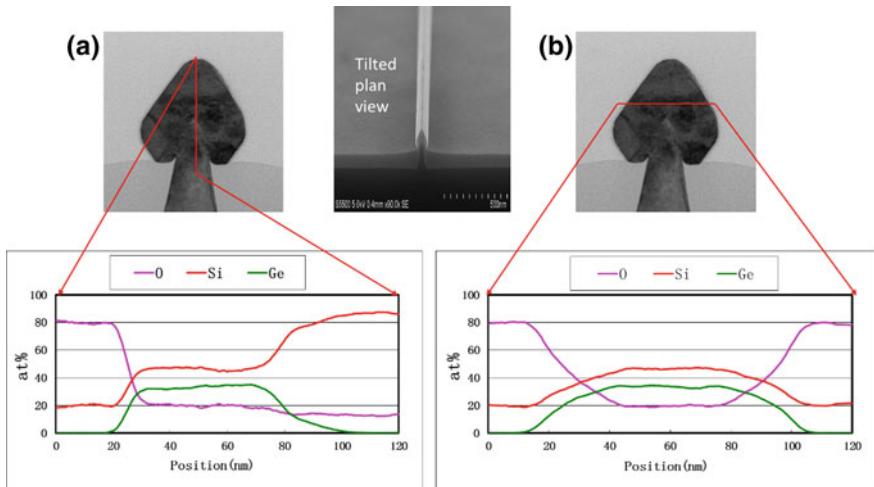
**Fig. 4.38** TEM and EDX line scan of elemental analysis in 22 nm node transistor with SiGe S/D [15]



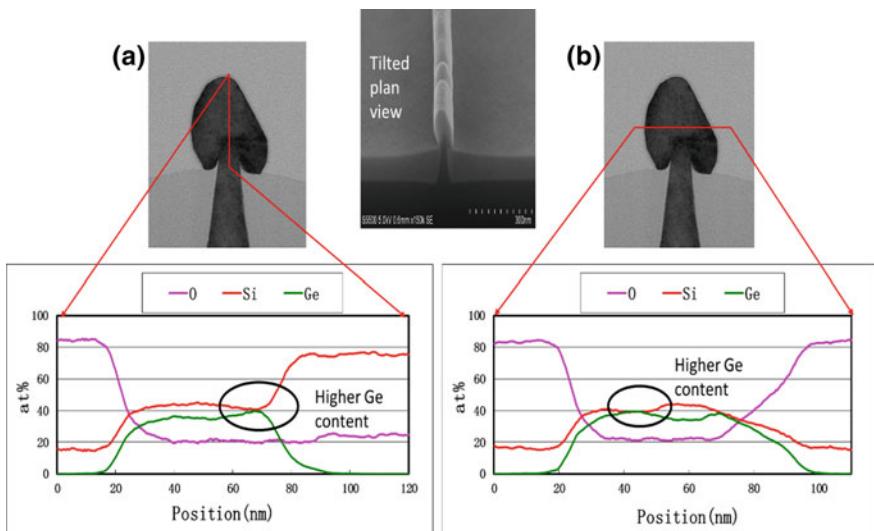
**Fig. 4.39** EDX element analysis of SiGe S/D in 22 nm planar transistors. **a** Si, **b** Ge, **c** O, **d** Ni [18]

#### 4.6.2 TEM Analysis of 16 nm FinFET SiGe S/D Devices

In Figs. 4.40 and 4.41, the epitaxially grown SiGe samples which are treated with two different pre-baking temperatures are characterized by TEM and EDX line scanning. The quality of the epitaxial SiGe film on Si Fins and the distribution of Ge content in different directions are analyzed. The composition of the oxygen in the two figures is very high (about 20%). The main reason is that the Si Fins are very small and it is easily interfered by  $\text{SiO}_2$  at both ends of Fin during EDX line scanning, which



**Fig. 4.40** TEM with EDX analysis in **a** vertical and **b** horizontal orientations for the SiGe layer grown on Si fin when pre-baking temperature is 800 °C [18]



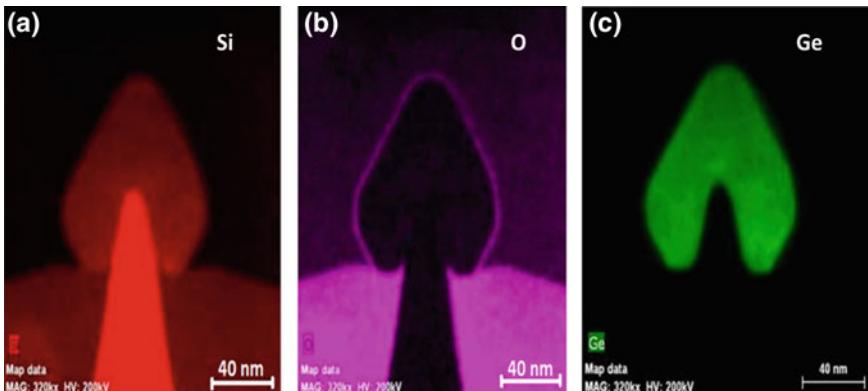
**Fig. 4.41** TEM with EDX analysis in **a** vertical and **b** horizontal orientations for the SiGe layer grown on Si fin when pre-baking treatment is 760 °C [18]

affects the content of Si component. Therefore, it would be more reasonable to add a 20% error in the oxygen component to the Si component test curve. Ge has a large atomic number and is less susceptible to interference in EDX scan.

If the SiGe film has good growth quality on Si-Fins, it will show a symmetric distribution of the morphology at both ends of Si-Fin. Whether the shape is symmetrical can indirectly reflect whether the natural oxide layer on the upper surface of Si Fin is cleaned or not. For example, the SiGe film grown after pre-baking at 800 °C in Fig. 4.40 is uniformly symmetric at both ends of Fin, while the SiGe film grown after pre-baking at 760 °C in Fig. 4.41 has asymmetric ends of Fin.

In addition, the SiGe contains stacking faults at the border between (111) and (001) facet planes (see Fig. 4.40) [18]. The maximum content of Ge is about 36%, and the highest Ge content at 760 °C is about 40%. The difference in Ge composition is mainly due to the difference in selectivity in the epitaxial process when baked at lower temperatures. However, the Ge components tested by EDX are unable to reflect the strain condition of the SiGe film.

Since there is a clear oxygen peak signal, in order to accurately verify the distribution of the analyzed oxygen, especially at the interface between Si and SiGe, it is necessary to further analyze the distribution of oxygen by EDX mapping. In the pattern of Si shown in Fig. 4.42a, Si is uniformly distributed in SiGe, SiO<sub>2</sub> and Si Fin, and the oxygen in (b) is only distributed in the filled dielectric SiO<sub>2</sub> and on the surface of the SiGe film. The Ge in (c) is only distributed in the SiGe film. Therefore, the EDX mapping shows that the oxygen is mainly from the SiO<sub>2</sub> film, not the interface between the SiGe film and Si [18].



**Fig. 4.42** EDX element mapping of SiGe S/D in 16 nm FinFET. **a** Si, **b** O, **c** Ge [18]

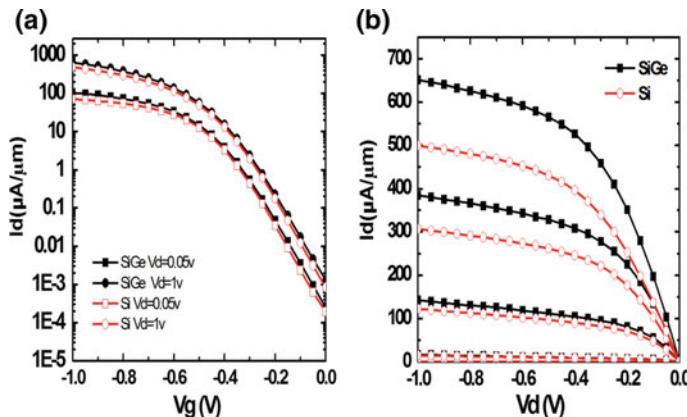
## 4.7 SiGe S/D Electrical Performance Verification

### 4.7.1 Electrical Performance Verification of 22 nm Planar SiGe S/D Devices

The 22 nm planar PMOS devices are successfully integrated with SiGe S/D and HKMG modules. The electrical measurements from test samples show that the  $I_{on}$  of the PMOS device with SiGe in S/D has a 30% performance improvement compared with traditional silicon device [15].

Figure 4.43a shows the  $I_d$ - $V_g$  transfer characteristic curves and (b) shows the  $I_d$ - $V_d$  output characteristic curves. The results indicate that saturation drive current of SiGe S/D device increases from 488 to 639  $\mu A/\mu m$ , while the  $I_{off}$  changes from 0.83 to 1.32 nA/ $\mu m$ , mainly due to SiGe S/D replacement processes and defects present in the film. The inserted Table 4.4 summarizes the device's electrical performance comparisons between 22 nm bulk PMOS SiGe S/D and Si device [15].

Figure 4.44 shows the  $I_{on}$ - $I_{off}$  switch ratio of the different gate lengths of the device. It can be seen from the figure that as the gate length decreases, the performance of transistors with SiGe in S/D improves more mainly due to the induced strain in channel becomes larger as the device size shrinks.

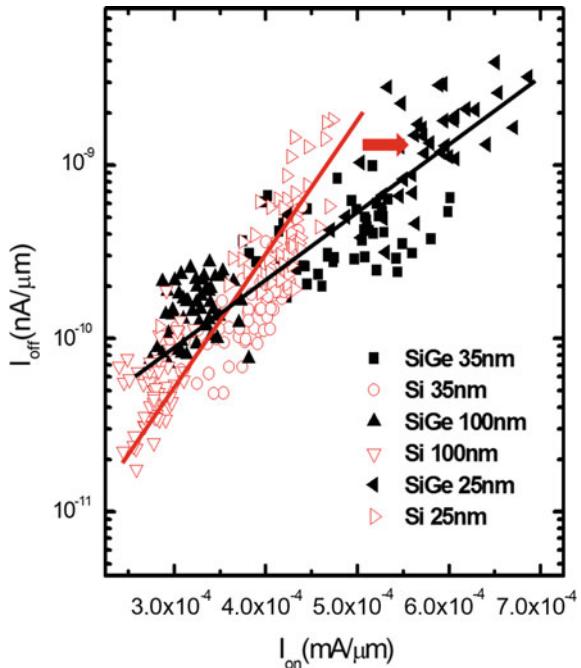


**Fig. 4.43** The **a**  $I_d$ - $V_g$  transfer, **b**  $I_d$ - $V_d$  output characteristic curves of 22 nm planar devices with SiGe in S/D compared to Si in S/D [15]

**Table 4.4** Electrical performance test summary of 22 nm planar SiGe S/D devices [15]

Parameter	$L_g$ (nm)	$I_{on}$ ( $\mu A/\mu m$ )	$I_{off}$ (nA/ $\mu m$ )	$V_{tlin}$ (V)	$V_{tsat}$ (V)	DIBL (V/V)	S.S. (mV/dec)
Si S/D	25	488	0.83	-0.41	-0.33	77	85
SiGeS/D	25	639	1.32	-0.40	-0.32	76	87

**Fig. 4.44** The  $I_{on}$ - $I_{off}$  switch ratio diagram of 22 nm planar PMOS SiGe S/D device



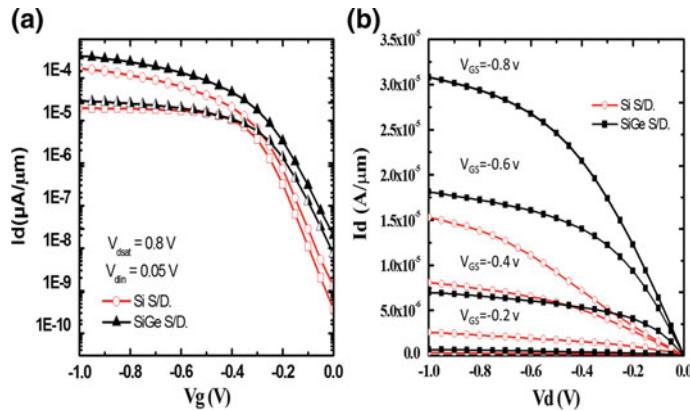
#### 4.7.2 Electrical Performance of 16 nm FinFET SiGe S/D Devices

Comparing and analyzing the electrical performance of 16 nm FinFET PMOS devices with and without SiGe in S/D show that SiGe in S/D improves device performance. The electrical performance of a SiGe S/D FinFET PMOS with 30 nm gate length are shown in Fig. 4.45.

The results in Fig. 4.45 show that the performance of FinFET devices with integrated SiGe S/D has been significantly improved. There are two main reasons:

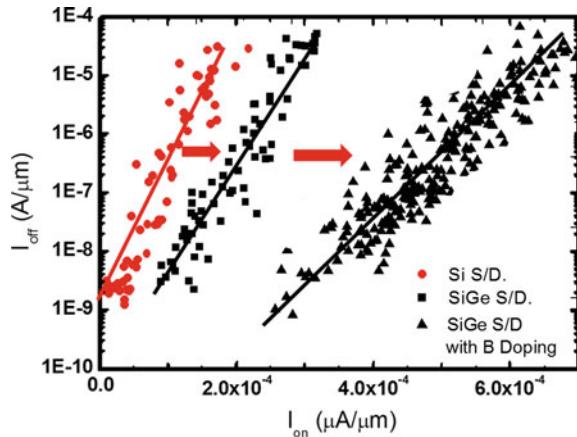
- (1) The SiGe S/D strain in the channel enhance the channel carrier mobility. The mobility of devices with Ge components of 0.35 and 0.4 is  $81 \text{ cm}^2/\text{V s}$  and  $88 \text{ cm}^2/\text{V s}$ , respectively. The mobility has largely increased compared with Si S/D device ( $\sim 70 \text{ cm}^2/\text{V s}$ ).
- (2) SiGe effectively increases the contact area of the S/D, reducing the contact resistance, and greatly increasing the drive current of the FinFETs.

Figure 4.46 shows the diagrams from  $I_{on}$ - $I_{off}$  switch ratio of 16 nm FinFET PMOS devices. The results show that the performance improvement of integrated SiGe S/D devices with in situ doped B is more obvious than that of intrinsic SiGe S/D transistors. The main reason is that although some strain is compensated by doping B, the decrease in S/D contact resistance increases  $I_{on}$ . It can be seen that the decrease



**Fig. 4.45** a  $I_d$ – $V_g$  and b  $I_d$ – $V_d$  output characteristic curves of 16 nm FinFET PMOS device with SiGe S/D compared to Si S/D

**Fig. 4.46** The  $I_{on}$ – $I_{off}$  switch ratio diagram of 16 nm FinFET PMOS integrated different S/D devices



in SiGe S/D contact resistance is the most important factor for the performance improvement of the 16 nm FinFET device.

## 4.8 Summary of This Chapter

This chapter presents the integration of SiGe S/D strain technology as the size of transistors shrinks, and the difficulties and challenges in process integration. The SiGe S/D integration scheme and the formation of special S/D features of 22 nm planar and 16 nm FinFET devices are introduced. This chapter focuses on different

issues about key processes affecting the integration of SiGe S/D in 22 nm planar and 16 nm FinFET devices includes the following aspects:

- (1) Optimization of interface cleaning method before epitaxy. It is found that the addition of DHF solution rinsing before SPM cleaning helps to improve the removal of organic groups on the S/D Si surface, effectively improving the quality and stability of the epitaxial film.
- (2) The influence of pre-baking process on S/D morphology during epitaxial process is systematically studied. It is found that the main reason for the Si loss in S/D during high temperature baking is due to the residual Cl group in the chamber which etches Si changing the shape of the S/D. The main reason for the change in morphology during low-pressure baking is the migration of surface Si atoms, which causes the size of Fin to become larger and the surface to become smoother. The ability to remove oxide layers at different temperatures during pre-baking is further investigated as well.
- (3) The effect of the amount of HCl on the selectivity of SiGe growth is analyzed. In the integration, an appropriate HCl amount has to be selected, otherwise a “mushroom” shape SiGe poly is formed on the top of dummy gate. The key factors affecting selectivity are summarized and analyzed.
- (4) The strain variation in the SiGe film during the device process is analyzed by TCAD simulation and HRXRD technique. XRD is used to characterize the Ge composition and strain in the SiGe film on Si Fin. In addition, the TEM and EDX are used to characterize the SiGe S/D regions of the 22 nm planar and 16 nm FinFET devices. The defects in the film, the composition of Ge and the distribution of interface elements are characterized. The integrity of the grown SiGe layers in terms of strain in core layer and in sacrificial layer is studied when the SiGe S/D are integrated.
- (5) The electrical performance of 22 nm planar and 16 nm FinFET SiGe S/D devices is been studied. The results show that the SiGe S/D strain improves device performance. The improvement of performance of 16 nm FinFET with SiGe S/D is related to reduction of contact resistance in S/D regions.

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# Chapter 5

## Pattern Dependency of SiGe Layers

### Selective Epitaxy Growth



## 5.1 Introduction

The pattern dependency has a great impact on SiGe selective epitaxial growth using RPCVD technology, not only on the quality of SiGe films, but also on the performance of transistors. Thus, the research on pattern dependency of SiGe layers grown selectively in 22 nm planar structure and 16 nm FinFET is necessary, which will provide a good foundation for large-scale advanced device integration and application.

### 5.1.1 *The Generation of Pattern Dependency*

Pattern dependency means that the SiGe layer profile depends on (local or global) variation of the pattern in selective epitaxial growth. The growth rate of SiGe thin films, germanium content and doping concentration all change with the patterns. This dependence originates from the kinetics of gas molecules, the wafer architecture (oxide or nitride) and non-uniform layouts of the wafers. The wafer architecture refers to the isolation materials and their thickness, whereas the layout concerns shape, size, and density of the openings over a chip [1–3]. As shown in Fig. 5.1, three selective Si substrate areas (a, b and c) are exposed with  $S_a > S_b > S_c$ . After epitaxy growth, the thickness of Si films will be different since the growth rate is affected by the pattern dependency ( $R_c > R_b > R_a$ ).



**Fig. 5.1** The schematic image of epitaxial growth with different exposed Si areas

In conclusion, the pattern dependency is closely related to the mechanism of SiGe selective epitaxy growth using RPCVD, which is in conformity with the fluid mechanism of reaction gases. The film growth process includes the process of gas adsorption at the surface of wafer, nucleation and by-product desorption. According to the interpretation of reaction rate by CVD gas reaction mechanism, the reaction rate on the surface of silicon wafer is controlled by two kinds of mechanism: mass transfer control and reaction control [4]. In selective epitaxy, the pattern dependency is mainly caused by the fact that when the gas phase reaction rate is controlled by mass transfer, it depends on the amount of reaction gas on the surface. Different silicon exposed areas will lead to the difference in the amount of reaction gas consumed locally, which makes the difference in the growth rate. When the gas phase reaction rate is mainly controlled by the surface reaction, the amount of reaction gas is no longer the determining factor of growth, so it is easier to suppress or eliminate the pattern dependency. Therefore, one method to reduce the pattern dependency of the selective epitaxy growth of SiGe layers is to control the process conditions, making reaction control to be the dominance instead of mass transfer control. For example, adopting lower growth temperature has a beneficial effect on reducing the pattern dependency. The effects of other factors will be discussed in detail in the next section.

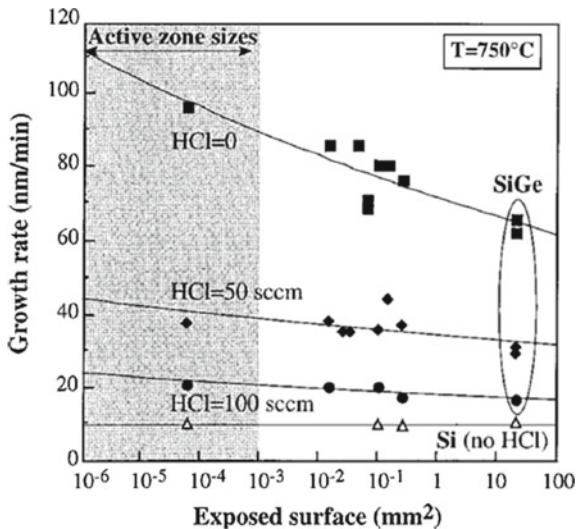
According to the influence of the reaction area, the pattern dependency in selective epitaxial growth can be divided into Micro Loading Effect and Macro Loading Effect. Micro loading effect means that in the same chip of a wafer, due to the differences of device arrangement and design, the exposed Si area is different, which will lead to different SiGe profiles (layer thickness, Ge content and doping level) [5]. Macro loading effect means the SiGe profile over different parts of a chip (or wafer) will be different due to the differences of Si exposed area. Thus, the pattern dependency should be investigated and removed, which brings negative impact to the device integration.

### 5.1.2 Recent Progress of Pattern Dependency

Since the discovery of pattern dependency, researchers have used various techniques and methods to suppress the generation and influence of the effect. Unfortunately, none of these methods could effectively remove the pattern dependency of the growth [1, 6]. In 1997, Bondnar has proposed using high HCl partial pressure to minimize the dependence of the SiGe growth rate on window size. As shown in Fig. 5.2, the selective SiGe growth rate tends to be consistent over different Si exposed areas. However, they didn't evaluate the effect on SiGe epitaxial growth quality and selectivity by increasing HCl partial pressure. In epitaxial reaction, Increasing HCl partial pressure can improve the selectivity of the medium, but it will inhibit the growth of SiGe, which is prone to produce defects in epitaxial process [7]. Therefore, the quality of the film cannot meet the requirements of device application.

Other methods, like decreasing the total growth pressure from 20 to 10 torr can make more uniform SiGe profiles in selective epitaxy [8]. However, this method has

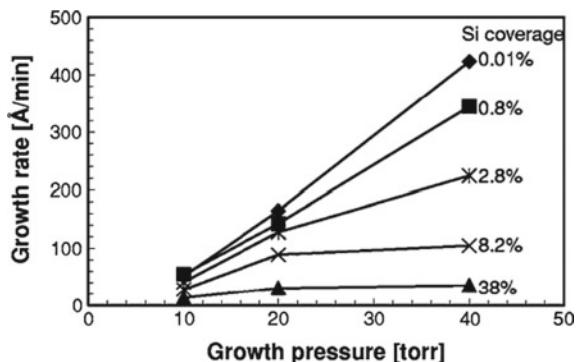
**Fig. 5.2** The selective growth rate at exposed surface with different HCl partial pressure [7]



a limited effect on improving the pattern dependency over wide range of exposed Si area. As shown in Fig. 5.3, when the reaction pressure is reduced to 10 torr, though the growth rate of SiGe on different Si area is decreased compared with that of high pressure, there still are big differences. Reducing the total pressure in the reaction chamber also tries to drive the growth to be controlled by surface reaction.

There are also studies on using high H<sub>2</sub> carrier gas flow and low reaction pressure to improve the pattern dependency [1]. However, high H<sub>2</sub> carrier gas flow is not conducive to the growth of high-component Ge and high-concentration doping, which are necessary for the integration application of SiGe S/D devices. In addition, high carrier gas flow and low reaction pressure in the chamber are also extreme tests of the epitaxial equipment. Researchers in IBM have studied the impact of different Si sources of SiH<sub>4</sub> and DCS on the morphology of selective growth SiGe films [9], which is helpful for the device size design. However, they didn't give a solution

**Fig. 5.3** Growth rate at different growth pressure [8]



for macro loading effect. At present, most of the methods for improving the pattern dependency are modulating the reaction conditions, such as the pressure of HCl, the total reaction pressure, the volume of carrier gas and the choice of reaction source. But these methods are not the optimal solution for all of devices. Suitable method should be used according to the actual manufacture.

## 5.2 Evaluation and Calculation Model of Pattern Dependency

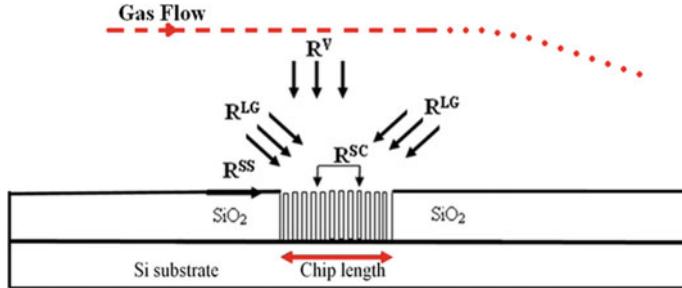
For evaluating the pattern dependency after SiGe selective growth, the layer thickness, Ge content and distribution should be measured. The layer thickness can be measured by HRTEM. Ge content and distribution can be obtained by EDS and XRD. To evaluate the micro and macro loading effect over the whole wafer, precise tests and analysis should be done at different parts of the chip (or wafer), which is time-consuming and costly. If there is a kinetic model [2] to estimate the pattern dependency of SiGe layer profile for the cases when the wafer has uniform or non-uniform pattern (global and local variations), it will be significant to the mass production.

### 5.2.1 Model Calculation of 22 nm Planar Device

During the progress of SiGe selective epitaxy, the growth rate on Si exposed area depends on many factors. In general, having a controlled rate of deposition and etch is the key role during epitaxy. When the rate of deposition is greater than that of etch, epitaxy can be realized. In this process, various reactive gas molecules divide into different particles or groups (such as Si, Ge, Cl, etc.) and reach to the exposed Si area from horizontal or vertical directions. This process determines the growth rate of this part. As shown in Fig. 5.4,  $R^V$  and  $R^{LG}$  respectively refer to the reactive gas molecules in the vertical and horizontal directions, while  $R^{SC}$  and  $R^{SS}$  respectively represent reaction molecules inside and outside the chip which reach the surface of the oxide layer.  $R^{SC}$  and  $R^{SS}$  will change with the coverage range of the exposed Si area. For example,  $R^{SC}$  and  $R^{SS}$  are different for chips located at the center and edge of a silicon chip.  $R_{HCl}$  is also one of the influence factors, which mainly reflects the etching rate of Si. The direction of the arrow in the figure indicates that the reaction gas molecules can be adsorbed when they diffuse to the surface of exposed Si area [10].

The growth rate of SiGe in selective epitaxy follows Eq. (5.1):

$$R_{Total} = R_{Si}^V + R_{Si}^{LG} + R_{Si}^{SS} + R_{Si}^{SC} + R_{Ge}^V + R_{Ge}^{LG} + R_{Ge}^{SS} + R_{Ge}^{SC} - R_{HCl}^V - R_{HCl}^{LG} - R_{HCl}^{SS} - R_{HCl}^{SC} \quad (5.1)$$

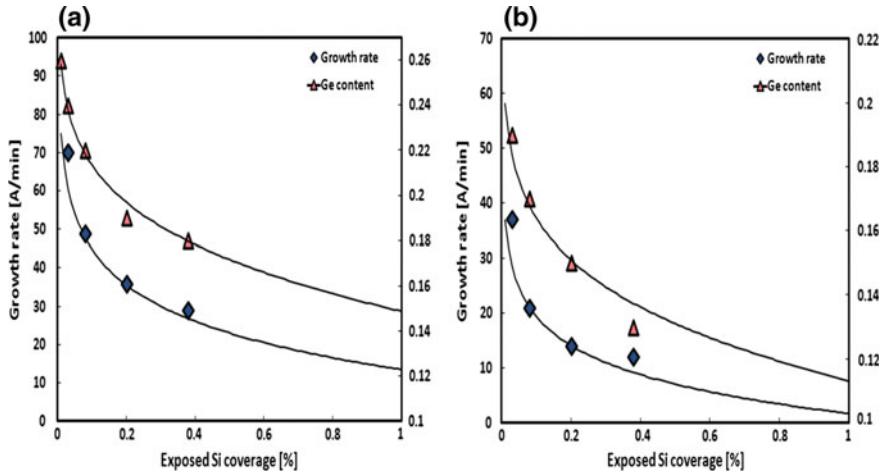


**Fig. 5.4** Schematic diagram of reaction gas molecules in different exposed Si area during SiGe selective epitaxy using RPCVD [10]

Equation (5.1) for the total growth rate is expressed in more detail as following:

$$\begin{aligned}
 R_{\text{Total}} = & \beta \frac{(1 - \theta_{\text{H(Si)}} - \theta_{\text{Cl(Si)}})}{N_0} \frac{P_{\text{SiH}_2\text{Cl}_2}}{(2\pi m_{\text{SiH}_2\text{Cl}_2} k_b T)^{\frac{1}{2}}} \left( \frac{E_{\text{SiH}_2\text{Cl}_2 \text{on Si}}}{k_b T} + 1 \right) \\
 & \exp\left(-\frac{E_{\text{SiH}_2\text{Cl}_2 \text{on Si}}}{k_b T}\right) + \chi \frac{(1 + m_r)(1 - \theta_{\text{H(Si)}} - \theta_{\text{Cl(Si)}})}{N_0} \frac{P_{\text{GeH}_4}}{(2\pi m_{\text{GeH}_4} k_b T)^{\frac{1}{2}}} \\
 & \left( \frac{E_{\text{GeH}_4 \text{on Si}}}{k_b T} + 1 \right) \exp\left(-\frac{E_{\text{GeH}_4 \text{on Si}}}{k_b T}\right) + \chi \frac{(1 + m_r)(1 - \theta_{\text{H(Si)}} - \theta_{\text{Cl(Si)}})}{N_0} \\
 & \frac{B P_{\text{GeH}_4 \text{on Si}} \ln(1/c)}{(2\pi m_{\text{GeH}_4} k_b T)^{\frac{1}{2}}} \left( \frac{E_{\text{GeH}_4 \text{on Si}} + 0.1 \text{ eV}}{k_b T} + 1 \right) \exp\left(-\frac{E_{\text{GeH}_4 \text{on Si}} + 0.1 \text{ eV}}{k_b T}\right) \\
 & - \frac{\gamma}{N_0} \frac{P_{\text{HCl}}^{0.596}}{(2\pi m_{\text{HCl}} k_b T)^{\frac{1}{2}}} \left( \frac{E_{\text{Etching}}}{k_b T} + 1 \right) \exp\left(-\frac{E_{\text{Etching}}}{k_b T}\right) \quad (5.2)
 \end{aligned}$$

where the equation constants:  $\beta$ ,  $\chi$  and  $\gamma$  are tooling factors which depend on the temperature distribution and gas kinetics over the susceptor in the CVD reactor.  $\theta$  parameters are for the occupied dangling bonds (in presence of H and Cl) on Si with a specific surface orientation where  $N_0$  is the number of atoms unit volume for Si. P and E respectively represent the partial pressure and activation energy of reaction molecules in the chamber. In selective epitaxy, there are more Ge atoms on the surface of oxide layer due to the easier reaction between HCl and Si. Thus, Ge term is the mainly influence factor for the pattern dependency. The variable "c" is the exposed Si coverage on the chip. The diffusion of Ge atoms on the surface of oxide layer adds additional 0.1 eV to the Ge activation energy and increases the numbers of free dangling bonds. The negative sign represents HCl will etch some of deposited atoms. To have a controlled rate of deposition and etch during the epitaxy is the key role during epitaxy. Therefore, the available dangling bonds at a growth temperature (T), the partial pressure of reactant gas molecules (P) and activation energy for breaking bonds in presence of reactant species (E) are important parameters to be determined in this equation.  $m_r$  is a research related factor, which is usually selected as 2.



**Fig. 5.5** The measured and calculated growth rate and Ge content at different  $\text{GeH}_4$  partial pressure: **a** 0.9 mTorr, **b** 0.5 mTorr [10]

In an ideal condition, the arrays of Si openings are repeated at different parts of the chip (or wafer). Figure 5.5 shows the measured and calculated growth rate and Ge contents with different exposed Si coverage. These values can be used to calculate the various factors in Eq. 5.2.

In practice, the exposed Si areas (or hanging keys) are not uniform because of the arrays of openings with different sizes and densities. The complexity of the chip leads to the non-uniformity of the distribution of reactive molecules and atoms on the chip, which causes the interaction between different regions of the chip. The interaction between the chips occurs when an array with large coverage of exposed Si area acts as a stronger attraction force compared to the surrounding regions for incoming reactant molecules. Thus, an interaction is established between the forces exerted on the molecules from the regions of a chip. Therefore, the growth rate over a region under such interactions is expressed as following (5.3) [2]:

$$R_T(d) = R_A + (R_{surr} - R_A) \left( 1 - e^{\frac{-d}{\tau(c_{surr})}} \right) \quad (5.3)$$

where  $d$  is the distance from the region of chip with large coverage of exposed Si area and  $c_{surr}$  is the exposed Si coverage of the surrounding regions. In this equation,  $R_A$  is the growth rate of an array with highest exposed Si coverage in a particular part of the chip. This part has dominant role in consumption of incoming atoms where  $R_{surr}$  is the growth rate of arrays situated in the neighbourhood of this array. In the above equation, the exponential function determines the interaction between the regions of the chip. The variable  $\tau$  is called interaction range and represents the length through which an array of transistors interacts with its surrounding arrays (5.4):

$$\tau = \frac{1}{\varepsilon c + \eta \sqrt{c} + \delta} \quad (5.4)$$

where,  $\varepsilon$  and  $\eta$  are the kinetic energy constants, which are related to the distance that the element moves from the beginning to being attracted by the hanging keys.  $\delta$  is another kinetic energy constant, it takes into account the interactions between gas molecules before they reach to the hanging keys.  $T$  decreases as the Si exposed area increases, as the distance of the gas molecules moving over the top of the chip decreases. The empirical values of each kinetic energy constant are as follows (5.5):

$$\varepsilon = 0.0004 \text{ } \mu\text{m}^{-1}, \quad \eta = 0.0011 \text{ } \mu\text{m}^{-1}, \quad \delta = 0.00048 \text{ } \mu\text{m}^{-1} \quad (5.5)$$

The Ge content in the SiGe layers is obtained from a ratio of Si and Ge partial pressures according to (5.6) [11]:

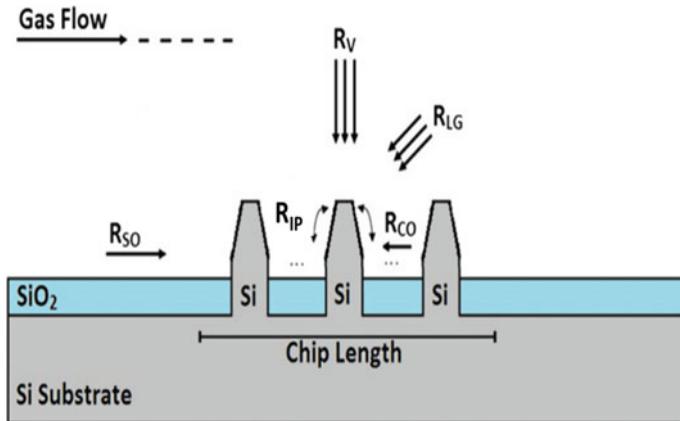
$$\frac{x^2}{1-x} = 1.88 \times 10^{-4} \exp\left(\frac{E}{kT}\right) \left( \frac{P_{\text{GeH}_4} + \left(5 \times 10^{-4} P_{\text{GeH}_4} \ln\left(\frac{1}{c}\right)\right) - (1-\lambda) P_{\text{HCl}}}{P_{\text{SiH}_2\text{Cl}_2} - \lambda P_{\text{HCl}}} \right) \quad (5.6)$$

where  $x$  and  $\lambda$  are the Ge content and reaction ratio, respectively.  $\lambda$  is related to the fraction of Cl atoms which interact with Si and Ge atoms. The  $\lambda$ -value is 1 when  $P_{\text{HCl}} < P_{\text{SiH}_2\text{Cl}_2}$  and is 0.8 for higher HCl amounts. E is the activation energy for the reaction which is extracted to 0.697 eV for SiGe, which is very close to the total activation energy of 0.58 eV. The total activation energy refers to the sum of adsorption energy difference ( $E_{a,\text{SiCl}_2} - E_{a,\text{GeH}_2} = 0.1 \text{ eV}$ ) [12] and adsorption energy difference ( $E_{d,\text{Cl}} - E_{d,\text{H}} = 0.48 \text{ eV}$ ) [13].

In conclusion, the growth rate of SiGe in 22 nm planar devices and the distribution of Ge contents on different exposed Si areas in the wafer can be determined by the above equations.

### 5.2.2 Model Calculation of 16 nm FinFET

A theoretical model to describe the selective epitaxy of SiGe for 22 nm planar devices has been discussed in last section. This model has been modified for the SiGe growth for 3D FinFETs. The modifications have considered the SiGe growth on a Si-fin surface containing a central part, (001) plane and (111) planes at the sides (for a fin with a trapezoid shape). A correction term  $R^{IP}$  is introduced in the equation, which represents the diffusion of atoms from the edges towards (001) plane in the centre of fins. The growth rate of SiGe on a Si-fin is a result of a series of contributions both in vertical and lateral directions as illustrated in Fig. 5.6.



**Fig. 5.6** Schematic illustration of a laminar gas stream flowing over the wafer and the molecules in gas form or absorbed species on the oxide surface diffusing towards the exposed Si-fins [14]

The impinging molecules (Si and Ge) perform deposition, while, at the same time, the Cl atoms etch away the absorbed atoms on the exposed Si areas and on the oxide surface. The main equation for the SiGe growth on a Si-fin structure can be written as following (5.7) [14]:

$$R_{Total} = R_{Si}^V + R_{Si}^{LG} + R_{Si}^{SO} + R_{Si}^{CO} + R_{Si}^{IP} + R_{Ge}^V + R_{Ge}^{LG} + R_{Ge}^{SO} + R_{Ge}^{CO} + R_{Ge}^{IP} - R_{HCl}^V - R_{HCl}^{LG} - R_{HCl}^{SO} - R_{HCl}^{CO} + R_{HCl}^{IP} \quad (5.7)$$

where  $R^V$  and  $R^{LG}$  are the contribution of gas molecules in vertical and lateral direction, while  $R^{CO}$  and  $R^{SO}$  are for the reactant molecules (indexed with Si, Ge and HCl) moving on the oxide surface within or surrounding a chip, respectively.  $R^{SO}$  varies over regions where more oxide is available e.g. between two neighbouring chips. As mentioned above,  $R^{IP}$  represents the diffusion of atoms from the edges towards (001) plane in the centre of fins. The diffusion of atoms over a Si-fin with facet planes is an important parameter which controls the kinetics of molecules. In this work, the diffusion theory for atoms over (001) and (111) surfaces has been applied [15, 16]. According to this theory, the atoms on inclined planes have a longer diffusion length compared to (001) plane. Therefore, a flow of atoms from inclined planes at the sides is established towards the (001) plane in central part of Si-fins.

When the growth temperatures for SiGe layers were in range of 600–650 °C, a diffusion length of ~200 and 300 nm is estimated for Si and Ge atoms, respectively. This means that both Si and Ge atoms will have the opportunity to migrate over the entire 16 nm Si-fins making a uniform SiGe profile. Thus, the contribution of  $R^{IP}$  for Si-fins with such small size is negligible. In fact, this conclusion was expected since the experimental results indicate that the Ge profile is constant over the Si-fins (as described in Fig. 4.42). In other words, if the size of Fin is similar to the diffusion length of Si and Ge, the contribution of RIP must be taken into account. In this case,

the profile of SiGe is no longer the “Diamond” symmetric type shown previously. Therefore, in the calculation of SiGe epitaxial growth rate on small-size Fin, Eq. (5.2) can be used to express the SiGe epitaxial rate on small-size Fin. A Si-fin has a shape where (001) plane is located at the central part and (111) planes at the sides. The  $\theta$  parameter has to be calculated for each orientation plane. The Ge content in the SiGe layers is obtained from a ratio of Si and Ge partial pressures according to Eq. (5.6).

### 5.3 Impact of Pattern Dependency on the SiGe Selective Epitaxy

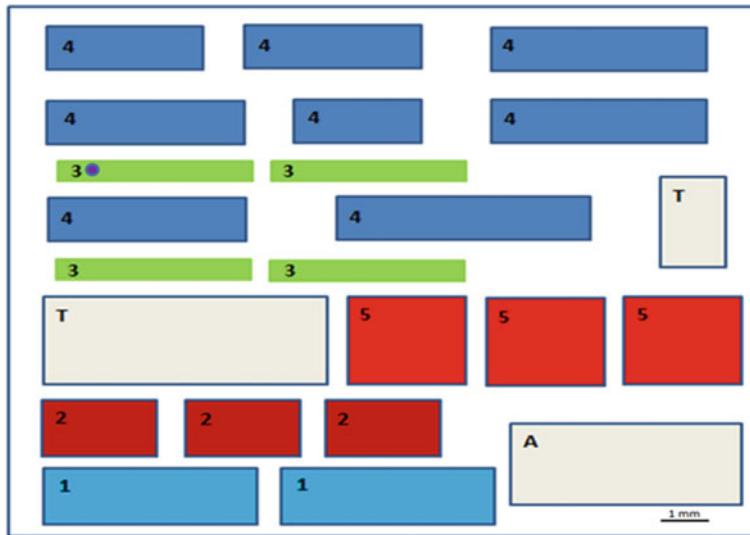
In this part, the calculated and measured results are compared and analysed to study the impact of pattern dependency of SiGe layers grown selectively in source/drain 22 nm planar and 16 nm FinFET devices on the SiGe profiles (growth rate and Ge content).

#### 5.3.1 *Experimental Details*

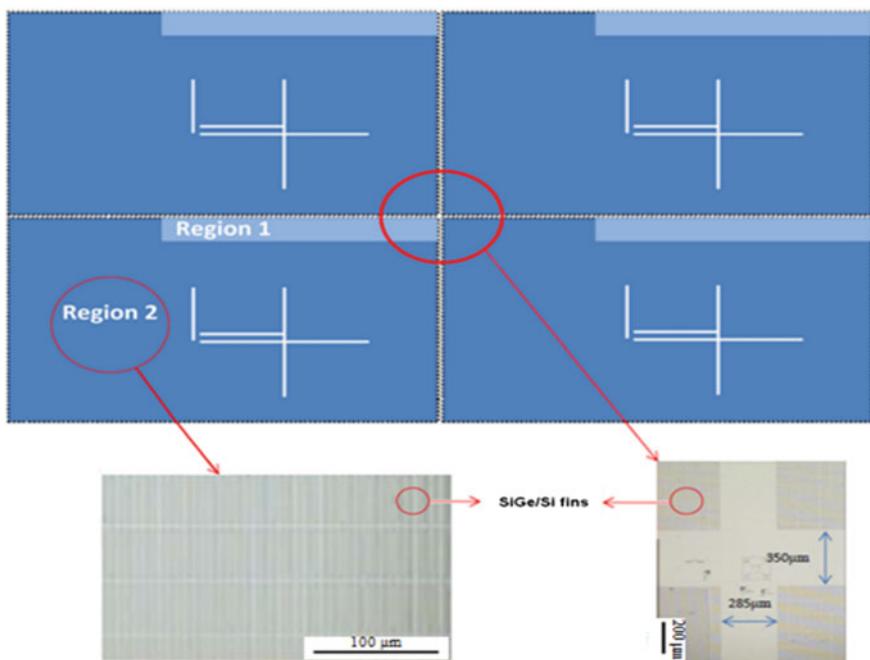
In 22 nm planar device layout, a specific chip was selected for the evaluation and analysis of the pattern dependency of SiGe layers grown selectively in source/drain. The calculated results of the model were validated by the measured parameters of TEM and HRXRD. Figure 5.7 shows the pattern of a typical die where the exposed Si area is different. The different exposed Si areas were designed for calculating growth rate and Ge content over different areas. The chip was divided into 5 sub-regions, in which the device density and exposed Si area were the same. There were also some sub-regions which contain calibration and test structures. However, due to the existence of the large sub-region 5, these sub-regions have little impacts [10].

In an ideal case, the Si-fin arrays are repeated over the whole chip (or over a wafer) but there are areas where this uniformity is disturbed. As examples, there are local and global alignment marks on each wafer or between the chips exists more oxide area. Thus, a specific area was chosen to study the pattern dependency of SiGe epitaxial layers. Figure 5.8 shows a schematic view of a mask layout which was used for SiGe growth calibration. A certain colour in the figure presents a specific exposed Si area where the density and size of Si-fins were constant. This chip was divided into two regions (light and dark blue which are region 1 and 2, respectively) in this figure. There are also other areas which contain alignment marks and test structures. It is important to mention here that fins in region 1 have more oxide around them compared to region 2. The exposed Si area of region 1 is same as that of region 1 in Fig. 5.7 [14].

In calculation, the partial pressures are  $P_{DCS} = 15.99$  Pa,  $P_{Ge} = 0.533$  Pa and  $P_{HCl} = 8.66$  Pa, respectively. Moreover, the atom density on (111) facet is



**Fig. 5.7** Scheme of a calibration mask pattern for selective epitaxy of SiGe layers in 22 nm planar device [10]



**Fig. 5.8** Scheme of a calibration mask pattern for selective epitaxy of SiGe layers in 16 nm FinFET device [14]

$7.8 \times 10^{14} \text{ cm}^{-2}$  compared to  $6.8 \times 10^{14} \text{ cm}^{-2}$  for (100) planes. The active energy  $E_a$  on each plane is about 2.08 eV.

The Ge content and thickness of SiGe layers was obtained by using EDS technique in HRSEM and cross-sectional images, respectively. The EDS technique was used to confirm the XRD results.

### 5.3.2 Results and Discussions

According to the calculation model of pattern dependency and the selected exposed Si area, the calculated and measured SiGe profiles in different sub-region of 22 nm planar device is obtained, shown as in Table 5.1.

Table 5.1 shows the calculated and measured SiGe profiles in different subdivisions in Fig. 5.7. Due to the more consumption of reaction gases of large exposed Si area (regional consumption ranked as follows: 5, 3, 2, 1, 4), the growth rate of SiGe thin films and germanium content are lower than other areas. In this condition, these regions need to be compared using Eq. 5.3. This also can be discussed from the perspective of the interaction of each region. The interaction scope of region 5 is 525  $\mu\text{m}$ , while that of region 3 and 2 is 982 and 1554  $\mu\text{m}$ , respectively. It indicates that region 5 has the least direct interaction with other chips, and the surrounding regions (including regions such as alignment markers) are most susceptible to this region. The Ge content and thickness of SiGe layer are measured by high resolution scanning electron microscopy (HRSEM) and elemental analysis of EDX, respectively.

The calculated Ge contents are in good consistency with the measured values. In Table 5.1, there is some discrepancy in Ge content for sub-regions 2, 3, 5. This can be due to the low accuracy of EDX technique for low density of transistor arrays (region 2) and thin layers (region 3 and 5). However, the discrepancy can be partially solved by adjusting the energy of HRSEM, as appropriate energy can make the penetration depth of electrons reach the thickness of the SiGe layer in this region. In this study, the energy values used in different regions are 10–30 keV. In order to obtain higher accuracy, we conducted repeated EDX tests. Then, the average value of Ge contents was used for calculation. Due to the area of regions 2 and 3 is smaller, fewer EDX

**Table 5.1** The calculated and measured SiGe profiles in different sub-regions in Fig. 5.7 [10]

Sub-region	Exposed Si (%)	Calculated Ge content	Measured Ge content (EDX)	Calculated growth rate	Measured growth rate (nm/s)
1	0.34	35.3	35.23	0.67	0.68
2	2.12	34.0	29.14	0.51	0.57
3	18.44	29.0	31.88	0.43	0.38
4	0.06	35.3	35.81	0.78	0.77
5	92.17	26.0	30.00	0.26	0.26

**Table 5.2** The calculated and measured SiGe profiles in different sub-regions in 16 nm FinFET device [14]

Region	Exposed Si (%)	Calculated Ge content (%)	Measured Ge content (EDX and XRD) (%)	Calculated growth rate (nm/s) (100) and (111)	Measured growth rate (100) and (111) (nm/s)
1	0.34	35.29	35.23	0.92 and 0.54	0.85 and 0.51
2	2.12	33.75	35	0.73 and 0.43	0.71 and 0.42

tests were performed. Thus, the error of Ge content is larger than other regions. The results in Table 5.1 illustrates that the SiGe profile is dependent on the exposed Si area and the growth parameters, then the above model can be applied for transistors for 22 nm planar or any technological node. In order to further verify the correctness of the calculation model, the SiGe profiles in two regions of FinFET device were also calculated and measured, shown as in Table 5.2.

For further verifying the accuracy of the calculation of SiGe growth rate, the selective area of the two regions in the FinFET device is the same as that of the regions (1) and (2) in the 22 nm planar device. EDX and XRD techniques are both used to measure the Ge content for improving the accuracy of the test.

The exposed Si coverage of the (111) facets is not the same as (001) planes. Considering the trapezoid shape of the fins, one can estimate 7 times more exposed Si coverage for (111) facets compared to (001) planes on the top side of the trapezoid. Moreover, the atom density on (111) facet is  $7.8 \times 10^{14} \text{ cm}^{-2}$  compared to  $6.8 \times 10^{14} \text{ cm}^{-2}$  for (100) planes. Considering these two factors, Table 5.1 shows the calculated and measured values for the fins located in regions 1 and 2, which was consistent with the measured results. For the same reason, the consumption of reaction gas of region 2 with larger area is more than that of region 1. And the number of dangling bonds in region 2 is also more than that in region 1, especially that (111) facets has a dominant role for the consumption of molecules during epitaxy. In this condition, the growth rate of region 2 is determined by the RA in Eq. (5.3), where  $R_{\text{sur}}^*$  is the growth rate of arrays situated in the neighbourhood of this array. The interaction range is 1541 and 1833  $\mu\text{m}$  for regions 2 and 1, respectively.

In conclusion, the growth rate of SiGe and Ge content are not only depending on the growth parameters, but also influenced by the pattern dependency of selective epitaxy of SiGe layer. With larger exposed Si area, the growth rate of SiGe is slower and the Ge content is lower. The measured Ge content of 27% for completely exposed Si wafer also verifies the existence of the pattern dependency. In order to avoid pattern dependency over the chip, the exposed Si areas have to be uniformly distributed so that the gas consumption is homogeneous over the chip. This can be taken as a main consideration in the mask design.

## 5.4 Impact of Pattern Dependency on the Electrical Performance of Integrated Devices

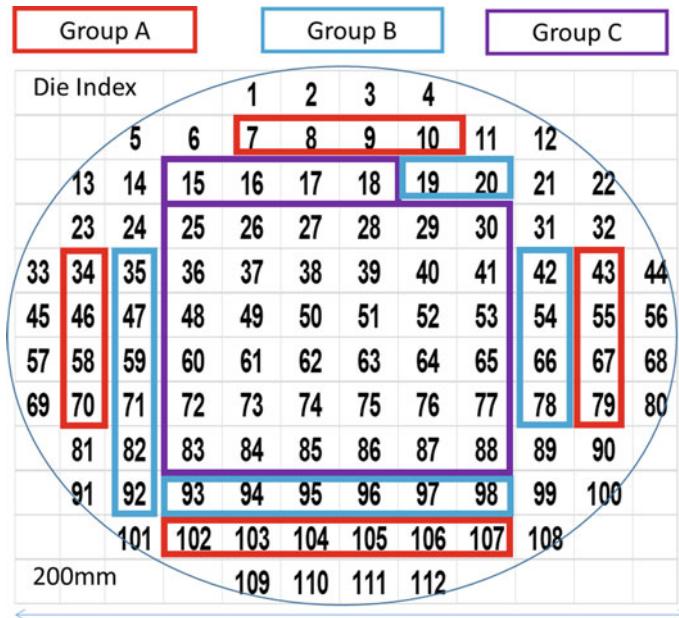
The uniformity of the SiGe source/drain device process and performance over the entire wafer is a crucial point for the chip manufacturer. And the epitaxial quality of SiGe layer and Ge content will influence the transistor performance. In transistor design, carrier mobility is one of the most important parameters, which was determined by the strain in the channel. The selective deposition of SiGe material in the source/drain is the most sensitive or may be vulnerable step in the transistor processing since it creates strain in the channel region. Thus, a high Ge content is needed to provide strain. The growth of SiGe is pattern dependent and is varied over the wafer (global effect), or inside a die due to the variation of layout (local effect). If all the dies over the wafer has same pattern the global effect will be ignored but still the presence of oxide at the preference of the wafer still may cause pattern variation and the dies in vicinity of the wafer edge will suffer from pattern dependency. The main reason for the pattern dependency is the different exposed Si coverage of dies in different location. In order to analysis the pattern dependency, we try to estimate the global effect and bring a new interpretation for the electrical performance of SiGe integrated devices, which help to improve the device quality.

### 5.4.1 Experimental Details

In order to study the electrical characteristics of different regions over the same wafer, 112 processed dies of 22 nm node PMOS SiGe source/drain devices in a processed 8 in. wafer were measured. As shown in Fig. 5.9, three groups of dies (A, B and C) are distinguishable in terms of how good the transistor characteristics are over the wafer (poor, good and best for A, B and C group, respectively) [17]. By comparing the measured electrical data, calculating and measuring the growth rate of SiGe and Ge content within the group, it's able to estimate the impact of pattern dependency on the performance of integrated devices.

More detailed view of a single die is shown in Fig. 5.7. The blue-marked cross indicates approximately the position of a transistor position in an array of transistor where the electrical measurements were performed on this die and repeated identically over all 112 dies of the wafer. The reason for choosing this position in a die is the possibility to combine material characterization from the test arrays in the neighborhood. The electrical measurements were  $I$ - $V$  curves where the transistor characteristics e.g.  $V_{sat}$ ,  $I_{on}$ ,  $I_{off}$ , drain-induced barrier lowering (DIBL) and carrier mobility were extracted. The electron mobility ( $\mu_e$ ) for a transistor can be calculated from the expression of Eq. 2.1 (W and L are width and length of the transistor,  $L = 25$  nm,  $W = 3 \mu\text{m}$ ).

A theoretical model has been already reported to describe the selective epitaxy of SiGe for 22 nm planar and 16 nm FinFET devices. These reports deal with 2D and



**Fig. 5.9** Schematic of the processed dies on Si bulk wafer where three groups were distinguished according to the transistor performance [17]

3D growth of SiGe layer in a broad way where the kinetic of gases was expressed in different incoming flux of molecules. In the present work, the same model has been applied to calculate the SiGe profile (Ge content and layer thickness) in different dies over the entire 8 in. wafer. By using, interaction model the SiGe profile could be calculated over transistor arrays where the effect of susceptor (SiC sample holder) and the variation of oxide at edge of the wafer (or between dies) as well as mutual interactions between the chips are calculated.

#### 5.4.2 Results and Discussions

A summary of electrical data for some the dies in group A, B and C are presented in Table 5.3 [17]. It is emphasized here that there is a statistical variation in the measured data and the boundary between the three die groups is vague. In general, carrier mobility data in this batch process is lower than the state of arts transistors published before. The main reason is that the processes are optimized in terms of annealing temperatures, dopant incorporation and strain. However, this will not disturb the purpose of this study which is to highlight the pattern dependency behavior of the selective epitaxy.

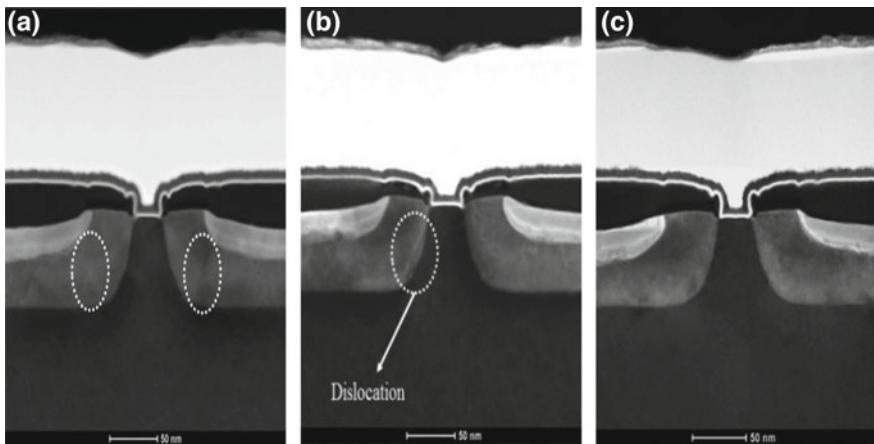
**Table 5.3** A summary of electrical performance for some the dies in group A, B and C in a 22 nm SiGe PMOS device [17]

Transistor group	Chip	Measured Ge content	$V_{T\text{sat}}$ (V) $V_{DD} = 1$ V	$I_{on}$ ( $\mu\text{A}/\mu\text{m}$ )	$I_{off}$ ( $\text{nA}/\mu\text{m}$ )	DIBL (mV)	Mobility ( $\text{cm}^2/\text{Vs}$ )
A	8		-0.46	263	0.34	75.4	24
	9	0.38	-0.54	111	0.24	91.3	13
	10		-0.56	86	0.47	112	9
B	71		-0.39	407	0.82	101	36
	82	0.40	-0.39	420	0.86	90	37
	92		-0.39	405	0.65	96	35
C	27		-0.32	598	4.8	115	65
	38	0.35	-0.30	618	9.8	123	71
	50		-0.28	619	10.2	119	75

Transistors from group C have highest  $I_{on}$ ,  $I_{off}$  and carrier mobility, and lowest saturation velocity compared to the other groups. The reason is that the defect density and Ge content of SiGe layer in the three groups are different, which needs further analysis. The measured germanium content in source/drain regions of transistors in A, B and C groups is 38%, 40% and 35%, respectively (the sacrificial SiGe layer is already consumed in Ni silicification). These values have been determined by EDS techniques which indicates the atomic composition in SiGe. The generated strain which is related to the lattice distortion in SiGe layers cannot be determined from these EDS values. High-resolution X-ray diffraction has also been applied to measure the strain in the transistors' structures. Unfortunately, the beam can be tailored for submicron size which is necessary to distinguish the transistor arrays. Therefore, a mean value of 35–40% was obtained for Ge content over a large area of the transistor arrays for A, B and C groups.

For further investigation, TEM technology was used to measure the density of misfit dislocation. Figure 5.10 shows the cross-section of three transistors from die 9, 82 and 38 from group A, B and C, respectively. The density of misfit dislocation is  $1 \times 10^8 \text{ cm}^2$  in Fig. 5.10c, which is lower than that in Fig. 5.10a, b ( $3 \times 10^9 \text{ cm}^2$  and  $1 \times 10^9 \text{ cm}^2$ , respectively). These dislocations were formed at the interface between SiGe/Si and have propagated towards the channel region. It is well-known that the presence of misfit dislocations leads to strain relaxation in the epi-layer. During measurement, the growth rate of SiGe is 0.58, 0.62 and 0.51 nm/s, respectively, in transistor 9, 82 and 38, which illustrates that the density of misfit dislocations also influences the growth rate [17].

We may conclude from these results that there is a large strain relaxation for transistor in die 82 from group B. The high Ge content and growth rate in group A and B is a result of the pattern dependency of selective growth combined with misfit dislocations.



**Fig. 5.10** Cross-section images of **a** Group A, die 9, **b** Group B, die 82 and **c** Group C, die 38 measured by TEM [17]

On the other hand, Ge content in group B is slightly higher than that in group A. Meanwhile, the Boron doping in group B is also higher than that in group A. Due to the strain compensation, SiGe profile in group B is better which leads to fewer dislocations. These results are consistent with the measured density of misfit dislocations. The Ge content in group C is the lowest and the SiGe profile is the best. The performance difference among three groups is a result of the pattern dependency, i.e. the SiGe profiles (growth rate and Ge content) are dependent on the coverage of the surrounding regions, which impacts the performance of devices.

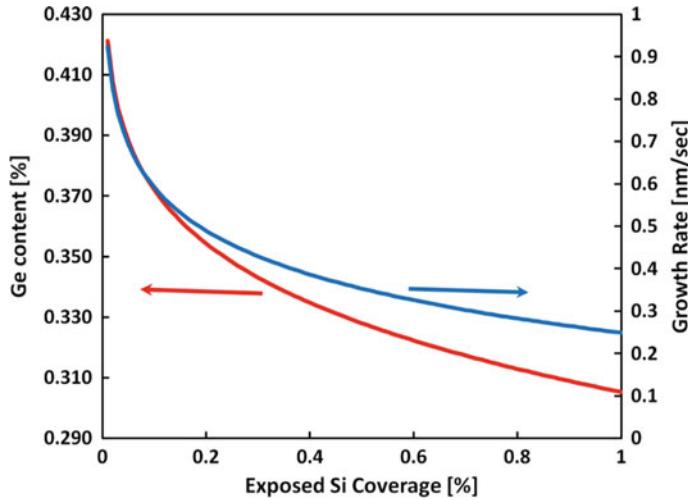
In order to further analysis the impact of pattern dependency on the performance of devices, Eqs. (5.2) and (5.6) were used to calculate the growth rate of SiGe and Ge content in different sub-divisions of group A, B and C. The calculated and measured results are shown in Table 5.4.

Equations (5.2) and (5.6) are used to calculate the growth rate and Ge content which are valid for global patterns. The calculated results are shown in Fig. 5.11 by adopting modified model and parameters.

The calculated SiGe profiles are in good consistency with the measured SiGe profile in Table 5.4. However, there is some discrepancy for group A which is caused

**Table 5.4** The calculated and measured SiGe profiles in different sub-divisions of group A, B and C [17]

Die group	Measured Ge content (EDX)	Calculated Ge content	Calculated growth rate (nm/s)	Measured growth rate (nm/s)
A	0.38	0.34	0.40	0.58
B	0.40	0.38	0.62	0.62
C	0.35	0.36	0.51	0.51



**Fig. 5.11** Calculated growth rate and Ge content with different exposed Si coverages [17]

by oxide at the edge of mask (3–4 mm). For example, die 10 form group A is heavily influenced by the susceptor on the right, upper and upper right side. Since the transistor distribution on the chip is non-uniform, which makes the interaction range hard to calculate, the equivalent exposed Si area of all chips over the entire wafer is calculated. For this mask, the value is about 7%, the resulted interaction range is 1251  $\mu\text{m}$ .

In addition, the misfit dislocations in SiGe layer for transistors in group A and B lead to the discrepancy, shown as in Fig. 5.10a, b. When establishing the kinetic energy model of SiGe growth, the Si exposed area on the chip was taken into account. The available dangling bonds on the surface would be attractive to the reaction molecules. As dislocations create more available dangling bonds on the surface, the collision probability and surface molecular absorption would increase. In order to avoid pattern dependency over the chip, the exposed Si areas have to be uniformly distributed so that the gas consumption is homogeneous over the chip. This can be taken as a main consideration in the mask design. Compensate design also can be considered for chip design at the edge of the wafer due to the pattern dependency.

## 5.5 Conclusion

In this chapter, we study the impact of pattern dependency in the integration process of SiGe source/drain devices. First, we introduce the production and mechanism of pattern dependency of SiGe layers selective growth. Different remedies have been proposed to make more uniform SiGe profiles in selective epitaxy. However, these methods are mainly adopted to regulate the reaction conditions, such as changing the

HCl partial pressure and total growth pressure, selecting reaction sources. None of these methods could effectively remove the pattern dependency of the growth. Thus, an appropriate approach should be selected based on chip manufacturers.

Then, A theoretical model and calculated method are established to estimate the pattern dependency (Micro and Macro Loading Effect) of SiGe layer selective epitaxy for 22 nm planar and 16 nm FinFET devices. In the estimation, repeat sample tests should be performed in different regions, which is time-consuming and costly. The pattern dependency can be modeled and calculated based on the mechanism of SiGe selective epitaxy growth using PRCVD, combined with the temperature and distribution of reactive molecules and atoms in the chamber, which is of practical value for SiGe device integration.

After that, the growth rate of SiGe and Ge content in sub-regions (the same chip) with different exposed Si area are calculated to estimate the micro loading effect for 22 nm planar and 16 nm FinFET devices. The results show that the calculated values are consistent with the test results, which provides an effective and rapid method to predict and estimate the pattern dependency for SiGe device integration.

Finally, we study the impact of macro pattern dependency on the electrical performance of 22 nm planar PMOS SiGe source/drain devices. By comparing the electrical characteristics of group A, B, and C, which located at the edge, middle and center of the wafer, we found that the quality of SiGe film in group C is the best, the Ge content is moderate, and the performance of the device is relatively good. However, the chip at the edge of the wafer is heavily affected by the graphite susceptor and oxide layer, which leads to a fast growth rate and large density of misfit dislocations. Accordingly, the device performance is the worst compared to the other groups.

In conclusion, in order to avoid pattern dependency in practical manufacture, the exposed Si areas have to be uniformly distributed so that the gas consumption is homogeneous over the chip, which could suppress the damage effectively caused by pattern dependency.

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# Chapter 6

## Conclusions and Prospects



### 6.1 Summary

In this thesis, we mainly studied SiGe selective epitaxy for source/drain engineering in 22 nm Node and beyond CMOS. The key processes in selective epitaxial of strained SiGe by RPCVD and device integration have been studied systematically, which lays a good foundation for the application of SiGe technology in advanced devices. The main research results can be summarized as follows:

- (1) In this thesis, key process parameters which affect the film quality and strain in SiGe selective epitaxy are studied. The growth parameters were optimized for growth highly strained SiGe film. The optimum growth parameters are as follows: reaction temperature:  $T = 650\text{ }^{\circ}\text{C}$ , total pressure:  $P = 20\text{ Torr}$ , HCl gas flow: 65 sccm, B doping:  $1\text{E}20\text{--}3\text{E}20\text{ cm}^{-3}$ , Ge content: 27–35%. Various growth parameters determine the SiGe growth rate and Ge content. The optimization of the growth parameters can improve the epitaxial quality, while enhancing the threshold of the critical thickness for films and keeping the maximum strain.
- (2) The key process steps in integration of SiGe in source/drain were analyzed and optimized in this paper. It was found that the addition of DHF in the cleaning procedure prior to epitaxy could help enhance the removal of organic contamination on the surface and improve the quality stability of epitaxial layers effectively. In addition, the optimization for the rinsing method and time of native oxide layers was performed. The using of DBOE was beneficial to the removal of Si surface oxide layer while improving the etch selection ratio of SiN side wall.
- (3) In this thesis, the impact of pre-baking on the shape of source/drain was studied in SiGe selective epitaxy. At high pre-baking temperature, the etching of Si by residual Cl in  $\text{H}_2$  atmosphere caused the altered shape of source/drain region and the loss of Si. The shape irregularity in low pressure pre-baking was ascribed to the thermal mismatch between Si and  $\text{SiO}_2$ , which leaded to Si atom migration.

The Fin would become larger and smoother. In addition, the impact of the amount of HCl on selective epitaxy was also analyzed. Appropriated amount of HCl should be selected to guarantee the quality of SiGe films and inhibit the production of “mushroom” on both sides and side walls of the replaced gate.

- (4) HRXRD technique and TCAD simulation were used firstly to analyze the strain of SiGe films in the integration for 22 nm planar and 16 nm FinFET devices. In particular, the microbeam enhanced HRXRD technique could be used to analyze the Ge content and strain of SiGe grown on Si-fins, verifying the high epitaxial quality. Besides, TEM and EDX techniques were employed to detect the defects, Ge profile and element distribution in the SiGe film. The rationality and necessity of the growth structure of SeGe source/drain integration were verified in the order of strain buffer layer (SRB), strain core layer ( $\text{Si}_{0.75}\text{Ge}_{0.25}$  or  $\text{Si}_{0.80}\text{Ge}_{0.20}$ ) and strain sacrifice layer ( $\text{Si}_{0.75}\text{Ge}_{0.25}$  or  $\text{Si}_{0.80}\text{Ge}_{0.20}$ ). In addition, by analyzing the electrical performance, it was found that the performance of 22 nm planar and 16 nm FinFET devices which integrated with SiGe source/drain was improved. The main reason was the increasing of source/drain area and reducing of the contact resistance in 16 nm FinFET devices with integrated SiGe S/D.
- (5) We firstly established a theoretical model to estimate the pattern dependency (micro and macro loading effect) of SiGe layers grown selectively in source/drain on 22 nm planar and 16 nm FinFET devices. The calculated results present that there is obvious micro loading effect, i.e. with smaller Si exposed area, the SiGe epitaxial growth rate is faster and the Ge content is higher. The macro loading effect provides an explanation for the performance difference of devices at different positions. The measured results were consistent with the calculated ones. This model can predict the SiGe profile over different parts of a chip (or wafer) rapidly and effectively, which lays a good foundation for the application of SiGe technology in advanced devices, especially in integrated applications for mass production.

## 6.2 Prospect

The work done in this paper only researched the mechanism of some key process in the integration of SiGe source/drain for 22 nm planar and 16 nm FinFET devices and some solutions were proposed. Although the strained SiGe source/drain were successfully applied for 22 nm planar and 16 nm FinFET devices, there are still many systematic studies that should be carried on.

- (1) In this paper, we studied the formation of “ $\Sigma$ ” morphology in 22 nm planar source/drain. However, SiGe source/drain with “ $\Sigma$ ” morphology was not applied in actual integration scheme. No further research was performed in the impact of the morphology of source/drain on the channel strain and performance for 22 nm HKMG device.

- (2) Due to the limitation of lithography equipment, the Fin spacing in FinFET device was large, so as the source/drain spacing. The integration of strained SiGe source/drain on Fin with small spacing didn't studied. The SiGe integration and the impact of strained SiGe source/drain on the device performance need to be further studied combined with practical production.
- (3) The micro-beam enhanced HRXRD technique was first used to detect the strain and Ge content of epitaxial SiGe films on 16 nm Fin. This technique has a great application prospect in the industrial production of small-size FinFET device, which is conductive to monitor the quality of SiGe film rapidly.
- (4) For SiGe selective epitaxy in different product and mask designs, the pattern dependency can be estimated by the theoretical model and growth parameters. In practical production, it is of great significance to improve the yield of SiGe devices. However, the model validation needs to be verified and further modified in the practical production.
- (5) SiGe selective epitaxy can be applied not only in the integration of source/drain, but also in the 10 nm and below node devices and nanowire device structures. It is a technology trend for replacing traditional Si material with selective epitaxial SiGe material. But the control of film defects and the selection of Ge content need to be studied.

With the development of integrated circuits, the discussion about whether the development of “Moore’s law” will end has never stopped. I think it doesn’t matter if the “Moore’s law” will end or not. The fact is that the “Moore’s law” has become a symbol of the rapid development of the information society, inspiring the continuous innovation and breakthrough of integrated circuit researchers. The development of integrated circuit has been far beyond our imagination. We can’t imagine what the development of integrated circuit technology will bring to us 30 years later, as people could not imagine that the smart phones we have now are much better than the supercomputers 30 years ago. However, good things are always worth looking forward to.