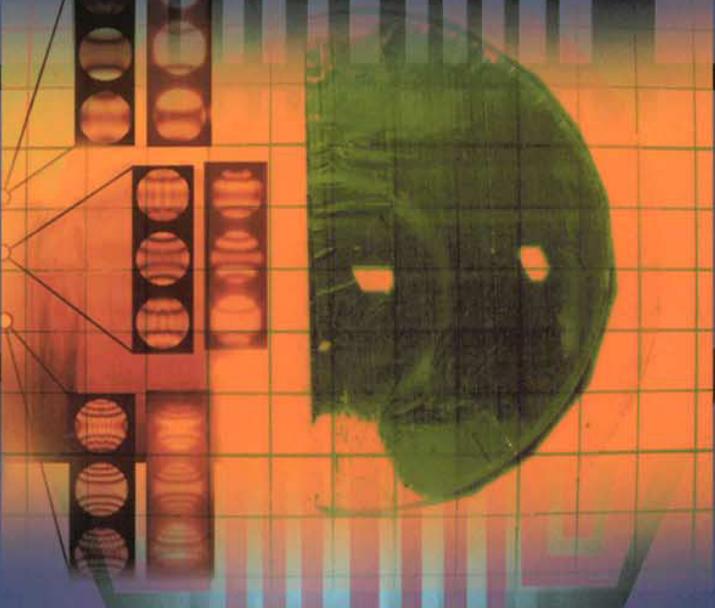


GaN-BASED MATERIALS AND DEVICES

Growth, Fabrication, Characterization
and Performance

Editors

M. S. Shur
R. F. Davis



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Growth, Fabrication, Characterization and Performance

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PREFACE

Unique materials properties of GaN-based semiconductors stimulated a great deal of interest in research and development in materials growth and optoelectronic and electronic devices using this semiconductor system. The major advantages of nitride-based materials and devices that make them extremely promising for high-power high-temperature applications are high electron mobility and saturation velocity, high sheet carrier concentration at heterojunction interfaces, high breakdown field, and low thermal impedance when grown over SiC or bulk AlN substrates. The chemical inertness of nitrides is another key property.

Khan et al were the first to report on two-dimensional electron gas at the AlGaN/GaN heterointerface and on the AlGaN/GaN Heterostructure Field Effect Transistor (HFET) in 1991 [1]. Several groups demonstrated high power operation of AlGaN/GaN HFETs at microwave frequencies [2,3,4], including a 100 W output power single chip amplifier developed by Cree, Inc. and devices with 100 GHz cut-off frequency reported in [5]. The characteristics of III-N HFETs can be further improved by implementing a new approach, which results from the demonstration of good quality of $\text{SiO}_2/\text{AlGaN}$ and $\text{Si}_3\text{N}_4/\text{AlGaN}$ interfaces.⁶ This approach opens up a way to fabricate insulated gate field-effect transistors, which have the gate leakage currents several orders of magnitude below those of regular HFETs, better linearity and higher channel saturation currents.

The papers in this volume address the entire spectrum of issues related to nitride materials and devices represented by sections on materials, transport and noise properties, and devices.

In Chapter 1.1, Rumyantsev et al list the most important nitride parameters. The goal of this chapter was to provide an update to their book⁷ dealing with the properties of nitrides published in 2001, since recent results require revisions of many important parameters for these materials (the energy gap of InN being a good example²⁴⁸.)

In Chapter 1.2, Roskowski et al discuss kinetics, microstructure and strain in GaN thin films grown via pendo epitaxy. Maskless pendo-epitaxy involves the lateral and vertical growth of cantilevered "wings" of material from the sidewalls of unmasked etched forms. They describe this technique and present high resolution X-ray diffraction and atomic force microscopy data that confirmed transmission electron microscopy results regarding the significant reduction in dislocation density in the wings. This result is important for the properties of both optoelectronic and microelectronic devices fabricated in III-Nitride structures.

In Chapter 1.3, Einfeldt et al analyze the effects of strain in GaN layers grown on 6H-SiC substrates with different buffer layers. They grew gallium nitride films of increasing thickness on either AlN or AlGaN substrates and demonstrated how the state of stress of these layers gradually changed from compression to tension with regard to both their average strain and their local strain along the [0001] growth direction.

In Chapter 1.4, Tavernier et al discuss growth of thick GaN films and seeds for bulk crystal growth. They describe the growth of low dislocation density GaN films by hydride vapor phase epitaxy and the separation of films from their growth substrates and also address issues of processing thin and thick films to create compliant layer substrates for thick film HVPE growth.

In Chapter 1.5, Etzkorn and Clarke describe cracking of GaN films and analyze the geometry, structure, and evolution of fractures. This analysis demonstrates that GaN films crack under tensile stress during growth and are subsequently overgrown and partially healed. This analysis also has important implications for Lateral Overgrowth Epitaxy (LEO) technology.

In Chapter 1.6, Lee et al discuss direct bonding of GaN and SiC as a novel technique for electronic device fabrication. The direct bonding method applied to the GaN/SiC system achieved at 900°C. Using capacitance–voltage measurements they determined the built-in potentials and the energy band offsets at the Ga/C interface.

In Chapter 1.7, Cook et al consider electronic Properties of GaN (0001) – dielectric interfaces. The characteristics of clean n- and p-type GaN (0001) surfaces and the interface between this surface and SiO_2 , Si_3N_4 , and HfO_2 have been investigated. The results show that Si_3N_4 should passivate n-type GaN surfaces but it may not be appropriate for p-type GaN surfaces. Interface dipoles contribute 1.6, 1.1 and 2.0 ± 0.2 eV to the band alignment of the GaN/ SiO_2 , GaN/ Si_3N_4 , and GaN/ HfO_2 interfaces, respectively.

In Chapter 2.1, Kim et al report on the theory of quasi-ballistic and overshoot transport in group III-nitrides. They show that in high fields electrons are characterized by the extreme distribution function with the population inversion.

In Chapter 2.2, Z. Sitar et al report on the high field transport in AlN. They directly measure the energy distribution of electrons transported through intrinsic AlN as a function of applied field and AlN film thickness. Velocity overshoot was observed in films thinner than 95 nm and at fields greater than 510 kV/cm. A transient transport length of less than 80 nm was deduced from these observations.

In Chapter 2.3, Rumyantsev et al describe generation-recombination noise in GaN-based devices. The generation-recombination noise provides valuable information about localized states and might dominate the overall low frequency noise in some frequency ranges.

In Chapter 3.1, Simin et al review novel III-N based insulating gate heterostructure field-effect transistors (IGHFETs). For the gate isolation, these devices use either SiO_2 layer (in Metal Oxide Semiconductor HFET (MOSHFET) structures) or Si_3N_4 layer (in Metal Insulator Semiconductor HFET MISHFET structures). Insulating gate HFETs have the gate leakage currents 4 – 6 orders of magnitude lower than HFETs, even at elevated temperatures up to 300 °C. Double MOSHFET with SiO_2 gate isolation (MOSDHFET) exhibit current collapse free performance with extremely low gate leakage current. Insulating gate devices, including large periphery multi gate structures, demonstrate high power stable operation and might find applications in high performance power amplifiers and microwave and high power switches with operating temperatures up to 300 °C or even higher.

In Chapter 3.2, McCarthy et al describe high voltage AlGaN/GaN heterojunction transistors and explore the use of AlGaN/GaN HEMTs and HBTs for switching power supplies. With its high electron velocities and breakdown fields, GaN has great potential for power switching. The field-plate HEMT increased breakdown voltages by 20% to 570V by reducing the peak field at the drain-side edge of the gate. The use of a gate insulator is also investigated. Their development of HBTs for switching applications included the development of an etched emitter HBT with a selectively regrown extrinsic base with current gains as high as 15.

In Chapter 3.3, Gao et al describe the fabrication of the CAVET (Current Aperture Vertical Electron Transistor) by Photoelectrochemical (PEC) formation of a current aperture. They describe the etch process, and the subsequent modification and optimization of the process for CAVET fabrication.

In Chapter 3.4, Estrada et al report on the first n-AlGaAs/p-GaAs/n-GaN heterojunction bipolar transistor formed via wafer fusion. Their results demonstrate the potential of wafer fusion for the production of electrically active heterostructures between lattice-mismatched materials.

We hope that this book will be useful for technologists, scientists, engineers, and graduate students who are working on wide band gap materials and devices. The book can also be used as a supplementary textbook for graduate courses on wide band gap semiconductor technology.

We gratefully acknowledge generous support of this work by the US Office of Naval Research under the MURI program (Grant No. N00014-98-1-0654) and guidance and support by Drs. H. Dietrich and J. Zolper who inspired this book.

Michael S. Shur
Robert Davis

Editors

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MATERIALS PROPERTIES OF NITRIDES. SUMMARY

SERGEY L. RUMYANTSEV AND MICHAEL. S. SHUR

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Introduction

The interest in III-N materials (stimulated by pioneering work of Pankove, Akasaki, Nakamura, and many others) dates back to 1970s. High-power microwave/millimeter wave and optoelectronic applications of nitrides have emerged, with nitride-based visible LEDs already accounting for billion dollar markets. These applications demand the improved materials quality and better device design, which in turn require the knowledge of nitride materials parameters.

Our recent book published in 2001¹ has listed important nitride parameters. However, intensive research on properties and device applications is continuing albeit with a saturated rate of growth (see Fig. 1.). The new results require revisions of the important parameters for these materials (the energy gap of InN being a dramatic example²⁵.) The goal of this Chapter is to provide such an update.

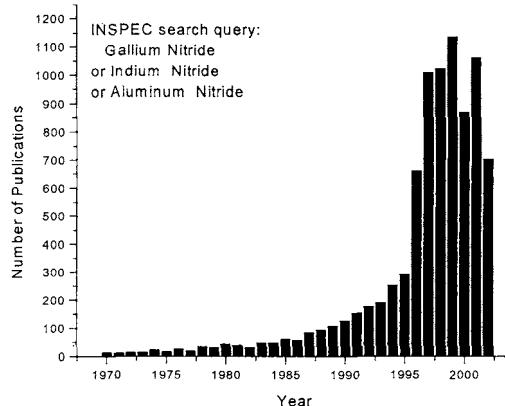


Fig. 1 Number of publication related to III-N materials versus year.

The discussion of semiconductor materials properties at a very basic level is given in² "Introduction to Electronic Devices", which also contains convenient tables summarizing the basic semiconductor equations and the definitions of basic semiconductor parameters. More detailed information is given in the two volumes "Survey of Semiconductor Physics" by Karl Boer³.

In certain cases, tensor parameters (such piezoelectric constants or elastic modulus) might be represented in different (but related) forms. R. E. Newnham's book⁴ can assist you in converting these parameters from the form given in this Chapter to any other form.

We attempted to include into this Chapter most important parameters and be selective in providing the values that we found to be more accurate or reliable. More information can be found in many reviews, tutorials, and books on nitrides and nitride device published in recent years (as well as on the WEB) given below.

Financial assistance from the Office of Naval Research, under the auspices of the MURI program, is gratefully acknowledged: Grant No. N00014-98-1-0654. (Monitored by Drs. J. Zolper and H. Dietrich).

Keywords: Nitrides; semiconductor parameters; materials properties.

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<http://nina.ecse.rpi.edu/shur/wofe2002/index.htm>

GALLIUM NITRIDE (GaN)

| Crystal structure | <u>Wurtzite</u> | <u>Zinc Blende</u> |
|---|---|---|
| Group of symmetry | $C_{6v}^4 P\bar{6}_3mc$ | $T_d^2 - F\bar{4}3m$ |
| Density (g/cm ³) | | 6.15 ^[22,49] |
| Dielectric constant | | |
| Static | 8.9-9.5 ^[49,75,78,100] | 9.7 |
| high frequency | 5.35 ^[42,49,75,78,100] | 5.3 ^[42] |
| Electron affinity (eV) | | 4.1 ^[88] , 3.4 ^[61] |
| Lattice constants (Å) o | a = 3.189 ^[109] c = 5.185 ^[49,109] | 4.52 ^[49] - 4.50 ^[78,109] |
| Optical phonon energy (meV) | 91.8 ^[27,49] | 91.9 ^[49] |
| Band structure | | |
| Energy gap (eV) | 3.51 ^[109] | 3.3 ^[109] |
| Temperature dependence of the energy gap ^[109] | 3.582-9.09×10 ⁻⁴ ×T ² /(T+830) | 3.358-5.93×10 ⁻⁴ ×T ² /(T+600) |
| Conduction band | | |
| Effective electron mass (in units of m ₀) (for electron mass in two dimensional electron gas see ref. ^[125]) | 0.20- 0.22 ^[80,109,111] | 0.15 ^[36] |
| Effective conduction band density of states (cm ⁻³) | 2.6×10 ¹⁸ | 1.4×10 ¹⁸ |
| Ionization energies of shallow donors ^[44,79,118] | | |
| Si (eV) | 0.012-0.03 | |
| O (eV) | 0.004-0.01 | |
| Valence band | | |
| Energy of spin-orbital splitting E _{SO} (eV) | 0.010- 0.018 ^[99,109] | 0.017 ^[109] |
| Energy of crystal-field splitting E _{cr} (eV) | 0.011- 0.022 ^[99,109] | |
| Effective hole mass (in units of m ₀) | | |
| heavy | 1.0 ^[109] | 1.3 ^[36,67] |

| | | |
|---|--|---------------------------|
| Effective valence band density of states (cm^{-3}) (For more details of the band structure see [109, 119] and references there in) | 2.5×10^{19} | 4.1×10^{19} |
| <i>Ionization energies of shallow acceptors</i> [5,44,100] | | |
| Mg (eV) | 0.14-0.21 | |
| Zn (eV) | 0.21 | |
| Native defect V _{Ga} (eV) | 0.14 | |
| <u>Electrical properties</u> | | |
| Breakdown field (Vcm^{-1}) | $\sim 5 \times 10^6$ [49] | $\sim 5 \times 10^6$ |
| Mobility ($\text{cm}^2 \text{V}^{-1} \cdot \text{s}^{-1}$) | | |
| Electrons (for temperature and concentration dependencies see also [22,40,59]) | ~ 1000 [50,69,85] | ≤ 1000 [59] |
| Holes | ≤ 200 [40] | ≤ 350 [10,38] |
| Diffusion coefficient($\text{cm}^2 \cdot \text{s}^{-1}$) | | |
| Electrons | 25 | 25 |
| holes | 5 | 9 |
| Electron saturation velocity (10^7cm s^{-1}) | 2 [112](experiment) 2-2.5 ^[8,15,60] (calc) | 2.0 ^[60] |
| Peak velocity (10^7cm s^{-1}) | 2 [112](experiment) 2.5-3 ^[8,15,60,112] (calc) | 2.5 ^[60] |
| Peak velocity field (kV/cm) | $150-180$ ^[8,15,60] | $100-150$ ^[60] |
| <u>Recombination parameters</u> | | |
| Hole diffusion length (μm) | 1-3.5 ^[21] | |
| Radiative recombination coefficient ($\text{cm}^3 \text{s}^{-1}$) | | 10^{-8} [83] |
| <u>Optical properties</u> | | [36] |
| Infrared refractive index | | 2.3 ^[49] |
| Refractive index spectra | [81,120] | [42] |

| | | |
|--|--|--|
| Reflectance spectra | [16, 32, 99,121] | |
| Absorption spectra | [9, 32, 42,81, 82, 92] | |
| Photoluminescence spectra | [24, 54,77, 99,92] | [51,115] |
| <u>Thermal properties</u> | | |
| Debye temperature (K) | | 820 ^[86] |
| Specific heat at 300K ($Jg^{-1}^{\circ}C^{-1}$) | | 0.49 ^[86] |
| 298<T<1773 | | 0.456+0.107×10 ⁻³ T ^[11] |
| Thermal conductivity ($Wcm^{-1}^{\circ}C^{-1}$) | | >2.1 ^[38,63,95,123,124] |
| Thermal diffusivity ($cm^2 s^{-1}$) | | 0.65 |
| Thermal expansion, linear ($^{\circ}C^{-1}$) | $\alpha_a = 5.59 \times 10^{-6}$ [49] | |
| | $\alpha_c = 3.17 \times 10^{-6}$ [49] | |
| <u>Mechanical properties</u> | | |
| Elastic constants (GPa)(see also ^[30,113]) | | |
| C_{11} | $390 \pm 15^{[90]}$ | 293 ^[113] |
| C_{12} | $145 \pm 20^{[90]}$ | 159 ^[113] |
| C_{13} | $106 \pm 20^{[90]}$ | |
| C_{33} | $398 \pm 20^{[90]}$ | |
| C_{44} | $105 \pm 10^{[90]}$ | 155 ^[113] |
| <u>Piezoelectric constants (C m⁻²)</u> ^[14,20,48,109,122] | | |
| e_{15} | -0.30 | |
| e_{31} | (-0.3)-(-0.55) | |
| e_{33} | 0.6–1.12 1,27 | |
| e_{14} | | 0.4 ^[94] |

ALUMINUM NITRIDE (AlN)

| | |
|--|--|
| Crystal structure | Wurtzite |
| Space group | $C_{6v}^4 - P\bar{6}_3mc$ |
| Density (g cm ⁻³) | 3.257 ^[96] |
| Dielectric constant | |
| static | 8.5 ^[49,78] |
| high frequency | 4.68-4.84 ^[100] 4.77 ^[49,78] |
| Electron affinity (eV) | 0.6 ^[13] , 1.9 ^[12,114] |
| Lattice constant (Å) | $a=3.112^{[109]}$ $c=4.982^{[109]}$ |
| Optical phonon energy (meV) | 113 ^[27,49] |
| Band structure | |
| Energy gap (eV) | 6.23 ^[109] |
| Temperature dependence of the energy gap ^[47,109] | $6.34 - 1.799 \times 10^{-3}$ $\times T^2 / (T + 1462)$ |
| Conduction band | |
| Effective electron mass (in units of m_0): | 0.3 ^[109] |
| Effective conduction band density of states (cm ⁻³) | 4.1×10^{18} |
| Ionization energies of donors ^[17,23,39, 43,53, 76, 98,105] | |
| Donor levels of N vacancies V_N (eV) | 0.17; 0.5; 0.8-1.0 |
| Donor level of N in Al sites N_{Al} (eV) | 1.4-1.85 |
| Donor level of Al in N sites Al_N (eV) | 3.4-4.5 |
| Donor level of C in Al sites C_{Al} (eV) | 0.2 |
| Valence band | |
| Effective hole masses (in units of m_0): | |
| Heavy: | |
| for k_z direction m_{hz} | 3.53 ^[102] |
| for k_x direction m_{hx} | 10.42 ^[102] |
| Effective valence band density of states (cm ⁻³) | 4.8×10^{20} |
| Ionization energies of acceptors ^[17,23,39, 43,53, 76, 98,102] | |
| Acceptor level of Al vacancies V_{Al} (eV) | 0.5 |

| | |
|---|--|
| Acceptor level of C in N sites C_N (eV) | 0.4 |
| Acceptor level of Zn in Al sites Zn_{Al} (eV) | 0.2 |
| Acceptor level of Mg in Al sites Mg_{Al} (eV) | 0.1 |
| (For more details of the band structure see ^[109] , and references there in) | |
| <u>Electrical properties</u> | |
| Breakdown field ($V\text{cm}^{-1}$) | $(1.2 \div 1.8) \times 10^6$ |
| Mobility ($\text{cm}^2 \text{V}^{-1} \cdot \text{s}^{-1}$) | |
| Electrons | 135 ^[91] |
| holes | 14 ^[40] |
| Diffusion coefficient($\text{cm}^2 \cdot \text{s}^{-1}$) | |
| Electrons | 3.3 |
| holes | 0.3 |
| Electron saturation velocity (10^7cm s^{-1}) | 1.4 ^[91] |
| Peak velocity (10^7cm s^{-1}) | 1.7 ^[91] |
| Peak velocity field (kV/cm) | 450 ^[91] |
| <u>Recombination parameters</u> | |
| Radiative recombination coefficient ($\text{cm}^3 \text{s}^{-1}$) | 0.4×10^{-10} ^[33] |
| <u>Optical properties</u> | |
| Infrared refractive index | 2.15 ^[49,100] |
| Refractive index spectra | [31,41, 42, 55,56,71, 118,] |
| Reflectance spectra | [7, 45,46,71] |
| Absorption spectra | [5, 31, 56, 71, 89] |
| Photoluminescence spectra | [66,101] |
| <u>Thermal properties</u> | |
| Debye temperature (K) | 980 ^[88] |
| Specific heat at 300K ($\text{Jg}^{-1} \text{°C}^{-1}$) | 0.73 ^[62,74,87] |
| At 300K<T<1800K ^[59] | $1.097 + 7.99 \times 10^{-5} \times T - 0.358 \times 10^5 \times T^{-2}$ |
| At 1800K<T<2700K ^[62] | $0.892 + 0.188 \times 10^{-3} \times T$ |
| Thermal conductivity ($\text{Wcm}^{-1} \text{°C}^{-1}$) | 2.85 ^[97] , 3.3 ^[124] |
| Thermal diffusivity ($\text{cm}^2 \text{s}^{-1}$) | 1.47 |
| Thermal expansion, linear, ($^{\circ}\text{C}^{-1}$) | $\alpha_a = 4.2 \times 10^{-6}$ ^[49] |
| | $\alpha_a = 5.3 \times 10^{-6}$ ^[49] |

| Mechanical properties | | |
|---|---|---------------------|
| Elastic constants (GPa)(see also ^[57, 113]) | | |
| C ₁₁ | 410.5±10 ^[73] | 410 ^[30] |
| C ₁₂ | 148.5±10 ^[73] | 140 ^[30] |
| C ₁₃ | 98.9±3.5 ^[73] | 100 ^[30] |
| C ₃₃ | 388.5±10 ^[73] | 390 ^[30] |
| C ₄₄ | 124.6±4.5 ^[73] 122±1 ^[126] | 120 ^[30] |
| Piezoelectric constants (C m⁻²) ^[14,19,48,68,84,102] | | |
| e ₁₅ | (-0.33)-(-0.48) | |
| e ₃₁ | (-0.38)-(-0.82) | |
| e ₃₃ | 1.26 – 2.1 | |

INDIUM NITRIDE (InN)

| | |
|---|---|
| <u>Crystal structure</u> | Wurtzite |
| Space group | $C_{6v}^4 - P6_3mc$ |
| Density (g cm ⁻³) | 6.81-6.89 ^[106] |
| Dielectric constant | |
| static | 15 ^[106] 15.3 ^[49, 78] |
| high frequency | 6.7-8.4 ^[49,78] ; 5.8-9.3 ^[58] |
| Lattice constants (Å) | $a = 3.54^{[49,109]}$ $c = 5.70^{[49,107]}$ |
| Optical phonon energy (meV) | 73 ^[49, 58] |
| <u>Band structure</u> | |
| Energy gap (eV) | Early studies showed 1.9 – 2.05 ^[47,104] Recent studies indicate 0.7-1.0 ^[25,26,29,52,72, 116,117] |
| <u>Conduction band</u> | |
| Effective electron mass (in units of m_0): | 0.07-0.26 ^[117] ; 0.14 ^[58] |
| Effective conduction band density of states (cm ⁻³) | $4.6 \times 10^{17} - 3.3 \times 10^{18}$ |
| <u>Ionization energy of donor</u> ^[105] | |
| Donor level of N vacancies V_N (meV) | 40-50 |
| <u>Valence band</u> | |
| Effective hole mass (in units of m_0): | |
| heavy | 1.63 ^[65] |
| <u>Electrical properties</u> | |
| Mobility (cm ² V ⁻¹ ·s ⁻¹) | |
| Electrons | 2700 ^[103] 1000-1900 ^[25,52,70,117] |
| Diffusion coefficient(cm ² ·s ⁻¹) | |
| Electrons | 67 25-47 |
| <u>Optical properties</u> | |
| Infrared refractive index | 2.9 ^[49] |

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|--|--|-----------------------------|
| Refractive index spectra | [118] | |
| Reflectance spectra | [108,117] | |
| Absorption spectra | [25,47, 52,72,116,117] | |
| Photoluminescence spectra | [25,26, 29,72,116] | |
| <u>Thermal properties</u> | | |
| Debye temperature (K) | 660 [28] | |
| Specific heat (Jg ⁻¹ °C ⁻¹) | 0.30 ^[28] | |
| Temperature coefficient of Specific heat 298K<T<1273K ^[86] | 9.39×10 ⁻⁵ | |
| Thermal conductivity (Wcm ⁻¹ °C ⁻¹) | 0.45 ^[64] | |
| Thermal diffusivity (cm ² s ⁻¹) | 0.2 | |
| Thermal expansion, linear,(°C ⁻¹) | $\alpha_a = 3.8 \times 10^{-6}$ ^[93,110] $\alpha_c = 2.9 \times 10^{-6}$ ^[93,110] | |
| <u>Mechanical properties</u> | | |
| Elastic constants (GPa) | [93, exper.] | (see refs. in [110], calc.) |
| C ₁₁ | 190±7 | 271-298 |
| C ₁₂ | 104±3 | 92-124 |
| C ₁₃ | 121±7 | 70-109 |
| C ₃₃ | 182±6 | 25-278 |
| C ₄₄ | 10±1 | 46-89 |
| <u>Piezoelectric constants (C m⁻²)</u> ^[14,122] | | |
| e ₃₁ | (-0.45)–(-0.56) | |
| e ₃₃ | 0.81–1.09 | |

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KINETICS, MICROSTRUCTURE AND STRAIN IN GaN THIN FILMS GROWN VIA PENDEO-EPITAXY

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Maskless pendo epitaxy involves the lateral and vertical growth of cantilevered "wings" of material from the sidewalls of unmasked etched forms. Gallium Nitride films grown at 1020°C via metalorganic vapor phase epitaxy on GaN/AlN/6H-SiC(0001) substrates previously etched to form [1100]-oriented stripes exhibited similar vertical [0001] and lateral [1120] growth rates, as shown by cross-sectional scanning electron microscopy. Increasing the temperature increased the growth rate in the latter direction due to the higher thermal stability of the GaN(1120) surface. The (1120) surface was atomically smooth under all growth conditions with a root mean square (RMS) = 0.17 nm. High resolution X-ray diffraction and atomic force microscopy of the pendo-epitaxial films confirmed transmission electron microscopy results regarding the significant reduction in dislocation density in the wings. This result is important for the properties of both optoelectronic and microelectronic devices fabricated in III-Nitride structures. Measurement of strain indicated that the wing material is crystallographically relaxed as evidenced by the increase in the c-axis lattice parameter and the upward shift of the E2 Raman line frequency. A strong D°X peak at 3.466 eV was also measured in the wing material. However, tilting of the wings of $\leq 0.15^\circ$ occurred due to the tensile stresses in the stripes induced by the mismatch in the coefficients of thermal expansion between the GaN and the underlying substrate.

Keywords: Pendo-epitaxy; strain; GaN.

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1. Introduction

Several research groups have determined that lateral epitaxial overgrowth (LEO) and pendoepitaxy (PE) can significantly reduce the dislocation density in GaN and AlGaN films grown on sapphire¹⁻⁵ and SiC.⁶⁻¹⁴ Pendoepitaxy is an overgrowth technique in which the stripes and/or other “seed” forms are etched through the nitride material and into the substrate. The material of the stripe, e.g., GaN or AlGaN or other material, is again grown either laterally and then vertically over a mask of, e.g., amorphous silicon nitride (Figure 1a), or laterally and vertically from the stripe material (Figure 1b), i.e., “maskless” PE. In the former, deposition is forced to selectively begin on the sidewalls,^{11,15} and the masks confine the threading dislocations originating from the heteroepitaxial growth to their original stripes. If the deposited material nucleates on the substrate, vertical growth from this surface must be minimized to prevent interference with the lateral growth from the sidewalls of the stripes. This process route has enabled growth of continuous films of GaN and AlGaN on SiC^{8,11,15} and Si(111)¹⁰ substrates to be realized. However, the growth fronts over the masked regions are tilted. As a consequence, vertical boundaries form above each mask during the coalescence of these growth fronts, due to the misregistry of the material. The presence of two crystallographic orientations tilted towards each other has also been reported in GaN films grown via LEO.^{4,16-19} The elimination of the growth mask reduces both the crystallographic tilt and a source for impurities, and the PE growth of AlGaN films can be realized as shown in Figure 2.¹⁰ This figure also shows that the threading dislocation density in the laterally grown sidewall regions is significantly reduced relative to the initial GaN seed stripe.

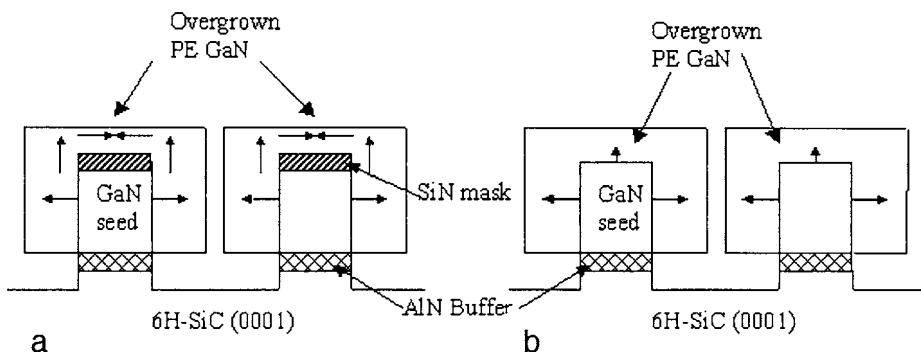


Figure 1. Schematic of a) PE growth from GaN seed laterally off the sidewalls then vertically and laterally over the silicon nitride mask and b) PE growth from GaN seed laterally off the sidewalls and vertically off the stripe

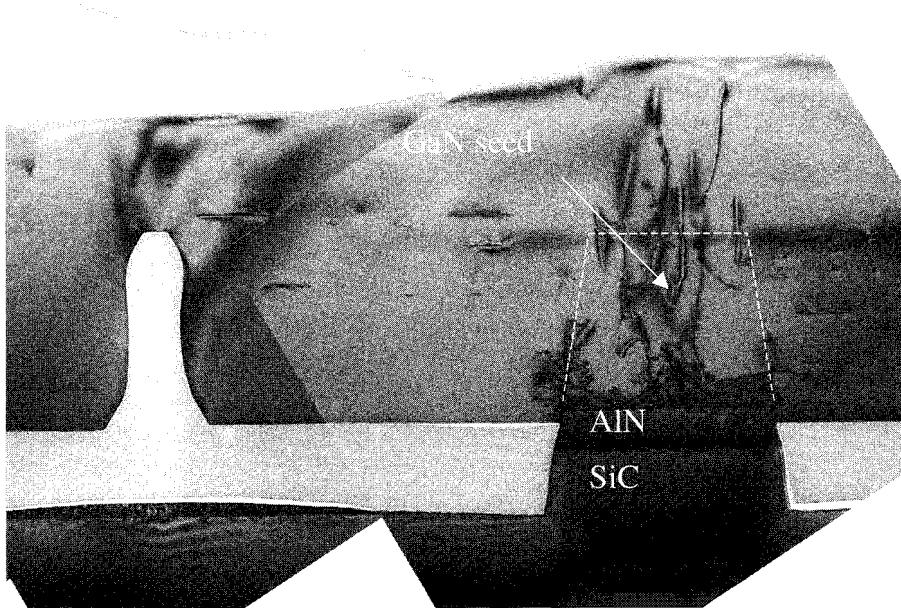


Figure 2. Composite of cross-sectional TEM micrographs of a PE Al_{0.1}Ga_{0.9}N film. Note the threading dislocations continue from the GaN stripes into the film.

In essence, PE is a new approach to selective epitaxy of GaN and AlGaN layers that incorporates mechanisms of growth exploited by the conventional LEO process, but usually alleviates the mask alignment problems through the use of the substrate itself as a pseudo-mask. The following Sections describe the recent advancements concerning the effect of growth parameters on growth rates, surface microstructure, the reduction in defects and strain, and the structural, microstructural and optical characteristics of maskless GaN thin films grown via PE.

2. Experimental

Each AlN buffer layer, GaN seed layer and maskless PE GaN and/or AlGaN layer was sequentially grown on a 6H-SiC(0001) substrate in a cold-walled, vertical, pancake-style metalorganic vapor phase epitaxy (MOVPE) system. The 100 nm thick AlN buffer layers and the 1 μ m thick GaN seed layers were grown at 20 Torr and platter temperatures of 1120°C and 1020°C, respectively. The precursor species (mass flow rates) of trimethylaluminum (TMA; 5.4 μ mol/min), triethylgallium (TEG; 101 μ mol/min) and ammonia (NH₃; 0.14 mol/min) were mixed with a high-purity H₂ diluent (3 slm) in a two-inch internal diameter sleeve located two inches above the substrate.

A Ni layer was deposited on patterned photoresist stripes on each GaN seed layer by e-beam evaporation. Etch mask stripes were subsequently produced using standard photolithography lift-off techniques. An inductively coupled plasma system and a mixture of Cl₂ and BC_l₃ gases were used to etch the unmasked striped regions through the GaN and the AlN and into the near-surface areas of the SiC substrate. The Ni was then removed using a 5 min dip in HNO₃. The remaining GaN seed layer consisted of 2 and 3 μm wide stripes separated by distances of 12 and 7 μm , respectively, and oriented along [1100]. The exposed (1120) sidewalls and the top (0001) face of the stripes were subsequently dipped in 50% hot HCl to clean the surface prior to regrowth of the PE layer.

The lateral and vertical growth rates of the PE GaN films were investigated over the ranges of temperature and TEG flow rates of 1040°C-to-1100°C and 17-to-100 $\mu\text{mole}/\text{min}$, respectively. The flow rates of the NH₃ and the H₂ diluent were maintained at 0.14 mol/min and 3 slm, respectively. The total gas flow into the reactor remained constant for all the experiments to assure a uniform laminar flow over the substrate.

Cross-sectional images of the surface microstructure of the wing and stripe material were obtained using scanning electron microscopy (SEM) and were used to calculate the lateral and/or vertical growth rates of these features. Atomic force microscopy (AFM) was employed in the tapping mode to obtain higher resolution micrographs of the growth surface as well as the aerial distribution of dislocations that terminated at the (0001) surface. Defect characterization and measurements of the strain via changes in lattice parameter were conducted using the results from on- and off-axis rocking curves and reciprocal space mapping acquired via high-resolution x-ray diffraction (HRXRD). Wing tilt in the uncoalesced pendo epitaxial GaN was measured using XRD via determination of an ω rocking curve about the GaN(0002) peak with the scatter plane perpendicular to the stripe. Optical characterization of spatially resolved (\approx 400 nm) band-edge emission was performed via micro-photoluminescence (PL) at 10K using a He-Cd (λ =325 nm) laser. Shifts in the frequency of the E2 line measured at 10K using an Ar-ion (λ =488 nm) laser coupled to micro-Raman unit with a spatial resolution of \approx 700 nm, revealed discrete regions of strain in the PE films. Micro-Raman spectra of the LO phonon also yielded information regarding the carrier concentration of the overgrown material. Secondary-ion mass spectroscopy (SIMS) depth profiles were obtained to determine the presence and concentrations of carbon, oxygen and silicon in the GaN films.

3. Results and Discussion

3.1. Growth and decomposition

The curves and micrographs in Figures 3 and 4 are related by the lower case letters in each and show analytically and pictorially, respectively, the effect of growth temperature for two V/III flow rate ratios on the lateral/vertical GaN growth rate ratios (R). The V/III ratio was increased from 1323 to 6160 at all temperatures via reduction in the TEG flow

Lateral and Vertical Growth Components

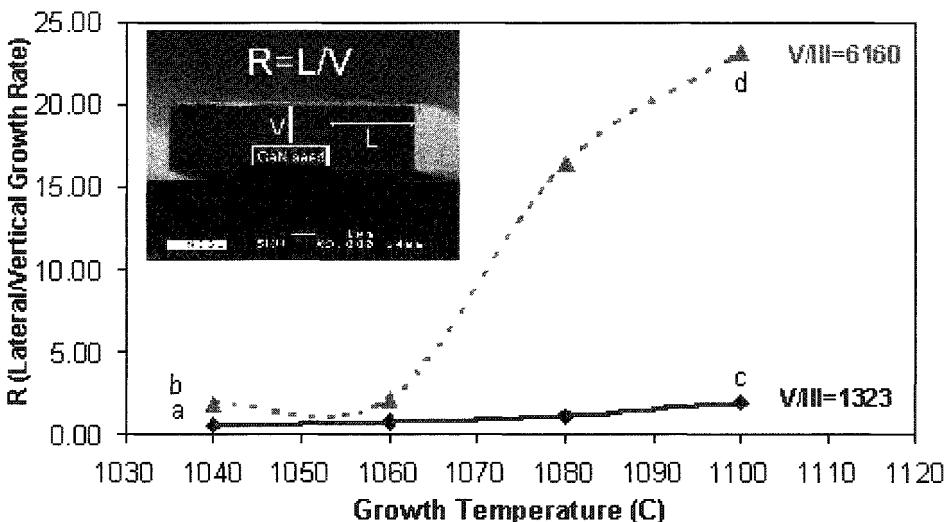


Figure 3. Ratio of lateral (L)-to-vertical (V) growth rates (R) as a function of growth temperature and $V(NH_3)/III(TEG)$ ratio. The NH_3 flow rate remained constant. The growth time was 1 hr for each point.

rate from 101.2 $\mu\text{mol}/\text{min}$ to 16.7 $\mu\text{mol}/\text{min}$. The most dramatic increase in R occurred for the V/III ratio of 6160 after the growth temperature was increased beyond 1060°C, as shown, e.g., in point d on the upper curve in Figure 3 and the associated Figure 4d. However, the roughness of the (0001) surface also increased above an R=10; as seen in the SEM image, Figure 4d, of a sample having a value of R of approximately 24. Uncoupling the lateral and vertical growth rates and plotting them as a function of temperature in the manner shown in Figure 5 can obtain additional understanding regarding the changes in the values of R. Calculation of the growth rates from the SEM cross-sectional micrographs shown in Figure 4 and additional micrographs acquired for the PE GaN films grown at the intermediate temperatures revealed that the lateral growth rate increased with increasing temperature and the vertical growth rate either remained constant or decreased for both V/III ratios. In Figure 5 the growth rates, both laterally and vertically, are greater for the V/III ratios of 1323 than for the ratio of 6160 due to the larger amount of TEG used in growth. For V/III ratios of 1323, the vertical growth was dominant over lateral growth at temperatures below $\approx 1080^\circ\text{C}$. An increase in lateral growth at 1100°C changed the value of R to greater than 1. The dramatic increase in the value of R above 1 for PE growth at a V/III ratio = 6160 for $T > 1060^\circ\text{C}$ occurred due to

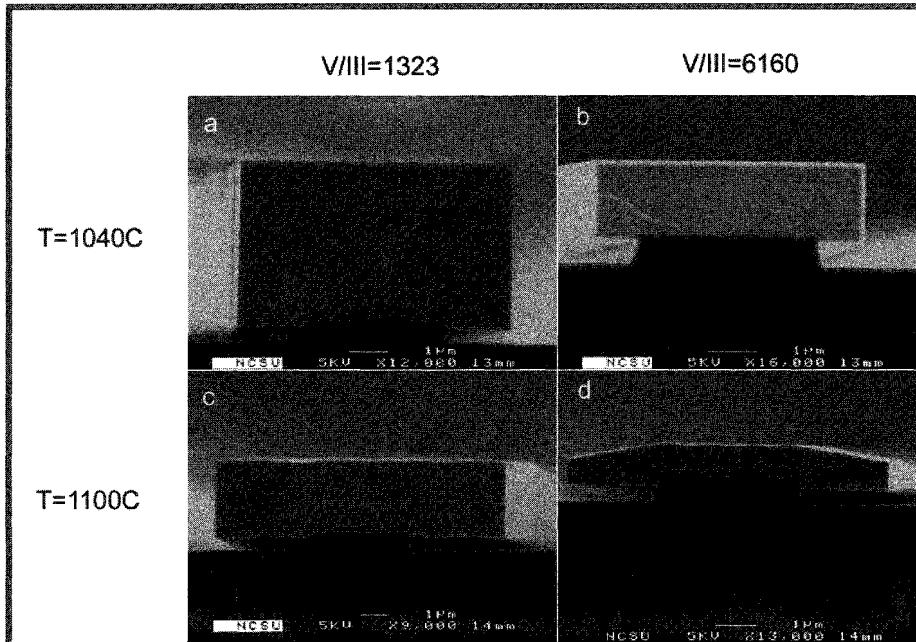


Figure 4. Cross-sectional SEM [1̄00] view of uncoalesced PE GaN films grown under different temperatures and V/III gas ratios for 1 hour at 20 torr total pressure. The original GaN seed was 1 μm tall. Note: the magnification for each SEM picture is different.

the drop in the vertical growth rate to near zero. At 1060°C and above, decomposition of the (0001) surface occurred in competition with the vertical growth of GaN; however, it did not affect lateral growth. This competition is obvious in Figure 4d where growth in the [1120] has produced large wings off the original seed, but the (0001) surface is rough and very little vertical growth has occurred.

Gallium nitride decomposes above 800°C in flowing hydrogen,²⁰⁻²³ and MOVPE becomes a near equilibrium competitive process between adatom incorporation, desorption into the gas phase and GaN decomposition. This competition was particularly relevant and made complex in the present research, as the PE GaN films were grown at temperatures exceeding those normally employed in the MOVPE of this compound in the presence of both H₂ and NH₃. This latter gas decomposes to provide atomic nitrogen as well as atomic and additional molecular hydrogen that chemically react with the GaN(0001) surface.^{24,25} However, the decomposition rate of the GaN(0001) surface at 1000°C in H₂ is reduced two orders of magnitude by the addition of NH₃, as it blocks sites needed for GaN decomposition.²³ For this reason a large NH₃/TEG ratio is used during MOVPE growth. Nitrogen generated from the decomposition of NH₃ must be larger than the desorption flux of N to guarantee a saturation surface coverage of this species²⁶. If too much NH₃ is used the number of open surface sites is reduced and the

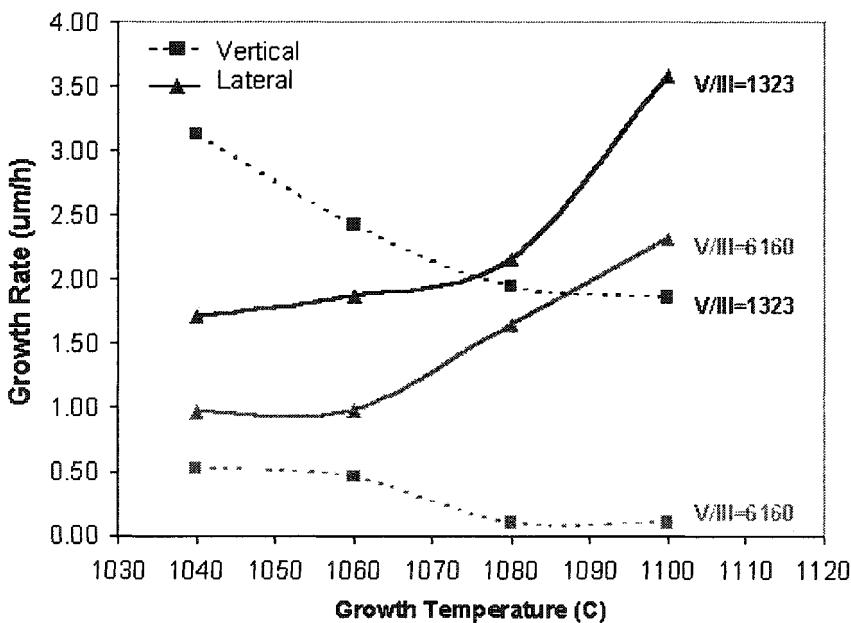


Figure 5. Lateral and vertical growth rates as a function of growth temperature and $\text{V}(\text{NH}_3)/\text{III}(\text{TEG})$ ratio. The NH_3 flow rate remained constant.

growth rate decreases.^{27,28} However, there are a range of NH_3 flow rates wherein the growth rates are controlled by the flux of metal species to the surface of the growing film. This is demonstrated in Figure 5 by the reduction in vertical growth of the PE samples at all temperatures with a reduction in TEG flow (increase in V/III ratio).

Early experiments of GaN growth on different crystallographic orientations of sapphire crystals also showed (1120) to have a higher thermal stability than (0001).²⁹ This was also borne out in our PE GaN experiments at 1100°C wherein growth occurred along [1120] and growth and decomposition occurred concomitantly along [0001]. Moreover, no indication of (1120) decomposition was observed under any growth conditions at 1100°C including low TEG and high NH_3 flow rates. As such, lateral growth rates along [1120] can be controlled solely by temperature.

3.2 Surface microstructure

The modes of nucleation and growth of a GaN(0001) film on an AlN(0001) buffer layer occur via the sequential formation of three-dimensional hexagonal islands that coalesce and allow the continuation of growth via step-flow mechanism,³⁰ as shown by the results of AFM studies presented in Figures 6a and b. The dislocation indicated by the white arrow in Figure 6a is one point (of two) of a heterogeneous step. These steps are generated on a terrace surface at the points of and due to the intersections of the terrace

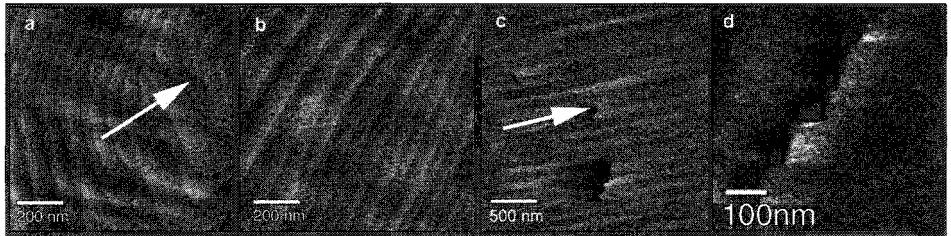


Figure 6. AFM micrographs acquired from a) the (0001) GaN stripe area, b) the wing GaN (0001) area, and c) and d) the GaN (1120) wing face. Arrows in a) and c) point to dislocations intersections at the surface of these respective planes. The striations in c) are electronic noise from the AFM; step structures have never been observed on this plane.

by a screw and/or mixed-type dislocations.³¹ Homogeneous steps are produced by the step-flow growth of the material. Similar dislocations and their associated heterogeneous steps were never observed in the wing regions of the (0001) surface; only homogeneous steps such as those shown in Figure 6b were present. The (1120) surface is nonpolar and consists of two surface Ga atoms and two surface N atoms per unit cell.³² No steps were observed on the (1120) plane over a 2.5 μm scan, as shown in Figure 6c. A higher resolution image of the very bottom volume of the (1120) surface in Figure 6d also shows the absence of steps as well as the termination of dislocations. The former observation suggests that either the step height, if steps exist, is less than 0.15 nm or below the noise-limited resolution of the AFM or that the terrace width of the steps is sufficiently small (or large) that they cannot be observed by our AFM. The dislocations were only observed near the bottom of the volume of the GaN wings, possibly indicating that they were generated at the vertical interface between the AlN buffer layer and the laterally grown GaN.

The presence of dislocations with screw and edge character in the stripe and wing areas were determined via ω scans of the (0002) and of the (1120) x-ray reflections. The FWHM values of the rocking curves in the on-axis (0002) reflection indicate the concentration of screw-type dislocations while values of off-axis (3032) FWHM determine the relative density of edge-type dislocations.³³ A reduction in screw-type dislocations in the wings with respect to the stripes is indicated by a reduction in FWHM of the (0002) reflections from 646 arcsec to 354 arcsec. The off-axis FWHM of the wing area was 126 arcsec compared to 296 arcsec for the stripe indicating a reduction in the edge-type dislocations as well.

The (0001) surface microstructure was very sensitive to growth temperature, even in regimes of temperature and V/III ratios where (0001) surface decomposition was not prevalent. For our reactor geometry and growth conditions, the optimum temperature for planar growth of conventional GaN films was 1020°C. The rates of coalescence of the growth fronts of the material growing laterally from the sidewalls of the PE stripes were enhanced by an increase in temperature. However, increasing the temperature beyond 1020°C increased the propensity for the growth of spiral hillocks on the (0001) surface

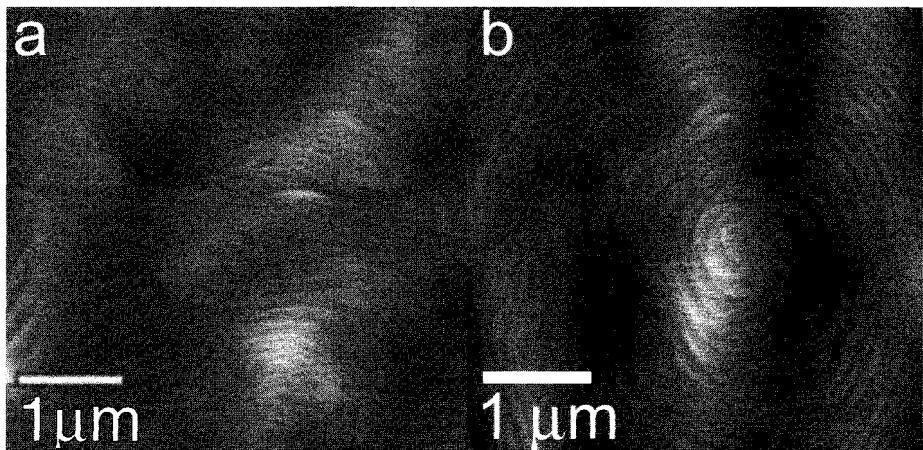


Figure 7. AFM images obtained from the center of a stripe region after early stages of coalescence on a pendo post (3-7 scheme) (a) stable surface formed at 1020°C, $R_{MS}=0.35\text{nm}$. (b) Unstable surface with quadruple hillock formed during deposition at 1100°C, $R_{MS}=0.31\text{nm}$

within the stepped microstructure.³⁴ Figures 7a and b shows a comparison of the stepped microstructures obtained on the (0001) surface during PE growth at 1020°C and 1100°C, respectively. The R_{MS} roughness was nearly the same in each case; however, the occurrence of hillocks such as that shown in Figure 7b represents the early stage of growth instability that occurred at elevated temperatures.

Spiral hillocks are a consequence of preferred growth at heterogeneous steps that have their origin at the intersections of the aforementioned dislocations with the (0001) growth surface.³⁵⁻³⁷ Stable growth of spiral hillocks occurs under conditions that allow continuous integration of adatoms at steps, if the rate of homogeneous step advancement is synchronous with the rotational velocity of the hillock. For the hillock to be annihilated under steady-state conditions, the advancing homogeneous step must reach the center of the hillock at the same time that the rotation of the hillock completes one revolution.

Unfortunately, hillocks increase in size due to the large lateral growth rate at high temperatures; they tend to eventually cover the laterally growing areas of the (0001) surface. In many cases of PE growth at $T=1100^{\circ}\text{C}$, the vertical growth is solely attributed to hillock growth. As mentioned in the previous section, the desorption flux of N and Ga species increases with an increase in temperature. Therefore, the adatom diffusion length decreases. The probability of adatom condensation at homogeneous steps relative to that at heterogeneous steps decreases with an increase in temperature, and the stable growth of spiral hillocks occurs.

All the hillocks were centered on the stripe regions, i.e., within the areas over the original seed material; no hillocks were observed to originate in the PE overgrowth

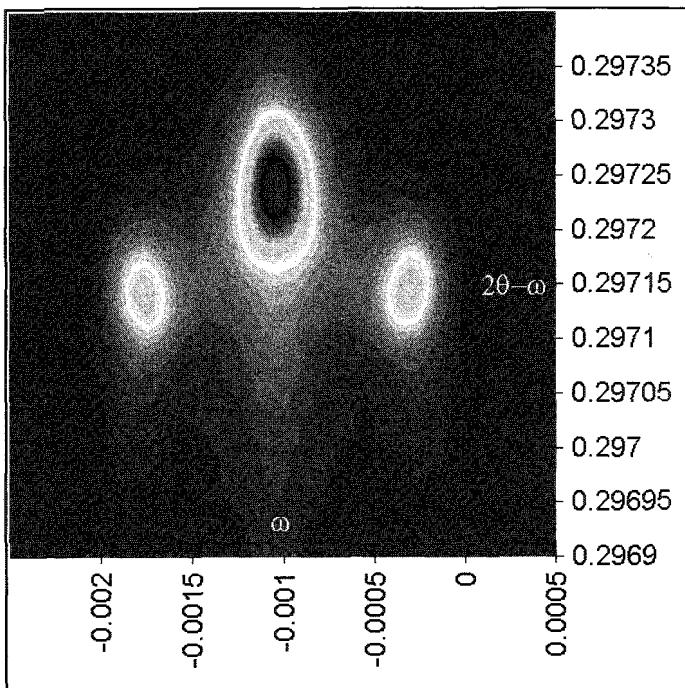


Figure 8. High resolution XRD reciprocal space map of stripe and wing regions in an uncoalesced pendo epitaxial GaN film.

regions even at the highest growth temperature of 1100°C. An investigation was conducted to observe and characterize the defects above the stripe regions, including the original seed material, as well as in the overgrowth or wing regions. As described above, the AFM studies of the (0001) surface structure of the stripe material revealed heterogeneous steps (see arrow in Figure 6a). An examination of Figure 2 reveals no apparent lateral propagation of the vertically oriented threading dislocations from within the stripe region into the wing region. The straight homogeneous steps shown in the AFM micrograph of the (0001) surface in the wing area in Figure 6b indicate the absence of threading dislocations. Hillocks did not grow on the (1120) surface under any conditions, even around the dislocations that intersect this surface, as shown in Figures 6c and 6d. This indicates that the intersecting dislocations are pure edge in character. The aforementioned thermal stability of this surface may also contribute to the absence of hillocks and in turn the low RMS value.

3.3 Tilt and strain

Reciprocal space maps of the uncoalesced PE material revealed a center peak produced by the seed material and two side peaks produced by the two wings, as shown in Figure 8, when the beam direction was perpendicular to the seed stripe direction. The two wing

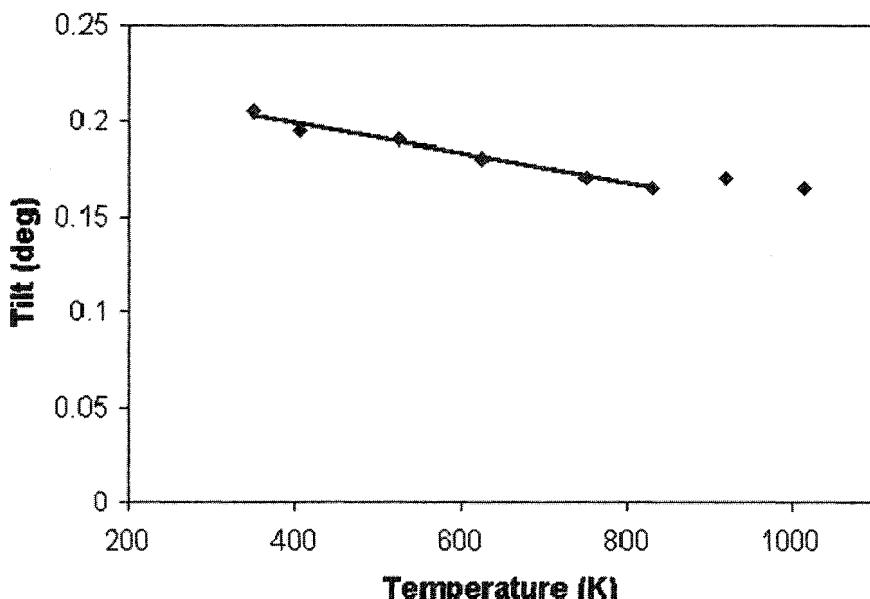


Figure 9. Plot of crystallographic tilt in uncoalesced PE GaN films, measured by XRD, as a function of film temperature.

peaks are shifted with respect to the seed layer peak in the omega direction as a result of crystal tilt in the wing regions. The $2\theta-\omega$ shift is due to strain relaxation in the wing regions.

The origin of the tilt in maskless PE is due to the mismatch in the coefficients of thermal expansion between the GaN stripe material and the SiC substrate. Experimental and theoretical simulations have shown that the crystallographic tilt of GaN is induced by tensile stresses.³⁸ The higher the tensile stress in the stripe region, the higher the wing tilt that is measured by XRD. The strains generated by these stresses cause the wings to bend upward during cooling from the growth temperature. The wing tilt in an uncoalesced PE film heated to 800°C was measured at selected temperatures via high-temperature XRD. The results of this experiment are shown in Figure 9.³⁹ As the temperature increased, the measured wing tilt decreased due to the relaxation of the GaN stripe material. The wing tilt is not completely relieved at higher temperatures as seen in Figure 9. Stress is also induced in the GaN epilayer due to the lattice mismatch between the AlN buffer layer and the GaN thin film. These stresses are not relieved thermally but also contribute to the wing tilt.

Once free of the strain effects caused by the SiC(0001) substrate, a slight relaxation of both the $a(-0.07\%)$ and $c(+0.03\%)$ lattice parameters was observed in the wing region. In Figure 8, the two wing peaks are shifted with respect to the seed layer in the ω direction due to strain relaxation in the wing regions. Micro-Raman measurements showed the

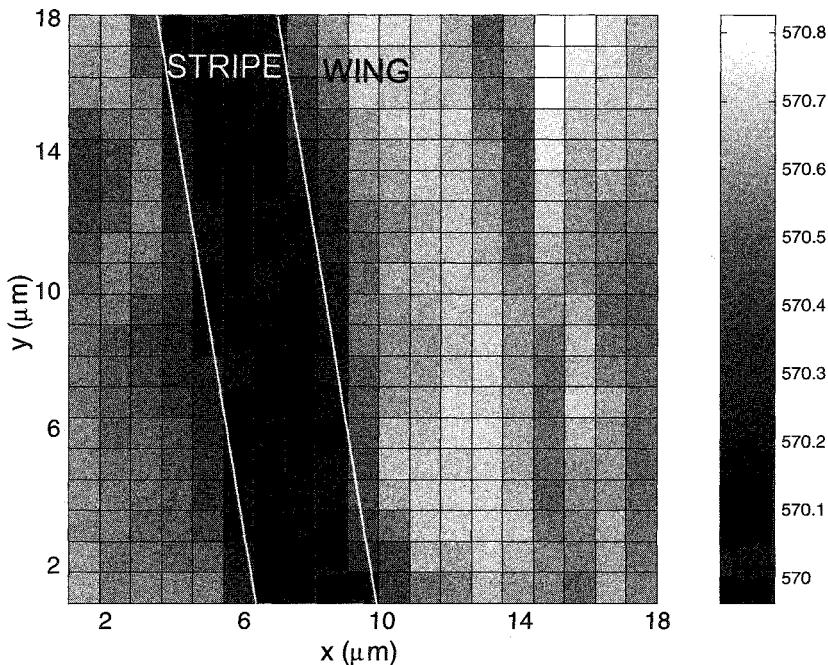


Figure 10. Two-dimensional plot of Raman line frequency of an uncoalesced PE GaN film (specifically a wing and stripe region). An increase in the line frequency represents a relaxation of strain in the material.

same strain reduction in the uncoalesced PE wings. An upward shift of the E2 Raman line of approximately 0.7 wavenumbers in the wing area with respect to the stripe was observed in the two-dimension plot of the E2 frequency distribution in Figure 10 and indicated a relaxation in the former. A change in the c-axis lattice parameter of $\sim 0.02\%$ has been calculated from the frequency shift in the E2 line using the methods developed by Kisielowski and co-workers.⁴⁰ The resulting shifts in lattice parameters agree well with the calculated change in the c-axis measured with XRD.⁴¹

3.4. Optical properties, impurities and carrier concentrations

Another important advantage of PE growth without a mask is the elimination of an impurity source. Analyses of the center frequency of the coupled LO phonon-plasmon (LPP) in micro-Raman spectra⁴² from cross-sections of LEO material showed that regions grown over an SiO_2 mask contain carrier concentrations that exceed 10^{18} cm^{-3} . This is significant evidence of considerable impurity incorporation.^{43,44} Micro-Raman spectra of the PE samples grown in the present research showed an uncoupled E1 (LO) phonon at 740 cm^{-1} indicating that the carrier concentration was $< 10^{17} \text{ cm}^{-3}$ in both the

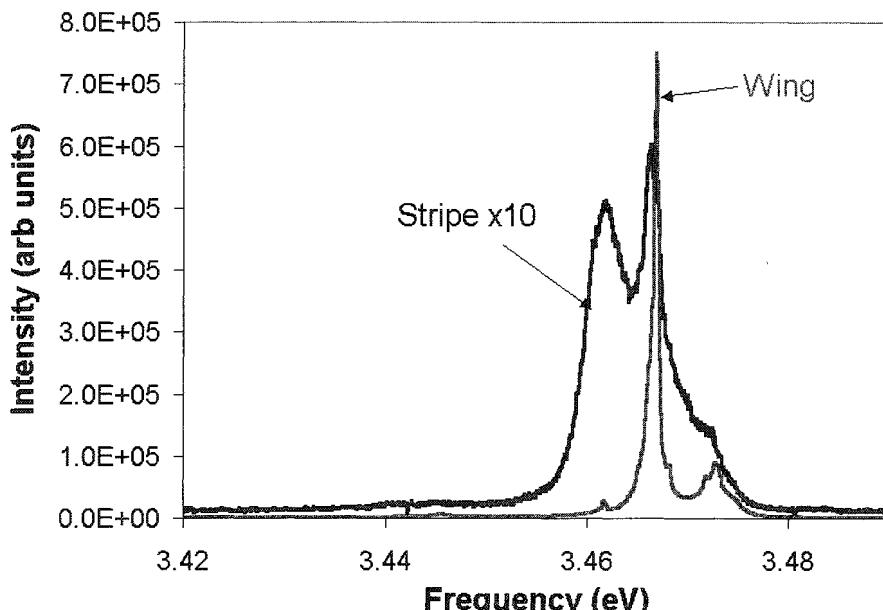


Figure 11. Photoluminescence (PL) spectra taken from the wing and stripe region of an uncoalesced PE GaN film. Note the FWHM value for the wing peak is <300 μ eV.

wing and the stripe material, as expected for overgrowth without a mask. This was further quantified by secondary ion mass spectrometry (SIMS) ion imaging that showed no difference in carbon, oxygen and silicon concentrations between the wing and stripe areas.

The strong donor bound exciton (D^0X) PL peak emitted from the wing material had a FWHM <300 μ eV (below the resolution of the equipment); the analogous peak for the stripe material had a FWHM of 12 meV, as shown in Figure 11. The former peak is a hallmark of the markedly lower strain in the wing material, and it is comparable to that emitted by completely relaxed homoepitaxial GaN film grown on bulk GaN crystals.⁴⁵ A downshift in the D^0X peak of 5 meV in the stripes with respect to the wing is due to the larger tensile strain in the former. Some shift in this peak could also be due to unintentional doping; however, analysis of the results of SIMS measurements revealed no evidence for this factor. The broadening of the D^0X line in the stripe material and its decreased intensity relative to that of the peak from the wing material is due both to the inhomogeneous strain and the higher dislocation density in the former.⁴¹

4. Summary

Crystallographically relaxed wing regions are produced during maskless pendo epitaxy of uncoalesced GaN(0001). The D⁰X PL signal from these regions is strong and has a FWHM less than <300 μeV. The stresses generated in the stripe regions are due mainly to the mismatch in the coefficients of thermal expansion between the GaN film and the SiC substrate. The resulting strains result in crystallographic tilt of the wing material on cooling from the growth temperatures. Growth rates in the [0001] and [1120] directions are different because of the different growth mechanisms and the differences in thermal stability of each surface and can be controlled by growth temperature and the NH₃/TEG molar gas ratio. Adatom diffusion is limited on the GaN(0001) surface at the 1100°C temperature normally used for PE growth due to decomposition of this surface. However, the diffusion is sufficient such that the adsorbed species reach the heterogeneous steps generated at the terminations of screw and mixed dislocations with the growth surface and subsequently results in the formation of spiral growth hillocks that propagate laterally across the surfaces of the stripe and wing regions. A reduction in growth temperature reduces the lateral growth rate; however, it also results in smooth, stepped, hillock-free (0001) PE surface with atomically smooth (1120) sidewalls.

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STRAIN OF GaN LAYERS GROWN USING 6H-SiC(0001) SUBSTRATES WITH DIFFERENT BUFFER LAYERS

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Gallium nitride films of increasing thickness have been grown on either AlN or AlGaN substrates. The state of stress of these biaxially stressed layers gradually changed from compression to tension with regard to both their average strain and their local strain along the [0001] growth direction. The components of both the compressive and tensile stresses are caused by the mismatch in lattice parameters between the GaN and the buffer layer and the mismatch in the coefficients of thermal expansion between GaN and SiC, respectively. The compressive stress is partially relieved within the first 20 nm in the GaN film grown on the AlN buffer layer. The relief of the remaining stress follows an exponential dependence on the thickness of the GaN layer with values for the characteristic decay length of 0.24 μm and 0.64 μm for the AlN and AlGaN buffer layer, respectively. The relaxation mechanism is discussed in terms of the formation of misfit dislocations via surface undulations.

Keywords: Strain; GaN; buffer layers.

1. Introduction

Silicon carbide has several advantages as a substrate for the growth of III-Nitride films and heterostructures, including moderately close lattice matching to AlN and GaN, higher thermal conductivity and relatively easy cleavage along [1120]. Buffer layers of non-conductive AlN¹⁻³ and, more recently, conductive AlGaN,^{4,5} are necessary to achieve GaN layers via metalorganic vapor phase epitaxy (MOVPE) with a smooth surface and a reasonably low density of threading dislocations.. The latter buffer layers allow the fabrication of light emitting diodes and laser-diodes on SiC with a completely vertical design.^{6,7} A minimum Al content of 6 % is required for the AlGaN to wet the SiC(0001) surface,⁸ however, recent reports claim the growth of GaN of reasonable quality on SiC(0001) via molecular beam epitaxy,⁹ MOVPE¹⁰ and hydride vapor phase epitaxy (HVPE)¹¹ without a buffer layer.

Films of GaN grown directly on SiC(0001) at 1000°C are usually under tensile strain of -0.1 % at room temperature¹² due primarily the differences in the coefficients of thermal expansion. The use of an AlN buffer layer reduces this tensile stress to the extent that even compressively strained GaN layers on SiC have been reported.^{11,13-17} The compensating compressive stress component is believed to result from the lattice

Table I: Experimental parameters used for the growth of the AlN buffer layer, the AlGaN buffer layer, and the GaN epilayer.

| | AlN buffer | AlGaN buffer | GaN epilayer |
|---|------------|--------------|--------------|
| Growth temperature (°C) | 1110 | 1010 | 1010 |
| V/III ratio | 24400 | 4600 | 1300 |
| Growth rate ($\mu\text{m}/\text{hr}$) | 0.30 | 0.60 | 1.8 |

mismatch of +2.5 % between GaN and AlN. Although the critical thickness, to which GaN layers can be coherently grown on AlN is only a few nanometers, for such a large mismatch¹⁸⁻²¹ a portion of the compressive stress remains beyond this thickness. High-resolution transmission electron microscopy (HRTEM) images have revealed a residual compressive strain of 0.9 % in GaN at the AlN/GaN interface.¹⁶ Moreover, it has been reported²²⁻²⁴ that the average strain in GaN on AlN depends on the GaN layer thickness and usually changes from compression to tension with increasing thickness. However, the opposite trend has also been reported.^{22,25} Finally, the stress in GaN grown on AlGaN buffer layers can be engineered by altering the composition and/or the thickness of this buffer layer.^{8,11,26}

In the present research the evolution of the average strain and the change in strain within GaN layers of different thickness and grown on 6H-SiC(0001) substrates using AlN and AlGaN buffer layers have been determined along the growth direction via high resolution x-ray diffraction (HRXRD) measurements.

2. Experimental Procedures

The as-received, on-axis 6H-SiC(0001) wafers were immersed in an HF:H₂O (1:10) solution for 10 min at room temperature to remove the native oxide, rinsed in de-ionized water and dried in flowing nitrogen prior to loading into the cold-walled vertical pancake-style MOVPE reactor. This system was evacuated to 10^6 Torr prior to growth. Trimethylaluminum (TMA), triethylgallium (TEG) and ammonia were used as the precursor species; hydrogen served as both the carrier and the diluent gas. The reactor pressure was fixed at 20 Torr throughout each growth run. The temperature of the SiC-coated graphite susceptor was measured by a single wavelength optical pyrometer. The main growth conditions are listed in Table I.

The thickness of both the AlN and the AlGaN buffer layers was 100 nm. The Al mole fraction of the AlGaN buffer layer was ~ 0.15, as estimated from HRXRD measurements. The surface morphology of the GaN layers grown on AlGaN buffer layers was very sensitive to the growth temperature and the growth rate of the latter. Growth temperatures and V/III ratios for the AlGaN buffer layer higher than those listed in Table I resulted in spiral hillocks on the GaN surface, as we recently described in detail.²⁷ No growth interruption was performed for the deposition of GaN on the AlGaN

buffer layer; whereas, the growth was suspended for 5 min after the deposition of the AlN buffer layer to readjust the growth temperature. The thickness of the GaN layer was varied between 0.25 nm and 4 μm without any problem of layer cracking. For the GaN layers with thicknesses below 2 nm, the standard growth conditions used for thicker layers had to be changed to achieve a reasonably small growth rate, as shown in Table I. However, AFM images of 2 nm thick layers grown with the two sets of GaN growth conditions did not reveal significant differences. The intended thicknesses of the GaN layers were confirmed by the interference effects observed in HRXRD scans; the numbers given for the thinner layers are nominal values based on the deposition time.

The HRXRD studies were conducted using a Philips X’Pert MRD diffractometer equipped with a fourfold Ge(220) monochromator, a threefold Ge(220) analyzer and an Eulerian cradle. The c - and the a -axis lattice parameters were determined using triple-axis ω - 2θ scans on the (002) and the (205) re-reflections, respectively, in tandem with correction of the Bragg angles for the refraction of the x-rays. AFM was performed using a Digital Nanoscope 30000 in the tapping mode.

3. Results and Discussion

3.1 Results

Figure 1(a) shows triple-axis ω - 2θ scans of the GaN(002) reflection for GaN layers with thicknesses between 20 nm and 4 μm which were grown on AlN buffer layers. All curves show a single dominant peak that shifts to larger Bragg angles when the layer thickness increases. That is, the average lattice parameter, c , decreases with increasing layer thickness. Moreover, all peaks are asymmetric which is particularly obvious for the thicker GaN layers by the shoulder at the low-angle side of the peak. The fact that the peaks become more narrow with increasing layer thickness is simply a consequence of the diffraction within crystals of different spatial extension along the c -axis. The scans of the thinner GaN layers in Figure 1(a) exhibit distinct thickness interference fringes which indicate a relatively smooth GaN surface and a smooth GaN/AlN interface. The thicknesses extracted from the fringe periods fit accurately to the intended GaN layer thicknesses.

The corresponding results for GaN layers grown on AlGaN buffer layers are shown in Figure 1(b). They exhibit features similar to those discussed before. However, for GaN layer thicknesses $\leq 0.1 \mu\text{m}$, a broad background from the AlGaN buffer layer is superimposed on the GaN peak making it difficult to extract the GaN peak position. The broad AlGaN peak points to large strain or compositional variations in the AlGaN buffer layer, the latter of which agrees with the phase separation observed in AlGaN buffer layers by Bremser et al.¹⁵ and Vennégues et al.²⁸ In the following, only the HRXRD data for the GaN samples having a thickness $\geq 0.1 \mu\text{m}$ and grown on the AlGaN buffer layers were evaluated.

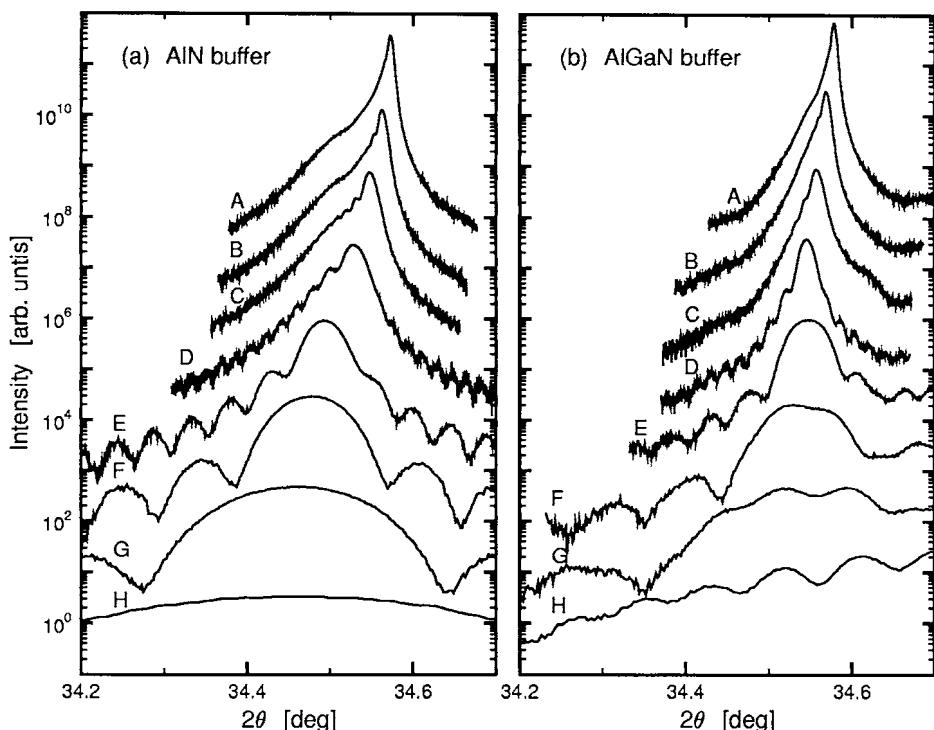


Figure 1. HRXRD triple-axis ω - 2θ scans of the GaN(0002) reflection for GaN layers of different thickness grown on (a) AlN and (b) AlGaN buffer layers, respectively. The GaN layer thicknesses are (A) 4 μm , (B) 2 μm , (C) 1 μm , (D) 0.5 μm , (E) 0.2 μm , (F) 0.1 μm , (G) 0.05 μm and (H) 0.02 μm , respectively. The curves are vertically shifted against each other for clarity.

Figure 2 shows the linear relationship between the average values of the c and the a lattice parameters determined for all GaN samples. Figure 3 shows the evolution of the average lattice parameters with the GaN layer thickness. The plotted strain values were obtained by relating the lattice parameters to the values of c_o and a_o determined for the 4 μm thick GaN layers, as listed in Table II. It should be emphasized that the 4 μm thick layers are not believed to be completely strain-free. Nevertheless, their lattice parameters, rather than published values for nominally unstrained GaN, were used as references to avoid confusion due to possible hydrostatic stresses in our samples. However, among all the samples investigated in this research, the 4 μm thick GaN layers exhibited a c/a ratio closest to the value of 1.626 which is believed to correspond to strain-free GaN.²⁹ The

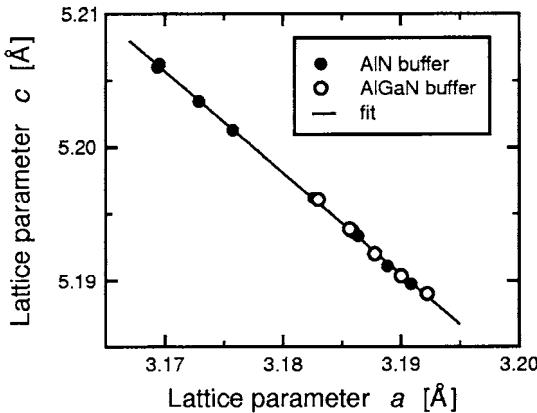


Figure 2. Lattice parameter, c , versus lattice parameter, a , for GaN layers of different thickness grown on AlN buffer layers (filled circles) and AlGaN buffer layers (open circles), respectively. The solid line is the result of a fit of Eq. 3 to the data with $-2c_{13}/c_{33} = -0.468$.

slope of the data in Figure 3 can be fitted assuming that (1) the local strain $\varepsilon(z)$ follows an exponential law and (2) the measured strain $\varepsilon(z)$ with t as the GaN layer thickness, corresponds to the average local strain, i.e.

$$\varepsilon(z) = \varepsilon_0 + \Delta \exp(-z/t_0) \quad (1)$$

$$\begin{aligned} \bar{\varepsilon}(t) &= \frac{1}{t} \int_0^t \varepsilon(z) dz \\ &= \varepsilon_0 + \Delta \varepsilon \left[1 - \exp\left(-\frac{t}{t_0}\right) \right] \frac{t_0}{t} \end{aligned} \quad (2)$$

where $\Delta\varepsilon$ is the total change in strain within an infinitely thick GaN layer and t_0 is a characteristic decay length. For a purely biaxial strain, the in-plane strain ε_{xx} and the out-of-plane strain ε_{zz} should not be independent of each other but satisfy the boundary condition

$$\frac{c - c_0}{c_0} = -2 \frac{c_{13}}{c_{33}} \frac{a - a_0}{a_0} \quad (3)$$

Table II. Measured lattice parameters, a_0 and c_0 for 4 μm thick GaN layers grown on AlN and AlGaN buffer layers, respectively. The numbers given for $-2c_{13}/c_{33}$, t_0 and $\Delta\epsilon_{xx}$ are the results of fitting Eqs. (2) and (3) to the experimental data shown in Figure 3.

| | Buffer layer | |
|--|---------------------|----------------------|
| | AlN | AlGaN |
| a_0 [\AA] for $t = 4 \mu\text{m}$ | 3.1909 ± 0.0008 | 3.1922 ± 0.0008 |
| c_0 [\AA] for $t = 4 \mu\text{m}$ | 5.1898 ± 0.0002 | 5.18900 ± 0.0002 |
| $-2c_{13}/c_{33}$ | | -0.470 ± 0.010 |
| t_0 [μm] | 0.24 ± 0.02 | 0.64 ± 0.10 |
| $\Delta\epsilon_{xx}$ [%] | -0.75 ± 0.05 | -0.34 ± 0.03 |

where c_{13} and c_{33} are elastic stiffness constants. Using Eq. (3) and assuming the strain in very thick GaN layers to be independent of the buffer layer used, the fitting of Eq. (2) to our data results in the solid curves shown in Figure 3. The corresponding fit parameters are listed in Table II.

3.2 Discussion

The stress in the GaN layers can be thought as a superposition of a hydrostatic stress and a biaxial stress in the growth plane. The observed linear dependence in Figure 2 indicates that the samples under investigation only differ in their biaxial stress; whereas, the hydrostatic stress component can be assumed as constant. For this case, the biaxial strain is given by Eq. (3) with c_0 and a_0 as the lattice parameters of GaN under zero biaxial stress. Fitting Eq. (3) to the x-ray data and employing $c_0/a_0 = 1.626^{29}$ resulted in $-2c_{13}/c_{33} = -0.468 \pm 0.004$ which is shown as a solid line in Figure 2. Similar procedures were employed by Perry *et al.*¹⁶ and Lahréche *et al.*¹⁰ who deduced the values -0.446 ± 0.03 and -0.53 , respectively. All these numbers are in reasonable with published values on stiffness constants of GaN for which $-2c_{13}/c_{33}$ is in the range from -0.509 to -0.598^{30-34} . In regard to Figure 3, thin GaN layers are under high in-plane biaxial compression. This results from the fact that GaN first grows coherently on both AlN and AlGaN buffer layers as described above. Beyond a critical layer thickness, this compression is relieved. As Figure 3 shows, the stress relief is not abrupt but the strain decreases steadily over a large thickness range. For very thick layers, the compressive stress due to the buffer layer is fully relieved and the remaining strain only results from defects and the mismatch in the coefficients of thermal expansion between the GaN and the SiC. The asymmetry of the scans shown in Figure 1 further indicates that not only does the average strain change with the thickness, but that there is a strain gradient along the growth direction within each sample. The GaN close to the buffer layer is under stronger compression compared to the GaN close to the surface.

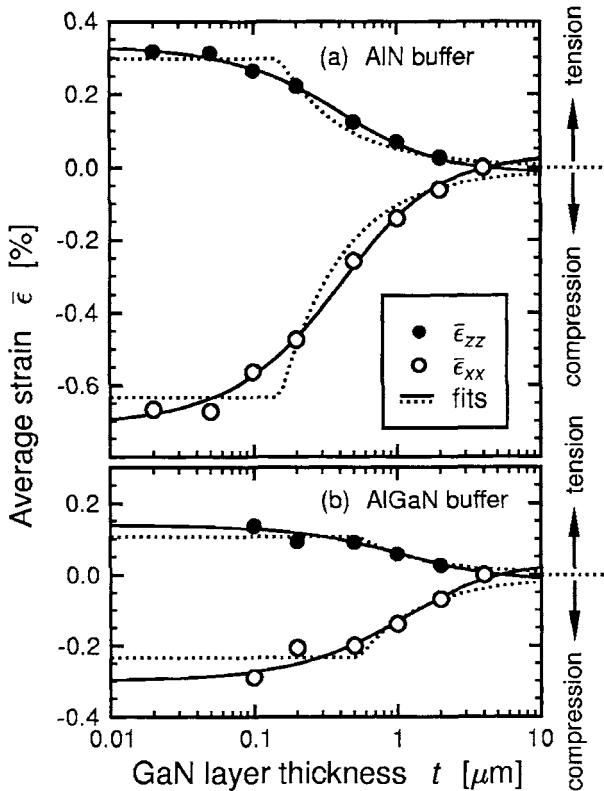


Figure 3. Average in-plane strain (open circles) and out-of-plane strain (filled circles) of GaN layers of different thicknesses grown on AlN buffer layers (a) and AlGaN buffer layers (b), respectively. The strain was set to zero at a thickness of 4 μm. The solid lines were fitted using Eq. (2). The dotted lines correspond to fits of hyperbolic functions similar to those given in Ref 19.

The in-plane lattice mismatches between relaxed GaN and the AlN and AlGaN buffer layers are about 2.5 % and 0.37 %, respectively. In contrast, the fit parameters $\Delta\epsilon_{xx}$ in Table II show that the strain, which relaxed within the thickness range accessible to HRXRD, is only about 0.75 % and 0.34 %, respectively. Therefore, if it is assumed that the GaN initially grows coherently on both AlN and AlGaN, only the data in Figure 3 corresponding to the growth on AlGaN cover the total relaxation process. It is suggested that the stress relief of GaN grown on AlN and AlGaN is a single and two-step process, respectively.

(i) The coherent stress of GaN on the AlN buffer layer is partially relieved within the first 20 nm of GaN growth. This thickness range includes the reported critical thickness values for the coherent growth of GaN on AlN, namely 3.0 nm from theoretical calculations,¹⁸ 2.9 ± 0.4 nm from the extrapolation of XRD data,¹⁹ and both the 0.5 nm

and the 3.1 ± 0.2 nm determined from *in-situ* lattice parameter measurements at different growth temperatures.^{20,21} The former numbers correspond to the plastic stress relief by misfit dislocations which, however, can be superimposed by an elastic relaxation of GaN islands via their sidewalls before coalescence occurs.³⁵ About 70 % of the coherent strain of GaN on AlN is relieved in the first step; this agrees well with the value of 64 % deduced by Perry *et al.*¹⁶ from HRTEM images.

(ii) The stress remaining in GaN on AlN after the first step is relieved in a second step, as illustrated by Figure 3. This stress relief extends over a large depth range in the GaN layer, as the decay length, t_0 , in Table II of about 0.24 μm indicates. The same effect was determined to be true for the total strain of GaN on AlGaN where the value of the decay length is even 0.64 μm . The long-range relaxation may result from the difficulty of threading dislocations in the group III-nitrides, most of which run along the *c*-axis, to bend over and glide in the *c*-plane.³⁶ A qualitative model for the long-range strain relaxation can be developed using the evolution of the film microstructure. The film becomes increasingly smoother, i.e. the undulations and pits become filled with material with increasing layer thickness. Therefore, the elastic relaxation of the film via the lateral deformation of the undulated structure is suppressed and plastic relaxation by dislocations begins to occur. It is assumed that the generation of misfit dislocations is promoted at the deepest regions of the pits and the undulations. A similar phenomenon has been shown for coherent AlGaN and InGaN layers in which the tips of cracks and V-shaped defects act as nucleation sites for dislocations.^{36,37} As the deepest regions of the pits and undulations rise, the generated misfit dislocations are distributed over different depths in the layer, and the strain becomes nonhomogeneous along the growth direction. The latter effect is responsible for the asymmetry of the HRXRD scans shown in Figure 1.

The use of the exponential function given in Eq. (2) to fit the data in Figure 3 represents an empirical approach, as it was not motivated by a certain model for the relaxation process. Interestingly, Hiramatsu *et al.*³⁸ used a similar dependence to describe the strain relaxation of thick GaN layers grown on AlN/sapphire. These investigators proposed the formation of microcracks at the sapphire interface to hold the thermally induced stress in the bent heterostructure below a critical value. The layers investigated in the present study, however, are assumed to be too thin to cause cracking. Kim *et al.*¹⁹ fitted hyperbolic thickness dependence, $\varepsilon_{xx} \propto 1/t$, to strain values obtained for GaN layers on AlN/sapphire beyond the critical thickness which was motivated by a model that balanced the energies for strain and dislocations. The same approach was used by Dunstan³⁹ who recently reviewed the strain relaxation in semiconductors with the focus on InGaAs layers on GaAs where the relaxation is assumed to result from dislocation multiplication. The fits of hyperbolic functions to our data are shown as dotted lines in Figure 3. The experimental results are better described by the exponential functions than by the hyperbolic functions.

It is generally known that thick GaN layers grown on SiC(0001) tend to crack beyond a critical layer thickness due to the build-up of a high tensile stress⁴⁰⁻⁴². However, the strain data of this study has shown that GaN layers grown on SiC(0001) are in

average under compression in the growth plane when either an AlN or an AlGaN buffer layer is employed. The compression is a consequence of the large lattice mismatch between GaN and the buffer layer that amounts to 2.5 % and 0.37 % for the AlN and AlGaN buffer layer, respectively. In comparison, the tensile strain at room temperature resulting from the mismatch in the coefficients of thermal expansion between the GaN and the SiC is only -0.1 % for typical MOVPE growth temperatures¹². Although the average strain in the GaN layers is compressive, the strain at the GaN surface can be tensile which gives rise to the formation of cracks. The evaluation of Eq. (1) using the fit parameters in Table II reveals that the GaN surface turns from compression into tension at a layer thickness of 0.7 μm and 1.4 μm for the AlN and the AlGaN buffer layer, respectively. Moreover, from growth experiments on AlGaN buffer layers it was found that the stress in GaN can, e.g., depend on the buffer layer thickness^{8,11}. Therefore, the problem of cracking in thick GaN layers on SiC can be minimized by optimizing the composition and the thickness of the buffer layer of choice towards a maximum compressive stress remaining at a certain GaN layer thickness.

4. Summary

The thickness of the GaN layer influences the biaxial strain in the layers. GaN layers grown on either AlN or AlGaN buffer layers were determined to be under compression in the growth plane due to incomplete relaxation of the coherent strain. With increasing thickness, this stress is progressively relieved. Approximately 70 % of the coherent strain remained after a first relaxation step in a 20 nm thick GaN layer on AlN. Relief of the remaining stress followed an exponential dependence over a large range of GaN layer thickness. Values of 0.24 μm and 0.64 μm were determined for the characteristic lengths of this relief for the growth on AlN and AlGaN, respectively. The misfit dislocations associated with the relaxation are assumed to be formed at the bottom of the surface undulations. As the latter fill with material during growth, the misfit dislocations are distributed throughout the GaN layer such that the strain within each layer becomes inhomogeneous, i.e., the GaN closer to the buffer layer is under higher compression than the GaN at the surface.

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GROWTH OF THICK GaN FILMS AND SEEDS FOR BULK CRYSTAL GROWTH

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The essential steps required to create thick GaN films and seed crystals for bulk crystal growth are described. These include the growth of low dislocation density GaN films by hydride vapor phase epitaxy and the separation of films from their growth substrates. Also addressed are issues of processing thin and thick films to create compliant layer substrates for thick film HVPE growth and chemical mechanical polishing methods to enhance surface morphology and remove material damage free. Growth of both gallium and nitrogen polar films is discussed with key issues identified regarding polarity inversion during growth and impurity incorporation along the -c growth direction. These are illustrated with examples that emphasize the growth of material with low threading dislocation density.

Keywords: GaN; crystal growth; seeds.

1. Introduction

Historically, one of the key steps in transitioning semiconductors from the research laboratory to the manufacture of functional devices, is the development of methods for reducing the density of threading dislocations. Whilst there are some specialized semiconductor materials and devices that can be fabricated from hetero-epitaxial materials, the yield is typically low, the reliability poor and the device variability high. This has proven to be acceptable in the manufacture of high-value added products where there is no competing product especially in the early stages of the establishment of a new materials-based technology. However, in the longer term, reduction in the density of threading dislocations has to be achieved before large scale manufacture becomes viable.

Despite some initial claims to the contrary, the presence of threading dislocations is as undesirable in GaN as in all other semiconductors since these can act as short-circuit leakage paths, especially when they penetrate through junction regions, and also serve as carrier recombination centers. The growth of thick GaN films provides one route to reducing the threading dislocation density. In fact, there are two principal motivations for growing thick GaN films. One is to decrease the density of threading dislocations since studies have shown that the dislocation density of

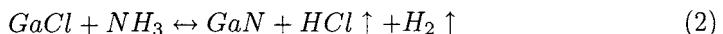
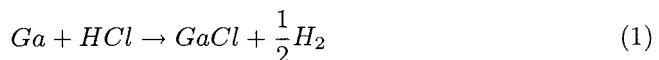
GaN films grown hetero-epitaxially decreases with thickness, h , as $1/h^n$ ($n>1$) so by growing a very thick film it can then be used as a “substrate” for subsequent device fabrication.¹ The other is to create sufficiently large pieces that can be used as “seeds” in subsequent growth of bulk single-crystals. Nominally, the growth of thick GaN films is straightforward but is limited, in practice, by cracking as described in a companion contribution.²

In this contribution we describe different approaches to the growth of thick GaN films for use as “seeds”. This requires accomplishing three essential steps. One is to grow thick films whilst also avoiding cracking. The second is the separation of the films from the substrate so as to produce “free-standing” GaN crystal films. The third is preparation of the surfaces so that subsequent growth on the crystal faces can occur in order to form a bulk single crystal without introducing more dislocations. The work described here concerns GaN films on sapphire substrates but similar considerations pertain in the growth of GaN seeds on SiC or Si substrates.

2. Hydride Vapor Phase Epitaxy

Hydride vapor phase epitaxy is well suited to the growth of thick films since growth rates of tens to hundreds of microns an hour can be readily achieved, depending on the design of the growth reactor and the gas flow. These growth rates are much higher than is possible by either MOCVD or MBE methods currently employed in making GaN films and devices.

The original demonstrations of HVPE growth of GaN date back to 1969.³ The method is comparable to earlier VPE growth of GaAs, GaP, and GaSb, in which hydrogen chloride gas is passed over a molten bath of Ga and reacts with a group V hydride (NH_3) over a hot substrate to deposit a film. The basic reaction can be expressed as:



The chemical reactions occurring during GaN growth have been studied by a number of authors even so, the intermediary species and the reactions taking place on the growing film surface all remain to be clarified so the above reaction is merely a short-hand representation of the actual reactions involved.^{4,5} Undoubtedly, several concurrent and competing reactions occur since the various diluents and carrier gases used to control the reaction rates and the surface morphology of the deposited films all have a profound effect on both the growth kinetics and crystal quality. Whilst the actual growth conditions are rather specific to different reactor designs, the highest quality films are grown at substrate temperatures in the range of 1050–1100°C.

As with MOCVD and MBE methods of growing GaN films, the preparation of the substrate surface and the actual growth conditions greatly affect the attainable film quality and the threading dislocation density in HVPE films. We have adopted two different approaches to reducing the threading dislocation density. One is the use of an intermediate temperature nucleation step followed by high-temperature growth, all within the same reactor. The second is a high-temperature growth procedure that can also lead to high quality films.

Two-step nucleation of HVPE GaN can be implemented within a single chamber by properly controlling the nucleation step, the annealing stage, and the subsequent re-nucleation and growth at high temperature.⁶ Our work has been carried out in a horizontal, three-zone, hot-wall HVPE reactor of our own design that operates at atmospheric pressure. Key features of the design are that the substrate is held vertically on the end of a rotating shaft mounted on a bellows arrangement so that the substrate can be rapidly introduced and withdrawn from the hot-zone of the reactor. This enables us to place the substrate into the reaction zone at low temperature for the nucleation step then withdraw the substrate as the temperature of the reaction zone is increased to the growth temperature and the substrate re-inserted into the reaction zone. This arrangement also allows the substrate to be rapidly withdrawn from the reaction zone so that the microstructure and crystallography of the film can be examined at different temperatures and at different stages in the nucleation and growth process.

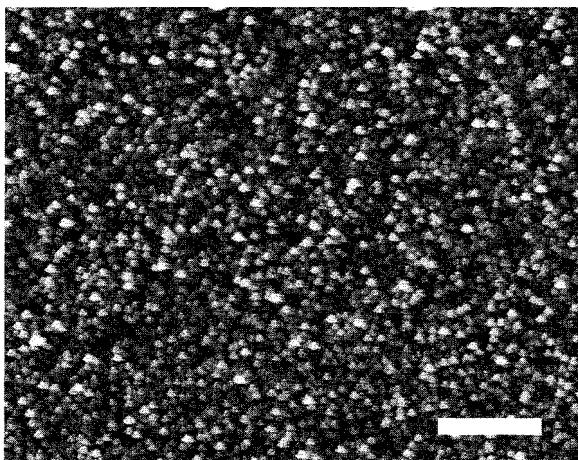


Fig. 1. AFM image of a low temperature nucleation layer grown by HVPE at 550°C. The scale bar indicates 1 μm , the Z-range of the image is 20 nm.

The structure of the film at the nucleation stage is shown in the atomic force micrograph (AFM) of figure 1. The AFM image reveals that the film consists of a high density of nuclei. On heating these evolve to form c-axis oriented grains that grow and coalesce to form a continuous film during growth at 1050°C. In this

respect, the microstructural evolution is similar to that reported for the growth of GaN films by MOCVD using a low-temperature nucleation step.⁷ For HVPE growth using nucleation layers, once this buffer layer is grown, the substrate is withdrawn from the hot zone and the reactor is heated to growth temperature. Prior to high temperature growth, the substrate is reinserted in ammonia and the growth is commenced. Figure 2 shows a typical growth schedule using a low temperature nucleation layer grown at 550°C and a high temperature growth at 1100°C. This process is in contrast to a direct high temperature nucleation scheme that is also used in the growth of HVPE GaN on sapphire. In this approach, a sapphire substrate is inserted at high temperature in the presence of ammonia for approximately seven minutes. Growth commences after this ammonia pretreatment with no additional nucleation schemes.

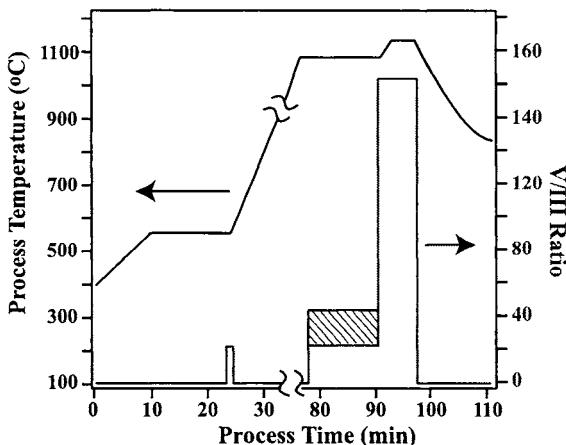


Fig. 2. Process timeline for HVPE growth with a low temperature nucleation layer

3. Laser-Assisted Debonding and Lift-Off

A key step in creating free-standing “seed” crystals is the innovative method, first described by Kelly *et al.*⁷, of using a laser to debond, and separate, epitaxial GaN films from the sapphire substrates on which they are grown. The basis of the method is the use of a laser wavelength that is heavily absorbed in the GaN but to which the sapphire substrate is essentially transparent. When the laser is shone on the substrate’s backside, it passes through the sapphire and the photons are then absorbed within a few absorption depths of the GaN/sapphire interface converting the laser energy into heat. Under favorable conditions, the absorbed energy drives the reaction



from left to right leading to the formation of a gallium-rich interface and the evolution of nitrogen gas.

In practice, the absorbed laser energy can also lead to other, less desirable phenomena such as cracking of the film and substrate, especially when the energy density is too large. However, sufficient energy must also be supplied in order to fully convert the interfacial region to a continuous layer of gallium. Analysis of the competing phenomena and their scaling with laser energy and beam diameter, has led to the identification of combinations of process parameters over which laser-assisted debonding can be achieved with minimum damage to the film.⁸ These conditions can be summarized in the process maps reproduced in figure 3. Fracture and damage during debonding are dependent on the duration of the laser pulse (τ_p), the beam energy (E_p), as well as the diameter of the laser beam (d_p). These maps indicate that there is only a narrow window of process parameters to avoid film cracking.

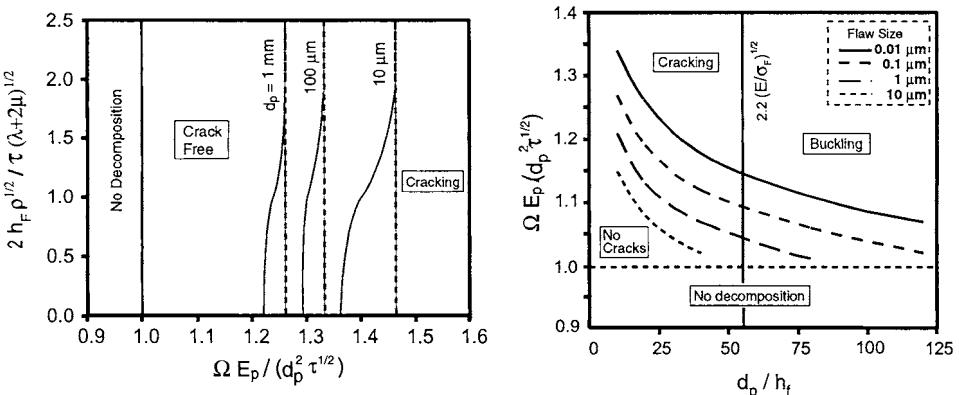


Fig. 3. Process maps delineating regions of damage free laser debonding of GaN films from sapphire.

An important pre-requisite for successful debonding is that the wafers selected as original growth substrates are polished as surface roughness can scatter the laser light. A slight roughening of the back-side can be advantageous by homogenizing the laser beam, but substantial roughness in the form of cracking can cause appreciable optical scattering and prevent successful laser-assisted debonding. An additional difficulty is encountered with thick films. Invariably, unless there is a compliant interface, the thermal expansion mismatch between the GaN film and the substrate causes the film and substrate to bend. This curvature and corresponding state of stress make it difficult to debond small portions of the interface which contributes to cracking in the GaN film upon its release from the substrate.

Despite these difficulties, it is possible by careful control to lift-off complete, intact films from sapphire wafers. The largest we have attempted have been the 2"

diameter films we grow but there is no reason to suppose that still larger diameter films cannot also be separated in this way. We have also shown that GaN films on which devices have been grown by MOCVD can also be separated from sapphire substrates.

4. Generation of a Compliant Interface

The difficulties in growing crack-free thick GaN films have motivated a number of exploratory approaches to avoiding cracking. One approach we have been exploring is to create a “compliant interface” between the film and the sapphire substrate once a continuous film has been formed but before the film thickness reaches the critical thickness for cracking. The process is shown schematically in figure 4. The compliant interface is created by laser-assisted debonding and, according to the chemical reaction above, ideally leads to the formation of a thin gallium layer between the sapphire substrate and the GaN. Since gallium is a liquid down to 30°C, the gallium layer should be effective as a compliant layer down to that temperature. The attraction of the “compliant interface” is that stresses associated with growth as well as those generated by thermal expansion mismatch on cooling can be relaxed by interface sliding on the molten gallium layer. Ideally, the compliant interface would be created at the growth temperature itself so that the growth would not need to be interrupted. Our present facilities do not have these capabilities and so we have had to cool down to debond the film.

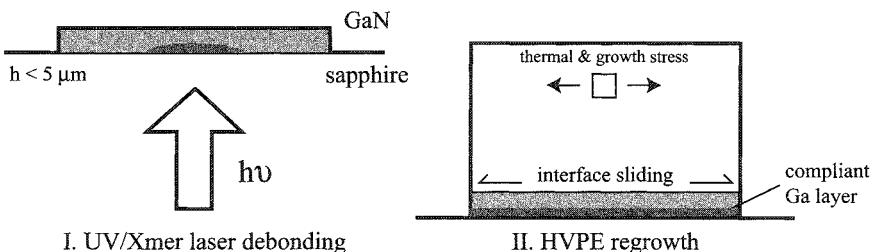


Fig. 4. Process schematic for compliant substrate laser debonding.

As mentioned above only a narrow process window exists since the objective is to convert a thin layer of GaN to Ga metal without either separating the GaN from the substrate or producing damage, including cracks, from an excessive laser intensity. In addition, the raster pattern has to enable the gas produced by the laser-induced reaction to leave the interface and escape from the sample. In seeking the optimum conditions to create a compliant interface, we have carried out an intensive series of experiments. The results of one are shown in figure 5, in which half of a 5 μm GaN template was uniformly debonded. Although a further 200 μm of GaN was grown on this sample, examination of the sample following growth indicated

that large areas of the debonded film had delaminated off the substrate after only 30 μm had been deposited. These 30 μm thick freestanding films were, however, crack-free, demonstrating that the compliant interface was successful in enabling the growth of films above the normal critical thickness for cracking. Investigations of debonding geometries to maintain film integrity throughout growth while still allowing sufficient interface compliance are currently underway.

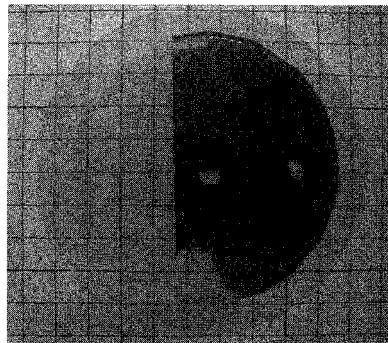


Fig. 5. 5 μm thick GaN template with right half of wafer laser debonded to produce a compliant substrate and the left side unprocessed. The dark color is dissociated gallium at the interface, and the observed buckling is a result of the room temperature compressive stress acting on the now compliant interface. Graph paper with a 0.2" scale is shown for reference.

5. Polarization Inversion During Growth

At this early stage in the development of methods of growing bulk GaN crystals from seeds, it is not known whether the polarity of the seed growth surface is important in forming crystals with the lowest dislocation densities. If it is, then the ability to change the polarity of the GaN film during growth so as to produce a film with the same polarity on opposing basal plane surfaces may be desirable. Some progress towards this objective has recently been made using Mg-doping.

GaN films deposited by HVPE, MOCVD and MBE on sapphire, SiC and Si substrates all grow with their Ga-face up corresponding to the growth direction being [0001], the positive c-axis direction. (In the wurtzite crystal structure, the positive c-axis direction is, by definition, parallel to the vector pointing from the cation to the anion). This growth direction and polarity have been confirmed in several different ways, the most direct being convergent beam electron diffraction (CBED). The exception to this growth polarity is the growth of heavily Mg-doped GaN by MBE or MOCVD, where the negative c-axis direction (N-face growth) has been reported.⁹ While there have been first principle studies of the mechanism by which Mg can alter the stacking sequence along the c-axis, it is still not entirely clear why Mg can cause inversion under certain growth conditions.⁹

Nevertheless, reasoning that the presence of Mg alters the growth polarity, Mg-doped films have been grown by MBE and MOCVD on lightly Si doped Ga polar MOCVD templates. Analysis of the resulting films by electron microscopy and CBED reveals that polarity inversion was achieved and an example is illustrated in the micrograph shown in figure 6. The position of the inversion boundary is delineated by the horizontal contrast change in the micrograph. CBED patterns taken on either side of the inversion boundary indicate the reversal in c-axis direction, a conclusion substantiated by the matching of the patterns of light and dark fringes in the simulated CBED patterns. The matching systematic row of CBED diffraction disks and their simulations (the full zone axis CBED patterns were used for the polarity determination, rather than just the center row) are superimposed on the micrograph. The CBED patterns indicate that both the top and bottom of the film have the same N-face polarity. Interestingly in this example, the threading dislocations are continuous across the inversion boundary hence the dislocation structure does not appear to be modified by the change in stacking sequence. This is not true under all conditions, however, and growth parameters have been shown to have a significant influence on the overall quality of inverted layers.¹⁰

6. Demonstration of Regrowth On Nitrogen Polar GaN

A key consideration in using GaN films as “seeds” for subsequent bulk single crystal growth is the ability to nucleate and grow on the two polar surfaces of the films. Regrowth on the Ga-face has routinely been demonstrated in the fabrication of device structures by both MOCVD and MBE and typically involves some deliberate or fortuitous *in-situ* “etching” of the growth surface in the reactor as the regrowth conditions are established. More problematic are the conditions for the regrowth on the N-face, especially after exposure to the atmosphere, and the control of the dislocation density in the film subsequently grown on the exposed surface. Investigations of inverted N-face GaN films grown by MOCVD reveal that the most common surface morphological faults are the formation of hillocks and hexagonal platelets. Surfaces of heavily Mg doped GaN films are marked by the formation of 30-50 micron wide hexagonal half-platelets which point towards the [10 $\bar{1}$ 0] direction of the GaN. Regrowth of Si doped GaN on these inverted layers results in formation of numerous flat-topped and pointed hillocks. The density of which is ultimately controlled by several factors including the inversion layer thickness and exposure of any interfaces to atmosphere. Figure 7 details the growth morphologies obtained after MOCVD growth of Mg and Si doped N-face GaN.

In addition to the large scale hexagonal surface features that are found after growth, atomic force microscopy reveals much about the growth mode of these layers. Similar to earlier reports by Weyher and coworkers, evidence of step flow growth is seen on the small scale as well as severe pitting on the nanoscale.¹¹ The steps on the surface also show evidence of faceting which is in contrast to Ga face GaN growth on which faceting is generally not observed. Figure 8 shows an AFM

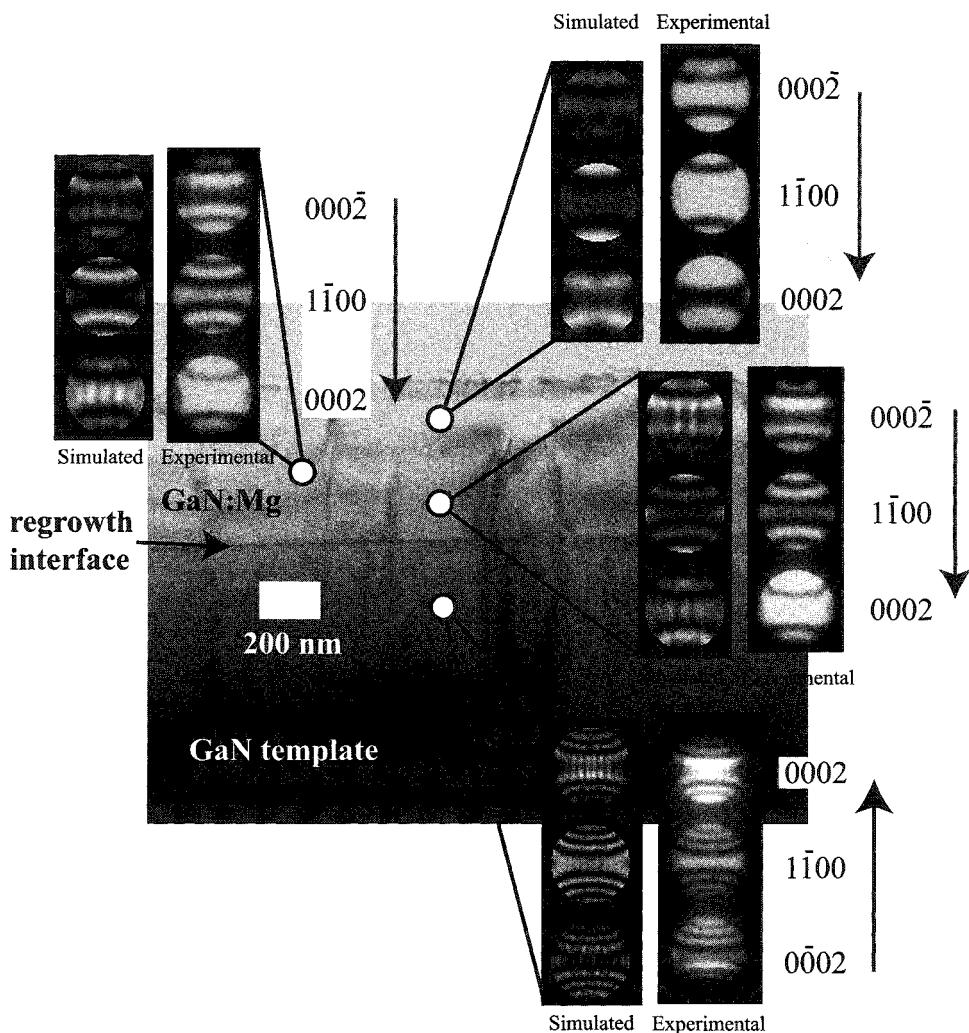


Fig. 6. MBE regrown GaN:Mg layer on a standard MOCVD GaN template. CBED information from both the base layer and the inverted layer indicate the polarity of the growth was switched from Ga-polar to N-polar.

image of the surface of an N-face polar sample.

One feature of -c direction growth appears to be a slightly higher incorporation of impurities compared with +c direction growth. SIMS analysis, for instance, reveals that incorporation of oxygen was found to be $1 \times 10^{17} \text{ cm}^3$, compared with $3.5 \times 10^{16} \text{ cm}^3$ along the +c axis, carbon was found to incorporate at $3 \times 10^{16} \text{ cm}^3$ versus $1 \times 10^{16} \text{ cm}^3$, and silicon doping was found to be suppressed incorporating at $1.4 \times 10^{17} \text{ cm}^3$ compared with $3.2 \times 10^{17} \text{ cm}^3$ for comparable disilane flows and growth rates.

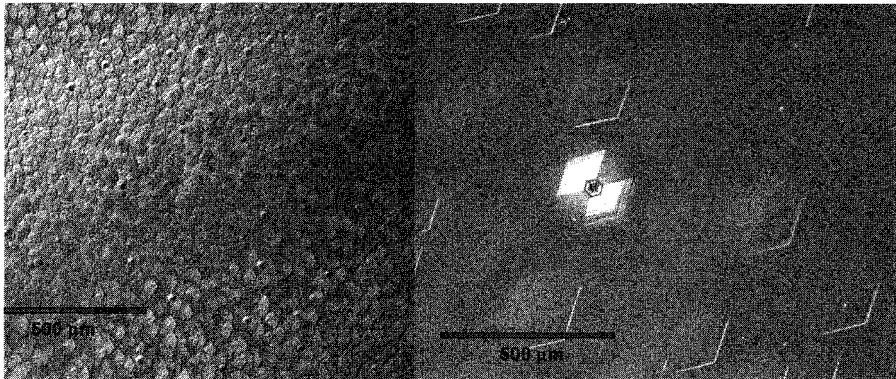


Fig. 7. Optical micrographs taken under Nomarski polarization of inverted GaN:Mg (left) and GaN:Si (right) layers.

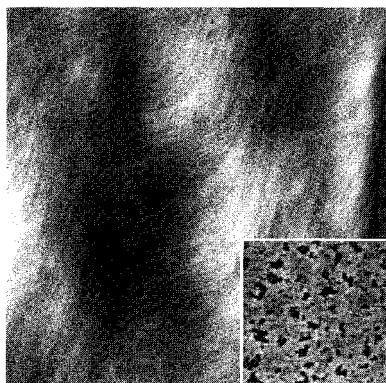


Fig. 8. A $25 \mu\text{m}^2$ AFM image of GaN:Mg layer. The inset shows a close up of the surface morphology including the fine-scale pitting observed on N-polar material after growth.

7. Chemo-Mechanical Polishing

The ability to polish a film or bulk crystal is an essential step in almost all optical materials and semiconductor device processing. The use of thick films as possible “seeds” may also require that the surfaces be polished. One reason is to shape the edges of the film to conform to specific crystallographic directions on which growth is favorable. Another is to remove material from the GaN film that had been in contact with the substrate since this portion of the film generally has lower quality. For instance, the dislocation density decreases with increasing film thickness, the dislocation density is highest in the region of the film near the substrate. In addition, inter-diffusion between the substrate and the film occurs during growth and so the region of the film near the substrate invariably contains a much higher concentration of O and Al than near the top surface.

It has been reported that KOH can be used to polish GaN but in our experience

this has not been effective or practical.¹² Alternatively colloidal silica can be used as a chemical-mechanical polishing agent under conditions more basic than those typically used to polish alumina or silicon.¹³ Our studies have revealed silica to be an extremely effective polishing agent on the nitrogen face of GaN, establishing both a damage free method of material removal, and a means of identifying nitrogen polar surfaces because of its high selectivity for this polarity surface.

In our work, the chemical mechanical polishing of nitrogen polar GaN surfaces was studied by investigating the polishing rate over a range of pH values and colloidal silica particle sizes. Removal rates as high as $1.1 \mu\text{m}/\text{hr}$ were obtained on nitrogen polar surfaces, no polishing action was observed on gallium polar surfaces. Each sample was also investigated using atomic force microscopy in order to quantify surface roughness, and overall effectiveness of the surface treatment. Figure 9 reveals the surface morphology resulting from a 10 minute polish on a N-face GaN layer grown by MBE. Overall roughness on a $400 \mu\text{m}^2$ area was found to be as low as 1.8 nm RMS, while on smaller $25 \mu\text{m}^2$ regions, the roughness dropped to 0.4 nm RMS. Since no polishing action is observed without colloidal silica and the sample is also not etched in a solution of silica, the polishing action is both chemical and mechanical in nature. This is also supported by the observation of a change in the polishing rate as a function of pH.

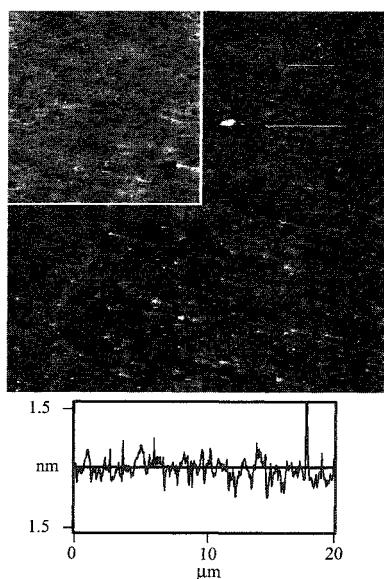


Fig. 9. $400 \mu\text{m}^2$ AFM image of a chem-mechanically polished GaN:Mg film with a corresponding cross-section shown below. The inset shows a $25 \mu\text{m}^2$ close up of the surface. The white dots are believed to be silica particles not removed by cleaning.

8. Summary

Several groups around the world have now demonstrated that large area single crystal GaN films can be grown by HVPE on sapphire and on SiC. One of the significant drawbacks, however, is that the films are frequently cracked when the thickness exceeds 10-20 microns. As the GaN growth community gains more experience, it will undoubtedly be possible to learn how cracking and its effects can be advantageously controlled for stress relief. Nevertheless, it can be expected that several of the processes, such as chem-mechanical polishing and laser-assisted debonding, as well as the optimum regrowth conditions developed in the course of the MURI program at UCSB, will be of continuing value in future GaN technology.

Acknowledgments

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CRACKING OF GaN FILMS

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The cracking of GaN films and the associated cracking of substrates are described. The geometry, structure, and evolution of fracture demonstrate that GaN films crack under tensile stress during growth and are subsequently overgrown and partially healed. The film cracks channel along the $(1010)_{\text{GaN}}$ planes and also extend a distance of $\sim 5 \mu\text{m}$ into the sapphire substrate. These incipient cracks in the substrate form a set of initial flaws that leads to complete fracture through the sapphire during cooling for sufficiently thick films. Each stage of this cracking behavior is well described by a fracture mechanics model that delineates a series of critical thicknesses for the onset of cracking that are functions of the film and substrate stresses, thicknesses, and elastic properties. Similar cracking behavior is found to occur independently of the choice of substrate between sapphire and SiC and is traced to a tensile stress generation mechanism early in the growth process, such as that provided by island coalescence. Cracking is the dominant stress relief mechanism, as opposed to dislocation generation or diffusion, because of the island growth mode and because of optimized growth temperatures at or below the brittle-to-ductile transition. Lateral epitaxial overgrowth (LEO) of GaN is shown to minimize substrate fracture even though film cracking remains unaffected. This effect explained in terms of the limits placed on the initial extent of insipient substrate cracks due to the LEO geometry.

Keywords: Strain; cracking; GaN.

1. Introduction

One of the practical problems experienced since the earliest days of the growth of GaN films, as well as GaN alloy films, is that the films have a propensity to crack.¹ In many cases, the cracking is so severe that the film and substrate fracture into separate pieces. In the last few years, it has been discovered that cracking can generally be avoided if the film thickness is less than a critical value but there are many device applications where films thicker than this critical thickness are desirable. Also, as the threading dislocation density in films

generally decreases approximately as the reciprocal of the film thickness, there are benefits to growing thicker GaN films and then fabricating device structures on top.² The occurrence of cracking raises a number of intriguing questions: Why does cracking occur during the growth of GaN? Why does GaN cracking occur irrespective of the nature of the substrate material? Why does GaN crack during growth whereas other semiconductors do not? Why does the substrate crack? And, of course, how can cracking be avoided?

In this contribution, we address each of these questions and provide a rational framework to identify the conditions under which cracking can be avoided. Although all cracking is undesirable, a distinction is made between cracking during film growth and cracking during subsequent cooling to room temperature. The distinction is important since different cracking mechanisms pertain during growth and during cooling and so different strategies apply in order to avoid film and substrate cracking.

2. Observations of Cracking

When the growth of thick GaN films is attempted, they frequently crack and in particularly severe cases the cracking has the appearance illustrated in figure 1. The cracks shown in the figure have a number of notable features: (a) The cracks

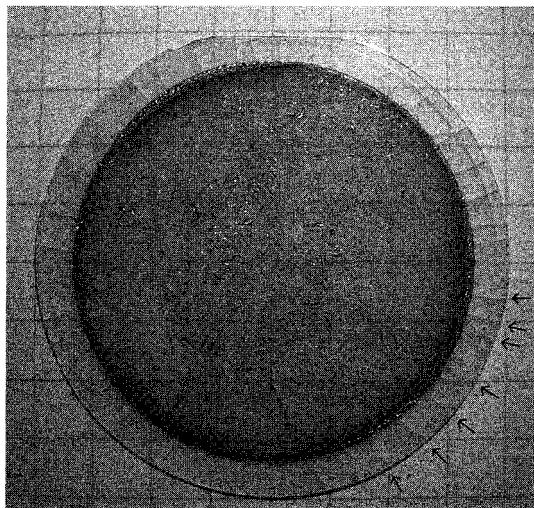


Figure 1. GaN film grown on a 2" diameter sapphire substrate, photographed on graph paper. The hexagonal symmetry of the tensile cracks can be seen in the film, as can be the extension of substrate cracks from under the film to the substrate edge (indicated by the arrows). The film thickness is 122 μm and the substrate thickness is 430 μm .

in the GaN film are principally aligned along crystallographic planes in the GaN and have a superficial similarity to ‘mud-cracking’; (b) Where cracks intersect both each other and the film surface, the film has a tendency to lift away from the substrate; (c) The spacing of the cracks in the film are typically of the order of tens to hundreds of microns. The other cracks visible in figure 1 are cracks in the sapphire and these are most clearly distinguished around the periphery of the sapphire substrate where no GaN film has been deposited.

One of the most intriguing, and often misleading, observations is that the cracks in the GaN are not always visible on the film surface, especially on thicker

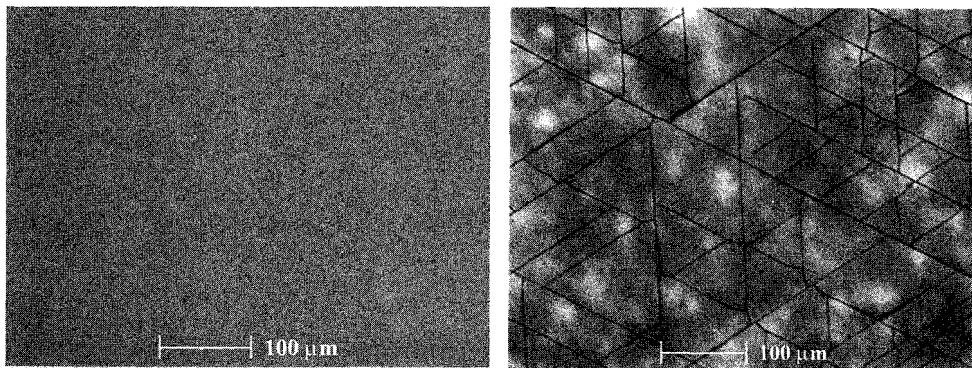


Figure 2. Optical microscopy of GaN/sapphire under different illumination conditions. The left micrograph is taken in reflected light, and illustrates the smooth, specular morphology of the film. In contrast, the right micrograph is taken in transmitted light and clearly shows the presence of channel cracks in the film that are not visible on the surface.



Figure 3. Cracking in a 180-μm thick GaN film. The geometry of cracking in GaN is clearly visible with the optical focal plane deep in the film; however, as shown in the overlaid inset in the lower right-hand corner, these cracks can no longer be seen when focused on the film surface.

films, and then can only be revealed in transmitted light. Thus, the appearance of an uncracked surface is not an indication, as many have claimed, of an uncracked film. This property of GaN cracking is demonstrated in figures 2 and 3. A second, equally intriguing observation is that cracking does not occur if the film thickness is less than a critical value, typically ranging from 4 to 8 μm . Fortunately, many device structures can be fabricated on GaN films less than this critical thickness, but in attempts to grow thicker films for other device structures or for bulk single crystal growth, cracking presently poses an almost insurmountable problem.

Insight into the film and substrate cracking comes from microstructural characterization of cross-sections, particularly those created by cleavage, of the type shown in figure 4. These reveal three features crucial to understanding the cracking processes and sequences. The first is that the cracks in thin films above the critical thickness extend all the way through the film whereas those in thicker films approach the film/substrate interface but generally do not approach the surface. Indeed, those that terminate within the film are typically not sharp as cracks normally are but rather have a blunted shape at their tip. Secondly, the cracks in the GaN are seen to extend a short distance, typically only 2 to 7 μm , into the substrate. There they bend presumably to adopt an orientation closer to a favorable cleavage plane in the sapphire. (The primary cleavage planes of GaN and sapphire are crystallographically the same, but as the crystal structure of the

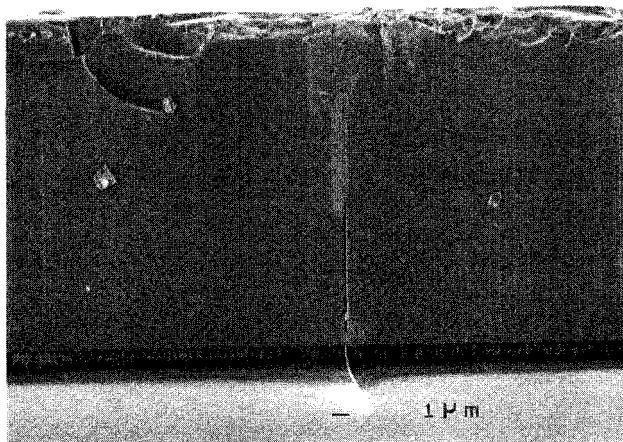


Figure 4. Cross-sectional SEM micrograph of a GaN film on a sapphire substrate. The profile of a typical channel crack illustrates two important features of their geometry: the crack does not propagate up to the film surface, and a small insipient crack has formed in the sapphire as a continuation of the crack in the film.

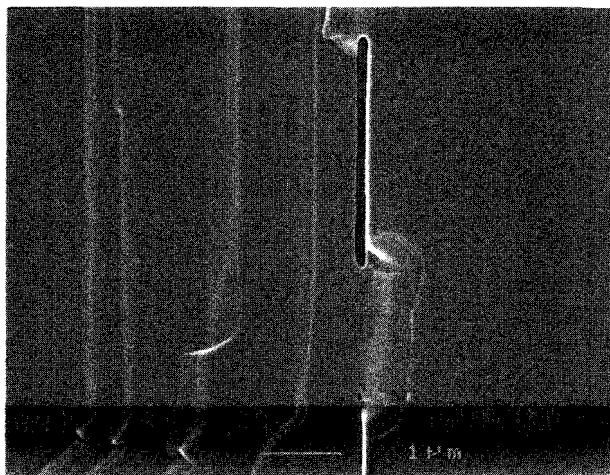


Figure 5. Cross-sectional SEM micrograph of a channel crack showing evidence of healing. The crack tips are significantly rounded, and the crack has closed and healed in the region immediately above the interface. The incipient crack in the sapphire, however, has not healed and remains sharp and narrow in profile.

GaN is rotated by 30° about the common c-axis with respect to the sapphire crystal structure, cracks along the cleavage planes in GaN cannot propagate directly into the sapphire without bending and twisting). The third important feature is that there is evidence for healing of the cracks, as evidenced by the rounded profile of the crack tips, illustrated in figure 5, and by the occasional pinching off and rounding of cracks along their depth.

The observed cracking behavior can be summarized as follows. Below a critical thickness, no cracking of either the film or the substrate occurs. This thickness is approximately 5 μm but varies somewhat depending on the type of substrate and the type of buffer layers or nucleation layers used in growth of the film. Above the critical thickness, the film "mud-cracks" and the cracks extend a short distance into the substrate. Films just above the critical thickness can be cooled down with little or no cracking of the substrate although the films themselves are cracked. On cooling thicker films, the substrate cracks as well, as shown in figure 1. Most significantly, some sapphire substrates do not crack on cooling or immediately after cooling but then spontaneously crack after exposure to air minutes to hours later.

In the case of GaN grown on silicon carbide, a similar crack geometry is observed in transmitted light, as seen in figure 6. Here, the presence of crystallographically faceted pits along the cracks indicates that cracking has

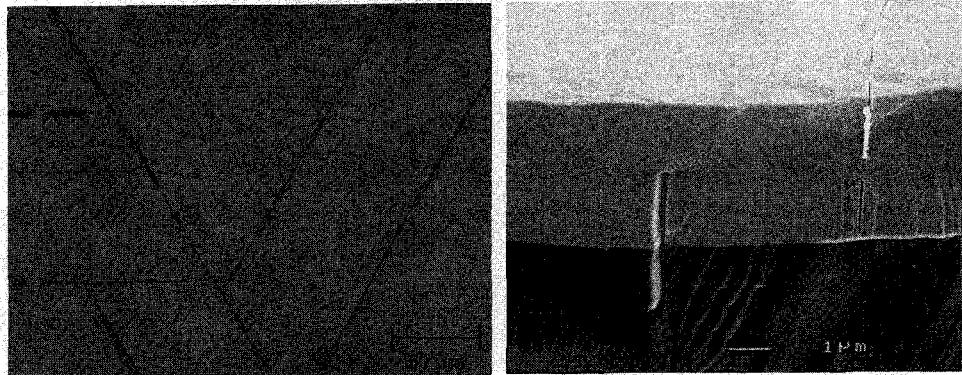


Figure 6. Crack geometry in GaN/SiC. Transmission optical microscopy reveals the crystallographic orientation of cracks in the film and the alignment of extended surface pits on cracks. Cross-sectional SEM shows the presence of two crack regimes within the same film: one that resembles cracking in GaN/sapphire, including crack healing and insipient cracks in the substrate; and one in which cracks are very sharp, propagate from the surface, and terminate at the interface.

taken place during growth. In other cases, there is no pitting along the cracks but there may be significant lift-up of the film from the SiC substrate.

3. Understanding the Observed GaN Cracking: The Mechanics of Cracking

The observation of cracks with a “mud-cracking” appearance is *a priori* evidence that the GaN films are cracking under a biaxial tensile stress and that the films behave in a brittle manner. Indeed, only a biaxial tensile stress state can lead to such “mud-cracking”, known in the mechanics community as “channel cracks”. (If the film were under a compressive stress its only way of stress-relief would be by delamination from the substrate and buckling.) The observation that these channel cracks are typically overgrown demonstrates that the tensile stress must be occurring during growth, as further supported by the fact that the thermal mismatch between GaN and sapphire produces only compressive film stress during cooling. The conclusion that GaN films are under tension during growth is somewhat surprising since the epitaxial lattice mismatch between the GaN and sapphire lattices would suggest that the coherency stress would be compressive. The evidence from the cracking that the films are under tension during growth has since been substantiated by the *in-situ* wafer curvature measurements of Hearne and colleagues at Sandia National Laboratories.³

The mechanics of channel cracking are now well understood and have a number of consequences for the growth of GaN films.⁴ The two most important

consequences are: that there exists a critical thickness below which it is energetically unfavorable for cracking to occur, and that when cracking occurs above the critical thickness it can, depending on the fracture resistance, propagate into the substrate. As described above, these characteristic features of channel cracking are indeed observed. In view of the importance of channel cracking in the growth of GaN films, a brief summary of the conditions for its occurrence is warranted. The reader will note that in many respects, the analysis parallels that of the critical film thickness for coherency loss during the growth of epitaxial films. A film under tension stores elastic strain energy that scales linearly with the film thickness, the elastic modulus and the square of the film strain. Thus as the film thickness increases, its total strain energy increases. This continues until it becomes energetically more favorable to form a network of cracks than to maintain the current elastic strain. As the formation of cracks relieves stress it decreases the stored elastic energy in the film but at the cost of creating new surface area. Detailed analysis indicates that cracks form at a critical thickness given by:

$$h_{crit} = \frac{\Gamma_f \bar{E}_f}{Z \sigma_f^2} \quad (1)$$

where Γ_f is the fracture toughness of the film, \bar{E}_f is the plane strain elastic modulus of the film, σ_f is the (uniform) film stress, and Z is a geometric factor that describes the crack shape.⁴

Just as with other defects, cracks must nucleate and grow so there are, in fact, two critical thicknesses. The smaller is that at which it is energetically favorable to form a penny-shaped crack at the surface. In this case, assuming the film and substrate to be elastically matched, $Z = 3.951$. The other, somewhat larger, critical thickness is for the penny-shaped crack to grow both along the surface of the film and down through the film thickness. In this case, $Z = 1.976$. The crack evolution from nucleation to growth through the film is shown schematically in figure 7.

The hexagonal pattern of cracks reflects the six-fold rotational symmetry of the GaN structure about the c-axis and the fact that the cleavage planes in GaN are {1010} planes that lie at 60° to one another. The spacing between the channel cracks in the “mud-cracking” pattern is not constant but is distributed around an average value. As described in detail elsewhere, the average crack spacing is a measure of the biaxial tensile stress in the film prior to crack nucleation and growth.⁵

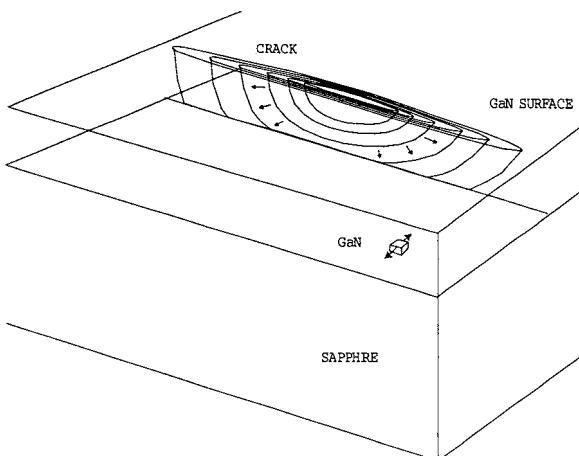


Figure 7. Schematic of a half-penny crack propagating from an initial surface flaw in a GaN film during growth. Crack extension cannot proceed a significant distance into the compressive stress field of the sapphire substrate, and the resulting crack "channels" laterally, extending across the film and crossing other channel cracks to form the characteristic "mud-cracks" shown in figures 1, 2, and 3.

Since the substrate is under compression during film growth, the propagation of the channel cracks into the substrate may seem counter-intuitive as it is usually thought that cracks cannot grow into regions of compressive stress. One would therefore think that the cracks would stop at the film/substrate interface. However, a crack growing in a region of tension, such as the channel cracks, can nevertheless extend a short distance into an adjacent region of compression provided that the stress intensity exceeds the fracture toughness. The explanation lies in the fact that the driving force for a crack to propagate is the release rate of the overall strain energy not simply the stress at the crack tip per se. Consequently, a crack can extend even though the crack tip is in a region of compression provided there is a net driving force for its extension from those regions where it is under tension. It cannot extend far, however, before the strain energy release rate falls below the critical value and the crack arrests.

4. Origin of Stresses

It is usual in analyzing the epitaxial growth of semiconductor films to consider the lattice mismatch between the film and the substrate and to calculate the coherency strain from the mismatch. The resulting stress in the film – usually referred to as the coherency stress – is then simply the lattice mismatch strain

multiplied by the appropriate elastic constants. When a film such as GaN grows by island growth and coalescence, however, additional stresses arise. These coalescence stresses can be large and, in contrast to coherency stresses, do not simply scale with the lattice mismatch. Indeed, the coalescence stresses are invariably *tensile*.

The fundamental origin of the tensile growth stresses in GaN has yet to be resolved, but this model for stress due to island coalescence is one that has been proposed and explored in the literature. The source of the coalescence stress is essentially a microstructural one, derived from a consideration of the energetics of joining two free surfaces by straining islands to form a single grain boundary. The simplest case is illustrated in figure 8, a schematic two-dimensional cross-section of adjacent islands on a substrate. As the initially stress-free islands grow in size, the gap, Δ , between two islands decreases, until a critical point is reached at which the free energy of the system can be reduced by laterally and uniformly straining the two islands so that the two adjacent faces snap together. This critical point is exactly that at which the strain energy generated per unit film area, $\bar{E}h(\Delta/2a)^2$, plus the grain boundary energy, $h\gamma_{gb}/a$, for the coalesced islands is equal to the surface energy of the two adjacent faces, $2h\gamma_{sv}/a$, for the separated islands. Here, \bar{E}_f is the biaxial elastic modulus of the film, h is the island height, and $2a$ is the island width. The maximum stress that can be generated by this mechanism is thus given by:⁶

$$\sigma_{coalesce} = \sqrt{\bar{E} \frac{2\gamma_{sv} - \gamma_{gb}}{a}} \quad (2)$$

For an island width of 10 μm at coalescence, $\sigma_{coalesce} \approx 400 \text{ MPa}$, which is quite sufficient to enable the observed cracking behavior. This calculation of the

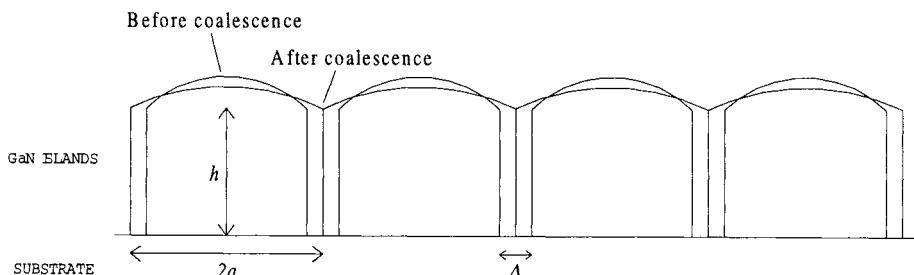


Figure 8. Schematic illustrating the coalescence of equally spaced islands. The coalescence fronts are assumed to be planar and parallel, and the figure shows a cross-section through the islands and the coalescing surfaces.

coalescence stress, however, is based solely on energetics and does not take into account the kinetics of island coalescence, nor does it account for the resistance to sliding along the film-substrate interface. Hence, the value of the coalescence stress given in Eq. 2 can be considered only as a maximum. The model nevertheless makes the primary prediction that the tensile stress generated increases as the island size at coalescence decreases, and thereby as the island density increases.

The degree of tensile stress generated is also a function of the geometry of the impinging grains, and whether the coalescing surfaces are parallel planes or curved surfaces. For GaN, the crystallographic faceting of surfaces suggests that the coalescing surfaces may indeed be parallel, and hence equation 5 is valid. If, however, the grains are growing as hemispheres, more detailed analysis by Freund and Chason based on contact theory predicts that the maximum coalescence stress is:⁷

$$\sigma_{\text{coalesce}} = \frac{2(2\gamma_{sv} - \gamma_{gb})}{R} \quad (3)$$

where R is the radius of the hemispherical island. Note that by this calculation, the coalescence stress for 10 μm diameter islands is only 0.8 MPa, significantly lower. The initial islands deposited in a GaN nucleation layer, however, are much smaller in size and might still allow for significant levels of tensile stress to develop.

The island coalescence mechanism provides a plausible means for tensile growth stress to vary as a function of the nucleation conditions. It has been observed that changes in the nucleation layer are indeed correlated to changes in cracking density in GaN films. Böttcher *et al.* have examined the density of edge threading dislocations as a function of the average grain diameter in GaN and correlated those to the residual in-plane stress at room temperature.⁸ Their results are consistent with an increase in tensile growth stress with increasing island density, as would be predicted by a coalescence model. In the work of Hearne *et al.*, on the other hand, the coalescence of islands during growth at high temperature was monitored and found to produce no change in the tensile stress.³ It remains possible, however, that a coalescence-type mechanism is operating during the deposition and subsequent anneal of the low-temperature nucleation layer.

5. Comparison with Other Semiconductors

Why do GaN films crack during growth whereas other semiconductors do not? There are two principal reasons, one related to the nature of heteroepitaxial growth of GaN on sapphire and SiC substrates and the other related to the temperature dependence of the stress relaxation mechanisms in GaN. These are discussed in the following paragraphs.

The majority of semiconductors are grown on lattice-matched substrates, usually by homoepitaxial growth on single crystals of the same material. Even when there is a small lattice mismatch with the substrate, growth is usually by layer-by-layer growth mechanisms and so islands do not form. Consequently no island coalescence can occur, there are no tensile stresses created by island coalescence, and hence there can be no cracking due to coalescence.

The second difference lies in the nature and temperature dependence of stress relaxation in GaN. In the growth of lattice mismatched semiconductors the films grow with the same lattice parameter as the substrate up to a critical thickness. At the critical thickness, dislocations are nucleated and propagate through the film relieving the mismatch stress. A rather complete and comprehensive understanding of this process has developed since Matthew and Blakeslee originally conceived of the "critical thickness" concept.⁹ Implicit in the concept is that dislocations can glide through the film to relieve the coherency stress. If, however, the growth occurs at a temperature at which there is little or no dislocation mobility then the strain energy cannot be relaxed by dislocation flow. Instead it can only occur by cracking or, possibly, by diffusional flow. The latter is generally ineffective during typical growth times but may be important in subsequent prolonged annealing if such a post-growth annealing procedure were implemented. The question of whether the stress in a material can relax by dislocation flow or by cracking is a longstanding one. Ultimately it depends on the value of the Peierls stress and the activation energy for dislocation glide. The macroscopic manifestation is in the brittle-to-ductile transition (BDT) and the BDT temperature: above its characteristic BDT a material can deform by dislocation flow to relax stresses whereas below that temperature dislocations cannot move and stresses can only be relaxed by cracking. The growth of silicon and GaAs devices is generally carried out at temperatures well above their BDT temperatures (~500°C for silicon and ~320°C for GaAs)¹⁰ and so stresses are relaxed during growth by dislocation flow. The BDT for GaN and its alloys are not known although there is some evidence from studies of the hardness of GaN that the BDT is approximately 1100°C, commensurate with temperatures typically employed in the growth of GaN films.¹¹ As the velocity of dislocation

flow is exponentially dependent on temperature, the relaxation rate of island coalescence stresses can be expected to be very sensitively dependent on the growth temperature relative to the brittle-to-ductile transition temperature.

6. Substrate Fracture

When a GaN film is grown to a thickness greater than the critical thickness and cracks, there is also a propensity for the substrate to crack into pieces. In many of the early reports, no distinction was made between cracking of the GaN film and the fracture of the substrate and it is difficult to distinguish the actual types of cracking observed in these reports. As mentioned earlier, observations of the cross-section of cracked films, such as those shown in figure 4, reveal that the channel cracks in the GaN extend a short distance into the substrate. From a fracture mechanics perspective, these short cracks in the surface of the substrate might be thought of as incipient flaws in the substrate but they cannot extend at the growth temperature since the substrate must be in compression in order to maintain mechanical equilibrium with the tensile stress in the growing film. However, on cooling the stresses in the film and substrate change because of differences in the thermal expansion coefficients between the two. The magnitude and distribution of the thermal expansion mismatch stresses created on cooling also depends on the thickness of the film and the substrate and their elastic constants. In such a bilayer system, the requirements of mechanical equilibrium produce an overall curvature of the system, resulting in a linear variation of the stress through thickness of each layer. The stress distribution through the thickness of the substrate on cooling from the growth temperature is thus given by:

$$\sigma_s(z) = \bar{E}_s \frac{r}{1+r} \Delta\alpha\Delta T + \bar{E}_s \frac{z+t}{R} \quad (4)$$

where z is the distance above the interface, $r = \bar{E}_f h_f / \bar{E}_s h_s$ is the weighted ratio of the film to substrate thickness, $\Delta\alpha\Delta T$ is the thermal expansion mismatch, R is the radius of curvature produced by the induced bending, and t is the distance of the neutral axis below the interface.

$$R = \frac{1}{\Delta\alpha\Delta T} \left[\frac{h_s^2}{6(h_s - 2t)} + \frac{h_f^2}{6(h_f - 2t)} + \frac{1}{2}(h_s + h_f) \right] \quad (5)$$

$$t = \frac{h_s - rh_f}{2(1+r)} \quad (6)$$

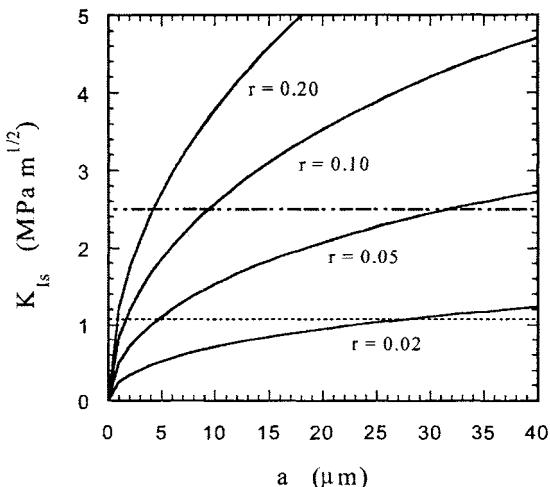


Figure 9. Stress intensity factor for an incipient crack in a sapphire substrate resulting from thermal expansion mismatch with GaN at room temperature. The individual curves correspond to different ratios of the film-to-substrate thickness. The two horizontal lines indicate the fracture toughness of sapphire in dry air ($2.5 \text{ MPa m}^{1/2}$) and in water ($1.1 \text{ MPa m}^{1/2}$), and thus the critical value of the stress intensity necessary for crack extension.

For GaN on sapphire, cooling changes the stress in the sapphire from compressive during film growth to tensile. Incipient flaws, such as those created by the channel crack extension into the sapphire, can then grow in this tensile stress field provided the stress intensity at the tip of the flaw exceeds the fracture resistance of the substrate. The stress intensity at the tip of a flaw that has extended a distance a into a 430- μm thick substrate is plotted in figure 9 for a range of weighted film-to-substrate ratios.¹²

Since the tensile stress in the sapphire substrate increases as the film and substrate are cooled, the stress intensity at the crack tip also increases. Consequently, the temperature at which fracture of the substrate occurs is not unique but rather depends on both the film thickness and the substrate thickness. A further complication is that the fracture resistance, sometimes referred to as the fracture toughness, of sapphire is sensitive to humidity. It has a value of $2.5 \text{ MPa m}^{1/2}$ in dry air but falls to $1.1 \text{ MPa m}^{1/2}$ in water.¹³ This moisture sensitivity indicates that it is important to keep films on sapphire dry throughout subsequent processing.

Silicon carbide differs in two important respects from sapphire. The first is that its thermal expansion coefficient is smaller than both GaN and sapphire.¹⁴ The second is that its fracture toughness is not sensitive to moisture. The consequence of the smaller thermal expansion coefficient is that on cooling the

stress in the GaN becomes increasingly tensile, in contrast to GaN on sapphire which becomes more compressive. The strain energy in the GaN film may reach a critical level at which it becomes favorable for channel cracks to be driven through the film and into the SiC substrate. This is mechanically identical to the case for crack propagation into the sapphire substrate during growth, only now the process is taking place during cooling and with a larger GaN stress field as a driving force. The pertinent crack length by which to assess fracture is now the crack length in the GaN film rather than the incipient crack length in the substrate as it was for the sapphire case. Additionally, for sufficiently thick films, the induced curvature can create a tensile stress at the back surface of the SiC substrate even though the average stress through its thickness is compressive. In such a case, the critical size in the consideration of substrate fracture would be the scratches and other polishing defects on this surface.

The fracture mechanics explanations presented here also provide an explanation for reports in the early literature (circa 1990's) demonstrating that the surface finish of the sapphire substrates influenced the propensity for sapphire fracture and that more carefully polished sapphire substrates were less prone to fracture in the growth of relatively thin (2-10 μm) GaN films. These observations are consistent with the fracture of the sapphire being controlled by surface flaws that extend during cooling. Poorly prepared or scratched sapphire substrates may fail preferentially from such scratches at a lower film thickness so it is important to ensure the use of well-polished (preferably chemo-mechanical-polished) substrates. However, it is important to emphasize that even the most highly polished sapphire substrates will still fracture from the incipient cracks produced in the sapphire by the extension of the GaN channel cracks if the stress intensity on them upon cooling exceeds the fracture resistance.

Finally, in addition to causing complete mechanical failure of the substrate for sufficiently thick films, cracks in the sapphire substrate scatter incident light. Processes for the excimer laser debonding of the GaN-sapphire interface require the transmission of high intensity light through the sapphire to the interface. The presence of substrate cracks thereby interferes significantly with the debonding of thick GaN films grown on sapphire, and attempts to debond such films have resulted in small regions that remain attached immediately above the channel cracks in the sapphire.

7. Growth on LEO Templates

It has been widely reported that thick GaN grown on LEO (lateral epitaxial overgrown) GaN templates on sapphire and SiC substrates do not crack or

fracture whereas those grown under identical conditions on bare substrates do.¹⁵ These reports have been especially puzzling as thick GaN films grown on GaN, GaInN and GaAlN templates still crack above a critical thickness so it is unlikely that the difference is solely due to re-nucleation effects when the thick film is grown homoepitaxially on the template, although this explanation cannot be completely ruled out at the present time.

An alternative explanation lies in the nature of the channel cracks in the GaN film when the critical thickness is exceeded and how they extend into the substrate. As described earlier, channel cracks nucleate at the top of the growing film and grow down through the film thickness (Fig. 7). When growing on a bare substrate or on a bare buffer or template layer, the channel cracks extend into the substrate since there is nothing to impede them. However, it appears that the LEO stripes block the channel cracks and prevent them extending down into the substrate below except in the window region between the stripes. This restricts the *length* of the crack segments generated in the substrate during growth. The effect of this restriction is to *increase* the stress required to propagate the crack through the substrate during cooling.

Formally, the condition for substrate cracking can be expressed in terms of the Griffith fracture condition for a periodic array of half-penny shaped cracks, shown schematically in figure 10. This can be approximated by the stress intensity factor at the lateral tip of a single half-penny crack at a free surface:¹⁶

$$K_{IA} = (1.211) \frac{2}{\pi} \sigma \sqrt{\pi a} \quad (7)$$

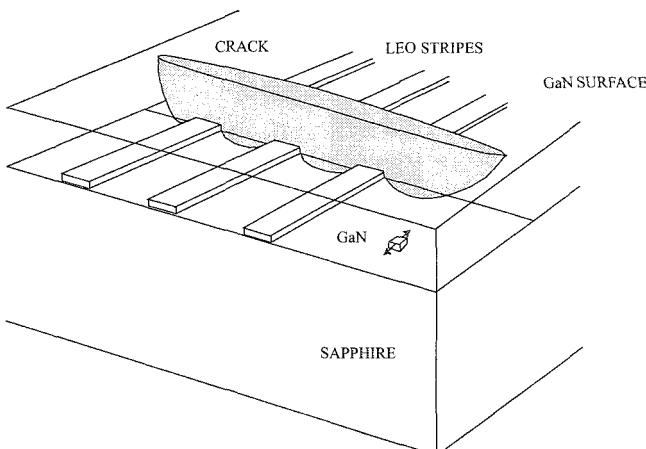


Figure 10. Schematic illustrating the spatial confinement in the sapphire of channeling cracks in the GaN film due to the LEO stripes pinning the channel cracks.

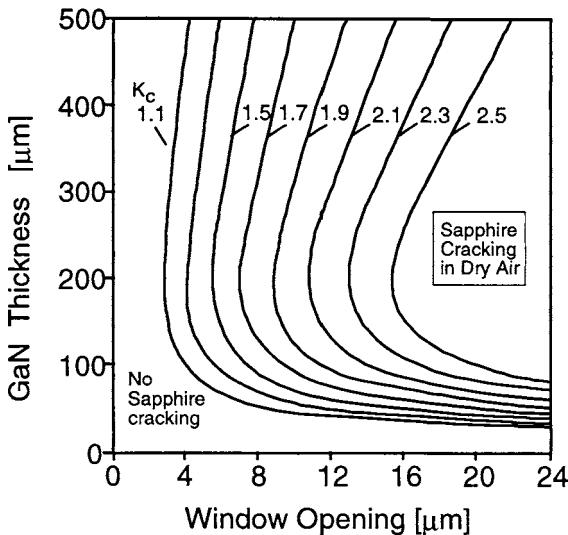


Figure 11. Conditions for sapphire crack extension as a function of film thickness and of lateral constraint due to LEO stripe structure. Each line represents the critical condition for crack extension for a particular value of the fracture resistance of sapphire, which is in turn a function of the environmental humidity. (A substrate thickness of 430 μm and a thermal expansion stress resulting from cooling to room temperature were used in the analysis).

Since the stress intensity is dependent on the stress and initial half-penny crack radius, a (equal to half the window stripe width), decreasing the size of the window opening decreases the stress intensity. Using this equation and equation 4 for the stress distribution through the substrate on cooling, the combination of film thickness and window opening over which substrate cracking can be avoided for different levels of humidity can be mapped out as shown in figure 11. These calculations indicate the importance of the window opening in determining whether substrate cracking occurs and also indicates that at sufficiently small window sizes, fracture can be avoided even for films several hundred microns thick.

Evidence supporting this model can be found in comparing the film cracking and substrate cracking in GaN films grown simultaneously on bare sapphire and on LEO templates. As can be seen in figure 12, the films grown on each are cracked to a similar density, but the sapphire substrate under the LEO template remains uncracked whereas the initially bare substrate is highly cracked.

This explanation naturally raises the question of how the stripes block and pin the channel cracks. The complete answer is not yet known but is most likely that silica and silicon nitride can both deform viscously at the growth temperature

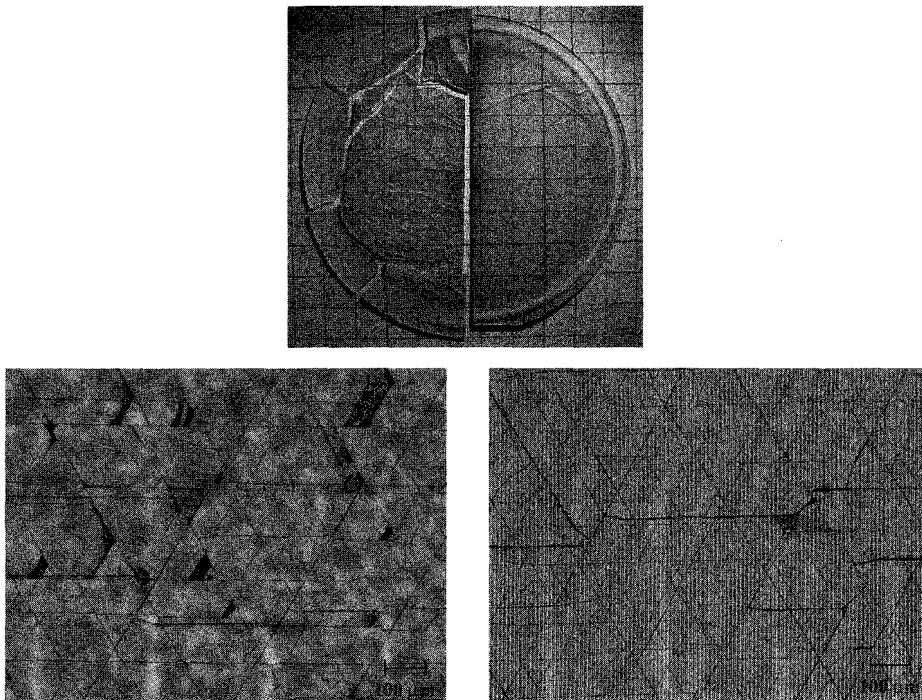


Figure 12. Comparison of films grown simultaneously on bare sapphire (left sector) and on an LEO template (right sector). The GaN film on the left was grown on directly on sapphire and shows significant substrate through-cracking. The film on the right was grown on an LEO substrate (5 μm SiO_2 stripes, 5 μm window width) and shows little sapphire cracking. Optical transmission microscopy reveals, however, that the density of cracks in the GaN is similar in the two half-wafers. (The vertical lines in the right hand micrograph are produced by the LEO stripes.)

and so blunt the channel cracks as they try to propagate through the stripes. At lower temperatures, for instance during cooling, where the stripe material becomes brittle, the stress state will have switched to being compressive and so there is no driving force for the cracks in the stripes to cut through them.

8. Summary

The nature of cracking in GaN on sapphire and on SiC has been characterized. The application of fracture mechanics models to the observed behavior indicates that there are three critical film thicknesses of importance: one for the generation of half-penny cracks from flaws at the surface during growth; one for the extension of these cracks into channels along crystallographic directions in the film and also a small distance into the substrate; and one, relative to the substrate

thickness, at which these small incipient cracks propagate through the substrate during cooling. Differences in the thermal expansion coefficient between sapphire and SiC lead to differences in the cracking behavior during cooling, but the same framework can be used to understand both. The fracture of the film under tensile growth stress, however, is identical for GaN/sapphire and GaN/SiC, indicating that the mechanism for generating this stress is independent of the substrate choice. The tensile stress is set early in the growth; an island coalescence model is one proposed mechanism by which the structure of the nucleation layer would be correlated to the stress, with a higher density of nuclei leading to a higher tensile stress. Unlike other semiconductor films, the relaxation of the stress by dislocation generation and motion is prevented by growth at temperatures at or below the brittle-to-ductile transition temperature, leaving fracture as the only mechanism by which the elastic strain energy in the system can be relieved. Finally, an understanding of how initial flaw size determines the critical point at which substrate cracking occurs can be applied to demonstrate how LEO GaN films reduce substrate cracking by altering the trajectory of the channel cracks and spatially confining them in the substrate to the window region.

Acknowledgments

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DIRECT BONDING OF GaN AND SiC; A NOVEL TECHNIQUE FOR ELECTRONIC DEVICE FABRICATION

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The direct bonding method is applied to the GaN/SiC system, and the processing conditions for successful direct bonding are clarified. Direct bonding of GaN/SiC is achieved at 900°C. The direct bonding of GaN to Si-face SiC is very dependent on the choice of chemical treatments but the bonding of GaN to C-face SiC is less dependent on surface preparation. It is found that an oxide-cleaned surface is essential to achieve good reproducibility of bonding. The electrical properties of the bonded interfaces are also characterized. If a native oxide is present when the bonded interface is prepared, the current through the interface is decreased, which is attributed to an energy barrier due to the presence of charged interface states. Cross section transmission electron microscopy indicates 10nm spaced dislocations at the interface, which form to accommodate the lattice mismatch and twist misfit. In some regions an amorphous oxide layer forms at the interface, which is attributed to inadequate surface preparation prior to bonding. Directly bonded GaN/SiC heterojunction diodes have been fabricated and characterized. The Ga-face (0001) *n*-type 2H GaN films were directly bonded to the Si-face or C-face (0001, 000-1) *p*-type 6H SiC. The I-V characteristics display diode ideality factors, saturation currents and energy barrier heights of 1.5 ± 0.1 , 10^{-13} A/cm², 0.75 ± 0.10 eV for the Ga/Si interface and 1.2 ± 0.1 , 10^{-10} A/cm², 0.56 ± 0.10 eV for the Ga/C interface. The built-in potential was determined from capacitance-voltage measurements to be 2.11 ± 0.10 eV and 2.52 ± 0.10 eV for the Ga/Si interface and the Ga/C interface, respectively. From the built-in potential the energy band offsets are determined to be $\Delta E_C = 0.87 \pm 0.10$ eV and $\Delta E_V = 1.24 \pm 0.10$ eV for the Ga/Si interface and $\Delta E_C = 0.46 \pm 0.10$ eV and $\Delta E_V = 0.83 \pm 0.10$ eV for the Ga/C interface.

Keywords: GaN; SiC; bonding.

1. Introduction

1.1. *GaN/SiC HBTs and direct bonding method*

Recently, Pankove, et al.¹ suggested a high-temperature GaN/SiC heterojunction bipolar transistor with high gain. Silicon carbide is considered for high power and high temperature semiconductor device operation because the material exhibits a wide bandgap (3.0 eV) and high thermal conductivity (5W/cm°C). The operation of silicon carbide bipolar junction transistors with an even larger bandgap emitter would display increased current gain due to improved emitter efficiency. The larger bandgap of the emitter would restrict the diffusion of holes from the base to the emitter, resulting in high electron injection efficiency into the base. Additionally, the increased bandgap of the emitter allows the base to be heavily doped, thereby decreasing the base resistance. Also, since SiC is an indirect bandgap material, free carriers exhibit longer lifetimes, compared to a direct bandgap material such as GaN. The increased lifetime yields a long diffusion length, and a high base transport factor. Furthermore, these devices have a short base width, which further enhances the transport factor, thereby increasing the current gain. Gallium nitride is a natural choice for a larger bandgap emitter for SiC. Gallium nitride

not only has a higher bandgap, 3.4 eV, than SiC, it also has a high thermal conductivity, 1.3W/cm°C.

However with a lattice constant of 3.18Å for GaN and 3.08Å for SiC, the lattice mismatch (~3.4%) can significantly limit the quality of an epitaxial film. The poor wetting of GaN on 6H-SiC(0001) substrates impedes direct nucleation and frequently results in GaN films of poor crystallinity. The use of an AlN buffer layer has been demonstrated to be effective in improving the crystallinity as well as in reducing the defect density in the GaN films, but simultaneously inhibits carrier injection across the AlN/SiC interface due to the insulating nature of AlN and its high band gap.² Reports of the growth of GaN directly onto 6H-SiC(0001) have noted the observation of an amorphous interlayer or zinc-blende inclusions at or near the GaN/SiC interface.² Epitaxial growth by conventional techniques, e.g., molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD), is affected by lattice mismatch strain. During MBE and MOCVD growth dislocations form to relax the strain energy as the layer thickness exceeds a critical value, known as the critical thickness. It is energetically preferred for dislocations to nucleate on the surface of the layer, subsequently gliding down towards the interface, and drawing threading dislocations behind, most of which remain during further layer growth. The critical thickness is on the order of 2nm. The dislocation density observed for GaN on SiC at a thickness of 0.5μm is typically ~ $5 \times 10^9 \text{ cm}^{-2}$.²

Direct wafer bonding is an alternative method of forming a heterointerface or heterojunction. It is an appropriate technique for materials of high lattice mismatch or with chemical instabilities. The method of direct bonding enables the formation of atomic bonds across atomically flat surfaces of different materials without introducing threading dislocations or stacking faults at the interface. This will result in a true ballistic electron transport and extension of mean free path of electrons in vertical structures.

1.2. Important parameters in direct bonding of GaN

In direct bonding of III-V compound semiconductors, annealing temperature and weighting pressure have been considered as critical parameters in the bonding process. Wada, et al.³ reported that when a lower temperature is used, O-mediated bonding due to dehydration of hydroxyl molecules might be dominant. This effect would result in an increase of the barrier height at the interface. Besides, since little migration of group III atoms is expected at lower temperatures, the wafer surfaces need to be made flat on an atomic scale or roughness on the original surfaces will remain as voids at the interface.⁴

Okuno, et al.⁴ and Tokuda, et al.⁵ suggested that the dissociation of group V atoms plays a primary role in the bonding mechanism of III-V materials. The dissociation promotes migration of group III atoms, which should effectively reduce the surface roughness, and thereby dissociated atoms would help establish the bond between two wafers. A temperature of 600°C–700°C was sufficient to cause a desirable level of dissociation in the In-Ga-P material system.⁴ Bonding at temperatures as high as 1000°C was reported in that system, but the high temperature resulted in excessive dissociation of the group V atoms.⁶

Tokuda, et al.⁵ reported bonding of a GaN/GaN materials system where the lowest temperature was 900°C. With annealing at 1000°C, The reproducibility of the bonded GaN/GaN interface was improved, but Ga extraction at the interface was observed. They suggested that 900°C was sufficient to cause a desirable level of N dissociation for GaN/GaN direct bonding, which led to sufficient mobility of Ga.

Tokuda, et al.⁵ used a larger weighting pressure in an attempt to lower the process temperature and improve the reproducibility with a larger weighting pressure. They proposed that because of the surface roughness there is a distribution of pressure in the contacted area and some regions of the contacted area are under very high pressure. The large pressure can induce a local strain, which enhances atomic redistribution to bring about strain relaxation. Therefore, successful direct bonding may be possible at low-temperatures, i.e. 500-800°C, at which III-V semiconductors scarcely dissociate. Moreover, reproducibility of the process may also improve. In their report of the GaN/GaN materials system, direct bonding occurred at 500°C when a large weighting pressure of 42 kgf/cm² was employed.⁵ The interface showed partial bonding, but the reproducibility was quite good. They expected that a modification of the process conditions could enable a uniform and completely fused interface. They also confirmed that the extraction of Ga did not occur at temperatures lower than 900°C. Even at higher than 900°C, when using a large weighting pressure, the amount of Ga extracted was very small. This result was attributed to an improvement of the uniformity of the wafer contact. The results indicate that increased weighting pressure can enhance successful fusion of III-V materials.

A theoretical model of the relationship between the weighting pressures, the amounts of strain of the contacted area, and the physical properties of the bonded interfaces has not been proposed for III-V materials bonding processes. But a model has been developed to describe Si bonding. Gui, et al.⁷ suggested that when an elastic sphere with high elasticity such as silicon and a rigid flat plane are contacted under a normal load P, the surface adherence forces act around the periphery of the contact area, and has a value of $2\pi\omega R$ where ω is the specific surface energy of adhesion (Nm⁻¹) and R is the radius of the elastic sphere, as calculated by Deryagin, Muller, and Toporov⁸ and Maugis.⁹ The distribution of the stresses within the contact regime is assumed to be Hertzian. Thus the radius of contact, a, and the elastic displacement, δ , at the tip of the sphere are given by^{8,9}

$$\frac{a^3 K}{R} = P + 2\pi\omega R, \quad (1)$$

$$\delta = \frac{a^2}{R}, \quad (2)$$

where $K=4/3[E/(1-\nu^2)]$ with ν the Poisson's ratio and E the Young's modulus of the sphere. This model also indicated that a large pressure (P) could induce a local strain (δ). This may enhance atomic rearrangement at sufficiently high annealing temperature to bring about strain relaxation.

1.3. Polarity effect in direct bonding of GaN/SiC

In addition to the temperature and pressure effects, another basic piece of information concerns the polarity of the GaN with respect to the SiC in the direct bonding process. Because it is fundamental for understanding of the bonding process in these materials, we have focused attention on polarity effects for GaN/SiC direct bonding. The SiC oriented in the hexagonal [0001] direction can be either Si-face or C-face, and the GaN can also be either Ga-face or N-face. It is evident that the bonding strength will be determined by the polarity matching of the GaN and the SiC.

Capaz, et al.¹⁰ calculated the total energies and bonding distances of four types of interfaces depending on the interfacial polarity matching with *ab initio* total energy methods.¹¹ Their approach is as follows. The 6H SiC is the polytype most used, which consists of a hexagonal Bravais lattice with a close packed stacking (...ABCACB...)

along the c axis. GaN also exists in a hexagonal structure with the (...ABAB...) stacking sequence known as the wurtzite structure. Structural parameters obtained in the bulk calculations were $a=3.040 \text{ \AA}$, $c/(pa)=0.8177$, $u=0.375$ for 6H-SiC and $a=3.020 \text{ \AA}$, $c/(pa)=0.8130$, $u=0.376$ for GaN, where c and a are the lattice constants, p is the number of bilayers per unit cell (6 for 6H-SiC and 2 for 2H-GaN) and u is an internal parameter describing the relative displacement between the Si(Ga) and C(N) layers along the hexagonal [0001] direction. For ideal tetrahedral coordination $c/(pa) = \sqrt{(2/3)}$ and $u=3/8$ were used in good agreement with experimental results and *ab initio* calculations.¹²⁻¹⁶

Contour plots of the total valence charge density and schematic ball-and-stick models for the four types of interfaces are displayed in Fig. 1. The plane of cut for all the figures is the hexagonal (10-10) plane, which contains two of the four bonds of the tetrahedrally coordinated atoms. The ball-and-stick models superimposed on each charge density plot give an accurate description of the bond lengths and bond angles for each structure. The C and N atoms are surrounded by regions of a high density of contours, reflecting the displacement in the bond maximum density towards these two atoms with higher electronegativity.

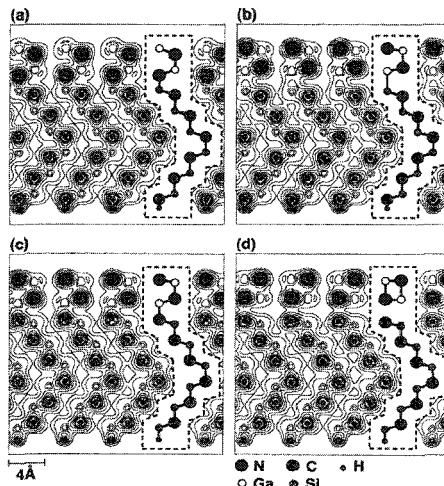


Fig. 1. Contour plots of electronic density for four interfaces. Twelve evenly spaced contours from 0.4 to 3.7 (in units of electrons/ \AA^3) are used. Two additional contours at 0.1 and 0.2 help to map the low charge density regions. Ball-and-stick models are superimposed for each case. Balls are placed at the actual atomic positions and differ by shade and size according to the atomic types. [Ref. 10]

Table 1. Electronegativity differences and bond distances of polarity matching in the GaN/SiC interface. [Ref. 10, 20]

| Bond | Electronegativity difference | Bond distance (\AA) |
|-------|------------------------------|--------------------------------|
| N-Si | 1.2 | 1.77 |
| C-Ga | 0.9 | 1.99 |
| N-C | 0.5 | >2.22 |
| Si-Ga | 0.2 | 2.43 |

Accordingly, Si and Ga atoms correspond to regions of depletion of valence charge density and appear smaller compared to C and N. Fig. 1 (a) corresponds to Si-face SiC bonded to N-face GaN. Notice that the Si and N atoms at the interface form a partly covalent, partly ionic bond. The Si-N bond distance was calculated to be 1.77 Å. Fig. 1 (b) corresponds to Si-face SiC, but the GaN is now Ga-face. A covalent bond is formed between the Si and Ga at the interface (the bond distance is 2.43 Å). However, this bond is weak since most of the charge remains concentrated around the C and N atoms. The total energy difference between the two configurations gave $E_{(a)} - E_{(b)} = -1.08\text{eV}$ per surface atom, indicating that for Si-face SiC the N-face GaN with Si-N interfacial bonds is energetically favorable over Ga-face GaN for direct bonding.

A similar situation was found for C-face SiC [Figs. 1 (c) and (d)]. In Fig. 1 (c), the Ga-face GaN with C-Ga bonds at the interface is shown, and the charge density contours resembled those of Fig. 1 (a), but with inverted polarity. A strong covalent and ionic bond between C and Ga (bond length 1.99 Å) was formed at the interface. However, for N-face GaN [Fig. 1 (d)] the situation was surprisingly distinct from all the previous cases. The N atoms at the interface preferred to form bonds along the c axis to the nearby Ga atoms (bond distance 2.22 Å) rather than to the C atoms of the substrate, yielding a very weakly coupled GaN-SiC system. The angles between the Ga-N bonds at the interface were very close to 90°, indicating sp^2 hybridization of the GaN. Although carbon and nitrogen form strong covalent bonds in a large variety of situations, the presence of the surrounding atoms seemed to make polarity effects very crucial, and the C and N atoms behaved almost like two repelling negative charges. The total energy difference $E_{(c)} - E_{(d)} = -1.07\text{eV}$ per surface atom, suggests that for C-face SiC, the Ga-face GaN with C-Ga bonds at the interface is energetically favorable for direct bonding. The electronegativity differences and the bond distances for polarity matching are summarized in Table 1.

The results presented above can be described in terms of a very simple rule of polarity matching at the interface. The lowest energy interfaces are those on which “positive” ions bind to “negative” ions. Besides being intuitively appealing, this picture is strongly supported by the large energy differences ($\sim 1\text{eV}$ per surface atom) found in the *ab initio* calculations.¹⁰

1.4. Outline of this research

The research is divided into two parts. The initial experimentation is to determine the optimum conditions such as annealing temperature and cleaning process for successful and reproducible bonding. The second experimental goal is to layer transfer the GaN film from the source substrate to the target substrate and to characterize the physical and electrical properties of the bonded structure.

For initial experimentation GaN was grown by MOCVD on SiC with a conducting AlN buffer layer. The optimum conditions such as cleaning process and annealing temperature for successful and reproducible direct bonding of this system are clarified.

After determining the optimum bonding conditions the bonding technique was applied to layer transfer of the GaN film from the source substrate to the target substrate. Although the lattice misfit between Si and GaN is as large as 20%, Si was selected as the source substrate due to the ease of removal after bonding. After layer transfer of GaN to SiC, the interface of the directly bonded GaN and SiC is investigated structurally by high-resolution transmission electron microscopy (HRTEM). The electrical characteristics of n-type GaN/p-type SiC directly bonded heterojunctions were studied using current–voltage (*I-V*) measurements in the temperature range of 300 to 600K and capacitance-voltage (*C-V*) measurements at different frequencies (1 MHz, 10 KHz).

2. Experiment

2.1. Direct bonding of GaN to SiC

The SiC wafers were obtained from Cree Research, and 50 mm 6H (0001)_{Si} SiC and 50 mm 6H (000-1)_C SiC wafers were used. A 1.5 μm thick 2H(wurzite) (0001)_{Ga} n-GaN film was grown by MOCVD onto (0001)_{Si} n-SiC with a (conducting) 0.1 μm thick AlN buffer layer. The (0001)_{Si} SiC wafer and the (0001)_{Ga} GaN film were nominally on-axis, but the (000-1)_C SiC wafer was cut 3° off-axis. Doping levels were $2\sim4\times10^{18}\text{ cm}^{-3}$ in the n-type SiC, $3\sim6\times10^{18}\text{ cm}^{-3}$ in the p-type SiC wafers and $1\times10^{16}\sim10^{17}\text{ cm}^{-3}$ in the GaN film. The SiC wafers showed a resistivity of less than 0.1 ohm-cm for n-type and >1 ohm-cm for p-type. The wafers were diced into $10\times10\text{ mm}^2$ or $6\times6\text{ mm}^2$ pieces and subjected to a sequential bonding process consisting of *ex situ* wet cleaning, *ex situ* contact and *in situ* annealing. The *ex situ* wet cleaning includes a standard RCA SC1 clean ($\text{NH}_4\text{OH}: \text{H}_2\text{O}_2: \text{H}_2\text{O}=0.25:1:5$, 80°C, 10min), DI water rinse (3min), N_2 blow dry and a standard RCA SC2 clean ($\text{HCl}: \text{H}_2\text{O}_2: \text{H}_2\text{O}=1:2:8$, 80°C, 10min), DI water rinse (3min), N_2 blow dry. A final HCl dip was employed for the GaN and a final HF dip was used for SiC substrates (each 10min), where two different concentrations of HF (10:1), (100:1) were used.

After wet cleaning SiC/GaN pairs were positioned in a chuck and loaded into UHV. Bonding was initiated through pressure applied to the surfaces while at room temperature. After the initial contact, *in situ* annealing was employed to form a high density of bonds at the heterointerface. The *in situ* UHV annealing process included 600-1000°C 1hr annealing, except for some GaN/SiC (Si-face) samples, which were annealed up to 5 cycles at 900°C for times up to 30min. The same processes were applied for n-p GaN/SiC pairs.

The surfaces were characterized prior to bonding with AFM and AES. After the bonding sequence, visible light images of the bonded pairs were recorded to characterize the degree of bonding. I-V measurements were completed after deposition of 2000Å of Ti on both sides of the bonded pair.

2.2. Layer transfer of GaN to SiC

The 0.5 μm thick 2H GaN (0001) epitaxial film was prepared by MOCVD growth onto 50mm diameter Si (111) with a 0.1 μm AlN buffer layer. The GaN was grown under conditions that the uncompensated Si impurity concentration in the n-type GaN layer was found to be $2\times10^{18}\text{ cm}^{-3}$ in CV measurements of Schottky barrier diodes. Both faces of 6H SiC (Si-face (0001) or C-face (000-1)) were used for the bonding pair.

Wet cleaning included standard RCA SC1, SC2 cleans with a final HCl dip for the GaN and a final HF (10:1) dip for the SiC substrates (each 10min). The surface RMS roughness measured by atomic force microscopy was $20\pm10\text{ \AA}$ in $20\text{ }\mu\text{m}\times20\text{ }\mu\text{m}$ scans for both the GaN and SiC surfaces. The AES showed ~7 atomic percent of O contaminant on both the GaN and SiC, and ~2 atomic percent of C on the GaN after wet cleaning. The GaN/SiC pairs were then positioned in a chuck, and the initial weak bonding was derived through manual pressure applied to the surfaces while at room temperature.

The pairs were loaded into the UHV chamber, and UHV annealing was employed to form a high density of bonds at the heterointerface. It was found that through UHV annealing, Ga-face 2H-GaN films (0001) were strongly bonded to the on-axis (0001) Si-face and 3° off-axis (000-1) C-face 6H-SiC substrates. The anneal temperature was kept at 900°C and the anneal time was 30 to 120 min. The heating and cooling rates were controlled to be 5°C/min. After bonding the Si substrate was removed using

$\text{HF}+\text{HNO}_3+\text{H}_2\text{O}$ (1+1+1) for 30min (termed HNA etching). After Si removal the sample structures consisted of a $0.5 \mu\text{m}$ -thick *n*-type ($2 \times 10^{18} \text{ cm}^{-3}$) 2H-GaN layer bonded to bulk *p*-type ($3 \sim 6 \times 10^{18} \text{ cm}^{-3}$) Si-face or C-face 6H-SiC. The crystal quality of the bonded GaN layer was studied by X-ray diffraction and room temperature photoluminescence. The full width at half maximum of the double crystal X-ray ω -mode rocking curve for the GaN (0002) reflection was ~ 1000 arcsecs indicating good crystal quality.¹⁷ Near-band edge photoluminescence was observed from the GaN with additional broad defect-related yellow luminescence. High-resolution transmission electron microscopy (HRTEM) was used for analysis of the interfacial microstructure using a JEOL 2010F operating at 200 kV.

The films were then cleaned with organic solvents, dipped in buffered oxide etch (H_2O : HF, 6:1), and rinsed in H_2O immediately prior to being loaded into a thermal evaporator. Using a shadow mask an array of $500\mu\text{m}$ diameter circles of 500\AA thick Al contacts was formed by vacuum thermal evaporation onto the n-GaN layer. No passivation was used for the mesa contact structure. The as-deposited Al contacts were ohmic without annealing.¹ Whole area, 1000\AA thickness Al was used as the backside ohmic contact to the p-type SiC.¹⁸ To investigate the electrical characteristics of the p-n heterojunctions, current-voltage ($I-V$) and capacitance-voltage ($C-V$) measurements were performed using a Keithley 236 source measure unit and a HP4284A LCR meter (in parallel mode), respectively. The I-V characteristics were measured in the temperature range of 300 to 600K. Conventional C-V measurements were performed at different frequencies (1 MHz, 10 KHz) and room temperature.

3. Results and discussion

3.1. Direct bonding of GaN to SiC: Optimum bonding conditions

Table 2 shows the relationship between bonding characteristics and the pretreatment process. When the final wet cleaning is an HF (100:1) 10min etch, the lowest temperature to bond GaN/SiC was 900°C. The GaN/SiC (Si-face) can be bonded at 900°C, however the reproducibility was poor. Only after repeated heating was a bonded interface formed. Even after annealing at 1000°C, the GaN/SiC (Si-face) was not bonded during the first annealing. In contrast, the GaN/SiC (C-face) samples were reproducibly bonded. The GaN/SiC (C-face) was bonded at 900°C without repeated heating, and the reproducibility of bonding GaN/SiC was improved by adopting a higher annealing temperature. When a final wet cleaning of SiC is an HF (10:1) 10min etch, the bonding characteristics of both samples, GaN/SiC (Si-face) and GaN/SiC (C-face) were similar. Repeated heating was not required and bonding occurred at 900°C with good reproducibility.

Figure 2 presents plan-view images of the GaN/SiC bonded pairs. The images show three typical characteristics of the bonded interfaces. When the direct bonding process is carried out under appropriate conditions, the two wafers are completely bonded together. As shown in Fig. 2 (a), neither voids nor GaN dissociation is evident at the interface, and it appears that the GaN and SiC are bonded uniformly. If the sample configuration is not completely parallel and the annealing process is carried out repeatedly at high temperature, GaN dissociation can occur, which may be due to nitrogen desorption, and can lead to the agglomeration of Ga.⁵ The interface in which Ga agglomeration occurs locally exhibits local dark areas as shown in Fig. 2 (b), which is similar to the plan-view image of the GaN/GaN fusion bonding in Tokuda's experiment.⁵

If bonding does not occur at the interface, the GaN/SiC pairs appear as shown in Fig. 2 (c). Interference fringes are observed in the unbonded pairs. Insufficient cleaning or low-temperature annealing tends to result in this type of unbonded interface. Figure 2

(d) shows a plan-view image of a partially bonded interface attributed to an annealing temperature gradient at the interface. A molybdenum bar contacted and pressed the sample during annealing, and heat loss occurred through the contacted area. This results in an annealing temperature gradient at the interface and, finally, partial bonding at the high temperature rim area of the sample. The cooler central region under the bar-contacted area was not bonded. This may indicate that there is a critical annealing temperature for bonding.

The bonding improvement, which results from adopting a high temperature, is also partly attributable to the surface roughness.⁵ Although the epitaxial growth technique of GaN has been developed in recent years, a certain roughness and thickness distribution is unavoidable in GaN epilayers. Because of such roughness, the GaN/SiC cannot be contacted completely over the whole area. The well-contacted region depends on the roughness, particularly the macroscopic undulations that can be observed using a surface roughness profiler. The contacted region induces local strain, which can enhance atomic redistribution to bring about strain relaxation.⁵ The atomic redistribution is also enhanced by annealing the sample. Therefore, successful direct bonding is possible at temperatures high enough to induce a considerable amount of atomic rearrangement. For this reason the reproducibility of the process is improved at increased temperatures.

Table 2. Summary of direct bonding of GaN/SiC surfaces with (100:1) or (10:1) HF etch of the SiC. All samples were UHV annealed for 60min at the indicated temperature except the GaN/SiC (Si-face) (100:1) HF, which was processed with 5 UHV anneal cycles from RT to 900°C. The results are represented as: × : not bonded, v: bonded with poor reproducibility, o: bonded with good reproducibility

| Annealing Temperature | Si-face SiC | | C-face SiC | |
|-----------------------|-------------------------|------------------------|-------------------------|------------------------|
| | HF (100:1) 10min dip | HF (10:1) 10min dip | HF (100:1) 10min dip | HF (10:1) 10min dip |
| 600°C | × | × | × | × |
| 700°C | × | × | × | × |
| 800°C | × | × | × | × |
| 900°C | v | o | o | o |
| 1000°C | v | o | o | o |

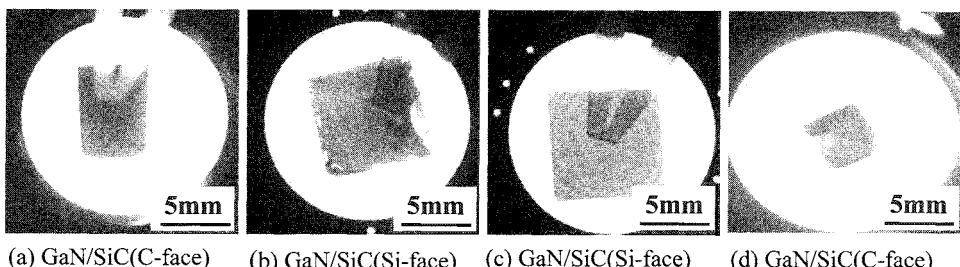


Fig. 2. Plan-view visible light images of directly bonded GaN/SiC pairs. Individual figures show (a) complete bonding after UHV annealing at 900°C for 60min, (b) bonding showing GaN dissociation after 5 UHV annealing cycles between RT and 900°C, (c) no bonding after UHV annealing at 800°C for 60min, and (d) partial bonding after UHV annealing at 900°C for 60min with contact by a molybdenum bar.

Fig. 3 indicates the crystal quality of the GaN layer bonded to SiC, where the GaN was layer transferred from Si to SiC. For the 900°C-annealed sample, the GaN XRD peak was detected at an angle of $2\theta=34.4^\circ$. But for the 1000°C-annealed sample, a GaN XRD peak was not observed suggesting that excessive dissociation of GaN is suppressed at 900°C but occurs at $>1000^\circ\text{C}$. The GaN surface has been reported to dissociate due to N desorption at above 700°C.¹⁹ But the critical temperature for dissociation of GaN is increased in the direct bonding process because of the capping effect of another material on top of the GaN. Tokuda, et al.⁵ reported in their GaN/GaN direct bonding experiment that the extraction of Ga due to N desorption was not detected at lower than 900°C, and even at higher than 900°C, the amount of Ga extracted is very small when a large weighting pressure is employed. In our GaN/SiC bonding experiments evidence of the dissociation of GaN was not observed for the 900°C-annealed sample as is shown in Fig. 2 (a), where a uniform coloration was observed. Moreover, as shown in Fig. 3(a), the GaN XRD peak was detected.

Fig. 4 shows an SEM image of samples annealed at different temperature. At 800°C and 850°C partial bonding was achieved, while whole area bonding was found above 900°C. We suggest that 900°C is sufficient to cause atomic rearrangement through which the interfacial bonding takes place. Fig. 5 shows the bonded GaN on SiC for different duration times all at 900°C. The fraction of bonded area increased as the annealing time increased. This also indicates that the bonding involves atomic rearrangement.

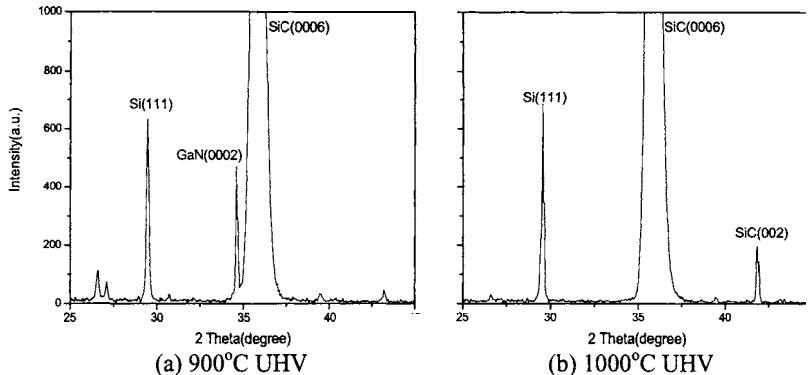


Fig. 3. θ - 2θ X-ray diffraction peak from directly bonded GaN/SiC samples. Although the reproducibility of bonding GaN/SiC was improved by adopting an annealing temperature of 1000°C, such a high temperature caused excessive dissociation of the GaN.

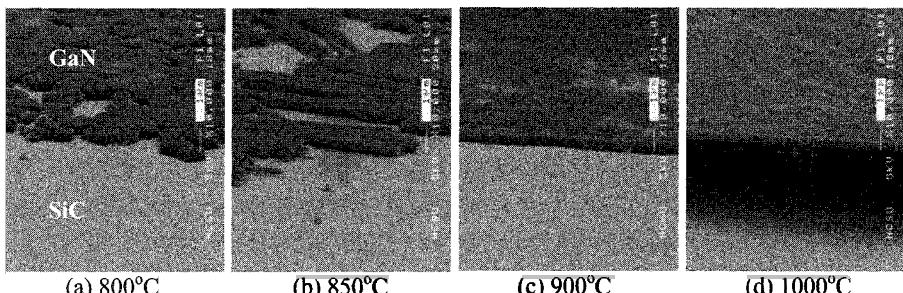


Fig. 4. SEM images of samples annealed at different temperature. Below 900°C partial bonding was found, and above 900°C whole area bonding was observed.

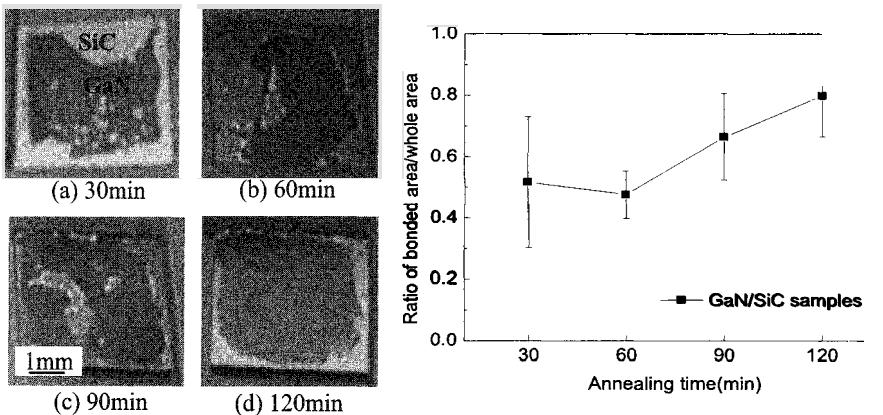


Fig. 5. The ratio of bonded area/whole area of GaN/SiC samples annealed at 900°C with different duration time (30, 60, 90, 120min). An increase of the ratio on the annealing time is evident for the 60 to 120min annealed samples.

3.2. Direct bonding of GaN to SiC: I-V Characteristics

The graphs in Fig. 6 (a) demonstrate the difference of the I-V characteristics of the bonded samples prepared from SiC (Si-face) with different surface pretreatments. These surface pretreatments were obtained by treating the SiC (Si-face) by the standard RCA cleaning procedure followed by either a diluted HF (100:1) etch or a concentrated HF (10:1) etch each for 10min. As is shown in Fig. 6 (a), the bonded samples with SiC (Si-face) pretreated with a diluted HF (100:1) etch showed a high-resistance and nonlinear behavior up to high voltages in the current-voltage curve. Figure 6 (c) shows the electrical characteristics of the n-p GaN/SiC (Si-face) bonded pairs. Again the GaN/SiC (Si-face), where SiC was pretreated by HF (100:1), showed high resistance, but the GaN/SiC (Si-face) pretreated by HF (10:1) showed lower resistance.

However, the influence of the chemical treatment on the I-V characteristics was not clear in the GaN/SiC (C-face). Figures 6 (b) and (d) show the I-V characteristics of the n-n or n-p GaN/SiC (C-face), where the SiC was pretreated by a HF (100:1) or HF (10:1) 10min dip. There was no considerable difference in current-voltage behavior compared with the behavior of the GaN/SiC (Si-face) in n-n and n-p structures (Figs. 6 (a) and (c)).

The AES data showed that the HF (10:1) treated SiC (Si-face) has ~7 atomic percent of O, and the HF (100:1) treated SiC (Si-face) has >50 atomic percent of O (Fig. 7 (a)). However, the C-face SiC had an unchanged atomic percent (~7%) of O on surfaces prepared with either the HF (100:1) or HF (10:1) chemical treatment (Fig. 7 (b)). The GaN was treated by the standard RCA cleaning procedure and a 10min HCl dip. The AES showed ~7 atomic percent of O and ~2 atomic percent of C on the GaN surface after the wet cleaning (Fig. 7 (c)).

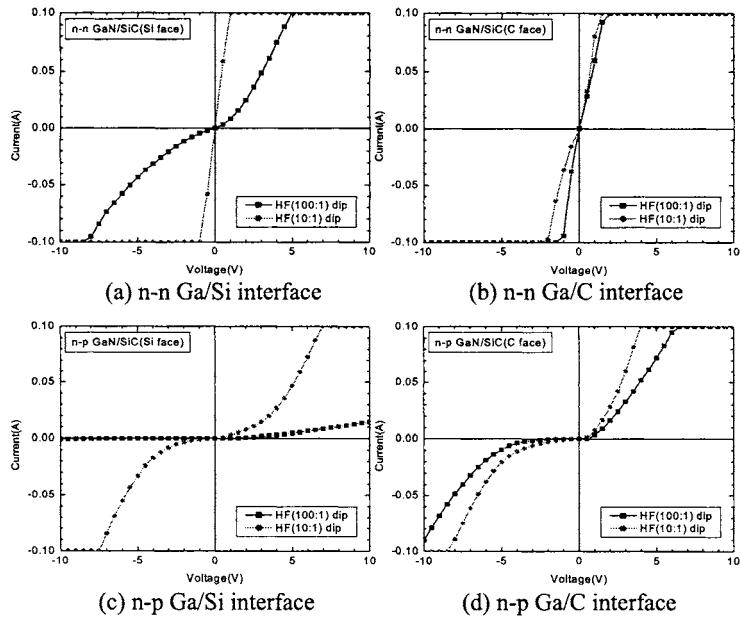


Fig. 6. Current vs. voltage characteristics of GaN/SiC samples: (a) n-n type, (c) n-p type GaN/SiC (Si-face) samples, (b) n-n type, and (d) n-p type GaN/SiC (C-face) samples. SiC was wet-cleaned with HF (100:1) or HF (10:1) 10min dip prior to bonding and GaN was cleaned with a 10min HCl dip. (Resistivity: 0.1 $\Omega\text{-cm}$ for GaN and n-type SiC, and $> 1 \Omega\text{-cm}$ for p-type SiC.)

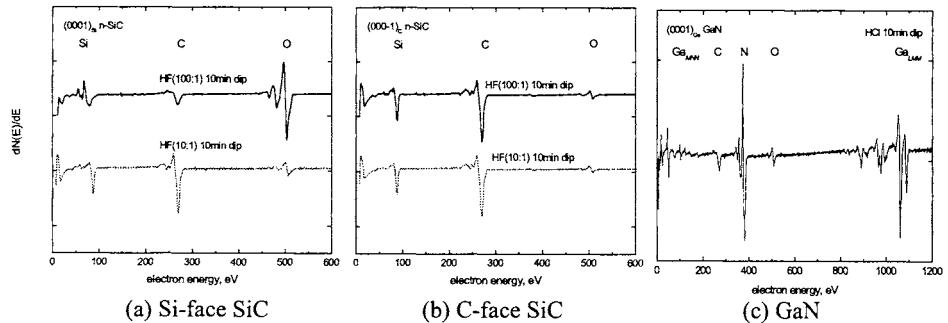


Fig. 7. AES data for (a) Si-face SiC treated by a 10min HF (100:1) dip or a 10min HF (10:1) dip, (b) C-face SiC treated by a 10min HF (100:1) dip or a 10min HF (10:1) dip, and (c) GaN treated by a 10min HCl dip.

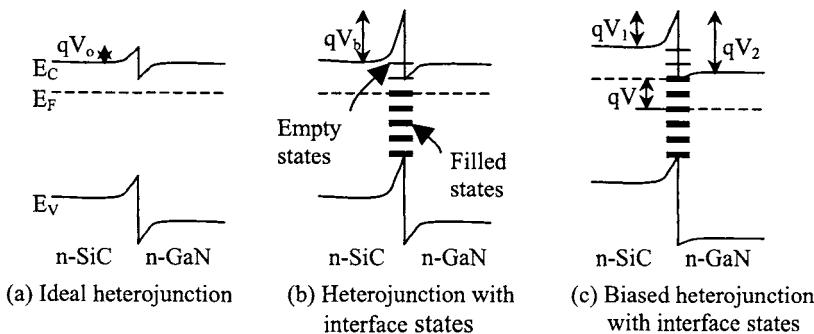


Fig. 8. Energy band diagrams for an n-n GaN/SiC heterojunction with an (a) ideal interface, (b) interfacial states at thermal equilibrium, and (c) interfacial states with an applied voltage V . The interface states increase the potential barrier at the heterojunction (qV_b) from the ideal case (qV_0) and results in nonlinearities in the I-V curves.

The electronegativity of C atoms (2.5) is higher than Si atoms (1.8),²⁰ and consequently, the electronegativity difference with O atom (3.5) is different. The electronegativity difference of C-O (1.0) is much smaller than the difference of Si-O (1.7). We suggested that this effect leads to a reduced amount of native oxide on the C-face SiC, which results in the similar O concentration after the different HF etching processes.

The influence of chemical treatment on current versus voltage linearity and differential resistance and thereby on the density of interface charges is evident. These results indicate that the thin native oxide layer present on the SiC surfaces treated in a diluted HF etch contributes to the formation of the interface states, giving rise to a barrier at the interface. Electrically charged defects at an interface may result in an increased barrier at a junction as shown in Fig. 8. The heterobarrier (qV_b) at the nonideal interface increases with the interface state (charged defect) density.^{6, 21} A defect density due to interfacial oxide forms the barrier, and this adversely affects the I-V characteristics.²¹ That is, increasing high-resistance nonlinearities in the I-V curves occur as the interfacial oxide amount increases.²¹

The effects of interface states are illustrated in the n-n GaN/SiC heterojunction in Fig. 8. Fig. 8 (a) represents low-resistance conduction across an ideal junction with a heterobarrier (qV_0) that is sufficiently small. The band diagram in Fig. 8 (b) represents an interface with defect states for two n-type materials at thermal equilibrium. Here acceptor states as well as donor states are present at the interface. The Fermi-level has a position at the interface so that a number of acceptor states are filled with electrons.²¹ These filled acceptor states trap negative interface charge and produce an electron energy barrier as shown in Fig. 8 (b).

Engström, et al.²¹ suggested that when a voltage, V , is applied as shown in Fig. 8 (c), the Fermi-levels on the two sides are separated by an energy corresponding to qV . This results in a decrease of the energy barrier qV_1 for electrons in the conduction band of the negatively biased side of the structure while the applied voltage is taken up mainly by increasing the barrier, qV_2 , on the positively biased side. Decreasing the barrier height qV_1 , by increasing V , results in a flow of majority carriers across the interface which are collected by the back biased space charge region on the positive side and transported into the external circuit. The separation of the Fermi-levels at the interface means that a repopulation takes place among the interface states.²¹ As is realized from Fig. 8 (c), in the n-n case, the separation of Fermi-levels then gives an increasing negative charge at the

interface, which counteracts the lowering of qV_1 when the bias voltage V is increased. Consequently, the interface states may have a pronounced influence on the resistance of bonded interfaces.²¹

3.3. Layer transfer of GaN to SiC: Interfacial microstructure

The interface morphologies of the GaN/SiC (Si-face) and GaN/SiC (C-face), which were bonded at 900°C for 1 hour, are imaged using high-resolution TEM (HRTEM) (Fig. 9). It is evident that the interface region was restructured after bonding. Apparently, significant atomic-rearrangement processes occurred during the high temperature annealing, resulting in a structurally ordered crystalline fused interface.

Figures 9 (a) and (b) display the dislocation network at the bonded interface. Misfit dislocations are observed at the interface and found to be spaced at an equal interval. The average spacing is about 10nm for the GaN/SiC (Si-face) interface and around 6nm for the GaN/SiC (C-face) interface.

The bonded interface microstructures including interface dislocation network in III-V compound semiconductors have been carefully studied by Jin-Phillipp, et al.²², and Patriarch, et al.²³. They suggested that after bonding two kinds of dislocation networks should form at the interface. The first dislocation network is to accommodate the lattice misfit and twist orientation. A single two-dimensional network of mixed dislocations can accommodate both misfit ε_0^* and twist θ . Since the edge and screw segments associated with a given Burgers vector are perpendicular, this can be achieved through a network whose lines incorporate screw and edge segments in the proportion l_e/l_s , thereby producing a square network of jagged lines with spacing D_1 with

$$D_1 = b^* / \sqrt{(\varepsilon_0^{*2} + \theta^2)}, \quad (3)$$

where $b^*=a^*$ for GaN, SiC where perfect dislocations have Burgers vector of $a/3<11\bar{2}0>$ with a glide on {0001} planes,^{24, 25} and a^* the lattice constant, and ε_0^* the lattice mismatch, both at the bonding temperature. The expected distance D_1 is ~ 9 nm with the assumption that the twist misorientation is around $1^\circ\text{-}2^\circ$.

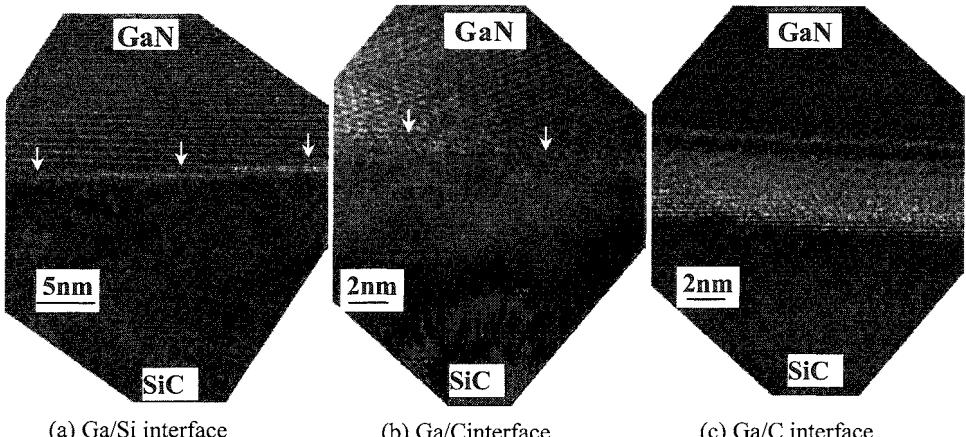


Fig. 9. Cross-sectional high resolution electron micrograph of (a) the GaN/SiC (Si-face) interface and (b,c) regions of the GaN/SiC (C-face) interface. The downward arrows in (a) and (b) indicate the presence of dislocations. In some areas ($\sim 30\%$) the interface was not as perfect, rather it contained a thin amorphous-like layer with a thickness of a few nanometers as shown in (c).

The second dislocation network is to accommodate the tilt misfit. Accommodation of this tilt requires dislocations with Burgers vectors having an edge component b_n normal to the bonding plane. In the limit of small tilt ω , the distance between these dislocations is expected to be

$$D_2 = b_n^*/\omega , \quad (4)$$

where $b_n^*=c^*$ is the Burgers vector parallel to the c-axis at the bonding temperature. The expected distance D_2 is ~ 150 nm for the GaN/SiC (Si-face) where ω is less than 0.2° and ~ 10 nm for the GaN/SiC (C-face) where ω is $\sim 3^\circ$.

The average spacing of dislocations is about 10 nm for the GaN/SiC (Si-face) interface and around 6 nm for the GaN/SiC (C-face) interface, which is consistent with the calculated values. Therefore, we suggest that the interfacial dislocations in Figs. 9 (a) and (b) are basically formed by mixed dislocations to adapt a lattice misfit in addition to twist and tilt misorientation. For the GaN/SiC (C-face) interface, the 2nd dislocation network would be spaced similarly to the 1st dislocation network. This would result in an average dislocation distance less than 9 nm.

As shown in Fig. 9 (c), some areas ($\sim 30\%$) contain a thin amorphous-like layer with a thickness of a few nanometers. Such an amorphous layer at the interface was observed in all samples of GaN/SiC (Si-face) and GaN/SiC (C-face) pretreated by the HF (10:1) 10 min dip. The formation of such an amorphous interlayer is attributed to the native oxide layer that formed on the wafer surface before the onset of the bonding process.²² The amorphous native oxide layer is attributed to an incomplete removal of oxide layers of the SiC and GaN prior to bonding. We note that ~ 7 atomic percent of O was present on both the surfaces of SiC and GaN (Fig. 7).

Shi, et al.^{26, 27} reported that generally during high temperature annealing, local formation of the amorphous regions takes place in the bonding process. A complex transformation process involving impurity atom interdiffusion has taken place, resulting in the formation of the amorphous area during annealing. Consequently a change of the interface morphology occurs. Diffusion and interdiffusion of the materials in the interface layer will even out the surface and may enable the bubble like regions to agglomerate, reducing the overall surface tension by becoming geometrically spherical. The thickness of the amorphous layer collapses to almost zero in most areas. However there will be an amorphous layer in some areas, and the areal percentage of the amorphous layer over the whole interface area will be dependent on the amount of the surface contaminant prior to bonding. During the formation of the bonded area, those impurities, contaminations, and defects will diffuse along the interface boundary and will be trapped into bubble like regions, forming the disordered nonconductive area. Through this process an irregularly distributed array of nanoscale, bubblelike regions formed at the bonded interface area.²⁶

3.4. Layer transfer of GaN to SiC: I-V characteristics

Fig. 10 presents a plot of semilog $I - V$ curves for the GaN/SiC *n-p* heterojunctions at different temperatures 300-600 K. The electronic properties exhibited typical diode behavior. The forward current varies exponentially with applied voltage and can be expressed by $I = I_0 \exp(qV_a/nkT)$, where I_0 the saturation current (A), n the ideality factor, V_a the applied voltage (V), k the Boltzman constant, and T temperature (K). At forward bias, the $\ln(I)$ vs. V plot exhibited linear regions before the effect of the series resistance becomes predominant. For the diode having a Ga/Si interface, at 300-500 K temperatures, an extracted ideality factor of 1.5 ± 0.1 was obtained.

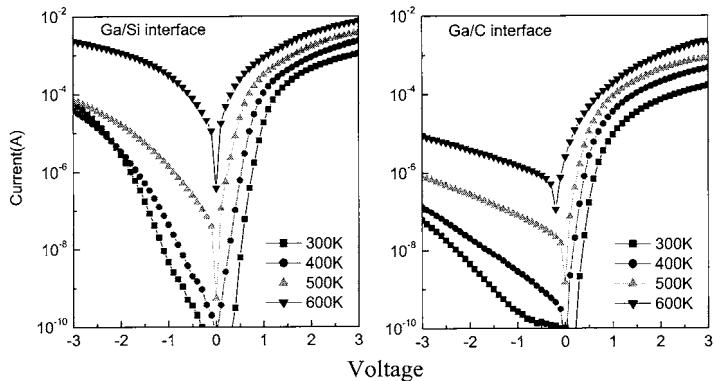


Fig. 10. I-V characteristics at different temperatures, 300 to 600K, from the directly bonded GaN/SiC n-p heterojunction diodes, with different interfacial polarity matching. The device area is a $500\mu\text{m}$ diameter circle.

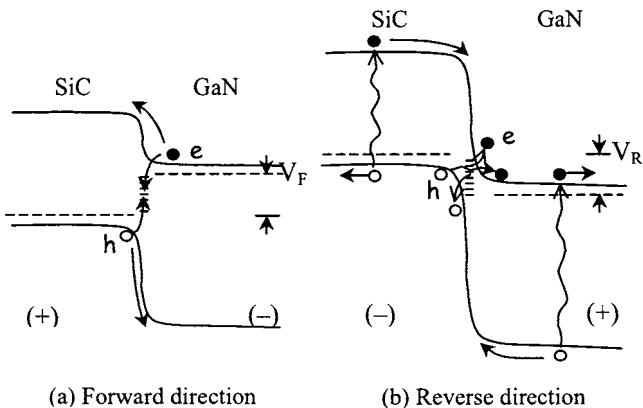


Fig. 11. Band diagrams of GaN/SiC n-p heterojunction, where the injection process and the tunneling assisted generation-recombination process have been indicated with arrows. These band alignments are of type II, and will result in decreased current in (a) forward direction and increased current in (b) reverse direction.

For the diode having a Ga/C interface, the ideality factor was determined to be 1.2 ± 0.1 . At 600K, the current was early saturated, and the ideality factor was >2 for both interface diodes. The room temperature extrapolated saturation current densities are 1×10^{-13} and $1 \times 10^{-16} \text{ A/cm}^2$ for the Ga/Si interface diode and the Ga/C interface diode, respectively. These values are similar to those measured for AlGaN/SiC diodes ($n=1.4$, $J_{\text{sat}} = 2 \times 10^{-17} \text{ A/cm}^2$)²⁸ but much higher than the predicted value by classical drift/diffusion theory ($\sim 10^{-43} \text{ A/cm}^2$)^{29,30} for an ideal diode ($n=1$). These diodes displayed high leakage currents of $6.4 \pm 0.1 \text{ mA/cm}^2$ for the Ga/Si interface diode and $2.3 \pm 0.1 \text{ mA/cm}^2$ in the Ga/C interface diode at -0.5V with catastrophic reverse failures between -30 and -50V .

To explain our experimental results, let us consider the energy-band diagram of the n-p heterojunction with interface traps shown in Fig. 11. This diagram suggests that mechanisms other than thermal recombination-generation are involved. Kuznetsov, et al.³¹ supposed that the electronic transport in the GaN/SiC n-p heterojunction, in the

forward direction, is limited by the tunneling rate of electrons from the conduction band of GaN into the interface traps with subsequent recombination with holes via the interface traps. This recombination rate depends on the effective mass of electrons in GaN, on the dielectric constant of the semiconductor, on the donor concentration in GaN, and on the effective barrier height. For reverse bias, the dominant leakage mechanism would include carrier generation mechanisms induced by a high density of morphological defects and also electrons tunneling from the bottom of the SiC valence band into the conduction band of the GaN, i.e. the so-called Zener effect.³¹

3.5. Layer transfer of GaN to SiC; activation energy measurement

We have attempted to draw activation energy plots of either the reverse currents at fixed bias voltage or the saturation current densities extrapolated from I-V forward characteristics. Neither yielded linear Arrhenius-like results. This is attributed to the various mechanisms of carrier recombination-generation explained above. To obtain the activation energy of such a device with a considerable amount of interfacial defects, we constructed Richardson plots of the forward current densities from the temperature dependence of the current-voltage characteristics.³²

The usual Richardson formula is given by:

$$J_f = A^* T^2 \exp\left(-\frac{q\Phi_{IV}}{kT}\right) \exp\left(\frac{qV_f}{nkT}\right) \quad (5)$$

where A^* is an effective Richardson constant ($A^* = m_{eff} \times 120 \text{ A cm}^{-2} \text{ K}^{-2}$), Φ_{IV} is the apparent barrier height as obtained from I-V measurements and J_f , V_f are the forward current density (A/cm^2) and forward voltage (V).

In Fig. 10 the forward current-voltage characteristics obtained at different temperatures in the range from 300 to 600 K are shown. The deviation from linearity in the high forward voltage region in Fig. 10 is attributed to the series resistance. In Fig. 12 the logarithm of J_f/T^2 vs. $1000/T$ is plotted (Richardson plot). The J_f -values used here are taken at a forward voltage of 0.5 V in order to avoid both the influence of currents additional to the thermionic emission in the low forward voltage region and the influence of series resistance at high forward voltage.³² From Fig. 10 it is evident that at 0.5 V, a linear relationship is obtained at all temperatures investigated. The straight line in Fig. 12 is in accordance with equation (5), which can be expressed as:

$$\ln\left(\frac{J_f}{T^2}\right) = \ln A^* - \frac{q\Phi_{IV}}{kT} + \frac{qV_f}{nkT} \quad (6)$$

From the temperature dependence of the current-voltage characteristics the apparent barrier height Φ_{IV} is obtained by the equation:

$$\Phi_{IV} = -\frac{\Delta \ln(J_f/T^2)}{\Delta(10^3/T)} \frac{10^3}{q/K} + \frac{V_f}{n} \quad (7)$$

The barrier height obtained from this equation was $0.75 \pm 0.10 \text{ eV}$ for the Ga/Si interface diode and $0.56 \pm 0.10 \text{ eV}$ for the Ga/C interface diode. The Ga/Si interface showed higher values of the ideality factor, the saturation current density, the leakage current density and the energy barrier height than the Ga/C interface. The extracted values are summarized in Table 3.

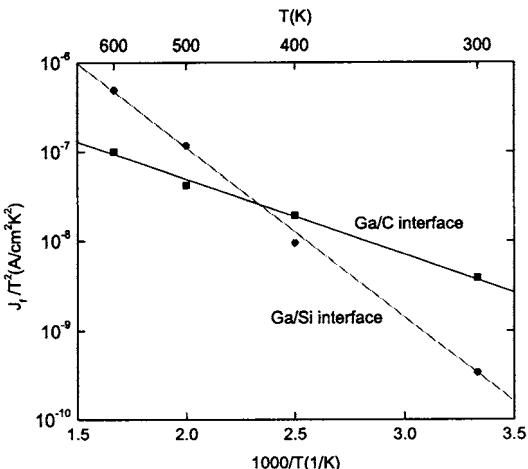


Fig. 12. Plot of $\log J_s/T^2$ vs. $1000/T$ as obtained from Fig. 10 at $V_f = 0.5V$. It is found that $\Phi_{IV} = 0.75 \pm 0.10$ eV for the Ga/Si interface and 0.56 ± 0.10 eV for the Ga/C interface.

Table 3. A summary of saturation current (J_{sat}), ideality factor (n), deduced barrier height (Φ_{IV}), and deduced built-in potential (Φ_{bi}^*) measured in the directly bonded GaN/SiC n-p heterojunctions having different interfacial polarity matching. Conduction and valence band offsets (ΔE_C , ΔE_V) were calculated from the measured built-in potential (Φ_{bi}^*). The total experimental error is ± 0.10 eV.

| Interfacial Bonding | I-V | | | C-V | | |
|---------------------|--------------------------------|----------------|------------------|--------------------|-------------------|-------------------|
| | J_{sat} (A/cm ²) | n | Φ_{IV} (eV) | Φ_{bi}^* (eV) | ΔE_C (eV) | ΔE_V (eV) |
| Ga/Si | $\sim 10^{-13}$ | $1.5(\pm 0.1)$ | 0.75 | 2.11 | 0.87 | 1.24 |
| Ga/C | $\sim 10^{-16}$ | $1.2(\pm 0.1)$ | 0.56 | 2.52 | 0.46 | 0.83 |

3.6. Layer transfer of GaN to SiC: C-V characteristics

Complementary C-V measurements have been performed using two different test signal frequencies. The capacitance was observed to change slowly as a function of frequency but there was no significant deviation in the extracted value for the built-in potential. The C-V characteristics were non-linear when plotted in C^2 versus V coordinates. This is attributed to the tunneling-recombination processes involving the interface traps. Because of this it was not possible to determine directly the built-in voltage from a conventional Anderson's treatment³³ of the capacitance measurements.

The Anderson's energy band model does not take into account the effects related to the interface states. However, it should be pointed out that a C^n -V plot (see Fig. 13) does show a linear dependence with $n= 2.5$. The $1/C^{2.5}$ was a linear function of the applied reverse bias up to at least 10V. This result suggests a conduction mechanism in these devices where the interface has a high density of defects that are effective tunneling centers. We used a modified Donnelly-Milnes model³⁴ of the C-V measurements in order to account for the presence of traps. Our result shows that the actual interfacial defects effect is described by the Donnelly-Milnes theory. Regarding the value of $n= 2.5$ in a C^n -

V plot, our results are very similar to those obtained by Kuznetsov, et al.³¹ who made GaN/6H-SiC n-p heterostructures by HVPE growth. Kuznetsov also attributed the $n=2.5$ value instead of $n=2$ to tunneling-recombination processes due to the participation of the interface traps.

The $(1/C^{2.5})-V$ curves of an abrupt heterojunction can be analyzed using the following expression³⁴:

$$\frac{1}{C^{2.5}} \propto \frac{2(\epsilon_{GaN}N_{GaN} + \epsilon_{SiC}N_{SiC})}{q(N_{GaN}N_{SiC}\epsilon_{GaN}\epsilon_{SiC})A^2} \left(\Phi_{bi} - \phi_m - \frac{1}{2q(\epsilon_{GaN}N_{GaN} + \epsilon_{SiC}N_{SiC})} Q_{IS}^2 - V_C \right), \quad (8)$$

where N_{GaN} , N_{SiC} , ϵ_{GaN} , ϵ_{SiC} are the donor and acceptor densities (cm^{-3}) and permittivities (F/cm) of *n*-GaN and *p*-SiC, respectively, A is the cross sectional area (cm^2) of the heterojunction, q is the electronic charge (C), Φ_{bi} is the built-in potential (V), ϕ_m is the interfacial dipole (V), Q_{IS} is the charge on interface states (C/cm^2), and V_C is the cut-off voltage (V) in the heterojunction. The number of charged interface states, that is, the minimum density of interfacial defects, is obtained by dividing $|Q_{IS}|$ by q . We used $n=2.5$ instead of $n=2$ from the original Donnelly-Milnes equation. Since the film and the substrate are highly doped ($2\sim6\times10^{18} \text{ cm}^{-3}$), the capacitance of the contact is assumed to be much larger than the capacitance in the heterojunction ($C_{\text{contact}} \gg C_{\text{HJ}}$). Furthermore, the bulk series resistance is negligible.

If the cut-off voltage is assumed to represent the built-in potential as in the conventional Anderson's theory, then equation (8) is simplified into equation (9), where the measured built-in potential Φ_{bi}^* contains the interfacial dipole and interfacial charge density.

$$\frac{1}{C^{2.5}} \propto \frac{2(\epsilon_{GaN}N_{GaN} + \epsilon_{SiC}N_{SiC})}{q(N_{GaN}N_{SiC}\epsilon_{GaN}\epsilon_{SiC})A^2} (\Phi_{bi}^* - V_C) \quad (9)$$

Because the measured built-in potential represents the bulk built-in potential reduced by the amounts of the interfacial dipole and the interfacial state charge, the measured built-in potential will be lower than the built-in potential. The cut-off voltage of the C-V characteristics was found to be 2.11 ± 0.10 V for the Ga/Si interface diode and 2.52 ± 0.10 V for the Ga/C interface diode. The C-V cut-off voltage is significantly less in the Ga/Si interface diode than the Ga/C interface diode.

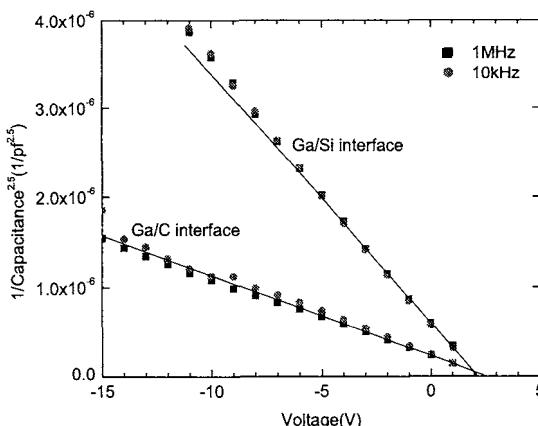


Fig. 13. C-V characteristics, i.e., $(1/C^{2.5})$ vs. V , for the directly bonded GaN/SiC n-p heterojunction diodes that have different interfacial polarity matching. The device area is $500\mu\text{m}$ diameter circle and the measurement was performed at two different test signal frequencies, 1MHz and 10kHz.

3.7. Layer transfer of GaN to SiC: Flat band energy diagram

From the measured built-in potential (Φ_{bi}^*), the band offsets (ΔE_C , ΔE_V) in these heterostructures can be determined as follows³⁵:

$$\Delta E_C = E_{G,SiC} - [(E_F - E_V)_{SiC} + \Phi_{bi}^* - (E_F - E_C)_{GaN}] \quad (10)$$

and

$$\Delta E_V = E_{G,GaN} - [(E_F - E_V)_{SiC} + \Phi_{bi}^* - (E_F - E_C)_{GaN}] \quad (11)$$

where E_G is the bandgap energy, E_F is the Fermi level, and E_C and E_V are the conduction and valence bands, respectively. The calculation of the Fermi levels in the *p*-SiC and in the *n*-GaN was performed using the Fermi-Dirac integrals and doping concentrations.³⁵ The values are $(E_F - E_C)_{GaN} = 0.005\text{ eV}$ ($n = 2 \times 10^{18} \text{ cm}^{-3}$), and $(E_F - E_V)_{SiC} = 0.045\text{ eV}$ ($p = 6 \times 10^{18} \text{ cm}^{-3}$). The conduction and valence band offsets are $\Delta E_C = 0.87 \pm 0.10 \text{ eV}$ and $\Delta E_V = 1.24 \pm 0.10 \text{ eV}$ in the Ga/Si interface diode and $\Delta E_C = 0.46 \pm 0.10 \text{ eV}$ and $\Delta E_V = 0.83 \pm 0.10 \text{ eV}$ in the Ga/C interface diode, respectively. The values are a statistical average from ~5 diodes, and the total experimental error is $\pm 0.1 \text{ eV}$. The built-in potential and the band offsets of the GaN/SiC heterojunction as determined from the *C-V* data are listed in Table 3.

It has been proposed that the conduction band offset of the GaN/SiC heterojunction is an intrinsic feature, i.e. the energy barrier height.³⁶ From our *C-V* measurements the energy barrier heights are $0.87 \pm 0.10 \text{ eV}$ for the Ga/Si interface diode and $0.46 \pm 0.10 \text{ eV}$ for the Ga/C interface diode. These values are slightly different from the apparent barrier height as obtained from I-V measurements ($0.75 \pm 0.10 \text{ eV}$ for the Ga/Si interface diode and $0.56 \pm 0.10 \text{ eV}$ for the Ga/C interface diode). Song, et al.³² proposed that the difference in apparent barrier height as obtained from capacitance-voltage and current-voltage measurements could be explained by introducing a distribution of barrier heights over the measured area and a temperature dependence of the real barrier height. Taking into account this barrier height distribution and the temperature dependence of the barrier height, *C-V* measurements also showed the same trend, namely that the Ga/Si interface has the higher barrier height than the Ga/C interface.

The flatband energy diagram for the 6H-SiC/GaN p-n heterojunction constructed according to the modified Donnelly-Milnes theory is shown in Fig. 14. This diagram shows the measured built-in potential (Φ_{bi}^*), the energetic distance from the Fermi level to the nearest band edge (δ), the discontinuities in conduction-band and valence-band edges (ΔE_C and ΔE_V). The basic characteristics of the flatband energy diagram were calculated from the cut-off voltage in the *C-V* measurements. The energy-band profile near the interface plays an important role in understanding the current flow mechanism in the heterojunction.

In the bonding process, the interface traps are at the heterojunction interface, and the density of interface traps depends on the lattice misfit and the twist and tilt misorientation of the two semiconductors.^{22, 23} Besides the misfit and misorientation effects, the polarity matching effects between the directly bonded GaN/SiC heterojunctions are also important. In our work values of $\Delta E_C = 0.87 \pm 0.10 \text{ eV}$ and $\Delta E_V = 1.24 \pm 0.10 \text{ eV}$ for the Ga/Si interface diode and $\Delta E_C = 0.46 \pm 0.10 \text{ eV}$ and $\Delta E_V = 0.83 \pm 0.10 \text{ eV}$ for the Ga/C interface diode were obtained. This result indicates that the band offset is apparently dependent on the interfacial polarity matching. Städele, et al.³⁷, Agrawal et al.³⁸, and Binggeli, et al.³⁹ reported that the electronic band offsets of GaN/SiC were found to depend strongly on the chemical composition of the interface layers. However, considering the origin of the interfacial charge related to the interfacial polarity matching, a detailed explanation of the

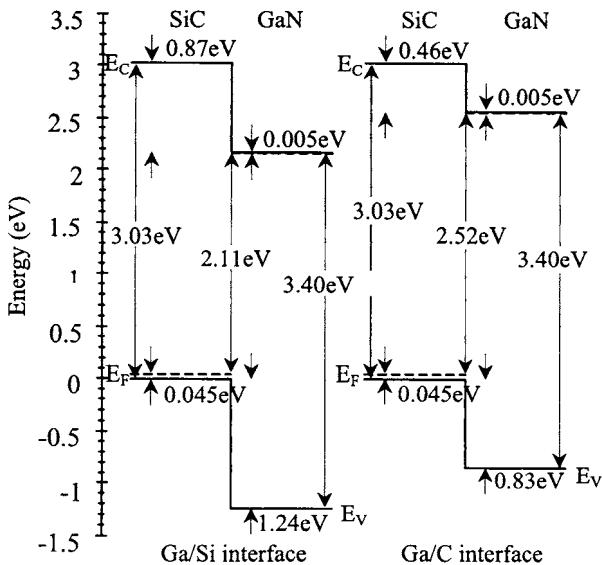


Fig. 14. Flatband energy diagram for the directly bonded GaN/SiC n-p heterostructures, with different interfacial polarity matching. This diagram is constructed from the measured built-in potential Φ_{bi} in CV characteristics. The zero energy is arbitrarily chosen at the top of the SiC valence band. E_F (broken line) is the Fermi level, and E_C and E_V (solid lines) are the conduction and valence bands,

interfacial charge effect is beyond the scope of this paper. The presence of interfacial charges is evident, but the knowledge of their influence on band alignment is still very limited.

4. Conclusion

In this research we have studied the application of the direct bonding technique for a novel material integration, namely the GaN/SiC materials system. We extensively examined the direct bonding of combinations of Ga-face GaN with C-face or Si-face SiC. The results from direct bonding of the different surfaces of SiC established that wet chemical cleaning prior to direct bonding is important. The feasibility of successful direct bonding depends on the pretreatment of the SiC. A SiC surface with a minimum amount of O on the surface can be fused with good reproducibility with GaN at 900°C. To obtain a minimum amount of O on the SiC surface an HF (10:1) 10 min dip was required for the Si-face SiC. For the C-face SiC, there was no specific change of the O amount by different HF concentration and this was attributed to a low electronegativity difference (1.0) between C and O. The reproducibility of the GaN/SiC bonding increased at 1000°C, but degradation of the GaN attributed to the dissociation of GaN was observed. The fact that the bonded area increased with the time duration at 900°C indicates that the bonding takes place by atomic rearrangement, and the amount of the atomic rearrangement is related to the annealing time.

The current-voltage characteristics of directly bonded GaN/SiC heterointerfaces have been investigated. Both GaN/SiC (Si-face) and GaN/SiC (C-face) interfaces were prepared by direct bonding. The properties of the GaN/SiC (Si-face) interfaces have been found to be very dependent on the choice of chemical treatments in the bonding

procedure. When a native oxide layer is present on the SiC surface during a GaN/SiC interface preparation, a significantly higher density of charged interface states is found, compared to the case when the native oxide layer is removed as the last step before the direct bonding. A model similar to the one for hydrophilic and hydrophobic Si/Si interfaces²¹ was used which explains the general electronic properties of the GaN/SiC (Si-face) interface. The measured current-voltage characteristics of the n-n interfaces can be explained by interface charges, which give rise to a potential barrier at the interface. For the bonded GaN/SiC (C-face) interfaces, low resistance I-V curves were found, indicating that a small amount of charge is present, which may be associated with the low amount of oxide during the direct bonding procedure. This latter structure is relatively insensitive to the different chemical treatments.

After determining the optimum bonding conditions (i.e. annealing temperature and cleaning process), the bonding technique was applied to obtain a layer transfer of GaN film from source substrate to target substrate. Although the lattice misfit between Si and GaN is large (i.e. 20%), Si was selected as the source substrate because of the ease of removal after bonding. After layer transfer of GaN to SiC an interfacial microstructure analysis, strain analysis and electrical characterization were completed for the GaN/SiC materials structure.

The interface microstructures of the GaN/SiC interface prepared by direct bonding were explored with HRTEM. The experimental results suggest that the high-temperature bonding results in a significant change of the interface morphology. Dislocations are observed in cross-sectional micrographs. The dislocations form to accommodate the lattice misfit and twist misorientation. For the GaN/SiC (Si-face) interface, the spacing of dislocations, ~10nm, indicate that it is the 1st network of dislocations. For the GaN/SiC (C-face) interface, the spacing of dislocations was ~6nm. We suggest that this is attributed to the overlap of the more closely spaced 2nd dislocation network (due to the large tilt misorientation, ~3°) to the 1st dislocation network (due to the lattice misfit, 3.4% and twist misorientation, 1~2°). An annealing at 900 °C for 60 minutes forms an interface layer, which is composed of a structurally ordered crystalline interface with about 30% of nanoscale, bubblelike amorphous or disordered regions. An amorphous layer of native oxide(s) may form at the interface due to incomplete removal of surface oxide prior to bonding. An atomically sharp interface without any interlayer, therefore, could be achieved by improving the surface preparation process, e.g., *in-situ* cleaning followed by an *in-situ* bonding.

The calculations of band offsets were accomplished by an empirical approach where band offsets result from the properties of the two components of the heterojunction and model calculations account for charge transfers across the interface. The temperature-dependent current-voltage and capacitance-voltage techniques were employed to determine the band offsets. The band offsets of directly bonded GaN/SiC n-p heterojunctions was compared with respect to the different interfacial polarity matching. Using of the modified Donnelly-Milnes theory³⁴, we conclude that direct bonding-induced polarity matching across the interface play a primary role in determining the GaN/SiC heterojunction potential step near the atomically “abrupt” interface. Besides the lattice misfit and misorientation, the polarity matching between directly bonded GaN/SiC heterojunctions is important. The Ga/Si interface showed larger band offsets ($\Delta E_C = 0.87 \pm 0.10$ eV and $\Delta E_V = 1.24 \pm 0.10$ eV) than the Ga/C interface ($\Delta E_C = 0.46 \pm 0.10$ eV and $\Delta E_V = 0.83 \pm 0.10$ eV).

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Electronic Properties of GaN (0001) – Dielectric Interfaces

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The characteristics of clean n- and p-type GaN (0001) surfaces and the interface between this surface and SiO₂, Si₃N₄, and HfO₂ have been investigated. Layers of SiO₂, Si₃N₄, or HfO₂ were carefully deposited to limit the reaction between the film and clean GaN surfaces. After stepwise deposition, the electronic states were measured with x-ray photoelectron spectroscopy (XPS) and ultraviolet photoemission spectroscopy (UPS). A valence band offset (VBO) of 2.0 ± 0.2 eV with a conduction band offset (CBO) of 3.6 ± 0.2 eV was determined for the GaN/SiO₂ interface. The large band offsets suggest SiO₂ is an excellent candidate for passivation of GaN. For the GaN/Si₃N₄ interface, type II band alignment was observed with a VBO of -0.5 ± 0.2 eV and a CBO of 2.4 ± 0.2 eV. While Si₃N₄ should passivate n-type GaN surfaces, it may not be appropriate for p-type GaN surfaces. A VBO of 0.3 ± 0.2 eV with a CBO of 2.1 ± 0.2 eV was determined for the annealed GaN/HfO₂ interface. An instability was observed in the HfO₂ film, with energy bands shifting ~ 0.4 eV during a 650 °C densification anneal. The electron affinity measurements via UPS were 3.0, 1.1, 1.8, and 2.9 ± 0.1 eV for GaN, SiO₂, Si₃N₄, and HfO₂ surfaces, respectively. The deduced band alignments were compared to the predictions of the electron affinity model and deviations were attributed to a change of the interface dipole. Interface dipoles contributed 1.6, 1.1 and 2.0 ± 0.2 eV to the band alignment of the GaN/SiO₂, GaN/Si₃N₄, and GaN/HfO₂ interfaces, respectively. It was noted that the existence of Ga-O bonding at the heterojunction could significantly affect the interface dipole, and consequently the band alignment in relation to the GaN.

Keywords: Electronic properties; GaN; dielectric interfaces.

1. Introduction

The bandgap of Al_xGa_{1-x}N can be engineered from 3.4 to 6.2 eV by varying the Ga to Al ratio in the material, and the GaN-AlN system is being studied extensively for applications in high-temperature, high-frequency, and high-power electronic devices. One area of significant research for any electronic device is the band alignment at a heterojunction interface. For these new materials, understanding the basic properties of the semiconductor surface and interfaces are required. In particular, the semiconductor-insulator (dielectric) interface is of significant interest for surface passivation and for the gate dielectric in field effect transistor (FET) device structures. The band alignment at a heterojunction defines the carrier transport or confinement properties of the potential device. As with all gate dielectrics, it is imperative that the barrier heights for electron and hole injection are sufficiently large to obtain low leakage currents. In this paper, we summarize our previous studies of the electronic properties of nitride-dielectric interfaces for both n- and p-type clean GaN.^{1,2,3}

The modeling of interface formation dates back to 1938, when Schottky and Mott independently introduced a model for determining the band lineup for metal-semiconductor heterostructures. The Schottky-Mott model for the formation of a metal-semiconductor heterojunction is based on the work function of the metal and the electron affinity of the semiconductor. The work function of the metal is the difference in energy from the Fermi level to the vacuum level, while the electron affinity is defined as the energy difference between the conduction band minimum and the vacuum level. According to the Schottky-Mott model, as the metal and semiconductor are brought into intimate contact, the relative positions of the metal Fermi level and the energy bands of the semiconductor remain the same at the interface.

This model for metal-semiconductor interfaces can be extended to semiconductor-semiconductor or semiconductor-insulator heterojunctions. The electron affinity model (EAM), put forth by Anderson,⁴ describes the band discontinuities that form when two semiconductors are brought into intimate contact. According to the model, the energy levels of the respective materials align at the vacuum level, resulting in a conduction band offset equal to the difference in the electron affinities of the materials:

$$\phi_{CBO} = (\chi_1 - \chi_2) \quad (1)$$

where χ_1 and χ_2 represent the electron affinity of each material. This result, along with knowledge of the respective bandgap of each material allows determination of the valence band offset to be:

$$\phi_{VBO} = (E_{g,2} - E_{g,1}) - (\chi_1 - \chi_2) \quad (2)$$

where $E_{g,1}$ and $E_{g,2}$ are the respective bandgaps of each material. Type I and type II band alignment are shown schematically in Figure 1 with the assumption the electron affinity model describes the heterojunction.

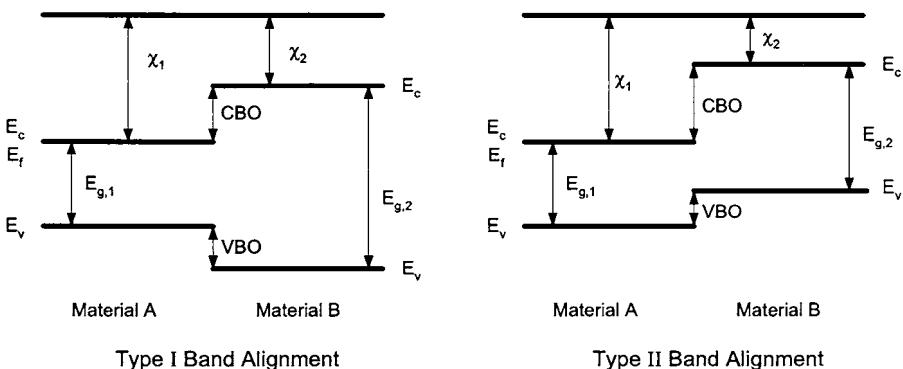


Fig. 1. Heterojunction band lineups for materials A and B, with type I and type II band alignment represented.

A first approach to describing a heterostructure interface is to apply the electron affinity model. This model holds in the ideal case, assuming there is no potential created as the heterostructure is formed. A model described by Tersoff^{5,6} based on metal induced gap states draws a connection between the metal-semiconductor junction and the semiconductor-semiconductor interface. The basic idea behind Tersoff's model is that the wave functions of the electrons in the metal extend across the interface and generate states in the gap. The effect of gap states at the interface is to screen any deviation from the canonical lineup by a characteristic dielectric constant, therefore pinning the Fermi level to maintain local charge neutrality.

Based on this concept, a model based on the charge neutrality levels (CNL) has been used to describe the band alignment of a heterojunction interface between two semiconductors. It has been proposed that heterojunction band alignments are determined by alignment of the charge neutrality levels (CNL) of the two materials. The

charge neutrality levels represent the branch point of the surface or interface states related to the valence or conduction band. Thus a neutral interface would have a Fermi level at the branch point. The presumption is that charge can transfer between the interface states of the two materials, which will cause an interface dipole. If the density of states is high or if the CNL of the two semiconductors are at similar relative energies, then the band offset will be determined by the relative position of the CNL of the two materials.

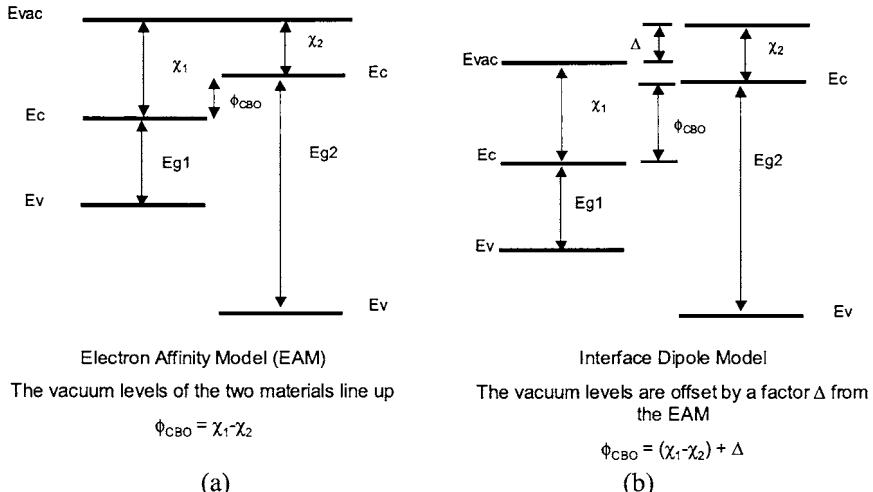


Fig. 2. Heterojunction band lineups representing the electron affinity model (a) and the interface dipole model (b). The interface dipole, Δ , is shown in Figure 2.2b.

Recently, Robertson⁷ adapted the interface defect model presented by Cowley and Sze¹⁰ to employ the CNL as the pinning levels. Robertson⁷ employed the S parameter, which reflects the dielectric screening, to relate the relative contribution of the electron affinity model and the dipole from the charge neutrality levels. Empirically, Monch^{8,9} found that S obeys the following relation:

$$S = \frac{1}{1 + 0.1(\epsilon_\infty - 1)^2} \quad (3)$$

where ϵ_∞ is the dielectric constant of a given material. The model was applied to analyze the band alignment of a range of oxides on silicon, and the model seems consistent with most experimental results. In this model, charge transfer across the interface creates a dipole, which modifies the band lineup given by the electron affinity rule and is described by the relation:

$$\phi_{CBO} = (\varphi_{CNL1} - \varphi_{CNL2}) - (E_{g,1} - E_{g,2}) + S\{(x_1 - x_2) + (E_{g,1} - E_{g,2}) - (\varphi_{CNL1} - \varphi_{CNL2})\} \quad (4)$$

where ϕ_{CBO} is the CBO, χ and ϕ_{CNL} are the electron affinities and charge neutrality levels for each semiconductor (a and b), and S is a pinning factor based on the dielectric properties of the materials. Here, the ϕ_{CNL} is defined relative to the VBM of each semiconductor. A value of S=1 represents the EAM while a value of 0 represents pinning at the CNL levels. Figure 2 presents a heterojunction lineup with and without a change in the interface dipole, corresponding to the electron affinity model and to the charge neutrality model, respectively. The focus of our research is to use photoemission to measure the band offsets and to observe a change in the interface dipole at the interface as the heterostructure is formed.

2. In situ characterization techniques

Photoemission techniques have been extensively employed to characterize the electronic states of surfaces and interfaces. Because the technique is surface sensitive, it is ideally applied as an in situ approach where photoemission spectra are acquired immediately after surface preparation and/or interface formation.

X-ray photoelectron spectroscopy employs x-rays as the photon source, with the most common being Mg k_α (1253.6 eV) and Al k_α (1486.6 eV). The purpose of the high energy x-rays is to excite core level electrons from deep within the atom. This technique is surface sensitive due to the escape depth of the electrons that are not scattered. Theoretical calculations and measurements show the escape depth for electrons excited by XPS is approximately 25 to 35 Å.⁸ The emitted electrons have energies representative of the elements they originated from while the scattered electrons originate from deeper in the sample and represent the broad background normally observed in photoemission spectra. The data obtained in XPS is typically represented in a plot of electron counts vs. binding energy. The binding energy of an electron can be related to the kinetic energy of the emitted electron by the relation:

$$BE = h\nu - KE \quad (5)$$

where $h\nu$ is the photon energy, and KE is the kinetic energy of the electron.

While high energy photons are necessary to excite core level electrons, the use of a low energy photon source allows information about valence band electrons to be obtained. UPS employs ultraviolet light generated from a gas discharge lamp. While several gases can be used, helium is the most common. The helium plasma generated creates two useful discharge energies: He I (21.2 eV) and He II (40.8 eV). The relatively low electron mean free path generated by the low photon energy allows valence band information to be obtained. Similar to XPS, UPS spectra is represented as intensity vs. binding energy, with the zero value usually set to that of the Fermi level. In addition to measuring the valence band states, UPS can also be useful for measuring the electron affinity of a material by tracking the low-energy cut-off (vacuum level). The electron affinity can be deduced from the relation:

$$\chi = h\nu - W - E_g \quad (6)$$

where $h\nu$ is the photon energy, W is the spectral width measured from the valence band turn on the low energy cut-off, and E_g is the bandgap of the material.

The use of photoemission to discern band discontinuities is a well-established method that has been reported in the literature.^{9,10,11} The method for determining the valence band discontinuity is similar to that of Waldrop and Grant¹⁷ and Kraut et al,¹⁸ which is represented in the following relation for the valence band offset:

$$\Delta E_{VBO} = \Delta E_{CL} + (E_{core}^1 - E_V^1) - (E_{core}^2 - E_V^2) \quad (7)$$

where $E_{core}^{1,2}$ is the core level energy of each material, $E_V^{1,2}$ is the valence band energy of each material, and $\Delta E_{CL} = (E_{core}^2 - E_{core}^1)$ is the difference in energy between the core levels of the two materials. Their basic approach is to reference the VBM to a core level in the XPS spectra for each semiconductor and to use the measured difference between the core level energies to discern the band discontinuities. In our studies, we have employed UPS to measure the energy of the VBM from the Fermi level, and XPS is used to measure core level energies relative to the Fermi level.

Specifically, XPS and UPS were employed after cleaning to measure initial core level positions and the valence band turn-on position, respectively. These measurements serve as a baseline with which to compare successive measurements. A sequential process involving the careful formation of a thin dielectric on the surface of the clean GaN is conducted until emission from the substrate can no longer be measured. XPS and UPS measurements are obtained after each step of the process, and the band bending is deduced from the shifts of the gallium and nitrogen core levels. The band offsets and electron affinities are determined from the UPS spectra, and the formation of the oxide and the value of the interfacial dipole are determined from the XPS and UPS measurements.

3. Band Offsets of SiO₂ – GaN(0001)

Several groups have reported the electrical characteristics of the SiO₂-GaN interface grown by plasma enhanced chemical vapor deposition (PECVD). Casey *et al*¹² found no observable hysteresis in room temperature C-V measurements, as well as an increase of capacitance with incident ultraviolet light while in deep depletion. These observations are consistent with a low concentration of interface traps. M. Sawada *et al*¹³ and Arulkumaran *et al*¹⁴ support this observation, measuring $1\text{-}2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ and $2.5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, respectively for the minimum interface state density at the SiO₂-GaN interface. T. Sawada *et al*¹⁵ investigated the effect of thermal annealing of the interface. The interface state density was reduced 33 % to $2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ after annealing in H₂ at 500 °C. Also noted was that the Fermi level was not pinned and could move within the upper band gap. The as-deposited sample had a Fermi level 0.2 eV from the conduction band edge under thermal equilibrium conditions, and the value increased to 0.5 eV after annealing. The relatively low interface trap density suggests the promise of applications for this interface.

In this research, *in situ* x-ray photoelectron spectroscopy (XPS) and ultra violet photoemission spectroscopy (UPS) measurements are used to determine the band discontinuities, or band offsets, at the GaN-SiO₂ interface. After achieving an atomically clean GaN (0001) surface, care is taken to avoid oxidation during the process. Our basic approach in this study is to obtain a clean GaN surface through an ammonia exposure at

an elevated temperature and to form an SiO_2 layer by depositing silicon and to employ low temperature oxidation to minimize disruption of the interface.

Care was taken to avoid oxidation of the clean GaN surface after the ammonia clean. A significant Ga_2O_3 layer at the interface can be a source of deep acceptors and interface states that can be detrimental to device fabrication.¹⁶ Although gallium oxide was not observed within our detection limits, we expect that Ga-O bonding exists at the SiO_2 -GaN interface. Therrien *et al*¹⁷ reported the significance of an ultra-thin Ga_2O_3 layer formation, which allowed a redistribution of electronic charge and reduction of the interfacial defect density.

The Ga face GaN (0001) is a polar surface, and the spontaneous polarization will lead to a negative bound charge at the GaN film surface and a positive bound charge at the back substrate interface. The GaN is also piezoelectric, but because the films are grown above the critical thickness there is only a small residual strain, and the piezoelectric induced polarization ($P_{pz}=0.002 \text{ C/m}^2$) is small in comparison to the spontaneous polarization ($P_{sp}=0.033 \text{ C/m}^2$).¹⁸ The piezoelectric polarization for biaxial tensile strain contributes in the same direction as the spontaneous polarization. The negative surface bound charge is compensated by surface states and screened by ionized donors while the positive bound charge at the substrate interface is screened by the free carriers. The polarization bound charge screened by the ionized donors would lead to upward band bending at the GaN surface. We note that the XPS measurements of the Ga and N core levels would be shifted by the polarization fields, but all measurements of the band offsets are made relative to these values, and thus the measured band offsets should not be affected by polarization induced band bending. Moreover, since the strain is relatively small, the effect of strain on the band offsets is anticipated to be less than the experimental uncertainties in our measurements.¹⁹

Figure 3 shows the proposed band lineups for the n-type GaN- SiO_2 interface. The decrease of 0.3 eV band bending from the clean surface indicates essentially flat band conditions are achieved. The valence band offset determination is the measured UPS turn-on for SiO_2 (5.3 eV), minus the GaN turn-on (3.0 eV), minus the change in band bending (0.3 eV). With this value and the knowledge of the bandgap of the material, the conduction band offset is obtained. The bandgap of SiO_2 has been widely reported to be 9.0 eV,^{20,21,22} and this value was used for the conduction band offset and electron affinity calculations. From our experiment, the valence band offset is deduced to be 2.0 eV, and the conduction band offset is 3.6 eV.

The p-type GaN- SiO_2 band lineup is represented in Figure 4. For the clean surface, the measured downward band bending and electron affinity were calculated to be 1.3 ± 0.1 eV and 3.2 ± 0.1 eV, respectively, assuming the Mg acceptor level lies ~ 300 meV above the VBM and a room temperature bandgap of 3.4 eV.²³ Using the considerations mentioned above, the valence band offset was calculated to be 2.0 eV, and the conduction band offset of 3.6 eV.

The electron affinity levels for GaN and SiO_2 are represented in Figures 3 and 4. The electron affinity model of heterojunction formation predicts these levels to align at the interface. Our results show a deviation from the electron affinity model of 1.8 eV for the n-type GaN substrate and 1.5 eV for the p-type GaN substrate.

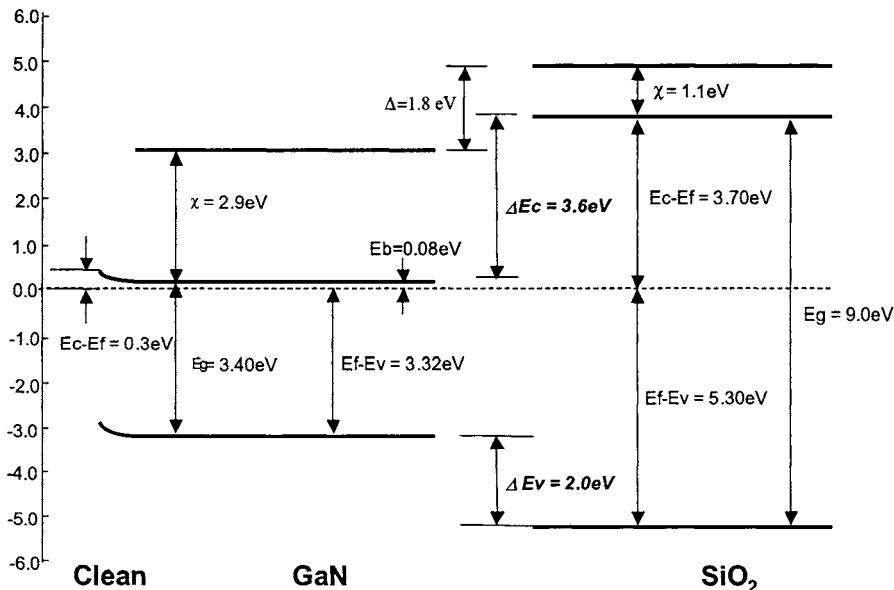


Fig. 3. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and SiO₂. The valence band offset, ΔE_V , conduction band offset, ΔE_C , band bending, and interface dipole, Δ , are represented.

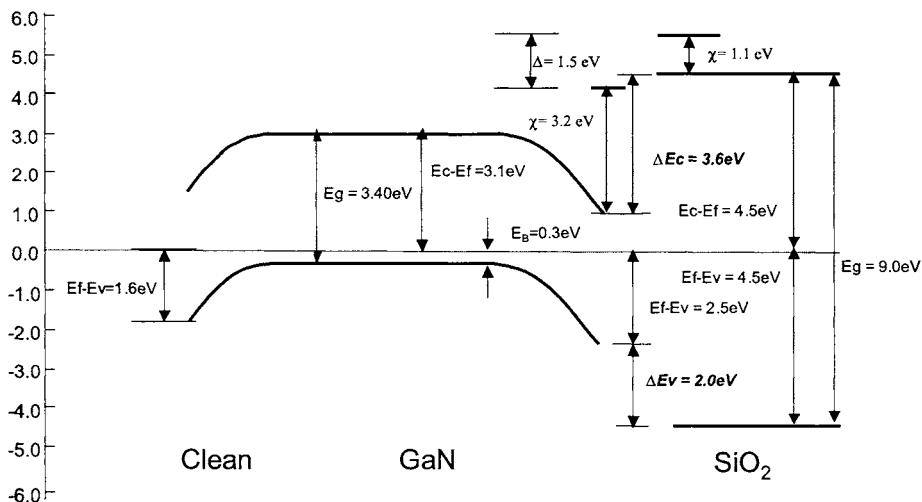


Fig. 4. Deduced bands for the clean p-type GaN surface (left) and the interface between p-type GaN and SiO₂. The valence band offset, ΔE_V , conduction band offset, ΔE_C , band bending, and interface dipole, Δ , are represented.

The electron affinity model is based on the premise that the interface is formed without disruption of the surface electronic states of either of the two materials. All reference is to the vacuum levels of the two materials. The measured difference between the prediction of the electron affinity model and the experimentally observed band offset represents a change in the interface dipole. In general, it is not possible to assign a specific interface dipole to the heterostructure, but it is reasonable to consider the change in interface dipole from that deduced by the electron affinity model. However, the relation to the vacuum level in the first place is somewhat arbitrary. While the electron affinity of a surface can be determined following the approach employed in this study, it is dependent on the details of the surface structure where surface reconstruction, steps, and adsorbates can cause changes of the electron affinity by several eV. Moreover, after interface formation, the vacuum level of the materials at the interface is not defined or measurable, and the interface structure may have little relation to the specific bonding of the free surface that was responsible for the value of the electron affinity.

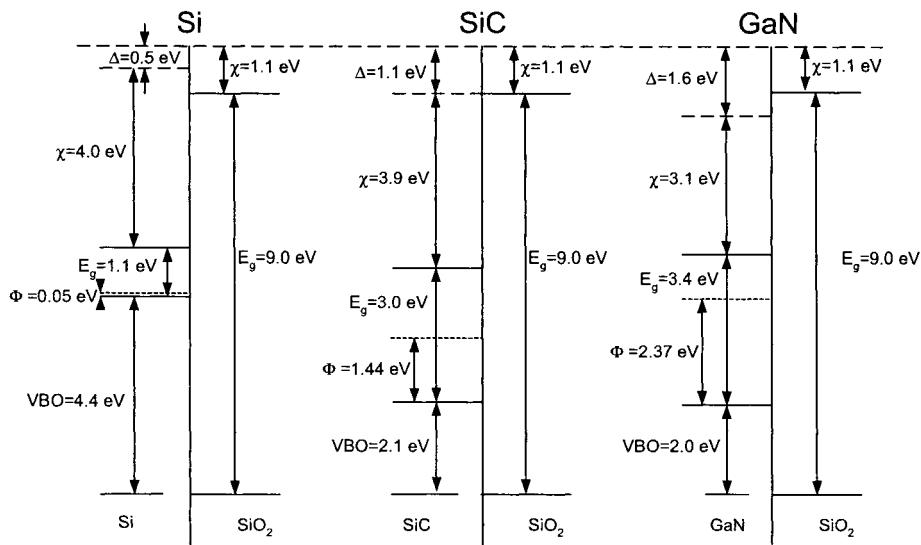


Fig. 5. Band alignment of Si/SiO₂, SiC/SiO₂, and GaN/SiO₂ interfaces. The dashed line at the top of the figure corresponds to the electron affinity of the SiO₂ surface, which is common in all three interfaces. The deviation from the electron affinity model is shown as Δ , and the charge neutrality level (CNL) is indicated as a dashed line within the band gap. The VBO are determined from the measurements and Δ is taken as an average of results from *p* and *n*-type GaN.

As an alternative to the electron affinity model, it has been proposed that heterojunction band alignments are determined by alignment of the charge neutrality levels (CNL) of the two materials. To our knowledge, the CNL of SiO₂ has not been reported, and because of the high value of S for the SiO₂-Si interface (0.86),⁷ we cannot use the experimental results of the Si/SiO₂ interface to reliably place the SiO₂ CNL.

In an attempt to understand the relation of our measured band alignment and the different models for heterostructure band alignment, we have compared our measured interface alignments to experimental results for SiO₂ on Si and SiO₂ on SiC in Figure 11. In each case the diagrams are aligned to the vacuum level at the SiO₂, which has been

measured to be at the same energy relative to the oxide bands. The bandgap of each material is indicated, as is the VBO. The position of the vacuum level of the clean surface of the semiconductor is indicated, and the difference between these values and the surface vacuum level is the deviation from the EAM. This difference represents the change in the interface dipole, and was found to be 0.5, 1.1, and 1.6 eV for SiO₂ on Si, SiC or GaN, respectively.

Also indicated in Figure 5 is the CNL of the semiconductors based on prior reports.^{7,24} We find that the CNL of the Si and the GaN are in relative alignment with respect to the SiO₂ band gap, but the CNL of the SiC falls substantially below these values. The variation of the CNL model for these three interfaces may be anticipated by the wide bandgap and the high value of S of the SiO₂.

The progression of the interface dipole deduced from the deviation from the EAM is most likely related to the changes at the semiconductor surface since the oxide is the same in all cases. For the SiO₂/Si interface, the surface reconstruction of the Si is not expected to survive the bonding and this effect alone could account for the change in the interface dipole. The same might be true for the SiO₂/SiC interface where the increased interface dipole could also represent the charge transfer from the Si to the nearest neighbor C atoms. For both Si and SiC, the oxide interface layer is expected to contain Si-O bonding. For the SiO₂/GaN interface, Ga-O bonding is expected at the interface. With the Ga atomic layer more positive and the O layer more negative, the interface dipole would be expected to lower the GaN electronic levels with respect to the SiO₂ levels, which is consistent with our observations.

4. Band Offsets of Si₃N₄ - GaN (0001)

Recent studies of the electrical properties of the Si₃N₄/GaN interface by Arulkumaran *et al*¹⁴ and Nakasaki *et al*²⁵ have reported interface trap densities of 6.5×10^{11} eV⁻¹cm⁻² and 5.0×10^{11} eV⁻¹cm⁻² with clear deep depletion behavior. Chang *et al*²⁶ found that silicon nitride passivation enhances light output and increases the reliability of GaN-based light emitting diodes by reducing the leakage current. Electrical data in the literature indicates the promise of advanced GaN metal-insulator-semiconductor (MIS) devices.^{14,25,26} While several groups have employed photoemission techniques to study GaN/metal interfaces,^{27,28,29} only Nakasaki *et al*²⁵ report band offsets for GaN/Si₃N₄ interfaces. They report type I band alignment with a valence band offset of 1.0-1.2 eV for the Si₃N₄/GaN(0001) interface.

The main focus of our experiment is to measure the band offsets and to explore the interface dipole at the heterostructure interface. Our basic approach in this study is to obtain clean GaN surfaces through an ammonia exposure at elevated temperatures and to form an Si₃N₄ layer by depositing silicon on the clean surface followed by a low temperature ECR plasma nitridation. The XPS and UPS measurements are obtained after each step in the process, yielding the band bending from the shifts in the gallium 3d and 3p core levels, and the band offsets and electron affinities are deduced from the UPS spectra.

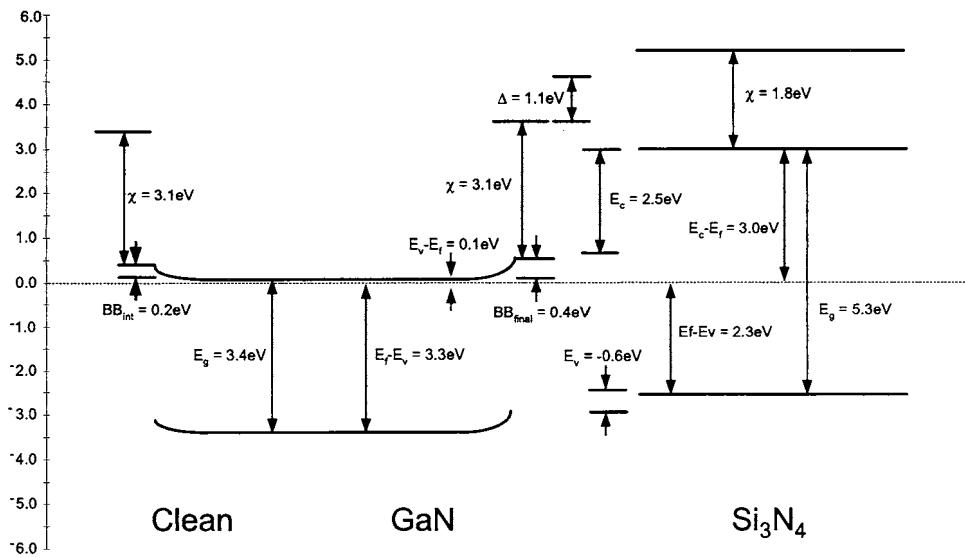


Fig. 6. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and SiO_2 . The valence band offset, E_v , conduction band offset, E_c , band bending, and interface dipole, Δ , are represented.

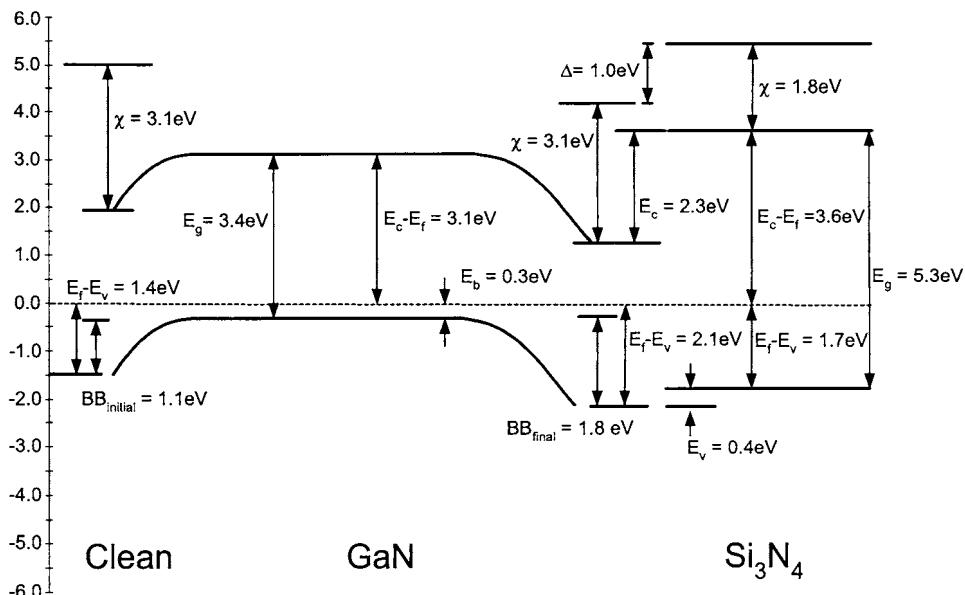


Fig. 7. Deduced bands for the clean p-type GaN surface (left) and the interface between p-type GaN and SiO_2 . The valence band offset, E_v , conduction band offset, E_c , band bending, and interface dipole, Δ , are represented.

Figure 6 shows the proposed band lineups for the n-type GaN/Si₃N₄ interface. The VBO determination is the measured UPS turn-on for GaN (3.1 eV), minus the Si₃N₄ turn-on (2.3 eV), minus the band bending (0.2 eV). This value, along with knowledge of the bandgap of the material, allows the CBO to be deduced. The VBO is found to be type II band alignment, where the valence band of the Si₃N₄ is 0.6 ± 0.1 eV above the GaN VBM, and the CBO is 2.5 eV. Figure 7 shows the proposed band lineups for the p-type GaN/Si₃N₄ interface. The UPS turn-on for the clean GaN and the Si₃N₄ was observed at 1.4 eV and 1.7 eV, respectively. XPS spectra showed a change in downward band bending of ~0.7eV during formation of the interface. The VBO is again found to be type II band alignment at 0.4 ± 0.1 eV above the GaN VBM, and the CBO is 2.3 eV.

The measured electron affinities for GaN and Si₃N₄ are represented in Figures 6 and 7. Our results show a deviation from the EAM of 1.1 eV and 1.0 eV for the n-type GaN and p-type GaN substrates, respectively.

As an alternative to the electron affinity model, it may be considered that the heterojunction band offsets are determined by alignment of the charge neutrality levels of the two materials. To our knowledge, the CNL of Si₃N₄ has not been reported. Using the value of S for the Si₃N₄-Si interface (0.51) and the measured band offset from previous work,^{7,30} we can deduce the CNL of Si₃N₄ to be 1.5 eV above the valence band maximum. While more research is necessary to assign a CNL value for Si₃N₄, it is reasonable to consider this prediction of the valence band offset for comparison to our experimental results. Monch²³ has reported the CNL of GaN to be 2.37 eV above the valence band maximum. Though the dielectric screening parameter S has not been determined for the GaN/Si₃N₄ interface, in the limits of S=0 and S=1 the valence band types and offsets would be type II 0.9 eV and type I 0.9 eV, respectively. If the assumption is made that the parameter S is similar to that for the Si/Si₃N₄ interface (0.51), the CNL relation given in Eq. 5 predicts the valence band offset to be ~0.1eV (essentially no offset) for the GaN/Si₃N₄ interface. Conversely, the dielectric screening parameter can be deduced for the interface using our results and the CNL of GaN and Si₃N₄. A value of S=0.26 is obtained for the GaN/Si₃N₄ interface.

This prediction, as well as our results, are significantly different from the results by Nakasaki *et al.*²⁵ who report type I band alignment with an offset of 1.0-1.2eV for the GaN/Si₃N₄ interface. A factor that could play a major role in this difference is the cleaning method used for the GaN. Their studies used an NH₄OH etch and a combination of H₂ and N₂ plasmas for *in situ* surface preparation. While the oxygen content was greatly reduced from the as-loaded case, a significant amount remained after surface preparation, suggesting Ga-O bonding.²⁵ As noted in the previous section,¹ the GaN/SiO₂ interface shows type I alignment and a VBO ~2 eV. We suggested that Ga-O bonding exists at the GaN/SiO₂ interface and contributes to the large offset and interfacial dipole change. Our study begins with a clean GaN surface (contamination levels of <1% for oxygen and carbon) that allows the GaN/Si₃N₄ interface to be measured more precisely.

In an attempt to understand the relation of our measured band alignment and the different models for heterostructure band alignment, in Figure 8 we have compared our measured interface alignments to experimental results for Si₃N₄ on Si.^{7,30,31} In both cases the diagrams are aligned to the vacuum level at the Si₃N₄, which has been measured to be at the same energy relative to the silicon nitride bands. The bandgap of each material is indicated, as is the VBO. The position of the vacuum level of the clean semiconductor surface is indicated, and the difference between these values and the surface vacuum level is the deviation from the EAM. This difference represents the change in the

interface dipole, and was found to be 0.5 and 1.2 eV for Si_3N_4 on Si and GaN, respectively.

Also indicated in Figure 8 is the CNL of the semiconductors.^{7,23} Additionally, the predicted CNL of Si_3N_4 (1.5 eV) deduced as described above is also represented. We observe that the CNL's nearly align for the GaN/ Si_3N_4 interface, suggesting the correlation of this interface with the CNL model with a low dielectric screening parameter S. The progression of the interface dipole deduced from the deviation from the EAM is most likely related to the changes at the semiconductor surface since the silicon nitride is the same in both cases. For the Si/ Si_3N_4 interface, the Si surface reconstruction is expected to change during the formation of the nitride layer. This effect alone could account for the small change in the interface dipole, and the same could be true for the GaN/ Si_3N_4 interface. For GaN/ Si_3N_4 , we expect N-Ga-N-Si bonding to exist within the first few monolayers at the heterojunction interface. Because of the similarity in bonding at the interface we may expect a smaller interface dipole than that of the GaN/ SiO_2 interface. Indeed, this is the case where we find a 1.1 ± 0.1 eV change due to the interface dipole for GaN/ Si_3N_4 and a 1.6 ± 0.1 eV for the GaN/ SiO_2 interface.

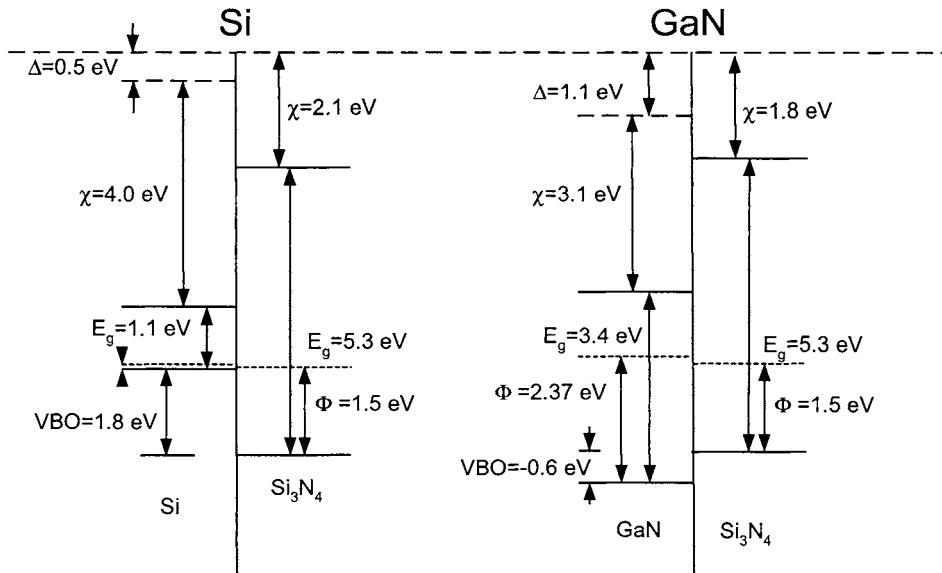


Fig. 8. Band alignment of Si/ Si_3N_4 and GaN/ Si_3N_4 interfaces. The dashed line at the top of the figure corresponds to the electron affinity of the Si_3N_4 surface, which is common in both interfaces. The deviation from the electron affinity model is shown as Δ , and the charge neutrality level (CNL) is indicated as a dashed line within the band gap. The VBO are determined from the measurements and Δ is taken as an average of results from *p* and *n*-type GaN.

5. Band Offsets of HfO_2 - GaN(0001)

Studies of HfO_2 dielectric films began in the 1970's for optical coatings and DRAM applications. Balog *et al*²² performed C-V measurements on CVD grown HfO_2 films on Si (100) and found no observable hysteresis and a minimum interface state

density of $\sim 1.6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. Additionally, the dielectric constant was measured to be $\kappa=22-25$ at 1 MHz, with a breakdown field of $\sim 4 \text{ MV/cm}$. Lee *et al*³³ found leakage currents $< 3 \times 10^{-2} \text{ A/cm}^2$ at -1.5 V for HfO₂ films on Si (100) with a capacitance equivalent oxide thickness of $\sim 10 \text{ \AA}$. Kirsch *et al*³⁴ investigated the effect of a nitride layer at the HfO₂/Si interface. At 1 V, leakage currents of 4×10^{-5} and $4 \times 10^{-3} \text{ A/cm}^2$ were measured for $\sim 50 \text{ \AA}$ HfO₂ capacitors fabricated with and without SiN_x, respectively. Properties such as high dielectric constant, low leakage current, and relatively low interface density suggest the promise of HfO₂ in electronic device fabrication.

In this study, *in situ* XPS and UPS measurements are again used to determine the band discontinuities, or band offsets, at the GaN-SiO₂ interface. After achieving an atomically clean GaN (0001) surface, care is taken to avoid oxidation during the process. Our basic approach is to obtain a clean GaN surface through an ammonia exposure at an elevated temperature and to form an HfO₂ layer by depositing hafnium and to employ low temperature oxidation to minimize disruption of the interface. Although gallium oxide was not observed within our detection limits, we expect that Ga-O bonding exists at the HfO₂-GaN interface.

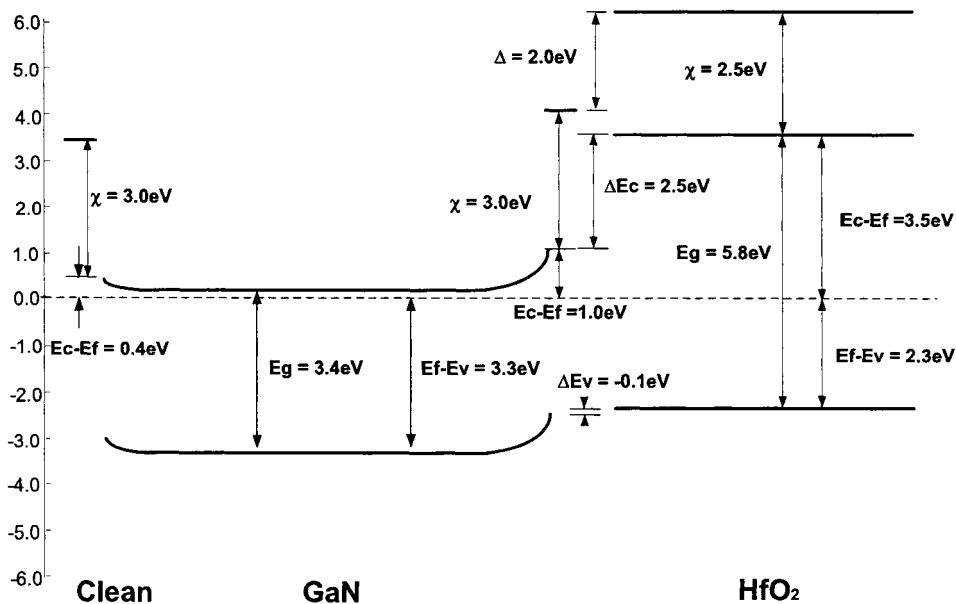


Fig. 9. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and HfO₂ before annealing. The valence band offset, ΔE_V , conduction band offset, ΔE_C , band bending, and interface dipole, Δ , are represented.

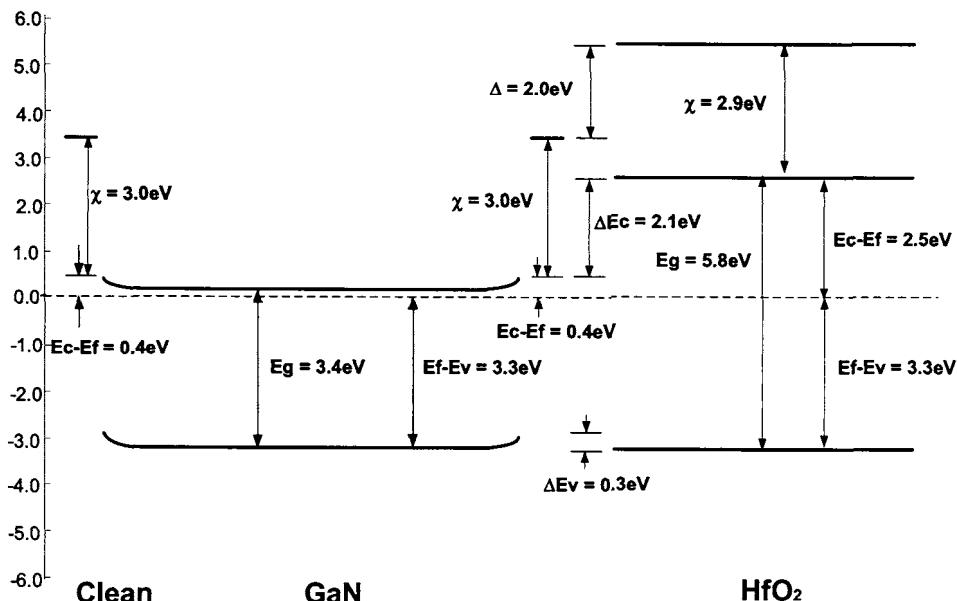


Fig. 10. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and HfO₂ after annealing at 650 °C. The valence band offset, ΔE_v , conduction band offset, ΔE_c , band bending, and interface dipole, Δ , are represented.

Figure 9 shows the proposed band lineups for the as-grown n-type GaN-HfO₂ interface. The increase of 0.6 eV band bending from the clean surface as the interface is formed is shown. The valence band offset determination is the measured UPS turn-on for the HfO₂ on the GaN (2.3 eV), minus the GaN turn-on (3.0 eV), plus the change of band bending (0.6 eV). With this value and the knowledge of the bandgap of the material, the conduction band offset is obtained. The bandgap of HfO₂ has been reported to be 5.7-6.0 eV.^{7,35,36} A value of 5.8 eV was used for the conduction band offset and electron affinity calculations. The valence band offset is deduced to be -0.1 eV (type II), and the conduction band offset is 2.5 eV for our as-deposited GaN/HfO₂ interface.

Figure 10 shows the proposed band lineups for the n-type GaN-HfO₂ interface after annealing at 650 °C. The valence band offset determination is the measured UPS turn-on for the HfO₂ on the GaN (3.3 eV), minus the GaN turn-on (3.0 eV), plus the change of band bending (0.0 eV). From our annealed interface experiment, the valence band offset is deduced to be 0.3 eV, and the conduction band offset is 2.1 eV.

Annealing above 600 °C is often required for densification of oxide films.^{37,38} Deposition of HfO₂ on the clean GaN resulted in a Ga 3p core level shift from 105.8 eV to 105.2 eV, indicative of downward band bending as the film was deposited. An anneal to 650 °C shifted the core level to 105.8 eV, bending the energy bands upward. Subsequent HfO₂ film depositions and anneals resulted in a Ga 3p energy levels of 105.2 and 105.8 eV, respectively. Depositing and subsequently annealing the sample could move the Ga 3p core level positions, and therefore the change in band bending, between the two energy positions. This result suggests a thermodynamic instability of the hafnium oxide film as the GaN/HfO₂ interface is formed.

The electron affinity levels for GaN and HfO₂ are represented in Figures 9 and 10. Our results show a deviation from the electron affinity model of 2.0 eV both before and after annealing, for the GaN-HfO₂ interface.

In an attempt to understand the relation of our measured band alignment and the different models for heterostructure band alignment, in Figure 11 we have compared our measured alignments for the annealed interface to experimental results for HfO₂ on Si.⁷ In both cases the diagrams are aligned to the vacuum level at the HfO₂, which has been measured to be at the same energy relative to the oxide bands. The bandgap of each material is indicated, as is the VBO. While the Si-HfO₂ interface does not present a deviation from the electron affinity model, the GaN-HfO₂ interface has a change in interface dipole of 2.0 eV. Also indicated in Figure 8 is the CNL of the semiconductors based on prior reports.^{7,23} We find that the CNL of the Si and the GaN are not in relative alignment with respect to the HfO₂ band gap. The *S* parameter in Eq. 4 was deduced from experimental results for the GaN/HfO₂ interface. A value could not be found for the dielectric screening between either extreme (0 to 1) for *S*, suggesting that a more complex analysis is required.

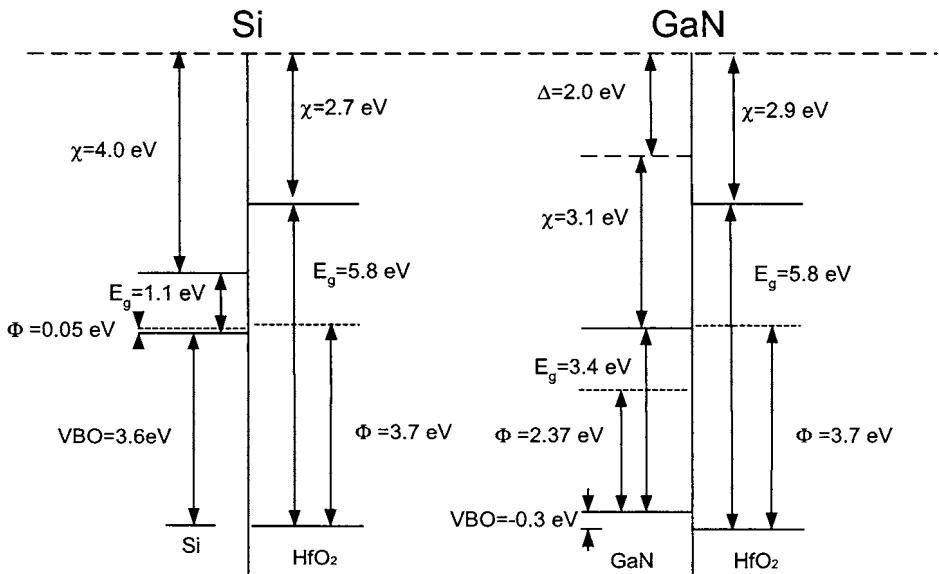


Fig. 11. Band alignment of Si/HfO₂ and GaN/HfO₂ interfaces. The dashed line at the top of the figure corresponds to the electron affinity of the HfO₂ surface, which is common in all three interfaces. The deviation from the electron affinity model is shown as Δ , and the charge neutrality level (CNL) is indicated as a dashed line within the band gap. The VBO are determined from the measurements.

The progression of the interface dipole deduced from the deviation from the EAM is most likely related to the changes at the semiconductor surface since the oxide is the same in both cases. For the GaN-HfO₂ interface, Ga-O bonding is expected at the interface. With the Ga atomic layer more positive and the O layer more negative, the interface dipole would be expected to lower the GaN electronic levels with respect to the

HfO_2 levels, which is consistent with our observations. In support of this explanation, we note that the interface dipole deduced from the GaN/SiO_2 interface is 1.6 eV with Ga-O bonding expected at the interface.³⁸

6. Summary

The surfaces and heterojunction interfaces of GaN were examined by x-ray and UV photoemission spectroscopy. The substrates used in these experiments were n- and p-type Ga-face GaN grown on 6H-SiC with an AlGaN buffer layer. The SiO_2 , Si_3N_4 , and HfO_2 were prepared using oxidation and nitridation plasma techniques to minimize disruption of the GaN surface.

UPS was used to measure the valence band maximum and the spectral width of the material, which allows the electron affinity to be calculated. A combination of XPS and UPS measurements provides a more complete understanding of the band alignment of the heterostructure. Table 1 contains a summary of the electronic properties obtained for the GaN/SiO_2 , $\text{GaN}/\text{Si}_3\text{N}_4$, GaN/HfO_2 interfaces and respective surfaces. XPS was used to measure band bending as the interface is formed.

Table 1. Summary of electronic properties of dielectric – GaN interfaces. BB and EA are band bending and electron affinity, respectively. The initial BB represents the clean surface, and the Interface BB represents the band bending after the interface has formed. The positive or negative sign on the band bending represents upward or downward band bending, respectively. The negative values for the VBO represents type II band alignment. The interface dipole represents the deviation from the EAM.

| Material | Initial BB | Interface BB | VBO | CBO | EA (GaN) | EA (dielect.) | Interface Dipole |
|---|---------------|-----------------|------|-----|-------------|------------------|---------------------|
| n-GaN/ SiO_2 | 0.3 | 0.0 | 2.0 | 3.6 | 2.9 | 1.1 | 1.8 |
| p-GaN/ SiO_2 | -1.3 | -2.2 | 2.0 | 3.6 | 3.2 | 1.1 | 1.5 |
| n-GaN/ Si_3N_4 | 0.2 | 0.4 | -0.6 | 2.5 | 3.1 | 1.8 | 1.1 |
| p-GaN/ Si_3N_4 | -1.1 | -1.8 | -0.4 | 2.3 | 3.1 | 1.8 | 1.0 |
| n-GaN/ HfO_2 (as deposited) | 0.3 | 0.9 | -0.1 | 2.5 | 3.0 | 2.5 | 2.0 |
| n-GaN/ HfO_2 (annealed) | 0.3 | 0.3 | 0.3 | 2.1 | 3.0 | 2.9 | 2.0 |

The valence and conduction band offsets for the GaN/SiO_2 interface were 2.0 and 3.6 eV. The (averaged) electron affinities of the GaN and SiO_2 surfaces were measured to be 3.0 and 1.1 eV, respectively. A deviation from the electron affinity model of ~1.6 eV was observed, which was ascribed to a change in the interface dipole. Band alignment measurements predict SiO_2 should passivate both n- and p-type GaN surfaces, making it an excellent choice for device fabrication.

For the $\text{GaN}/\text{Si}_3\text{N}_4$ interface, the (averaged) valence and conduction band offsets were ~0.5 and ~2.4 eV. The interface represents type II band alignment, where the valence band of the GaN lies below the valence band of the Si_3N_4 . The electron affinities of each material were measured to be 3.1 and 1.8 eV. An interface dipole of ~1.1 eV was deduced for the $\text{GaN}/\text{Si}_3\text{N}_4$ interface. These measurements predict that Si_3N_4 should passivate n-type GaN surfaces, but may not be appropriate for p-type surfaces.

The valence and conduction band offsets for the annealed GaN/HfO_2 interface were found to be 0.3 and 2.1 eV. The electron affinities of each material were measured to be 3.0 and 2.9 eV, respectively. A deviation from the electron affinity model of 2.0 eV

was observed. An instability of the HfO₂ film was demonstrated, as energy levels shifted by ~0.4 eV during an 650 °C anneal of the as-deposited HfO₂ film. Band alignment measurements suggest HfO₂ could passivate n-type GaN surfaces. The valence band offset of ~0.3 eV could passivate p-type GaN surfaces, but the thermal instability should be examined further before device fabrication is considered.

In an attempt to understand the relation of the measured band alignments and the different models for heterostructure band alignment, our measured interface alignments for GaN/SiO₂, GaN/Si₃N₄, and GaN/HfO₂ are compared in Figure 12. In each case the diagrams are aligned to the vacuum level at the dielectric. The bandgap of each material is indicated, as is the VBO. The position of the vacuum level of the clean GaN surface is indicated, and the difference between these values and the surface vacuum level is the deviation from the EAM. This difference represents the change in the interface dipole, and was found to be 1.6, 1.1, and 2.0 ± 0.2 eV for SiO₂, Si₃N₄, and HfO₂ on GaN, respectively. It is evident from the figure that the electron affinity model does not adequately describe the GaN-dielectric interface.

Also indicated in Figure 12 is the CNL of the materials based on the literature. Though the values for the CNL of SiO₂ and Si₃N₄ have not been reliably determined, a calculated value for the level of Si₃N₄ was obtained. The high value (0.86) for the dielectric screening parameter, S , as well as the large bandgap of SiO₂ does not allow the CNL to be reliably determined. A combination of the charge neutrality level of Si₃N₄ and experimental band alignment information allowed the dielectric screening parameter ($S = 0.26$) to be calculated. This suggests the band alignment and resulting interfacial dipole should be similar to the relative charge neutrality levels, which is the case shown in Figure 12. For the GaN/HfO₂ interface, a value of S does not exist between 0 and 1 that can make the CNL's align indicating that a more complex analysis is required.

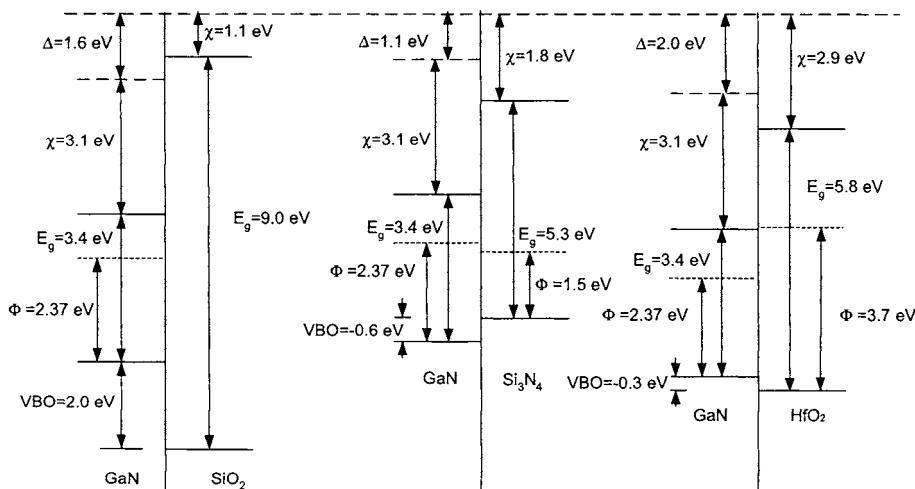


Figure 12 Experimental summary of the band alignment of GaN/SiO₂, GaN/Si₃N₄ and (annealed) GaN/HfO₂ interfaces. The dashed line at the top of the figure corresponds to the electron affinity of the dielectric surfaces, which is common in each interface. The deviation from the electron affinity model is shown as Δ , and the charge neutrality level (CNL) is indicated as a dashed line within the band gap.

A developing trend shown in Figure 12 is the interface dipole in relation to the dielectric. Though below the detection limits of XPS, Ga-O bonding undoubtedly exists at the GaN-oxide (SiO_2 and HfO_2) interface. With the Ga atomic layer more positive and the O layer more negative, the resulting interface dipole would be expected to significantly increase the oxide levels with respect to the GaN electronic levels, which is consistent with our observations. The interface dipole for the GaN/ Si_3N_4 is significantly lower than that of the other two interfaces, as N-Ga-N-Si bonding may be present at the interface. Our results suggest that the presence of a Ga-O layer may substantially change the band alignment as the heterostructure is formed.

Of the dielectrics characterized here, SiO_2 is the dielectric of choice for passivation of n- and p-type GaN. Careful considerations must be made if an oxide is chosen to passivate GaN devices, as Ga-O bonding is expected at the interface. As compared to oxides, Si_3N_4 shows a significant reduction of the interface dipole. Alternatively, HfO_2 can be used for passivation, but the thermal instability must be carefully considered before device design can be implemented.

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QUASI-BALLISTIC AND OVERSHOOT TRANSPORT IN GROUP III-NITRIDES

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We analyze steady-state and transient electron transport in the group III-nitride materials at high and ultra-high electric fields for different electron concentration regimes. At high electron concentrations where the electron distribution function assumes a shifted Maxwellian, we investigate different time-dependent transient transport regimes through the phase-plane analysis. Unexpected electron heating pattern is observed during the velocity overshoot process with a moderate electron temperature near the peak velocity followed by rapid increase in the deceleration period. For short nitride diodes, space-charge limited transport is considered by taking into account the self-consistent field. In this case, the overshoot is weaker and the electron heating in the region of the peak velocity is greater than that found for time-dependent problem. The transient processes are extended to sufficiently larger distances as well. When the electron concentration is small, we propose a model which accounts the main features of injected electrons in a short device with high fields. The electron velocity distribution over the device is found as a function of the field. It is demonstrated that in high fields the electrons are characterized by the extreme distribution function with the population inversion.

Keywords: Ballistic transport; overshoot; III-nitrides.

1. Introduction

Group III-nitride semiconductors and heterostructures have unique fundamental material properties which make them very promising for a number of optoelectronic and high-power, high-frequency applications. They have the energy band-gaps ranging from 0.8 eV (InN) to 6.2 eV (AlN), relatively small effective masses¹ of $0.11m_0$ (InN), $0.2m_0$ (GaN), and $0.48m_0$ (AlN) for the electrons and approximately $(0.3 - 0.5)m_0$ for the holes (m_0 is the free electron mass), and large optical phonon energies of about $(90 - 100)\text{ meV}$. Yet, electron-polar optical phonon coupling is much stronger in comparison to that of the III-V compounds; the Frölich phonon-coupling constant α is estimated to be 0.22, 0.41, and 0.74 for InN, GaN and AlN, respectively (for GaAs $\alpha = 0.075$). This results in high-field carrier transport mainly determined by the interaction with the polar optical phonons. The energy splitting between the lowest (Γ) and upper ($M - L$) conduction valleys is large ($\approx 2\text{ eV}$ for InN, $\approx 1.5...2\text{ eV}$ for GaN, and $\approx 0.7\text{ eV}$ for AlN). This leads to large peak velocities in the steady-state regime for the group III-nitrides. The velocities

are estimated to be $4.3 \times 10^7 \text{ cm/s}$ (InN), $3.1 \times 10^7 \text{ cm/s}$ (GaN), and $1.7 \times 10^7 \text{ cm/s}$ (AlN).¹ The materials are also expected to demonstrate the negative differential resistance due to the intervalley electron transfer or occurrence of the “inflection point” in the Γ band with a high threshold electric field (for example, $\approx 150 \text{ kV/cm}$ for GaN). The breakdown fields for these materials are in the MV/cm range. Other remarkable properties of these materials include large pyro- and piezo-fields allowing a new type of doping, high thermal conductivity, etc.

The steady-state high-field transport and, particularly, the velocity-electric field characteristics of the group III-nitrides were studied in a number of works.^{2–8} One can group these works into two main approaches. The first approach² is based on analytical calculations assuming a drifted Maxwellian function for the carriers with two parameters, the electron temperature and the drift velocity, which are determined by the energy and momentum balance equations. The method can be justified for large electron concentrations and dominant electron-electron (e-e) scattering. The second approach^{3–6,9} is a numerical Monte Carlo method, which frequently does not take into account e-e scattering at all and, thus, can be applied to the low carrier concentrations. The low-carrier concentration case was also treated analytically in the literature^{7,8} for the modest fields. The high-field transport in the two-dimensional nitride structures was studied in Refs. 10 and 11. All of these studies were performed for the steady-state regime in uniform bulk-like materials and structures.

The transient (time- or space-dependent) transport and the velocity overshoot effect in the nitrides^{12,13} were evaluated using the Monte Carlo technique^{10,14,15} and a nonstationary balance-equation procedure.^{16,17} It was found that the velocity overshoot effect takes place in the subpicosecond time scale and the ten-nanometer spatial scale at the fields approximately twice those for the peak velocities. It is expected that the maximum velocities of about $(6 - 8) \times 10^7 \text{ cm/s}$ may be achieved for InN and GaN.^{1,14}

As for experimental studies of the nitrides, most of the results for high electric biases were obtained for particular device structures (HEMTs, HETs, etc.). There are only a few reports with analyses of specific parameters in the three-dimensional and two-dimensional nitride materials under high electric fields. The objective difficulty of electric measurements is related to the principal fact: high-field effects in the nitrides are accompanied by strong electric currents that cause considerable *Joule lattice heating*. To avoid the lattice self-heating and to observe purely electron effect, one needs to use *pulse measurement methods*. For example, the authors of Ref. 18 observed the current-voltage (I-V) characteristic of a bulk-like GaN up to 200 kV/cm and found a negative differential conductivity with the critical field of about 150 kV/cm ; however, no analysis of the lattice heating effect was done. In Ref. 19, high microwave fields were used to measure the nonlinear transport. Microwave field pulses of about $1 \mu\text{s}$ in duration were applied to a GaN/AlGaN structure and I-V characteristics showing a tendency to saturate at fields above 50 kV/cm were measured; no proof of avoiding the Joule heating was presented. In Ref. 20, electron heating and lattice self-heating effects were separated for a GaN/AlGaN heterostructure, and the nonlinear electron transport was reported for the fields less than 10 kV/cm . Another, Joule-heating-free approach is based on ultra-short all-optical measurements (see Refs. 21 and 22). Typically this approach employs

short $p - i - n$ homo- or heterostructures under a reverse bias. In the i -region, electric fields can reach the MV/cm range with the reverse currents suppressed. Femtosecond pulse electron excitation and simultaneous optical probe experiments allow one to observe transient electron transport. By this method, GaN was found to exhibit the overshoot effect with a maximum drift velocity up to $7 \times 10^7\text{ cm/s}$ and the negative differential conductivity at the fields above 300 kV/cm .

In general, the earlier studies in the literature demonstrated great promises of group III-nitrides for high-power and high-frequency electronics.^{1,23} However, there are still many interesting and important high-field effects in the nitrides that have not been investigated in detail. We start with a reminder of basic factors that determines different electron kinetic regimes.

2. Electron Transport Regimes in the Nitrides

Hot-electron transport regimes are dependent on multiple parameters and factors. First of all, the properties of the electron band structure – effective masses, non-parabolicity parameters, upper valley characteristics, etc. – should be taken into account. Then, the kinetic factors such as momentum and energy relaxation mechanisms and intervalley scattering are of importance. Other parameters and factors controlling transport regimes include the carrier concentration, physical geometry, and bias conditions. Let us briefly discuss the influence of these factors.

The magnitude of the carrier concentration determines the role of e-e interaction under transport regimes. At large carrier concentrations, e-e scattering dominates over other relaxation mechanisms and the electron subsystem has *common* (“*collective*”) momentum and energy budgets. Nonequilibrium carrier distributions in the momentum and energy spaces occur in the form close to the shifted Maxwellian function (or Fermi-Dirac function) with an effective electron temperature and a drift velocity. At low concentrations where e-e scattering does not prevail, the electrons have *independent* (“*individual*”) momentum and energy budgets, and the electron distribution generally has a non-Maxwellian form frequently showing a strong anisotropy, inverted population, and other nontrivial features.

Geometrical factors (sample and device feature sizes, intercontact distances, etc.) as well as the character of electron confinement also affect the hot-electron kinetics. Indeed, when a characteristic size of a device becomes comparable to one of the semiclassical kinetic lengths (the intervalley scattering length, energy relaxation length, mean free path, etc.) the electron kinetics becomes dependent on the device size. Correspondingly, the size-dependent transport may be appreciably different from that in the bulk-like materials.¹³ For example, intervalley transfer processes and energy relaxation can be avoided in sufficiently short devices. In samples shorter than the mean free path, the transport occurs in a quasi-ballistic regime, and so on. Furthermore, electron quantum confinement can modify the energy spectra of the carriers, reduce their scattering,¹³ and considerably change the hot-electron effects.

Different combinations of the parameters and factors mentioned above give a variety of the transport regimes. For such materials as Ge, Si, and III-V compounds, these regimes were studied in detail during the past four decades. However, perspective application of the nitrides with their unique material properties makes the investigation of various hot-electron regimes far more realistic and fascinating.

Particularly, the effects originated from strong electron-optical phonon coupling inherent in the polar nitride materials is the focus of our study. One such effect is *the electron runaway effect*. The runaway is a well-known hot-electron phenomenon^{24,25} that arises in the polar crystals with predominant scattering by the polar optical phonons. Because of the Coulomb nature, the polar optical phonon scattering rate is inversely proportional to the square of the momentum change during a scattering event, and thus decreases for the electrons with large momenta and energies. The runaway effect occurs at high electric fields when a sufficient number of carriers stream into the high energy states with a low scattering rate. Above a critical field, the momentum and energy gained by the electrons from the field cannot be relaxed to the lattice. The carriers then continue to accelerate toward higher and higher energies and the steady state is absent.²⁶ The subsequent scenarios are different for the two cases. In a *bulk-like sample*, the electron runaway is to be stabilized by one of the following effects: a nonparabolicity of the energy band and electron transfer to upper valleys, etc. In a sufficiently *short sample*, however, these effects may not be important and the electron transport can occur in the runaway regime.

It is instructive to compare the two transient phenomena, the overshoot effect and the runaway effect. Literally the overshoot effect is a nonmonotonous behavior of the electron velocity during the transient process of reaching the steady state after a very fast switching on a high electric field. It is generally accepted that the overshoot manifests itself if the momentum relaxation length is much smaller than that of the energy relaxation.^{12,13} Particularly, the overshoot can be observed even in nonpolar materials (for example, in Si). In contrast, the runaway *does not require* an inequality between the momentum and energy relaxation lengths or times and can occur only in polar materials.²⁷ Below we will show that in polar materials such as group III-nitrides, the runaway effect is responsible for a large velocity overshoot.

In general, the runaway effect is more pronounced for crystals with stronger electron-optical phonon coupling. It was found and treated by the quantum mechanical approach under arbitrarily strong coupling²⁶ as well as by the classical framework of Boltzmann transport theory.²⁵ Due to the relatively strong electron-optical phonon coupling and high breakdown fields, the group III-nitrides can exhibit the runaway effect at different transport regimes, including both high and low electron concentration cases.

3. Boltzmann Transport Equation

In electrically biased semiconductors and their heterostructures, the distribution of nonequilibrium electrons in the momentum space determines the basic electric properties. Assuming that in a general case there are several actual energy valleys in the conduction band,^{13,25} we introduce the distribution function $f_l(\vec{P}, \vec{R}, t)$, where the subscript l denotes different energy valleys, \vec{P} and \vec{R} are the electron momentum- and real-space coordinates, and t is the time. Then, the Boltzmann transport equation for f_l can be written as

$$\frac{\partial f_l}{\partial t} + \frac{\partial f_l}{\partial \vec{P}} \left(-\frac{\partial U}{\partial \vec{R}} \right) + \frac{\partial f_l}{\partial \vec{R}} \frac{\partial E_l(\vec{P})}{\partial \vec{P}} = \left(\frac{\partial f_l}{\partial t} \right)_{coll}. \quad (1)$$

Here $E_l(\vec{P})$ and $\partial E_l(\vec{P})/\partial \vec{P} = \vec{V}_l(\vec{P})$ are the kinetic energy and the velocity of

electrons in the valley l , and $U(\vec{R})$ is the potential energy. In moderate electric fields, when the electron energy spectrum may be assumed to be parabolic, we will use the simple relation $E_l = P^2/2m_l$ with the electron effective mass m_l in the valley l . For the electron transport under high fields and high electron energies, we shall take into account the nonparabolicity of the energy spectrum and use the Kane formula for a spherical valley relating P and E_l :

$$\frac{P^2}{2m_l} = E_l (1 + \beta_l E_l) , \quad (2)$$

with the nonparabolicity parameter β_l .

The right-hand side of the Boltzmann equation [Eq. (1)] is the collision integral. The latter, in general, includes both intravalley and intervalley scattering:

$$\left(\frac{\partial f_l}{\partial t} \right)_{coll} = \bar{I}_l \{ f_l \} + \bar{I}_{iv} \{ f_l, f_{l'} \} . \quad (3)$$

Also it is convenient to formally distinguish contributions from the e-e collisions and the scattering by phonons, possible crystal imperfections, etc.:

$$\bar{I}_l = \bar{I}_l^{e-e} + \bar{I}_l^{ph} + \dots, \quad \bar{I}_{iv} = \bar{I}_{iv}^{e-e} + \bar{I}_{iv}^{ph} + \dots . \quad (4)$$

Equation (1) is a set of differential equations with partial derivatives with respect to the coordinates. To analyze a finite-size device, one needs to impose boundary conditions to these equations. Let, for example, the electron parameters be dependent on a single coordinate along the electric current, Z . Then, one needs to specify the distribution function of the injected electrons at the left contact [$f_l(\vec{P}, Z = 0), P_z > 0$] and at the right contact [$f_l(\vec{P}, Z = L), P_z < 0$], where L is the intercontact distance (i.e., the channel length). These electron distributions $f_l(\vec{P}, Z = 0)$ and $f_l(\vec{P}, Z = L)$ depend on the contact properties. Finally, the electron distribution function should be normalized:

$$2 \times \frac{1}{(2\pi\hbar)^3} \int d^3P f_l = n_l(\vec{R}), \quad \sum_l n_l(\vec{R}) = n(\vec{R}).$$

Here n_l is the electron concentration for the l^{th} -valley and n is the total electron concentration. Generally, all concentrations depend on the coordinates.

For a uniform electric field F , we present the potential energy in the form $U(Z) = -eFZ$ ($e > 0, F > 0$). For the hot electrons in the nitrides with the dominant scattering by the optical phonons, the characteristic energy of the problem is the phonon energy $\hbar\omega$, and the characteristic momentum and velocity are $P_O = \sqrt{2m_c\hbar\omega}$ and $V_O = P_O/2m_c$, respectively. Here we introduced the effective mass in the central valley $m_l = m_c$ for $l = c$. For further analysis, it is convenient to use the dimensionless momentum, energy, velocity, and potential energy:

$$\vec{p} = \frac{\vec{P}}{P_O}, \quad \epsilon_l = \frac{E_l}{\hbar\omega}, \quad \vec{v}_l = \frac{\vec{V}_l}{V_O}, \quad u = \frac{U}{\hbar\omega}.$$

By taking advantage of a characteristic length l_O specified below, we also define the dimensionless coordinate z , time τ , field \mathcal{E} , potential energy $u(z)$, and crystal

temperature θ_0 :

$$z = \frac{Z}{l_O}, \quad \tau = \frac{t}{\tau_O}, \quad \tau_O = \frac{l_O}{V_O}, \quad \mathcal{E} = \frac{F}{F_O}, \quad F_O = \frac{\hbar\omega}{el_O}, \quad u(z) = -\mathcal{E}z, \quad \theta_0 = \frac{k_B T_0}{\hbar\omega},$$

where T_0 is the crystal temperature and k_B is the Boltzmann constant. Then the Boltzmann equation can be rewritten as

$$\frac{\partial f_l}{\partial \tau} + \frac{\partial f_l}{\partial p_z} \left(-\frac{\partial u}{\partial z} \right) + \frac{\partial f_l}{\partial z} v_{l,z} = \frac{P_O l_O}{\hbar\omega} (\bar{I}_l \{f_l\} + \bar{I}_{iv} \{f_l, f_{l'}\}). \quad (5)$$

The contribution of the optical phonons to the “dimensionless” collision integral is expressed by

$$\begin{aligned} I_l^{op} \equiv \frac{P_O l_O}{\hbar\omega} \bar{I}_l^{op} &= \frac{e^2 P_O^2 l_O}{2\pi\hbar^3\omega} \left(\frac{1}{\kappa_\infty} - \frac{1}{\kappa_0} \right) \frac{1}{e^{1/\theta_0}-1} \times \\ &\int \frac{d^3 p'}{(\vec{p} - \vec{p}')^2} \left\{ [e^{1/\theta_0} f_l(\vec{p}') - f_l(\vec{p})] \delta[\epsilon_l(p) - \epsilon_l(p') + 1] + \right. \\ &\quad \left. [f_l(\vec{p}') - e^{1/\theta_0} f_l(\vec{p})] \delta[\epsilon_l(p) - \epsilon_l(p') - 1] \right\}. \end{aligned} \quad (6)$$

Here the collision integral is provided for the nondegenerate electrons in a bulk-like sample; κ_0 and κ_∞ are the low-frequency and high-frequency permittivities of the crystal, respectively. We set $1 = l_O \frac{e^2 m_e}{\hbar^2} \left(\frac{1}{\kappa_\infty} - \frac{1}{\kappa_0} \right)$ and thereby define the optical phonon scattering length l_O as

$$l_O = a_B \frac{\kappa_\infty}{\kappa_0 - \kappa_\infty}, \quad (7)$$

with the effective Bohr radius a_B for the electrons in the central valley.

4. High Concentration Regimes

4.1. Basic equations

The cases with high electron concentrations are the most typical for group III-nitrides and their heterostructures. Under such conditions, e-e collisions dominate over all other scattering processes in Eqs. (3) and (4). Accordingly, the Boltzmann equation may be solved as follows.

In the first approximation, one may consider only the e-e terms and neglect all the other terms in the transport equations. This gives the set of equations:

$$\bar{I}_l^{e-e} \{f_l\} + \bar{I}_{iv}^{e-e} \{f_l, f_{l'}\} = 0.$$

The equations can be satisfied by a shifted Fermi-Dirac function with two arbitrary parameters T_e and V_{dr} , which have the meaning of the electron temperature and the drift velocity. For nondegenerate electrons, we obtain:

$$f_l(\vec{P}) \propto \exp \left[-\frac{E_l(P) - \vec{P}\vec{V}_{dr}}{k_B T_e} \right]. \quad (8)$$

Intensive momentum and energy exchange between the electrons in different valleys establishes the distributions with the same T_e and V_{dr} . Note that the form of

Eq. (8) is valid for an arbitrary electron dispersion $E_l(P)$, including the nonparabolic dependence of Eq. (2).

The parameters T_e and V_{dr} are to be found from the momentum and energy balance equations, which can be obtained by multiplying Eq. (1) by P_z and $E_l(P)$, respectively, followed by integrating and summing them over \vec{P} and l . As a result, the leading terms $\bar{I}_l^{e-e} + \bar{I}_{iv}^{e-e}$ are cancelled, while the other terms contribute to the momentum and energy balances. For a spatially uniform problem, these equations are

$$\frac{\partial \langle p \rangle}{\partial \tau} = \mathcal{E} - Q_p [\theta, v_{dr}], \quad (9)$$

$$\frac{\partial \langle \epsilon \rangle}{\partial \tau} = \mathcal{E} v_{dr} - Q_\epsilon [\theta, v_{dr}], \quad (10)$$

where the dimensionless parameters $\theta = k_B T_e / \hbar \omega$ and $v_{dr} = V_{dr} / V_O$ are introduced. The average momentum $\langle p \rangle$ and energy $\langle \epsilon \rangle$, as well as the dimensionless momentum and energy relaxation rates (Q_p and Q_ϵ , respectively) are calculated as functions of θ and v_{dr} .

Below, we confine ourselves to the case of two effective conduction valleys: *the central valley* (c) and the group of *satellite valleys* (s) with the intervalley energy spacing $E_s = \Delta_s \hbar \omega$ and the valley degeneracy factor g_s . Then the distribution function is given by

$$f_l(p) = A g_l \exp \left[-\frac{\Delta_l}{\theta} \right] \exp \left[-\frac{\epsilon_l(p) - p v_{dr}}{\theta} \right], \quad l = c, s,$$

with $\Delta_c = 0$, $g_c = 1$. The normalization constant A equals:

$$A = \frac{(2\pi\hbar)^3}{2P_O^3 I_N^c} \frac{n}{1 + G_s}, \quad G_s = g_s \gamma_s^3 \frac{I_N^s}{I_N^c} \exp \left[-\frac{\Delta_s}{\theta} \right],$$

$\gamma_l = \sqrt{m_l/m_c}$. The carrier concentrations in the central and satellite valleys are

$$n_c = \frac{n}{1 + G_s}, \quad n_s = \frac{G_s n}{1 + G_s}.$$

The average momentum and energy can be readily calculated by using the distribution in the form of Eq. (8):

$$\langle p \rangle = \frac{I_P^c + g_s \gamma_s^4 e^{-\Delta_s/\theta} I_P^s}{(1 + G_s) I_N^c},$$

$$\langle \epsilon \rangle = \frac{I_E^c + g_s \gamma_s^3 e^{-\Delta_s/\theta} I_E^s}{(1 + G_s) I_N^c}.$$

The momentum and energy dissipation rates in Eqs. (9), (10) have the form:

$$Q_p[\theta, v_{dr}] = \frac{I_{Qp}^{c,1} + e^{1/\theta_0} I_{Qp}^{c,2} + g_s \gamma_s^5 e^{-\Delta_s/\theta} (I_{Qp}^{s,1} + e^{1/\theta_0} I_{Qp}^{s,2})}{\pi (e^{1/\theta_0} - 1) (1 + G_s) I_N^c},$$

$$Q_\epsilon[\theta, v_{dr}] = \frac{e^{1/\theta_0} I_{Q\epsilon}^{c,1} - I_{Q\epsilon}^{c,2} + g_s \gamma_s^4 e^{-\Delta_s/\theta} (e^{1/\theta_0} I_{Q\epsilon}^{s,1} - I_{Q\epsilon}^{s,2})}{\pi (e^{1/\theta_0} - 1) (1 + G_s) I_N^c}.$$

The integrals $I_N^{c,s}$, $I_P^{c,s}$, $I_E^{c,s}$, $I_{Qp}^{c,s}$, $I_{Q\epsilon}^{c,s}$ are the functions of θ and v_{dr} , and depend parametrically on the dimensionless nonparabolicity factor

$$\nu_l = \beta_l \hbar \omega. \quad (11)$$

The integrals are summarized in Appendix A.

Equations (9) and (10) as well as other relationships described above allow one to analyze both the steady-state and transient transport regimes in detail.

4.2. Steady-state characteristics

We start with the stationary regime where the electric field and electron parameters do not depend on time. Then, Eqs. (9) and (10) take the form of two coupled nonlinear algebraic equations for the two characteristic parameters of the nonequilibrium electron gas θ and v_{dr} :

$$\mathcal{E} - Q_p[\theta, v_{dr}] = 0, \quad \mathcal{E}v_{dr} - Q_\epsilon[\theta, v_{dr}] = 0. \quad (12)$$

Note from Eqs. (12) that the field \mathcal{E} can be excluded and the field-independent relationship between θ and v_{dr} can be obtained: $v_{dr}Q_p[\theta, v_{dr}] = Q_\epsilon[\theta, v_{dr}]$. This equation depends only on the conduction band parameters.

Consider first the model with a single electron valley c ($g_s = 0$ in the relationships described above). Interestingly, this single-valley model and the accepted dimensionless form give the results that are dependent on one material parameter, namely the nonparabolicity parameter ν_c . This allows one to conduct a comprehensive analysis. In Figs. 1(a) and 1(b), $\theta(\mathcal{E})$ and $v_{dr}(\mathcal{E})$ are presented for different ν_c . We find that the electron transport crucially depends on ν_c . For the parabolic band with $\nu_c = 0$ (curve 1), both $\theta(\mathcal{E})$ and $v_{dr}(\mathcal{E})$ exhibit two, lower and upper, branches. The lower branch, which increases with the field, is stable, while the upper one is electrically unstable. Indeed, the latter corresponds to a decrease of v_{dr} with \mathcal{E} , i.e., the decreasing electric current with the field and the negative differential conductivity. Then the solutions exist only for the fields below a threshold value $\mathcal{E}_{th} = 0.53$. This value is the *runaway field*. At $\mathcal{E} > \mathcal{E}_{th}$, there are no normalized solutions of Eq. (1), as discussed in Section 1.

For a finite value of the nonparabolicity parameter, $\theta(\mathcal{E})$ and $v_{dr}(\mathcal{E})$ evolve as follows. The solutions, in principle, exist for any \mathcal{E} . For the interval $0 < \nu_c < 0.013$, both $\theta(\mathcal{E})$ and $v_{dr}(\mathcal{E})$ become *three-valued* functions (see curves 2 and 3 as well as the insets in Fig. 1). Clearly, $\theta(\mathcal{E})$ exhibits a well-known S-shape while $v_{dr}(\mathcal{E})$ has an unusual form with a crimp; both should be unstable provided they can be achieved. For $\nu_c = 0.013$, the three-valuedness in θ and v_{dr} disappears. Instead, both have almost vertical portions at $\mathcal{E} = 0.62$ (curve 4 in Fig. 1). Further increase in ν_c leads to $\theta(\mathcal{E})$ increasing with \mathcal{E} . The case of $v_{dr}(\mathcal{E})$ demonstrates negative derivatives due to an increase of the effective mass of the electrons with larger energy.

Though the nonparabolicity effect formally suppresses the electron runaway and leads to the existence of the solutions under arbitrarily large fields, these steady-state solutions have no significant implications for bulk-like samples, since they correspond to nonphysically high electron temperatures, as followed from Fig. 1(a). For such electron temperatures, the one-valley model fails, and the upper valleys and intervalley electron transfer must be taken into account for bulk materials.

However, two important conclusions can be made from the above analysis: (i) Independent of the magnitude of the nonparabolicity parameter, the runaway effect manifests itself in polar materials as a rapid increase in the electron energy and the velocity in a narrow range of electric fields ($\mathcal{E} \approx \mathcal{E}_{th}$); (ii) For transient transport and short-scale devices, the runaway effect as well as the multi-valued solutions should have obvious significance.

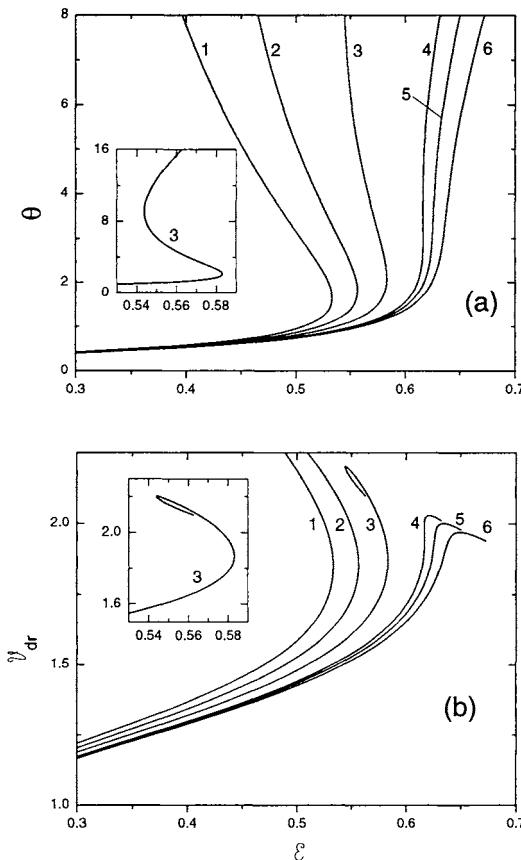


Fig. 1. (a) Dimensionless electron temperature θ and (b) drift velocity $v_{d\tau}$ versus dimensionless electric field \mathcal{E} calculated for the one-valley model with different values of nonparabolicity parameter ν_c : $\nu_c = 0$ (curve 1, parabolic band), 0.005 (curve 2), 0.01 (curve 3), 0.015 (curve 4), 0.016 (curve 5), 0.0172 (curve 6). The insets show curve 3 as an example of the three-valued solutions.

After the analysis of the one-valley model, let us return to a more realistic case with two types of valleys in the conduction band: the central valley and the satellite valleys. To obtain numerical results, we use the material parameters discussed in Ref. 1. Particularly, for GaN we use the nonparabolicity parameter $\nu_c = \nu_s = 0.017$

and the intervalley energy splitting $\Delta_s = 14.36$ ($E_s = 1.31$ eV).

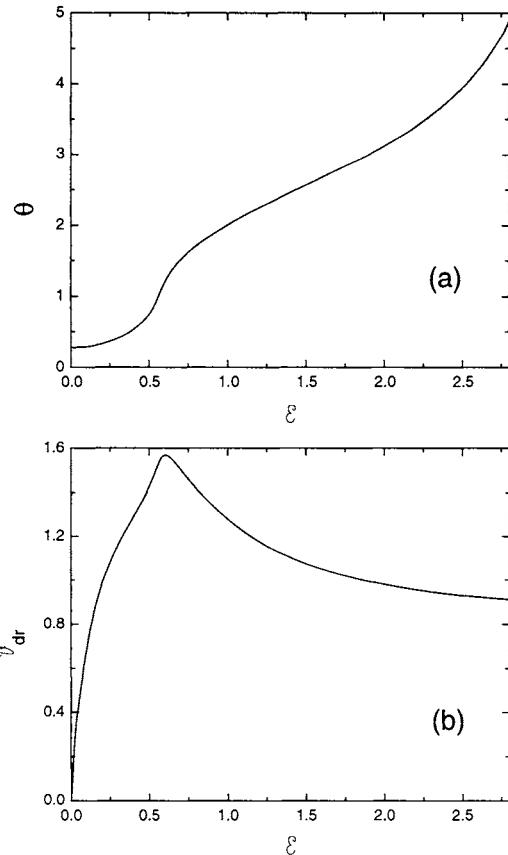


Fig. 2. (a) Electron temperature θ and (b) drift velocity v_{dr} versus the electric field E calculated for GaN using the multi-valley model.

In Fig. 2, we present $\theta(E)$ and $v_{dr}(E)$ calculated in the multi-valley model for bulk GaN at $T_0 = 300$ K. From the figure, the three characteristic high-field regimes are clearly seen. At $E < E_{th}$, we observe a modest increase in $\theta(E)$ and $v_{dr}(E)$ typical for hot electrons populating the central valley. In a narrow range around E_{th} , a sharp increase in θ and a characteristic “turn-up” in v_{dr} occur due to the runaway effect discussed above. The temperature reaches values of about 1.5. Starting from these fields, the electrons populate the “heavy” upper valleys. Further increase in E leads to electron temperatures typical for intervalley transfer resulting in a drop in the average electron velocity (the so-called Ridley-Watkins effect). The drift velocity reaches its maximum value equal to 1.57 ($V_{dr} = 3.14 \times 10^7$ cm/s) at $E = 0.595$ ($F = 153$ kV/cm). These parameters are in good agreement with results of other papers in the literature.¹⁸ One fact demonstrated by Fig. 2(a) should be stressed: At the higher fields $E > 2$, the electron temperature θ reaches the magnitude of about 3...4 ($T_e > 3150...4200$ K). This means that we deal with *extremely overheated* electrons in this field range.

4.3. Transient regimes

All possible time-dependent regimes are described by Eqs. (9) and (10). In these equations, $\langle p \rangle$, $\langle \epsilon \rangle$, Q_p , and Q_ϵ are defined as functions of θ and v_{dr} . Thus, we obtain an *autonomous system* of two differential equations for the variables θ and v_{dr} . Such the autonomous system permits detailed study by using the so-called *phase-plane* analysis (see, for example, Ref. 28). The phase-plane analysis is based on simple reduction of the system [Eqs. (9) and (10)] to a single differential equation of the first order:

$$\frac{dv_{dr}}{d\theta} = \frac{\langle p \rangle'_\theta (\mathcal{E}v_{dr} - Q_\epsilon) - \langle \epsilon \rangle'_\theta (\mathcal{E} - Q_P)}{\langle \epsilon \rangle'_{v_{dr}} (\mathcal{E} - Q_P) - \langle p \rangle'_{v_{dr}} (\mathcal{E}v_{dr} - Q_\epsilon)}, \quad (13)$$

where $\langle p \rangle'_\theta$, $\langle p \rangle'_{v_{dr}}$, $\langle \epsilon \rangle'_\theta$, and $\langle \epsilon \rangle'_{v_{dr}}$ are the derivatives of $\langle p \rangle$ and $\langle \epsilon \rangle$ with respect to θ and v_{dr} . At a given field \mathcal{E} , any solution of Eq. (13) can be presented as a certain “trajectory” in the $\{\theta, v_{dr}\}$ -phase plane. A chosen point $(\theta_i, v_{dr,i})$ can be interpreted as an initial condition attributed to the moment $\tau = 0$. The trajectory which crosses this point determines the dynamics of the electron gas at $\tau > 0$. The arrows at the trajectory indicate the direction of evolution for θ and v_{dr} . The singular points of Eq. (13) obviously correspond to the steady-state regimes. Equating the numerator and denominator in Eq. (13) to zero, we obtain two *isoclines*: a trajectory $v_{dr}(\theta)$ crosses the first (*h*) isocline always horizontally ($dv_{dr}/d\theta = 0$), while the second (*v*) isocline is always crossed vertically ($|dv_{dr}/d\theta| \rightarrow \infty$). These properties of the trajectories allow one to reconstruct readily the topology of the phase plane and to study the transient regimes with different initial conditions.

Consider first the electric fields below the threshold value ($\mathcal{E} < \mathcal{E}_{th}$). According to our earlier analysis in this field range, the stable stationary solutions $\theta(\mathcal{E})$ and $v_{dr}(\mathcal{E})$ can be well described by the one-valley model. It is instructive to start with the phase-plane analysis for this model with the parabolic energy band ($\nu_c = 0$). In addition, such a consideration helps one to understand the role of the runaway effect in the transient transport regimes.

In Fig. 3(a), the phase-plane analysis of the parabolic one-valley model is presented for $\mathcal{E} = 0.5$. The two steady-state solutions achievable in this case (see curve 1 in Fig. 1) produce two singular points: the node **N** and the saddle **S**. Both *h*-isocline and *v*-isocline are presented, they cross each other at the **N** and **S** points. Two separatrices s_1, s_2 of the **S** point divide the phase plane into two regions with very distinct behavior of the trajectories. In the phase plane below these separatrices, all trajectories are attracted by the **N** point, i.e., a transient dynamics is completed by the steady state. Depending on the initial conditions, different types of the trajectories and transient dynamics occur. For the electrons with small initial velocities v_i and $\theta_0 < \theta_i < 2$, the trajectories (curves 1 and 2) exhibit a nonmonotonous behavior with cooling and subsequent heating of electrons and the drift velocities demonstrate a small overshoot effect. For the electrons with small initial velocities and higher temperatures ($2 < \theta_i < 5$), the trajectories (curves 3 and 4) correspond to monotonous cooling and the velocity overshoot. At high initial velocities ($v_i > 1.8$), the trajectories (curves 5 and 6) show monotonous deceleration of the electrons with an increase in the electron temperature, etc.

Finally, in the part of the phase plane above the s_1, s_2 separatrices, the tra-

jectories tend to “runaway” within the sector defined by the h -, v -isoclines, as illustrated by curves 7 and 8. The latter effect can be interpreted as the *low-field* runaway effect: despite the fact that the applied field is smaller than the threshold value, the electrons with large enough initial kinetic energies, or thermal energies, raise their velocity and temperature without bound as the time increases. If the field magnitude is greater than \mathcal{E}_{th} , the phase plane changes drastically, as shown in Fig. 3(b) for $\mathcal{E} = 0.55$. No singular points occur (the steady state is absent) and the sector between the h - and v -isoclines becomes an attractor for *all trajectories* leading to “run away” toward high θ and v_{dr} .

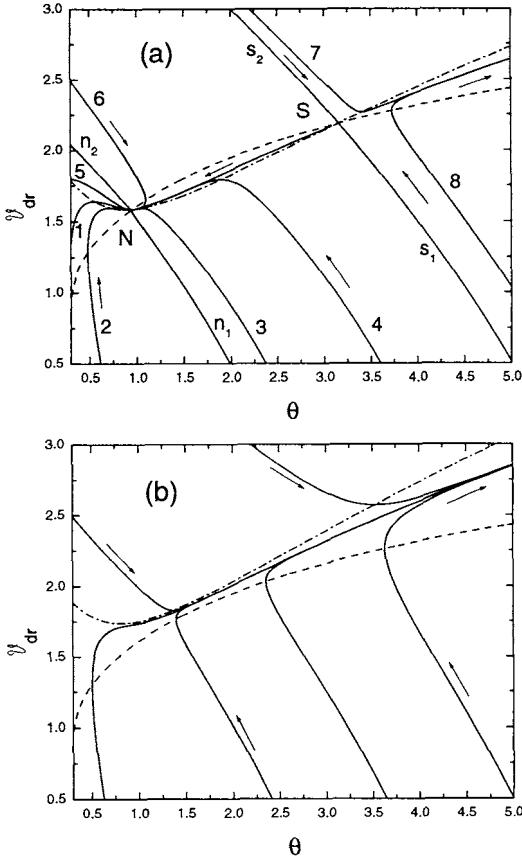


Fig. 3. Phase-plane analysis obtained by the one-valley parabolic model. The dashed and dashed-dotted curves are the v - and h -isoclines, respectively. The arrows indicate the direction of motion along the phase trajectories with time. In (a), $\mathcal{E} = 0.5 < \mathcal{E}_{th}$. $n_{1,2}$ and $s_{1,2}$ are separatrices of the node (N) and the saddle (S). Solid curves (1-8) are phase trajectories corresponding to different starting values of (θ_i, v_i) : 1 - $(\theta_0, 0)$, 2 - $(0.75, 0)$, 3 - $(2.75, 0)$, 4 - $(4, 0)$, 5 - $(\theta_0, 1.8)$, 6 - $(\theta_0, 2.5)$, 7 - $(2.2, 3.0)$, 8 - $(6, 0.5)$. In (b), $\mathcal{E} = 0.55 > \mathcal{E}_{th}$. Different types of the trajectories are presented, all of which tend to approach an attractor.

Let us return to the phase-plane analysis of the more realistic two-valley model. Concentrating on the high-field regimes, we present the results for $\mathcal{E} = 2$ in Figs. 4(a) and 4(b).

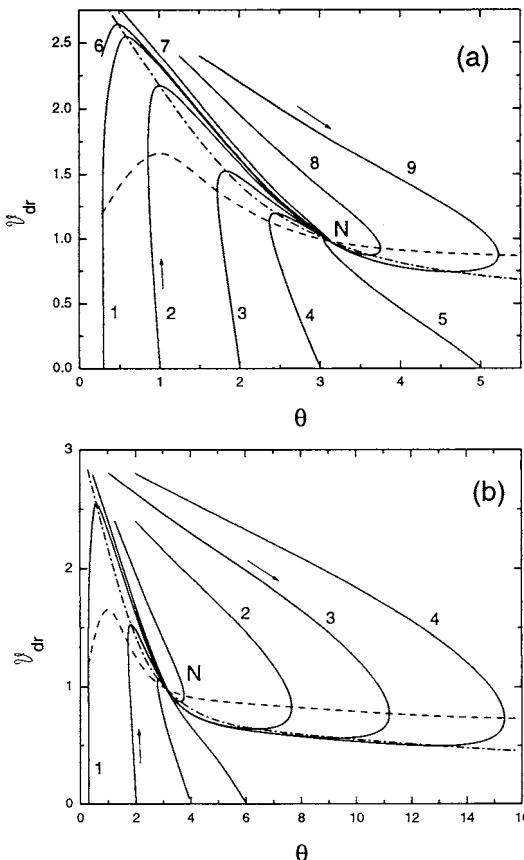


Fig. 4. Phase-plane analysis obtained by the two-valley model illustrating the high-field transport regime for $\mathcal{E} = 2$. The designations are similar to those of Fig. 3. (a) Curves 1-4 illustrate the overshoot regimes. (b) The same results as in (a) are shown in the extended temperature range. Curves 2-4 illustrate the strong overheating regimes.

The only steady-state solution corresponds to the node point N. Other notations are similar to those in Fig. 3. As shown in Fig. 4(a), all trajectories starting with small v_i and $\theta_i < 5$ demonstrate the velocity overshoot and nonmonotonic cooling-heating behavior of $\theta(\tau)$. Among them, the largest overshoot occurs for $v_i = 0$, $\theta_i = \theta_0$. There are no “runaway” trajectories at all. Instead, the trajectories with high-velocity initial conditions ($v_i > 2.9$, $\theta_i = \theta_0$) behave very unusually: they

correspond to considerable *dynamic overheating* of the electrons.

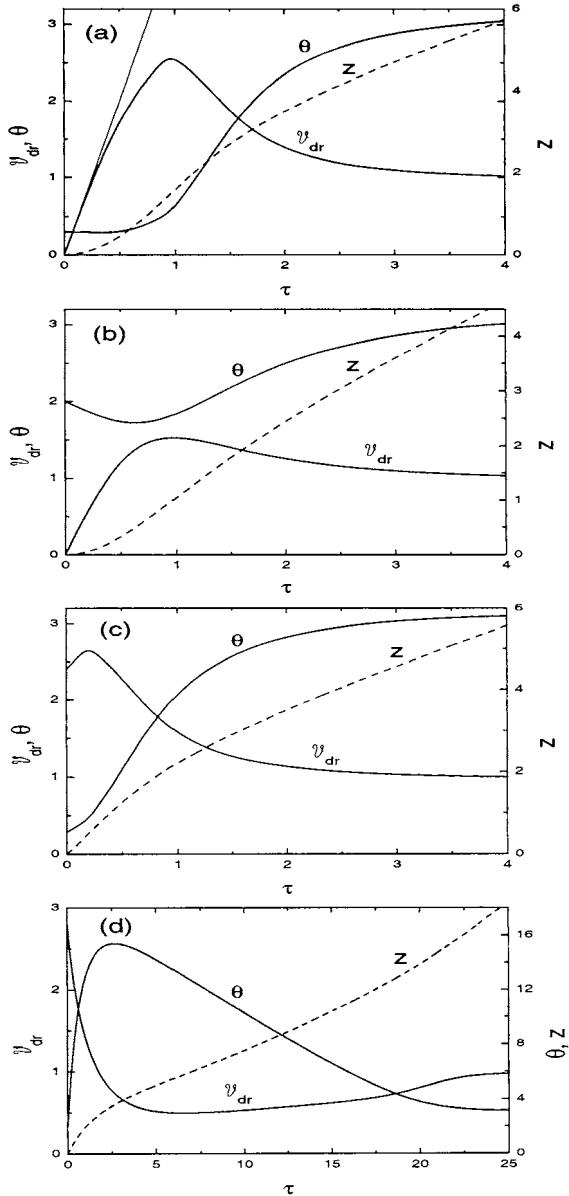


Fig. 5. Electron parameters $\theta(\tau)$ and $v_{dr}(\tau)$ (solid) along with the coordinate $z(\tau)$ (dashed) for the time-dependent transient regimes in bulk GaN samples. The calculations correspond to different trajectories for $\mathcal{E} = 2$ shown in Fig. 4. (a) Trajectory 1 ($\theta_i = \theta_0, v_i = 0$); the thin solid curve shows the ballistic $v_{dr}(\tau)$ -dependence. (b) Trajectory 3 ($\theta_i = 2, v_i = 0$). (c) Trajectory 6 ($\theta_i = \theta_0, v_i = 2.4$). (d) Trajectory 4 ($\theta_i = 2, v_i = 2.8$). (a)-(c) correspond to the trajectories shown in Fig. 4(a), and (d) to that in Fig. 4(b).

Moreover, a small deviation in the initial velocity gives rise to a large variation in these trajectories, as illustrated in Fig. 4(b). The trajectories 2, 3, and 4 of Fig. 4(b) correspond to small deviation in the initial velocities from 2.9 to 3. Nevertheless, the maximum temperatures achieved are 8, 11, and 15, respectively. Concluding this analysis, we can state that there are two types of trajectories with distinct behavior: the trajectories with small v_i manifest a strong velocity overshoot, whereas the trajectories with large v_i show a strong dynamic overheating of the electrons.

Now we discuss the characteristics of $v_{dr}(\tau)$ and $\theta(\tau)$ for some typical trajectories. In Fig. 5(a), we present these dynamic dependences for $\mathcal{E} = 2$ and the initial conditions $v_i = 0$, $\theta_i = \theta_0$ (trajectory 1 in Fig. 4). We also plot the dimensionless coordinate

$$z(\tau) = \int_0^\tau v_{dr}(\tau') d\tau', \quad (14)$$

which allows one to understand the dependence of these parameters on the coordinate. Comparison of $v_{dr}(\tau)$ with the ballistic dependence (the thin curve) confirms that the electron transport is essentially dissipative even at the early stage of the dynamics ($\tau > 0.4$). The overshoot holds in short time- and space intervals ($\tau \leq 2$, $z \leq 4$). The curve $v_{dr}(\tau)$ reaches the maximal overshoot at $\tau \approx 1$ with a peak value of $v_{dr} = 2.55$ ($V_{dr} = 5.1 \times 10^7 \text{ cm/s}$), which is greater than the steady-state velocity by as much as 2.6 times. It is interesting to note that during the overshoot stage the electron temperature increases up to modest values [$\theta(1) = 0.56$], while the electrons quickly gain their thermal energy at larger τ [for example, $\theta(3) = 2.9$].

Time evolution of the parameters for the electrons with $v_i = 0$ and $\theta_i = 2$ [trajectory 3 in Fig. 4(a)] is shown in Fig. 5(b). For this case, the velocity overshoot is rather small ($\max v_{dr} = 1.53$ at $\tau = 0.98$) and cooling of the electrons at the initial stage ($\tau \leq 1.4$) is followed by relatively slow electron heating. In Fig. 5(c), the results are shown for a finite initial velocity [$v_i = 2.4$ and $\theta_i = \theta_0$, see also trajectory 6 in Fig. 4(a)]. The overshoot is almost suppressed. Instead, the electron temperature increases much quickly in comparison to the case presented in Fig. 5(a).

Further increase in the initial velocity changes the electron dynamics drastically. This is illustrated in Fig. 5(d) where the results are given for $v_i = 2.8$, $\theta_i = 2$. Now the velocity decreases below the steady-state level ($\min v_{dr} = 0.5$ at $\tau = 6.6$). The large dynamic overheating leads to $\theta = 15.4$ at $\tau = 2.5$ followed by a slow temperature relaxation to the steady-state value of $\theta = 3.1$ during the period $\tau = 2.5 \dots 20$. This unusual behavior can be interpreted in terms of the peculiarity of electron scattering by optical phonons and the cooperative dynamics of the electrons. Indeed, a large initial velocity, i.e., a large initially stored energy of the electrons, gives rise to suppression of electron scattering by the polar optical phonons. The initial velocity cannot be supported by the applied field and during cooperative dynamics driven by e-e collisions, the directed motion is converted to chaotic motion of the electrons resulting in the increase in electron temperature. Then it is followed by a slow energy relaxation. The rise in the transient process time also leads to considerable increase of spatial distances necessary to reach the steady state ($z \approx 14$).

Finalizing discussion of the transient regime, we mention that all the initial conditions analyzed above can be realized in experiments. Indeed, low velocities and

large temperatures can be reached under fast photogeneration of the carriers with an excess energy in an electrically biased structure (the time-domain problem). High initial velocities at low initial temperatures are achieved under overbarrier injection of the electrons into a semiconductor (the space-domain problem), etc.

4.4. Transient transport in ultra-short diodes

Time-dependent transient transport analysis, which relates the time and the coordinate, allows one to obtain approximate estimates for spatially-dependent characteristics in short devices. Indeed, the results discussed in the previous sections were obtained for constant electric fields, while the fields in small-scale devices are strongly spatially-dependent. The electron parameters v_{dr} , θ , and the field \mathcal{E} should be calculated self-consistently. In this subsection, we analyze the steady-state electron transport in ultra-short devices. Specifically, we consider a $n^+ - i - n^+$ diode with the electric current provided by the injected electrons. The electric field in the diode is determined by both the applied voltage and the space-charge of injected electrons (the so-called *space-charge limited* transport). We assume that all parameters are dependent only on the coordinate z and the receiving contact absorbs all the injected electrons. Then we arrive at the electric current density conservation: $J_z = -e n(z) V_{dr}(z) = \text{const}$. The dimensionless Poisson equation for the electric field reads:

$$\frac{d\mathcal{E}}{dz} = \frac{j}{v_{dr}(z)}, \quad (15)$$

where $j = |J|/J_O$ with $J_O = eV_O n_O$ and $n_O = \kappa_0 \hbar \omega / 4\pi e^2 l_O^2$. The quantity j can be interpreted as the dimensionless current density. Interestingly, the current is scaled to the value J_O which is determined by properties of the lattice and electron-optical phonon interaction. Equation (15) is valid in the i -region. At the emitting contact ($z = 0$), we set the field equal zero, which corresponds to the approximation of “virtual cathode”.²⁹ Now the differential equations given in Eqs. (9), (10), and (15) as well as the relationship of Eq. (14) compose the system which describes self-consistently the electron parameters $v_{dr}(z)$, $\theta(z)$, and the field $\mathcal{E}(z)$ at a given current density j . The boundary conditions at the virtual cathode are: $\mathcal{E} = 0$ and $v_{dr} = v_i$, $\theta = \theta_0$ (i.e., given characteristics of the injected electrons are assumed).

Solutions of the formulated problem are presented in Fig. 6 for several magnitudes of the electric current in a short GaN diode. For this material, we estimate $J_O = 11 \times 10^3 \text{ kA/cm}^2$. To reach transient electron dynamics with the pronounced velocity overshoot, the currents j should be chosen with a large magnitude. The dependences $v_{dr}(z)$ and $\theta(z)$ presented in Fig. 6 are qualitatively similar to those obtained previously within the time-domain analysis. Consider, for example, Fig. 6(a) with the results plotted for $v_i = 0$ and $j = 0.1$. The drift velocity reaches its maximum at $z = 9.9$ where $\max v_{dr} = 1.94$, $\theta = 1.1$, $\mathcal{E} = 0.9$ (in the steady state at $\mathcal{E} = 0.9$, we obtain $v_{dr} = 1.3$). At larger distances, the velocity decreases while the temperature rises sharply. For the diode of the length $L = 20 \times l_O \approx 700 \text{ \AA}$, the current $j = 0.1$ corresponds to the voltage drop of $18.5 \times \hbar \omega = 1.68 \text{ V}$. Presented in Figs. 6(a) and 6(b) are the results for $j = 0.1$ calculated with different initial velocities of $v_i = 0$ and $v_i = 2\sqrt{\theta_0/\pi}$ (the thermal velocity), respectively. From the comparison of Figs. 6(a) and 6(b), one can see that the results are not strongly

dependent on the initial velocity of the injected electrons. The dependences plotted in Fig. 6(c) are calculated for larger current $j = 0.2$.

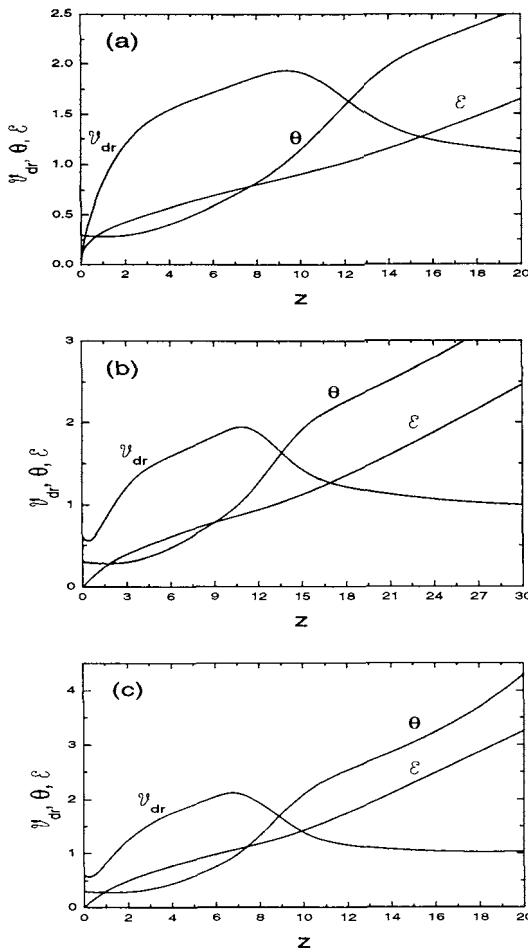


Fig. 6. Characteristic $v_{dr}(z)$, $\theta(z)$, and $\epsilon(z)$ for spatially dependent transport in GaN short diodes at a given current density j and electron velocity v_i at the virtual cathode. (a) $j = 0.1$, $v_i = 0$. (b) $j = 0.1$, $v_i = 0.6$. (c) $j = 0.2$, $v_i = 0.6$.

In general, we conclude that the overshoot observed in the present subsection is weaker and the electron heating is greater in the region of the peak velocity compared to those for the time-dependent problem. The transient processes are extended to sufficiently larger distances than those predicted by using the simple estimates made in the previous subsection. All these changes are caused by the spatial variation of the electric field due to the charge-limited transport at high electron concentrations.

5. Low-Concentration Regimes: Short Scale Devices

In this section, we will analyze the steady-state transport in short diodes under small concentrations of injected electrons. This case is interesting because extremely nonequilibrium electron distributions can be achieved, which makes new applications possible.

For small electron concentrations, the space-charge does not affect the transport and the electric field is almost constant across the device. Confining ourselves to the case of small/intermediate electric fields, we can neglect both the nonparabolicity and upper-valley effects. In contrast to the previous analysis, where two parameters v_{dr} and θ characterized the electron distribution, we now need to solve Eq. (1) and find the distribution function $f_c(p)$. Assuming only the optical phonon scattering, we rewrite Eq. (1) in the following form:

$$\begin{aligned} \frac{\partial f_c}{\partial p_z} + 2 \frac{\partial f_c}{\partial \zeta} p_z &= -\frac{f_c(\vec{p})}{\pi \mathcal{E}} \int \frac{d^3 p' \delta(p^2 - p'^2 - 1)}{(\vec{p} - \vec{p}')^2} + \frac{1}{\pi \mathcal{E}} \int \frac{d^3 p' f_c(\vec{p}') \delta(p^2 - p'^2 + 1)}{(\vec{p} - \vec{p}')^2} \\ &\equiv -\frac{1}{\mathcal{E}} [f_c(\vec{p}) a(p) - r(\vec{p})], \end{aligned} \quad (16)$$

where we introduce new dimensionless coordinate $\zeta = \mathcal{E}z$. The equation contains a single “controlling” parameter – the dimensionless field \mathcal{E} . Injection from the collector electrode and reflection of the electrons from this electrode are supposed to be absent and the distribution function of the injected electrons is assumed to be:

$$f_c(p_\perp, p_z, z = 0) = \frac{2}{\pi} n_0 \delta(p_\perp^2) \delta(p_z - p_i), \quad (17)$$

i.e., the electrons are injected with the concentration n_0 and initial momentum $p_z = p_i$. The resulting function $f_c(p_\perp, p_z | p_{\perp,i}, p_i)$ is, in fact, *the Green function* of the problem. To find the distribution function in the sample for any injected electron distribution, one should use this Green function and the “injection” distribution in an arbitrary form instead of Eq. (17).

We apply the following transformations to Eq. (16): $p_z = \pm \sqrt{w + \zeta}$ and $f_c(p_\perp, p_z, \zeta) = \Theta(p_z) \mathcal{F}^+(p_\perp, w, \zeta) + \Theta(-p_z) \mathcal{F}^-(p_\perp, w, \zeta)$. The functions \mathcal{F}^\pm are the solutions of equations:

$$\pm \frac{\partial \mathcal{F}^\pm}{\partial \zeta} = -\frac{1}{2\mathcal{E}} \frac{\mathcal{A}(p_\perp, w, \zeta)}{\sqrt{w + \zeta}} \mathcal{F}^\pm + \frac{1}{2\mathcal{E}} \frac{\mathcal{R}^\pm(p_\perp, w, \zeta)}{\sqrt{w + \zeta}}, \quad (18)$$

where \mathcal{A} and \mathcal{R}^\pm are obtained from the coefficients a and r of Eq. (16) by the transformation $p_z \rightarrow w$ discussed above. The boundary conditions to Eq. (18) are: $\mathcal{F}^+(p_\perp, w, \zeta = 0) = \frac{2}{\pi} n_0 \delta(p_\perp^2 + w - p_i^2) \delta(\sqrt{w} - p_i)$, $\mathcal{F}^-(p_\perp, w, \zeta = 0) = 0$.

For the injection conditions given in Eq. (17), we can expect that emission of dispersionless optical phonons should lead to electrons descending down the ladder of the total energy, $\epsilon = p_\perp^2 + w$: $\epsilon_0 = p_i^2$, $\epsilon_1 = p_i^2 - 1, \dots, \epsilon_s = p_i^2 - s$, where s enumerates the “energy stairs”. Then, the distribution function takes the following form:

$$\mathcal{F}^\pm(p_\perp, w, \zeta) = \sum_{s=0} \mathcal{F}_s^\pm(p_\perp, w, \zeta) = \sum_{s=0} \delta(p_\perp^2 + w - p_i^2 + s) \Phi_s^\pm(p_\perp, w, \zeta). \quad (19)$$

The δ function in Eq. (19) means that Φ_s is actually a function of two arguments and is non-zero when $\zeta \geq s + p_{\perp}^2 - p_i^2$. For the s^{th} -stair, we also introduce the functions R_s^{\pm} instead of \mathcal{R}^{\pm} by extracting the δ function:

$$\mathcal{R}^{\pm}(p_{\perp}, w, \zeta) = \delta(p_{\perp}^2 + w - p_i^2 + s) R_s^{\pm}(p_{\perp}, w, \zeta). \quad (20)$$

In such a formulation, the problem can be solved *exactly*. Indeed, let us consider the structure of Eq. (16). In terms of the function \mathcal{F}_s , this is an integro-differential linear equation, which can be considered as a set of coupled equations for the “energy stairs”. At a given w and p_{\perp} corresponding, say, to the energy stair s , the last integral term proportional to \mathcal{R} depends on the distribution function of the electrons with the energy $w + p_{\perp}^2 + 1$, namely, on the distribution of the previous “energy stair” ($s - 1$). For the stair $s = 0$, we obtain $\mathcal{R}^{\pm} = 0$ according to the boundary condition of Eq. (17) and, thus, the equation for \mathcal{F}_0^+ reduces to the *homogeneous* linear differential equation, which can be easily solved. With a known \mathcal{F}_0 , one can calculate the functions \mathcal{R}_1^{\pm} that enter into the equations for the electrons on the next energy stair $s = 1$. Thus, for $s = 1$ Eq. (18) becomes simply *nonhomogeneous* linear differential equation and \mathcal{F}_1^{\pm} can be found analytically. This allows one to calculate the functions \mathcal{R}_2^{\pm} , then obtain a simple equations for \mathcal{F}_2^{\pm} , etc. The general *recurrent* procedure of finding solutions for the s^{th} -energy stair can be found elsewhere.³⁰

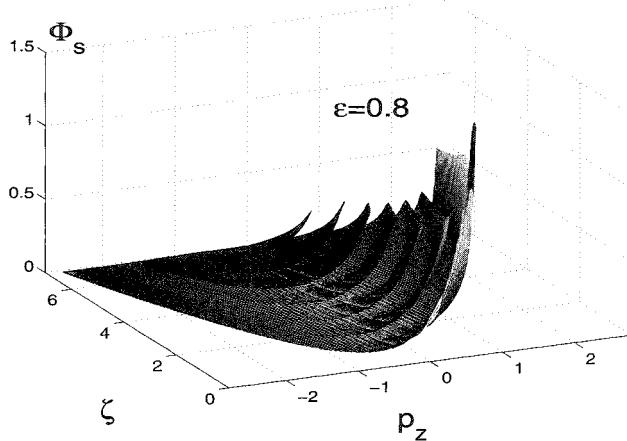


Fig. 7. Factors Φ_s as functions of p_z and ζ at $\epsilon = 0.8$; $s = 1, \dots, 7$. The results are depicted for the electrons with the initial momentum $p_i = 0.9$.

Now we can calculate the distribution functions in the form of Eq. (19), total populations of different energy stairs, and average velocities at different ϵ . For small ϵ (≤ 0.2), we found that for any ζ the electrons occupy approximately lowest energy stairs and Φ_s almost reproduce themselves. In other words, the distance-independent steady-state dissipative transport occurs.³¹ The gradual increase in the average energy and velocity with the distance is found at $\epsilon > \epsilon_{th} \approx 0.5$. This value can be interpreted as the threshold field for runaway field. In Fig. 7, we depict the

factors $\Phi_s(p_z, \zeta)$ for $\mathcal{E} = 0.8$ which is slightly above the threshold. The distance-independent nature is destroyed; they are considerably different for different s . At a given ζ , the factors are strongly asymmetric functions of p_z with sharp peaks near maximal $p_z = \sqrt{p_1 + \zeta - s}$. The electron population is now lower in the stairs with high kinetic energies. The distribution as a whole depends considerably on the coordinate ζ . This behavior corresponds to the beginning of the runaway effect.

Further increase in the field $\mathcal{E} > 1$ changes the distribution dramatically: The 0^{th} -stair remains the most populated for distances $\zeta \approx 10$. Moreover, the electrons are distributed over the two-three high-energy stairs ($s = 1\dots3$), while the lower stairs are almost empty. The developed runaway effect is reached under this field.

Evolution of the runaway effect can be studied by analyzing the average electron velocity as a function of ζ for different electric fields. Using the calculated \mathcal{F}^\pm as the Green function, we obtained the results for the electrons injected into the sample at $T_0 = 300\text{ K}$. These results are shown in Fig. 8 in terms of the dimensionless average velocity $v = \frac{V_z}{V_O}$ ($V_O = \sqrt{\frac{\hbar\omega}{2m_e}}$). Though the velocity magnitude under the runaway effect is below that of the ballistic case, the transport can be reasonably interpreted as *quasiballistic*.

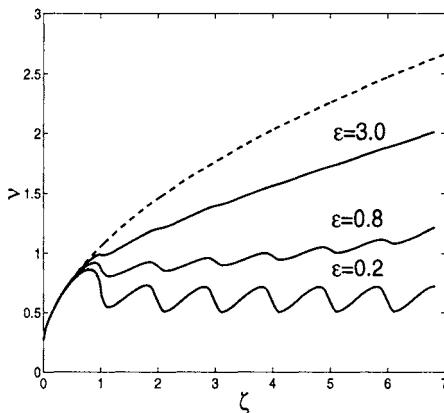


Fig. 8. Average velocity vs. distance dependence for different fields. For comparison, the velocity under the ballistic regime is shown by the dashed line.

A remarkable property of the developed runaway effect is the extremely nonequilibrium distribution of the electrons over the momentum and energy. In Fig. 9, we show the calculated electron population at the energy stairs under three different electric fields for the distance $\zeta = 7$. The results demonstrate the formation of *population inversion* as the field increases. At the small field $\mathcal{E} = 0.2$, the distribution is of usual character decreasing for higher kinetic energies. When the field increases up to about the threshold value $\mathcal{E} = 0.6$, the distribution becomes wider, but still decays with the energy. Above the threshold, the population inversion is apparently formed. At the high field of $\mathcal{E} = 3$, the populations at almost all the energy stairs are inverted, except for the highest one with $s = 0$.

To apply these results to a specific group III-nitride semiconductors, we need to calculate the following characteristic parameters: the length l_O , the field F_O , and

the velocity V_O ; the results are given in Table 1. All variables are scaled to these parameters.

Table 1. Relevant material parameters for the nitrides from Ref. 1. The GaAs parameters are given for comparison.

| Material | $l_O(\text{\AA})$ | $\tau_O(\text{ps})$ | $F_O(kV/cm)$ | $V_O(10^7 \text{ cm/s})$ |
|----------|-------------------|---------------------|--------------|--------------------------|
| InN | 90 | 0.04 | 99 | 2.65 |
| GaN | 35 | 0.018 | 257 | 2 |
| AlN | 12 | 0.01 | 828 | 1.35 |
| GaAs | 525 | 0.26 | 6.9 | 2.3 |

Then we shall estimate the conditions when the model described above can be applied to the nitrides. We neglect the optical phonon absorption processes, which is valid when the number of equilibrium optical phonons is small, i.e., the first criterion is $\exp(-\frac{\hbar\omega}{k_B T_0}) \ll 1$. If this inequality holds, the optical phonon scattering in the nitrides dominates for the electrons with the kinetic energies greater than $\hbar\omega$ and can be neglected for the energies less than $\hbar\omega$. Since at every energy stair there are electrons in the low energy region, we must find the respective criterion. Let τ_p be the momentum scattering time in this region. The time necessary to gain the kinetic energy equal to $\hbar\omega$ from the field F is $\tau_{eg} = \sqrt{2m_e\hbar\omega}/eF$. If $\tau_{eg} \ll \tau_p$, the scattering in the passive region can be neglected. We come to the second criterion of the dominant optical phonon emission: $F \gg \frac{\sqrt{2m_e\hbar\omega}}{e\tau_p}$. Thus, relatively low temperature and high fields are necessary to apply the model.

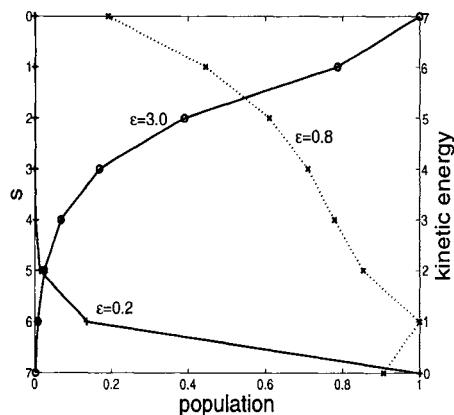


Fig. 9. Formation of population inversion with an increase in the field. The kinetic energy is given in the units of $\hbar\omega$, and the population is normalized to its maximum at each field. The results are obtained for $\zeta = 7$.

Using Table 1, we find that in the nitrides the first criterion is met for the temperatures below 300 K. Then, τ_p can be estimated from the mobility: $\mu = e\tau_p/m_c$, where the neglected mechanisms, such as scattering by acoustic phonons and impurities, contribute to μ . In terms of μ , the second criterion is: $\mu \gg \frac{V_O}{F} \equiv \frac{V_O}{\epsilon F_O}$.

From the data of Table 1 for the ratio V_O/F_O , we obtain $540 \text{ cm}^2/\text{Vs}$, $160 \text{ cm}^2/\text{Vs}$ and $35 \text{ cm}^2/\text{Vs}$ for InN, GaN, and AlN, respectively. For high quality nitrides, the contributions to the electron mobilities of the mechanisms, other than the optical phonon scattering, give values considerably larger than these numbers.¹

Next, in the proposed model, we neglected both nonparabolicity and upper valleys effects. Thus, the model is restricted to the consideration of moderate kinetic energies. For the developed runaway effect, the kinetic electron energy is of the order of the applied bias eU . Let us require the accuracy better than 20% for the calculation of the velocity, then we find the boundaries for the bias: $U_b = 0.43 \text{ V}$ and $U_b = 0.9 \text{ V}$ for InN and GaN, respectively. For AlN, the restriction comes from the intervalley transfer effect: $U_b \leq 0.7 \text{ eV}$. In terms of the optical phonon energies, the model is restricted to 5 energy steps for InN, 10 steps for GaN, and 7 steps for AlN. The restrictions in the applied voltage imply a restriction to the device length L . Indeed, the runaway effect occurs at $F > 0.5 F_{th}$, then, $F = U/L$ leads to $L \leq L_c = 2U_b/F_{th}$. This results in $L_c = 860 \text{ \AA}$, 740 \AA , and 170 \AA , for InN, GaN, and AlN, respectively.

In the case of GaAs, for comparison, the above criteria require $T_0 \leq 80 \text{ K}$ and $\mu \gg 6400 \text{ cm/Vs}$, which can be easily achieved. Then, we obtain $U_b = 0.27 \text{ V}$ (about 7 energy stairs) and sufficiently larger distance: $L_c \approx 4000 \text{ \AA}$.

Now we return to the discussion of the runaway effects. The characteristic electric fields, required to achieve the effect and given in Table 1, are below the breakdown fields. Other conditions discussed above may be met for nanoscale nitride devices. Next, the characteristic length l_O is a mean free path of the electrons between two sequential events of optical phonon emission at the electric fields $F \approx F_O (\mathcal{E} \approx 1)$. The small l_O and large F_O mean that purely ballistic transport does not occur in the nitrides: the transport is always *dissipative*. Once the runaway regime is reached in a short nitride-base device, this can provide electron velocities above $5 \times 10^7 \text{ cm/s}$.

Let us discuss briefly a possibility of observing the distributions characteristic for the runaway transport regimes in short-scale nitrides. It is known that in thin III-V-compound layers at low temperatures, where the collisionless regime occurs, the ballistic electrons can be observed and studied by using the hot-electron spectroscopy method.^{32,33} The method exploits a three terminal device, where the emitter and the base are separated by a thin barrier, and a relatively wide barrier is placed between the base and collector electrodes. The emitter barrier provides for the hot-electron injection controlled by the base voltage. The collector barrier is designed to avoid electron scattering and control the energy of electrons traversing the device by the base-collector voltage. Typically, the active part of the device is of about, or smaller than 1000 \AA for AlGaAs-GaAs and GaAs-AlGaAs-InGaAs structures. Using the injection principle of the ballistic electrons, a variety of monopolar hot-electron devices (transistors) has been proposed for ultra-fast operation.^{13,34}

Similar three terminal devices can be exploited to observe and measure the runaway effect in the nitrides. For this, the emitter barrier needs to be somewhat wider to satisfy the above discussed conditions for the effect, while the base and the collector barriers should be as thin as possible to avoid the scattering and perturbation of the electron distribution, and to allow the operation by the emitter-base and collector-base currents. For example, to measure the runaway effect in GaN, the

following InGaN-GaN-InGaN-GaN-InGaN heterostructures could be used. Three doped narrow-gap n^+ -InGaN layers are contacts. An i -GaN emitter barrier is of about 700 Å width. The collector barrier is an i -GaN layer of the width below 100 Å and designed to isolate electrically the base and collector (in general, it can be narrow InAlGaN layer, etc.). In such a device, the biased emitter barrier will provide the runaway electron transport and the collector barrier will control the energy of collected electrons. Using this spectrometer, one can prove the runaway effect by measuring the distribution of collected electrons at different emitter-base biases. The devices with identical layers, but wider emitter barriers should demonstrate higher energies of collected electrons at the same emitter-barrier field (until the conditions of the effect are fulfilled). Instead of the described all-solid-state spectrometer, one can extract the electrons traversing the emitter barrier and the base into vacuum, where the kinetic energy can be measured by means of the vacuum technique.³⁵ First experiments of this kind with hot electrons in AlN were reported recently.³⁶

6. Conclusions

We have analyzed the steady-state, transient time-dependent and spatially-dependent electron transport in the group III-nitride materials at high and ultra-high electric fields. Particularly, various transport regimes were investigated under the high electron concentration and the low concentration conditions.

When the electron concentration is high, the transport is characterized by cooperative dynamics of the electrons. Specifically, their distribution functions assume the shifted Maxwellian form with two parameters, the electron temperature and the drift velocity. These parameters should be found from the momentum and energy budgets *common* for all electrons. We have derived time-dependent differential equations for these parameters assuming that the optical phonon scattering is the dominant relaxation mechanism. Considering the importance of energy band structure for high-field transport, we performed a general investigation of two models for the conduction band, the single-valley model and multi-valley model, both of which take into account the nonparabolicity effects.

For the one-valley model, we found that the nonparabolicity parameter ν plays a crucial role. At $\nu = 0$, *two* stationary solutions exist at the electric fields less than the threshold value \mathcal{E}_{th} . One of these solutions corresponds to a stable steady-state regime, while the other is unstable. At the fields larger than \mathcal{E}_{th} , no stationary solutions exist at all. Then, at a certain interval of the nonparabolicity parameters there are *three* solutions. One of the solutions is stable in a finite field interval restricted by the value close to \mathcal{E}_{th} , and two others are unstable. At a larger nonparabolicity, only one solution exists which is stable again at fields less than \mathcal{E}_{th} . Despite the modification of the steady-state characteristics with ν , the one-valley model demonstrates a sharp increase in both the electron temperature and the drift velocity at the fields near \mathcal{E}_{th} . The time-dependent analysis of the one-valley model shows that at larger fields the runaway effect occurs.

The multi-valley model includes the central “light” valley and the upper “heavy” valleys. In the case of multi-valley model, the steady-state solutions exist at arbitrary fields. Using the material parameters typical for GaN, we have obtained

the current-voltage characteristic reasonably compatible with the published results available in the literature. Interestingly, at the fields $\mathcal{E} \approx \mathcal{E}_{th}$, we again found a sharp increase in the temperature and the velocity followed by electron transfer to the upper valleys. This sharp increase can be interpreted as a rudiment of the runaway effect characteristic for the one-valley model. We also studied various time-dependent transient regimes and found considerable velocity overshoot effect. It is widely accepted that the velocity overshoot occurs due to the difference in the momentum and energy relaxation times.^{12,13} Under the dominant and strongly inelastic scattering by the optical phonons, these relaxation times are of the same order. Instead of the usual interpretation, the overshoot effect can be thought as a manifestation of the runaway in the lower valley under a transient transport.

We calculated the temperature and the velocity as a function of time at different electric fields and different initial conditions. We found that the maximum of the velocity during the transient regime can be 2...2.5 times greater than that in the steady state. It was also noted that when the velocity reaches the maximum, the electron temperature remains of moderate magnitude but it increases considerably just beyond the acceleration period. This can give rise to a high level of hot electron fluctuations and degradation of the device parameters.

Under high electron concentrations the screening effect can be large, particularly in the short nitride diodes. We self-consistently obtained the spatially dependent electron temperature, drift velocity, and electric field in the diodes. We concluded that for the short diodes with the space-charge limited transport, the overshoot is weaker and the electron heating in the region of the peak velocity is greater than those found in the time-dependent problem. The transient processes are extended to sufficiently larger distances than it is predicted by the simple estimates assuming a constant electric field.

For the case of carrier transport under the low electron concentrations, we proposed a model which accounts for the main features of the injected electrons in a short device with high fields. The analysis resulted in the determination of the electron distribution as a function of momentum and real-space coordinates. The model has a single “controlling” parameter – the dimensionless electric field \mathcal{E} . We determined the critical field for the runaway regime (which almost coincides with \mathcal{E}_{th} obtained for the high electron concentrations) and studied this regime in detail. The electron velocity distribution over the device was found as a function of the field.

We analyzed the criteria and limitations, which allow one to apply the model to the particular nitrides – InN, GaN, and AlN. For these materials, we obtained the basic parameters and characteristics of the high-field electron transport. We estimated that the electron mean free path between two sequential optical phonon scattering is of the order of few nanometers. Thus, in most cases the transport in the nitrides is *always dissipative*. However, for the runaway effect regime, we found that the electrons progressively gain their energy and velocity. As a result, the average velocity can reach higher values than the peak velocity in the bulk-like samples. These results are in agreement with the published Monte Carlo numerical results on the transient electron transport in the nitrides. We also demonstrated that the runaway electrons are characterized by the extreme distribution function with a population inversion. We suggested a three-terminal heterostructure to observe and

measure the electron distribution under the runaway effect. These findings strongly indicate that the runaway effects are of major importance for high-field transport regimes in the group III-nitride nanoscale devices.

Acknowledgments

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Appendix A: Summary of Transport Integrals

In the integrals given below, one should use $\epsilon_l(x) = (\sqrt{1 + 4\nu_l x^2} - 1)/(2\nu_l)$ and besides take $l = c, s$, and $\gamma_c = 1$:

$$I_N^l(\theta, v_{dr}) = \frac{4\pi\theta}{\gamma_l v_{dr}} \int_0^\infty dx x \sinh \left[\frac{\gamma_l v_{dr} x}{\theta} \right] \exp \left[-\frac{\epsilon_l(x)}{\theta} \right]. \quad (A1)$$

$$I_P^l(\theta, v_{dr}) = \frac{4\pi\theta^2}{\gamma_l^2 v_{dr}^2} \int_0^\infty dx x \left\{ \frac{\gamma_l v_{dr} x}{\theta} \cosh \left[\frac{\gamma_l v_{dr} x}{\theta} \right] - \sinh \left[\frac{\gamma_l v_{dr} x}{\theta} \right] \right\} \exp \left[-\frac{\epsilon_l(x)}{\theta} \right],$$

$$I_E^l(\theta, v_{dr}) = \frac{4\pi\theta}{\gamma_l v_{dr}} \int_0^\infty dx x \epsilon_l(x) \sinh \left[\frac{\gamma_l v_{dr} x}{\theta} \right] \exp \left[-\frac{\epsilon_l(x)}{\theta} \right]. \quad (A2)$$

$$I_{Qp}^{l,j} = \frac{2\pi^2\theta^2}{\gamma_l^2 v_{dr}^2} \int_0^\infty dx \frac{M_{l,j}(x, \nu_l)}{x^2} e^{-\frac{\epsilon_l(x)}{\theta}} \left\{ \frac{\gamma_l v_{dr} x}{\theta} \cosh \left[\frac{\gamma_l v_{dr} x}{\theta} \right] - \sinh \left[\frac{\gamma_l v_{dr} x}{\theta} \right] \right\},$$

where $j=1, 2$ and

$$M_{l,1}(x, \nu_l) = \left(2\nu_l + \sqrt{1 + 4\nu_l x^2} \right) \left\{ 2x \sqrt{x^2 + \nu_l + \sqrt{1 + 4\nu_l x^2}} - (\nu_l + \sqrt{1 + 4\nu_l x^2}) \ln \left[\frac{\sqrt{x^2 + \nu_l + \sqrt{1 + 4\nu_l x^2}} + x}{\sqrt{x^2 + \nu_l + \sqrt{1 + 4\nu_l x^2}} - x} \right] \right\},$$

$$M_{l,2}(x, \nu_l) = \left(\sqrt{1 + 4\nu_l x^2} - 2\nu_l \right) \left\{ 2x \sqrt{x^2 + \nu_l - \sqrt{1 + 4\nu_l x^2}} - (\nu_l - \sqrt{1 + 4\nu_l x^2}) \ln \left[\frac{\sqrt{x^2 + \nu_l - \sqrt{1 + 4\nu_l x^2}} + x}{x - \sqrt{x^2 + \nu_l - \sqrt{1 + 4\nu_l x^2}}} \right] \right\} \theta [x^2 - (1 + \nu_l)]. \quad (A3)$$

$$I_{Q\epsilon}^{l,j} = \frac{4\pi^2\theta}{\gamma_l v_{dr}} \int_0^\infty dx Y_{l,j}(x, \nu_l) e^{-\frac{\epsilon_l(x)}{\theta}} \sinh \left[\frac{\gamma_l v_{dr} x}{\theta} \right], \quad j = 1, 2,$$

where

$$Y_{l,1}(x, \nu_l) = \left(\sqrt{1 + 4\nu_l x^2} - 2\nu_l \right) \ln \left[\frac{x + \sqrt{x^2 + \nu_l - \sqrt{1 + 4\nu_l x^2}}}{x - \sqrt{x^2 + \nu_l - \sqrt{1 + 4\nu_l x^2}}} \right] \times \theta [x^2 - (1 + \nu_l)],$$

$$Y_{l,2}(x, \nu_l) = \left(\sqrt{1 + 4\nu_l x^2} + 2\nu_l \right) \ln \left[\frac{x + \sqrt{x^2 + \nu_l + \sqrt{1 + 4\nu_l x^2}}}{\sqrt{x^2 + \nu_l + \sqrt{1 + 4\nu_l x^2}} - x} \right]. \quad (A4)$$

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HIGH FIELD TRANSPORT IN AlN

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The energy distribution of electrons transported through intrinsic AlN was directly measured as a function of applied field and AlN film thickness. The electron energy distribution featured kinetic energies higher than that of completely thermalized electrons. Transport through films thicker than 95 nm at an applied field between 200 kV/cm and 350 kV/cm occurred as steady-state hot electron transport following a Maxwellian energy distribution with a characteristic carrier temperature. At higher fields (470 kV/cm), intervalley scattering was evidenced by a multi-component energy distribution featuring a second peak at the energy position of the first satellite valley. Velocity overshoot was observed in films thinner than 95 nm and at fields greater than 510 kV/cm. In this case, a symmetric energy distribution centered at an energy above the conduction band minimum was measured, indicating that the drift component of the electron velocity was on the order of the "thermal" component. A transient transport length of less than 80 nm was deduced from these observations.

Keywords: High field transport; AlN; runaway.

1. Introduction

Experimental characterization of the electronic properties of aluminum nitride (AlN) is scarce and most of the current understanding originates from theoretical estimates. Besides the basic electronic properties (e.g., Hall mobility and carrier concentration), not much more is known about the nature of electron transport in AlN and transient effects have not been studied experimentally at all.

Considerable interest has arisen for the III-nitride based devices exploiting transient electron transport. Simulations and calculations done for GaN show that ballistic transport can occur at applied fields greater than 140 kV/cm.^{1,2} For AlN, the expected maximum overshoot has been predicted to occur at electric fields larger than 450 kV/cm.¹ A theoretical calculation of the electron energy relaxation time indicates that the predominant, limiting interaction is the electron-LO phonon scattering.³ Results of optical experiments that directly measured the scattering rates in wurtzite GaN^{4,5}, were found to be consistent with the model calculations, indicating scattering rates on the order of 10^{12} - 10^{13} s^{-1} .

In general, there are three basic types of electron transport in semiconductors:

(1) Steady-state thermalized transport occurs when the transport of electrons is confined to the conduction band minimum. In this case, the kinetic energy saturates at a certain value from which the drift velocity can be calculated. This type of transport is common in the working regime of most electronic devices, where the drift velocity of electrons can be approximated as a linear function of the applied electric field. This linear dependence defines the mobility under low-field conditions, which is a figure of merit for materials used for electronic devices.

(2) Steady state hot electron transport occurs when the energy gained by the electrons due to the acceleration in the applied electric field is not completely lost through various electron scattering mechanisms, i.e., primarily through electron-phonon interactions. Under hot electron transport conditions there is only a partial loss of energy due to these interactions, thus raising the carrier (electron) temperature to values higher than the host (crystal lattice) temperature.

(3) As an extreme case (usually in very thin films), transient (quasi-ballistic or ballistic) transport occurs when there is minimal or no energy loss to the lattice. Transient transport is characterized by an overshoot of the average electron velocity with respect to the steady state velocity.

The nature of electron transport through materials can be determined by directly measuring electron energy distributions (EED). This technique was used to characterize the high-field electron transport properties of AlN described in this chapter. The EED technique was developed using the knowledge acquired through research on field emission energy distribution (FEED) analysis⁶ and the proliferation of electron spectroscopy. The experimental procedure consists of extracting hot electrons into vacuum through a semitransparent electrode and performing direct measurements of their kinetic energy by means of an electron spectrometer. Figure 1 shows this procedure schematically. Different biases are applied across the semiconductor structure and between the top contact and the spectrometer. Measured energy spectra allow distinguishing between the aforementioned types of electron transport.

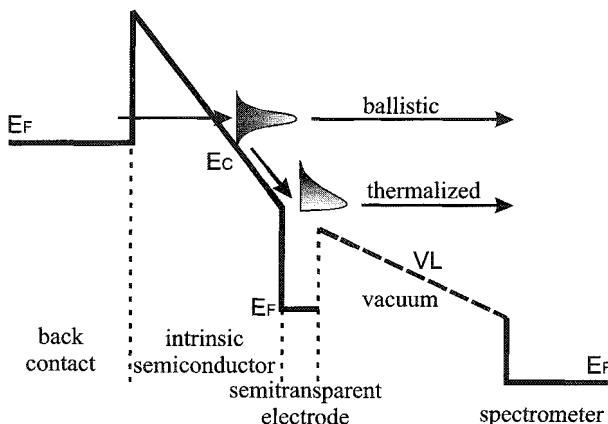


Figure 1. Basic experimental procedure for performing direct measurements of electron energy distribution. Electrons are injected from a back contact into the intrinsic semiconductor layer. The electrons are transported through this layer, and are extracted into vacuum through a semitransparent electrode.

This experimental technique is similar to a Tunneling Hot Electron Transistor (THETA) device,⁷ with the electron spectrometer being equivalent to the THETA collector. A THETA hot-electron spectrometer (with a tunnel emitter and an abrupt heterojunction collector barrier) was used in the works of Heiblum *et al* to characterize electron transport in GaAs.⁸ The analyzer plane is located at the collector edge of the

base-collector heterojunction barrier. Using such a heterojunction spectrometer, Heiblum et al. were able to make an unambiguous observation of ballistic electron transport. In contrast to the complexity of a THETA device, the structure needed to perform the measurements described in this work is simple and can be readily fabricated.

The direct measurement of EED was initially used to understand electron transport under strong electric fields through thin layers of SiO₂. Fitting performed experiments using electron emission from SiO₂ into vacuum to understand the electron heating during transport through this insulator.⁹ Thorough experiments addressing the problem of electron heating in SiO₂ were carried out by DiMaria *et al.* by means of electroluminescence and charge carrier separation in metal-oxide-semiconductor (MOS) structures and metal-oxide-semiconductor field effect transistor (MOSFETs), respectively, as well as field emission from MOS samples into vacuum.¹⁰ In this way, they obtained electron energy distributions from which the average electron energy was estimated, thus experimentally establishing conditions for hot electron transport.

In addition to SiO₂, Fitting et al. studied other semiconductor materials, including ZnS.¹¹ Their interest in ZnS was motivated by the development and understanding of thin film electroluminescent devices (TFELD). The field emission of hot electrons from Si-SiO₂-Au sandwich structures and from indium-tin-oxide (ITO)-Al₂O₃-ZnS-Au film stacks into vacuum was investigated by means of a spherical grid retarding field analyzer using electron counting by an electron multiplier. While the top, semitransparent gold electrode was grounded, the substrate electrodes (Si or ITO, respectively) were connected to a drive voltage to produce the desired field across the sample structure. By varying the grid voltage, the retarding field curve was recorded, and subsequently differentiated to yield the energy distribution. Measurement of field emission energy distribution is especially difficult with a retarding grid analyzer due to the exponentially decreasing electron count rate for energies below the Fermi energy and the severely reduced signal-to-noise ratio of the differentiated signal. Recently, the same group used the same technique to demonstrate hot and ballistic transport in GaAs under high-field conditions.¹²

In this chapter, we will describe the high-field electron transport properties of AlN through experiments performed and results obtained in the form of electron energy distributions (EED). In addition, we will briefly introduce the semi-classical Boltzmann transport theory in light of which the experimental observations are interpreted. Using these energy distributions, we were able to determine the carrier temperature as a function of applied field, and to establish the conditions for transient and steady state transport. Furthermore, material parameters and important electronic properties can be estimated from this information.

2. Semi-Classical Boltzmann Transport Theory

The Boltzmann transport theory deals with the effects of crystal imperfections, fields and gradients on the carrier transport in a semiconductor.¹³ In a completely homogeneous system (no gradients), imperfection scattering limits the momentum/energy gain of the

electrons as they are swept by an external field^a. Our experiments have been performed under these conditions.

The effects of the imperfections on the electron transport are calculated using the Fermi golden rule which results from first-order time-dependent perturbation theory.¹⁴ The transition rates between different states for scattered electrons given by the golden rule are calculated for Bloch states. Komirenko et. al¹⁵ studied the applicability of this formalism to calculate the transition rates for polar optical phonon scattering in the nitrides. Their results suggested that the standard perturbative treatment can be applied to GaN and AlN despite the relatively strong electron-phonon coupling in this material system, with intercollision times (τ) of the order of the period of the phonon oscillation. In the materials considered here, the condition for the applicability of the Fermi Golden rule, $\tau \gg \hbar/\Delta E$, where ΔE is the electron transition energy, is hardly met. Nevertheless, the results from Komirenko et al. justify the use of the formalism and the applicability of the Boltzmann transport theory for transport studies in the nitride semiconductors.

In the semi-classical treatment, the electron is described as having a well-defined position and momentum^b while the transition rates are calculated using Bloch states.¹⁶ For most semiconductors, this requires that the region of transport be larger than about 100 nm. In the nitrides, larger effective masses lower this limit, allowing us to use the formalism for the range of thicknesses investigated in the experiment.

The main assumptions, which justify the Boltzmann transport approach, are: (a) the carrier density should be sufficiently low so that only binary collisions occur, (b) the time between successive collisions τ should be long as compared to the duration of a collision τ_{coll} , and (c) the density gradients should be small over the range of the interparticle potential.¹⁷

2.1. The Transport Equation

In operator form, the Boltzmann equation can be written as¹⁷

$$\left(\frac{d}{dt} + I_k \right) f(\mathbf{k}, \mathbf{r}, t) = 0 \quad (1)$$

where $f(\mathbf{k}, \mathbf{r}, t)$ is the single particle distribution function and I_k is the scattering operator. The function $(4\pi^3)^{-1} f(\mathbf{k}, \mathbf{r}, t) d\mathbf{k} d\mathbf{r}$ gives the number of particles in $d\mathbf{r}$ at a position \mathbf{r} and in $d\mathbf{k}$ at a wavevector \mathbf{k} at time t . The one-electron approximation allows us the identification of a quantum state with the wavevector \mathbf{k} . Closely connected with this approximation is the band structure, which describes the energy $\epsilon(\mathbf{k})$ of the state \mathbf{k} as a function of \mathbf{k} . The equation of motion under the influence of an applied field is

$$\dot{\mathbf{k}} = \frac{e}{\hbar} \mathbf{E}(\mathbf{r}, t) \quad (2)$$

and the group velocity is given by

^a More generally, these statements remain valid for any charge carrier transported in a semiconductor.

^b This ignores the uncertainty relation $\Delta x \Delta k \approx 1$ for a wavepacket.

$$\mathbf{v}(\mathbf{k}) = \frac{1}{\hbar} \nabla_{\mathbf{k}} \epsilon(\mathbf{k}). \quad (3)$$

The scattering operator I_k describes the rate of change of $f(\mathbf{k}, \mathbf{r}, t)$ due to scattering with phonons and imperfections, thus interacting with the thermal bath. The effects of long-range Coulomb interaction between electrons (space-charge) and carrier-carrier scattering are neglected. Expanding the total time derivative of equation (1) into its implicit terms gives

$$\left(\frac{\partial}{\partial t} + \dot{\mathbf{k}} \cdot \nabla_{\mathbf{k}} + \mathbf{v} \cdot \nabla_{\mathbf{r}} + I_k \right) f(\mathbf{k}, \mathbf{r}, t) = 0. \quad (4)$$

The steady-state transport condition is established when $\frac{\partial f_k}{\partial t} = 0$, while in transient conditions the distribution function is an explicit function of time. Under steady state conditions, the 2nd, 3rd, and 4th term in equation (4) can be described as¹⁶

$$\left(\frac{\partial f_k}{\partial t} \right)_{\text{fields}} + \left(\frac{\partial f_k}{\partial t} \right)_{\text{diffusion}} + \left(\frac{\partial f_k}{\partial t} \right)_{\text{scattering}} = 0. \quad (5)$$

In the absence of any fields and diffusion gradients, the solution to equation (1) is the equilibrium distribution. For electrons, the equilibrium distribution is simply the Fermi-Dirac distribution with chemical potential μ at a temperature T , (which is equal to the lattice temperature)

$$f^0(\mathbf{k}) = \frac{1}{\exp\left(\frac{\epsilon_k - \mu}{k_b T}\right) + 1}. \quad (6)$$

This distribution function describes the equilibrium electron gas and is independent of any collisions that may be present. While the collisions will continuously remove electrons from one \mathbf{k} -state to another, the net distribution of electrons is always statistically given by the Fermi-Dirac function as long as there are no external influences to disturb the equilibrium. For non-degenerate semiconductors, the equilibrium function can be approximated by the Maxwell-Boltzmann distribution function at a temperature T

$$f^0(\mathbf{k}) = \exp\left(-\frac{\epsilon_k}{k_b T}\right) \quad (7)$$

The solution to the Boltzmann transport equation is a function that describes the distribution of the electrons in real and \mathbf{k} -space under different conditions away from equilibrium. While the Boltzmann equation looks quite simple in its form, it is an extremely complex integral equation. One approximation method used to solve this equation is the relaxation time approximation.¹⁶

2.2. Relaxation time approximation

Scattering processes are assumed to be local and instantaneous and change the state of the electron from \mathbf{k} to \mathbf{k}' . The transition rate from state \mathbf{k} to \mathbf{k}' is given by $W(\mathbf{k}, \mathbf{k}')$,^c if the

^c The scattering rate according to the Fermi golden rule is given by

$W(\mathbf{k}, \mathbf{k}') = \frac{2\pi}{\hbar} |H_{kk'}|^2 \delta(\epsilon(\mathbf{k}') - \epsilon(\mathbf{k}) - \Delta\epsilon)$ where $\Delta\epsilon$ is the energy change during scattering.

state \mathbf{k} is occupied and the state \mathbf{k}' is empty. The total transition rate is the sum of the transition rates due to different processes:

$$W(\mathbf{k}, \mathbf{k}') = \sum_i W_i(\mathbf{k}, \mathbf{k}'). \quad (8)$$

For any i th process the transition rate is assumed to be independent from field strength and is calculated by means of the time-dependent perturbation theory.¹³

To find the actual rate of transfer one must weigh the effect of occupation probability. The rate of change of the distribution function $f(\mathbf{k}, \mathbf{r}, t)$ due to scattering is¹⁷

$$\left. \frac{\partial f_k}{\partial t} \right|_{\text{scattering}} = I_k f(\mathbf{k}, \mathbf{r}, t) = \frac{1}{(2\pi)^3} \int (f_k' - f_k) W(\mathbf{k}, \mathbf{k}') d^3 k' \quad (9)$$

where the principle of microscopic reversibility has been assumed^d.

The relaxation time approximation allows us to write the scattering term in the following form¹⁷

$$I_k f(\mathbf{k}, \mathbf{r}, t) = \frac{f_k - f_k^0}{\tau}, \quad (10)$$

$f^0(\mathbf{k}, \mathbf{r}, t)$ is the equilibrium distribution, and τ is the relaxation time. The time τ represents the time constant for relaxation of the perturbation back to the equilibrium distribution. Generally, this relaxation time is related to the relaxation of momentum (τ_m) after an electron has gained momentum from an applied field.

Considering a uniform applied electric field in an infinite homogeneous system in the relaxation time approximation under steady state conditions, equation (4) becomes

$$\frac{e}{\hbar} \mathbf{E} \cdot \nabla_{\mathbf{k}} f_k + \frac{f_k - f_k^0}{\tau} = 0. \quad (11)$$

Rearranging equation (11), we obtain an expression for $f(\mathbf{k})$

$$f_k = f_k^0 - \frac{e}{\hbar} \tau \mathbf{E} \cdot \nabla_{\mathbf{k}} f_k. \quad (12)$$

Assuming small field intensities, the derivative of f_k can be approximated as the derivative of f_k^0 . This is called the diffusive approximation (a first order approximation) where¹³

$$\begin{aligned} f_k &= f_k^0 - \frac{e}{\hbar} \tau \mathbf{E} \cdot \nabla_{\mathbf{k}} f_k^0 \\ &= f^0 \left(\mathbf{k} - \frac{e\tau}{\hbar} \mathbf{E} \right). \end{aligned} \quad (13)$$

In \mathbf{k} -space the effect of the electric field is to shift the origin of the \mathbf{k} -space by an amount $e\tau\mathbf{E}/\hbar$. This type of distribution is called a "drifted" distribution, only valid at low field intensities. At higher fields, similar to the ones used in these experiments, the drifted distribution is a good approximation only if the temperature associated to the distribution is considerably higher than the lattice temperature and no intervalley scattering occurs. This temperature defines the electron temperature, thus the name "hot"

^d $W(\mathbf{k}, \mathbf{k}') = W(\mathbf{k}', \mathbf{k})$

electron transport referring to carrier temperatures higher than the lattice temperature. Higher temperature drifted distributions are far from the equilibrium distribution.

2.3. Scattering processes

The electronic transitions of interest in charge transport in semiconductors can be classified as (1) intravalley transitions, when the initial and final states of the electron lie in the same valley, or (2) intervalley transitions, when the initial and final states lie in different valleys. The most important scattering mechanisms that determine these transitions are phonon, defect, impact-ionization, and carrier-carrier scattering.^{16,17}

Defects can arise in a crystal owing to dislocations of different types and geometries, to impurities (neutral or ionized) due to extra atoms, and to the random distribution of component atoms among available lattice sites in alloys.

Impact ionization occurs when the carrier energy is close to or above the magnitude of the energy gap of the semiconductor. Related to this kind of scattering is the possibility of charge carrier multiplication, a phenomenon that leads to the electronic breakdown of the material.

The effect of carrier-carrier interaction is very limited under hot-electron conditions because of its electrostatic nature that results in a smaller efficiency at increasing carrier velocity.

The interaction of phonons with charge carriers can be due to lattice vibrations produced by the phonons, or to the electrostatic forces produced by the polarization waves that accompany the phonons. The electrostatic interaction, typical for polar materials, is called piezoelectric interaction in the case of acoustic phonons, and polar interaction in the case of optical phonons.

For polar semiconductors, under high field intensities, the most important scattering process is polar optical phonon scattering. To characterize the strength of the interaction one usually introduces the dimensionless Fröhlich coupling constant α defined by¹⁵

$$\alpha = \frac{e^2}{\hbar} \left(\frac{m}{2k_B \Theta_{op}} \right)^{1/2} \left(\frac{1}{\epsilon_\infty} - \frac{1}{\epsilon_0} \right) \quad (14)$$

where $\Theta_{op} = \frac{\hbar\omega}{k_B}$ is the phonon associated temperature, and $\epsilon_\infty, \epsilon_0$ are the optical dielectric constant and static dielectric constant, respectively.

In AlN, the Fröhlich constant is 0.75, falling in the intermediate range for the electron-photon coupling. The optical phonon branch with the lowest energy is the LO branch with 99.2 meV.¹⁸ The phonon population at equilibrium with the lattice is given by the Bose-Einstein distribution function as

$$N_q = \frac{1}{\exp\left(\frac{\hbar\omega_q}{k_B T}\right) - 1}. \quad (15)$$

The LO-phonon population in AlN at room temperature is negligible due to the large energy as compared to $k_B T$, thus the process of phonon absorption is quenched.

Therefore, in electron-optical phonon scattering, the process of phonon emission dominates the scattering and the overall transport at high fields.

Intervalley phonon scattering often is a dominant source of scattering, particularly at high electric fields. A requirement for scattering into a higher valley is a sufficiently large carrier energy, which needs to be at least close^e to the energy difference of the two valleys. Phonon absorption or emission may scatter the carriers into the upper valley, provided that the resultant energy is large enough for this transition and the resultant momentum magnitude and direction is compatible with the upper valley. The net result of this scattering in AlN is the removal of electrons from the central Γ valley into the upper energy satellite valleys. Intervalley scattering is directly related to the negative resistance effect or Gunn effect, common in GaAs devices.¹⁹

3. EED Experiment Description

The nature of electron transport through materials can be determined by directly measuring electron energy distributions (EED). This is only possible by extracting the electrons into vacuum through a semitransparent electrode and by subsequently measuring their energy with an electron spectrometer. The experimental device structure that allows such measurements consists of the semiconducting layer to be investigated, sandwiched between a semitransparent top electrode, and an Ohmic back contact. Electrons can be transported through the semiconductor and emitted into vacuum by the application of an electric potential between these two contacts, thus establishing an internal electric field that can be easily determined in this planar structure by knowing the thickness of the semiconducting layer. The bands of the semiconducting layer are bent due to the internal electric field. The energy of the conduction band at the surface can be used as an absolute reference to measure the kinetic energy of the electrons prior to their extraction into vacuum.

The test structure consist of an (0001) oriented AlN layer grown on a highly conductive, research-grade, n-type 6H-SiC substrate by metalorganic chemical vapor deposition (MOCVD).²⁰ Electrical contacts were deposited by electron beam (e-beam) evaporation in a UHV chamber. A complete description of the sample preparation and the experimental procedure can be found elsewhere.²¹

Figure 2 shows an I-V curve taken from the n^+ -SiC/*i*-AlN/Au structure. It shows a typical Schottky diode characteristic with a low series resistance under forward bias and a low leakage current under reverse bias. A large turn-on voltage in the forward direction indicated a large Schottky barrier at the SiC-AlN interface ($> 1\text{ eV}$). In typical experiments, the normal mode of operation was in the forward direction, so relatively large currents flowed through the sample.

^e For optical phonon mediated intervalley scattering, the minimum electron energy necessary for the valley transition is $E = \Delta E_{\Gamma L-M} - \hbar\omega$, where by absorbing a phonon the electron can move to the upper valley.

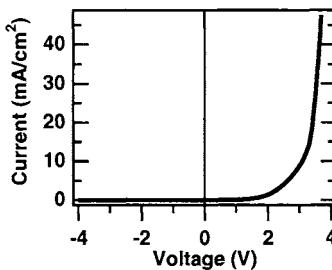
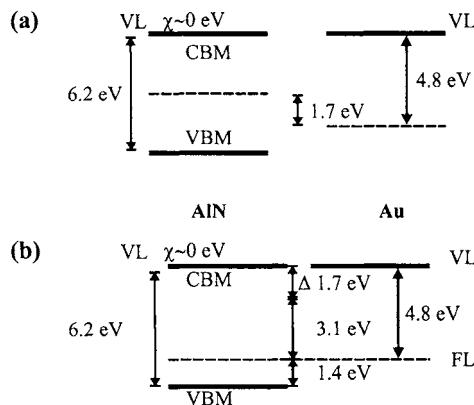


Figure 2. I-V curve taken from n+-SiC/i-AlN/Au structure.

Figure 3. Schematic of the band relations of the AlN/Au interface before (a) and after (b) forming the junction. The electron affinity of AlN was assumed to be close to 0 eV. An upward bending of the conduction band (Δ 1.7 eV) was observed after forming the junction.

In order to properly establish an energy reference for the electron energy spectra, the band structure of the SiC/AlN/Au structure had to be known. Precise knowledge of the band alignment at the interfaces is of crucial importance. The Schottky barrier height at the interface between SiC and AlN has been reported to be 2.5 eV.²² The core level X-ray Photoelectron Spectroscopy (XPS) technique, as described in previous references²³, was used to estimate the band bending of AlN at the Au interface. The valence band bending was determined by the relative shifts of the core level XPS peaks in presence of a thin layer of Au. Subsequently, the conduction band bending was derived from these data. An upward bending of $1.7 \text{ eV} \pm 0.2 \text{ eV}$ was estimated to occur in AlN at the AlN/Au interface. Consequently, the conduction band minimum of AlN lined up approximately with the vacuum level at the Au surface. Figure 3 shows the band relations of the AlN/Au interface before (a) and after (b) the formation of the junction. It is interesting to remark that AlN has been reported to feature a small, negative electron affinity²⁴, thus the vacuum level was assumed to be at the same energy as the conduction band minimum, as represented in Figure 3.

Figure 4 shows a simplified band diagram for the whole structure at equilibrium and under an applied bias. No voltage drop occurs at the back and top contacts due to their high conductivity. A constant 30 V accelerating bias was applied between the top

contact and the spectrometer as shown in Figure 4 (b). Under an applied bias, electron injection from the SiC layer into the AlN occurs by the tunneling mechanism. After tunneling through the heterojunction barrier between the SiC and the AlN, the electrons are transported through the AlN layer, while they interact with the lattice through various scattering mechanisms.

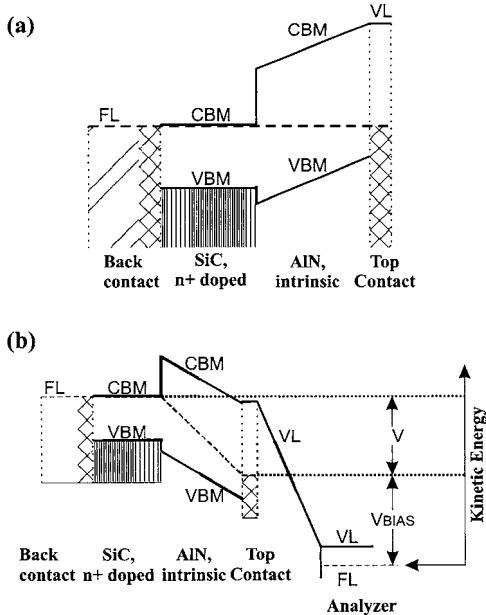


Figure 4. Band diagram of the Au-Ti/SiC/AlN/Au structure at equilibrium (a) and under an applied bias (b) and referenced to the Fermi level of the analyzer. The bold dashed lines represent the Fermi level across the whole structure.

4. Steady-State Hot Electron Transport

Figure 5 shows a cascade plot of energy distributions of extracted electrons referenced to the conduction band minimum of AlN, obtained at different applied fields across a 120 nm thick sample. As can be seen from the results (Figure 5), the electrons originated from close to the conduction band minimum. The observed peaks are characterized by a steep slope on the low kinetic energy side and a long tail on the high energy side. The steep slope on the low kinetic energy side is a result of the termination of available states at the conduction band minimum; there are no available states with lower energies. Under these experimental conditions, we expect the majority of the electrons to be completely thermalized, i.e., they lost all their gained energy to the lattice. The broad high-energy side should correspond to the fraction of the electrons that were not at equilibrium with respect to the lattice and remained "hot" after transport through the AlN.

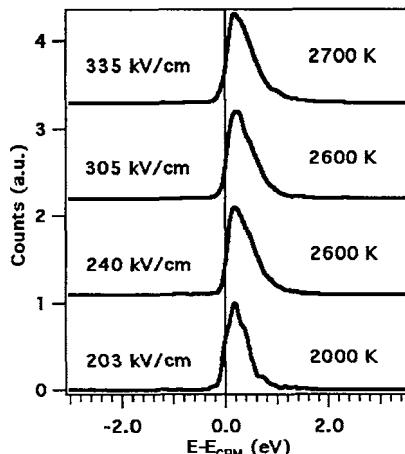


Figure 5. Cascade plot showing normalized electron energy distributions taken at different applied fields across the sample for a 120 nm thick AlN layer and resulting carrier temperatures.

The energy distribution of hot electrons during transport is traditionally described by an equilibrium distribution function at a temperature T_e higher than the lattice temperature. In the case of the central Γ valley of AlN, we can assume a parabolic three-dimensional conduction band minimum, resulting in a density of states increasing with the square root of energy. The density of states for a parabolic, three-dimensional conduction band is directly proportional to the effective electron mass of the semiconductor. Using this dependence, along with the Fermi-Dirac distribution at a higher temperature than the lattice and taking into account the finite resolution of the electron spectrometer by convolving the expected energy distribution with a Gaussian spectrometer transmission function, we were able to fit the measured energy distributions.^f Figure 6 shows the Fermi-Dirac distribution fitted to the experimental data corresponding to the energy distribution measured at 335 kV/cm. The measured distribution suggests an electron temperature of $2700 \text{ K} \pm 200 \text{ K}$. The carrier temperature in Figure 5 corresponds to the temperature used in the fitting of the energy distributions.

^fThe electron energy distribution is given by $\frac{dn}{d\varepsilon} = n'(\varepsilon) = \rho(\varepsilon)f_k(\varepsilon)$, where $\rho(\varepsilon)$ is the electron density of states and $f_k(\varepsilon) = \left[\exp\left(\frac{\varepsilon_k - \mu}{k_B T_e}\right) + 1 \right]^{-1}$ is the Fermi-Dirac distribution corresponding to a carrier

temperature T_e and μ is the chemical potential. The density of states in a three dimensional parabolic band is $\rho(\varepsilon) \propto \sqrt{\varepsilon}$. The measured energy distribution is a result of a convolution between the energy distribution and the spectrometer function $n'_{\text{exp}}(\varepsilon) = \int_{-\infty}^{\infty} I(\varepsilon, \varepsilon')n'(\varepsilon')d\varepsilon'$, where the instrument function is given by $I(\varepsilon, \varepsilon') = (\sqrt{2}\pi\Gamma)^{-1} \exp\left\{-\frac{1}{2}\left[\frac{(\varepsilon - \varepsilon')}{\Gamma}\right]^2\right\}$. The full width at half-maximum is related to Γ by $\Delta E_{FWHM} = 3.44\Gamma$.

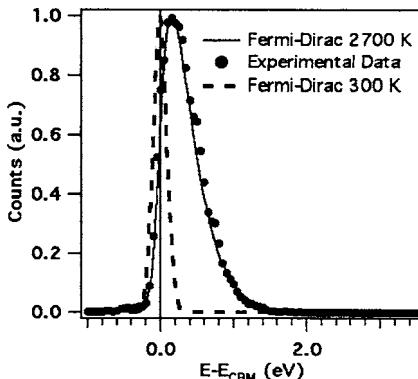


Figure 6. Normalized energy distribution for an applied field of 335 kV/cm. The Fermi-Dirac distribution has been fitted to the experimental data to estimate the carrier temperature. The calculated distribution takes into account the resolution limitations of the spectrometer (0.2 eV).

It should be noted that we neglected the non-parabolicity of the conduction band. Non-parabolicity increases the density of higher-energy states beyond the simple square root of energy dependence. Thus, neglecting the non-parabolicity generally leads to an overestimation of the electron temperature, as the increase in the high-energy tail of the distribution, resulting from the increase in the density of states, would be mistaken as a simple increase in electron temperature. In AlN, however, due to its large direct energy band gap of 6.2 eV, the non-parabolicity remains small as compared to other, narrower band gap semiconductors. The Kane model estimates the non-parabolicity coefficient for AlN to be as small as 0.044 eV⁻¹, as compared to Si and GaAs with non-parabolicity coefficients of 0.5 eV⁻¹ (X valley) and 0.610 eV⁻¹ (Γ valley), respectively.¹⁶ For the energy range considered here, the systematic error introduced by neglecting the non-parabolicity is expected to be less than half of the experimental error in the electron temperature data (± 200 K).

It is assumed that the quasi-Fermi energy describing the non-equilibrium carrier population close to the conduction band minimum of AlN is close to 0 due to a small number of carriers injected into the conduction band from the SiC. Under low injection current conditions the electron energy distribution can be approximated by a Maxwellian distribution, with the average carrier energy given by $w = 3k_B T_e / 2$. In the presence of the electric field, the electron gas is heated up and therefore it is no longer at equilibrium with the lattice.

Figure 7 shows a cascade plot of energy distributions of extracted electrons, obtained at different applied fields across the sample and an AlN layer thickness of 95 nm. A second prominent feature becomes evident at large fields. At fields of 470 kV/cm and 590 kV/cm, a second peak is located at 0.7 eV and 0.8 eV, respectively, above the conduction band minimum. This feature could be reproduced in many different measurements.

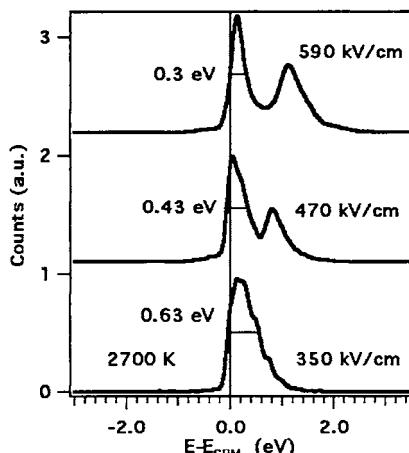


Figure 7. Cascade plot showing normalized electron energy distributions taken at different applied fields across a 95 nm thick AlN layer. Note the multi-component energy distributions at fields starting at 470 kV/cm.

The location of these second peaks with respect to the conduction band minimum of AlN suggests that these electrons underwent intervalley scattering into neighboring satellite valleys. In AlN, it is known that there are six L-M valleys and two K valleys parallel to the direction of the applied electric field in this experiment. Lambrecht et al.²⁵ place these valleys at 0.7 eV and 1.0 eV above the conduction band minimum, respectively. At and above 470 kV/cm, the electrons gained enough energy to populate these high-energy conduction band minima, and underwent transport at these higher energy states in the band structure. Sufficient carrier heating was necessary for the electrons to populate these higher satellite valleys. These multi-component energy distributions are no longer represented by a simple Maxwellian distribution; thus a single value for the carrier temperature cannot be extracted from the energy distributions. Monte Carlo simulations on bulk AlN show that the relative electron occupation of the satellite valleys increases as the electric field increases and, consequently, the population of the central valley decreases.²⁶

In the case of multi-component energy distributions, the density of states can no longer be described by the simple parabolic approximation. In this situation, the electrons already occupy higher satellite valleys with different densities of states. Intervalley scattering will effectively cool down the carrier distribution at the central valley, as electrons with higher energies are preferentially lost to higher conduction band satellite valleys. This corresponds to a decrease in the full width at half maximum (FWHM) of the main, low-energy peak as can be seen in Figure 7. This is in agreement with the traditional thermalization picture where both phonon scattering and intervalley scattering play a role in thermalizing electrons with higher energies.

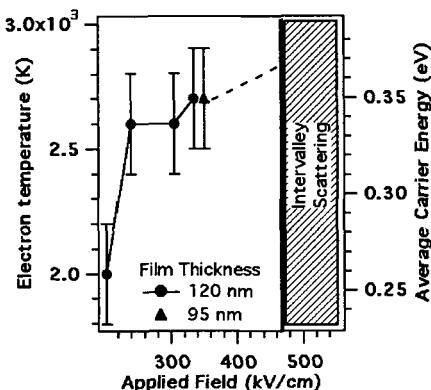


Figure 8. Average carrier energy and corresponding carrier temperature for the different lengths as a function of the applied field.

Figure 8 shows the carrier temperature and average carrier energy under different applied fields. As the electric field was increased, the carriers were continuously heated during transport through thicker layers until the onset of intervalley scattering (470 kV/cm). Intervalley scattering occurs during hot electron steady-state transport.

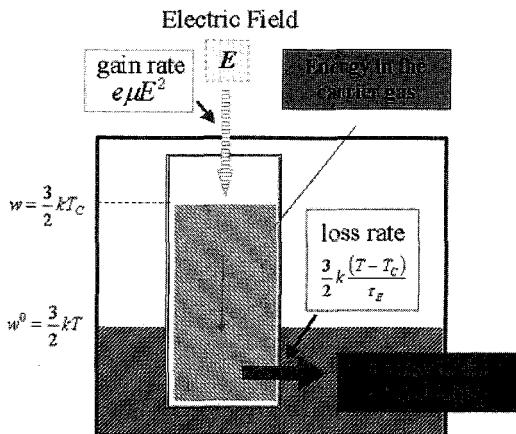


Figure 9. Schematic representation of the carrier energy balance indicating the energy gain from an applied electric field E and the energy loss to the crystal lattice. At steady state for $E \neq 0$ the mean carrier energy is always greater than the mean thermal energy.

Some energy gained by the electron gas through the applied field is lost to the lattice through diverse scattering mechanisms. Under steady state conditions, the energy gain rate is equal to the loss rate, thus sustaining an electron temperature higher than the lattice temperature. Figure 9 shows a schematic description of this relationship. The time scale in which this energy loss occurs is limited by the energy relaxation time (τ_E). Processes occurring within this time only partially relax their energy. Therefore, the energy relaxation time establishes the time scale within which transient effects take place.

5. Transient Electron Transport

Transient transport is characterized by the onset of ballistic or velocity overshoot phenomena. It takes place in spatial lengths in the sub-micron range, and occurs in rapidly changing applied fields or immediately after the application of a field. In AlN, this phenomenon is expected to occur for transport lengths of less than 100 nm, and field strengths greater than 450 kV/cm.¹ Ballistic transport can be simply described by the acceleration of an electron immediately after the application of a field: inertial effects limit the acceleration of the electron, while subsequent scattering events start randomizing the momentum and limiting the energy, thus causing the system to eventually reach a steady state. Nevertheless, a velocity overshoot with respect to the steady-state velocity is obtained before the steady state is reached. The energy relaxation time characterizes the time scale of this overshoot²⁷, which is usually of the order of tenths of picoseconds.

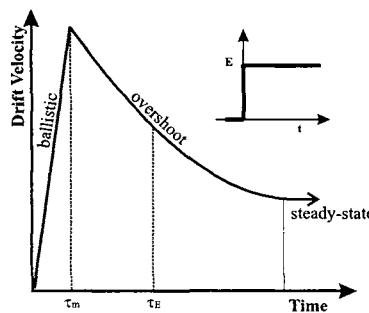


Figure 10. Transient drift velocity versus time resulting from a time-step configuration of the electric field. The curve can be divided in three regions: ballistic, velocity overshoot and steady state.

Transport with velocity overshoot occurs between the limit of the ballistic transport and before it reaches a steady-state transport condition. The velocity in this regime is still higher than the steady-state velocity but slightly smaller than the ballistic velocity. This is shown diagrammatically in Figure 10. In this transient regime, the energy increases progressively from the equilibrium energy (thermal energy) towards its steady-state value.²⁷ The overshoot effect can be explained in the following way: the electron mobility decreases with increasing average carrier energy for most semiconductors; as a result, the instantaneous drift velocity reaches higher values at the beginning of the motion when the average carrier energy is close to the thermal energy and thus the mobility will keep a value higher than that of the steady state.

Energy distribution of electrons which traversed an 80 nm thick AlN film was measured. Figure 11 shows a cascade plot of energy distributions for different applied electric fields. In a first order approximation, under an applied field E , a carrier momentum distribution function is given by $f_p = f_p^0(p - e\tau_m E)$, where τ_m is the momentum relaxation time, and p is the electron momentum. If the distribution is of Maxwellian type, the carrier energy is given by $w = 3kT_e/2 + m^*v_d^2/2$, where the first term represents the thermal component at an electron temperature T_e and the second term the

drift component corresponding to the electron drift velocity v_d and an effective mass m^* . In a thermal distribution, the drift component of the energy is negligible as compared to the thermal component, especially if the carrier temperature is higher than the lattice temperature. A symmetric energy distribution, however, indicates that the drift component of the carrier energy cannot be neglected, even though some carrier thermalization may have occurred. Usually, this condition is observed as a transient effect, leading to a drift velocity overshoot or, as an extreme case, ballistic transport. The electron energy distributions corresponding to fields greater than 560 kV/cm were clearly symmetric around a specific energy above the conduction band minimum and shifted towards higher energies as the field was increased. These symmetric distributions were not observed for thicker AlN layers in the same range of applied fields.

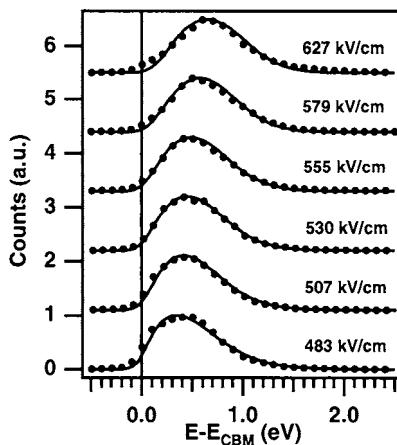


Figure 11. Cascade plot showing normalized electron energy distributions taken at different fields across the sample for an AlN layer 80 nm thick. The solid lines represent the best fits of the experimental data to the drifted Fermi-Dirac distribution.

The relaxation time approximation can be used to characterize the drift component of the distribution. The drifted, or displaced, momentum distribution is $f_p = f_p^0(\mathbf{p} - m^* \mathbf{v}_d)$ in the first order approximation. Considering a Fermi-Dirac distribution and a parabolic band approximation, the energy distribution can be written as

$$f(\epsilon, \cos\theta) = \left[\exp\left(\frac{w_d + \epsilon - 2 \cos\theta \sqrt{\epsilon w_d}}{k_B T_e} \right) + 1 \right]^{-1}, \quad (16)$$

where the drift component of the energy is given by $w_d = m^* v_d^2 / 2$. The distribution depends on the angle between the carrier momentum and its drift component, θ . As the drift component becomes considerable with respect to the thermal component, the energy distribution will become more pronounced in the forward direction. A completely thermal distribution will have spherical symmetry. Under our experimental conditions, angle-dependence could not be measured; instead, angle-averaged electron energy distributions were recorded. If the drift component of the energy is at least half as large as the thermal

component, the distribution can be assumed to be completely oriented in the forward direction,²⁸ thus $\langle \cos \theta \rangle \approx 1$. Moreover, the metallic top contact and the electron analyzer act as electron lenses, averaging the actual angular distribution. Considering this angle averaging, the energy distribution becomes

$$f(\varepsilon) = f(\varepsilon, \langle \cos \theta \rangle) = \left[\exp\left(\frac{w_d + \varepsilon - 2\sqrt{\varepsilon w_d}}{k_B T_e} \right) + 1 \right]^{-1}. \quad (17)$$

Using this expression, we fitted the experimental electron energy distributions obtained from an 80 nm thick AlN layer; results are shown in Figure 11. The fitting procedure, which takes into account the conduction band density of states and a peak broadening induced by the finite resolution of the spectrometer, is described in the previous section. For all the experiments, the energy scale was referenced to the bottom of the AlN conduction band. The drift energy and the carrier temperature were obtained as fitting parameters.

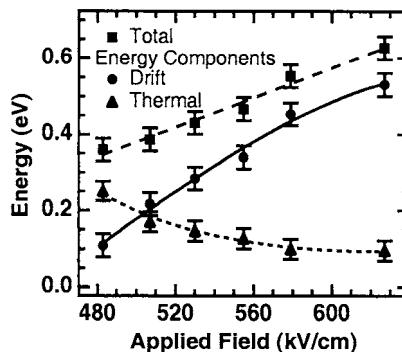


Figure 12. Drift and thermal component of the average carrier energy as a function of field strength for the energy distributions shown in Figure 12. The total average carrier energy is the sum of both energy components. The lines are visual guidelines only.

In all the measurements, the average angle θ was close to 0° , as the value of the drift energy was comparable to the thermal component of the average carrier energy. Figure 12 shows the field strength dependence of the drift and the thermal energy. The average carrier energy as a function of field strength is also shown.

For low fields, and in particular in the case of steady-state distributions, the drift component is smaller than the thermal component. As can be seen in Figure 12, the total average carrier energy increases monotonically with the applied field and the drift component becomes higher than the thermal component for fields greater than ~ 510 kV/cm. This is a signature of velocity overshoot. Figure 13 shows the drift velocity characteristic curves for this field range. Data points are calculated for the two values of effective electron mass used in previously published Monte Carlo simulations.^{29,26} The error bars are estimated from the ± 0.03 eV uncertainty in the drift energy fit parameter.

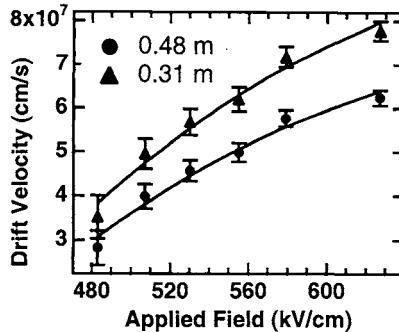


Figure 13. Drift velocity characteristic curves for a transport length of 80 nm. Effective electron masses of 0.48 m_0 and 0.31 m_0 are used for this curve. The solid lines are visual guidelines only.

In transient effects, the effective mass plays an important role in determining the overshoot velocity. For example, at a field of 627 kV/cm, the drift velocity is 6×10^7 cm/s for an effective electron mass of 0.48²⁹, while an effective electron mass of 0.31²⁶ yields a drift velocity of 7.7×10^7 cm/s, or 30 % higher. These values are approximately five times higher than the respective saturation velocities. We do not expect the drift velocities reported here to be the maximum overshoot velocities; it is likely that the transient length in AlN, defined as $\ell_E \approx v_d \bar{\tau}_E$, is smaller than the layer thickness of 80 nm investigated here. Experiments using thicker samples indicated that for transport lengths of 100 nm steady-state transport was already realized.

6. Summary

Energy distributions of electrons that were transported through an *i*-AlN film were used to characterize the high-field transport properties. A Au-Ti/ n^+ -SiC/*i*-AlN/Au structure was used for this purpose. After the semi-transparent top Au electrode had been completely characterized and its continuity verified, bending of the AlN conduction band at the Au interface was determined. These measurements provided a suitable reference frame for subsequently recorded energy distributions. In all cases, the electron energy distributions featured kinetic energies higher than that of completely thermalized electrons. These distributions were described by a free electron gas at a temperature higher than the lattice temperature. In addition, different conditions for steady-state and transient transport were identified. During the steady-state transport, sufficient heating of the carriers resulted in the intervalley scattering.

Transient transport under high electric fields was identified to occur in AlN. Velocity overshoot, a characteristic of transient transport, was recognized from a large drift component of the average carrier energy. These parameters were determined by fitting the experimental energy distributions to a drifted Fermi-Dirac distribution. Overshoot drift velocity characteristic curves were estimated from the drift component of the energy for two different values of the effective electron mass. Overshoot as high as five times the expected saturation velocity^{26,29} was observed for the highest applied

electric fields. From these observations, we determined that the transient length for AlN is likely to be shorter than the transport length used for these experiments, i.e. 80 nm.

Acknowledgments

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GENERATION-RECOMBINATION NOISE IN GaN-BASED DEVICES

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AlGaN thin films and Schottky barrier Al_{0.4}Ga_{0.6}N diodes exhibit generation-recombination (GR) noise with activation energies of 0.8 - 1 eV. GR noise in AlGaN/GaN Heterostructure Field Effect transistors (HFETs) corresponds to activation energies in the range from 1 - 3 meV to 1 eV. No GR noise is observed in thin doped GaN films and GaN MESFETs. GR noise with the largest reported activation energy of 1.6 eV was measured in AlGaN/InGaN/GaN Double Heterostructure Field Effect Transistors (DHFETs). Local levels responsible for the GR noise in HFETs and DHFETs might be located in AlGaN barrier layers.

Keywords: 1/f noise; generation recombination noise; III-nitrides.

1. Introduction

GaN-based Field Effect Transistors (FETs) have potential for high temperature, high power, high frequency, and radiation hard applications.¹⁻³ GaN/AlGaN FETs can operate in a wide temperature range from cryogenic temperatures up to several hundred degrees Celsius.⁴ When these devices are used as oscillators or mixers in microwave and optical communication systems, their low frequency noise is one of the major factors determining the phase noise characteristics. Low frequency noise measurements are also a powerful tool to study impurity and defects in semiconductor structures^{5,6} and to diagnose quality and reliability of semiconductor devices.⁷ The first measurements of the low-frequency noise in GaN films were reported in 1998 in Ref. 8. Since that time, several groups have reported on the low frequency noise properties of III-Nitrides and GaN-based devices (see reviews in^{9,10}).

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Low frequency noise in semiconductors and semiconductor devices is a superposition of the $1/f$ noise and generation-recombination noise. In this paper, after a brief summary of the recent results on the $1/f$ noise, we review in detail the recombination-generation (GR) noise in GaN-based devices. The GR noise provides valuable information about localized states and might dominate the overall low frequency noise in some frequency ranges.

2. $1/f$ noise: Brief Summary

The $1/f$ noise level in different semiconductor materials and structures is usually characterized by the dimensionless Hooge parameter, $\alpha = (S/I^2)fN$, where N is the total number of the carriers in the sample, f is the frequency, $S_{1/f} = S/I^2$ is the relative spectral density of the $1/f$ noise.¹¹ The values of α for semiconductors vary by several orders of magnitude depending on the material properties and structural perfection. For example, in silicon (Si) and gallium arsenide (GaAs) the values of α range from 10^{-8} to 10^{-2} .^{12,13}

The typical values of α for GaN vary from 10 in thin ($1\mu\text{m}$) layers to 5×10^{-2} in $20\mu\text{m}$ thick high quality GaN layer (electron mobility $\mu_n = 790\text{ cm}^2/\text{Vs}$ at 300 K).^{14,15} The lowest value of $\alpha=2 \times 10^{-3}$ was reported for thin (60 nm thick) GaN films^{16,17} and MESFETs¹⁸⁻²⁰ with a relatively high electron concentration (10^{18} cm^{-3} at 300 K) and low electron mobility $\mu_n \approx 100\text{ cm}^2/\text{Vs}$. Typical values of $\alpha=10^{-3}-10^{-4}$ in GaN/AlGaN Heterostructure Field Effect Transistors (HFETs) are smaller than in GaN layers.^{21,22}

Many different $1/f$ noise sources in field effect transistors might be important, including the contact noise, channel noise, surface noise and gate leakage current noise.

To evaluate the contribution of the gate leakage current, we measured the gate current fluctuations in GaN/AlGaN HFETs^{23,24} and calculated the contribution of gate current fluctuations to the output noise. The correlation between the gate and drain current fluctuations was measured and analyzed as well. In the majority of devices, the gate current gives only small contribution to the overall low frequency noise.^{23,24}

To determine the contribution of the contact noise to the measured noise spectra, the noise measurements were performed on the TLM structures. Assuming that the contributions from contact noise and from channel noise are not correlated and taking into account that the contact resistance is much smaller than the channel resistance, we calculated the dependence of noise on the distance L between the contact pads. In the limiting case when the contact noise is dominant, the spectral noise density, S/I^2 , should be proportional to L^2 . In the opposite limiting case, we have $S/I^2 \sim L^1$. Since the experimental dependence was close to the I/L law, we concluded that contacts do not contribute much to the overall noise.¹⁸

To determine the relative contributions from the channel and the surface to the overall noise, we measured the gate voltage dependence of noise in HFETs at small drain voltages (linear regime).²⁵ We found that depending on the surface preparation, passivation, etc., the open surface might strongly contribute to the total noise. This agrees with the conclusion of the recent paper reporting on the low frequency noise in submicron GaN HFETs, where the surface of the ungated regions was shown to contribute to the $1/f$ noise.⁵⁷ For all measurements reported here, we selected transistors with negligible contribution of the surface noise. (For the devices with highly defective surface, the surface noise might become dominant.)²⁵

To determine the location of the noise sources in the channel, we studied concentration and temperature dependencies of the $1/f$ noise in GaN-based HFETs.²⁶⁻²⁸

We found that in spite of the differences in the absolute values of α , the $\alpha(n_s)$ dependencies are almost identical for all the structures. At low channel concentrations, α decreases with the increase of n_s , as $\alpha \sim 1/n_s$, then α reaches a minimum and increases with a further increase of n_s . Similar α versus $1/n_s$ dependencies were found for AlGaN/InGaN/GaN Double Heterostructure Field Effect Transistors (DHFETs). In contrast, noise measurements in GaN MESFETs showed no gate voltage dependence of the Hooge parameter α .^{18, 29}

The dependence $\alpha \sim 1/n_s$ indicates that the spectral density S_f does not depend on the channel concentration. Such situation is very typical for Si MOSFETs, where the noise arises from the electron tunneling from the semiconductor to traps in the oxide. Hence, the observed $\alpha \sim 1/n_s$ dependence might be linked to the electron tunneling from the 2D gas into the tail states in GaN or AlGaN.

It can be attributed to the electron spillover from the 2D-channel to a parallel low electron-mobility "parasitic conduction" channel. The noise level in such "parasitic channel" could be very high.

Measurements of the noise at temperatures from 8K to 300K in GaN-based FETs showed that noise originated from the 2D channel depends only weakly on temperature.

In contrast, the noise temperature dependence in the special structures with Si doped GaN layer adjoining the channel, showed a clear maximum. In Ref.^{30, 31}, we showed that this maximum might be explained by the tunneling of electrons from the channel to the Si level in GaN. A model based on this mechanism gives a reasonable agreement with experimental results. However, it needs further verification.

3. Generation-Recombination Noise in GaN Thin Films and MESFETs

The GaN thin films studied in References¹⁶⁻²⁰ were grown by low pressure Metal Organic Chemical Vapor Deposition (LP-MOCVD) on sapphire substrates.¹⁶⁻²⁰ The deposition of approximately 2 μm of nominally undoped GaN was followed by the growth of a Si-doped GaN layer. The thickness and doping level of that layer (extracted from capacitance-voltage characteristics) were ~60 nm and 10^{18} cm^{-3} , respectively. The electron Hall mobility was close to $\mu = 100 \text{ cm}^2/\text{Vs}$ at 300 K. MESFETs fabricated on these films had the source-drain spacing of 4 μm and the gate length of 1.5 μm .

Fig. 1 shows the temperature dependence of noise for one of the GaN MESFETs. As seen from the figure, the weak noise maxima shifted to higher temperatures at higher frequencies. This behavior is typical for the GR noise caused by a local level. However the level of GR noise was weak compared to the $1/f$ noise. The Arrhenius plot for this GR noise yields the activation energy of 0.4-0.5 eV.

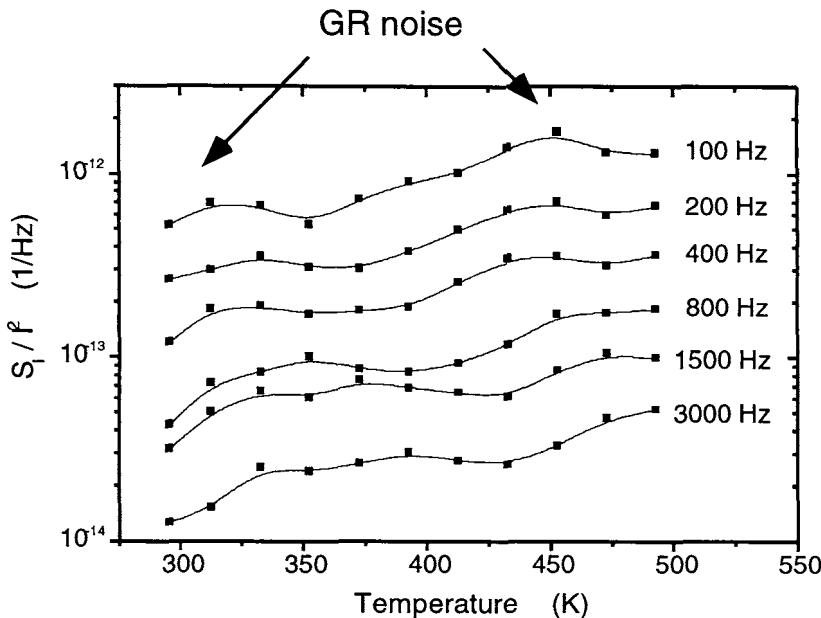


Fig. 1 Temperature dependencies of noise S_I/I_d^2 for GaN MESFET at different frequencies in linear regime.¹⁸

4. Generation-Recombination Noise in AlGaN Thin Films

The measurements of the low frequency noise in AlGaN films have been reported in Ref. 32–34

$\text{Al}_{0.4}\text{Ga}_{0.6}\text{N}$ thin (50 nm) films were grown by LP-MOCVD on sapphire substrate. A 50 nm AlN buffer layer was followed by the deposition of a 1 μm insulating AlGaN layer and a 50 nm n-AlGaN layer with the doping level of approximately $5 \times 10^{18} \text{ cm}^{-3}$. Figure 2 shows the temperature dependencies of the noise spectral density S_I/I^2 at a number of frequencies. In the temperature interval between 420 and 520 K, these dependencies exhibit a maximum. (A sharp decrease of noise at temperatures 300–350 K might be linked to the contribution to noise from another local level.)

As seen, the temperature T_{max} corresponding to the maximum noise at given frequency, increases with frequency, which is typical for the GR noise caused by a local level. The slope of $1/kT_{max}$ versus $\ln(f)$ (the Arrhenius plots) dependence yields the activation energy $E_a \approx 1 \text{ eV}$.

Let us estimate what is the minimum concentration of the level responsible for GR noise assuming that the centers are located in the bulk. The spectral noise density of the bulk GR noise (see Ref.⁶) is given by:

$$\frac{S_I}{I^2} = \frac{4N_{nv}}{Vn^2} \frac{\tau F(1-F)}{1 + (2\pi f\tau)^2}, \quad (4)$$

where N_n is the trap concentration, V is the sample volume, n is the electron concentration, f is the frequency, τ is the time constant associated with return to equilibrium of the level occupation, and F is the occupancy function.

As discussed in Ref.⁶, the activation energy of GR noise is the sum of level energy position E_0 and activation energy E_l of temperature dependence of level capture cross section. Following the procedure described in Ref.⁶, we plotted the dependence of the noise at maximum $\log(S_{max})$ versus $\log(f)$ and found the slope of this dependence to be equal to unity. This indicates that $E_l \gg E_0$, i.e. a relatively shallow surface local level is responsible for the GR noise in AlGaN films. For the studied AlGaN layers the doping level $N_d = 5 \times 10^{18} \text{ cm}^{-3}$ is about the same as the effective conduction band density of states and hence the Fermi level is located very close to the conduction band edge. Therefore, in order to estimate the lower bound of the level concentration we can set $F=0.5$.

Taking $F=0.5$, $n=N_d$, $(S/I^2)=S_{max}$ and $\tau=1/2\pi f$,⁶ we get $N_n=2.4 \times 10^{19} \text{ cm}^{-3}$. Since this is a lower bound of the level concentration and it is about one order of magnitude higher than the doping level N_d the assumption of the bulk noise level location can be considered as unrealistic.

In thin AlGaN layers, GR noise might originate from a surface level. An approach for extracting the local surface level parameters from noise spectroscopic data was proposed in Ref.³⁵ If the concentration of the levels is high enough so that this level determines the position of the Fermi level at the surface (surface Fermi level pinning), all level parameters can be extracted.

Let us assume that a local level with concentration N_{ls} and energy position E_{ls} exists at the surface of a semiconductor structure (see Fig. 3). A current I flows through the channel of thickness t (see inset in Fig. 3). On one side, the channel is bounded by the space charge region (SCR) of thickness a , formed as a result of the depletion caused by the surface charge. Fluctuations of the level occupancy cause fluctuations of the SCR width a . The fluctuations δa lead to fluctuations of the channel thickness $t = h_0 - a$ and, consequently, to the current fluctuations, δI .

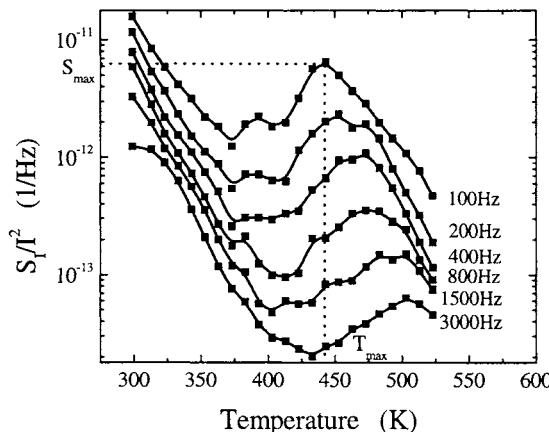


Fig. 2 Temperature dependencies of noise in $\text{Al}_{0.4}\text{Ga}_{0.6}\text{N}$ thin films at different frequencies.^{32,33} (© 2002, IEEE)

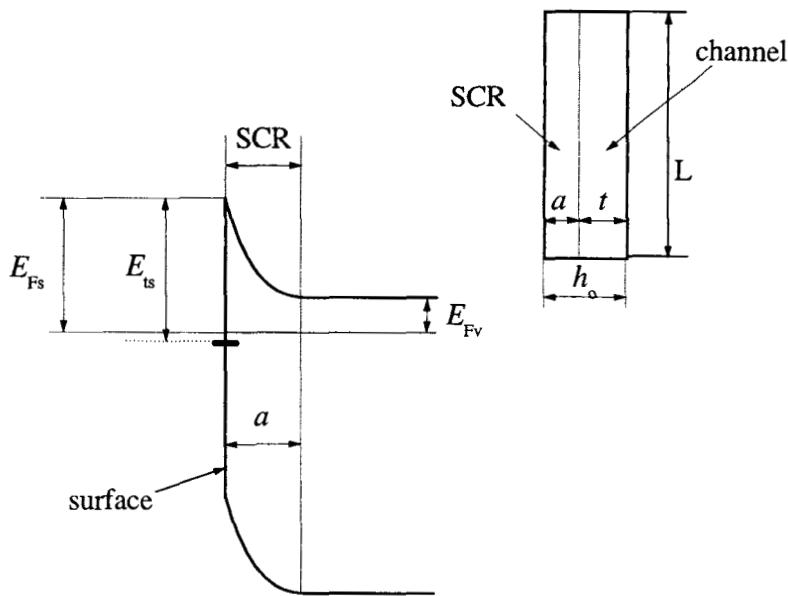


Fig. 3 Qualitative surface band diagram at surface of the thin film. Inset shows schematically a cross-section view of the sample.³⁵

Let us first estimate what is the minimum concentration of the surface level, in order to satisfy the electro-neutrality condition:

$$FN_{ts} = aN_d \quad (1)$$

Here N_{ts} is the surface level concentration, F is the Fermi-Dirac occupancy function of the level under consideration. Space charge region thickness a is given as

$$a = \left(\frac{2\epsilon_0 e V_s}{e N_d} \right)^{1/2} \quad (2)$$

where ϵ is the dielectric constant of the semiconductor, ϵ_0 is the permittivity of vacuum, e is the electron charge, $V_s = \frac{E_{Fs} - E_{Fv}}{e}$ is the surface potential, and N_d is the doping level

The position of the Fermi level in the bulk, E_{Fv} , is determined by the doping level N_d and temperature T . Taking $F=0.5$, $N_d=5\times 10^{18} \text{ cm}^{-3}$, and $V_s=1.0 \text{ V}$ we find $N_{ts} \approx 1.5 \times 10^{13} \text{ cm}^{-2}$.

The upper bound of N_{ts} can be also found from Eq. (7) of Ref.³⁵

$$N_{ts} = 4S_{\max} N_d^2 t^2 \pi f A, \quad (3)$$

where S_{max} is defined in Fig.2, $t=3.5\times10^{-6}\text{cm}$, is the thickness of the conducting layer, $A=1.3\times10^{-5}\text{cm}^2$ is the surface area involved in the measurement, and f is the frequency. Eq. (3) gives $N_{ls} \approx 3\times10^{13}\text{cm}^{-2}$, which is in qualitative agreement with the previous estimate. Hence, the assumption of the surface location of noise sources lead to a rather high but still reasonable surface concentration.

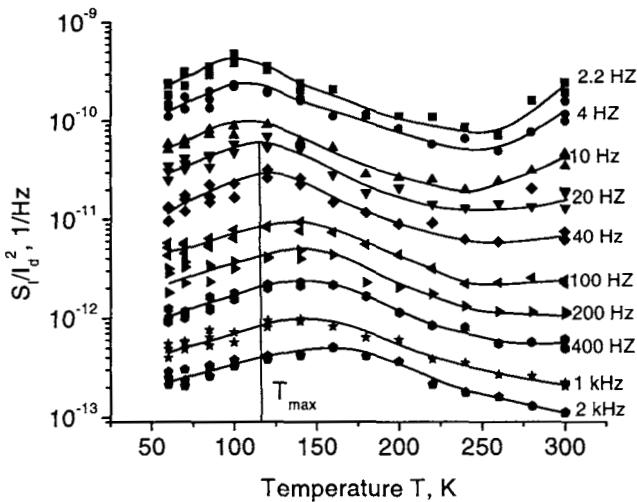
5. Generation-Recombination Noise in AlGaN/GaN Heterostructure Field Effect Transistors (HFETs)

The generation-recombination (GR) noise was reported for the first time in GaN/AlGaN HFETs grown on sapphire substrate in Refs. ^{36, 37}. The temperature dependence of low-frequency noise revealed a contribution to the noise from a local level with the activation energy, E_a , of approximately 0.42 eV. ³⁷ The level with activation energy $\Delta E = 0.35\text{ eV}$ in AlGaN/GaN heterostructures grown on high-doped ($N_d = 2\times10^{18}\text{ cm}^{-3}$) GaN layers was reported in Ref. ³⁶. In Ref. ³⁸ both noise spectroscopy and deep-level transient spectroscopy (DLTS) techniques were used to investigate the GR noise in AlGaN/GaN HFETs. The levels with $\Delta E \sim 0.85\text{ eV}$ for the samples grown on a sapphire substrate and with $\Delta E \sim 0.20\text{ eV} - 0.36\text{ eV}$ for the samples grown on SiC substrate were observed. ³⁸ The nature of these levels and the location of the GR noise sources were not identified.

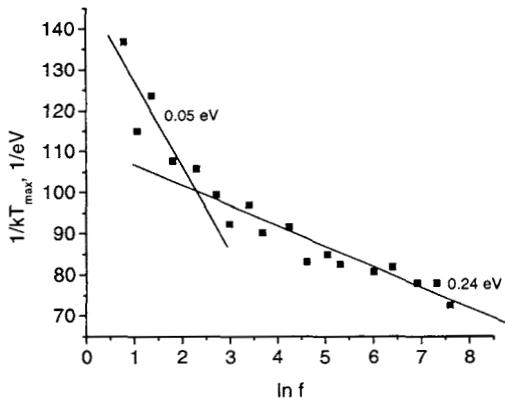
We investigated three types of GaN based HFETs: 1) conventional AlGaN/GaN HFETs, ^{4,30} 2) SiO₂/AlGaN/GaN MOSHFETs, ^{4,39} and 3) AlGaN/InGaN/GaN Double Heterostructure Field Effect Transistors (DHFETs). ^{40,41}

5.1. GR noise in HFETs at low temperatures ^{30, 42}

AlGaN/GaN heterostructures were grown by LP-MOCVD on 4H-SiC-substrate. A deposited 50 nm AlN buffer layer was followed by the deposition of a 0.4 μm insulating GaN layer. Some structures included a 50 nm n-GaN layer with an estimated doping level between $2\times10^{17}\text{ cm}^{-3}$ and $5\times10^{17}\text{ cm}^{-3}$ ("doped channel HFETs"). Heterostructures were capped with a 30 nm Al_{0.2}Ga_{0.8}N barrier layer, which was doped with silicon approximately to $2\times10^{18}\text{ cm}^{-3}$. The measured room temperature Hall mobility and sheet carrier concentration were $1150\text{ cm}^2/\text{Vs}$ and $1.2\times10^{13}\text{ cm}^{-3}$, respectively. The transistors had source-drain spacing L_{SD} of 5 μm , the gate length L of $\sim 1.5\text{ }\mu\text{m}$, and gate width W in the range of 150 -250 μm .



(a)



(b)

Fig. 4 Temperature dependencies of noise in AlGaN/GaN HFETs at $V_g=0$ (a). The $1/T_{\max}$ vs $\ln f$ dependence (Arrhenius curve) plotted with the data of Fig. 4a in the temperature interval from 50 K to 150 K (b). Arrhenius plot manifests clearly the presence of two local levels with energy activation of 0.05 and 0.24 eV. Gate voltage $V_g = 0$.⁴²

Fig. 4a shows the temperature dependencies of noise at different frequencies.⁴² As seen in the figure these dependencies have broad maxima in the temperature range from 50 K to 150 K. Fig. 4b shows the $1/T_{\max}$ versus $\ln f$ dependence (Arrhenius curve) plotted using the data of Fig 4a. The Arrhenius plot clearly demonstrates that two levels with activation energies of $\Delta E = 0.05$ eV and 0.24 eV contribute to the GR noise. At relatively low temperatures, the noise from a shallow level dominates. With a temperature increase, (i.e. the Fermi level shifting down), the deeper level gives the main contribution to the

noise. Measurements of the gate voltage dependence of noise showed that, at gate voltage $V_g \sim 0$, the noise only weakly depends on V_g . As shown in Ref.⁴² this noise behavior indicates a dominant contribution to noise from the open surface of the gate-to-source and gate-to-drain regions.

Fig. 5 shows the noise spectra at lowest temperatures $T < 50$ K. In the doped channel HFETs a clear contribution of GR noise superimposed on $1/f$ noise is seen. The activation energy of this GR noise was estimated to be 1 – 3 meV.³⁰

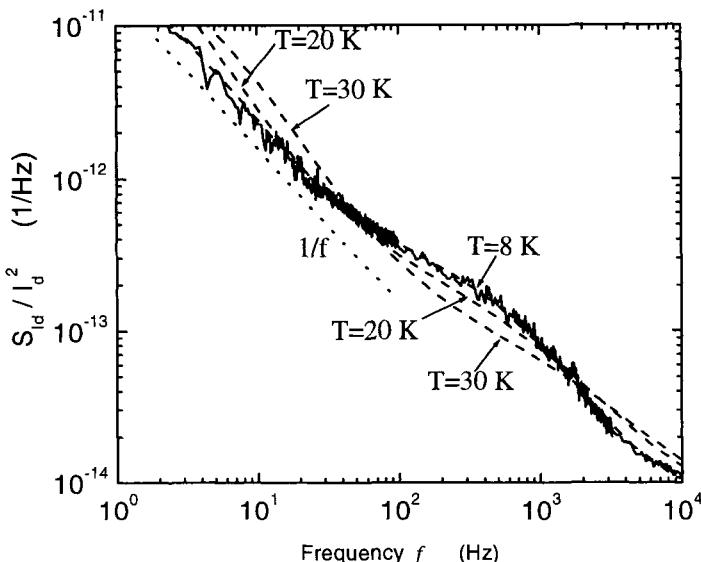


Fig. 5 Noise spectra at $T < 50$ K.³⁰

5.2. GR noise in HFETs and MOSHFETs at high temperatures⁴

Heterostructures for MOSHFETs were grown in the same process as HFETs. In order to fabricate MOSHFETs a 7 nm SiO₂ layer was deposited on part of the heterostructures using plasma enhanced chemical vapor deposition (PECVD) to fabricate MOSHFET devices.

Fig. 6 shows the temperature dependencies of the relative noise density of short circuit drain current fluctuations S/I^2 for conventional AlGaN/GaN HFETs (a), and for AlGaN/GaN MOSHFETs (b) in the frequency range from 110 Hz to 3200 Hz. The $S/I^2(T)$ dependencies for both types of devices exhibited a broad maximum. The temperature of the maximum, T_{max} , increases with frequency. The S_{max} value decreases with the frequency increase.

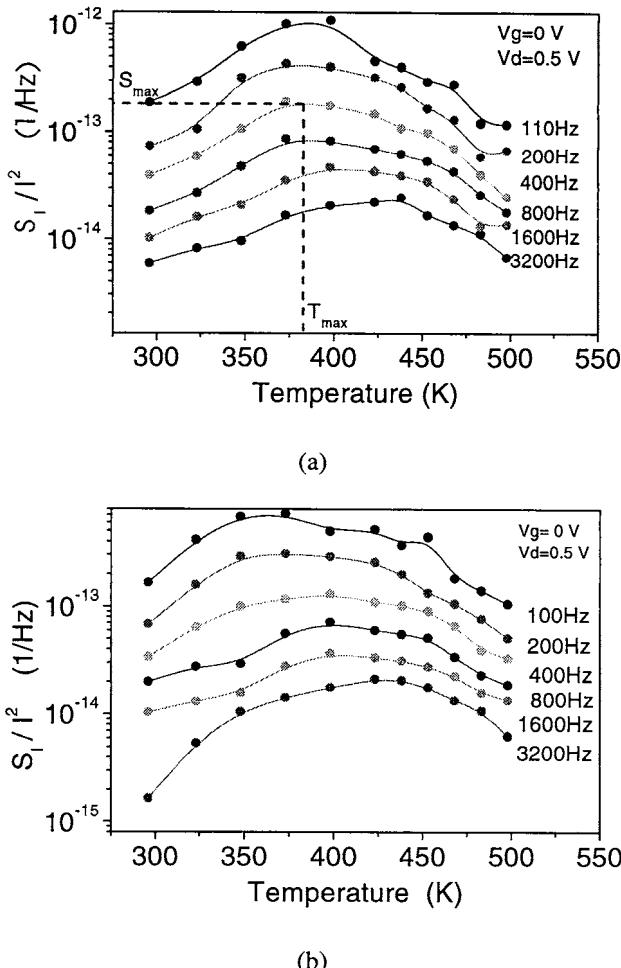


Fig. 6 The temperature dependencies of relative current noise density for conventional AlGaN/GaN HFETs (a) and for SiO₂/AlGaN/GaN MOSHFETs (b) from the same wafer at different frequencies of analysis f . Gate voltage $V_g = 0$, drain-source voltage $V_{ds} = 0.5 \text{ V}$. ⁴ (© 2001, IEEE)

Fig. 7 shows the dependencies of $1/kT_{\max}$ versus $\ln f$ (the Arrhenius plots) for several HFETs and MOSHFETs samples. Since the maxima on $S_I/I^2(T)$ dependencies are rather broad, we can only establish that the activation energy is in the range between 0.8 and 1 eV. As can be seen from Fig. 9, this energy is approximately the same for HFETs and MOSHFETs. The difference in the noise dependencies between HFETs and MOSHFETs structures does not exceed the difference between the data for different HFETs samples.

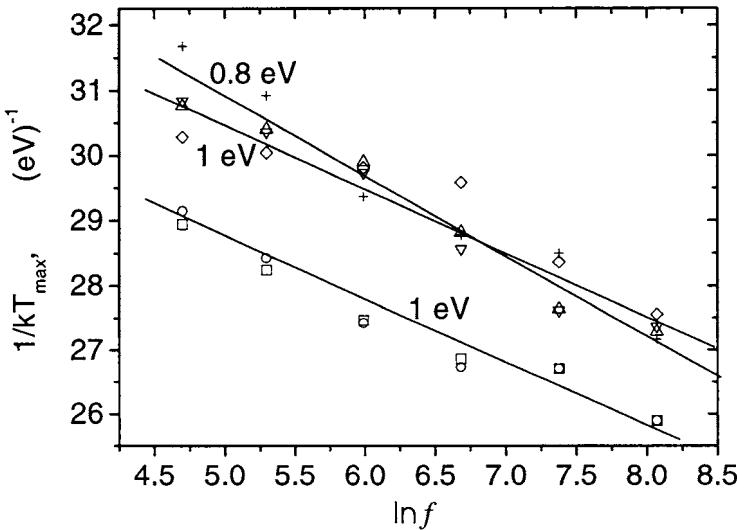


Fig. 7 The $1/kT_{max}$ versus $\ln f$ (the Arrhenius plots) for several samples of conventional HFETs and MOSHFETs. Crosses represent MOSHFET. All other symbols represent HFETs. The slope of the lines determines the characteristic activation energies of local level $E_a \approx 0.8 - 1.0$ eV.⁴ (© 2001, IEEE)

5.3. GR noise in Heterostructure Field-Effect Transistors (DHFETs)⁴¹

AlGaN/InGaN/GaN DHFETs attracted attention since they showed no current collapse in either the pulsed I - V or the RF output power characteristics.⁴⁰

The double heterostructures were grown by LP-MOCVD and consisted of a 1.4 μ m thick undoped GaN buffer layer on insulating 4H-SiC substrate, followed by 50 Å In_xGa_{1-x}N layer with $x < 0.1$ and capped by a 250 Å Al_{0.25}Ga_{0.75}N layer. Traces of indium were present through the structure and played an important role in improving the overall materials quality. Transistors with the gate length and width of 1.5 μ m and 200 μ m and source-drain separation of 5 μ m and transmission line model (TLM) test structures were fabricated. The room temperature Hall mobility and sheet carrier concentration for the deposited DHFET structures were measured to be 800 cm²/Vs and 1×10^{13} cm⁻³, respectively.

Fig. 8 shows the temperature dependencies of the noise spectral density S/I^2 for the frequency range from 100 Hz to 3000 Hz. The dependencies have a wide and pronounced maximum at elevated temperatures. The temperature T_{max} corresponding to the maximum noise increases with frequency revealing the GR noise caused by a local level.

Fig. 9 shows the dependence of $1/kT_{max}$ versus $\ln(f)$ (the Arrhenius plots). The slope of this dependence gives the activation energy $E_a = 1.6$ eV. This is the largest activation energy reported for GaN based devices.

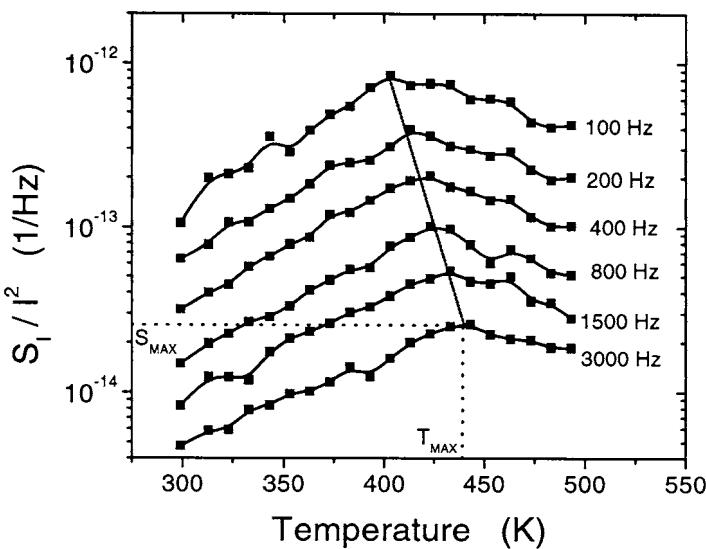


Fig. 8 The temperature dependencies of low frequency noise in AlGaN/InGaN/GaN DHFETs at different frequencies of analysis.⁴¹

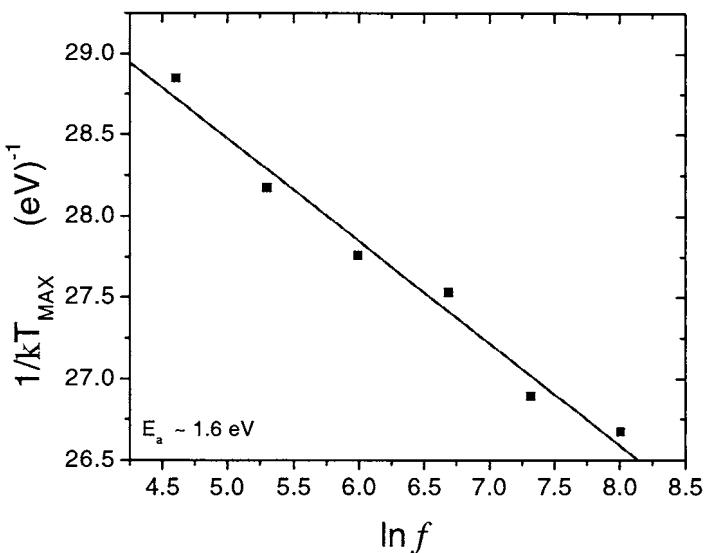


Fig. 9 The $1/T_{\max}$ vs $\ln f$ dependence (Arrhenius curve) plotted with the data of Fig 6. Slope gives the activation energy as 1.6 eV.⁴¹

5.4. Discussion of the GR noise nature in HFETs

As mentioned above, the nature and the location of the levels responsible for GR noise are not yet clear. Let us show, however, that these levels cannot be localized in the GaN/GaAlN HFETs channels.⁴

For a two-dimensional (2D) case, the expression for relative spectral noise density S/I^2 generated by the single trap in the channel has the following form⁶

$$\frac{S_I}{I^2} = \frac{4N_{ts}}{L_0 W n_s^2} \frac{\tau F(1-F)}{1 + (\omega\tau)^2} \quad (5)$$

where N_{ts} is the trap sheet concentration, L_0 and W are the channel length and width respectively, n_s is the electron sheet concentration, $\omega = 2\pi f$ is the circular frequency, $\tau = \tau_c F$ is the time constant associated with return to equilibrium of the occupation of the level, τ_c is the capture time constant

$$\tau_c = \frac{1}{\sigma n_s v_F} \quad (6)$$

where $v_F = \sqrt{2E_F/m^*}$ is the electron velocity at the Fermi level.

For the 2D degenerate electron gas ($F \approx 1$), the capture cross section is given by:

$$\sigma \approx \frac{1}{\tau n_s v_F} \quad (7)$$

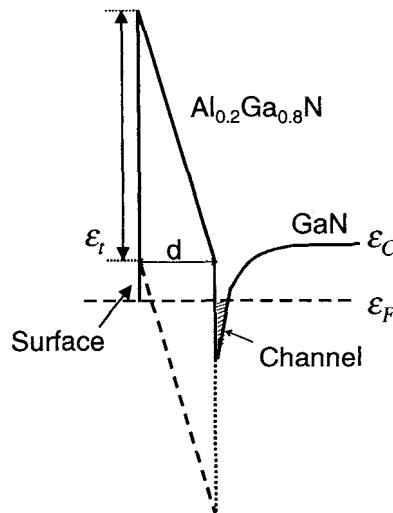


Fig. 10 Schematic of band diagram illustrating possible GR noise mechanism in AlGaN/GaN HFETs assuming the noise sources localized in AlGaN barrier layer.⁵⁶

Local level located at 1eV below the Fermi level is practically fully occupied by the electrons ($(1-F) \approx 10^{-17}$). The estimates using Eq. (5) yield unrealistically large concentration of traps responsible for the observed GR noise. Hence, we conclude that the source of low frequency generation-recombination noise cannot be located in the 2D channel.

Another possible location of the traps responsible for generation recombination noise is in the fully depleted AlGaN barrier layer including AlGaN surface at the gate side (see Fig. 10). Shallow levels in GaN which coincide with the Fermi level at small distance from the channel might also contribute to GR noise.

The GR noise from the traps in the AlGaN layer can be approximately described by Eq. (5), where N_{ts} is replaced with $N_t d$. Here N_t is the volume concentration of traps and d is the thickness of the AlGaN layer. In this case, the time constant τ is given by the Shockley-Hall-Read theory. For zero free carrier concentration within the depletion region and for the level location in the upper half of the energy gap, the expression for τ can be written as^{44,45}

$$\tau = \tau_0 \exp(E_t / kT) \quad (8)$$

where $\tau_0 = (\sigma_n v_n N_c)^{-1}$ and N_c is the density of states in the conduction band. Differentiating Eq. (4) with respect to $1/T$ and setting the derivative equal to zero, we find:

$$\frac{1}{kT_{\max}} = \text{const} - \frac{1}{E_t} \ln \omega \quad (9)$$

With E_t known, the time constant τ_0 can be found from Eq. (8):

$$\tau_0 = \frac{1}{\omega} \exp\left(-\frac{E_t}{kT_{\max}}\right) \quad (10)$$

and electron capture cross section of the level can be found as

$$\sigma_n = \frac{1}{\tau_0 v_n N_c} \quad (11)$$

Taking for the estimate the point in Figs. 8a and 9, where $f = 400$ Hz and $T_{\max} = 384$ K, the value of electron thermal velocity in $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ at 384 K $v_n = 2.6 \times 10^7$ cm/s, and density of state in the conduction band $N_c = 2.3 \times 10^{18}$ cm⁻³, we find the electron capture section $\sigma_n \approx (10^{-12} - 10^{-13})$ cm². This estimate for the capture cross-section looks quite reasonable.

Fig. 11 shows the $\ln S_{\max}$ versus $\ln f$ dependencies plotted for several samples of MOSHFETs and HFETs (see Figs. 8a and 8b). It is seen that in all cases, the slope is equal to unity.

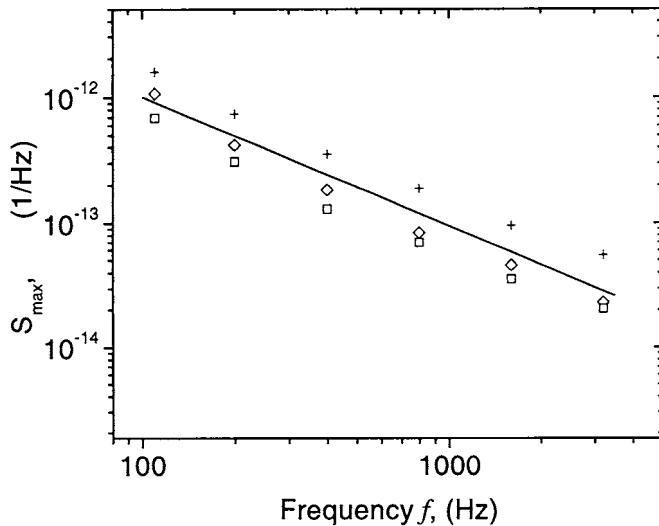


Fig. 11 The dependencies of S_{\max} versus f plotted for several samples conventional HFETs and MOSHFETs (see Fig. 8). The slope of the line is equal to unity.⁴ (© 2001, IEEE)

Such dependencies usually indicate that the noise temperature dependence is primarily determined by the temperature dependence of τ .^{35,46} Then, the trap concentration N_t can be crudely estimated as follows. Assuming that the main contribution to noise comes from the level with occupancy close to 0.5, we find for the trap concentration from Eq. (4)

$$N_t = \frac{4\pi f_{\max} S_{\max} n_s^2 L_0 W}{d} \quad (12)$$

Taking $S_{\max} = -125$ dB/Hz, at $f=400$ Hz, we obtain $N_t \approx 5 \times 10^{16}$ cm⁻³.

If we assume that the level under consideration is located at the surface of AlGaN layer, Eq. (12) reduces to Eq. (3), and sheet trap concentration N_{sAlGaN} is found to be $N_{sAlGaN} \approx 1.5 \times 10^{11}$ cm⁻². This value is two orders of magnitude smaller than what was estimated above for AlGaN thin films. This difference might be related to the difference between the free surface of AlGaN and the AlGaN surface covered by the metal gate.

6. Generation-Recombination Noise in GaN-Based Photodetectors

The low frequency noise in GaN-based photodetectors has been studied in several publications.⁴⁷⁻⁵⁰ Measurements of the noise properties of reverse biased GaN *p-n* junction photodetectors, Schottky barrier GaN, and AlGaN photodiodes (with Al mole fraction of 25%) have been reported. In these papers, the noise properties of the GaN-based Schottky diodes have been studied under the reverse bias. The noise properties of forward biased Schottky diode that can provide very important information on the location and nature of noise sources was reported in References⁵¹⁻⁵³.

The device epilayer structures were grown on sapphire substrate. The 200 Å thick AlN buffer layer was followed by the n⁺-Al_{0.4}Ga_{0.6}N layer. The n⁺-Al_{0.4}Ga_{0.6}N layer was co-doped using disilane (Si₂H₆) and trimethylindium (TMI). As confirmed by SIMS analysis, this co-doping procedure introduces a trace amount (about 0.5%) of In the active layer. From the capacitance-voltage (C-V) measurements, the carrier concentration of this n⁺ Al_{0.4}Ga_{0.6}N layer was found to be $n \approx 2 \times 10^{18} \text{ cm}^{-3}$. The n⁺-Al_{0.42}Ga_{0.58}N layer was capped with a 0.2 μm thick n⁺-Al_{0.4}Ga_{0.6}N active layer grown with the disilane flux reduced by a factor of 10. The C-V measurements showed a doping level of $N_d \approx 2 \times 10^{16} \text{ cm}^{-3}$ in this layer. Photodetectors demonstrated the peak responsivity in excess of 0.033 A/W at zero bias and cut-off wavelength of 275 nm.⁵⁴

The low-frequency noise of the forward biased Schottky diode was measured in the temperature interval from 300 K to 480 K.⁵⁵

Fig. 12 shows the temperature dependencies of noise S_I for different frequencies for the current density, $j = 10^3 \text{ A/cm}^2$. In the investigated frequency range, S_I versus T dependencies exhibited two weak maxima. The temperature of every maximum T_{max} , increases with a frequency increase, which indicates the existence of local levels. Since the measurements were performed at a small current density corresponding to the noise related to the Schottky barrier, we can conclude that the space charge region is the most probable location of the levels responsible for the GR noise.

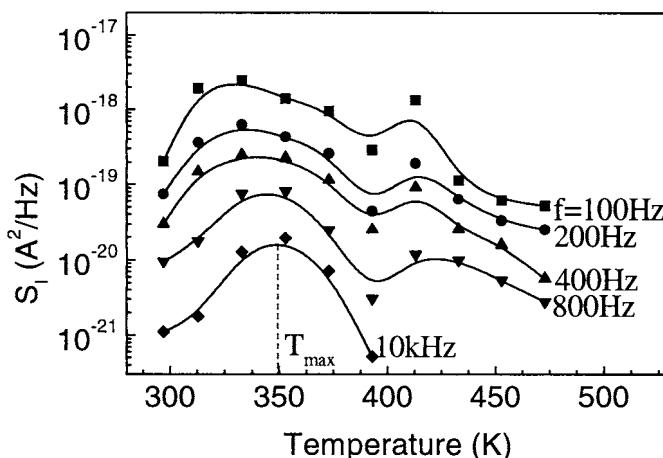


Fig. 12 The temperature dependencies of noise for Schottky barrier Al_{0.4}Ga_{0.6}N diode at different frequencies. Forward current density $j = 10^3$.⁵⁵

The maxima on S_I dependencies are relatively broad. However, for the low temperature maximum in Fig. 12, an estimate of the activation energy E_a of the local level contributing to noise is still possible. The Arrhenius plot (Fig. 13) yields the characteristic activation energy $E_a \approx 1 \text{ eV}$ for the low temperature maximum in Fig. 12. This value of the activation energy is close to those found in AlGaN thin layer (see Fig. 2) and AlGaN/GaN heterostructure field effect transistors (see Fig. 9.)

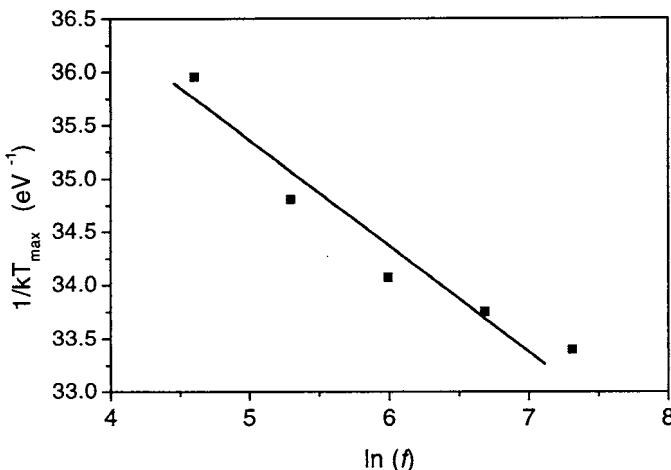


Fig. 13 The Arrhenius plot for Schottky barrier low frequency noise. Slope gives the activation energy $E_a \approx 1$ eV.⁵⁵

7. Conclusion

We reviewed the studies of the generation-recombination (GR) noise in GaN and AlGaN thin films, GaN based Metal Semiconductor Field Effect Transistors (MESFETs), Heterostructure Field Effect Transistors (HFETs), and Schottky diode photodetectors. Fig. 14 presents the summary of all local levels extracted from noise measurements for different AlN/GaN/InN based films and structures.

Thin GaN films with the thickness of 60 nm and the MESFETs exhibited very weak GR noise that did not allow us to extract the parameters of the local levels that might be responsible for the GR noise in these structures. AlGaN thin films yielded the GR noise with activation energy of 1 eV. Analysis showed that the source of the observed GR noise might be a local level at the AlGaN surface. Measurements on AlGaN HFETs, MOSHFETs and Schottky barrier Al_{0.4}Ga_{0.6}N diodes revealed the GR noise with the same activation energy of 0.8eV – 1.0 eV. Therefore, we concluded that AlGaN layer is the most probable source of the GR noise in AlGaN HFETs. Our estimates yielded a reasonable capture cross-section and concentration of traps located in AlGaN, which might be responsible for this noise. AlGaN/GaN HFETs also exhibited the GR noise with activation energies of 1 – 3 meV, 50meV, and 0.24 eV at cryogenic temperatures. GR noise with the activation energy of 1.6 eV was found in AlGaN/InGaN/GaN DHFETs. This is the largest reported activation energy for GaN based devices.

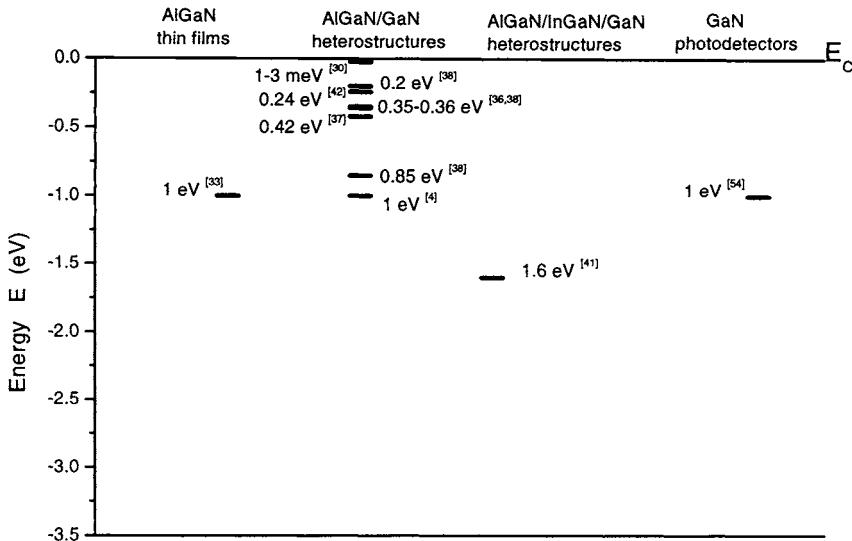


Fig. 14 Summary of the local levels extracted from the GR measurements for different AlN/GaN based films and structures.^{25,56}

Acknowledgment

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INSULATED GATE III-N HETEROSTRUCTURE FIELD-EFFECT TRANSISTORS

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Unique materials properties of GaN-based semiconductors that make them promising for high-power high-temperature applications are high electron mobility and saturation velocity, high sheet carrier concentration at heterojunction interfaces, high breakdown field, and low thermal impedance (when grown over SiC or bulk AlN substrates). The chemical inertness of nitrides is another key property. An AlGaN/GaN Heterostructure Field Effect Transistor (HFET) has been a topic of intensive investigations since the first report in 1991 [1]. Several groups demonstrated high power operation of AlGaN/GaN HFETs at microwave frequencies [2,3,4], including a 100 W output power single chip amplifier developed by Cree, Inc. and devices with 100 GHz cut-off frequency reported in [5]. However, in spite of impressive achievements, the potential of nitride based HFETs has not been fully realized as yet. The RF powers expected from the fundamental properties of nitride based materials significantly exceed the experimental data. One of the key problems limiting the HFETs RF characteristics is high gate leakage currents causing DC and RF parameter degradation. When the gate voltage goes positive the forward leakage current shunts the gate-channel capacitance and thus limits the maximum device current. When the gate voltage is negative, high voltage drop between the gate and the drain causes premature breakdown and thus limits maximum applied drain voltage. In addition, gate leakage currents increase the device sub-threshold currents, which decrease the achievable amplitude of the RF output. These limitations become even more severe at high ambient temperatures. The characteristics of III-N HFETs can be considerably improved by implementing a new approach, which results from the demonstration of good quality of $\text{SiO}_2/\text{AlGaN}$ and $\text{Si}_3\text{N}_4/\text{AlGaN}$ interfaces. This approach opens up a way to fabricate insulated gate heterostructure field-effect transistors (IGHFETs), which have the gate leakage currents several orders of magnitude below those of regular HFETs, and exhibit better linearity and higher channel saturation currents. In this chapter, we describe design, characterization and applications of these novel devices.

Keywords: Insulated gate FETs; III-N heterostructures; MOSHFET.

1. IGHFET types, fabrication and characteristics [6]

In the past, different insulating materials were proposed and studied for use as the gate insulator in the IGHFETs. Khan et al. and Binari et al. have reported on GaN-based Metal Insulator Field Effect Transistors (MISFETs) using i-GaN [7], i- AlGaN/GaN [8] and Si₃N₄ [9] as the gate insulator. These devices were operational but exhibited the current-voltage characteristic collapse at high drain biases related to a large density of interface states. Ren et al. have also reported on a GaN MOSFET using Ga₂O₃ and Gd₂O₃ oxides for the gate insulator.¹⁰ All these initial devices suffered from low transconductances and/or high threshold voltages due to large density of the interface states and poor control of the dielectric thickness. In the year 2000, novel AlGaN/GaN Metal-Oxide-Semiconductor Heterostructure Field Effect Transistors (MOSHFETs) on sapphire [11] and on SiC [12] substrates with excellent gate control were demonstrated. Later on it was also shown that high performance insulated gate HFETs can be made using Si₃N₄. These devices are referred to as MISHFETs below. Both device types operation is based on a high quality of the interface between deposited SiO₂ or Si₃N₄ layer and the AlGaN barrier layer. Since the MOSHFETs and MISHFETs have a lot in common we will first discuss the main properties of IGHFETs using MOSHFET as an example and then consider the difference between MOSHFETs and MISHFETs.

1.1. SiO₂-based IGHFETs - MOSHFETs

The MOSHFET design combines the advantages of the MOS structure, which suppresses the gate leakage current, and an AlGaN/GaN heterointerface that provides high density, high mobility two-dimensional (2D) electron gas channel. The MOSHFET approach also allows for application of high positive gate voltages to further increase the sheet electron density in the 2D channel and, therefore the peak device current. The MOSHFET built-in channel is formed by the high-density 2D electron gas at the AlGaN/GaN interface as in regular AlGaN/GaN HFETs. However, in contrast to a regular HFET, the gate metal is isolated from AlGaN barrier layer by a thin SiO₂ film (see Figure 1 (a)). Thus, the MOSHFET gate behaves more like a MOS gate structure rather than a Schottky barrier gate used in regular HFETs. Since the properly designed AlGaN barrier layer is fully depleted by electron transfer to the adjacent GaN layer, the gate insulator in the MOSHFET consists of two sequential layers: the SiO₂ film and the AlGaN epilayer. This double layer ensures an extremely low gate leakage current and allows for a large negative to positive gate voltage swing. Due to the wide band gap and to the full depletion of the AlGaN barrier neither electron nor hole parasitic channel forms at the SiO₂-AlGaN interface at the gate voltages up to +10 V.

The device epilayer structures were grown by low-pressure Metal Organic Chemical Vapor Deposition (MOCVD) on insulating 4H-SiC substrates. The AlGaN/GaN layers for this structure were deposited at 1000 °C and 76 Torr. A 50 nm AlN buffer layer was first grown at 1000 °C, followed by the deposition of a 1.5 μm insulating GaN layer. The heterostructure was capped with a 30 nm Al_{0.2}Ga_{0.8}N barrier layer, which was unintentionally doped. We also had a low-level flux of trimethylindium (TMI) present during the growth of all the layers of the structure. We had a low-level flux of trimethylindium (TMI) present during the growth of all the layers of the structure. Also, small concentration of carbon was present in all our grown layers. The presence of the indium surfactant and of trace amounts of indium helps in improving the surface and

interface roughness. As shown in [13], the surface roughness decreases from 7 nm RMS to 2.5 nm RMS with incorporation of In. The beneficial role of carbon was explained in [14]. We found the combination of indium and carbon in all our layers to be especially beneficial for both improving the materials quality and for obtaining better ohmic contacts. The measured room temperature Hall mobility and sheet carrier concentration were $1200 \text{ cm}^2/\text{V}\cdot\text{s}$ and $1.2 \times 10^{13} \text{ cm}^{-2}$, respectively.

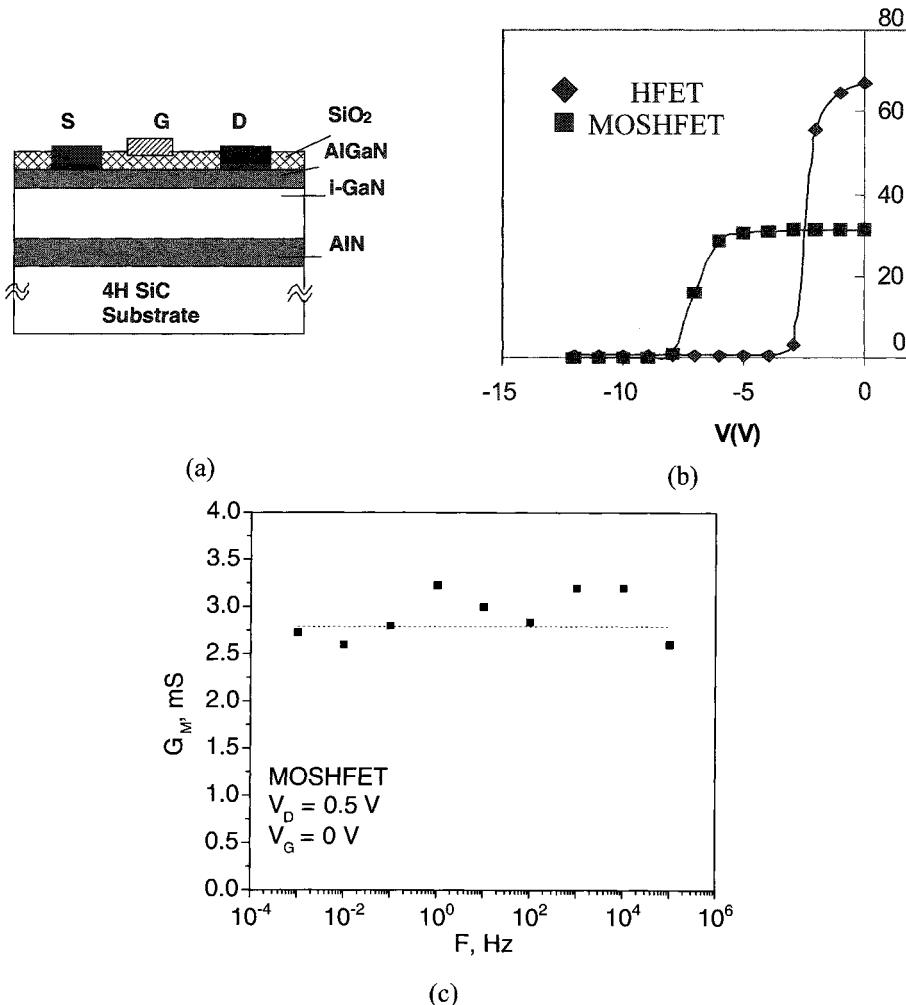


Figure 1. Schematic MOSHFET layout (a), capacitance – voltage characteristics of MOSHFET and HFET test structures (b) and small – signal transconductance dispersion of MOSHFET (c) [6] © IEEE 2003

These devices were fabricated using Ti(200 Å)/Al(500 Å)/Ti(200 Å)/Au(1500 Å) for the source-drain ohmic contacts. These were annealed at 850 °C for 1 min. in nitrogen ambient. A Reactive Ion Etching (RIE) was used for device isolation. Prior to the gate fabrication, a 10 nm SiO₂ layer was deposited on part of the heterostructure using plasma enhanced chemical vapor deposition. The thickness of this layer, d_{ox} , was extracted from

the capacitance-voltage (C-V) measurement at 1 MHz on the regions with and without the SiO₂ layer. In Figure 3(b) we include the C-V plots for 100 μm x 200 μm pads over the HFET and MOS-HFET regions. From the zero volt capacitance of these metal-semiconductor structures (without SiO₂ layer), and using AlGaN layer permittivity ε_B = 8.8, we estimate the AlGaN barrier thickness d_B to be 23 nm. This is very close to the 25 nm value estimated from the deposition rate.

The oxide thickness d_{ox} can be extracted from the measured pad capacitances:

$$C_{MOS} = \frac{\epsilon_0 \epsilon_B}{d_B} \times \left(1 + \frac{d_{ox}}{d_B} \cdot \frac{\epsilon_B}{\epsilon_{ox}} \right)^{-1} = C_{MS} \times \left(1 + \frac{d_{ox}}{d_B} \cdot \frac{\epsilon_B}{\epsilon_{ox}} \right)^{-1} \quad (1)$$

Here C_{MOS} and C_{MS} are the capacitances of equal area pads on the oxide and non-oxide areas and ε_{ox} = 3.9 is the SiO₂ dielectric permittivity. Using the data of Figure 3 and Eq. (1), the SiO₂ thickness, d_{ox}, was estimated to be 11 nm. This value is in reasonable agreement with the d_{ox} value of 10 nm expected from the deposition rate. Due to a larger gate-to-channel separation, the threshold voltage of the MOSHFET is larger than that of HFET. Assuming the same sheet charge density in the channel for MOSHFET and HFET devices at zero gate bias and ignoring the surface charge at the SiO₂/AlGaN interface, the threshold voltages for the MOSHFET and HFET can be related as:

$$Q_s = q N_s = C_{MOS} \times V_{TMOS} = C_{MS} \times V_{TMS}; \quad (2)$$

or

$$V_{TMOS} = V_{TMS} C_{MS} / C_{MOS} = V_{TMS} \times \left(1 + \frac{d_{ox}}{d_B} \cdot \frac{\epsilon_B}{\epsilon_{ox}} \right); \quad (3)$$

For the MOSHFET data of Figure 3 the threshold voltage increases 2.1 times compared to the HFET. The threshold voltages of the MOSHFET (~7.5 V) and HFET (~3.5 V) extracted from the C-V characteristics of Figure 3 are in good agreement with the above estimate. The deviation of the measured data from the estimate given by Eq. (3) is related to the interface charge. Since this deviation is small, the surface charge density at the SiO₂/AlGaN interface must be sufficiently low compared to qN_s at zero gate bias. To further prove the absence of significant surface trapping, we have measured the frequency dependence of the small-signal transconductance in the linear regime at low drain voltage and zero gate bias. Zero gate bias was chosen to eliminate the effects related to the current collapse (see below in this paper). The measurements were done on a number of MOSHFETs from different wafers. For comparison we have also measured HFET devices fabricated on the same wafers. No difference between HFET and MOSHFET behavior was observed. Figure 3 (c) shows typical frequency dependence of small-signal transconductance for MOSHFET device. As seen the MOSHFET does not exhibit any noticeable dispersion. The predicted and measured increase in the threshold voltage is not detrimental for high-power high-voltage nitride based devices. The MOSHFET transconductance is about 50 % lower compared to HFET due to larger gate – channel separation. However, the linearity of the transconductance – gate voltage dependence for the MOSHFET is much better compared to that for the HFET. Therefore, as shown below in this paper, the MOSHFET has lower nonlinear distortions in high power microwave and switching applications.

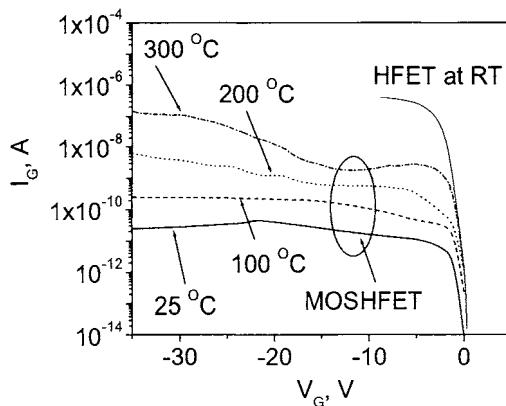


Figure 2. Gate leakage currents for the MOSHFET at different temperatures and the base-line HFET at room temperature measured in diode mode (drain disconnected).) [6] © IEEE 2003

The suppression of the gate leakage current is one of the most important features of the MOSHFET. In Fig. 2, we show the gate leakage current for the $1.5\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$ gate MOSHFET at different temperatures. The data shows that the MOSHFET leakage current is as low as 200 pA at -20 V gate bias at room temperature and is approximately six orders of magnitude smaller than for the regular HFET with similar gate dimensions which is presented for the reference in the inset of Figure 2. Even at $+300\text{ }^{\circ}\text{C}$ the gate leakage current for MOSHFET remains 3 to 4 orders of magnitude lower than for regular HFETs. The pinch-off characteristics of AlGaN/GaN MOSHFET were also measured in the temperature range $25\text{ }^{\circ}\text{C}$ - $300\text{ }^{\circ}\text{C}$. The pinch-off current as low as 0.15 nA/mm at room temperature and $38\text{ }\mu\text{A/mm}$ at $250\text{ }^{\circ}\text{C}$ was measured at the gate voltage $V_g = -15\text{ V}$ and the drain bias of 10 V. Figure 3 shows the measured current-voltage (I-V) characteristics of AlGaN/GaN MOSHFET with a source - drain separation of 5 μm and the gate length of 1.5 μm at elevated temperatures at the gate bias $V_G = +3\text{ V}$. As seen, the device saturation current is close to 1 A/mm. This current decrease with the temperature follows the temperature dependence of the electron saturation velocity [15].

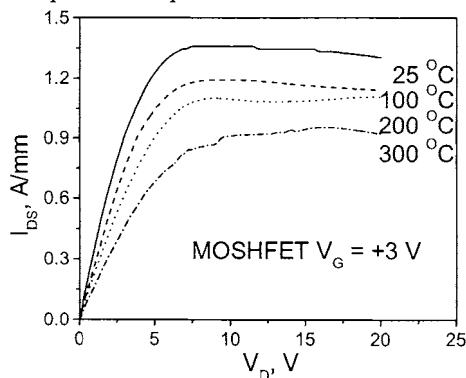


Figure 3. I-V characteristics of MOSHFET with the source – drain opening of 5- μm and gate length of 1.5 μm .) [6] © IEEE 2003

The maximum DC saturation drain current I_{DSM} at positive gate voltages is a key parameter controlling maximum output RF-power. For conventional AlGaN/GaN HFETs, gate voltages in excess of + 1.2 V result in excessive leakage current, which limits I_{DSM} . In a MOSHFET, the gate voltages as high as +10V could be applied. This results in approximately 100% increase in the I_{DS} value with respect to the zero gate bias value. The gate leakage, however, remains well below 1 nA/mm. Figure 4 shows the transfer characteristics for the 1 μ m gate MOSHFET and HFET measured at the drain voltage sufficient to shift the operating point into saturation regime. Figure 4 also shows the gate bias dependence of the HFET and MOSHFET current in the saturation regime (for the MOSHFET the gate current remains in the low nanoampere range). As seen, the gate voltage corresponding to the maximum of I_{DS} in the HFETs also corresponds to a sharp increase of the gate leakage current. This indicates that the mechanism responsible for the I_{DS} saturation at high gate bias is the gate leakage current. This explains why the measured values of I_{DSM} for the HFETs at high gate bias are substantially smaller than those predicted by the approximation based on the 2D electron channel capacity [16]. In the MOSHFETs, where the gate leakage is suppressed, the 2D electrons spillover into the AlGaN barrier becomes a limiting mechanism. According to the model developed in [17], this electron spillover occurs at the source edge of the gate at a certain value of the gate voltage, V_{GM} , that depends on the geometry of the 2D channel and on the Fermi level position. A larger gate-channel separation in MOSHFET also contributes to a higher value of V_{GM} for MOSHFETs. Due to these factors, both the MOSHFET saturation gate voltage and the saturation current for the MOSHFETs are higher than those for the HFETs. Assuming that the maximum sheet carrier density in the 2DEG channel (limited by the 2D density of states), n_s , is about $2 \times 10^{13} \text{ cm}^{-2}$ [18] and the effective electron drift velocity in the channel, $v = 5 \times 10^6 \text{ cm/s}$, we estimate the maximum achievable channel current $I_{DSM}/W = q \times n_s \times v \approx 1.6 \text{ A/mm}$. The measured saturation current in our MOSHFET is close to this maximum value.

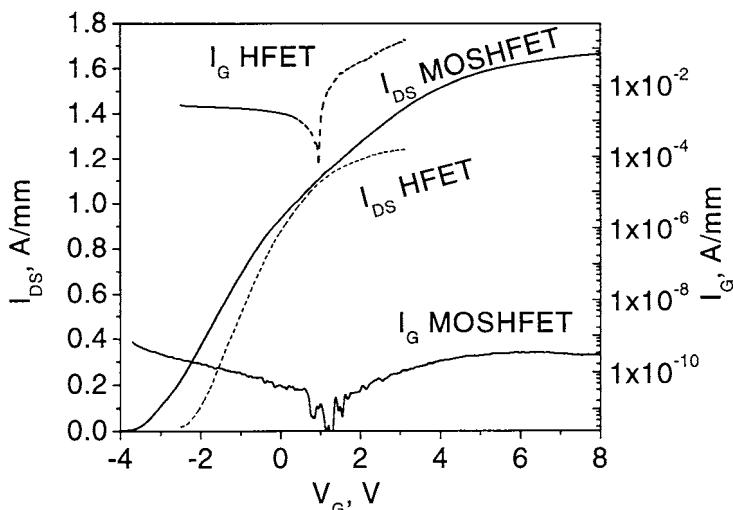


Figure 4. Maximum saturation and gate leakage currents in 1.5 μ m gate MOSHFET and HFET devices. [6] © IEEE 2003

1.2. Si_3N_4 based IGHFETs - MISHFETs

The SiO_2 material is not the only choice for making insulating gate III-N devices. In past, the MOSFETs using $\text{Ga}_2\text{O}_3/\text{Gd}_2\text{O}_3$ as the gate insulator [19] were reported. However, the charge control in this structure was fairly poor and the transconductance achieved was not high enough for practical applications. The use of Si_3N_4 for insulating gate III-N devices was first proposed in [20]. Several groups have recently shown that Si_3N_4 passivation in the source-gate and gate-drain region improves the device performance and reduces the transconductance dispersion [21, 22]. These results suggest that high quality of insulator/barrier interface can be also achieved using Si_3N_4 material. We have fabricated insulating gate transistors using Si_3N_4 [23]. We called these devices MISHFETs. A device fabrication procedure was similar to that reported earlier for the MOSHFETs. Two sets of devices with identical geometry (gate length 1 μm , source-drain opening 5 μm , and gate width 100 μm) were fabricated on the same wafer. They consisted of MOSHFETs (100 Å SiO_2 under the gate and in the source-gate and drain-gate regions) and MISHFETs (100 Å Si_3N_4 insulator replacing SiO_2). Both the SiO_2 and the Si_3N_4 layers were deposited using plasma enhanced chemical vapor deposition (PECVD). In Figure 5, we include the transfer curves and the gate-leakage current curves for the MOSHFETs and MISHFETs. As seen, the maximum saturation currents in both MOSHFET and MISHFET are close. Either oxide or the nitride insulator layers reduce the gate leakage by 6 to 5 orders correspondingly below that measured for the typical HFET devices. The gate leakage current of the MISHFET is higher than of the MOSHFET, probably due to a lower quality of the thin Si_3N_4 layer. However, the increase in the threshold voltage for the MISHFET device is not as large. This follows directly from a higher value of the dielectric constant of the Si_3N_4 layer ($\epsilon_r = 3.9$ for SiO_2 and $\epsilon_r = 7.5$ for Si_3N_4).

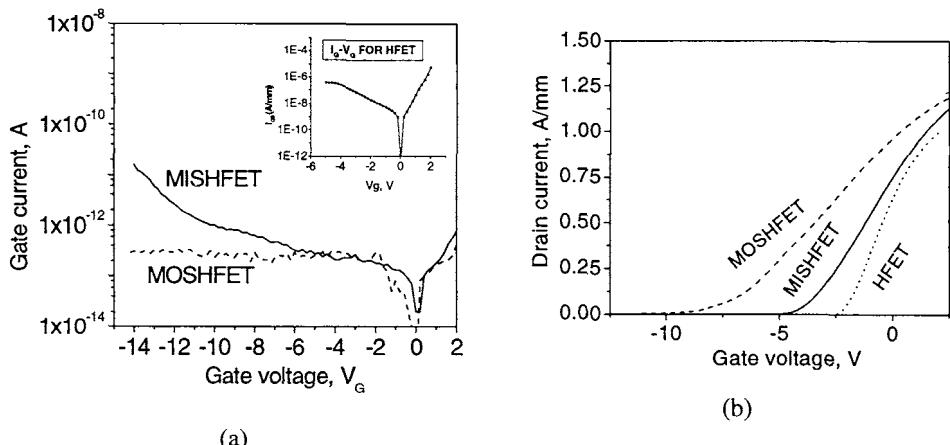


Figure 5. Gate leakage current (a) and transfer characteristics (b) comparison for the MOSHFET and MISHFET fabricated on the same wafer (after [15]). The inset shows the gate leakage current for a regular HFET. [6] © IEEE 2003

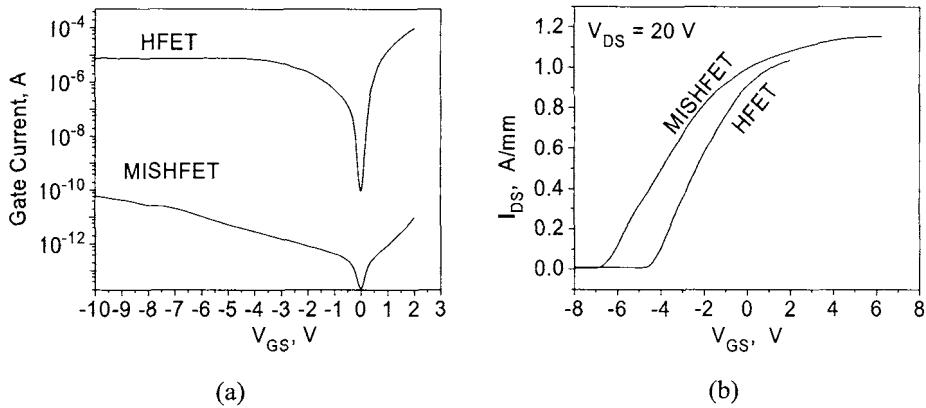


Figure 6. Gate leakage currents and transfer characteristics of MISHFET and HFET with $0.25\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$ gates [24] ©IEEE 2003

1.3 Submicron Gate IGHFETs

High-frequency applications require the HFET devices with submicron gate length. Scaling the gate length down to the submicron range is not only the technological challenge but also an important physical problem as it describes the IGHFET operation in the deep velocity saturation regime. In this section we describe the experimental study of the $0.25\text{ }\mu\text{m}$ gate MISHFETs [24], however, general conclusions are as well applicable to the MOSHFET devices.

The device epilayer structures for submicron MISHFETs were grown by low-pressure Metal Organic Chemical Vapor Deposition (MOCVD) on insulating 4H-SiC substrates. The AlGaN/GaN layers for this structure were deposited at $1000\text{ }^\circ\text{C}$ and 76 Torr. A 50 nm AlN buffer layer was first grown at $1000\text{ }^\circ\text{C}$, followed by the deposition of a $1.5\text{ }\mu\text{m}$ insulating GaN layer. The heterostructure was capped with a 25 nm undoped $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ barrier layer, which was unintentionally doped. We also had a low-level flux of trimethylindium (TMI) present during the growth of all the layers of the structure to improve the surface and interface roughness by incorporation of trace amounts of indium. The measured room temperature Hall mobility and sheet carrier concentration were $1200\text{ cm}^2/\text{V}\cdot\text{s}$ and $1.2 \times 10^{13}\text{ cm}^{-2}$, respectively. The HFETs and MISHFETs were fabricated on the same wafer using $\text{Ti}(200\text{\AA})/\text{Al}(500\text{\AA})/\text{Ti}(200\text{\AA})/\text{Au}(1500\text{\AA})$ for the source-drain ohmic contacts. These were annealed at $850\text{ }^\circ\text{C}$ for 1 min. in nitrogen ambient. A Reactive Ion Etched (RIE) mesa was used for device isolation. The source-drain spacing was $3\text{ }\mu\text{m}$. For the MISHFETs, prior to gate formation, an 8 nm thick layer of Si_3N_4 was deposited using plasma enhanced chemical vapor deposition (PECVD). Submicron gates were then formed using e-beam lithography with a bilayer polymethyl-methacrylate/polydimethyl-glutarimide resist followed by $\text{Ni}(500\text{\AA})/\text{Au}(500\text{\AA})$ metal layer deposition and lift-off process. The gate length $L_G = 0.25 \pm 0.02\text{ }\mu\text{m}$ was measured using JEOL 5900LV scanning electron microscope.

Figure 6 (a, b) show the gate leakage currents and transfer characteristics of the identical geometry MISHFETs and HFETs with the gate width of $100\text{ }\mu\text{m}$. As seen, the MISHFET gate leakage is 5 orders of magnitude lower than that of HFET at -10 V gate bias. The threshold voltage of MISHFET is -7 V as compared to -4.5 V of the HFET. This

increase of 1.55 times, due to large gate-channel separation, is in excellent agreement with the zero gate bias capacitance ratio of 1.6 measured on the same devices. This implies that no significant interface charge exists at the insulator - semiconductor interface. Maximum transconductance $g_m = 0.15 \text{ S/mm}$ (at - 4.5V gate bias) and 0.24 S/mm (at -3.4V) for the MISHFET and the HFET also correspond to a transconductance ratio of 1.6, as expected from the threshold voltage and the capacitance ratios.

Small-signal microwave performance was characterized on wafer using HP 8510 vector network analyzer and Cascade probe station with Ground-Signal-Ground RF probes. To extract the intrinsic cut-off frequency value the parasitic capacitance of the probe pads was first extracted by measuring the C_{GS} as a function of device width and taking the intercept corresponding to zero width. The source - gate capacitance, C_{GS} was found from the small-signal $\{y\}$ parameters as $C_{GS} = \text{Im}(y_{11}+y_{12})/\omega$ (see e.g. [25]). This expression is valid in the frequency range where $\omega^2 C_{GS}^2 R_S \ll 1$, which corresponds to $f < 25 \text{ GHz}$ for the MISHFET under study. These data yielded the intrinsic cut-off frequency for the MISHFET, $f_T \approx 63 \text{ GHz}$. The same value was extracted for the HFET. Therefore, despite of a larger gate - channel separation, the fringe effects are negligible in the MISHFETs with 0.25 μm long gates. The average electron velocity in the channel, v_s , can be found from the intrinsic f_T value as $v_s = 2\pi f_T L_G$. This yields $v_s \approx 9.9 \times 10^6 \text{ cm/s}$ both for the HFET and MISHFET. This shows that the deposition of Si_3N_4 layer does not result in any degradation of high quality AlGaN/GaN heterointerface.

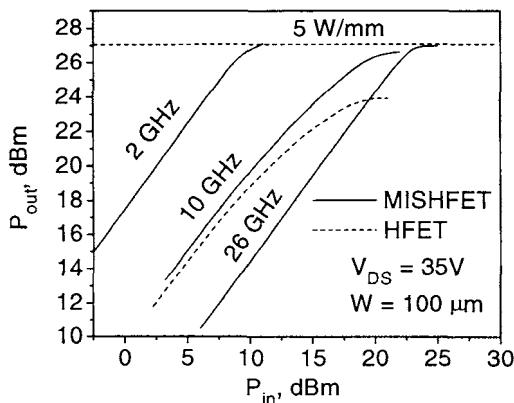


Figure 7. Output - input RF power dependencies for MISHFET at 2GHz, 10GHz and 26GHz. For comparison the dependency for the HFET at 10GHz is also shown [24]. ©IEEE 2003

On-wafer high-power RF testing was performed using Maury and Focus Microwave automated Tuner Systems (at 2-10 GHz and 26 GHz respectively) and Cascade RF probe stations. All the measurements were taken in CW mode without cooling the wafer or using any other thermal management. Figure 7 shows the RF output- input power dependencies for MISHFET at 2 GHz, 10 GHz and 26 GHz. For comparison, we also show the dependence for the HFET measured at 10 GHz. As seen, the maximum CW output RF power for the MISHFET of 5 W/mm (at 35 V drain bias) practically does not change with operating frequency implying no significant parameter dispersion in the device. This power level is about 3 dB higher than that of the HFET. Our data show that

in the HFET the RF power saturates when the input signal level causes significant rise of the forward gate current. In the MISHFET this limitation is absent and, therefore, the maximum output power is considerably higher. At 40 V drain bias the maximum output CW power of 6 W/mm was obtained for the MISHFET at 26 GHz. An important observation is that the RF power gain of the MISHFET is very close to that of the HFET. The voltage gain, $g_m \times R_L$, of the MISHFET is lower compared to the HFET due to a lower transconductance. However, the current gain under impedance matching conditions is *inversely proportional* to the device input capacitance C_{GS} , which is lower for the MISHFET. As stated above, the ratio of (g_m/C_{GS}) is nearly the same for MISHFET and HFET, and, therefore, the power gain is nearly the same too.

Another important parameter affecting the achievable RF power and power added efficiency (PAE) is the knee voltage - the drain voltage at which the device current saturates. For high power devices, the knee voltage at zero gate bias is of most importance as it affects the maximum output RF power. One might expect MISHFETs to have higher knee voltages as a result of a higher threshold voltage. Whereas this is true for long gate devices, in the submicron gate transistors the knee voltage is mainly affected by the velocity saturation and the voltage drop across the source-gate and gate-drain openings. Assuming these mechanisms to be responsible for the I-V characteristics saturation, the knee voltage, V_{KN} as a function of the channel saturation current, I_S can be found as follows: $V_{KN} = E_S \cdot L_G + I_S (R_S + R_D)$, where E_S is the characteristic field for the electron velocity saturation, R_S and R_D the source-side and the drain-side resistances correspondingly. In Figure 8 we show the knee voltage- saturation current dependencies measured for the MISHFET and HFET under study. It is clearly seen that the dependencies are nearly linear and at the same saturation currents the knee voltages for the both device types are very close. The extrapolation of $V_{KN}(I_S)$ line down to zero currents gives an estimate for the knee voltage component associated with the velocity saturation. For both the HFET and MISHFET this value is below 1V. At very high currents, only achievable for the MISHFET at positive gate biases, the slope of the $V_{KN}(I_S)$ dependence slightly increases. This is due to the effective channel resistance increase at high currents due to self-heating effects and/or field-dependent electron mobility in the channel.

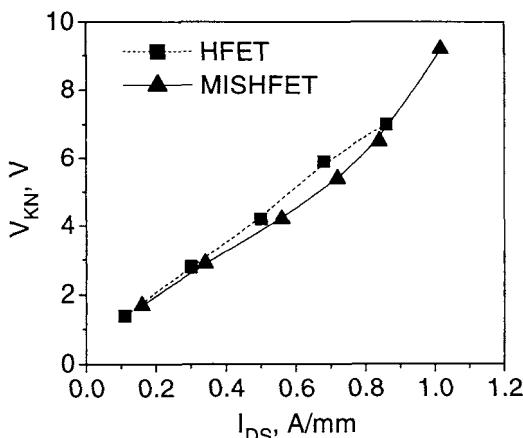


Figure 8. Knee voltage - saturation current dependencies for 0.25 μ m gate MISHFET and HFET [24]. ©IEEE 2003

These results show that the submicron gate MISHFET have all the key parameters defining the RF performance better or equal to those of regular III-N HFETs. The MISHFET gate leakage current is ~ 5 orders of magnitude lower, the maximum RF power is ~ 3 dB higher, the RF power gain, the cut-off frequency and the knee voltage are the same as compared to the HFET. Therefore, the MISHFET is a viable alternative to HFETs for high-power high-temperature RF applications.

2. RF-current collapse in IGHFETs

2.1. Pulsed return current technique

A so-called current collapse [26-29] and long-term stability are the most important problems preventing large-scale practical usage of nitride-based HFETs in ultra-high power microwave systems. The current collapse usually manifests itself as a reduction of the device current when a large RF signal is applied to the gate. This reduction is the main reason why the output power of AlGaN/GaN HFETs is considerably smaller than the value expected based on the steady-state I-V characteristics. For example, a typical AlGaN/GaN HFET with the maximum saturation current about $I_{DSM} \approx 1\text{A/mm}$ and the knee voltage $V_{KN} \approx 5\text{ V}$ at a moderate operating point of $V_D = 35\text{ V}$, should deliver an output power

$$P_{OUT} \approx I_0 \times (V_D - V_{KN})/2 \approx 7.5\text{ W/mm}, \quad (4)$$

where $I_0 \approx I_{DSM}/2$ is the operating DC current. However, for such a device, even under pulsed drain bias and pulsed RF drive conditions eliminating the device self-heating, the measured RF output power is typically about 2 to 4 W/mm (excluding some hero device results, which show the power close to this expected value or higher, usually for a short time).

The collapse phenomenon has been observed in almost all AlGaN/GaN HFETs and MOSHFETs. However, in spite of a large number of studies (see [27-32]), the physical mechanism of the effect has remained somewhat mysterious. In this chapter, we present the results of the experiments that allow us to identify the device regions responsible for the current collapse and compare the current collapse in different types of HFET devices. In order to compare the current collapse effects in MISHFET, MOSHFET and HFET devices, we measured their pulsed I-V characteristics (see Figure 9). For these measurements, the source-drain bias was fixed at a value well in the saturation regime. The gate voltage was then pulsed using 1 μsec pulses with a 50% duty cycle. The gate-voltage pulse amplitude varied from 0 V (channel open) to a value below the device threshold voltage. The "return" pulsed current, i.e. the pulsed current when the gate voltage pulse returns to zero (as shown in Figure 9, a) was measured. Since the three device types had different threshold voltages, we plotted in Figure 9 the gate voltage normalized to the threshold voltage and the pulse current normalized to the DC current at zero gate bias.

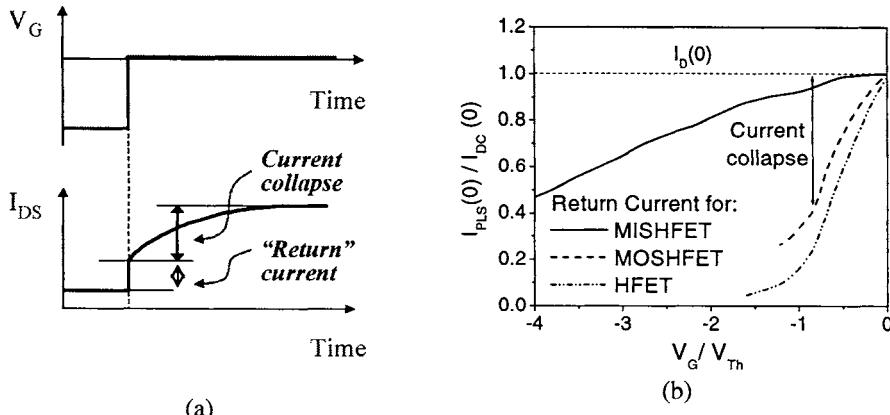


Figure 9. Pulsed return current technique (a) and pulsed transfer characteristics of MISHFET, MOSHFET and HFET (b) [6]. ©IEEE 2003

As seen, at a non-zero value of the gate bias pulse, the device current does not return to its DC value, I_{DC} , for the gate pulse voltage ($V_G = 0$). This is the manifestation of the current collapse. After a negative voltage is applied to the gate, it takes a certain time for the current to recover to its peak value when the gate voltage returns back to $V_G = 0$. Therefore, the difference between DC and pulsed values of drain currents at zero gate voltage (illustrated by the arrowhead line) is a direct measure of the RF-current collapse. As seen, this reduction in current is present for all measured devices. The presence of SiO_2 layer practically does not affect the current collapse. However the current collapse in Si_3N_4 MISHFET occurs at the gate voltage amplitude larger than those for MOSHFET and HFET devices, i.e. the MISHFETs exhibit lesser RF current collapse. Several mechanisms might be responsible for this difference. Surface charge modification at $\text{SiO}_2/\text{AlGaN}$ or $\text{Si}_3\text{N}_4/\text{AlGaN}$ interfaces may be different. It is also possible that the Si_3N_4 being extremely hard material reduces the deformation of the HFET cap/channel layer caused by strong electric field under the gate (this possible mechanism was proposed in [33]).

We used the Gated Transmission Line Model (GTLM) measurements [33, 34] on HFET and MOSHFET devices under pulsed gate bias conditions in order to isolate the changes of channel resistance under the gate and outside the gate during the transient. The gate lengths in sequential sections of the GTLM (Figure 10 (a)) varied from $L_G=10 \mu\text{m}$ to $L_G=100 \mu\text{m}$, whereas the gate - source and gate - drain openings were kept constant at $L_{GS}=L_{GD}=10 \mu\text{m}$. The width of all the sections was $W=200 \mu\text{m}$.

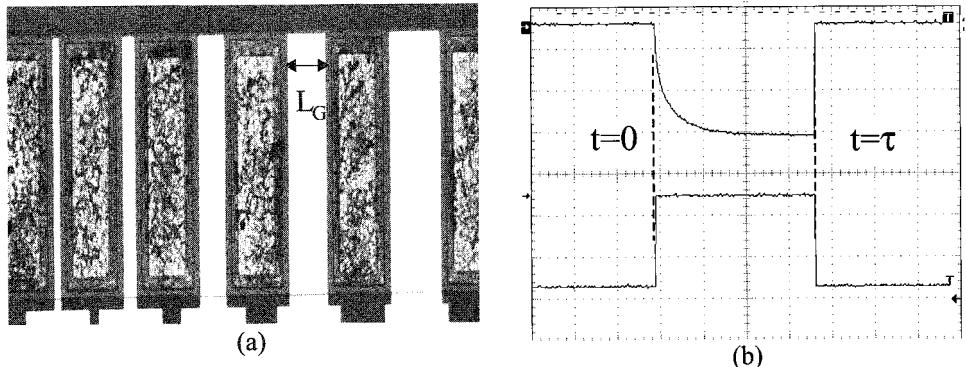
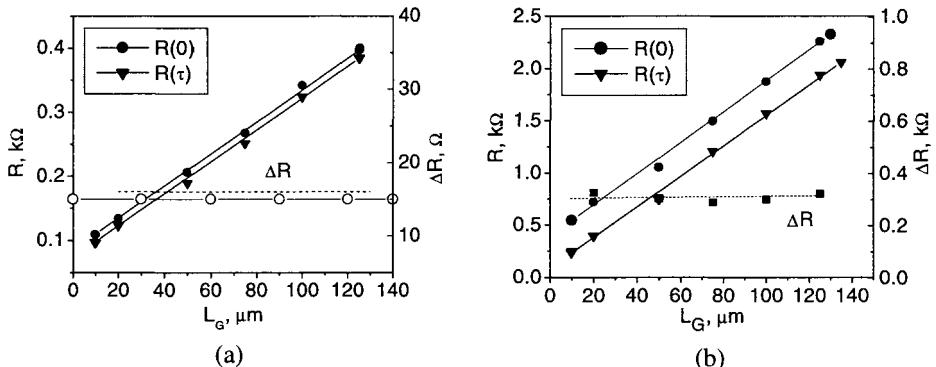


Figure 10. Gated TLM structure (a) and measured waveforms (b) [33]

Gate voltage pulses (typically 1 to 100 s long) were used to bias the devices from pinch-off to the zero gate bias conditions. The total resistances of the GTLM sections $R_T(0)$ and $R_T(\tau)$ were measured in the beginning of the transient process ($t=0$) and at the end of the gate pulse ($t=\tau$, when the current is close to its steady state value), respectively. The dependencies $R(L_G)$ in both linear mode (V_{DS} is less than the knee voltage) and saturation mode (high V_{DS}) are shown in the Figure 11(a, b) correspondingly. As seen, these dependencies are straight lines with the slopes being inversely proportional to the channel resistance *under the gate* with the intercept at $L_G = 0$ giving the total resistance *outside the gate*. Our measurements [33] showed that the current collapse under pulsed gate bias results from the edge effects at the source and/or drain sides of the gate. No difference between HFET and MOSHFET behavior was observed.

Figure 11. Dependencies $R(L_G)$ in both linear regime (a) and saturation regime (b) [33]

2.2. Dynamic I-V characteristics and RF current collapse model [35]

The pulsed return current and GTLM data provide important information regarding transient processes in the HFETs and IGHFETs in the presence of current collapse. However these data is not sufficient to describe quantitatively the reduction of RF powers neither do they allow explaining the nature of the current collapse. In this section, we present the experimental studies of the current collapse using the dynamic current-voltage

characteristics (DI-Vs) and propose the model of the current collapse based on the observed DI-Vs.

Our approach to measure the DI-Vs of the HFET devices is a further extension of the previously described pulsed return current method. The DI-Vs are measured when large AC signal is applied at the gate. The DC offset of the gate bias is chosen such that the minimal gate voltage is close to threshold, whereas the maximum voltage is around or slightly exceeds zero. The drain bias, V_b , is applied via the series load resistance, R_L (see the inset to Figure 12). To obtain the DI-Vs, we measure peak drain currents corresponding to the instant when the gate voltage reaches zero. The variable load resistances are used to trace the DI-Vs.

First, the transfer characteristics of AlGaN/GaN HFETs were measured at different frequencies in the range of 0.1-10⁶ Hz (Figure 12). In the frequency range of 0.1-100 Hz strong hysteresis was observed during the gate sweep and the maximum current decreased with frequency increase. At the frequencies above 1 kHz, the hysteresis disappeared and no further decrease in the maximum current was observed. The frequency of 1 MHz was chosen to measure the dynamic I_D - V_D dependencies.

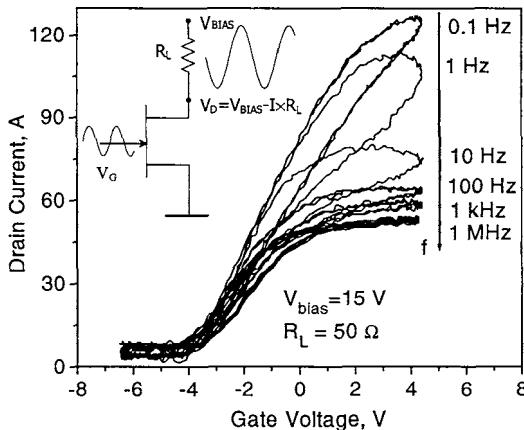


Figure 12. Transfer characteristics of AlGaN/GaN HFETs were measured at different frequencies in the range of 0.1-10⁶ Hz

The HFET DI-V characteristics differ drastically from the DC characteristics of the same device (see Figure 13(a)). As seen, the DI-Vs do not exhibit current saturation at high drain biases. Several HFETs tested up to 100 V drain bias showed this resistor-type behavior. The slope of the I-V curve (the equivalent resistance) increased with the drain bias. Hence, the DI-Vs demonstrated “the run-away” of the HFET knee voltage. The Figure 13 (b) shows the DI-Vs of the AlGaN/InGaN/GaN DHFET. This device discussed in the following section has significantly improved carrier confinement and as a result it does not exhibit any considerable current collapse. As seen, for this current collapse-free device, the DI-Vs practically coincide with the static I-V characteristics.

To establish the relevance of the DI-Vs to the device RF performance, we compared the measured RF output powers with those simulated using the DI-Vs for the same devices. For the HFETs, the load dependence of the output RF power $P_{RF}(R_L)$ can be estimated assuming the DI-Vs to be quasi-linear with the equivalent resistance of R_D (drain bias dependent):

$$P_{RF} \sim \frac{R_L}{(R_D + R_L)^2}, \quad (5)$$

This dependence has a maximum at $R_D \approx R_L$. In contrast, for the DHFETs in saturation regime, $R_D \gg R_L$ and $P_{RF} \sim R_L$ as long as the voltage drop across the device remains larger than the knee voltage: $V_{bias} - I \times R_L > V_{Knee}$.

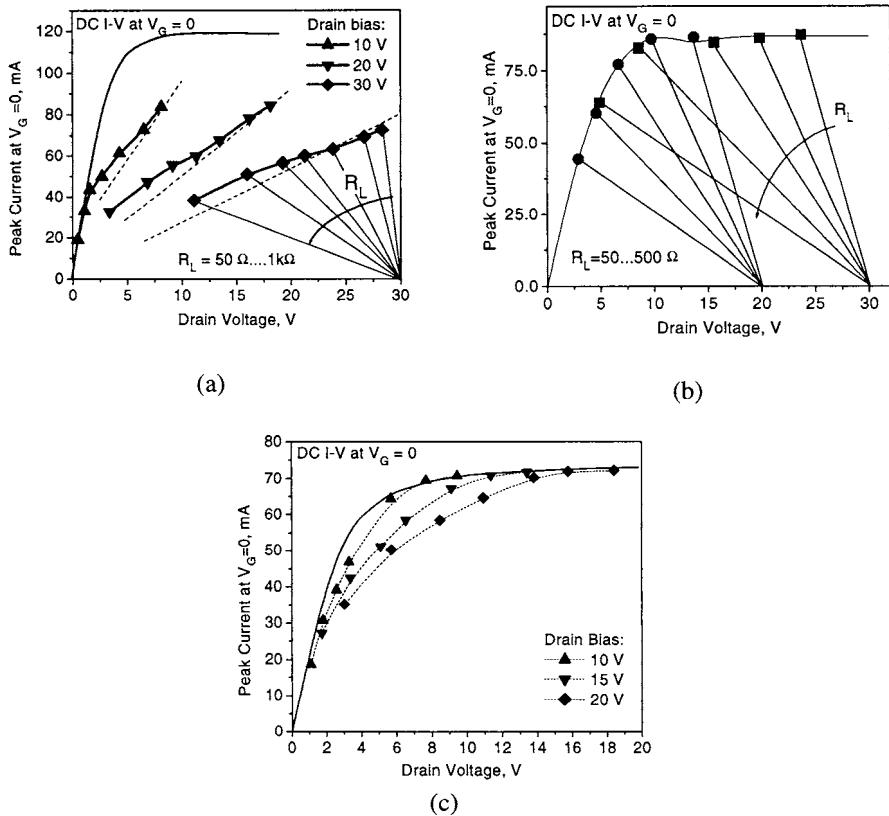


Figure 13. HFET DI-V characteristics [35]. © IEEE 2003

Figure 14 shows the normalized experimental load dependencies of the HFET and DHFET CW output powers measured at 2 GHz at 25 V drain bias. The load impedance was tuned using Maury calibrated automated tuner system. Also shown is the load impedance dependence simulated using the DI-Vs for the same devices. As seen, the simulated curves accurately describe the experimental dependencies. However, for the HFETs, the load impedance dependence of the output power is quite weak exhibiting the change in the RF power by only 2.5 dB in the wide range of the load impedance 100...800 Ω. The RF power peaks at $R_L \sim 170 \Omega$, which corresponds closely to the maximum of $P_{RF}(R_L)$ dependence at $R_D \approx R_L \approx 170 \Omega$ given by Eq. (5). For the DHFET, the output RF power increases with the load impedance up to $R_L \approx 420 \Omega$. This value of

R_L corresponds closely to the slope of the load line that intercepts the $I_D(V_D)$ curve at the knee voltage of the DHFET.

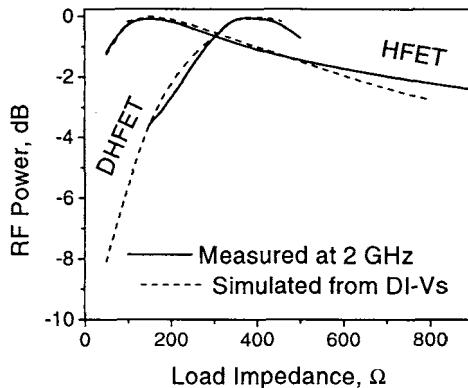


Figure 14. Normalized experimental load dependencies of the HFET and DHFET CW output powers measured at 2 GHz at 25 V drain bias[35]. © IEEE 2003

We propose the following physical model considering space-charge limited current at the gate edges to explain the observed DI-Vs and RF performance of the HFETs. As seen from the transfer characteristics of the Figure 12, the HFET threshold voltage does not change as the gate signal frequency increases. Therefore, the decrease in the current is not associated with the sheet carrier density reduction under the gate. This is consistent with our recent Gated-Transmission-Line-Model (GTLM) experiments showing that the channel resistance outside the gate not under the gate increases during the transient process. When the gate voltage goes negative, the charge can be trapped in the buffer layers due to electron spillover. The trapped charge may accumulate consequently during multiple cycles until the equilibrium is reached. This effect is more important when the gate voltage is close or below the threshold, as in this case the 2D gas does not screen the applied field. When the gate voltage returns to zero, the trapped charge remains nearly the same as at the threshold. The above effect is much more pronounced at the edges of the gate. The regions at the gate edges differ from the region under the gate in several ways. First, the transition from the metal covered part of the channel to the ungated region results in additional gate voltage dependent strain. Second, the electric field is very large at the gate edges and significantly changes with the gate and drain bias in both longitudinal and transverse directions. Third, the drain bias directly affects the charge trapping at the drain side of the gate. The large electric field at the gate edges leads to a band banding. This allows the Fermi level to cross the trap level responsible for the collapse in some region near the gate edge resulting in a very effective trapping. If the minimal gate voltage is above or close to threshold the depletion region appears mainly at the drain edge. However, if minimal gate voltage goes below threshold (when operating in class B mode) the depletion can also occur on the source side. In general, the surface trapping may also affect the appearance of the depletion regions by changing the surface potential distribution. The HFET and DHFET used in our experiments mainly differ by carrier confinement [37] and, therefore, surface effects were not dominant.

Under strong current collapse conditions, narrow highly-resistive depletion regions appear at the gate edges. The current through these regions can be described by the

space-charge limited current (SLC) model. (This current mechanism was previously found to be important in submicron GaAs HFETs [36].) At high drain bias, the electron velocity in the depletion region is saturated and SLC can be described by the following equation [36]:

$$I = \frac{2\epsilon_o \epsilon v_s \Delta V}{L_D^2} W t, \quad (6)$$

where v_s is the electron saturation velocity, L_D is effective length of the depletion region, ΔV is the voltage drop across the depletion region at the minimum value of the gate bias, W is the gate width, and t is the thickness of the region supporting this current. The length L_D of the depletion region at the gate edge is determined by the drain voltage *when the gate voltage reaches its minimum value*:

$$V_B + V_{PO} = \frac{qN_T L_D^2}{2\epsilon_o \epsilon}, \quad (7)$$

where N_T is concentration of the trapped charges in the buffer layer. The surface concentration of the trapped charges is given by $N_{TS} = N_T \times t$. This trapped charge is a fraction of the 2D electron sheet charge, N_s , at zero gate bias: $N_{TS} = \alpha N_s$, where α is dimensionless parameter characterizing the degree of the carrier spilling-over and trapping (the trapping confinement factor). From the Eq. (6 -7), we obtain the resistance associated with the SLC region:

$$\Delta R_s = \frac{V_B + V_{PO}}{\alpha q N_s v_s W} = \frac{V_B + V_{PO}}{\alpha I_s}, \quad (8)$$

where I_s is the HFET saturation current in the velocity saturation regime. Eq. (4) shows that under strong current collapse condition, the intrinsic transistor does not reach the saturation even at high drain biases, since ΔR_s is large and increases with V_B so that nearly all drain bias drops across ΔR_s . For the HFET used in our experiments, the value $\alpha \approx 0.63$ fits the dynamic I-Vs obtained at all the bias voltages in the range of 10 V to 30 V (see the dashed lines in the Figure 13(a)).

According to our proposed mechanism, trapping at the gate edges results in additional bias dependent series resistances. Even though this semi-quantitative model applies to a very strong current collapse, the qualitative conclusions are also valid for an intermediate case of a smaller degree of depletion at the gate edges when the saturation can be reached. At large bias voltages, the series resistance at the drain edge of the gate dominates. Therefore, a relatively weak current collapse primarily manifests itself in the increased bias-dependent knee voltage. This type of DI-Vs was observed in the DHFET with very low In composition as shown in the Figure 13 (c). The increase of the knee voltage under RF drive was also reported by S. Binari et. al. (see e.g. [1]). The proposed model therefore describes all important experimental data related to the RF current collapse in III-N FETs.

3. Double Heterostructure Field-Effect Transistors (DHFETs) and Insulated gate DHFETs (IGDHFETs).

The MOSHFET and HFET devices fabricated from the same wafer exhibit nearly the same degree of current collapse. In other words, SiO_2 layer incorporation under the gate does not affect the mechanism responsible for the current collapse in AlGaN/GaN

HFETs. The presence of Si_3N_4 layer does not eliminate the current collapse completely as well. Recently we proposed and demonstrated a double heterostructure field-effect transistor (DHFET) where the 2D electron gas (2DEG) channel is confined within a thin InGaN layer sandwiched between GaN buffer and AlGaN barrier [37]. The insertion of the InGaN layer forms a quantum well with the depth and shape being determined by AlGaN/InGaN and GaN/InGaN bandgap offsets and interface polarization charges. This quantum well significantly improves the confinement of the channel electrons for all applied drain and gate bias voltages. The electron spatial distributions in a regular HFET and DHFET structures are shown in Figure 15.

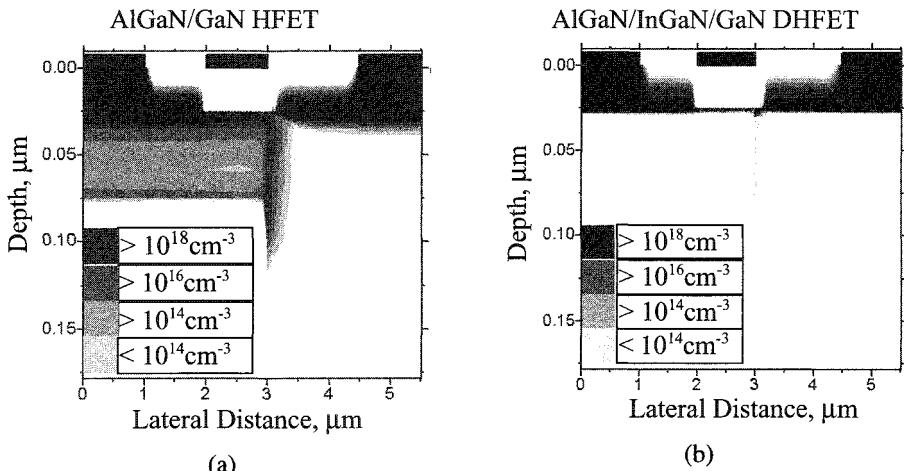


Figure 15. Electron spatial distributions in a regular HFET and DHFET structures [6] © IEEE 2003

A significantly reduced electron spillover is clearly seen in DHFET as compared to HFET structure. This should significantly reduce the total charge that can be trapped outside the channel. This practically eliminates the current collapse. This was confirmed by pulsed measurements similar to those discussed above for the MOSHFET, MISHFET and HFET. These data for DHFET and MOSDHFET are shown in Figure 16. As seen, the pulse return current for these devices is nearly independent on the gate amplitude and is very close to the DC current at zero gate bias.

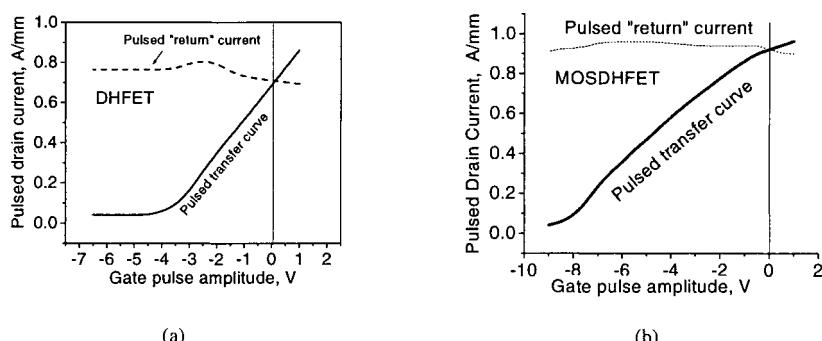


Figure 16. Pulsed measurements data for DHFET and MOSDHFET [38] © IEEE 2002

We also fabricated a novel structure combining the advantages of the SiO₂ gate insulation (MOSHFET) and the InGaN channel double heterostructure DHFET design [39]. The resulting metal-oxide semiconductor double heterostructure FET (MOSDHFET) devices are current collapse free and exhibit gate leakage currents about 4-6 orders of magnitude lower than the regular Schottky gate HFETs (depending on the thickness and quality of the oxide layer). As described in Section 1, the epilayers for the MOSDHFET were grown on insulating SiC substrates using conventional low-pressure metal organic chemical vapor deposition (LP-MOCVD). The growth temperatures for the GaN buffer, InGaN channel and the AlGaN barrier layers were 1000 °C, 760 °C and 1100 °C respectively. The InGaN were doped *n*-type with their bulk electron concentration of approximately $2 \times 10^{17} \text{ cm}^{-3}$. The presence of In in the InGaN layer was confirmed by SIMS profiling. The room temperature Hall mobility and the sheet carrier concentration for the deposited DHFET structure were measured to be $730 \text{ cm}^2/\text{V}\cdot\text{s}$ and $1.1 \times 10^{13} \text{ cm}^{-3}$, respectively. The MOSDHFET device fabrication procedure is similar to that used earlier for the MOSHFETs. Devices with a 5 μm source-drain opening and a 1 μm gate length were fabricated. Several DHFET devices were also fabricated on the same wafer by protecting the source-drain opening during SiO₂ deposition. As reported earlier for the MOSHFET devices, the threshold voltage of MOSDHFETs is larger than that for the HFETs. The DHFET and MOSDHFET threshold voltages ($V_T \approx -4.8 \text{ V}$ and $V_T \approx -10 \text{ V}$, respectively) calculated using Eqs. (2) and (3) correspond closely to our experimental data. The gate leakage current for the MOSDHFET device was below 10 pA for gate voltages $V_G = 0 \dots -15 \text{ V}$. In the DHFET, the gate leakage current for the same gate voltage range increased up to 10 μA. Therefore as we could see for the MOSHFET devices before, the introducing of thin SiO₂ layer decreases the gate leakage current of DHFET by about 4-6 orders of magnitude. The pulse MOSDHFET characteristics show the return current that is very close to the DC value at zero gate bias, therefore, not exhibiting any current collapse. As shown below, the MOSDHFET devices also demonstrate stable current collapse free behavior under intense RF drive conditions.

4. Multi-gate large periphery MOSHFETs and MOSDHFETs

In this section, we describe large periphery multi-gate (MG) MOSHFET and MOSDHFET devices, fabricated on SiC substrates, using oxide bridging for source interconnects [40]. These high power devices demonstrate a nearly linear dependence of saturation current, transconductance, microwave gain and saturation power on the total device width in the range from 0.15 to 4 mm. The MG device geometry consists of an interlaced source-gate-drain electrode structure. The source-to-source connections go over the gate electrodes with an oxide layer in between used for isolation. This MG MOSDHFET design is shown in Figure 17. Unlike for a single section dual gate MOSDHFET processing, we use PECVD to deposit 0.3 μm thick SiO₂ isolation "islands" at the gate - source intersections for the MG device. Ti(200)/Au(6000) metal electrodes are then deposited to form low resistance section interconnects and device contact pads. A relatively low dielectric permittivity of the SiO₂ islands allows for the bridging with a small parasitic capacitance. For the 5 μm × 5 μm source - gate overlap area and 0.3 μm thick islands, the bridge capacitance is only 0.003 pF. This is about 100 times lower than the gate capacitance of MOSHFET or MOSDHFET device with 1 × 150 μm gate dimensions (around 0.25 pF).

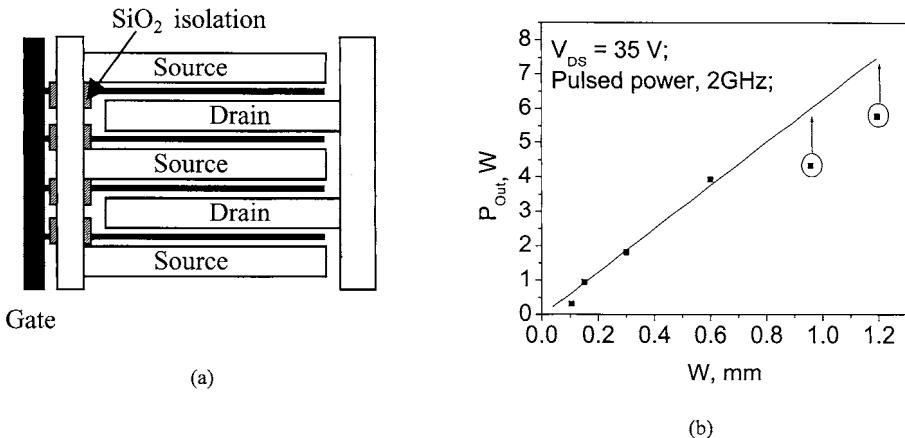


Figure 17. MG MOSDHFET design [6] © IEEE 2003

The current-voltage characteristics of a single section for the MOSDHFET ($150 \mu\text{m}$ gate width) showed the saturation current to be 0.6 A/mm at zero gate bias. It increased to 0.86 A/mm at the positive gate bias of $V_g = +3 \text{ V}$. The threshold voltage was about -9.5 V . The pulsed I-Vs show nearly linear scaling with the gate periphery for both device types. However the DC peak current for both device types saturates when the device periphery exceeds 1.5 mm . The DC current saturation with the increase of the device periphery is due to device self-heating. In pulsed I-V measurements, we achieved the saturation currents as high as 5 A for a 6 mm wide device [40].

5. Large-Signal RF Linearity of IGHFETs [41]

In Field-Effect-Transistor (FET) amplifiers, three major effects contribute to the nonlinearity [42, 43]: the modulation of input capacitance C_{GS} by the gate voltage, the transconductance-gate voltage dependence, $g_m(V_{GS})$, and the modulation of the output impedance at high input signals. As shown in [42-45], the contribution from the input capacitance nonlinearity is usually small compared to other sources of nonlinearity. This is particularly true for the HFETs where the gate capacitance above threshold is nearly independent on the gate bias. As we will show in this section, the more flattened $g_m(V_{GS})$ is the major factor responsible for a significantly better linearity of IGHFETs. Since the current collapse may result in significant RF distortion, for this comparative study we selected current collapse-free MOSDHFET and DHFET devices.

Figure 18(a) shows the measured DC I-V transfer characteristics of MOSDHFET and DHFET of the same device geometry ($100 \mu\text{m}$ total gate width) at the drain voltage in saturation region ($V_{\text{DS}} = 24 \text{ V}$). In the Figure 18 (b), we show the DC transconductance for the MOSDHFET and DHFET with the characteristics shown in Figure 18 (a). As seen, the MOSDHFET has significantly more linear current-gate voltage dependence (a more constant transconductance). As we will show below in this paper, this improvement in $g_m(V_{GS})$ flatness is the major factor responsible for low RF distortions.

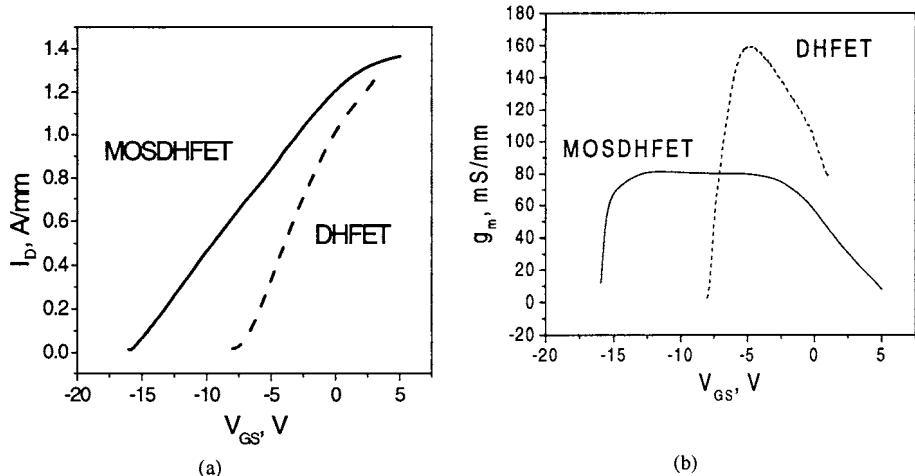


Figure 18. DC I-V characteristics (a) and transconductance (b) of the MOSDHFET and DHFET devices used for RF linearity study [41]. © IEEE 2003

The output RF power dependences on the delivered RF input power P_{out} (P_{del}) are shown in Figure 19. These data were obtained using an optimal source/load-pull tunings at 2 GHz. In spite of lower g_m , the power gain of the MOSDHFET is very close to that of the DHFET under optimum input impedance matching. The reason is a higher input impedance of the MOSDHFET that increases the gain.

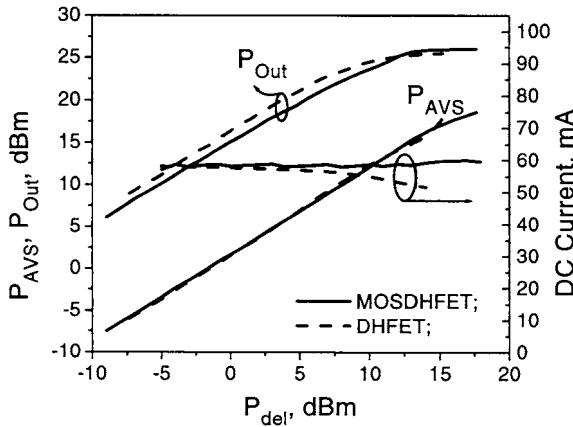


Figure 19. Measured RF powers available at source, delivered powers and output powers in the MOSDHFET and DHFET. Also shown are the input RF voltage dependencies of the DC currents [41]. © IEEE 2003

The input capacitance of MOSDHFET is lower compared to that of DHFET so that g_m/C_{GS} ratio (where C_{GS} is the input capacitance) is nearly the same for both device types. Therefore, for the same delivered RF power the input voltage amplitude ($V_{GS} \sim 1/C_{GS}$, see below in this paper) is larger for MOSDHFET under impedance matching conditions. The maximum saturation CW RF powers at 2 GHz and at 28 V drain bias and $V_{GS} = -7.5$

V and -3V were 4.1 and 3.5 W/mm for MOSDHFET and DHFET, respectively. The increased MOSDHFET RF output power is attributed to a larger gate voltage swing and to an increase in the device maximum drain current [16]. As also shown in Figure 19, the DC operating currents do not decrease with an increase in the input power, P_{del} , which indicates the absence of the RF collapse. In Figure 19, we also include the plot of input Power Available at Source (P_{AVS}) versus P_{del} . Linear P_{AVS} (P_{del}) dependence in both MOSDHFET and DHFET device types implies the absence of the modulation of the input impedance. Therefore, the modulation of the input capacitance modulation does not contribute noticeably into nonlinearities.

To study the output RF signal nonlinearities, the system output tuner was set to 50Ω . This was done to eliminate the frequency dependence of the load impedance. Under such conditions, the ratio of the output signal powers in the higher harmonics over the fundamental harmonics is independent on the load impedance and can be found as

$$\frac{P_2}{P_1} = \frac{i_2^2 \cdot \text{Re}\{Z_2\}}{i_1^2 \cdot \text{Re}\{Z_1\}} = \frac{i_2^2}{i_1^2}, \text{ where the } i_2 \text{ and } i_1 \text{ are the amplitudes of the 2}^{\text{nd}} \text{ and the}$$

fundamental rf current harmonics correspondingly, Z_2 and Z_1 are the load impedances at the frequencies of 1st and 2nd currents harmonics correspondingly. The dependencies for the third order distortions are similar. Figure 20 shows the experimental and simulated dependencies of the P_2/P_1 and P_3/P_1 on the input RF voltage amplitude for both the MOSDHFET and the DHFET devices. The amplitude of the RF input voltage, v_{RF} , was calculated from the measured RF input powers, accounting for the effective source signal amplitude, v_S at the input impedance matching condition $P_{\text{AVS}} = \frac{v_S^2}{8R_S}$. From this

$$\text{equation, } v_{\text{RF}} = \frac{v_S}{2R_S} \cdot \frac{1}{2\pi f C_{GS}} = \frac{1}{\pi f C_{GS}} \cdot \sqrt{\frac{P_{\text{AVS}}}{2R_S}}. \text{ Here } f \text{ is the fundamental signal}$$

frequency, R_S is the real part of device input impedance. Values for R_S and C_{GS} were determined from the measured large signal input impedance of MOSDHFET and DHFET ($39+j132 \Omega$ and $39+j67 \Omega$) while the P_{AVS} values were directly measured with a power meter. As seen from Figure 20, the MOSDHFETs have very low levels of the third and second harmonic outputs, which are below -30 dB even at large input signals. These levels are 15 - 20 dB lower than those for the DHFET.

To clarify the factors responsible for the nonlinear distortions, we simulated the

$$\frac{\delta g_m}{\delta V_{GS}} (V_{GS}) \text{ dependencies for the MOSDHFET and DHFET using the Charge Control}$$

Model [46]. According to this model, the saturation current – gate voltage dependence is given by:

$$I_{ds} = 2C_{GS} \frac{\mu}{L_G} W V_{GT} \left(1 + \sqrt{1 + \left(\frac{\mu V_{GT}}{v_s L_G} \right)^2} \right)^{-1} \quad (1)$$

Here, μ is the low-field carriers mobility, v_s is the electron saturation velocity, L_G is device gate length, W is the device width, $V_{GT} = V_{GS} - V_T$, where V_{GS} and V_T are the gate

and the threshold voltages. For simplicity in the Eq. (1), we are neglecting the source parasitic resistance. Differentiating Eq. (1) twice, we find,

$$\frac{\partial g_m}{\partial V_{GT}} = -2C_{GS}v_s \left(2 + \frac{1}{\sqrt{1+u^2}} \right) \cdot \left(1 + u^2 + \sqrt{1+u^2} \right)^2 \quad (2)$$

Here, $u = \frac{\mu V_{GT}}{v_s L_G}$ is the dimensionless gate voltage swing. It can be readily seen from Eq.

(2), that the $\frac{\partial g_m}{\partial V_{GT}}$ decreases with u , and the values of u are larger for the MOSDHFET

at the same value of I_{ds} . This enhanced stability yields smaller distortions in MOSDHFETs. Simulations were performed for a 50Ω load impedance by weighting a 2 GHz input signal with the devices transfer characteristics of Figure 18(a) and using FFT technique. These results are plotted by solid lines for the MOSDHFET and DHFET in Figure 20. Based on good agreement between the measured and the simulated P_2/P_1 , P_3/P_1 ratios in a wide range of input signal amplitudes (the difference does not exceed 1.5 dB), we conclude that the major mechanism responsible for the large-signal distortions in III-N HFETs is the transconductance gate-voltage dependence. Figure 3 also shows the relative levels of the higher harmonic powers at the load impedances corresponding to the maximum output powers. As seen, the slope of the (P_2/P_1) and (P_3/P_1) vs. V_{RF} dependencies increases slightly at high input signals as compared to 50Ω loads. This increase might be due to the contribution of the output impedance nonlinearity, which is only pronounced at very large input powers.

At relatively low input signal amplitudes the levels of the 2nd and 3rd harmonic power for MOSDHFET are as low as -40... -45 dB. This feature of MOSDHFET is very important for practical applications where the level of the high order harmonic powers is critical. These include wireless communication systems, broadband amplifiers, etc. It also simplifies significantly large signal impedance matching in high power amplifiers.

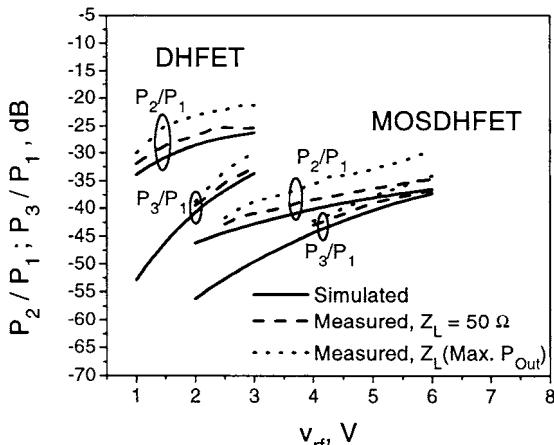


Figure 20. Measured and simulated 2nd and 3rd harmonics to fundamental power ratios for the MOSDHFET and DHFET [41]. © IEEE 2003

6. Microwave and switching characteristics of MG Insulated gate devices

RF testing of MG MOSDHFETs was carried out using an HP 8510C network analyzer for small-signal cutoff-frequency measurements and a Maury Automated Tuner system for large signal power measurements. The cutoff frequency f_c of 9.5 GHz was measured for 0.5 mm wide device with 1 μm gate length at -5 V gate bias. The source- and load- pull high power measurements were performed at the drain bias of 35 V. This yields the effective saturation velocity

$$v_s = 2\pi L f_c = 0.6 \cdot 10^7 \text{ cm/s}$$

in good agreement with the value extracted from the maximum drain saturation current. The pulse length of 1 μs with the 1% duty cycle was used for these power measurements. Similar to the DC parameters, the RF pulse output powers also scale almost linearly with the device periphery. The output power for the optimally tuned MOSDHFETs is close to 6.3 W/mm. The measured power level was somewhat lower for the narrow device ($W \approx 50 \mu\text{m}$) due to difficulties with tuning to very high input and output impedances. For the largest devices, $W \geq 1 \text{ mm}$, the available input RF signal was not large enough to saturate the MOSDHFET. Hence, only the power at 3 db compression was measured and then extrapolated to the saturation level.

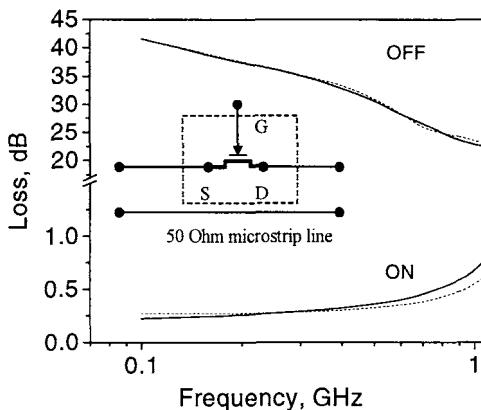


Figure 21. Performance of RF MOSHFET switch [47] ©IEEE 2002

The MOSDHFET devices demonstrated a very stable behavior under continuous RF drive. In the course of a 16 hours test at 25 V drain bias, the RF power degraded by about 0.5-0.6 W/mm in the first 2 - 3 hours of operation and then stabilized. This stabilization was irreversible, i.e. when the test was repeated the initial RF output power was close to its stable value and did not change with time. We believe that this stable MOSDHFET behavior is due to extremely low gate leakage currents and a perfect confinement of the 2DEG in the InGaN channel, which avoids trapping and long-term relaxation effects.

We have also demonstrated an efficient microwave switch based on a multi-gate AlGaN/GaN MOSHFET [47]. Record high saturation current and breakdown voltage,

extremely low gate leakage current and low gate capacitance of the MOSHFETs described before make them excellent active elements for RF switching.

A simplest single element test RF switching circuit is shown in the inset to Figure 21. In the open state, the MOSHFET switch can be described as a series resistance R connected to the microstrip line with the characteristic impedance Z_0 . For $Z_0=50$ Ohm and $R \ll Z_0$, the insertion loss can be estimated as

$$L_{\text{ins}} (\text{dB}) = 10 \log \frac{1}{1 + R / 2Z_0} \approx 0.087 R_{\text{SQ}} \times L / W, \quad (9)$$

where R_{SQ} is the sheet resistance of the 2D channel in the source-drain opening of the length L and the width W . For a typical MOSHFET with the 5 μm source-drain opening, $R_{\text{SQ}} \approx 300 - 400$ Ohm at zero gate bias. Since the MOSHFET allows for a high positive gate bias, this resistance can be further decreased by about a factor of 2. The shunting effect of the gate-source and gate-drain capacitances is insignificant in MOSHFETs due to a larger gate - channel separation and lower gate capacitance. It follows from Eq. (9) that the insertion loss of 0.1 - 0.25 dB can be easily achieved in the ON state for a 1 mm wide device. For the OFF state, the gate voltage biases the device into the pinch-off state. In this state the isolation is mainly determined by the source - drain capacitance, assuming that gate is RF-grounded. Using a 1 mm wide MOSHFET with 1 μm long gate, we have achieved 0.25 dB insertion loss and more than 40 dB isolation at 100 MHz (see Figure 21). The frequency dependence of the insertion loss is mainly due to the series inductance of the bonding wires as seen from the simulated curve (dashed curve in Figure 21). The isolation decreases down to 22 dB at 1GHz due to the drain - source capacitance of 0.01 pF/mm found for the planar device geometry. The maximum MOSHFET switching power in the ON state is limited by the maximum saturation current I_{DSM} and

the drain knee voltage, V_{KN} : $P_{\text{inn}} = \frac{V_{\text{KN}} \cdot I_{\text{DSM}}}{2} \frac{1}{1 - K_p}$, where $K_p = P_{\text{Out}}/P_{\text{In}}$ is the

power transfer ratio of the switch. As shown above, both these parameters are higher for the MOSHFETs compared to the HFETs. Using $I_{\text{DSM}} \approx 1.6$ A/mm and $V_{\text{KN}} \approx 5$ V and $K_p \approx 0.95$ (corresponding to 0.2 dB insertion loss), the maximum switching power of the MOSHFET based switch can be estimated as $P_{\text{inn}} = 80$ W/mm. This power level is about 80 times higher than that reported for a GaAs based switch [48]. These results show a high potential of MOSHFET devices for microwave switching. As we have shown before [49], the MOSHFETs can be also used as extremely high power DC switching devices. The breakdown voltage as high as 500 V was measured for the MOSHFET devices with the 10 μm gate-to-drain opening. With the maximum current of MOSHFET of about 5 A (demonstrated for the 6 mm wide device, see above) the maximum switching power was 7.5 kW/mm². For these estimations, we used the total device area including a 100 μm separation between the adjacent gate sections. If only the active source-drain region area is used for this estimate, the switched power density estimate increases to 50 kW/mm².

Conclusions

The insulating gate III-N devices demonstrate a much superior performance compared to regular AlGaN/GaN HFETs. The gate leakage current for these devices is 4 to 6 orders of magnitude lower; the maximum saturation currents might be twice as high. The combination of the MOS- design with a double heterostructure transistor design, the

DHFET, results in a low gate leakage current collapse free MOSDHFET device. Due to a larger threshold voltage and gate voltage swing, the MOSHFETs and MOSDHFETs have a lower level of RF nonlinear distortions. They can be also used as extremely efficient microwave and power switches.

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High Voltage AlGaN/GaN Heterojunction Transistors

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The use of AlGaN/GaN HEMTs and HBTs for switching power supplies is explored. With its high electron velocities and breakdown fields, GaN has great potential for power switching. The field-plate HEMT increased breakdown voltages by 20% to 570V by reducing the peak field at the drain-side edge of the gate. The use of a gate insulator is also investigated, using both JVD SiO₂ and e-beam evaporated SiO₂ to reduce gate leakage, increasing breakdown voltages to 1050V and 1300V respectively. The power device figure of merit (FOM) for these devices: $V_{BR}^2/R_{on} = 9.94 \times 10^8 [V^2 \cdot \Omega^{-1} \text{cm}^{-2}]$, is the highest reported for switching devices. To reduce trapping effects, reactively sputtered SiN_x is used as a passivant, resulting in a switching time of less than 30 ns for devices blocking over 110V with a drain current of 1.4A under resistive load conditions. Dynamic load results are also presented.

The development of HBTs for switching applications included the development of an etched emitter HBT with a selectively regrown extrinsic base. This was later improved upon with the selectively regrown emitter devices with current gains as high as 15. To improve breakdown in these devices, thick GaN layers were grown, reducing threading dislocation densities in the active layers. A further improvement included the use of a bevelled shallow etch and a lateral collector design to maximize device breakdown.

Keywords: AlGaN; GaN; high voltage transistors.

1. Introduction

The size and weight of switched power supply systems is often dependent on the switching speed of the component power switch transistors, while the efficiency is limited by the on-state resistance, off-state power dissipation and steady-state gain of these devices. For low voltage systems, high performance can be achieved using conventional silicon technology. For high voltage, high power switch systems however, silicon devices are currently limited in switching speed. With the advent of electronic aircraft, electric and hybrid vehicles, and a variety of other applications, a significant demand has emerged for switching devices operating at voltages in the 600V range switching at MHz frequencies. Figure 1 indicates applications where GaN may enable higher switching speeds than conventional technologies.

Table 1 compares various figures of merit (FOM) applicable to devices engineered for high voltage switching. The relatively high FOM for GaN results from the high critical electric field $E_c \sim 2 \times 10^6$ [V/cm], and high electron velocities: $v_{sat} \sim 2 \times 10^7$ cm/s. $\mu \sim 1500$ [cm²(V · s)⁻¹].

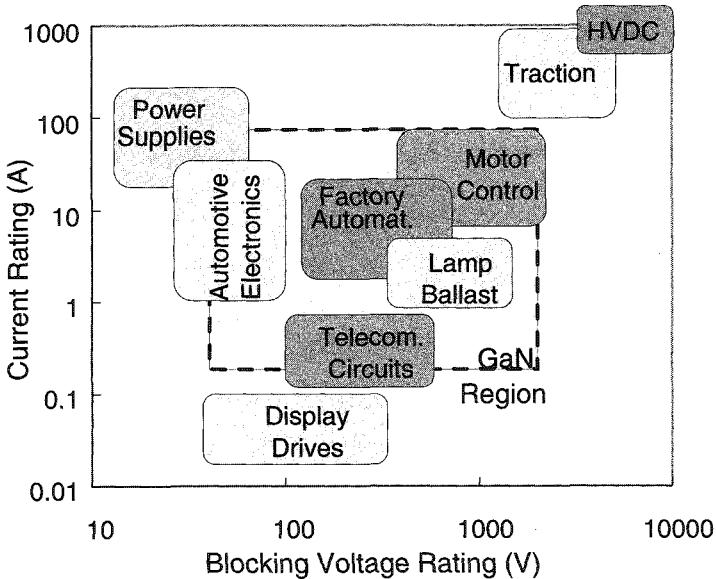


Fig. 1. Map of switching applications

| Figure of Merit | Material | | | | |
|---|----------|--------|------|-------|---------|
| | Si | 4H-SiC | GaN | AlN | Diamond |
| BM [$\epsilon_n \mu E_c^3$] | 1 | 130 | 650 | 31700 | 4110 |
| BHM [μE_c^2] | 1 | 22.9 | 77.8 | 1100 | 470 |
| JM [$E_c v_{sat}/2\pi$] | 1 | 180 | 760 | 5120 | 2540 |
| KM [$\Theta_K(v_{sat}/\epsilon_r)^{1/2}$] | 1 | 4.61 | 1.6 | 21 | 32.1 |

Table 1. Values are normalized to Silicon

As mentioned, the reduction of on-resistance is critical for high efficiency operation, and in a comparison with devices in other material systems GaN shows excellent performance. (Figure 2). Two device types were developed for high power switching, the AlGaN/GaN HEMT and the AlGaN/GaN NPN HBT. The HEMT offers high power density, low drive currents, and a more mature technology which can be implemented in the short-term. The HBT is a normally off device and can in principle handle larger current densities than HEMTs. Presently, the low current gain in the HBT leads to high drive current requirements and coupled with high parasitic base resistance leads to reduced efficiency.

2. AlGaN/GaN HEMT for High Power Switching

The priorities in designing AlGaN/GaN HEMTs for switching applications include increasing the breakdown voltage, reducing on-resistance, and eliminating traps which can lead to increased switching times. Simulations for standard HEMT structures show a large peak in electric field at the drain-side edge of the gate electrode. This peak field leads to premature breakdown of the device and can be reduced using a field plate tech-

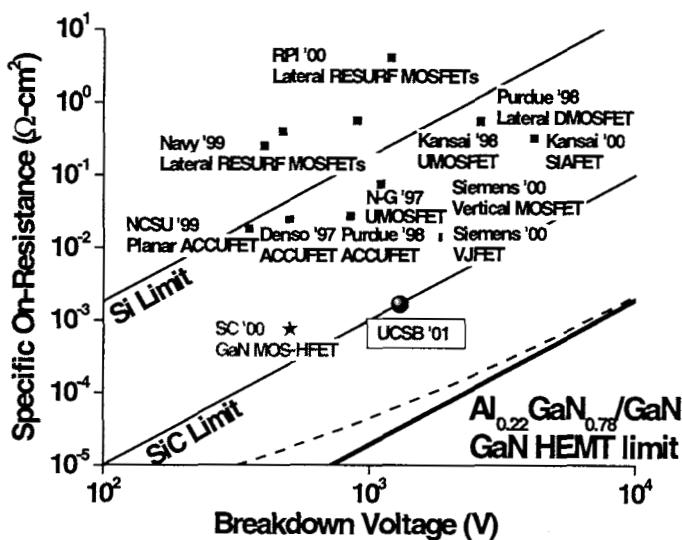


Fig. 2. Theoretical and measured values for specific on resistance versus breakdown for various material systems

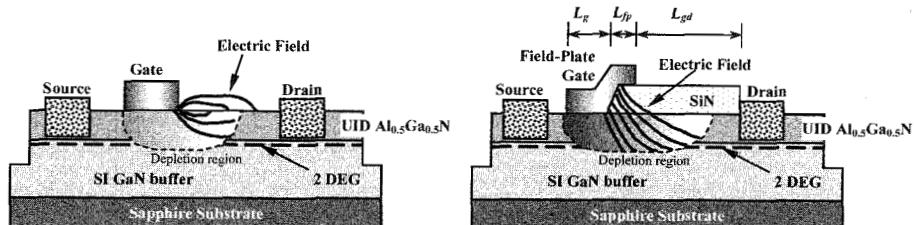


Fig. 3. The Field plate HEMT uses the overlapping gate to reduce the peak electric field.

nology. Reducing on-resistance is achieved by optimizing contacts, reducing source-gate spacing, and keeping the gate-drain length as small as possible while maintaining the necessary breakdown voltage. An additional challenge with AlGaN/GaN HEMTs is the presence of trap states on the surface of the AlGaN, which when ionized, reduce the channel charge and lead to RF-DC dispersion effects associated with the charging and discharging times of the trap states. These surface states can in some instances be passivated by surface layers such as SiN_x . Another important goal is the reduction of gate leakage, which can be accomplished using gate dielectrics.

2.1. Field Plate HEMT

Borrowing from work in AlGaAs/GaAs MESFETs^{1,2}, the ‘field-plate’ or ‘overlapping-gate’ design uses an extension of the gate metal over a dielectric to reshape the electric field, reducing the peak electric field at the drain-side edge of the gate. Figure 3 shows a diagram of this structure compared to a conventional structure. An illustration of electric field lines shows how field crowding is reduced at the edge of the gate for the

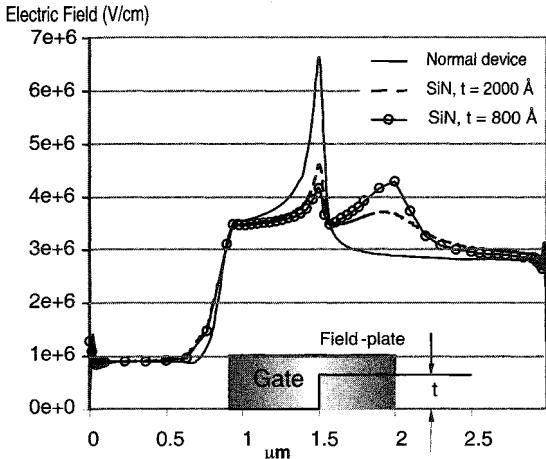


Fig. 4. The simulated electric field in an AlGaN/GaN HEMT with varying field plate insulator (SiN_x) thickness.

field plate device. Simulations of the electric field in the AlGaN/GaN HEMT show the expected reduction in the peak field. Figure 4 shows the expected electric field at the drain-side gate edge for different field plate configurations. Another variable in the field plate design is the length of the overlap. While increasing the overlap reduces the peak field, it may degrade the high frequency performance of the device.³

Figure 5 shows a simulation of the expected breakdown voltage as a function of the field plate overlap length, L_{fp} for a given field plate dielectric thickness. From these simulations the optimum dielectric thickness and field plate length can be determined.

2.1.1. Field plate device fabrication

Heterostructures for the AlGaN/GaN HEMTs were grown on c-plane sapphire using a GaN nucleation layer and 3 μm i -GaN buffer layer with typical resistivities above 200 $\text{M}\Omega \cdot \text{cm}$. The AlGaN barrier layer was 20 nm with carrier concentration in the channel of $8 \times 10^{12} \text{ cm}^{-2}$ and a mobility of $1000 \text{ cm}^2(\text{V} \cdot \text{s})^{-1}$. Ti/Al/Ni/Au with thicknesses of 20/200/50/40 nm respectively were deposited as ohmic contacts and annealed at 870°C for 30 seconds. The insulating layer under the field plate was 150 nm of sputtered SiN_x . Evaporated Ni/Au (20/300 nm) was used for gate metallization, overlapping (in the case of the field plate) by 300 nm. Device isolation was achieved with a Cl_2 RIE etch. Devices were fabricated with various gate/drain spacing (L_{gd}), gate lengths (L_g), and field plate lengths (L_{fp}). For all devices, the gate width was $25 \times 2 \mu\text{m}$.

2.1.2. Device performance

Improved source-drain breakdown voltages (570V) were obtained for the field plate HEMT with $L_{gd} = 13 \mu\text{m}$ and $L_g = 1 \mu\text{m}$. These devices exhibited 'hard' breakdown, suggesting that the gate-drain breakdown determined the source-drain breakdown voltage. Figure 6 shows the I-V characteristics of such a device in both the on-state and the off-state. The maximum drain current for this device was 520 mA/mm and the specific on-resistance was measured to be $1.5 \text{ m}\Omega \cdot \text{cm}^2$. By comparison, for conventional (no field-plate) devices the maximum breakdown achieved in this study was 470V, 20% lower

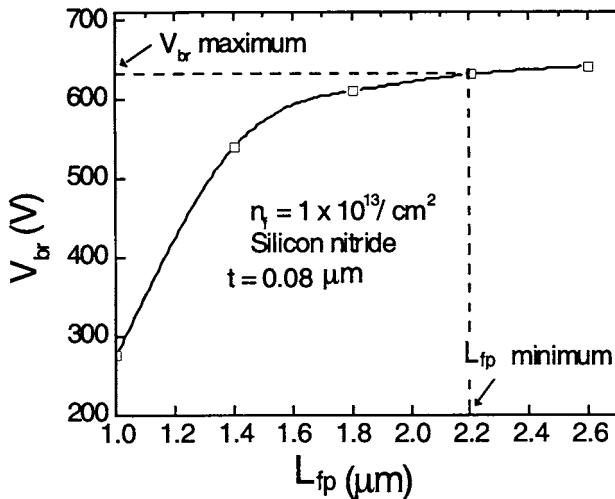


Fig. 5. Simulated breakdown voltage for an AlGaN/GaN HEMT with sheet charge, $N_f = 1 \times 10^{13} \text{ cm}^{-2}$ as a function of field plate overlap length, L_{fp} .

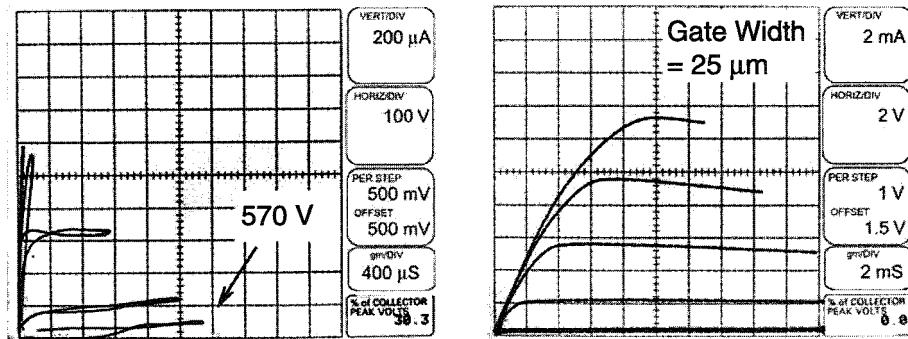


Fig. 6. Left: Maximum breakdown in the off-state measured at 570V. Right: Maximum current for field plate HEMT 520 mA/mm

than the field-plate device⁴.

2.2. Improving the *i*-GaN buffer

In the field plate experiments, devices with short gate-drain spacings had high gate leakage currents, and the field plate did not significantly increase the breakdown voltage as it did for larger spacings (see Figure 7). For short spacings it was thought that the breakdown mechanism was excessive gate leakage through the *i*-GaN buffer. Initial studies were performed on MOCVD grown GaN buffer layers grown on sapphire substrates. Oxygen was found to be the dominant source for excess carriers in the buffer layer, and

to reduce buffer leakage currents, growth conditions were tailored to introduce increased levels of carbon impurities, compensating the oxygen and reducing leakage currents from 20 mA/mm to 0.2 mA/mm⁵. Another, later improvement was the introduction of Fe doped GaN to create a more insulating buffer⁶. To improve thermal conductivity, future structures were grown by MOCVD on semi-insulating SiC substrates.

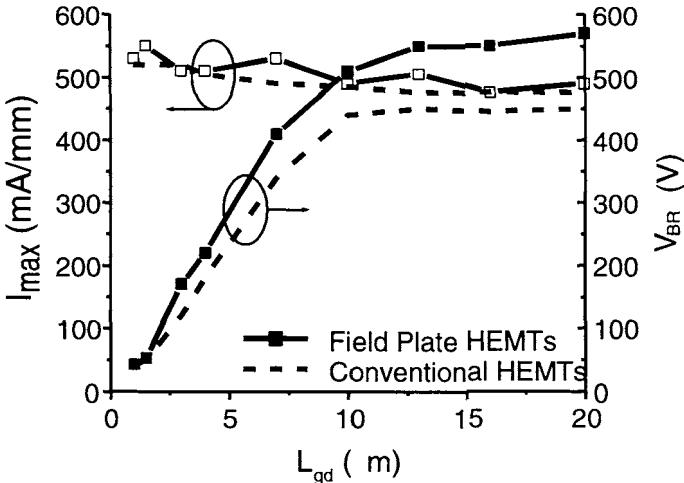


Fig. 7. Breakdown voltage of field plate and conventional AlGaN/GaN HEMTs as a function of gate-drain spacing.

2.3. Insulated Gate HEMT

Although changes to the buffer were effective in reducing leakage, and thus increasing breakdown voltages, the observed maximum breakdown voltage was still low for the AlGaN/GaN HEMT. A second improvement, the insulated gate HEMT further reduced leakage currents in these devices.

Figure 8 shows the relative breakdown voltages of two devices with differing leakage currents. The trend suggests that gate leakage is still a contributing cause of the early breakdown of the devices. With a 10 nm JVD (Jet Vapor Deposition) SiO₂⁷ layer under the gate in a conventional planar-gate structure, the gate leakage was reduced by more than 2 orders of magnitude, from 5×10^4 [A·cm⁻²] to 100 [A·cm⁻²]⁸. The drain current-voltage characteristics (Figure 9) for a HEMT with $L_{gd} = 20 \mu m$ and $w_g = 200 \mu m$ show a breakdown voltage in the off-state of more than 1000V, with a specific on-resistance of $3.1 \text{ m}\Omega \cdot \text{cm}^2$ with a gate bias of 2V.

Further improvements were made by switching to an e-beam evaporated SiO₂ layer under only the gate (the JVD sample had SiO₂ in the source and drain access regions as well). For this device, gate leakage was further reduced, and a breakdown voltage of 1300V achieved with a specific on-resistance of $1.65 \text{ m}\Omega \cdot \text{cm}^2$ at a gate bias of 0V. The threshold voltage for this device was -8V (see Figure 10). The resulting power device FOM: $V_{BR}/R_{on} = 9.94 \times 10^8$ [V²·Ω⁻¹cm⁻²] was higher at that time than any figures reported in the III-Nitrides or competing technologies⁸.

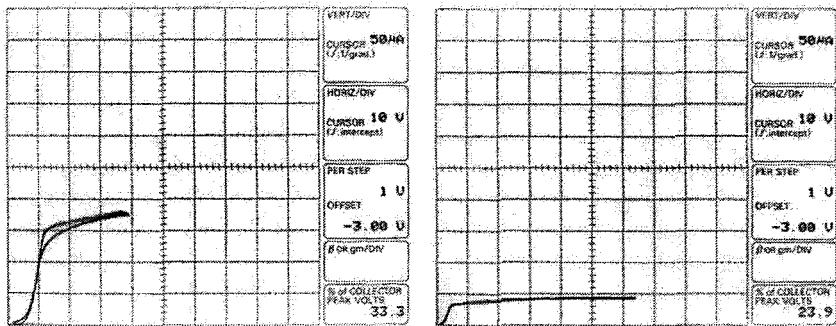


Fig. 8. Comparison of breakdown voltages for two devices. Left: Transistor with high leakage ($175 \mu\text{A}$) shows lower breakdown (310V). Right: Similar device with lower leakage current ($50 \mu\text{A}$) shows significantly higher off-state breakdown (400V).

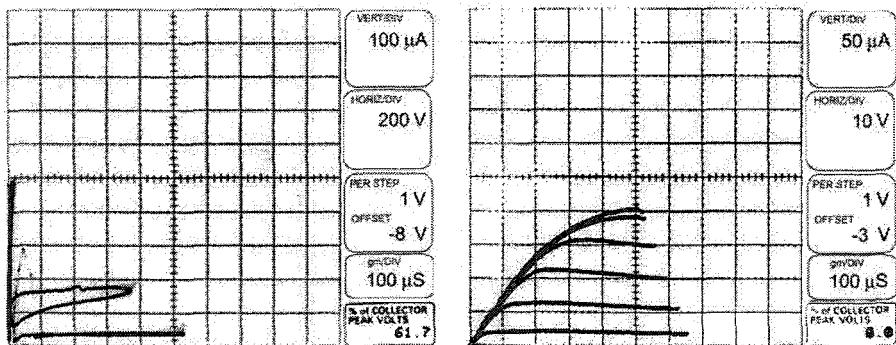


Fig. 9. GaN/Al_{0.22}GaN(25 nm) HEMT on SiC with 10 nm JVD SiO₂ cap as gate insulator. Left: Off-state characteristics show breakdown voltage over 1000V. Right: On-state characteristics show 1A/mm maximum drain current.

2.4. Surface Trapping and Passivation

Pulsed measurements revealed the effects of traps on the surface of the AlGaN barrier layer and in the insulating layer. Measurements made with an $80 \mu\text{s}$ gate voltage pulse showed significant reduction in the maximum gate current. Figure 11 shows this DC-RF dispersion clearly. Under pulsed conditions the maximum transistor current was very low, $<20\%$ of $I_{\text{max,DC}}$. The dispersion is caused by deep traps at the surface, or in the material where high fields exist during transistor operation. Electrons injected from the gate or the channel populate these traps and remain trapped over large time constants where they deplete channel charge and reduce the maximum drain current for the device⁹. The $80 \mu\text{s}$ pulse width corresponds to a switching speed lower than 6.25 kHz.

Although this problem is also common among microwave AlGaN/GaN HEMTs, its usual solution (SiN_x passivation) led to increased gate leakage and lower breakdown in these devices. To address this problem, interface properties of several potential gate dielectrics and passivants were studied by temperature dependent CV and photo-CV.

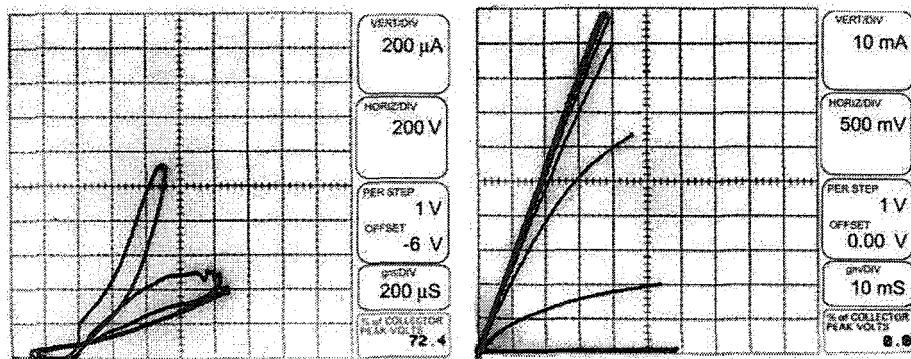


Fig. 10. Current-voltage characteristics of insulated gate HEMT using e-beam evaporated SiO_2 as a gate insulator.

| Material | $Q_F [\text{cm}^{-2}]$ | $D_{IT} [\text{cm}^{-2}]$ |
|--------------------------|------------------------|---------------------------|
| MOCVD SiN_x | -2.6×10^{12} | 7.9×10^{12} |
| PECVD SiN_x | -4.1×10^{12} | 5.8×10^{12} |
| PECVD SiO_2 | -5.0×10^{11} | $>> 1 \times 10^{13}$ |
| E-Beam SiO_2 | 6.4×10^{11} | $>> 1 \times 10^{13}$ |
| Sputtered SiN_x | -3.6×10^{12} | high $\times 10^{12}$ |

Table 2. Fixed charge and interface state density for various dielectrics and deposition methods

The properties of these materials are summarized in table 2.

SiN_x deposited using various methods produced lower trap densities than SiO_2 , and pre-deposition cleans were able to further reduce interface trap and fixed charge densities to 2.1×10^{12} and $2.9 \times 10^{11} \text{ cm}^{-2}$ respectively. The reactively sputtered SiN_x was the most effective in reducing DC-RF dispersion, however, and was therefore the passivant of choice for the power switch devices. To combine the benefit of reduced leakage afforded by the SiO_2 gate insulator and the dispersion reduction from sputtered SiN_x , a structure was developed with SiN_x passivated access regions and SiO_2 only under the gate with a final thick SiN_x passivation layer covering the entire device (Figure 12). The result is a device with several orders lower gate leakage than a conventional device, but with low dispersion measured by pulsed IV curves, and thus high switching speed and a high breakdown of 1000V.

2.5. Large Scale Devices

Although hall and pulsed IV characterization can give some prediction of large device performance, large devices must be fabricated and tested in order to characterize them. For the large periphery devices, a series of circular FETs are bonded together to form a single large device. The circular layout was chosen to reduce electric field crowding at the ends of the gate fingers. Ultrasonic wire bonding was used to combine the many small discrete cells into a larger periphery device. $\text{Al}_{0.28}\text{GaN}/\text{GaN}$ heterostructures were grown on SI SiC with 20 nm AlGaN barrier layers resulting in a charge of $1.24 \times 10^{13} \text{ cm}^{-3}$ with a room temperature hall mobility of $1725 \text{ cm}^2(\text{V} \cdot \text{s})^{-1}$. Ohmic contact metals were deposited: Ti/Al/Ni/Au (22/160/55/45 nm) and annealed at 870°C for 30 seconds. The

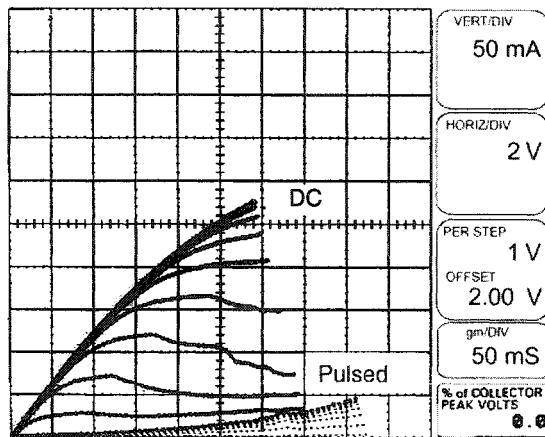


Fig. 11. Drain current-voltage characteristics for AlGaN/GaN SiO₂ insulated gate HEMT with DC and pulsed (80 μ s) gate bias.

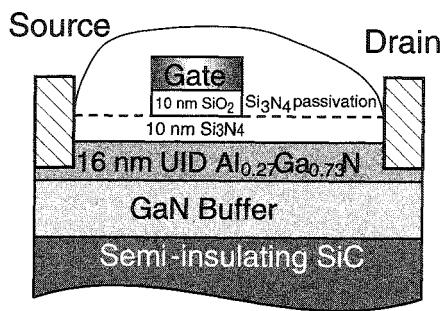


Fig. 12. AlGaN/GaN HEMT is passivated by reactively sputtered SiN_x after ohmic contact anneal, then gate metal is evaporated with SiO₂ insulating layer to reduce gate leakage.

measured contact resistance was $0.8\Omega \cdot \text{mm}$. After a surface clean, SiN_x was reactively sputtered (12 nm thick) over the entire sample. Gate metal is then evaporated on an SiO₂ insulation layer (also evaporated) and the stack is patterned using lift-off lithography techniques. A second thicker layer (100 nm) of sputtered SiN_x is then deposited for further protection of the surface, and the SiN_x is dry etched over the contact pads. Thick metal (Ti/Au) evaporated over the contact pads provides a base for wire bonding, which is used to connect gate and drain pads to the larger device.

2.6. Switching Characterization of AlGaN/GaN HEMTs

Although the highest breakdown voltage measured on small devices was 1300V, large periphery devices rely on many small devices bonded together and the breakdown voltage is limited by the smallest device. In initial experiments, 64 devices (38.4 mm total periphery) were bonded together with a breakdown voltage of only 600V. In addition, due to large parasitic interconnect resistances, the measured on-resistance of the device was measured at 1.8 Ω , or 70 $\Omega \cdot \text{mm}$. The interconnect resistance in this case, however was

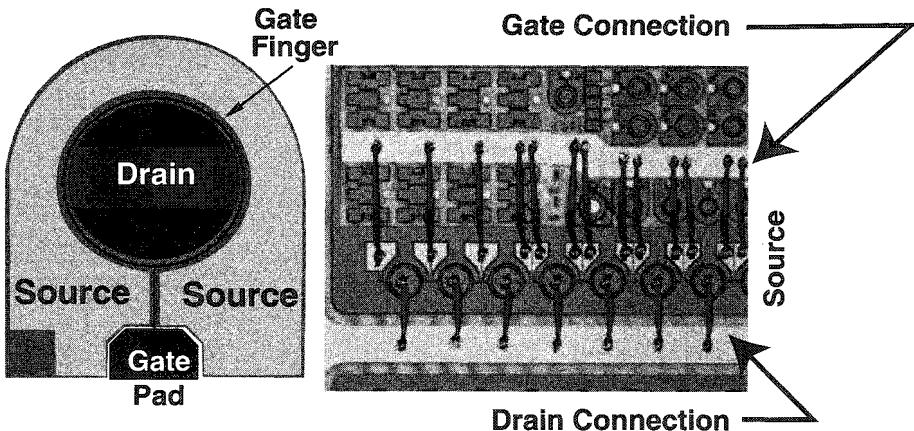


Fig. 13. Device layout for large periphery switching HEMT. Wire bonds connect individual gate and drain contacts to main bus lines. Each cell can be tested separately before connecting to the network to mitigate yield issues. Each smaller device has a gate width of 0.6 mm.

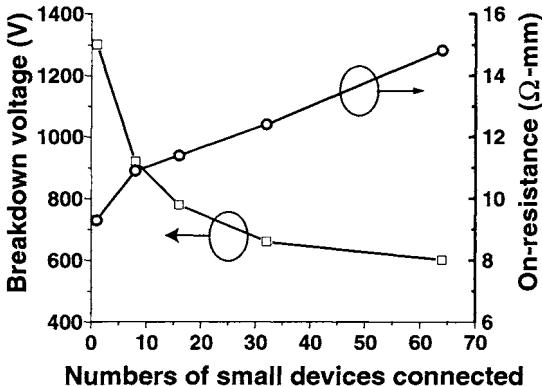


Fig. 14. As the number of connected devices increases, the breakdown decreases with the statistical spread of the individual device breakdown, and on resistance increases with parasitic interconnect resistance.

1.4Ω , implying an intrinsic R_{on} of 0.4Ω , or $14.8 \Omega\text{-mm}$. To mitigate this issue, individual transistors were pre-tested for breakdown, and only devices having a breakdown higher than $750V$ were connected to the bus. Figure 14 shows the dependence of the breakdown and on-resistance on the number of interconnected devices.

Devices were measured under conditions of resistive and dynamic load. Figure 15 is a schematic of the circuit for dynamic load measurement, performed by V. Mehrotra at the Rockwell Science Center (RSC)¹⁰. During a charging pulse, the DUT is 'on' long enough to establish the desired current in the inductor. With the channel pinched off, the inductor current flows freely through the diode/inductor pair, and the voltage across the DUT rises to the voltage of the source (blocking voltage). Next, another pulse is sent

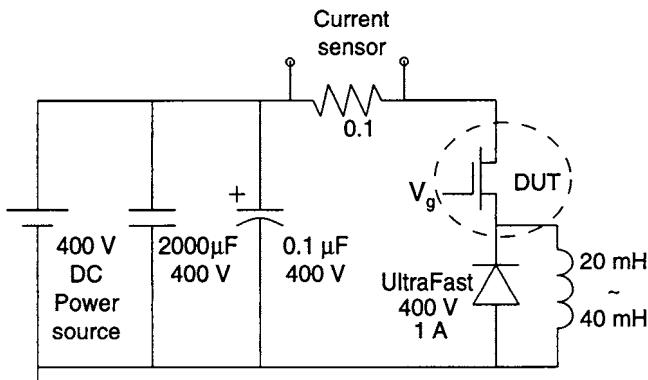


Fig. 15. The circuit used to test the switching speed of the AlGaN/GaN HEMT under realistic conditions. A free flowing current through the inductor circuit supplies the constant current source for the turn-on of the device

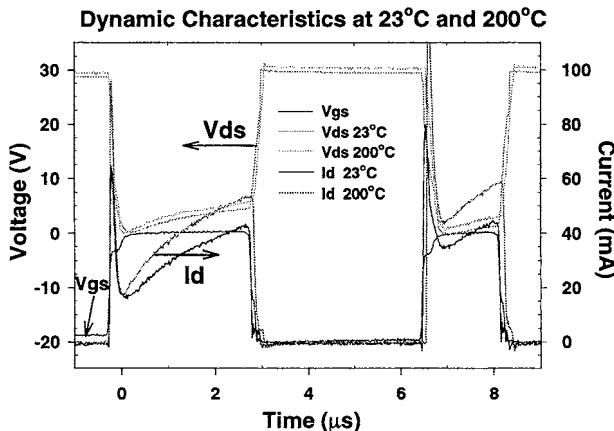


Fig. 16. Dynamic characteristics of an element of a 64 device array of AlGaN/GaN HEMTs at room temperature and at 200°C.

to the gate of the DUT, and as the device enters the forward active regime, the current sensor measures the turn-on transient as the DUT discharges the large capacitance through the inductor. A final short pulse turns off the transistor again, and the turn-off transient is measured.

2.6.1. Device measurements

The switching characteristics of the transistors were measured using dynamic and resistive loading. Under resistive load, devices blocked 110V, had a maximum drain current of 1.4A, with a switching time under 30 ns. Conduction losses were $\sim 0.68\text{W}$, corre-

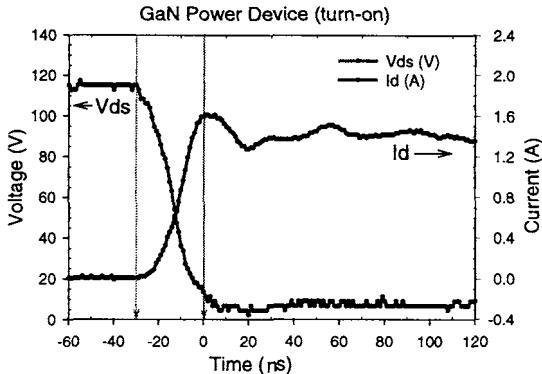


Fig. 17. Turn-on characteristics of GaN HEMT device under resistive load.

sponding to an on-resistance of $0.4\ \Omega$ (See Figure 17). Devices were also measured to a blocking voltage of 250V with a switching current of $\sim 2.5\text{A}$.¹⁰ Figure 16 shows results from switching measurements on a single element with a dynamic load at room temperature and 200°C .

3. Heterojunction Bipolar Transistors for High Power Switching

AlGaN/GaN HBTs have potential applications in power switching due to the higher current density (in terms of die area) and high breakdown. Partly due to difficulty of growth and processing as well as inherent problems with the GaN:Mg p-type base, however, the AlGaN/GaN HBT is several years behind the AlGaN/GaN HEMT. In addition to high breakdown, the HBT as a high voltage switch must have high current gain to reduce the load on the driving circuit, and low parasitic resistances to maximize switching speed and efficiency.

3.1. Etched Emitter AlGaN/GaN HBT

Etched emitter device structures were grown by MOCVD on sapphire substrates. Typical structures included a low temperature nucleation layer followed by several hundred nm of UID GaN. The subcollector was 500 nm GaN doped $1\text{-}5\times 10^{18}\text{cm}^{-3}$ Si, with a 250 nm UID ($\sim 5\times 10^{16}\text{cm}^{-3}$) collector, 100-200 nm GaN:Mg ($p\sim 5\times 10^{17}\text{cm}^{-3}$) and 100 nm $\text{Al}_{0.1}\text{Ga}_{0.9}\text{N}:Si$ emitter capped with a GaN:Si contact layer. The structure was patterned by Cl_2 RIE into a conventional stacked mesa structure. Due to the lack of an effective wet etch for GaN, the emitter mesa was defined with an isotropic dry etch, and base contacts were not self-aligned.

The most difficult aspects in developing npn AlGaN/GaN HBTs are associated with the Mg doped p-type base. Because Mg is a deep acceptor (110 - 200 meV)¹¹, the doping concentration to achieve sufficient carrier concentration is much higher than the hole concentration ($1\times 10^{20}\text{cm}^{-3}$ Mg leads to about $1\times 10^{18}\text{cm}^{-3}$ holes). In addition, holes in GaN, with about 4 times the effective mass of electrons, have mobilities in the range of $5\text{-}20\text{ cm}^2(\text{V}\cdot\text{s})^{-1}$. An early improvement was to add an extrinsic base regrowth step to improve the base contact, resulting in the first demonstration of a GaN bipolar transistor¹². This device had a common emitter current gain of 3, a high early voltage, and an unusually high offset voltage.

The regrown base HBT reduces the contact voltage barrier to the p-GaN surface (Figure 18). After the RIE emitter mesa etch, the emitter is capped with a dielectric

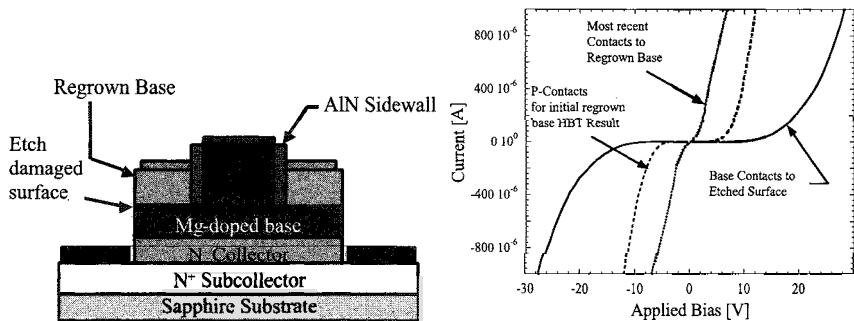


Fig. 18. Comparison showing the improvement resulting from a combination of a less-damaging etch and a regrown extrinsic base.

mask, AlN_x . In addition to protecting the emitter mesa during the MOCVD regrowth, the AlN_x mask is selective to GaN growth, and chemically inert in the reducing $\text{NH}_3 + \text{H}_2$ environment. The etch damage is buried with the new GaN:Mg growth, resulting in an improvement in contact quality as well as increased base conductivity. Used in conjunction with a low-etch-damage RIE process, the base contact voltage barrier is as low as 1V (Figure 18).

A second improvement was a move, in the case of the etched emitter device, to an MBE grown structure. MBE growth of the active layers allowed, in this case, for more precision layer thicknesses, better uniformity, and sharper junction placement. Experiments with these devices yielded insight into the role of dislocations in emitter-collector leakage¹³, as well as the offset voltage of the devices¹⁴ and small signal RF characteristics¹⁵. With etched emitter structures, however, current gain at the time was limited to values below 4.

3.2. Regrown Emitter HBT

The motivation for the regrown emitter HBT is the lack of a need for an etch stop for the emitter mesa etch, and improved base contacts leading to lower parasitic base resistance and common emitter offset voltage. In addition, the regrown emitter HBT allows for more accurate base emitter junction placement than conventional structures grown by MOCVD because it is not subject to the Mg memory effect. The common emitter characteristics of a regrown emitter device in Figure 19 show a current gain of 15, a low offset voltage, and an early voltage, $V_A > 400\text{V}$. The structure was grown by MOCVD on sapphire. The base thickness was 100 nm with an acceptor concentration, $N_A = 2 \times 10^{19} \text{ cm}^{-3}$, leading to a carrier concentration of $p \sim 5 \times 10^{17} \text{ cm}^{-3}$. The emitter was GaN:Si, $N_D = 5 \times 10^{18} \text{ cm}^{-3}$ 100 nm thick. The collector was $8\mu\text{m}$ UID GaN with a background donor concentration of $N_D = 4 \times 10^{15} \text{ cm}^{-3}$. The initial device growth consisted of the subcollector, collector, and base layers. An AlN_x dielectric mask was patterned with openings for the emitter structure (Figure 20). The emitter mesa is then grown selectively. The growth mask is removed, and device processing completed with the conventional Cl_2 RIE step to access the subcollector. Although attempts were made to selectively grow the emitter by MBE, these efforts have not yielded a working device. Photo-Electro-Chemical, PEC, wet etch techniques show promise for selectively etching n-type over p-type material¹⁶, this etch would allow conventional processing of fully grown devices without the damage associated with the RIE etch. The etch stop becomes less effective, however, when the etch stop layer thickness, W_b is less than L_n , the diffusion length of electrons in the base - a necessary condition for transistor operation.

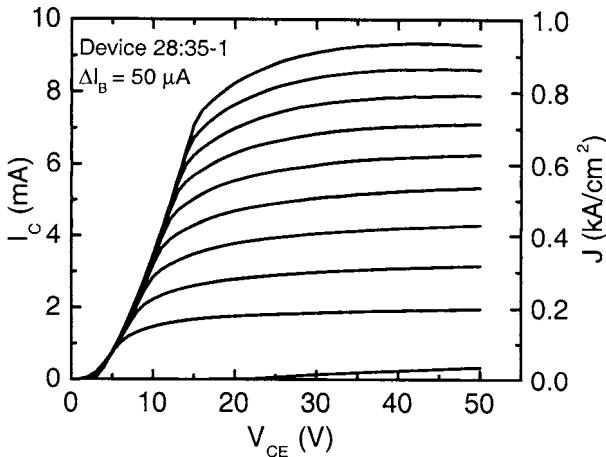


Fig. 19. Common emitter characteristics of AlGaN/GaN HBT with current gain of 15.

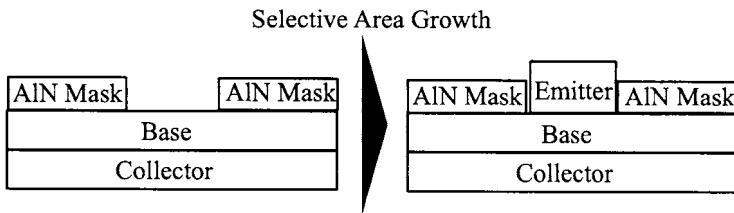


Fig. 20. The selective emitter regrowth step is shown above. The AlN_x mask is used to protect the base surface. The emitter structure is then selectively grown by MOCVD to form emitter mesas. Later, the mask is removed, and the base mesa is etched by Cl_2 RIE. Finally, base, emitter, and collector metallizations are applied using standard lift-off lithographic techniques.

Although the regrowth interface at the base-emitter junction of the regrown emitter device, may lead to reduced transport or injection efficiency, this device has achieved superior current gain to etched emitter devices. This is because of difficulties in the etched emitter approach with the non-selective RIE emitter mesa etch and the base surface damage it causes.

3.3. Offset Voltage

The effect of the poor base conductivity and contact voltage barrier is apparent in the common emitter offset voltage. The offset voltage is the collector-emitter voltage in the common emitter mode where the net collector current becomes positive. At this point, both the base-emitter and base-collector diodes are forward biased. The collector current

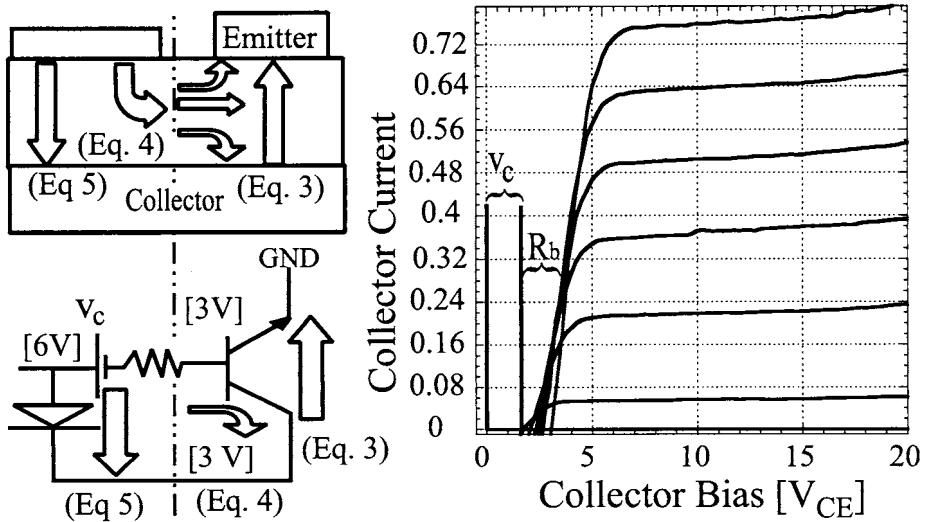


Fig. 21. Large parasitic offset is due to the voltage drop associated with lateral base current. The numbered arrows in the schematic (above left) refer to equations which describe them. The voltages in the wiring diagram (below left) are examples of a bias condition in which the parasitic base-collector diode is forward biased, while the intrinsic device is zero-biased. This is the mechanism for the parasitic offset voltage observed in GaN HBTs.

saturates as the base-collector diode becomes reverse biased. The parasitic offset voltage observed in the GaN HBT is explained as follows:

Because of a high voltage drop across the base contact and a high lateral resistance, the voltage of the base layer under the contact is substantially higher than the voltage of the base in the active device (Figure 21). This effectively divides the area under the emitter and the area under the base contact into two devices - the active transistor and a parasitic base-collector diode. The difference between the base voltage under the base contact and the base voltage under the emitter mesa at any given base injection current is the parasitic offset voltage of the transistor. For example, it may require a 6V base emitter contact voltage to inject a $100 \mu\text{A}$ base current. While the base-emitter junction forward bias is limited by the bandgap to 3.4V, the base voltage under the base contact is $\approx 6\text{V}$. If the collector-emitter voltage is 3.4V, the base-collector diode under the base contact is then forward biased even while the base-collector junction under the emitter mesa is zero-biased (Figure 21). Also, because the contact characteristic is nonlinear, the voltage drop across the contact varies strongly with current density. This leads to a much larger voltage drop across the portion of the contact contributing to the lateral current which feeds the active transistor. This is indicated in Figure 21 as a 'battery' element. The following are equations for the collector current components in an HBT relevant to the common emitter offset voltage:

$$V_{\text{offset}} \equiv V_{CE} \Big|_{I_C=0} \quad (1)$$

$$I_{C_{\text{total}}} = I_{CE} - I_{BC_i} - I_{BC_x} \quad (2)$$

$$I_{CE} = \alpha \cdot A_{\text{emitter}} \cdot J_s |_{BE} \cdot \exp \left[\frac{V_{BE}}{V_T} \right] \quad (3)$$

If $V_{CB_{\text{intrinsic}}} \neq V_{CB_{\text{extrinsic}}}$

$$I_{BC_i} = A_{\text{intrinsic}} \cdot J_{s_{BC}} \cdot \exp \left[\frac{V_{BC_i}}{V_T} \right] \quad (4)$$

$$I_{BC_x} = A_{\text{extrinsic}} \cdot J_{s_{BC}} \cdot \exp \left[\frac{V_{BC_x}}{V_T} \right] \quad (5)$$

Here we use α as an overall efficiency term that includes emitter injection efficiency as well as the transport efficiency across the base. Equations (4) and (5) split from a single equation when the external base-collector bias differs from the internal bias. In this case, a higher voltage is required to turn off the extrinsic base collector diode. Figure 21 shows the contributions of the offset voltage equations to the total collector current, I_C . Analysis of a measured common emitter characteristic show these effects on the DC performance. To reduce this offset voltage, the base contact and lateral resistances must be reduced- or the extrinsic collector eliminated as in the transferred substrate Schottky collector technology¹⁷.

3.4. Increasing the Breakdown of AlGaN/GaN HBTs

As discussed earlier, devices fabricated in the III-N system are capable of withstanding very high blocking voltages. Calculations predict an ideal breakdown voltage of over 1000V for an HBT with a 10 μm collector doped $\sim 1 \times 10^{16}\text{cm}^{-3}$.¹⁸ Technological issues currently limit the realization of this goal, however, and several approaches were used to increase the breakdown of the AlGaN/GaN HBT.

3.4.1. Thick collector and dislocations

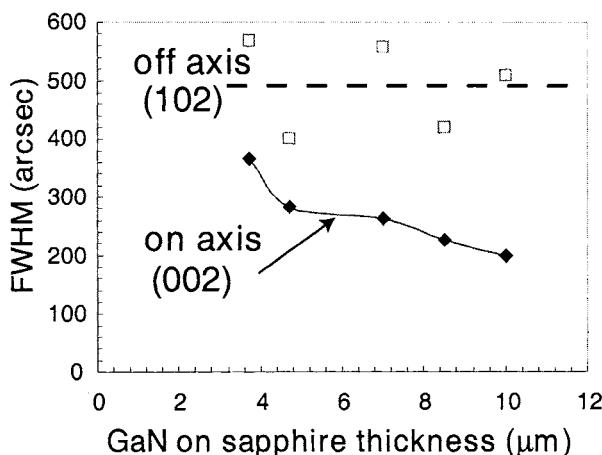


Fig. 22. FWHM of x-ray reflections from GaN on sapphire as a function of GaN thickness. Reduction in on-axis peak width suggests a reduction in dislocations at the surface for thicker films

Devices were heteroepitaxially grown on sapphire substrates using MOCVD and had threading dislocations on the order of $5 \times 10^8\text{cm}^{-2}$. Evidence suggests that dislocations

act as vertical leakage paths^{19,13} and as base collector leakage can assist in the breakdown of the junction, dislocations are undesirable. By growing thicker GaN layers, a certain number of these dislocations react and sometimes are annihilated, leaving fewer threading dislocations at the surface²⁰. Figure 22 shows the full width at half maximum (FWHM) of on axis (002) and off-axis (102) x-ray rocking curves measured on different thickness GaN templates grown on sapphire. The FWHM of the (002) reflection decreases with increasing GaN thickness while the FWHM of the (102) reflection remains flat. This indicates a reduction in screw character dislocations intersecting the surface without a significant change in edge-character dislocations. This is consistent with the observation that screw character dislocations are more likely to react and change direction or be annihilated than those with edge character. By growing the underlying GaN films thicker, the number of threading dislocations intersecting device layers is reduced, and collector leakage likewise reduced. Another advantage of using thicker layers for HBT substrates is a reduction in background oxygen concentration as the thickness increases. Except for limitations associated with Kirk effect onset, the lowest collector doping achievable is desirable for increased base/collector breakdown voltage.

3.4.2. Reducing base mesa etch damage

Although alternatives exist to the dry etching of GaN, technical challenges currently make these impractical for the HBT. Therefore, to contact the collector/subcollector layers, a Cl₂ RIE dry etch was used to pattern the base mesa. A drawback to this technique is the damage done to the base-mesa sidewall during the etch. It is desirable to reduce collector contact resistance by etching the base mesa down to the heavily doped subcollector, but the result, especially in structures with thick collector layers, may be detrimental to collector-base leakage. One of the methods explored to mitigate this issue was to reduce the etch depth and separate the collector contact laterally from the base mesa. This offers a combination of a lateral collector, similar to the drain in a HEMT, and the vertical injector structure of the HBT. While the as-deposited contacts to the thick UID layer are typically not ohmic, in forward active mode, the Schottky collector is forward biased and does not introduce a barrier to current flow.

Base/collector diodes were fabricated to optimize this lateral spacing, and investigate the use of a bevelled etch and SiN_x passivation of the etched sidewall. Figure 23 shows the reverse breakdown voltage of the diode as a function of base/collector separation.

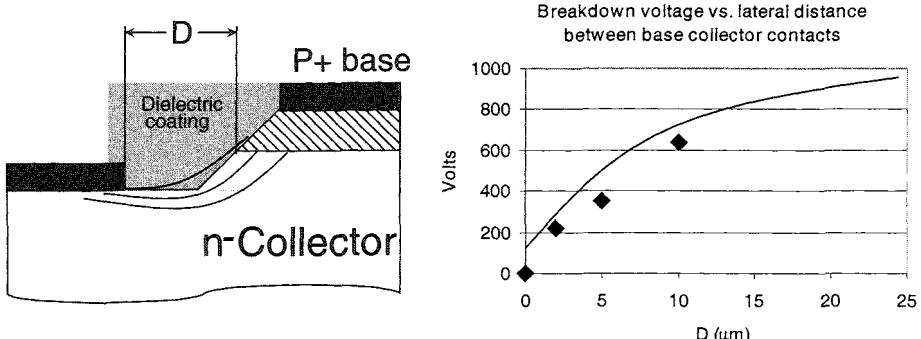


Fig. 23. Left: Schematic of lateral diode structure with bevelled shallow etch and surface passivation. Right: Measured breakdown voltage of diodes as a function of contact separation.

4. Conclusions

Over the past several years, the power performance of AlGaN/GaN HEMTs has steadily improved. Difficulties in the MOCVD growth of the AlGaN/GaN heterostructures were overcome and the physical understanding of these heterostructure electronic devices has matured considerably. Currently, several industrial interests are actively pursuing the use of AlGaN/GaN HEMTs for military and commercial applications. In addition, recent progress in AlGaN/GaN HBTs has shown promise, as well as illuminating several obstacles to be overcome. Future work in the HEMT arena will focus on the refinement of the AlGaN/GaN HEMT with further investigation into the role and interrelation of material defects, polarization effects, and device performance. Further effort on AlGaN/GaN HBTs will seek to solve the many remaining technological issues to gain understanding of the potential for these devices.

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ETCHED APERTURE GaN CAVET THROUGH PHOTOELECTROCHEMICAL WET ETCHING

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We describe the fabrication of the CAVET (Current Aperture Vertical Electron Transistor) by Photoelectrochemical (PEC) formation of a current aperture. Etch process is quite naturally critical to the achievement of the etched aperture in CAVET. We provide some background on that etch process, and the subsequent modification and optimization of the process for CAVET fabrication.

Keywords: GaN; etching; device fabrication.

I. Introduction

Recently, great progress has been made in the demonstration of high power devices in the III-nitride materials. These devices include AlGaN/GaN high electron mobility transistors (HEMTs)¹ and heterojunction bipolar transistors (HBTs)². In HEMTs, it appears that the nature of the surface states gives rise to a large DC-RF dispersion, limiting the large signal operation of these devices³. Some mitigation has been provided - through various passivation schemes, but these approaches are not yet fully reproducible and reliable, and thus are still under assessment. A novel device in which the primary current flows in a direction perpendicular to the surface should offer performance advantages. This is the Current Aperture Vertical Electron Transistor (CAVET), shown in Figure I.1. A two dimensional electron gas (2DEG) is formed at the interface of the AlGaN and GaN materials. The current flows vertically between the sources and drain, and is modulated by voltage applied to the gate. A current aperture limits the extent of the current flow in the z-direction.

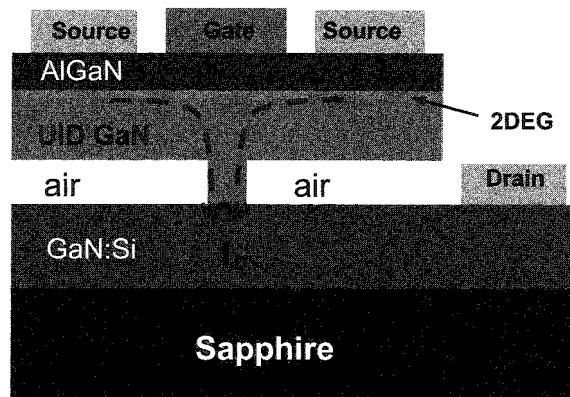


Fig. I.1. Systematic structure of Current Aperture Vertical Electron Transistor (CAVET)

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One approach to fabricate the CAVET is to form the current-confining layer by etching an aperture through insulating GaN and regrowing active material, an additive approach ('regrown' CAVET). A complementary technique for the formation of the CAVET structure involves the formation of a current aperture through a subtractive technique: *i.e.*, etching away material in the aperture region. To achieve this goal, there must be a high degree of control and selectivity associated with the lateral etch process to be used. Although dry etching⁴ techniques have been successfully used on the nitrides, there continue to be issues associated with ion-induced damage⁵ using dry etching. In addition, there has been no demonstration of substantial lateral etching in gas-phase etch processes. An alternative process is wet PhotoElectroChemical (PEC) etching. Since first demonstrated by Minsky *et al.*⁶, PEC wet etching has been widely applied to etch nitride materials. In addition to the basic characterization of PEC etching on nitride materials⁷⁻¹⁵, reports have focused on achieving smooth, etched surfaces with PEC etching¹⁶⁻¹⁹, as well as dopant selective^{20,21} and bandgap selective etching^{22,23}. The application of PEC etching to the fabrication of CAVET devices requires the development of a process that will produce a smooth, controlled and selective lateral etch. In Sections II through III below, we will first give a short summary of the important features of PEC etching, and then discuss the particular optimization process used to identify the etch conditions to form the CAVET.

II. Vertical PEC Etching of GaN

Photoelectrochemical wet etching includes two primary components: a light source and electrochemical cell (Fig. II.1). The electrochemical cell is basically an electrical circuit between the semiconductor and the Pt electrode with an electrolyte serving as the conductive medium. When the UV light illuminates the semiconductor, electron/hole pairs are created. Holes oxidize the semiconductor (anode) to a soluble form, which is dissociated by an electrolyte. Thus, etching occurs. In our experiment, a Xe lamp is used as the light source, and a variety of electrolytes are used, including dilute KOH, HCl, and $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$. The bias can be applied between the semiconductor and a Pt wire.

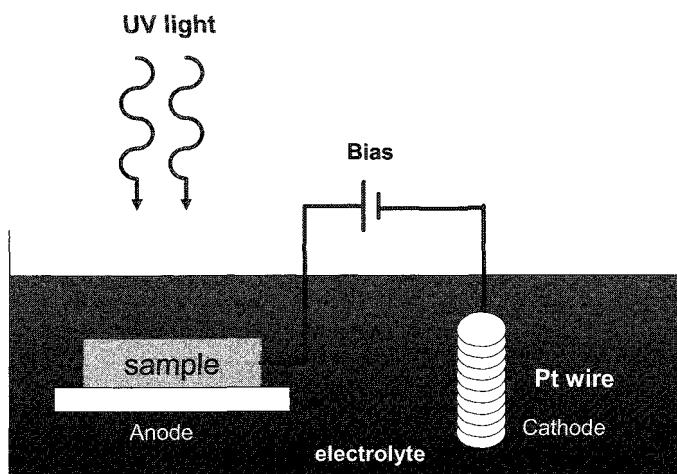


Fig. II.1. Photoelectrochemical wet etching experiment set-up

A. Power and Bias

Since we had earlier found that KOH produced rapid vertical etch rates in GaN, most of our initial experiments were carried out using 2.2M KOH. The following experiments characterize the etch rate of n-GaN, grown by MOCVD on sapphire substrates. Ti/Au is patterned on n-GaN and serve as a metal mask. Bias can be applied between the metal on GaN and Pt wire. Figure II.2a shows the evolution of the etched profile of GaN subject to illumination power of 1000W and an applied bias of 1V. A fairly rapid etch rate of 2 $\mu\text{m}/\text{minute}$ was achieved (Figure II.2b), with resulting vertical sidewalls. The rough texture of the etched surface after 20 seconds etching is characteristic of the etch morphology of the material, and indicates the important role of threading dislocations in the GaN.

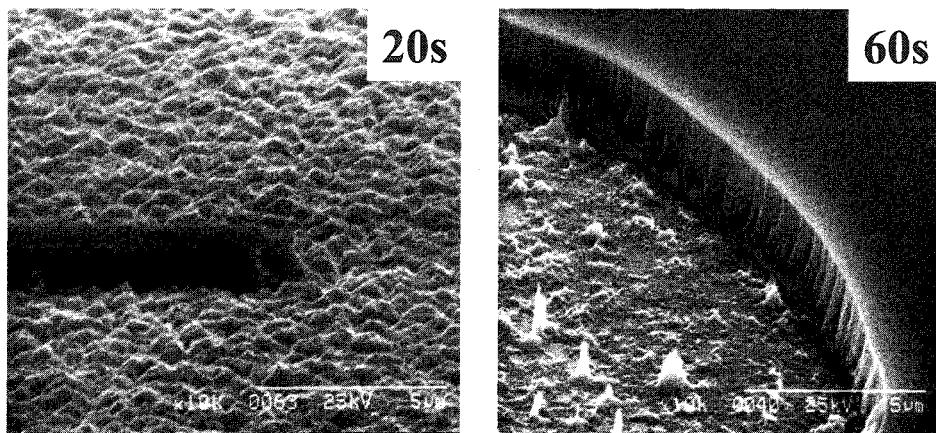


Fig. II.2a. Time dependence of n-type GaN etching morphology

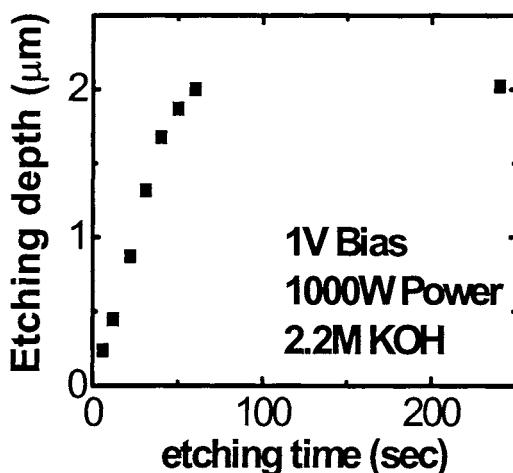


Fig. II.2b. Time dependence of n-type GaN etch depth

Keeping the bias voltage constant, the change in GaN etch rate as a function of incident power is shown in Figure II.3. The linear dependence of the etch rate with lamp power is a good indication that the etching is photo-driven in nature. For a fixed value of incident power, the increase in bias similarly produces an increased etch rate.

Bias can change the electrical field in the semiconductor near the electrolyte interface, which can modulate the hole confinement at the anode. It also permits more efficient electron removal to the cathode, which is shown in Figure II.4.

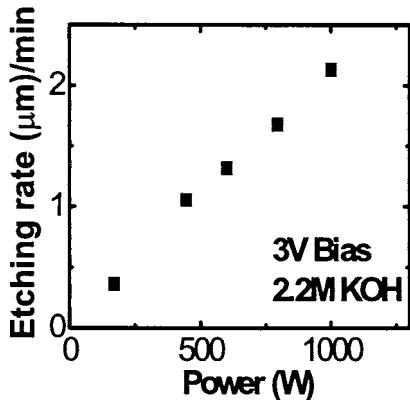


Fig. II.3. Power dependence of n-GaN etch

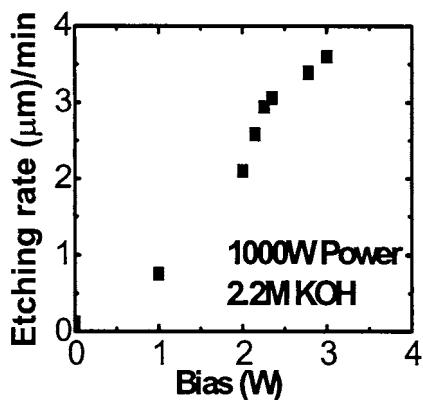


Fig. II.4. Bias dependence of n-GaN etch

B. Concentration dependence of KOH

A remarkably different etch morphology is revealed when the KOH concentration is modified, as shown in Figure II.5. The rough, hillock morphology seen at 2.2 M KOH or higher concentrations is replaced by the whisker like morphology seen in Figure II.5a. This was first reported by Youtsey *et al.*²⁴, who identified the whiskers with the distribution of threading dislocations in the GaN. The threading dislocations serve as traps for the photogenerated carriers²⁵, creating regions of reduced etch rate. The diameter of the whisker can be related to the hole diffusion length and depends on the electrolyte type and concentration. Concentration dependence in Figure II.5b shows the etch rate increase with concentration at low concentration, and then decrease with high concentration. This may due to less efficient removal of the reactants at the high concentration, which limits the etch process.

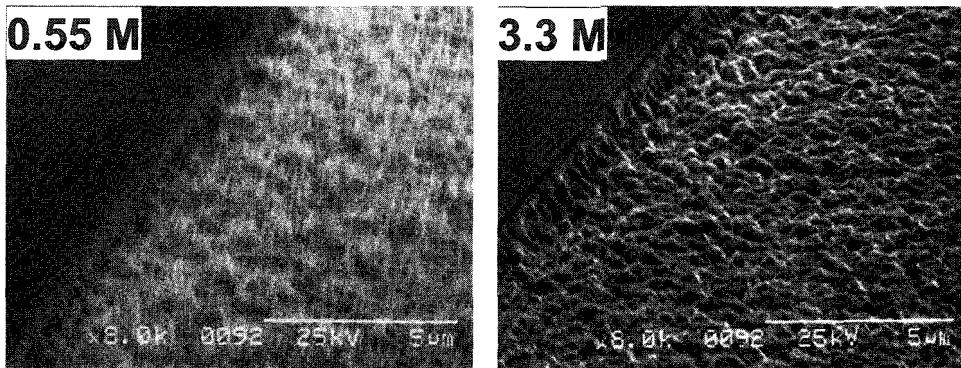


Fig. II.5a. Whiskers morphology under 0.55M KOH and hillock morphology under 3.3M KOH (1000W Power, 2.9V Bias, 40sec Time)

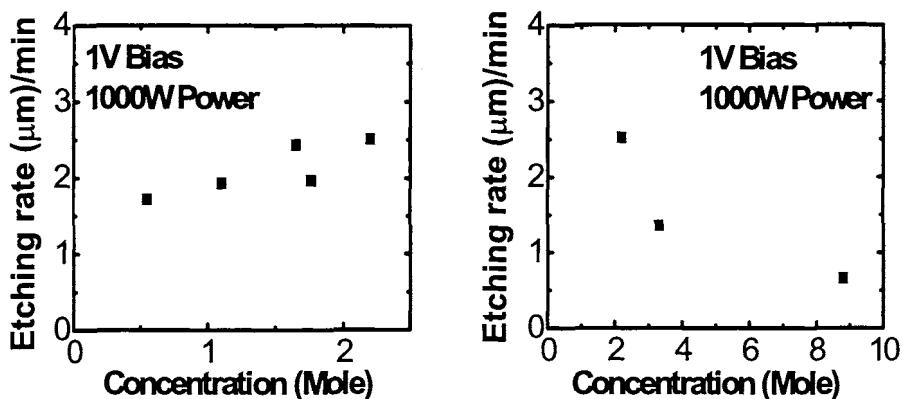


Fig. II.5b. Concentration dependence of n-type GaN etch rate

C. Selective Etching

A signature of PEC etching in most semiconductors is the dramatically higher rate of etching n-type materials over semi-insulating or p-type materials²⁶. This is referred to as dopant selective etching. This is a consequence of the bandbending at the material-electrolyte interface, and the efficacy of hole confinement. Holes in n-materials at the semiconductor /electrolyte interface prefer to move to the electrolyte due to the upward band banding. For p-type semiconductors, the downward bandbending take holes away from the interface. Thus, the selectivity is achieved between n and p materials in PEC etching. The selectivity of etching n-GaN over p-GaN²¹ is shown in Figure II.6.

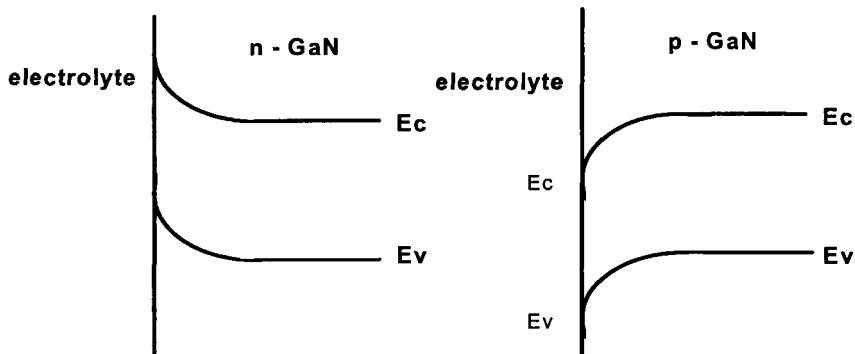


Fig. II.6a. Different bandbending of n-GaN/electrolyte and p-GaN/electrolyte interface

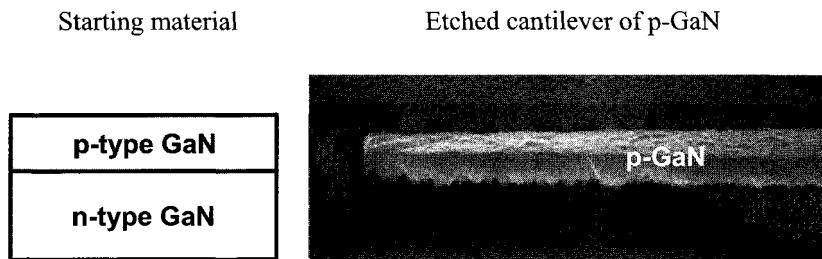


Fig. II.6b. Selective etch n-type GaN over p-type GaN

In addition, etch selectivity in a PEC process should be controlled by the wavelength of the illuminating source relative to the bandgap of the material to be etched. It should be possible to design a process where the lower bandgap material is etched selectively, leaving only the higher bandgap material intact. This is called bandgap selective etching²². This last feature of PEC etching will be a critical component in designing an appropriate etching process for the CAVET.

III. Designing an Etch Process for the CAVET

The CAVET will be formed through the selective removal of material to form a thin aperture below the gate (see Figure I.1). To achieve the controlled formation of an aperture, we insert a thin layer of ‘sacrificial’, lower bandgap material that will be selectively removed by the PEC etch.

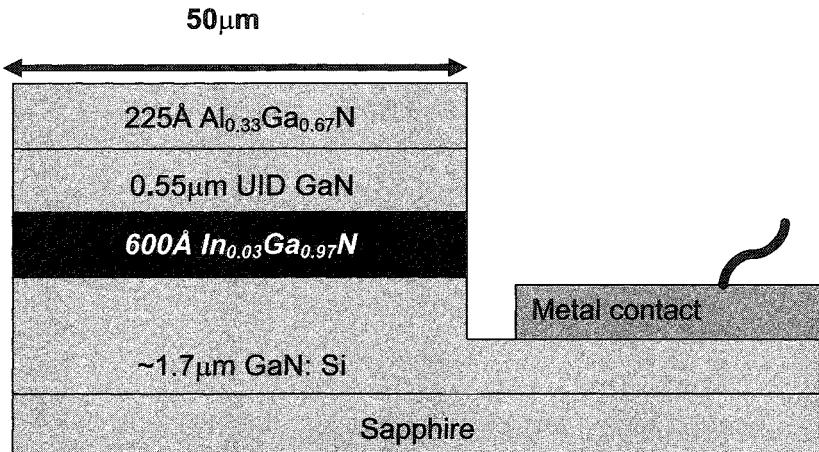


Fig. III.1. Test Structure for CAVET Etch studies

Our initial structures comprised 60 nm of $\text{In}_{0.03}\text{Ga}_{0.97}\text{N}$. The composition of the Indium was chosen to produce a high enough band offset from the surrounding GaN so that bandgap-selective etching could be achieved. The thickness of the InGaN layer was chosen to assure a reasonable lateral etch rate of the material, while at the same time not providing a large perturbation to the operation of the device. The full structure is shown in Figure III.1, and is comprised of a $\sim 1.7\mu\text{m}$ n-type ($\sim 6 \times 10^{17} \text{ cm}^{-3}$ Si doped) GaN base layer, followed by $600\text{\AA} \text{In}_{0.03}\text{Ga}_{0.97}\text{N}$, and $0.55\mu\text{m}$ unintentionally doped (UID) GaN ($N_D \sim 5 \times 10^{16} \text{ cm}^{-3}$), $225\text{\AA} \text{Al}_{0.33}\text{Ga}_{0.67}\text{N}$ cap. $50\mu\text{m}$ wide stripes were patterned using optical lithography. 1 μm thick mesas were formed by Reactive Ion Etching (RIE) to expose the InGaN layer. 300 Å Ti/ 1500 Å Au was deposited to the bottom GaN so a bias can be applied between the sample and cathode during the etching. Initial etch results, using the 2.2M KOH concentration described above produced rough-etched surfaces with poor InGaN-GaN selectivity, which is shown in Fig. III.2.

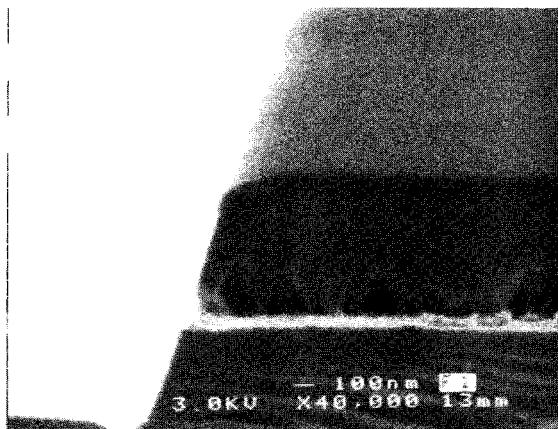


Fig. III.2. Rough etched surface – cones morphology, under 2.2M KOH

A. Orthogonal Array Experiments and Importance of KOH Concentration

In order to achieve bandgap selective PEC etching, a filter of $2\mu\text{m}$ thick MOCVD grown n-type GaN on sapphire is placed between the light source and the sample to be etched during the etching. The sharp absorption spectrum of the GaN filter is shown in Fig III.3a.

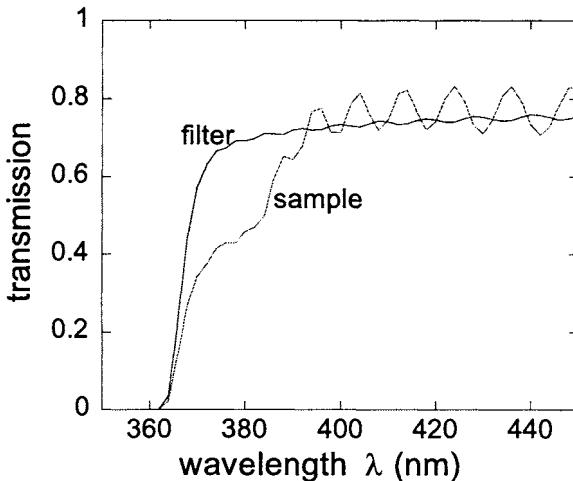


Fig. III.3a. Absorption spectrum of the GaN filter

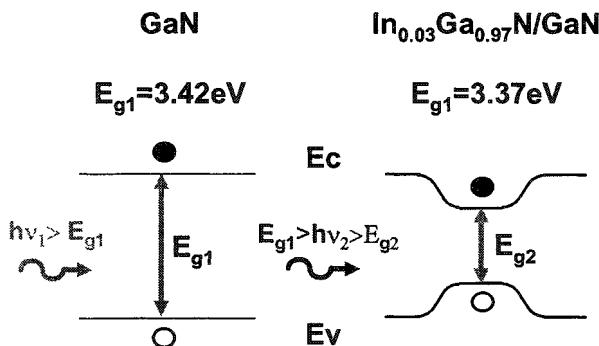


Fig. III.3b. Schematic illumination of selective etching

The higher energy components of the light are absorbed by the GaN filter, and the transmitted light therefore selectively creates electron-hole pairs only in the lower bandgap InGaN (Fig. III.3b). In order to efficiently determine an appropriate PEC etch process, we employed an orthogonal array to quickly determine the etch parameters of greatest influence in producing a smooth lateral etch with high bandgap selectivity. This array is shown in Table 1a & 1b.

Table 1a: 4 parameters with 3 level settings in Orthogonal array.

| | Bias (V) | Power (W) | Concentration (M) | Time (min) |
|---|----------|-----------|-------------------|------------|
| 0 | 2.71 | 170 | 2.2 | 3 |
| 1 | 1.24 | 400 | 8.8 | 3 |
| 2 | 0.62 | 600 | 0.55 | 3 |

Table 1b: Orthogonal Array employed

| Run | Concentration (M) | Bias (V) | Power (W) | Time (min) |
|-----|-------------------|---------------|--------------|------------|
| 1 | 0=2.2 | 0=2.71 | 0=170 | 0=3 |
| 2 | 0=2.2 | 1=1.24 | 2=600 | 1=3 |
| 3 | 0=2.2 | 2=0.62 | 1=400 | 2=3 |
| 4 | 1=8.8 | 0=2.71 | 1=400 | 1=3 |
| 5 | 1=8.8 | 1=1.24 | 0=170 | 2=3 |
| 6 | 1=8.8 | 2=0.62 | 2=600 | 0=3 |
| 7 | 2=0.55 | 0=2.71 | 2=600 | 2=3 |
| 8 | 2=0.55 | 1=1.24 | 1=400 | 0=3 |
| 9 | 2=0.55 | 2=0.62 | 0=170 | 1=3 |

We used our previous experience to highlight the three parameters that we believed would most greatly influence the process: (1) the intensity of illumination of the optical source, (2) the bias voltage applied to the sample during the etch process, and (3) the concentration of the KOH in the etch solution. 3 different values of each of the parameters were used, and were placed within an L₉3⁴ Table²⁷, spanning 4 parameters, each with 3 different values (or level settings), comprising 9 separate experiments. The 4 parameters in this L₉3⁴ Table include the above 3 ones and time. Since the above 3 input parameters are simply more influential on the etching compared with changing time, time can be set as constant simply and conveniently. The values (level settings) for each parameter are chosen to cover the variable range of our PEC etching experiment. The intent is to rapidly assess the most important etch factors through the completion of just 9 different experiments.

The full analysis and results of the orthogonal array experiments will not be reported here. The most dramatic and important result of the experiments was the correlation between KOH concentration and the smoothness of the etched surface. Referring back to Table 1b, experiments 1-3; 4-6; 7-9 have a single concentration of KOH while all other parameters are equally represented among all the experiments. Thus, analyzing data by averaging over experiments with the same value of KOH concentration should allow us to identify whether there is a significant dependence on the KOH concentration alone. The results are demonstrated in Figure III.4: the 0.55M KOH produces a much smoother etched surface than the 2.2M KOH solution.

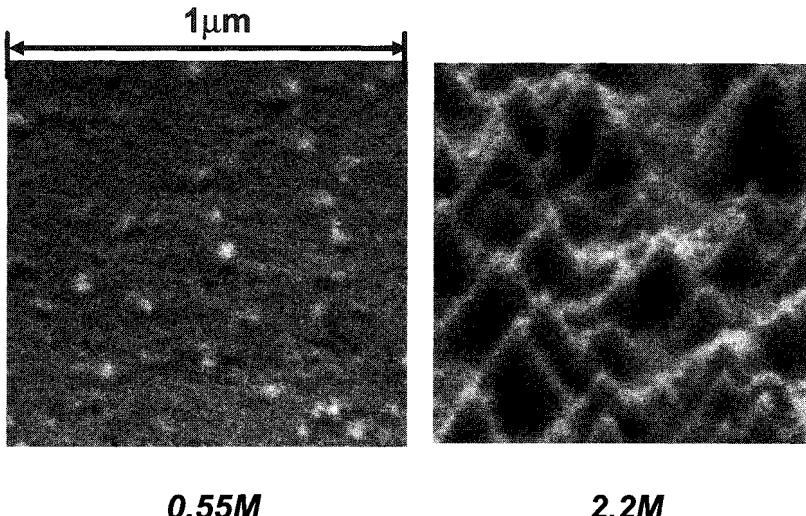


Fig. III.4. SEM images under lower concentration (0.55M KOH) and higher concentration (2.2M KOH). The roughness of the right image is around 100nm.

The correlation between smoothness of the etched surface and low KOH concentration has already been observed in more conventional PEC etching of GaN. For example, Youtsey *et al.* found that PEC etching of n-GaN formed hillocks for KOH concentration $> 0.04\text{M}^{7,28}$, produced whiskers for concentrations between 0.01M and 0.04M²⁴, and yielded a smooth etched surface for KOH concentration $< 0.01\text{M}^{16}$ in their etching conditions. The role of dislocation in PEC etching was demonstrated in Fig. III.5.

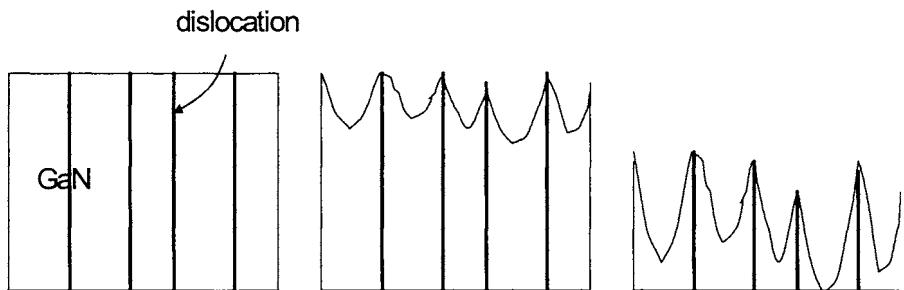


Fig. III.5. Schematic diagram illustrate dislocation role in PEC etching of GaN

Youtsey claimed that the low KOH concentration produced etching in the diffusion-limited regime, where the etch rate is controlled by mass-transport considerations rather than purely chemical etching. We had previously mentioned the effect of threading dislocations in the vertical etching of n type GaN on the morphology of the etched surface. Under conditions that are sensitive to chemical etching, we may observe strong differences in the etch rates of materials near or at the threading dislocations (low etch rates), compared to material more remote from the defects (higher etch rates). The

variation in etch rates would result in a rough surface morphology, and possibly the non-uniform lateral etch front observed in higher concentration. Diffusion-limited etching reduces the differences in etch rate by forming thick oxidation layer, which smooth out the distinction between dislocation etching and good materials (dislocation free) etching — more finely delineating the threading dislocation ‘whiskers’ as Youtsey discussed, and ultimately producing the smoothest etched surfaces. More recent experiments carried out on a-plane, Lateral-Epitaxial Overgrown (LEO) materials shows a crystallographic PEC etch of the N-face of GaN (0001), which also produces a non-planar etched surface. Further experiments were carried out, and very low concentration — 0.004M was chosen as the concentration for smooth, straight undercut for CAVET fabrication. This low concentration can also provide reasonable etch rate and etch selectivity.

B. Uniformity of the Etch and Stirring of the Electrolyte

Etches operating in the diffusion-limited regime are sensitive to conditions that alter the transport of reactants and etch products. Stirring is applied to transport the reactants and etch products more efficiently. Fig. III.6 compares the etching undercut without stirring and with stirring. Without stirring, the connected cones exist between top GaN and bottom GaN. Clean undercut is achieved with stirring. Stirring maintains a constant lateral etch rate by enhancing mass-transport in narrow channels.

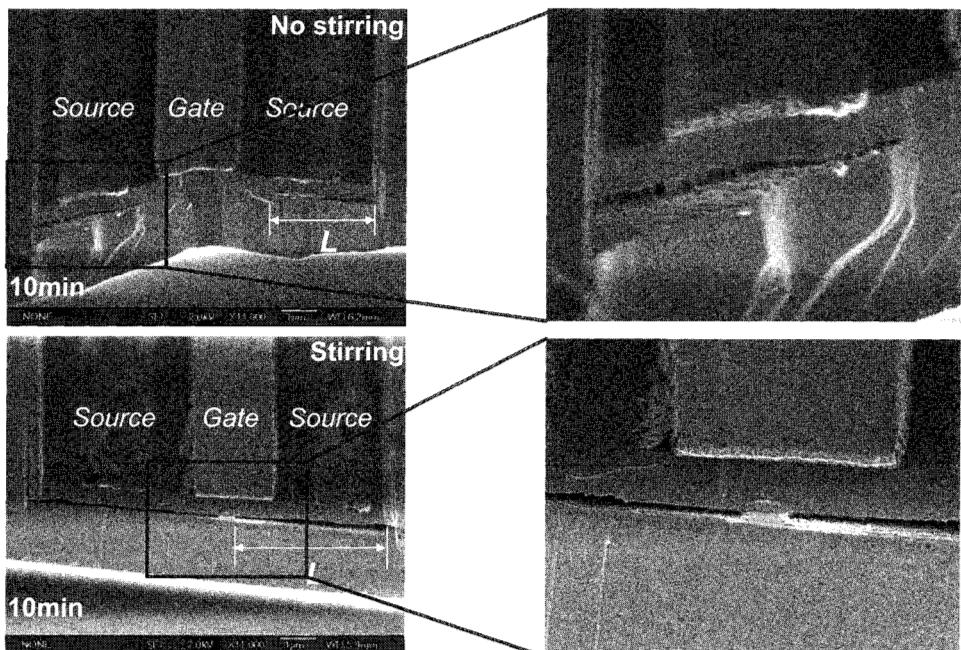


Fig. III.6a. Undercut etching morphology with stirring and without stirring

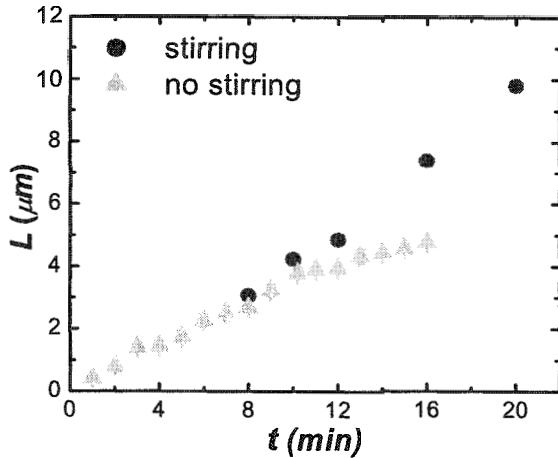


Fig. III.6b. Time dependence of undercut etch depth L with stirring and without stirring

C. Uniformity of Etch Front, and Effect of Illumination Power

Using a greatly reduced KOH concentration (0.004M), we assessed the influence of the incident power on the etch rate. Fig. III.7a gives the SEM image under 1000W, 0.004M, 12min etching condition. L is the etched depth. Fig. III.7b shows the time-dependence of undercut depth examined under lamp powers of 170W, 450W, and 1000W. The error bars in the plot represent the measured undercut depth from 8-10 mesa structures over the entire sample. As shown in Figure III.7b, the lateral etch rate increases in proportion to the lamp power. More importantly, however, the error bars on the data of Figure III.7b reveal that the higher lamp power produces less variation of the undercut distance, which means a straighter undercut edge.

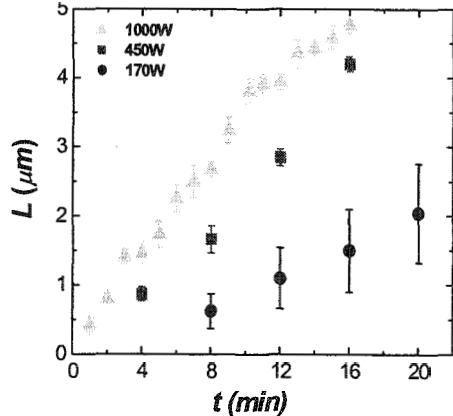
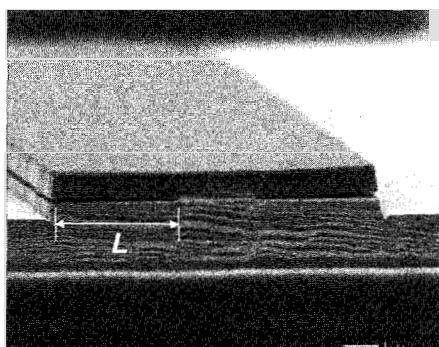


Fig III.7a. SEM under 1000W, 0.004M, 12min etching. L is the etched depth;

Fig III.7b. Time-dependence of undercut depth under different lamp power.

Higher power provides less variation of the undercut depth

IV. Initial Etched CAVET Device

The CAVET structure is shown in Fig I.1. Initially, reactive ion etching in chlorine was used to form a device mesa, etching into the lower GaN layer. This exposed the sides of the $\text{In}_{0.03}\text{Ga}_{0.97}\text{N}$ layer, which will be selectively removed during the PEC etching. Then Ti/Al/Ni/Au (200/1500/375/500Å) was evaporated and annealed at 870°C for 30sec to form source and drain contacts. The source metal contacts the 2DEG near the A1GaN/GaN interface, while the drain metal contacts the bottom Si-doped GaN template. Ni/Au/Pt (300/1000/1000Å) is deposited directly onto the middle of the mesa and serves as the gate. We used 0.004 M KOH and stirring of the etchant was important to achieve smooth, uniform undercut etching. The nominal power provided by the Xe lamp was 1000W, resulting in a fairly rapid undercut etch rate, around 1μm/min. The total power density is ~ 20W/cm², but the power density above the bandgap (measuring the light filtered by GaN template) is ~2W/cm². Following the PEC etch, 3000Å thick SiO₂ was deposited as an insulator around the mesa, covering the sidewalls of the mesa. Ti/Au (200/5000Å) was then deposited as the metal pad on the source, gate and drain regions. The gate length is 2.8μm, gate width is 75 μm, and current aperture is 1 μm wide. The resulting DC I-V curve is shown in Figure IV.1, below²⁹.

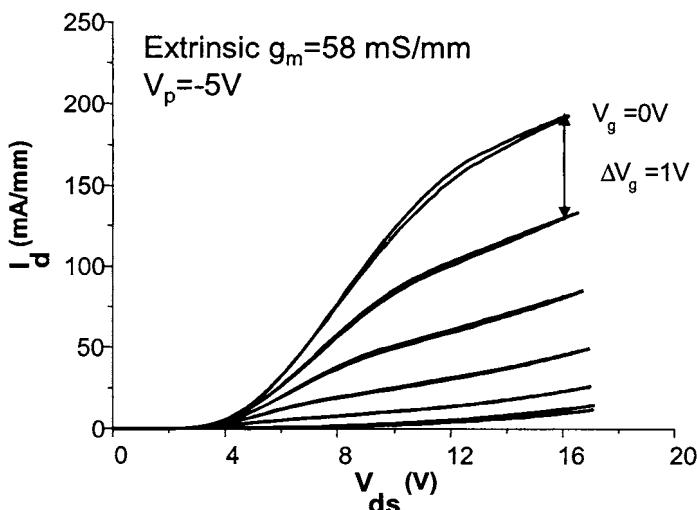


Fig. IV.1. DC I_d - V_{ds} curve of etched aperture CAVET

The I-V shows that the gate controls the flow of the current through the etched aperture. The maximum value of the drain current (I_{dss}) of this device is 190 mA/mm and the extrinsic transconductance (g_m) is ~58mS/mm at $I_{dss} \sim 190\text{mA/mm}$ and $V_{ds} \sim 16\text{V}$. The pinch-off voltage V_p of this device is -5V. All devices display a large offset voltage ranging from 2.5 to 4V, which is not observed in the ‘regrown’ CAVETs. We believe that the offset may originate from an appreciable piezoelectric field present in the strained InGaN layer.

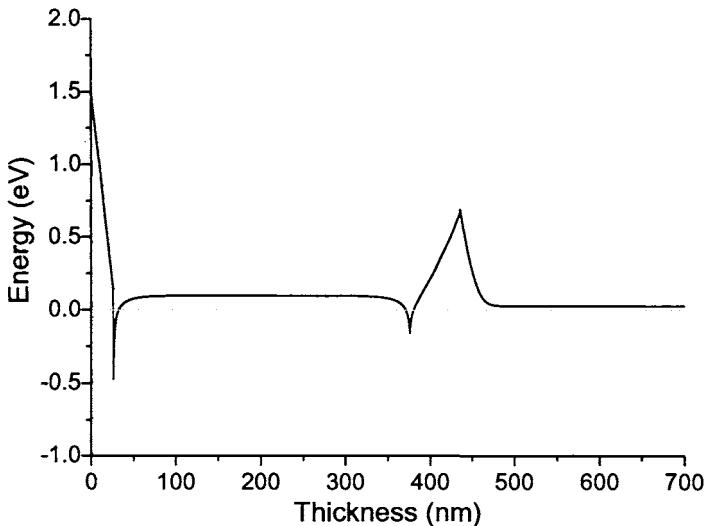


Fig. IV.2. Conduction band diagram of unintentionally doped InGaN

Fig. IV.2 gives the schematic conduction band diagram of the CAVET structure obtained by 1D Poisson Solver. The 600Å $\text{In}_{0.03}\text{Ga}_{0.97}\text{N}$ layer is observed to be fully strained by X-ray spectroscopy. With the high piezoelectric coefficients of the nitrides, the resulting piezoelectric field in the InGaN layer forms a barrier between the InGaN and underlying GaN. This barrier is around 0.7eV for $\text{In}_{0.03}\text{Ga}_{0.97}\text{N}$ layer we used, and forms a large resistance to current flow, resulting in the large offset we observe. Thus, contrary to our original assumptions, the introduction of a thin, 600Å InGaN sacrificial layer did indeed introduce a substantial perturbation to the operation of the CAVET device. The next generation of CAVET design will need to modify the sacrificial layer substantially so that the barrier to electron flow is removed.

V. Second-generation Etched Aperture CAVET

The PEC etch process was shown to be sufficiently optimized to produce a well-controlled, highly selective etch of the InGaN sacrificial layer. In redesigning the CAVET structure, we wish to maintain that quality of that etch process, but alter the device structure to remove the piezoelectrically formed barrier. An immediate possible solution involves the screening of the piezoelectric field by doping the InGaN layer n-type. The simulation of the band diagram that would result from the uniform doping of the InGaN with $1 \times 10^{18} \text{ cm}^{-3}$ Si, is shown in Figure V.1a. Although the electron barrier is not entirely removed, it is substantially reduced (from 0.7eV to 0.3eV). From our earlier experience in the *vertical* PEC etching of the nitride materials, our expectation is that etching of n-InGaN should progress more easily and rapidly than that of the unintentionally doped (uid) InGaN.

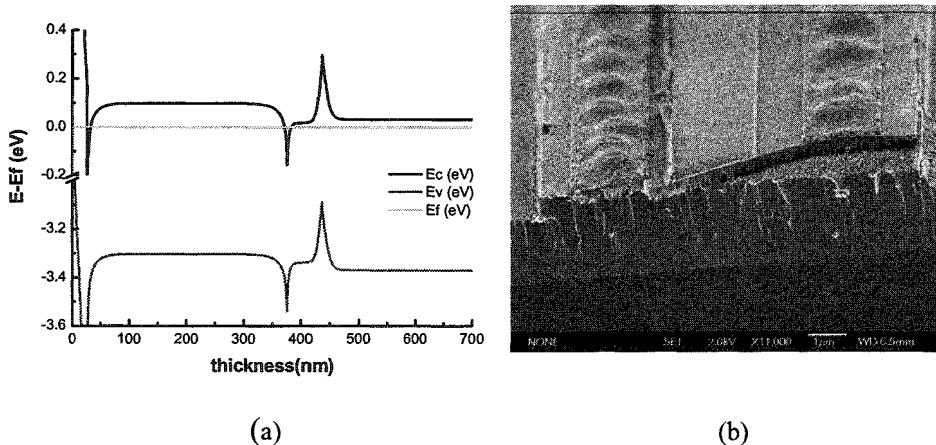


Fig. V.1a. Band diagram of uniformly Si doped InGaN
Fig. V.1b. Etch morphology of uniformly Si doped InGaN

In fact, using the same etch parameters as were previously described for the uid InGaN, the quality of the etch structure is severely degraded, with a loss of surface smoothness and etch selectivity (Figure V.1b). There are some possible reasons for this etching behavior: The faster etching rate of n-type GaN produces the larger difference of etch rate between n-type and dislocation, which enhances the dislocation selectivity and produces worse etching morphology. Secondly, from the valence band in Fig. V.1a, the holes have higher energy in the InGaN than in the top GaN. Once the e-h pairs are generated in the InGaN, holes prefer to move to the top GaN region and contribute to the etching of the top GaN. Thus, we lose the etching selectivity by Si doping InGaN. Si clusters and more induced pits in Si doped InGaN can perhaps affect the etching morphology as well.

In order to minimize the differential etch rate introduced by the doping of the InGaN, and to maintain a reasonable level of hole confinement, we next modified the sacrificial layer by utilizing delta-doping, rather than uniform doping of the InGaN. The first structure placed the δ -doped Si layer at the interface between the InGaN and the lower GaN material to pull down the barrier. Figure V.2b shows that the etching remains unsatisfactory. Etching morphology shows the etching occurs along the InGaN and bottom GaN interface. Since Si etch is very fast in KOH, this may be due to the rapid etch of the delta-doped material in KOH. Figure V.2a also suggests that the modification to the band structure may have resulted in inadequate hole confinement in the InGaN. Better results can be achieved by placing the δ -doped layer slightly removed from the InGaN-GaN interface, within the GaN layer itself. Figure V.3a shows the variation of barrier in the conduction band with varying distance, d , into the GaN. in the model, we have assumed delta Si doping of Si with $1 \times 10^{18} \text{ cm}^{-3}$ within 1 Å. The valence band follows in a similar way to the conduction band. It is apparent that there is a range of values of d for which we can still obtain sufficient hole confinement to drive the etch process, and yet maintain a reduced barrier for electron flow. Figure V.3b shows that

with the incorporation of a delta-doped Si layer 6 nm from the InGaN-GaN interface, within the GaN, a satisfactory PEC etch profile can be obtained.

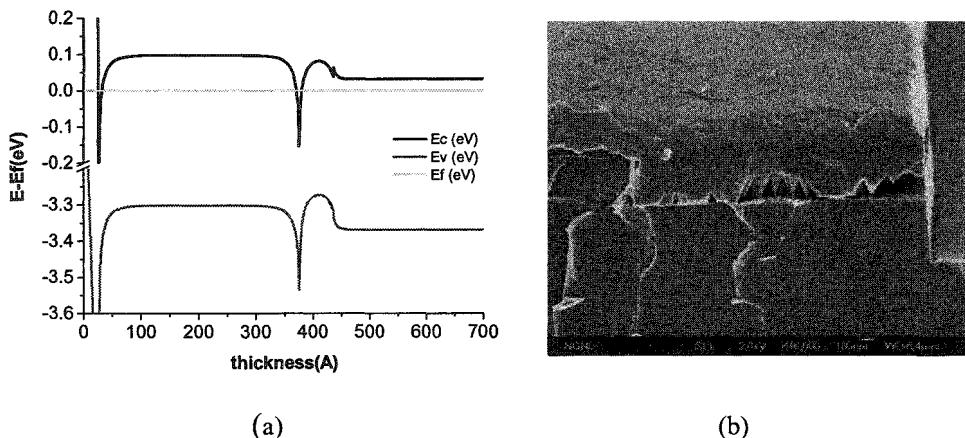


Fig. V.2a. Band diagram of delta Si dope InGaN
Fig. V.2b. Etching morphology of delta Si dope InGaN

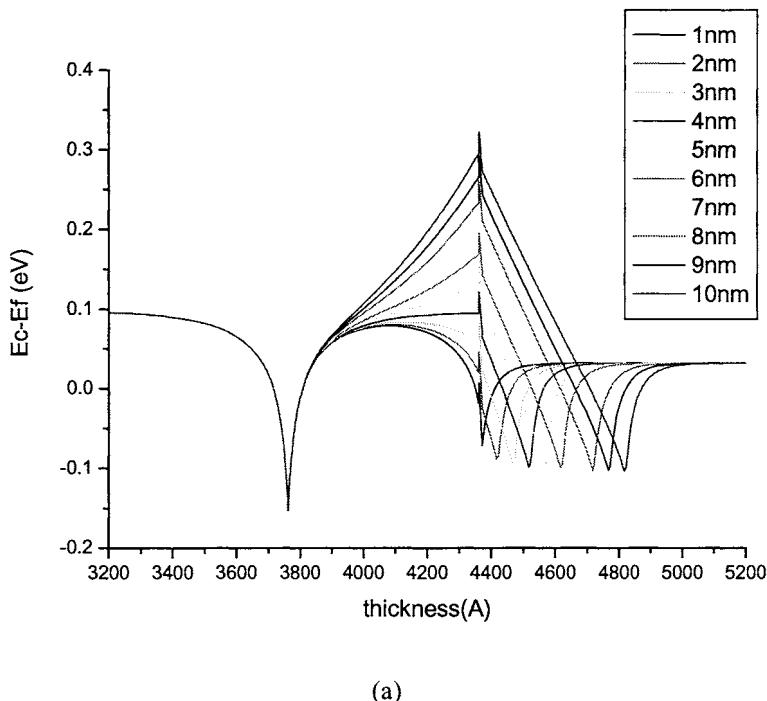
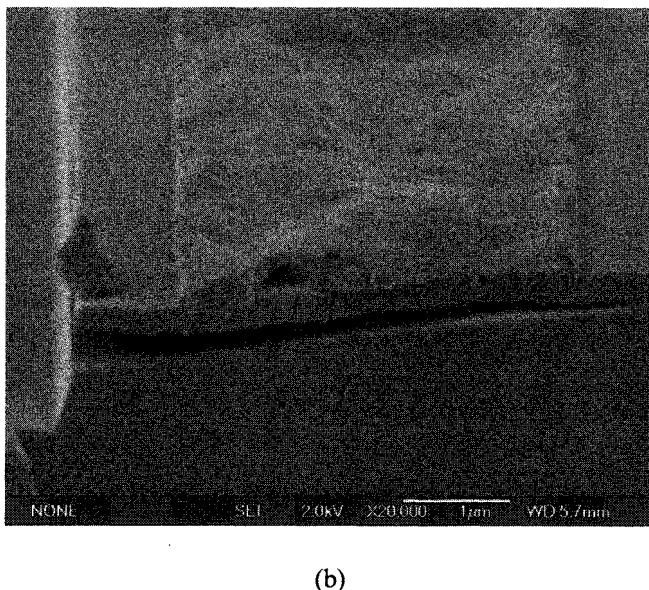


Fig. V.3a. Conduction band and the barrier vs. the delta Si doping position



(b)

Fig. V.3b. Undercut etching with delta Si doping 6nm away from the interface

Utilizing a device structure that incorporates the modified InGaN sacrificial layer with the delta-doped Si layer located 6 nm from the InGaN-GaN interface, we achieve the DC I-V curve shown below (Fig. V.4). There is a clear reduction of the voltage offset, and an increase in the total current delivered by the device. $I_{max} \sim 0.3A/mm$. the $g_m \sim 67mS/mm$.

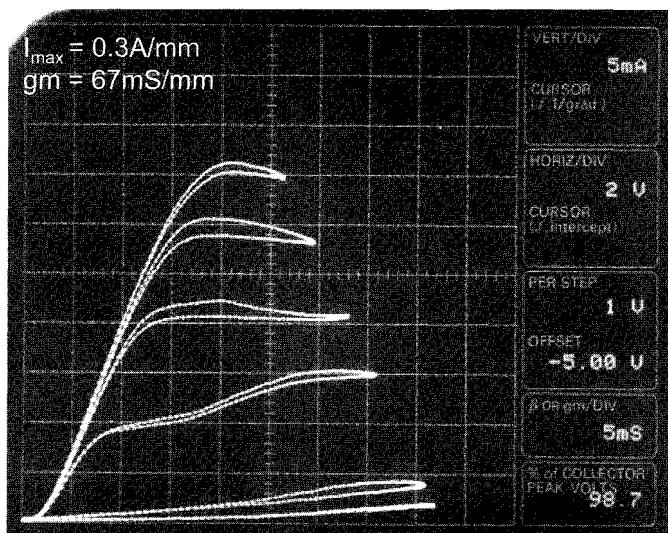


Fig. V.4. DC I-V curve with small voltage offset

VI. Summary and Conclusions

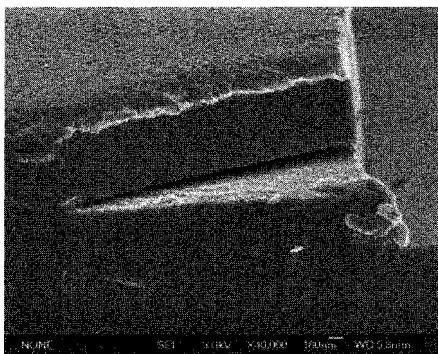
A. Selective, lateral PEC etching

The formation of etched current apertures for the CAVET has exacted important demands on the PEC etch process, and has helped to guide our etch optimization process. As well, the experiments carried out during the optimization have helped to distinguish critical features of the lateral etch process.

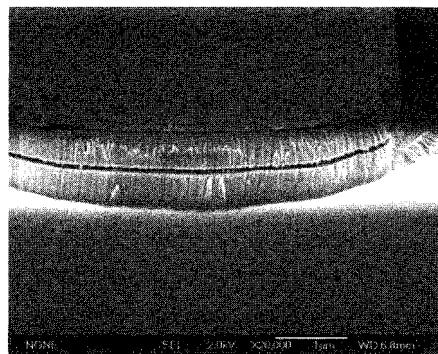
Threading dislocation is very important for the Photoelectrochemical wet etching of GaN compared to other semiconductors. Smooth etching requires lowering the etch rate of the inter-dislocation materials to balance the etching between dislocation regime and good material regime. The schematic diagram in Fig. III.5 illustrates the dislocation role in PEC etching.

Hole confinement is very critical in PEC etching. Small changes in doping and in the location of the delta-doped layer can vary the banddiagram and change the hole confinement, thus influence the quality of the etch.

All the above experiments are done with KOH as the electrolyte. Since the electrolyte type can produce different etching mechanisms and different etching morphologies, other electrolytes were explored during our PEC experiments, including HCL and $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ mixed solution. In both case, GaN/uid InGaN/GaN materials are used. Fig. VI.1a and 1b below show the undercut etching achievable with 0.004M HCL and $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O} = 1:8:100$ mixed solution.



(a) HCl



(b) $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$

Fig. VI.1. Smooth undercut under 0.004M HCl & $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$

B. Etched aperture CAVET structures:

Two generations of etch-aperture CAVETS are fabricated. The design of these materials has required an integrated interplay between process and device optimization. The use of a uid InGaN sacrificial layer produced an unacceptably high electron barrier because of

the unrelaxed strain and the high piezoelectric properties of these materials. A simple matter of doping the sacrificial layer, in order to screen the piezoelectric field, dramatically altered the quality of the PEC etch. Etch optimization required the full understanding of the band diagram and dynamics of the etch process. Removing the barrier in conduction band and keeping enough hole confinement in the valence band are required for a further optimized CAVET.

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n-AlGaAs/p-GaAs/n-GaN HETEROJUNCTION BIPOLAR TRANSISTOR: THE FIRST TRANSISTOR FORMED VIA WAFER FUSION

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We discuss the first reported device characteristics of a wafer-fused heterojunction bipolar transistor (HBT), demonstrating the potential of wafer fusion for the production of electrically active heterostructures between lattice-mismatched materials. n-GaAs/n-GaN (“n-n”) and p-GaAs/n-GaN (“p-n”) heterojunctions were successfully fused and processed into current-voltage (I-V) test structures. The fusion and characterization of these simple structures provided insight for the fabrication of the more complicated HBT structures. Initial HBT devices performed with promising dc common-emitter I-V characteristics and Gummel plots. n-n, p-n, and HBT electrical performance was correlated with systematically varied fusion conditions, and with the quality of the fused interface, given both chemical information provided by secondary ion mass spectroscopy (SIMS) and structural information from high resolution transmission electron microscopy (HRTEM) analysis.

Keywords: Nitrides; nitride heterostructure bipolar transistors; GaAs; GaN.

I. Introduction

The large breakdown field and anticipated saturation velocity of GaN make this novel material particularly promising for high-frequency, high-power devices. With this goal in mind, quite a few researchers are working to develop GaN-based heterojunction bipolar transistors (HBTs).^{1–6} Although results thus far have been promising, there are still a number of outstanding materials issues. For example, AlGaN-GaN HBTs appear to be limited by large acceptor ionization energies and low hole mobilities.¹ We describe the use of wafer fusion to form HBTs with an AlGaAs-GaAs emitter-base and a GaN collector. In this way, we hope to make use of both the high breakdown voltage of the GaN and the high mobility of the technologically more mature GaAs-based materials. Because the high degree of lattice mismatch between GaAs (lattice constant of 5.65 Å) and GaN (3.19 Å) precludes an all-epitaxial formation of this device, we fabricate the GaAs-GaN heterostructure via the novel technique of wafer fusion (also called direct wafer bonding).

Wafer fusion, which joins two materials placed in intimate contact under elevated temperature and pressure, has proven to be effective in forming a number of heterogeneous devices from lattice-mismatched materials. These devices include GaAs-InP vertical-cavity⁷ and microdisk⁸ lasers, InGaAs-Si avalanche photodiodes⁹, and InGaAsP-AlGaAs photonic crystal lasers¹⁰. However, the device demonstrated here places stringent demands on the electronic quality of the fused interface, as it serves also

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as the base-collector junction of an HBT. Uncontrolled bond reconstruction or residual impurities at the fused interface can produce electronic traps, which in turn may produce the low common-emitter current gain observed thus far in these initial devices. Aside from the issue of bond reconstruction at the fused interface, the elevated temperature of the fusion process (500-750°C) may itself accelerate dopant and defect diffusion, degrading the entire material structure. We note that the fusion temperature is often higher than the growth temperature of the AlGaAs-GaAs materials (585°C). Lower fusion temperatures would thus seem to be desirable, but for our device application the fusion conditions (anneal time and temperature) must provide enough thermal energy to form a mechanically stable and electrically active fused interface. (Given the thermal stability of GaN, GaN fusion has been reported at high temperatures, up to 1000°C.¹¹⁻¹⁴) Due to these two competing factors, wafer fusion processes must be studied systematically, in order to achieve proper characterization and optimization. In our studies, fusion conditions (anneal time and temperature) were systematically varied and correlated with the electrical and chemical quality of the resulting interface.

II. Fusion Procedure

We began our studies of the wafer fusion process by examining the quality of simple fused GaAs-GaN structures, and used those data to determine the starting points of the process for the AlGaAs-GaAs-GaN fused HBT. Hence, three wafer-fused device structures were studied initially: (1) the n-GaAs/n-GaN heterojunction, henceforth called the “n-n structure”, (2) the p-GaAs/n-GaN diode, called the “p-n structure”, and (3) the n-AlGaAs/p-GaAs/n-GaN HBT.

Starting materials are depicted in Figure II.1. (Al)GaAs structures were grown by molecular beam epitaxy (MBE) at 585°C in a Varian Gen-II system. In the p-n structure, both carbon and beryllium were investigated independently as potential p-GaAs dopants. In the HBT carbon was chosen, rather than beryllium, in order to minimize dopant diffusion during the high-temperature fusion procedure. GaN structures were grown by metal-organic chemical vapor deposition (MOCVD) on c-plane (0001) sapphire at 1160°C. (Al)GaAs and GaN were cleaved into rectangles (5-10mm), cleaned, rinsed in methanol, joined together in methanol, and annealed (“wafer-fused”) under a uniaxial pressure of 2 MPa in a nitrogen ambient. Structures were fused over a wide range of systematically varied temperatures (500-750°C) and times (0.25-2hours).

Wafer-fused interfaces can be disordered on the scale of several monolayers, often with amorphous layers, probably oxides. By cross-sectional high resolution transmission electron microscopy (HRTEM), it was determined that our GaAs-GaN interface, fused at 550-750°C for 0.25-1hour, consistently exhibits disorder which is limited to 0.5-2nm. A thinner disordered interlayer results from higher fusion temperature (Figure II.2). This compares favorably to other fused materials systems. Shi *et al.* observed an interlayer thickness of 5nm at GaAs-GaAs interfaces fused at 400°C for 1hour.¹⁵ Black and Jin-Phillipp *et al.* observed an interlayer thickness of 6-8nm at GaAs-InP junctions fused at 630°C for <0.5hour.^{16,17} Our GaAs-GaN fused interface was studied via cross-sectional and plan-view TEM. Detailed TEM analysis is published elsewhere.^{18,19}

After fusion the GaAs substrate was removed via wet etching in $H_2O_2:NH_4OH$. This selective etch terminated at the AlAs layer, which was subsequently removed in HF. For the HBT structure, n-AlGaAs emitter mesas ($1 \times 10^{-5} cm^2$) and p-GaAs base mesas ($5 \times 10^{-5} cm^2$) were defined via wet etching in $H_3PO_4:H_2O_2:H_2O$. For the n-n and p-n structures, larger GaAs mesas ($100 \times 100 \mu m^2$) were wet-etched. n-GaAs contacts were AuGeNi annealed at $415^\circ C$, p-GaAs contacts were ZnAu, and n-GaN contacts were unannealed AlAu.

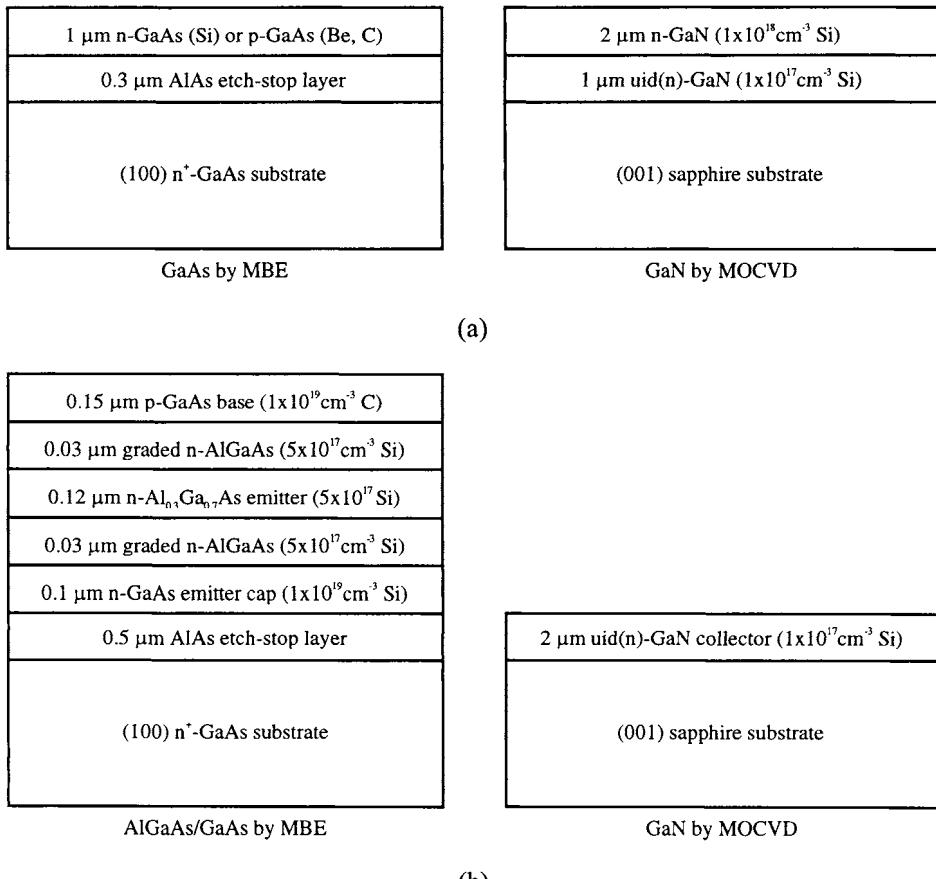


Fig. II.1. Starting materials for the wafer fusion of (a) the “n-n” and “p-n” GaAs/GaN structures and (b) the n-AlGaAs/p-GaAs/n-GaN HBT. In the formation of all three structures, the GaAs and GaN top surfaces are fused together, and then the GaAs substrate and AlAs etch-stop layer are sequentially removed. In figure (a), n-GaAs doping is $1 \times 10^{18} cm^{-3}$ Si and p-GaAs doping is $5 \times 10^{18} cm^{-3}$ Be or C.

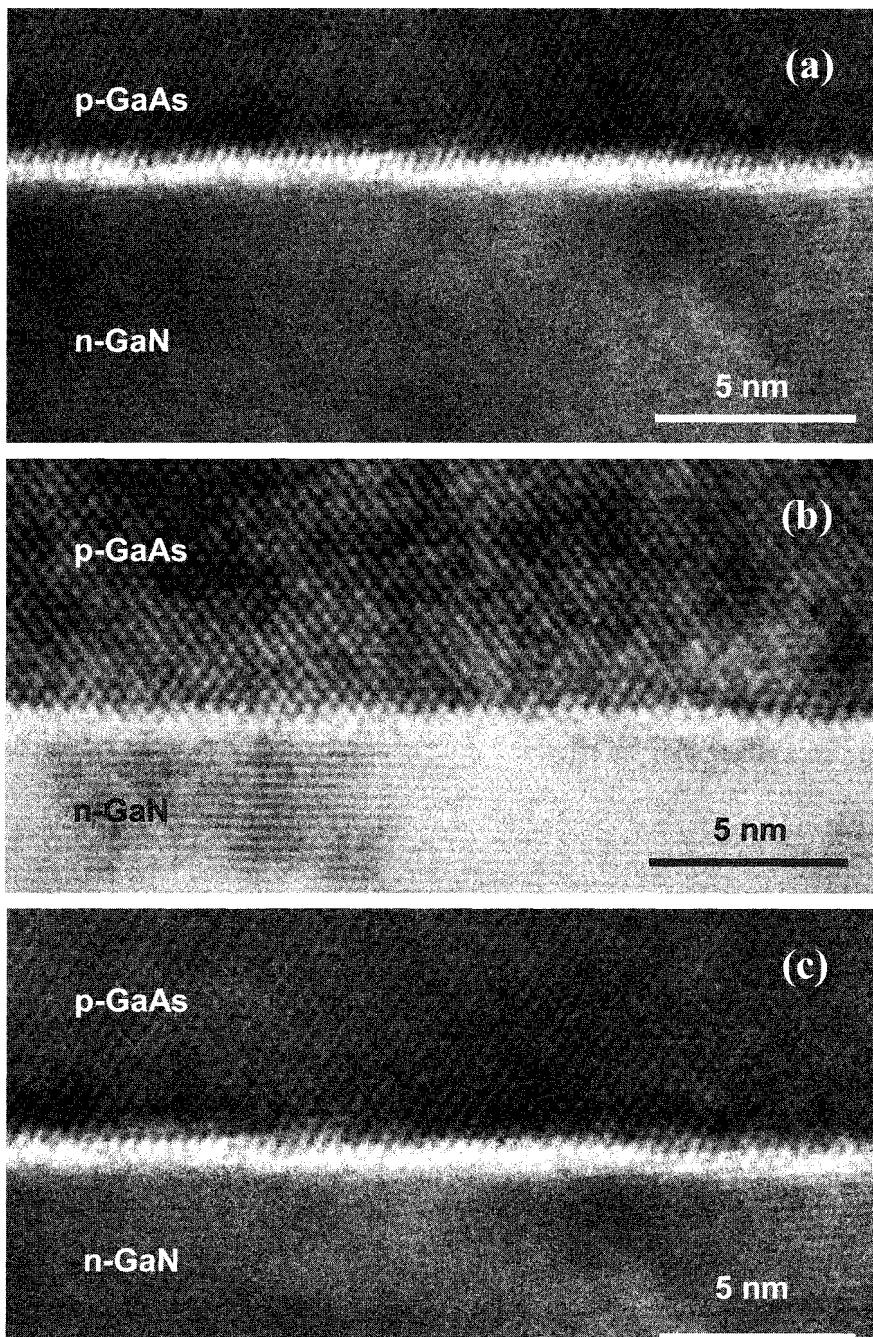


Fig. II.2. HRTEM of the GaAs-GaN interface wafer-fused (a) at 750°C for 0.25hr, (b) at 750°C for 1hr, and (c) at 550°C for 1hr. These images of our samples are courtesy of J. Jasinski and Z. Liliental-Weber, LBNL.

III. The “n-n” and “p-n” GaAs-GaN Fused Junctions

We demonstrate the successful wafer fusion of n-GaAs/n-GaN and p-GaAs/n-GaN heterojunctions, achieved over a wide range of process conditions (500–750°C, 0.25–2hr). Two principal characterization methods were used to assess the quality of the fused junctions: (1) electrical, or I-V characteristics, and (2) secondary ion mass spectroscopy (SIMS) analysis of the chemical composition. I-V characteristics alone suggest that elevated process times or temperatures are more optimal fusion conditions. However, SIMS data reveal substantial inter-diffusion of dopants and contaminants, especially with elevated process times and temperatures. The details of the characterization are described below.

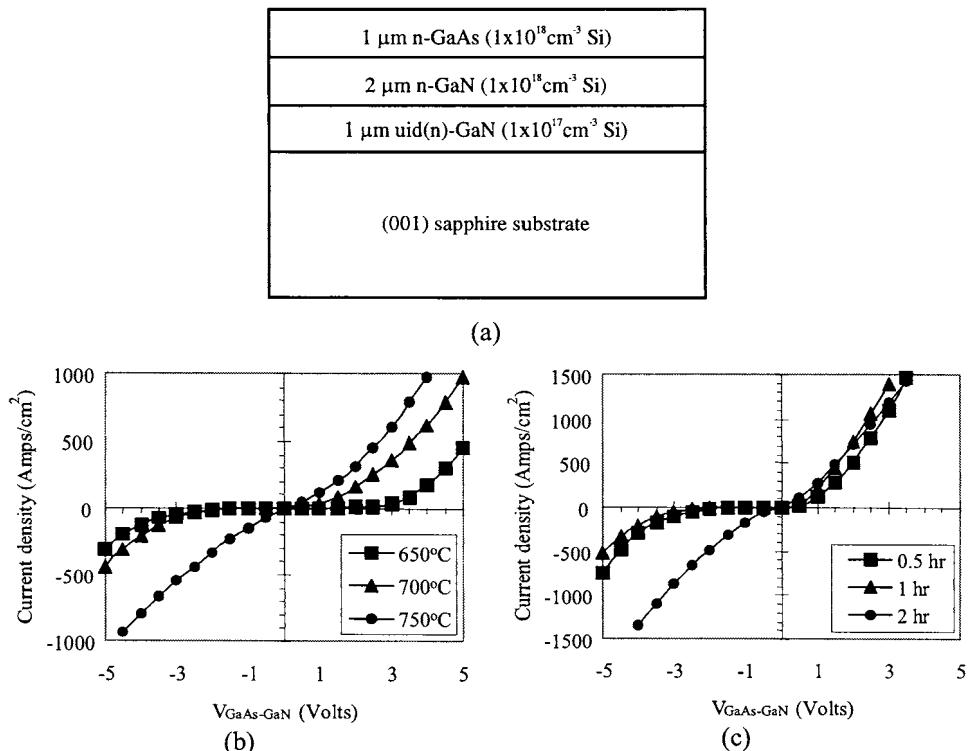


Fig. III.1. (a) The “n-n” structure and I-V data for various samples of this same structure: (b) all fused for two hours but each fused at a different temperature (650–750°C), and (c) all fused at 750°C but each fused for a different duration (0.5–2hr).

III.A. Electrical analysis of n-n and p-n fused junctions

Figure III.1.b displays I-V data for various samples of the same n-n structure (Figure III.1.a), all fused for 2 hours but each fused at a different temperature (650–

750°C). I-V curves become more linear and less resistive with elevation in process temperature. Data for the same n-n structure fused at shorter times, but over the same range of temperatures, demonstrate the same trend. Figure III.1.c reveals that a similar trend results from various samples of the same n-n structure, all fused at 750°C but each fused for a different time (0.5-2hr); I-V curves become more linear and less resistive with elevation in process time.

Figure III.2 displays a subset of I-V data for various p-n samples, all fused for 1 hour but each fused at a different temperature (650-750°C). Two different p-GaAs dopants were investigated: beryllium (Figure III.2.a) and carbon (Figure III.2.b). In reverse bias, leakage current varies with voltage. In forward bias, turn-on threshold is low. At higher fusion temperatures, diodes demonstrate softer breakdown in reverse bias, higher turn-on in forward bias, and lower ideality factors (closer to 1). Data for the same Be-doped structure fused at longer times, but over the same range of temperatures, display the same trend. Compared to the Be-doped structure, the C-doped structure exhibits more uniform turn-on and lower resistance in forward bias.

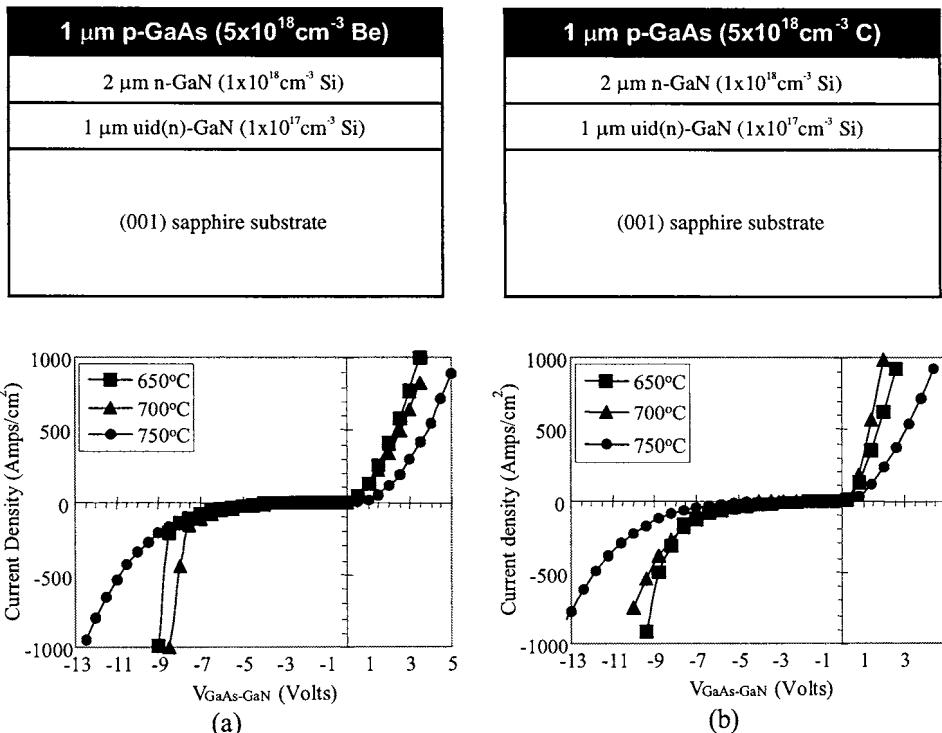


Fig. III.2. Materials structures and I-V data for various “p-n” samples all fused for one hour but each fused at a different temperature (650-750°C). The two p-n structures are the same, except for the two different p-GaAs dopants: (a) beryllium and (b) carbon.

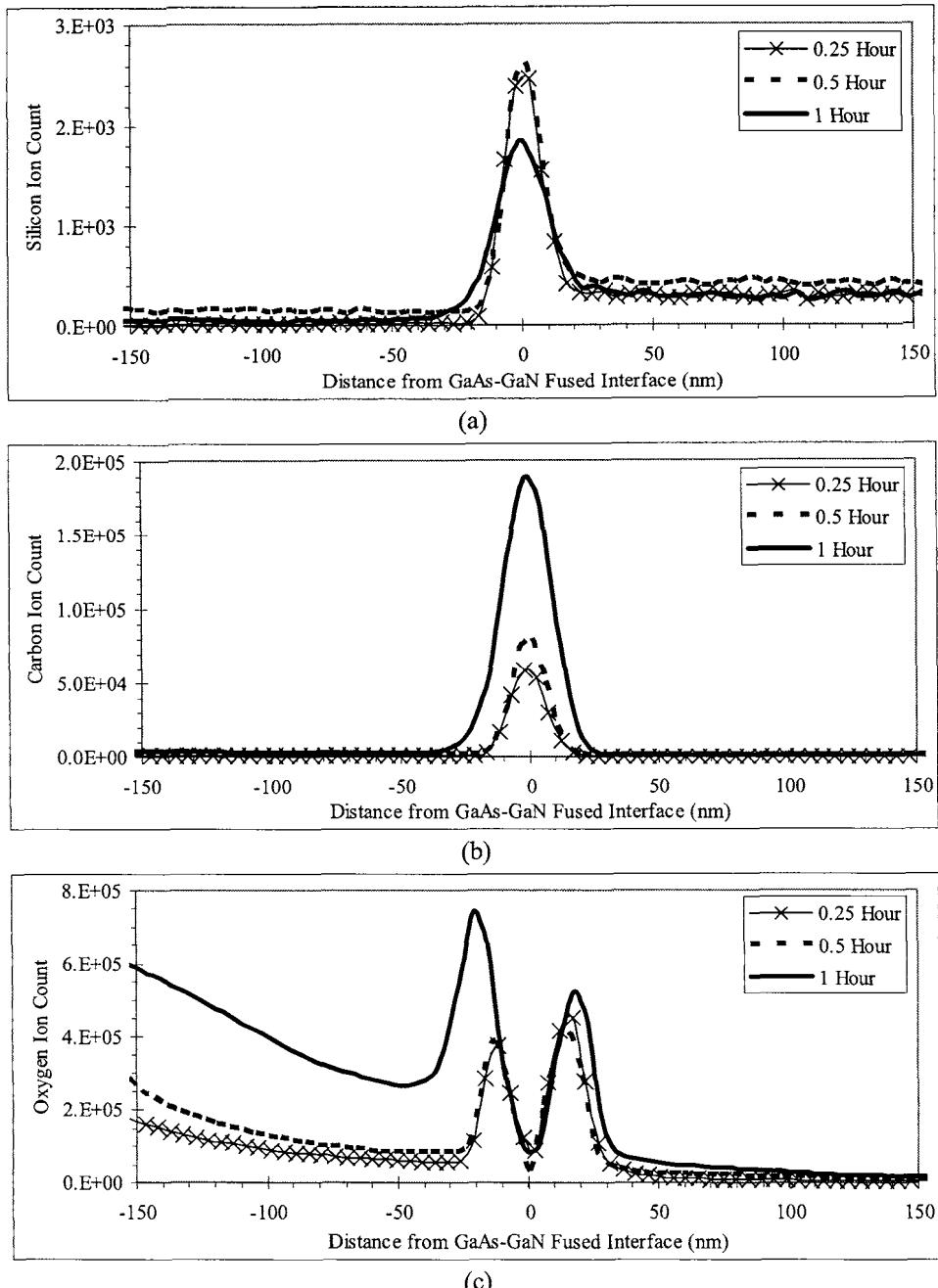


Figure III.3. SIMS profiles in various samples of the same C-doped p-n structure, all fused at 550°C but each fused for a different duration (0.25-1hr). Profiles are shown for (a) silicon, (b) carbon, and (c) oxygen.

III.B. Chemical analysis of n-n and p-n fused junctions

SIMS was used to profile dopants and impurities from the GaAs layer, through the fused interface, into the GaN layer. As with the electrical data, comparisons were made among the systematically varied fusion conditions (time, temperature) and the different p-GaAs dopants (Be, C).

SIMS data consistently reveal high dopant signals (Si, Be, and C) at the fused interface (Figure III.3.a). The highest Si and Be concentrations occur for the reduced fusion times or temperatures. With increased time or temperature, the peak concentration diminishes in height and broadens into the surrounding materials, diffusing more extensively into the GaAs than into the GaN. It has been previously noted that a disordered interface acts as a gettering site for dopants and impurities, especially with strain due to thermal expansion mismatch.²⁰ The data suggest that dopants readily diffuse to the GaAs-GaN interface early in the bonding process; with continued thermal treatment, the high concentration at the interface encourages redistribution of the dopants into the surrounding materials. As expected, more diffusion occurs in Be-doped p-n structures than in C-doped p-n structures, as verified by SIMS data for the two different p-n structures fused at the same temperature and time.

Regardless of fusion condition, SIMS data also reveal strong contaminant signals (oxygen and carbon) at the fused interface, as shown in Figures III.3.b and c. As with the dopants, O and C also display interface signals which broaden with increasing fusion time or temperature. Although C and O may originate from residual surface impurities on the GaAs and GaN starting materials (prior to intimate contact and fusion), an increase of these signals with elevated fusion time or temperature suggests that O and C may also emerge as they diffuse from deep in the bulk starting materials. As C serves as a p-type dopant, this aggravates the issues of dopant compensation and alteration of the device energy band structure. The O signal consistently reveals a double-peak at the interface. The nature of the double-peak is unknown.

IV. The n-AlGaAs/p-GaAs/n-GaN HBT

The data of Section III describe the importance of understanding the effect of the process parameters on the electrical properties and chemical composition of the fused interface. Subsequently we explored a similar systematic variation of the fusion temperature in forming the GaAs-GaN base-collector junction of the HBT. This study reveals the important correlation between fusion temperature, base-collector leakage, and emitter-base degradation. Fusion temperatures as low as 550°C can be used to produce HBTs with mechanically stable and electrically active fused interfaces. In fact, the device characteristics of the HBT *improve* with reduced fusion temperature. With reduced fusion temperatures, devices demonstrate improvements in leakage, output current, and common-emitter current gain. Optimization of the initial device structure (Figure IV.1) should further improve performance.

IV.A. Systematic variation of the HBT fusion temperature

Since the characteristics of the n-p-n HBT must depend on the behavior of the two constituent back-to-back diodes, we first examine the current-voltage (I-V) characteristics of the base-collector and emitter-base junctions independently (Figure IV.2). Figure IV.2.a shows the I-V characteristics of base-collector diodes fused at 550-750°C. (These measurements were taken with the emitter open.) The base-collector leakage current increases with elevated fusion temperature, ranging from 4×10^{-5} mA for $T_f=550^\circ\text{C}$, to 20mA for $T_f=750^\circ\text{C}$. Additionally, the ideality factor n increases with increasing fusion temperature T_f , from $n=2.3-2.9$ at $T_f=550-700^\circ\text{C}$, to $n=5.9$ at $T_f=750^\circ\text{C}$. It may appear that the wafer fusion produces a high value of n ; we note that epitaxially grown GaN p-n junctions have also been reported with high ideality factors ($n \sim 1.5-9.0$).^{21,22}

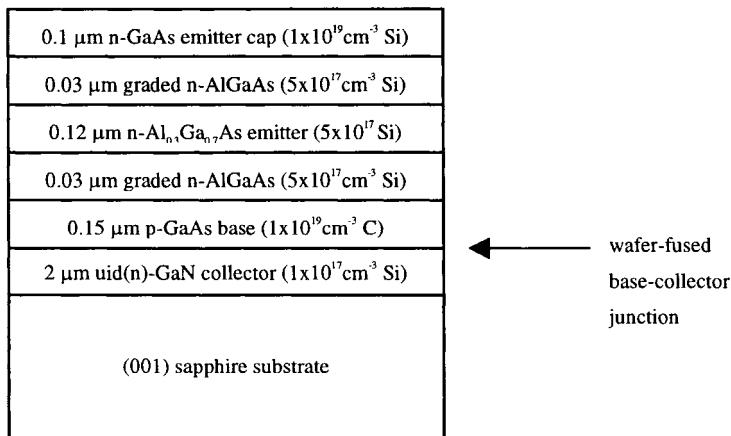


Figure IV.1. Initial materials structure of the n-AlGaAs/p-GaAs/n-GaN HBT, in which the GaAs-GaN base-collector junction is formed via wafer fusion at 550-750°C for one hour.

The AlGaAs-GaAs emitter-base junction is formed directly through MBE growth, but it is important to assess the diffusion effects of the fusion conditions on the quality of that junction (i.e. the elevated fusion temperature for one hour). All emitter-base I-V characteristics (collector-open) are nearly identical to those of the as-grown sample, except for the emitter-base diode subjected to the highest fusion temperature 750°C, yielding a lower current at a given voltage. A subset of these data is displayed in Figure IV.2.b. All emitter-base diodes (including the diode of the 750°C sample) exhibit an ideality factor of 1.2-1.5, similar turn-on, low reverse-bias leakage current, and similar breakdown.

It is interesting to study the emitter-base diode further. Figure IV.2.c shows the I-V data of the as-grown (unannealed) diode, as well as that of a diode capped and annealed at 750°C for one hour. The two I-Vs appear to be identical, suggesting that the elevated temperature alone has a negligible effect on diode characteristics. However, the I-V does

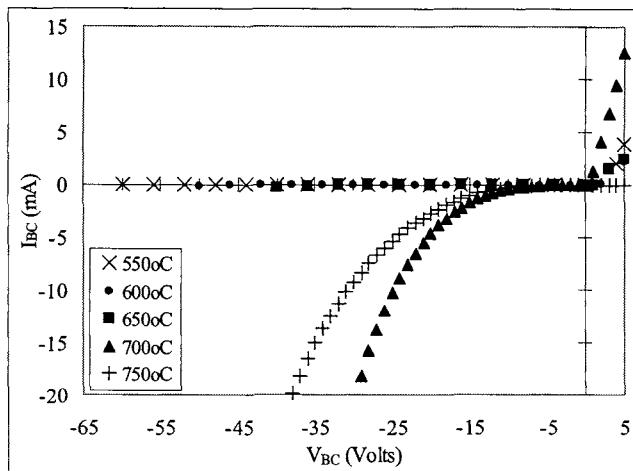


Figure IV.2.a. I-V characteristics (emitter-open) of base-collector diodes in HBT structures wafer-fused at 550-750°C for one hour.

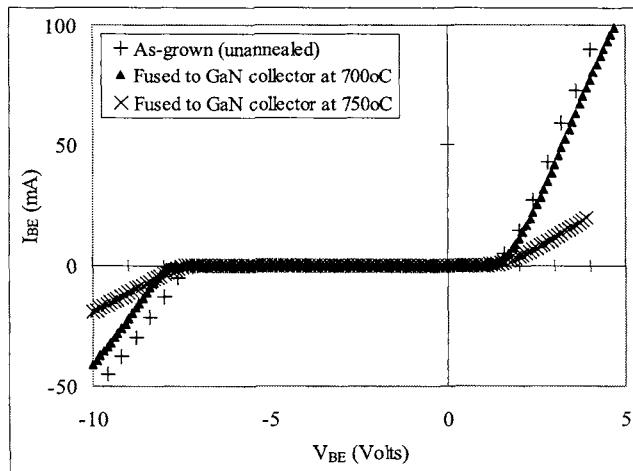


Figure IV.2.b. I-V characteristics of the as-grown emitter-base diode (prior to fusion), and of the base-emitter diodes (collector-open) in HBT structures wafer-fused at 700°C and 750°C for one hour.

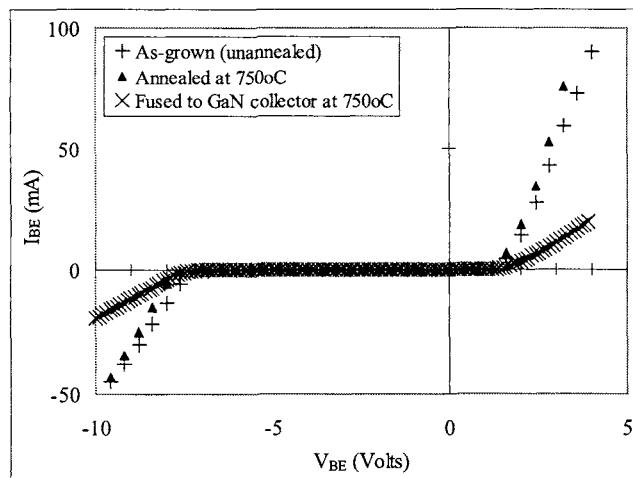


Figure IV.2.c. I-V characteristics of the MBE-grown emitter-base diode subjected to three different thermal processes: (1) as-grown (unannealed), (2) capped and annealed at 750°C for one hour, and (3) wafer-fused to an n-GaN collector at 750°C for one hour.

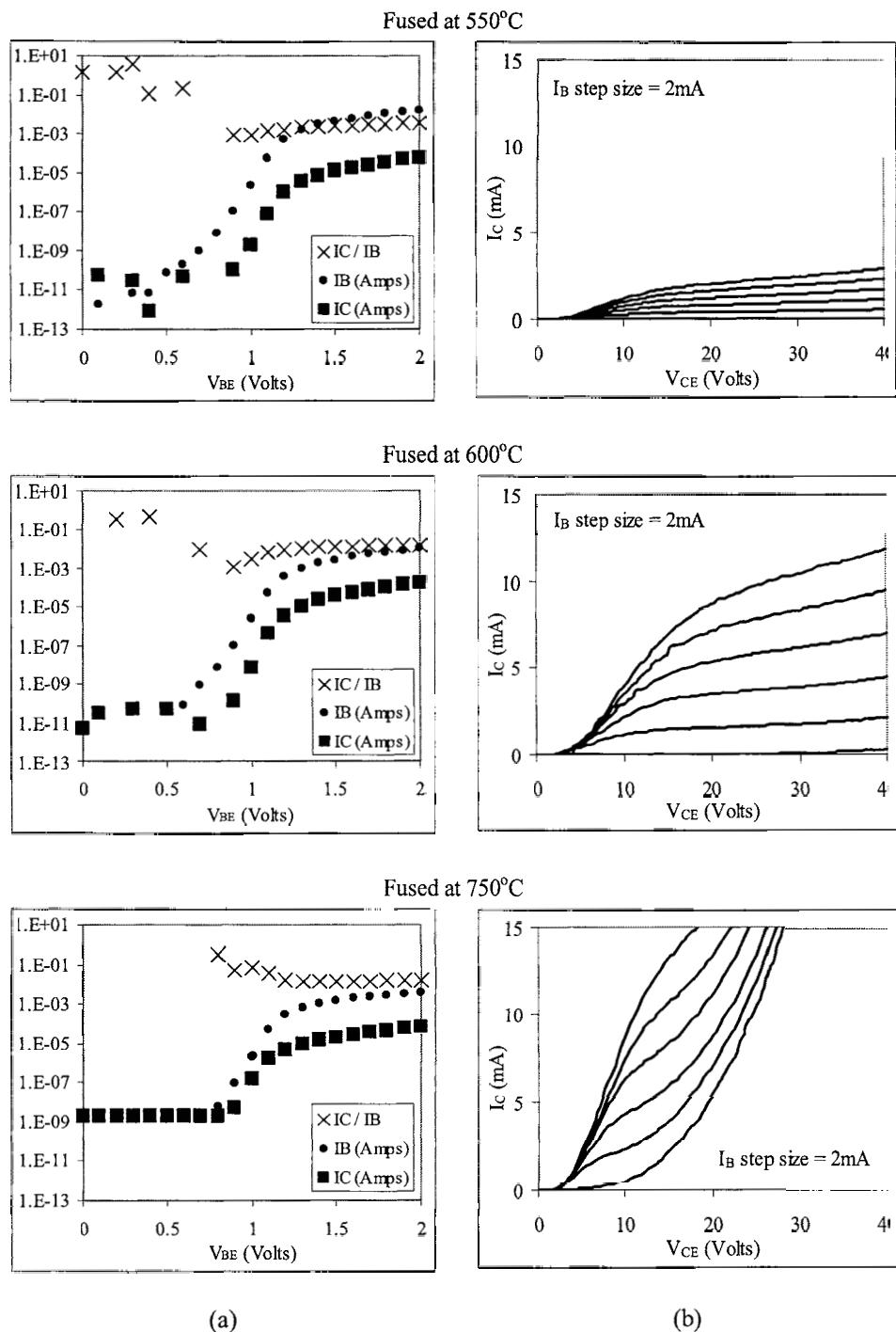
appear to degrade for a diode fused to GaN under those same annealing conditions (750°C for one hour). This same behavior was seen in studies of GaAs-InP wafer-fused interfaces; disorder at the fused interface can produce enhanced diffusion of defects and dopants under elevated temperature.²³ Vacancies or other defects may originate at the disordered fused interface, then diffuse away from the fused interface during the fusion anneal, degrading the surrounding materials such as the nearby emitter-base junction. Figure IV.2.b suggests that reduced fusion temperatures mitigate this diffusion effect.

Gummel plots and common-emitter characteristics were measured for HBTs fused at 550, 600, 650, 700, and 750°C. A subset of this data is shown in Figure IV.3. Gummel plots indicate that the base current (I_B) is reasonably high for fusion temperatures (T_f) of 550–700°C ($I_B=10\text{--}15\text{ mA}$ at $V_{BE}=2\text{ V}$), but I_B is much lower for the highest T_f of 750°C ($I_B=4\text{ mA}$ at $V_{BE}=2\text{ V}$). This reduction in base current is to be expected, given the emitter-base degradation in the HBT fused at 750°C (Figures IV.2.b and IV.2.c). Common-emitter I-V curves are dominated by base-collector leakage for HBTs fused at 700–750°C, but are well-behaved for the lower T_f of 550–650°C. Current gain increases with increasing T_f , but consistently remains low. Common-emitter current gain (β) increases from $\beta=0.29$ for $T_f=550^\circ\text{C}$, to $\beta=1.2$ for $T_f=600^\circ\text{C}$. The gain is undetermined for HBTs fused at 700–750°C, as these devices are dominated by base-collector leakage. It is important to recognize that the observed collector currents are not due to emitter-collector leakage currents,²⁴ which remain at least an order of magnitude lower than the base and collector currents given high enough voltage ($V \sim V_{E-B\text{ turn-on}}$). It is interesting to note that the emitter-collector leakage current increases with increasing T_f , as does the base-collector leakage current.

The current gain (β) is consistently low, and it is important to understand the major limitations of β . Under the conditions that the emitter injection coefficient is nearly ideal (~ 1), β would have the following dependence:

$$\beta = 2D_{nB}\tau_{nB}/W_B^2$$

where D_{nB} is the minority carrier (electron) diffusivity constant in the base, τ_{nB} is the minority carrier lifetime in the base, and W_B is the width of the base (0.15 μm). Since the emitter-base junction is an MBE-grown AlGaAs-GaAs heterostructure, we would expect to exhibit values of β comparable to those demonstrated in AlGaAs-GaAs HBTs ($\beta \sim 20\text{--}100$ for similar emitter-base structures and device sizes^{25,26}). However, our work with simple n-n and p-n GaAs-GaN structures has shown that wafer fusion at elevated temperatures promotes the diffusion of dopants across interfaces (Section III.B). This “cross-diffusion” could in turn reduce both τ_{nB} and D_{nB} , leading to a reduced value of β . Lower temperatures would mitigate such diffusion effects, which is consistent with the improvement of HBT characteristics at lower fusion temperatures. In addition, uncontrolled bond reconstruction or residual impurities at the fused interface may produce electronic traps, which could also limit β . Moreover, the true GaAs-GaN conduction band gap offset is unknown. It may be that the GaAs-GaN heterojunction (regardless of any fusion-induced conduction band barriers) has a natural barrier or spike in the conduction band, which could lead to a substantial reduction in collector current and hence current gain. Optimization of the HBT materials structure should limit the effect of such a spike in the conduction band, and thereby improve device performance.



(a)

(b)

Figure IV.3. I-V data of HBT structures wafer-fused at 550, 600, and 750°C for one hour: (a) Gummel plots and (b) common-emitter characteristics.

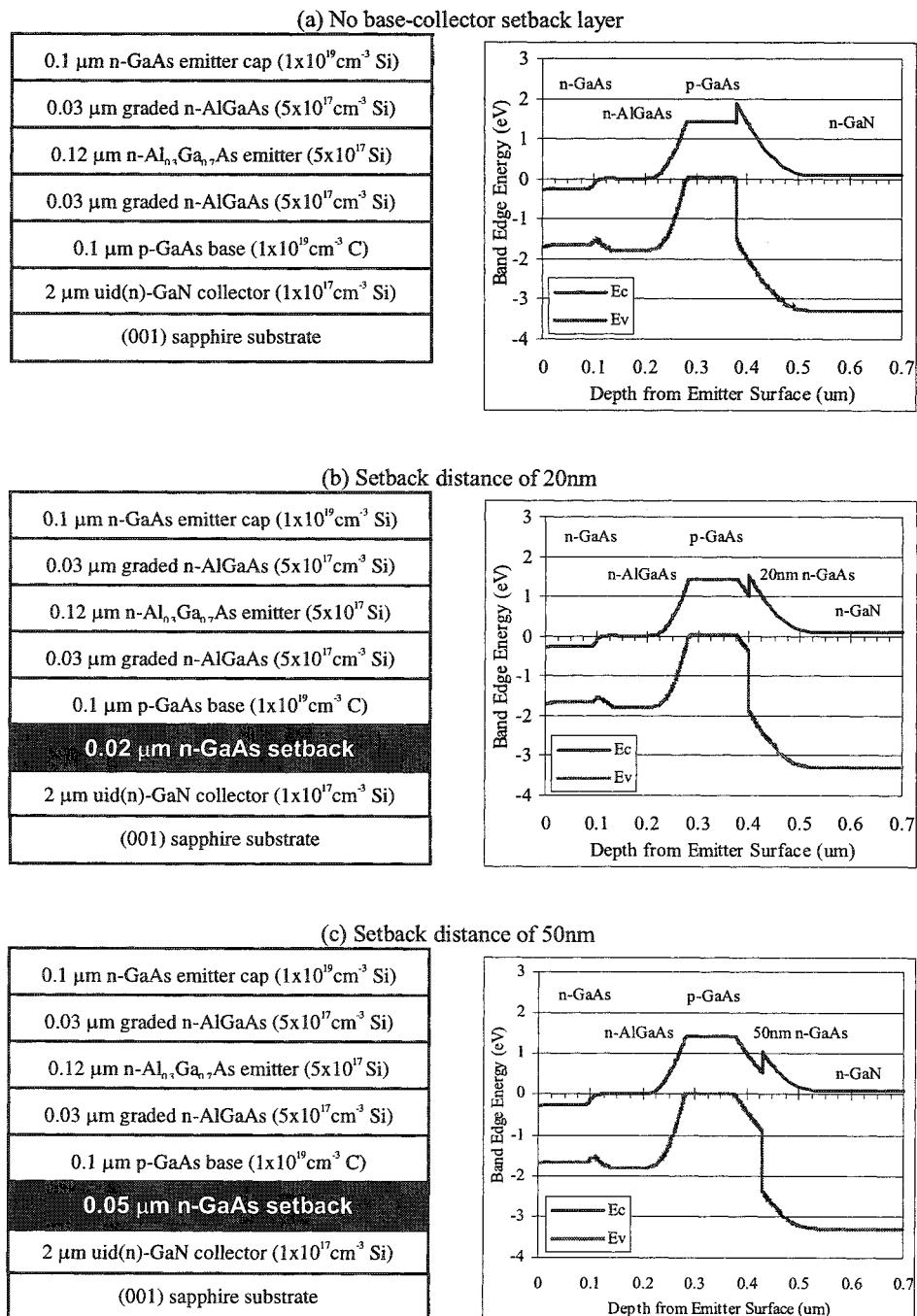


Figure IV.4. Materials structures and simulated energy band diagrams of HBTs (a) without an n-GaAs base-collector setback layer, and with such a setback layer of thickness (b) 20nm and (c) 50nm. Doping of the setback layer is $1 \times 10^{17} \text{ cm}^{-3}$ Si.

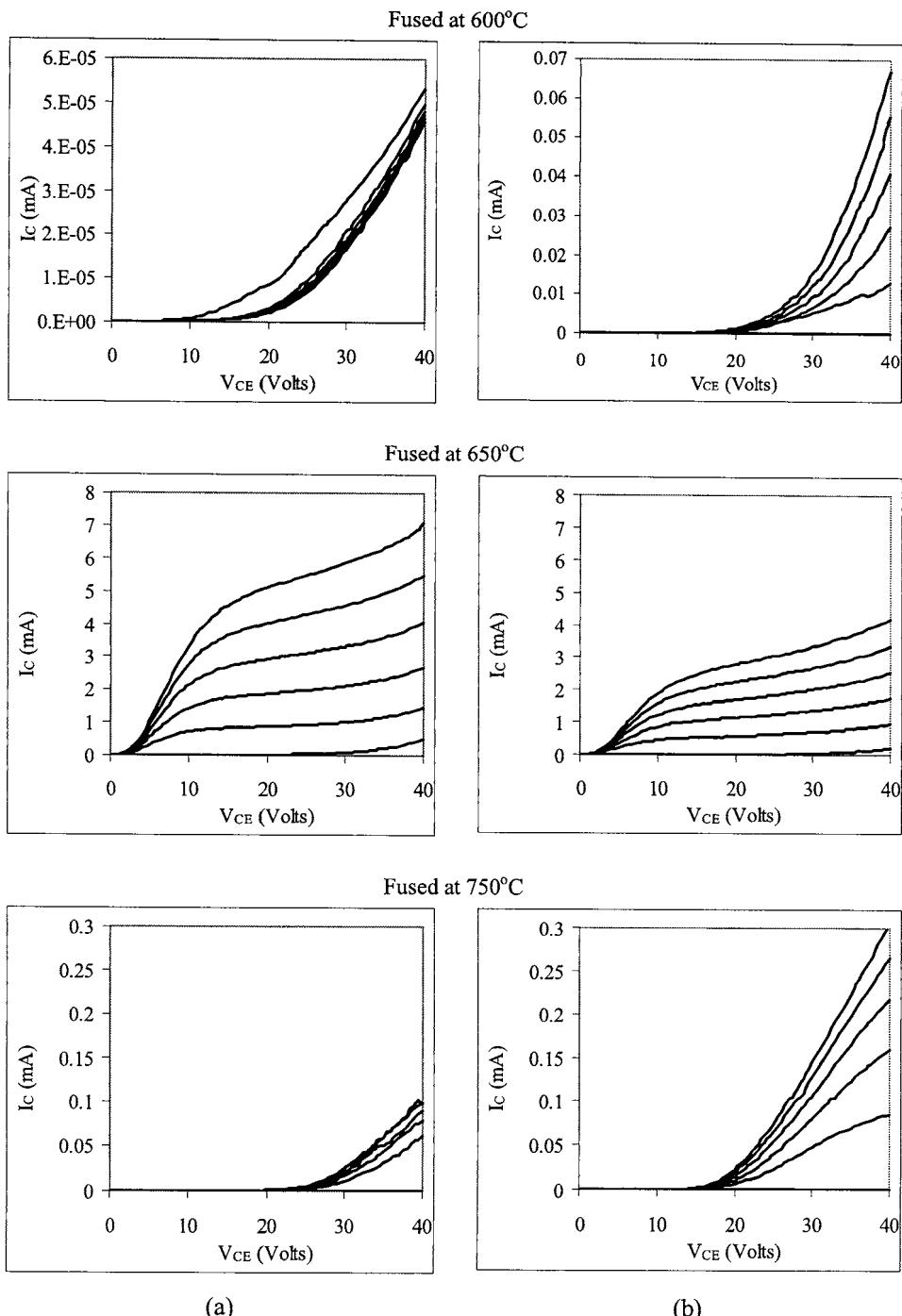


Figure IV.5. Common-emitter I-V characteristics of HBTs fused at 600, 650, and 750°C, with an n-GaAs base-collector setback distance of (a) 20nm and (b) 50nm. I_B step size = 2mA.

IV.B. HBTs with an n-GaAs base-collector setback layer

The conduction band offset (ΔE_C) of the wafer-fused GaAs-GaN heterojunction is unknown. However, a positive ΔE_C is likely, given the observed HBT electrical characteristics (Section IV.A). Assuming a ΔE_C of +0.5eV, we can simulate the energy band diagrams of various new HBT materials structures, then fabricate the device structures that would best counteract a positive ΔE_C . By decreasing the barrier in the conduction band at the base-collector junction, these potential new device structures may increase collector current and hence current gain.

Figure IV.4 shows the materials structures and the simulated energy band diagrams, for HBTs with and without an n-GaAs base-collector setback layer. A setback layer could shift the fused GaAs-GaN interface slightly into the collector, decreasing the barrier prior to the conduction band spike at the fused junction, potentially increasing collector current and hence current gain. For this study, we fused HBTs at 600–750°C, with n-GaAs setback layers of two different widths, 20 and 50nm. Also, a thinner base (100 rather than 150nm) was implemented.

Common-emitter I-V characteristics are shown in Figure IV.5. As with the simple HBT devices (without a setback layer, Section IV.A), a mid-range fusion temperature (600–650°C) results in the most promising I-V data. The I-V of the thicker setback layer (50nm) is worse than that of the thinner setback layer (20nm), and both setback HBT structures produce I-Vs which are worse than the simple HBT structure (without setback, Figure IV.3.b). Because dopant diffusion is certainly occurring in these structures at the high fusion temperatures, and because the diffusivity of Si is higher in GaAs than in GaN, it is likely that the addition of an n-GaAs setback layer is providing both an additional Si source and an additional medium through which the Si can diffuse toward the fused interface (which can act as a gettering site, per section III.B). Figure IV.6 illustrates that an increased Si concentration at the fused interface can substantially alter the simulated energy band structure, and likely decrease the HBT collector current. Thus, future HBT materials structures should address the issue of dopant diffusion, as well as the issue of a likely conduction band spike at the fused interface.

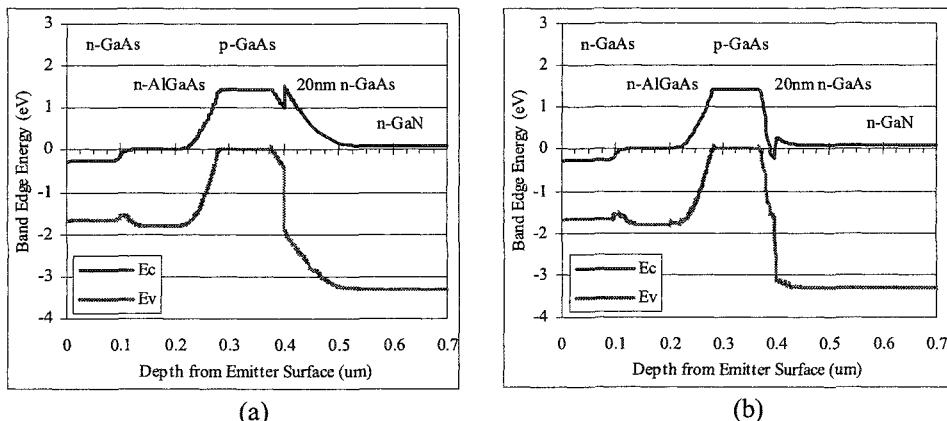


Figure IV.6. Simulated energy band diagrams of HBTs with a 20nm n-GaAs base-collector setback layer (a) assuming no Si diffusion during the fusion anneal at 600–750°C, and (b) assuming aggregation of active Si dopants at the fused interface.

IV.C. Further optimization of the HBT materials structure

Simulated energy band diagrams suggest potential improvements for the HBT materials structure. Possibilities include the addition of a Si δ-doped layer at the collector side of the fused junction (Figure IV.7), the use of a p-GaAs (rather than n-GaAs) base-collector setback layer (Figure IV.8), and the use of a higher band-gap setback material such as AlGaAs (Figure IV.9). By decreasing the barrier in the conduction band at the base-collector junction, these potential new device structures may increase collector current and hence current gain.

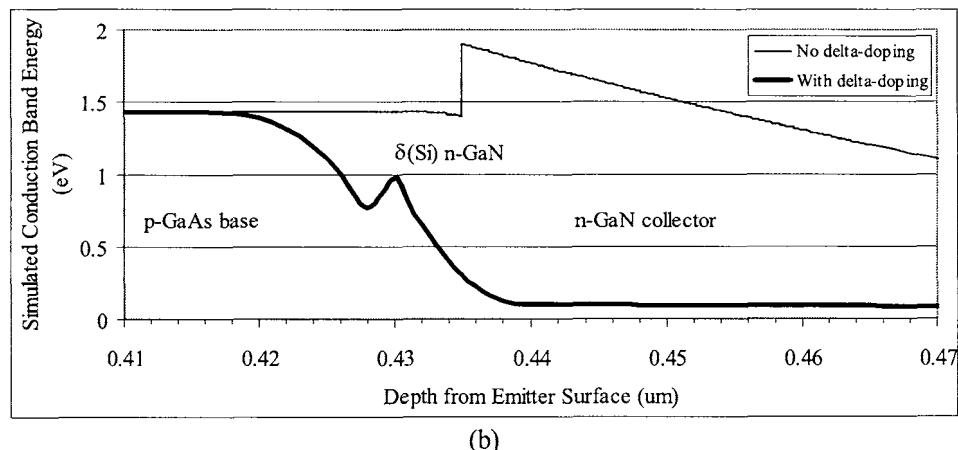
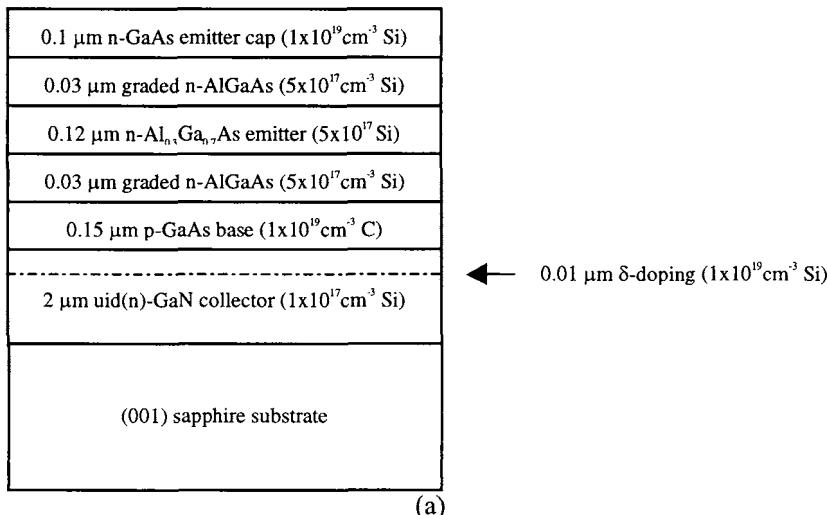
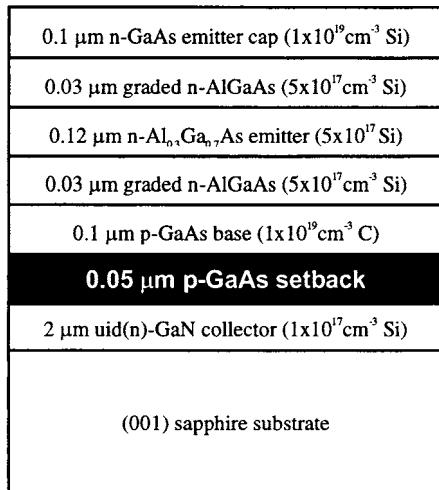
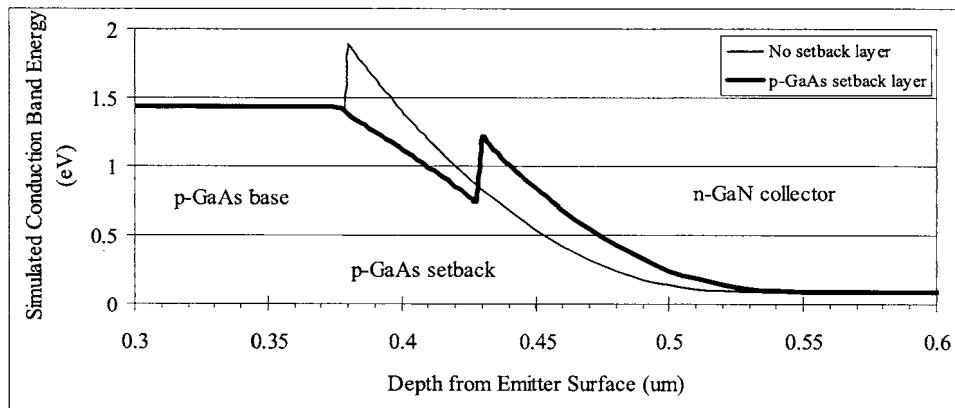


Figure IV.7. (a) Structure and (b) simulated conduction band diagram of a potential new HBT materials structure, implementing a Si δ-doped layer at the collector side of the fused junction.



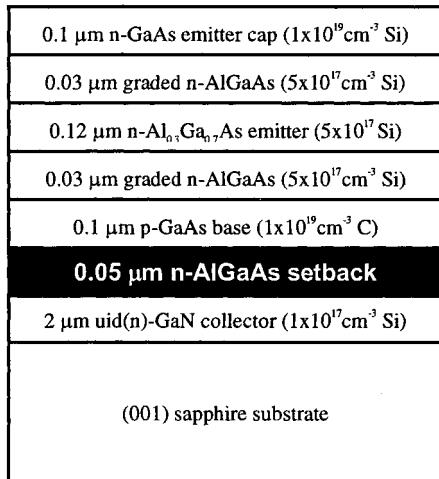
(a)



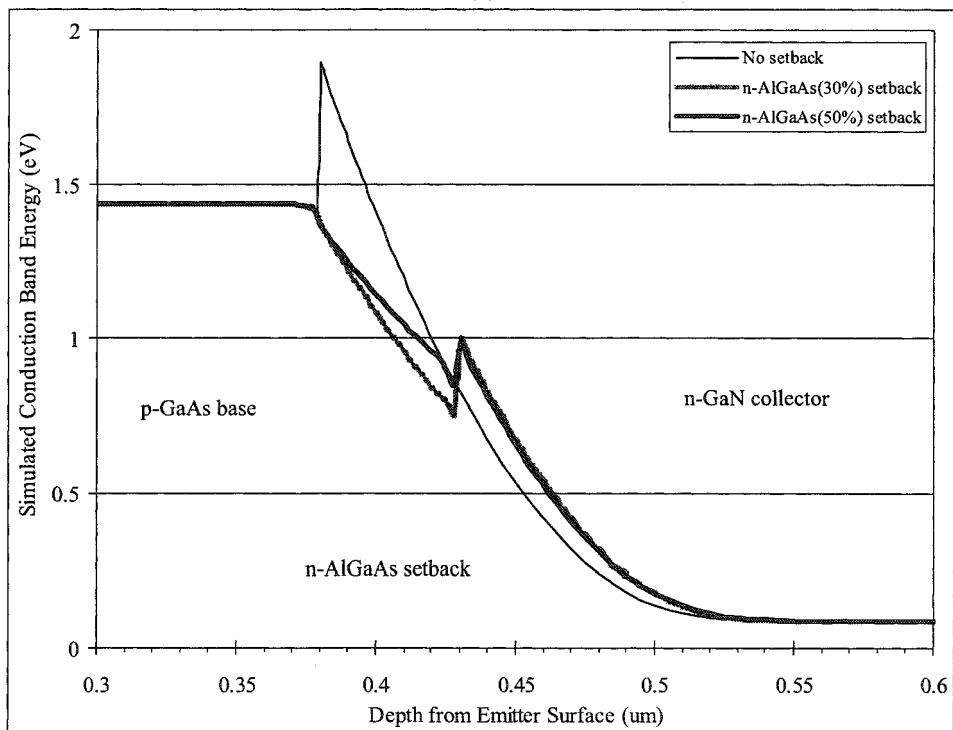
(b)

Figure IV.8. (a) Structure and (b) simulated conduction band diagram of a potential new HBT materials structure, implementing a p-GaAs, rather than n-GaAs, base-collector setback layer. The doping of the p-GaAs setback layer is simulated as $5 \times 10^{16} \text{ cm}^{-3}$ C.

However, as demonstrated with the n-GaAs setback structure (Figure IV.4.), this hope may be complicated by the issue of dopant and defect redistribution during the high-temperature fusion process. In the case of a Si δ-doped layer at the collector side of the fused junction, Si may diffuse across the fused junction toward the p-GaAs base, perhaps effecting the same degradation simulated in Figure IV.6.b. However, Si should diffuse less rapidly in the δ-doped structure than in the n-GaAs setback structure, due to the lesser diffusivity of Si in GaN than in GaAs.



(a)



(b)

Figure IV.9. (a) Structure and (b) simulated conduction band diagram of a potential new HBT materials structure, implementing a base-collector setback material with a higher band gap, such as AlGaAs. The doping of the n-AlGaAs setback layer is simulated as $1 \times 10^{17} \text{ cm}^{-3}$ Si.

V. Conclusion

This study demonstrates the first reported device characteristics of a wafer-fused HBT, and reveals a marked improvement in electrical performance due to a substantial reduction of the fusion temperature from 750°C to 600-650°C. Further reduction in the fusion temperature degrades electrical characteristics; this is likely due to many factors, such as the more elevated dopant concentrations at the interface for lower fusion temperatures (as indicated by SIMS), or such as a possible lack of the thermal energy required for proper bond reconstruction across the fusing interface. We expect further improvements in future investigations, as we optimize the HBT materials structure, in order to counteract the effects of a likely conduction band spike at the fused interface, as well as the complicated effects of dopant and defect diffusion. Through the course of development of the AlGaAs-GaAs-GaN fused HBT, we have made a great deal of progress in understanding the critical process parameters that will ensure reliable, reproducible mechanical robustness of the fused structures. Although there is much remaining work needed to fully understand the details of the fusion process, we believe that these experiments will ultimately provide much insight into the applicability of wafer fusion for electronically active, lattice-mismatched heterodevices, especially involving GaN.

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