

# FD-SOI的mVt之基本功

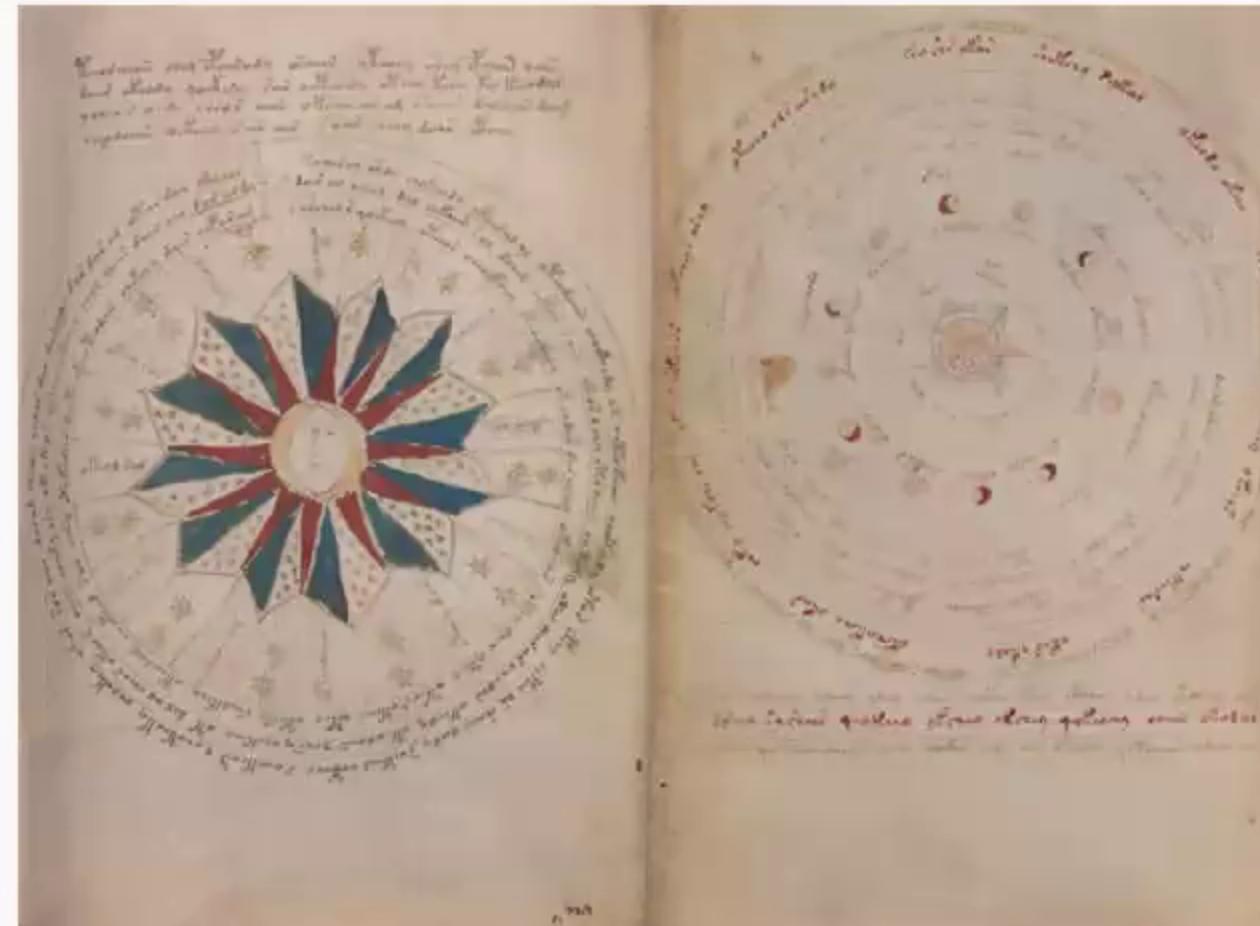
## —HKMG與鋁的故事

**IBM vs Intel and TSMC**

王不老說半导

# 伏尼契天書 (Voynich manuscript)

- 世界最神秘的一本牛皮紙書(1420年作)
- 每一页都包含綠、棕、黃、藍和紅等各色科學和植物图纸
- 無人知書中內容，許多大學教授都在研究 (**Mamamia!**博士論文都有了)



# 顧客要求: 7nm的伏尼契mVt奧義

- 右圖為硅逻辑芯片的理想國總綱，它代表了一個目前先進硅逻辑芯片顧客設計(7nm為例)所想要得到的一個伏尼契mVt奧義：
  - 外加电压  $V_{GS}$  ( $\& V_{dd}$ ) 是線性 ( $< \pm 0.7V$ )，而电流  $I_{DS}$  是指數
  - 晶圓代工廠若能提供高良率制程解碼伏尼契奧義，則必日進斗金，大賺特賺，否則只有日漏斗金，大虧特虧

ASAP7: 7-nm PDK (Microelectronics Journal 53 (2016) 105–115)

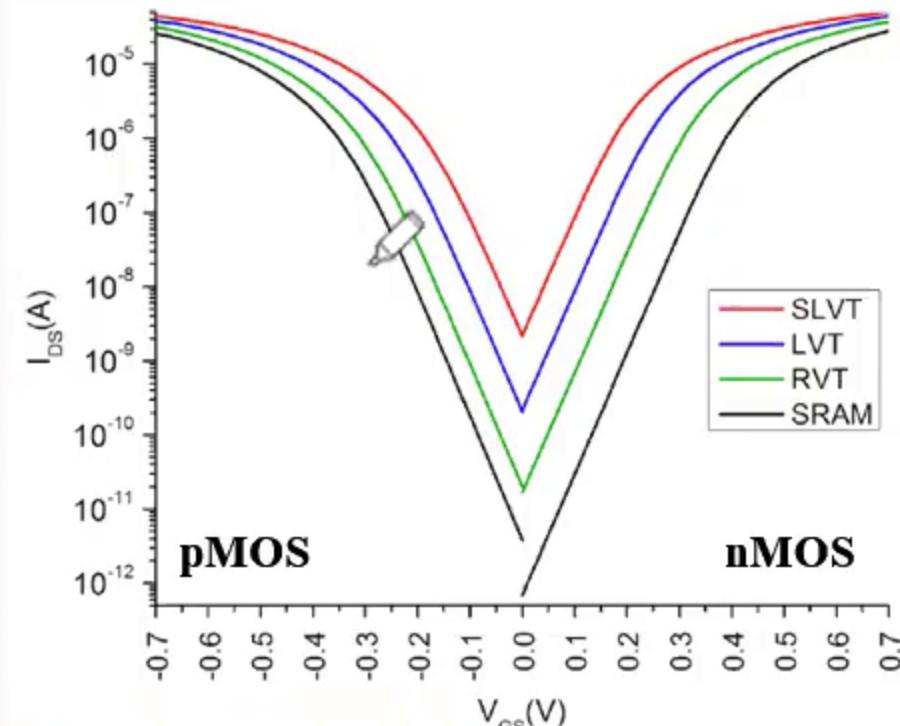
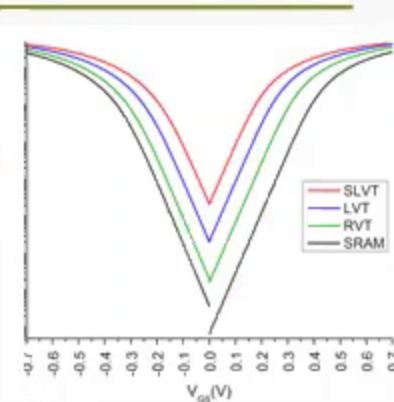


Fig. 8. Spice simulated transistor PMOS (left) and NMOS (right)  $I_{DS}$  vs.  $V_{GS}$  transistor characteristics.  $I_{off}$  drops about one order of magnitude as the  $V_{th}$  choice moves through SLVT, LVT, RVT and SRAM. PMOS  $I_{dsat}$  is approximately 90% that of the corresponding NMOS device.

# 顧客要求:7nm的伏尼契mVt奧義

internal MOS devices and layers. Four threshold options, namely high-Vt (HVT), regular Vt (RVT), low Vt (LVT) and Super low VT (SLVT) are usually proposed [Clark2016]:

- HVT – High Threshold Voltage causes less power consumption, but switching is slow. HVT are used in power critical functions.  $I_{off}$  is around  $0.1 \text{ nA}/\mu\text{m}$ ,  $I_{dsat}$  around  $1.2 \text{ mA}/\mu\text{m}$ .
- RVT – Regular Threshold Voltage (sometimes called Standard VT or SVT) offers trade-off between HVT and LVT i.e., moderate delay and moderate power consumption.  $I_{off}$  is around  $1 \text{ nA}/\mu\text{m}$ ,  $I_{dsat}$  around  $1.4 \text{ mA}/\mu\text{m}$ . **RVT 量約占 60-80%**
- LVT – Low Threshold Voltage causes more power consumption and switching timing is optimized. LVT are used in time critical functions.  $I_{off}$  is around  $10 \text{ nA}/\mu\text{m}$ ,  $I_{dsat}$  around  $1.6 \text{ mA}/\mu\text{m}$ .
- SLVT – Super Low Threshold Voltage causes even more power consumption but switch at the highest speed. SLVT are used in time-critical functions without consideration of leakage currents.  $I_{off}$  is around  $100 \text{ nA}/\mu\text{m}$ ,  $I_{dsat}$  around  $1.8 \text{ mA}/\mu\text{m}$ . **SLVT 电流最大漏电量也最多**



ASAP7:7-nm PDK  
(MicroelectronicsJournal5  
3(2016)105–115)

# 十萬大軍齊解甲，只有一個是男兒

- 兩綠區中適合nMOSFET的金屬必須有較低的功函數，其電子很容易受外界引誘，皆不安於室，易紅杏出牆，特別愛與氧苟合
- 結果只有鋁可以用
- 反之，適合pMOSFET的，卻較不愛氧，品格高尚，所以人稱貴重金屬(noble metals)
  - 基本上，全軍覆沒

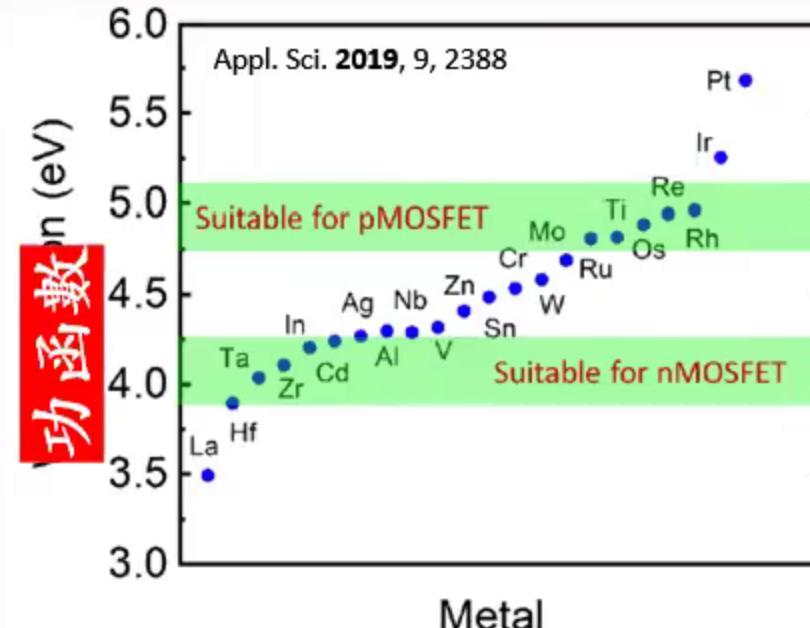


Figure 7. Work function of metals.

# Intel石破天驚鋁制程

- 2007，英特尔石破天驚宣布HKMG制程，大家跌破眼镜的新材料，除了HK( $\text{HfO}_2$ )之外，就是MG(门极金属)裡面竟然含鋁
  - 右图应是美商应用材料的4nm nWF 即含鋁(= TiAlN or TiAlC)
  - 鋁熔点低(660.4C)，芯片制程，随便便就是五六百度C，甚至更高，有鋁在内，鋁原子岂不是四处乱窜
    - 为了避免这种状况发生，HK制程必须改变→ Gate Last

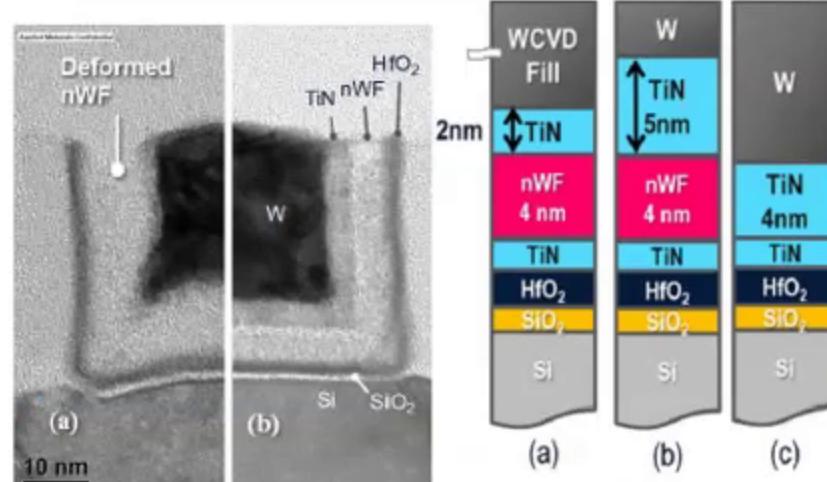


Fig. 8. Cross-sectional TEM (x-TEM) of MOSFET gate with (a) 2 nm, (b) 5 nm barrier TiN and schematics of the film stacks. No TEM image shown with the sample (c).

IEDM'17, N. Yoshida et al.

# TSMC解碼伏尼契2Vt奧義

- **p-1<sup>st</sup> 2Vt**: 先放上一個高功函數(例如TiN)給每個人(如右上圖a)
- 用TaN來選擇性的去掉(一般用wet etch)特定地區的TiN (b, c)
- 最後，再放上一個低功函數，也就是TiAlC(d) + TiN保護 (e)
- 但今後所有制程  $T < 500\text{C}$ ，否則鋁會又開始亂竄作亂
- **試問**: 哪個元件會有最厚的金屬層？

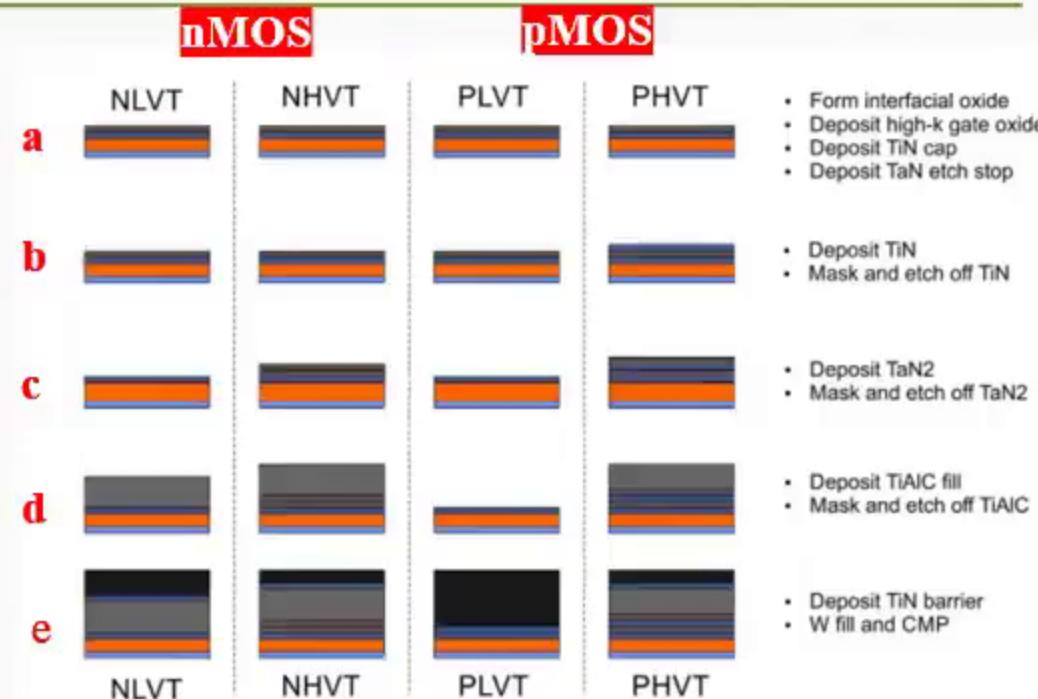


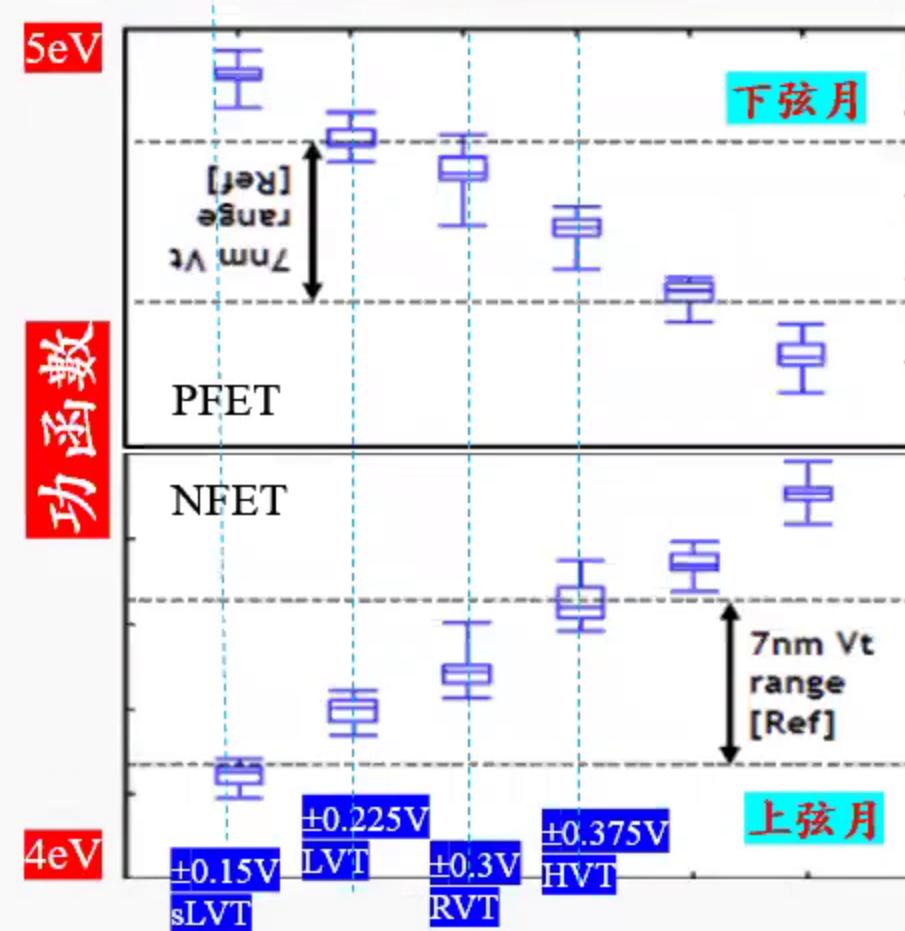
Figure 4. Four work function metals.

This process flow was developed after examining cross sections of 10nm TSMC process provided by TechInsights.

<https://semiwiki.com/semiconductor-services/ic-knowledge/7259-iedm-2017-controlling-threshold-voltage-with-work-function-metals/>

# TSMC解碼伏尼契6Vt奧義

- sLVT: super low V<sub>t</sub>, 提供手機最大電流，所以當你一直在快速網搜之時，手機知道你所需急切，會自動启动此模式(但漏电量也最大，手機會更熱)
- LVT/RVT: low and regular V<sub>t</sub>, 提供手機一般電流，所以當你普通網搜之時，自动启动之模式
- HVT: high V<sub>t</sub>, 一般而言，自动启动此模式於手機關機時，省電之用



# 鋁制程與HK愛恨交加

- 鋁制程的目的，就是要降低功函数(effective work function)，所以此值必须越低越好，然而鋁制程在其他的材料上面作用不大，反而对HK( $\text{HfO}_2$ )降低功函数的效应特别显出(如右上图)
- 此特殊的作用应归功于鋁与HK( $\text{HfO}_2$ )介面产生一个特殊的費米能階釘扎效應(Fermi-level Pinning Effect)，如右下图

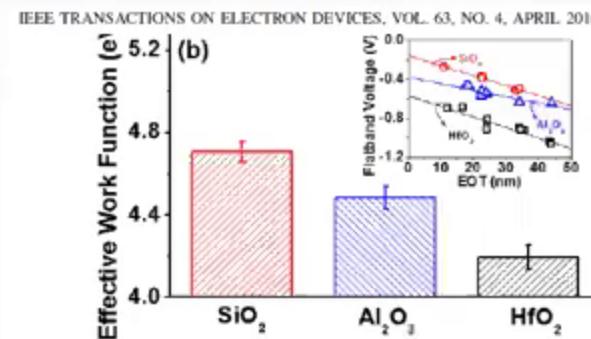
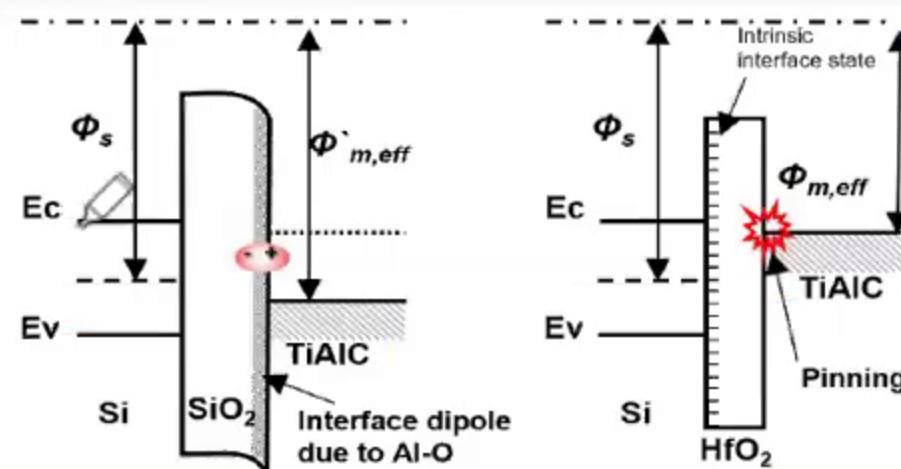


Fig. 1. (a) Normalized C-V curves of ALD-TiAlC on  $\text{SiO}_2$ ,  $\text{HfO}_2$ , and  $\text{Al}_2\text{O}_3$  at 100 kHz after FGA. (b) Extracted eWLF of the ALD-TiAlC on three different gate dielectrics. Inset: eWLF was obtained via linear fitting from the plot of  $V_{FB}$  versus EOT.



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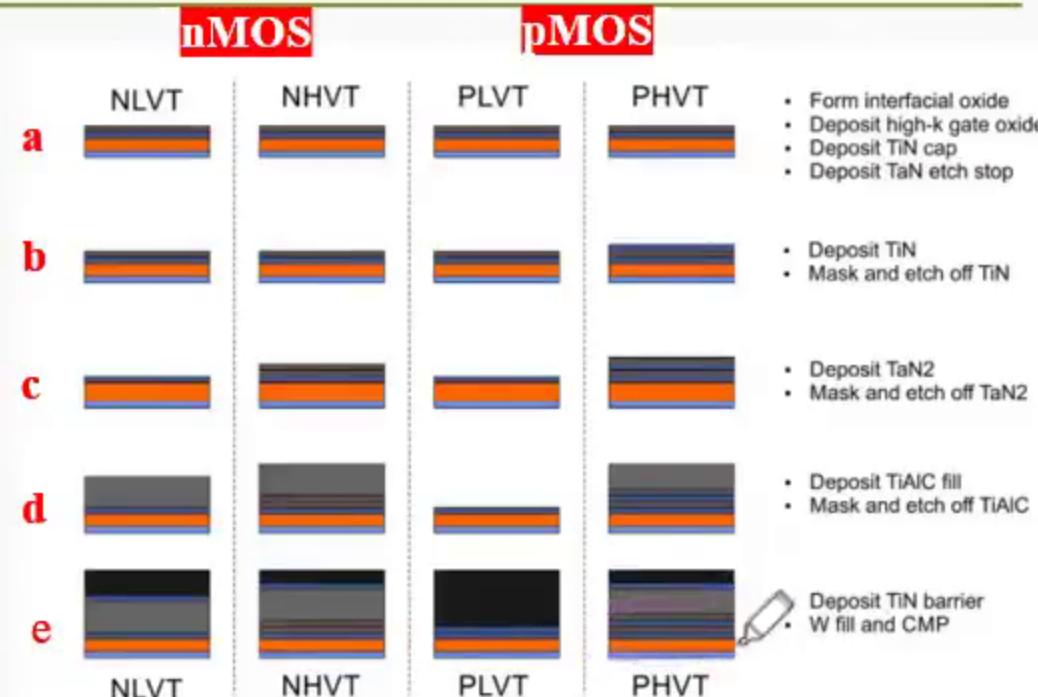


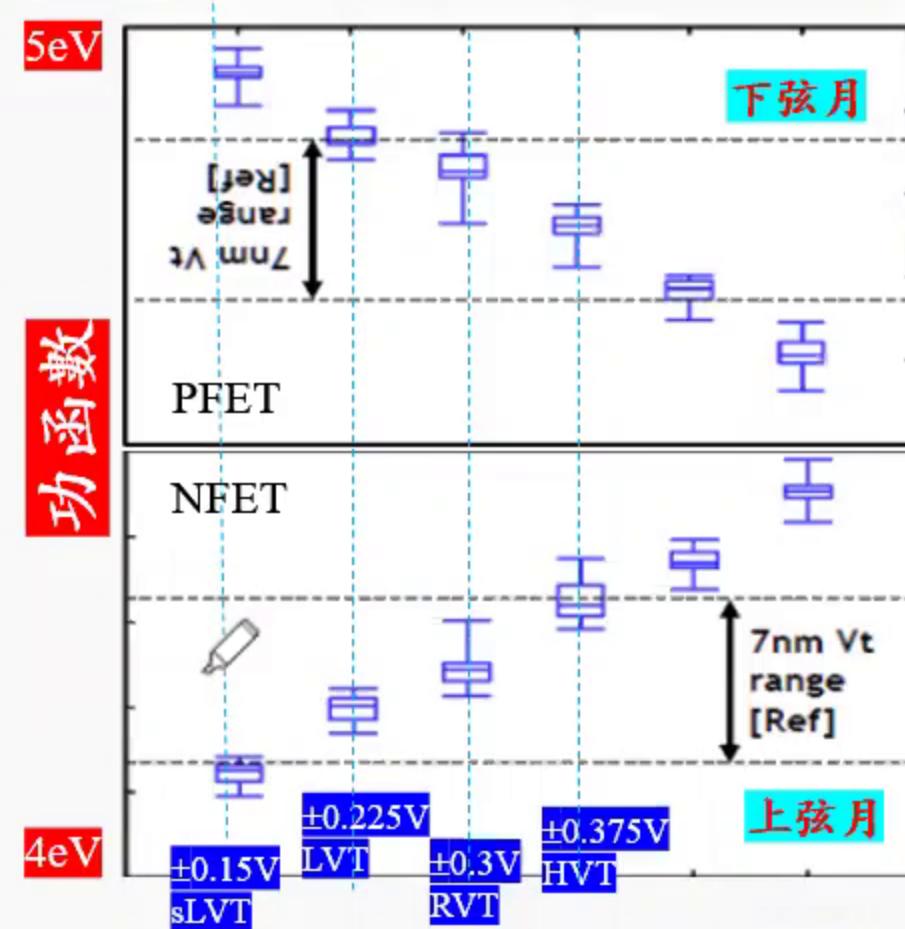
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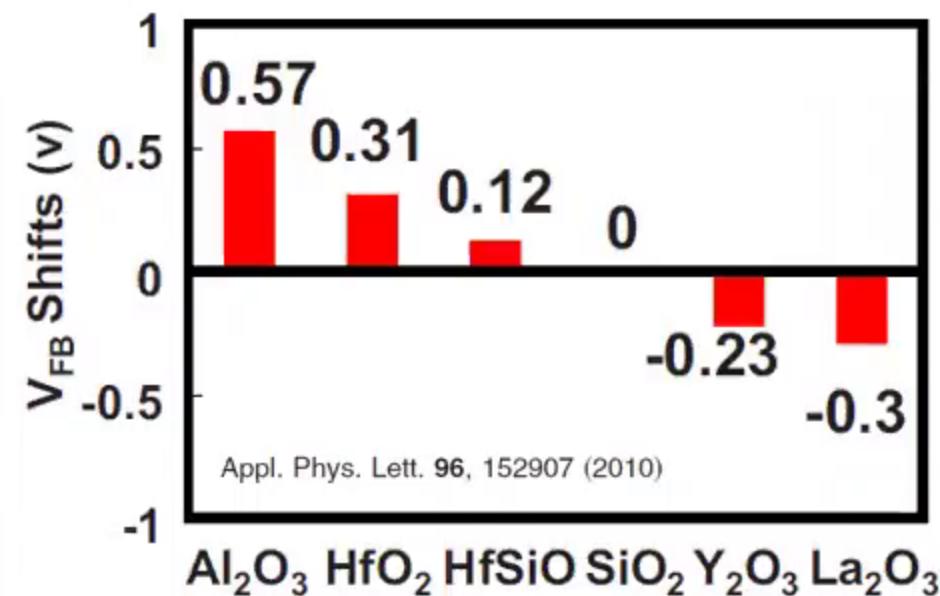
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# IBM別出心裁陶瓷功函數制程

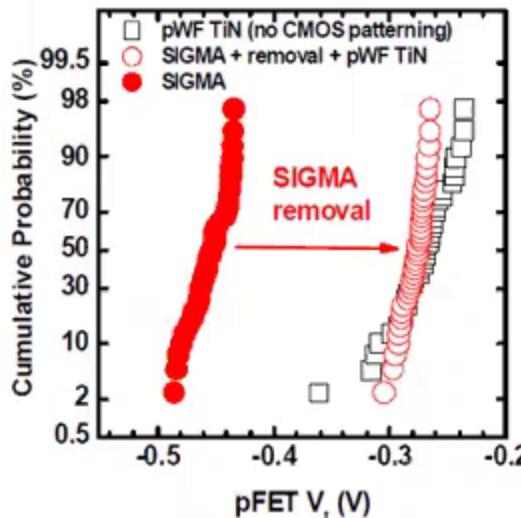
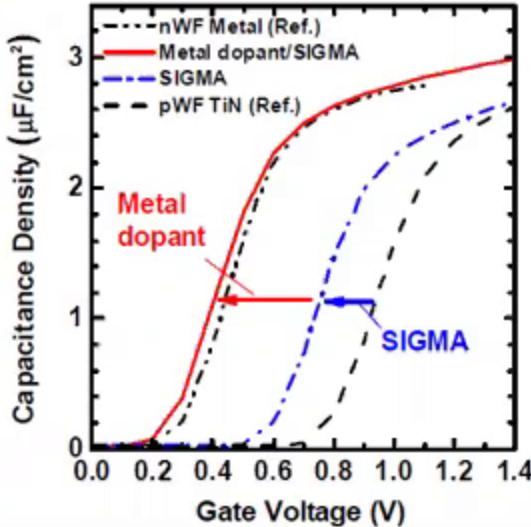
- 右圖顯示不少陶瓷材料與SiO<sub>x</sub>(附骨之疽氣不許也)親密接觸後，發現個性其實大不相合，二者之間立馬有了缺陷(曰之“DCIGS”)，最後竟然扭曲了電場，改變了V<sub>t</sub>(-0.3到0.57V)，幅度還真不小，絕不比金屬差)
- IBM利用此一特性，別出心裁，實現於其mVt制程上



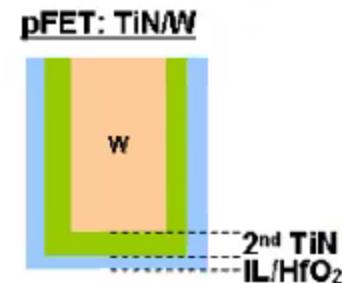
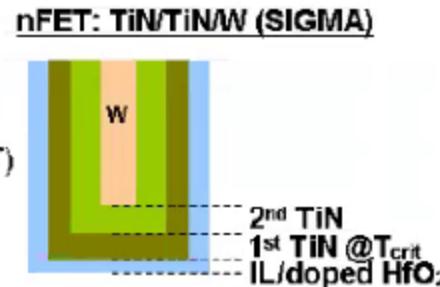
DCIGS = dielectric contact induced gap states

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- IBM (Ando T.) 別出心裁以**金属氧化物**，以ALD方式鍍於HK上，在以高溫退火(**drive-in anneal**)驅動，最後花落HKIL之上，再輔與**SIGMA Anneal**，可以調節V<sub>t</sub>



- Dummy gate removal
  - IL/HfO<sub>2</sub> preparation
  - Metal dopant deposition
  - Litho./dopant etch (from pFET)
  - Dopant drive-in anneal
  - 1<sup>st</sup> ALD TiN (@T<sub>crit</sub>)**
  - a-Si deposition
  - WF-setting anneal
  - a-Si etch
  - Litho./TiN etch (from pFET)
  - 2<sup>nd</sup> ALD TiN**
  - W deposition
  - Metal CMP
- SIGMA formation**



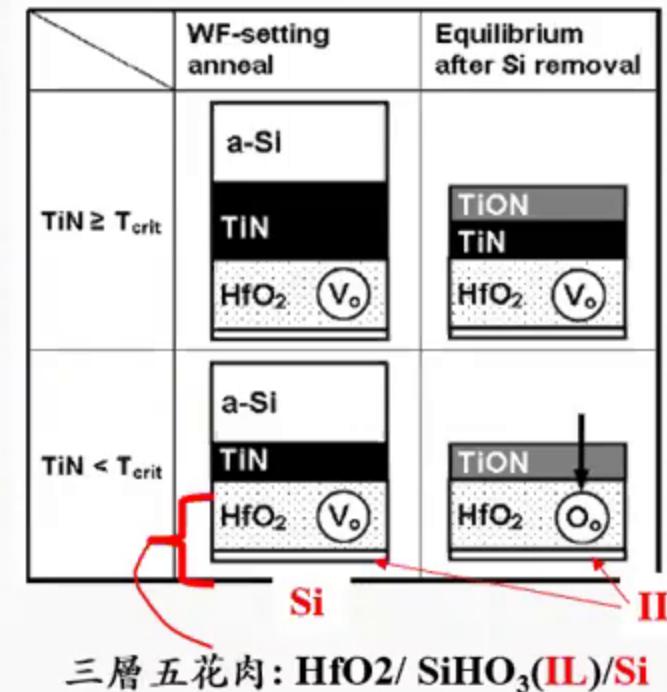
Simple Gate Metal Anneal (SIGMA) Stack for FinFET Replacement Metal Gate toward 14nm and beyond, Ando et al, VLSI 2014

# RMG Nano Reflow - SIGMA

鍍上一屢數nm厚的TiN目的為何？

解答：

- 金光闪闪的氮化鈦TiN也是奇妙，它不僅化學穩定，可當炒鍋，竟然也導電，還可用來做許多先進製程內特殊材料的保鏢
- 右下圖中的TiN，就是用來保護那重要的三層五花肉： $\text{HfO}_2/\text{SiHO}_3(\text{IL})/\text{Si}$ ，可以使得第三步的高溫迴流退火(anneal)能夠更加安全有效



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- 钛金属本身是活性非常大，见到氧就吃(oxygen scavenger)，
- 氮化钛可能含有相当高成分的氧气，例如右图中所示氧成分可以高达30到40百分比(thermal ALD)
- 氮化钛內含的氧，在第三步的高温迴流退火(anneal)時，會被灌入 HfO<sub>2</sub>/ SiH<sub>4</sub>O<sub>3</sub>(IL)/Si 中，對mVt又是一功

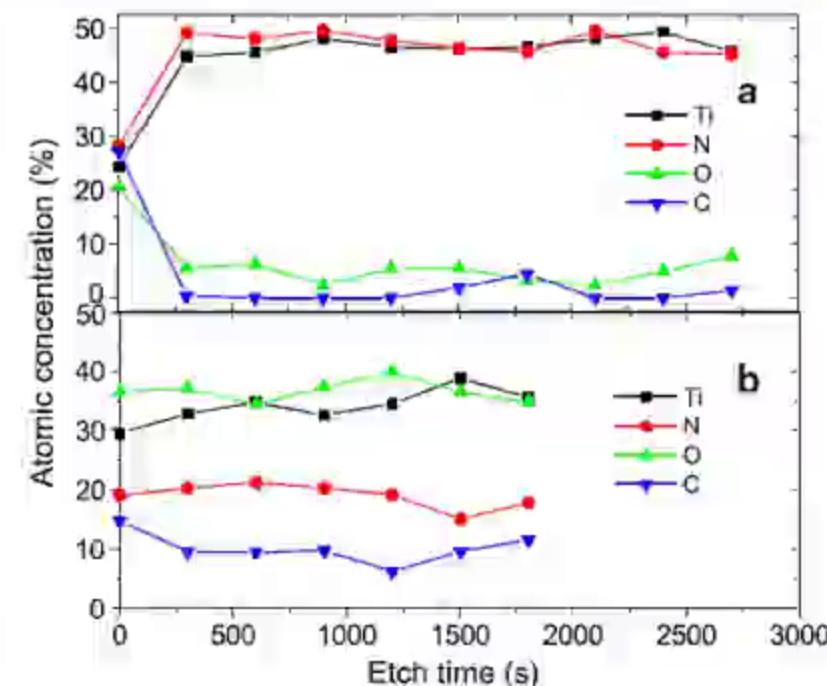


Fig. 8. XPS depth profile of films deposited by (a) plasma enhanced ALD with 30 s 500 W NH<sub>3</sub> plasma and (b) thermal ALD with 6 s NH<sub>3</sub> pulse, both at 200 °C. The film deposited by PE ALD has far fewer impurities.

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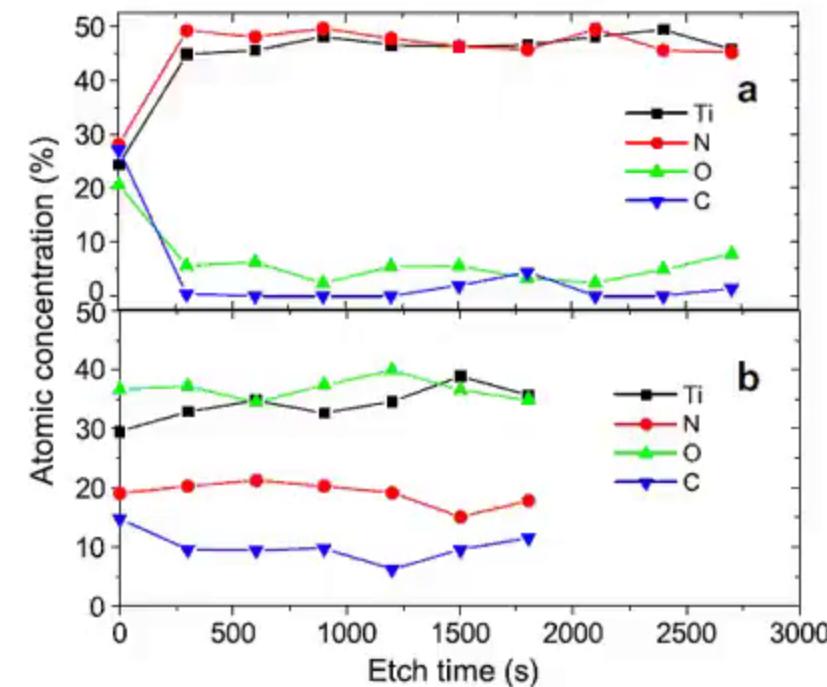


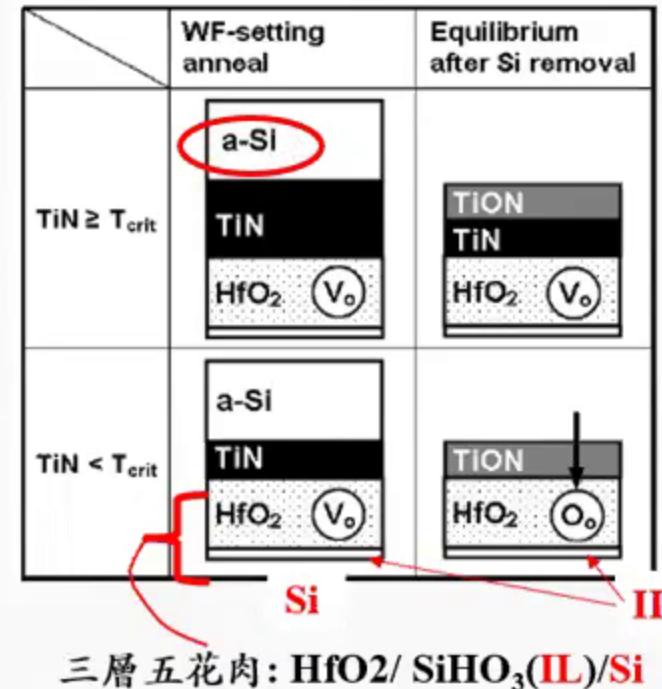
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試問: 鍍上一層數nm厚的aSi目的為何?

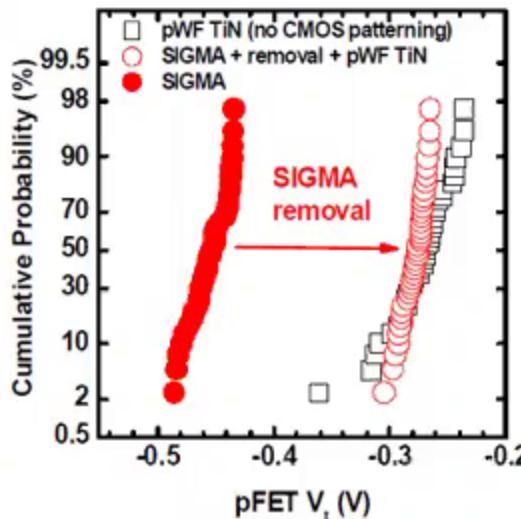
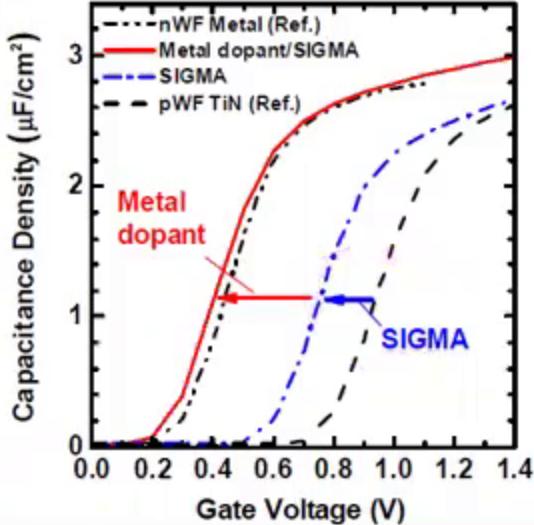
解答:

1. aSi內也有氧(氧無處不在), 在第三步的高溫迴流退火(anneal)時, 也會被灌入其下方的HKIL
2. Si的热传导系数( $130\text{W/m/C}$ ) >> TiN ( $3\text{W/m/C}$ ), 所以aSi可以使得高溫迴流退火更均匀, 增加與此有關製程的晶圓均匀性(WIW)及良率

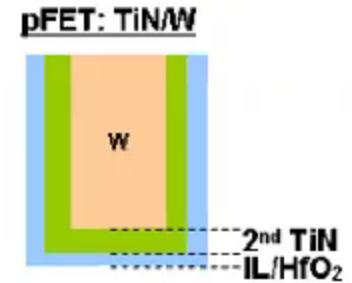
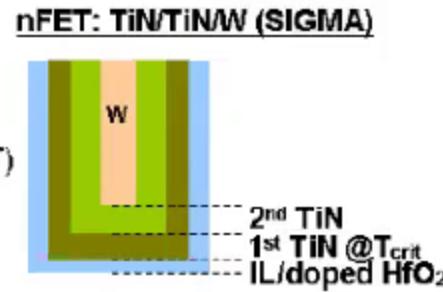


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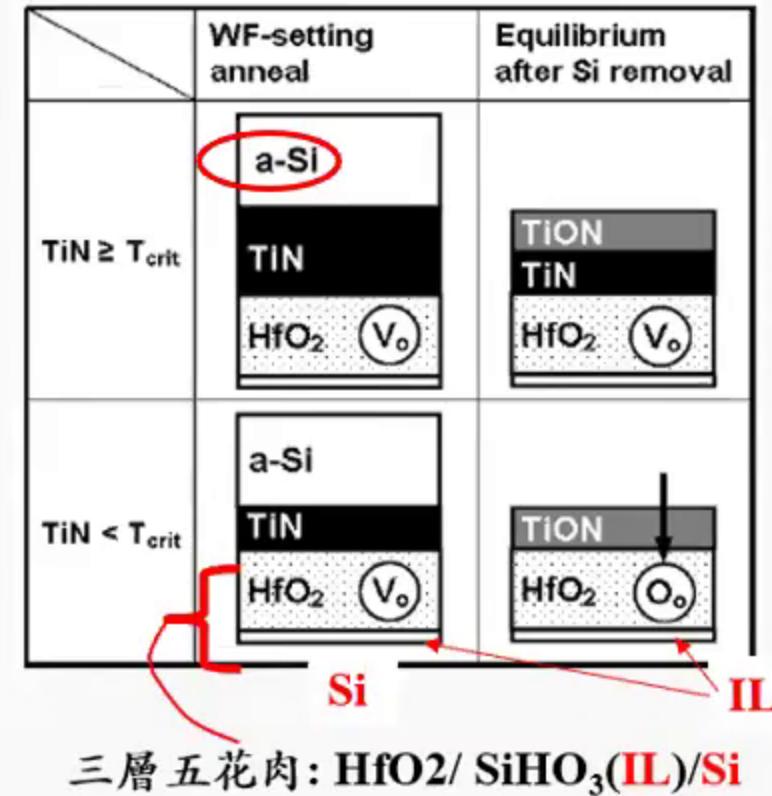
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- 高溫迴流退火(anneal)目的:
  1. 灌氣  $\text{HfO}_2/\text{SiHO}_3(\text{IL})/\text{Si}$  (見右)
  2. 修補  $\text{HfO}_2/\text{SiHO}_3(\text{IL})/\text{Si}$  所有的天生缺陷，目的是使得缺陷密度  $< 10^{10}/\text{cm}^2$  (原來可能有  $> 10^{12}/\text{cm}^2$ )，使得芯片的性能及可靠性得以完善

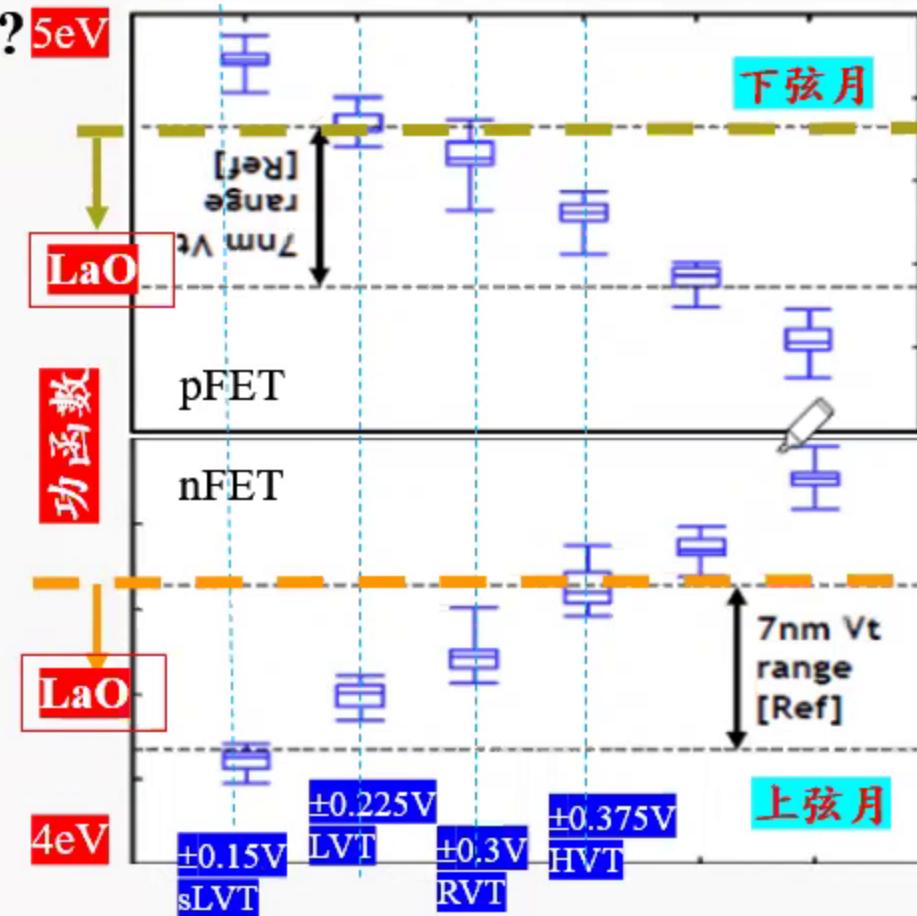


# 陶瓷功函數:La-O (n-dipole)

試問:n-dipole對nFET與pFET都有用嗎? 5eV

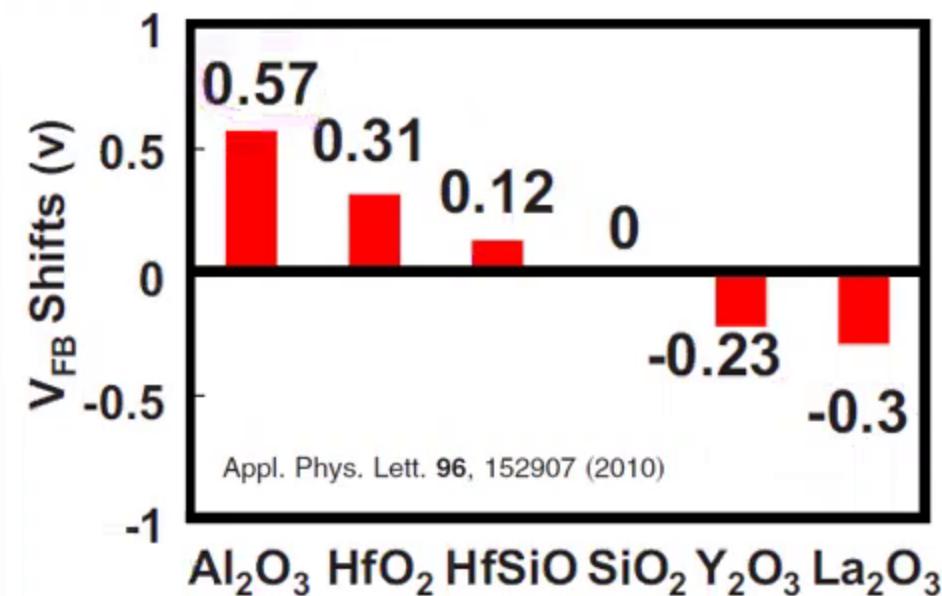
解答: 是的, 但卻可能有不同的副作用

- 例如La-O了減少系統功函數→原始功函數被逼向**下走**, 結果導致:
  - LaO植入pFET區→**Vt向右走**
  - LaO植入nFET區→**Vt向左走**, 與pFET相反
  - 注意: 要牢記右圖二曲線趨勢



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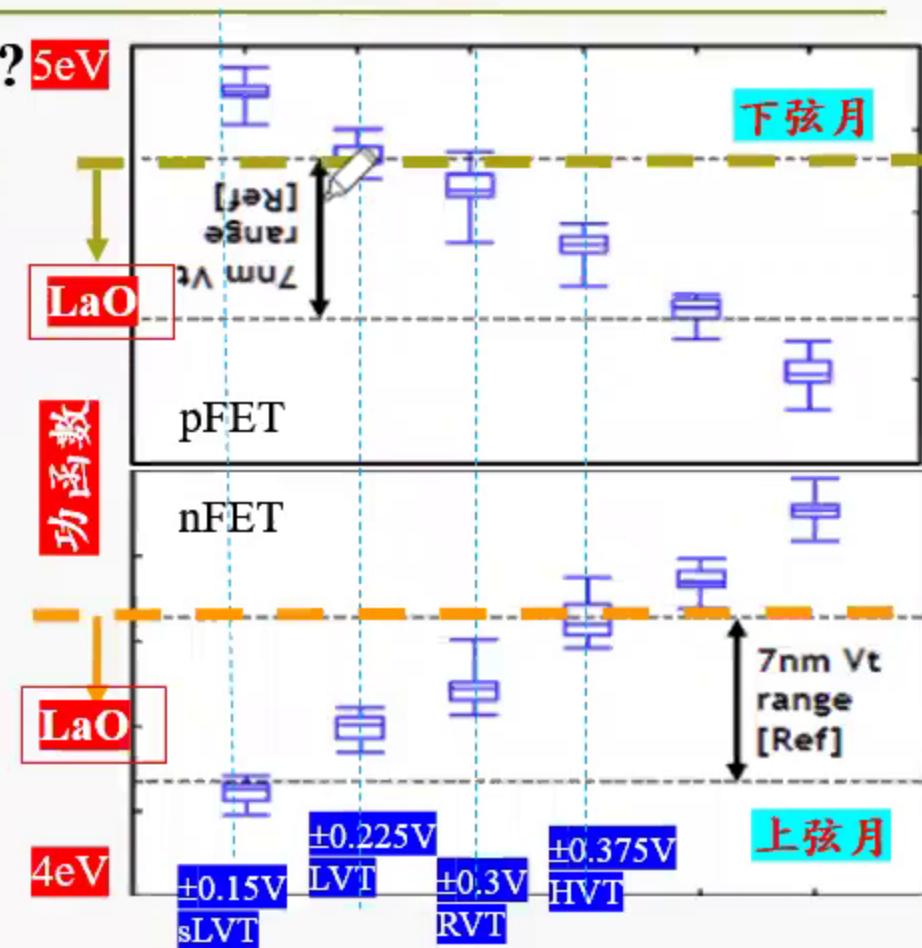
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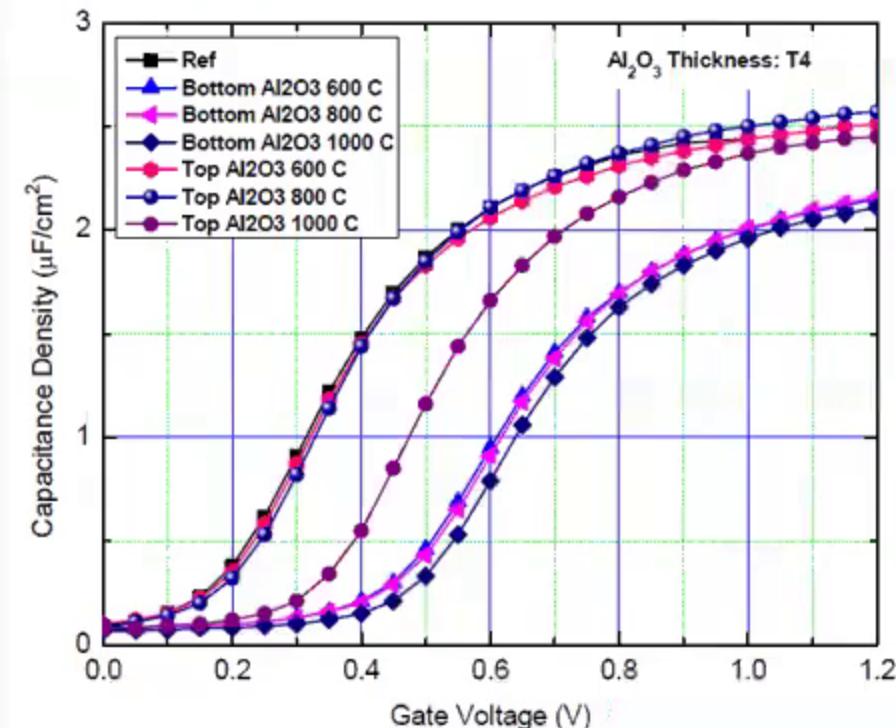


# 陶瓷功函数:Al-O (p-dipole)



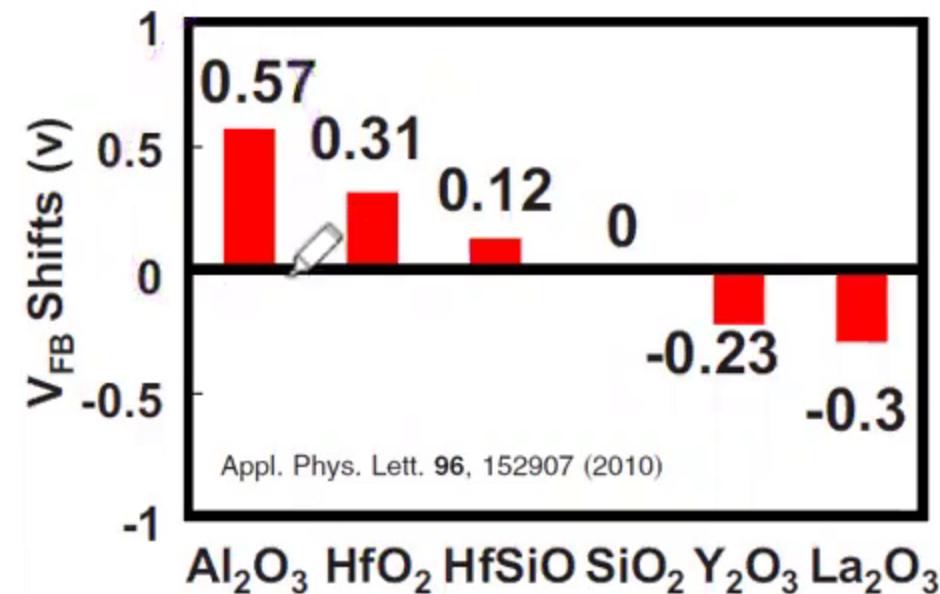
解答: AlO也

- 例如右圖形成 $\text{SiO}_x/\text{AlSiO}/\text{HfO}_2$ 或者 $\text{SiO}_x/\text{HfO}_2/\text{AlO}$ 三層膜都可改變 $V_t$
- AlO對nFET與pFET也都同樣有用，且與LaO的作用正好相反
- 是為p-dipole
- Dipole的使用要小心，任何物質跑到介面，都對可靠性產生影響，是好是壞，卻很難說



# IBM別出心裁陶瓷功函數制程

- 右圖顯示不少陶瓷材料與SiO<sub>x</sub>(附骨之疽氣不許也)親密接觸後，發現個性其實大不相合，二者之間立馬有了缺陷(曰之“DCIGS”)，最後竟然扭曲了電場，改變了V<sub>t</sub>(-0.3到0.57V)，幅度還真不小，絕不比金屬差)
- IBM利用此一特性，別出心裁，實現於其mVt制程上



DCIGS = dielectric contact induced gap states

# 加場演出：IBM的2nm高溫混搭n/p制程

評論：IBM最新2nm nanosheet mVt制程以混搭方式(n-LaO, p-AlO)有成

- Vt確實可以隨意調整(厲害了)

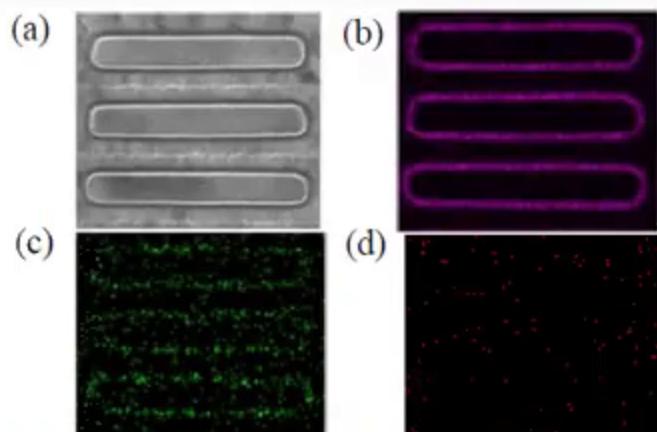


Fig. 7 TEM analysis for NS pFET with dipoles. (a) TEM image, (b) Hf signal, (c) p-dipole signal, and (d) n-dipole signal.

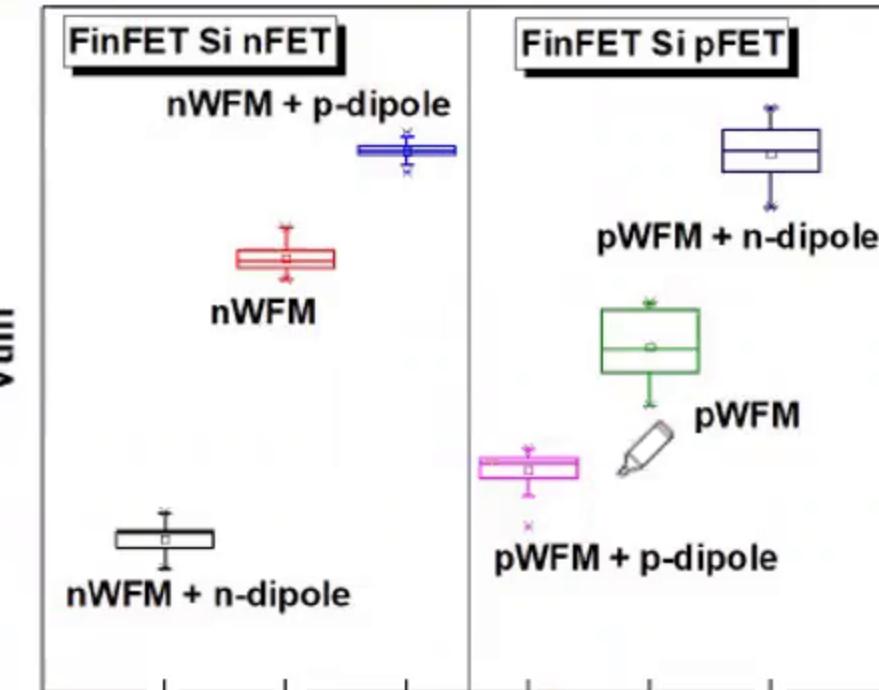


Fig. 9 The Vt trend for dual dipole selective enablement on FinFET.

# 加場演出：IBM的2nm高溫混搭n/p制程

- IBM的高溫制程(HT drive-in dipole-last), 混搭方式對(EOT與reliability)影響存疑?
- 而且東西混太多，往往缺陷(餓死鬼)必多，通常沒好下場!!

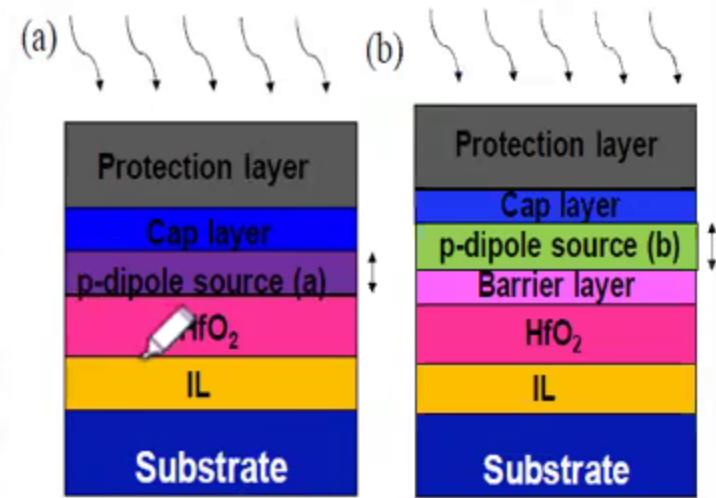
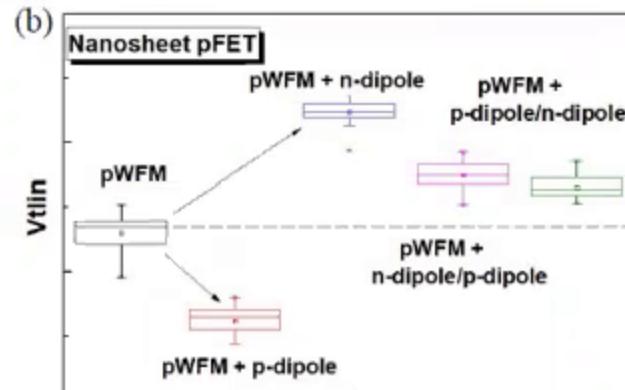
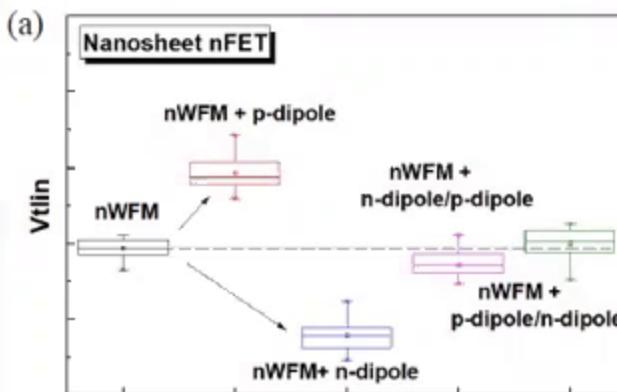
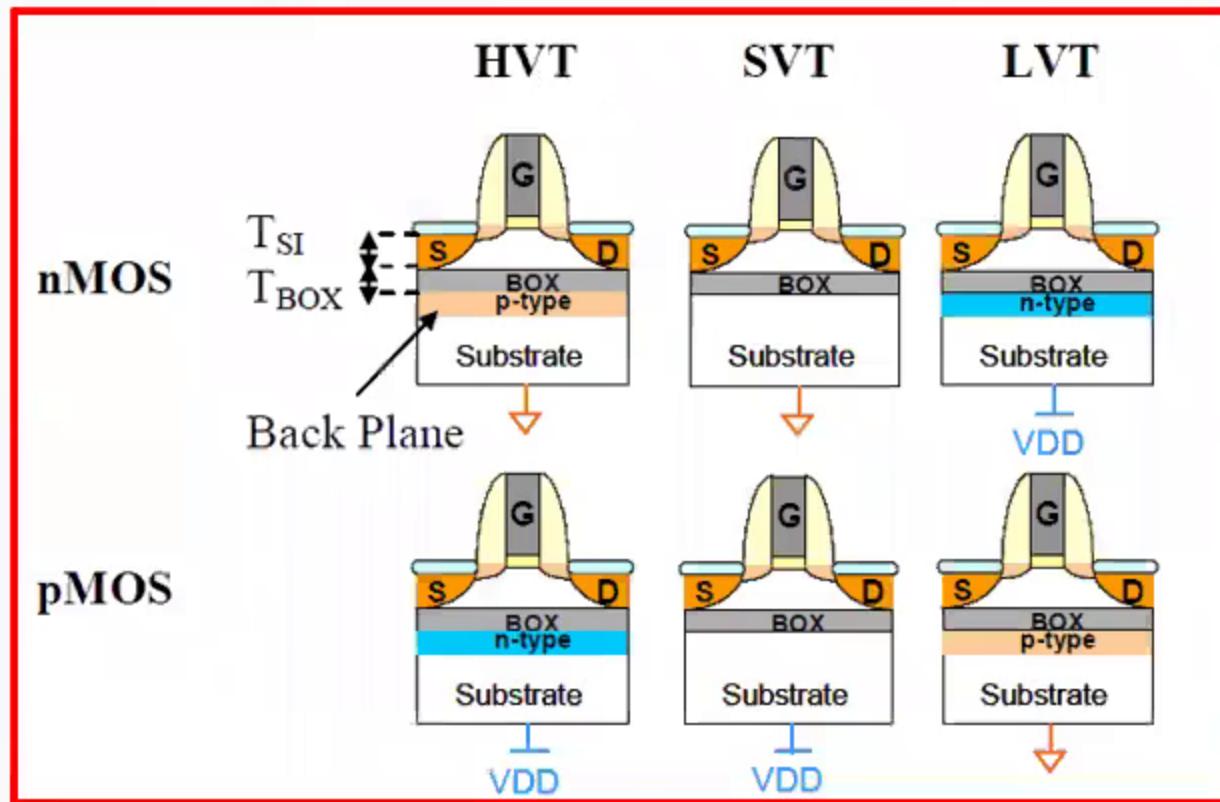


Fig. 1 Two different Al sources for p-dipole  
(a) Process A and (b) Process B.

Selective Enablement of Dual Dipoles for Near Band edge Multi-Vt Solution in High Performance FinFET and Nanosheet Technologies, R. Bao et al., VLSI'20, TC3.2

# 終場加演：32nm FDSOI的混搭n/p制程

- 其實mVt中混搭n/p制程的，還有32nm FD-SOI
- 例如右图所示，LETI就曾建議以混搭 n/p Back Plane (也叫Ground Plane) 的方式達到 $\pm 3Vt$ 的目的，也是漂亮的
- 對於FD-SOI的mVt制程，**曰之隔山打牛**，將陸續深入探討之



O. Thomas et al., "32nm and beyond Multi-VT Ultra-Thin Body and BOX FDSOI: From device to circuit," ISCAS 2010, pp. 1703-1706