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TSMC Yields

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GlobalFoundries $GFS IPO – Mubadala Lost Over $22.4B, Now They Are Hoping Public Markets Bail Them Out

October 6, 2021 Dylan Patel 0 Comments GlobalFoundries, Mubadala

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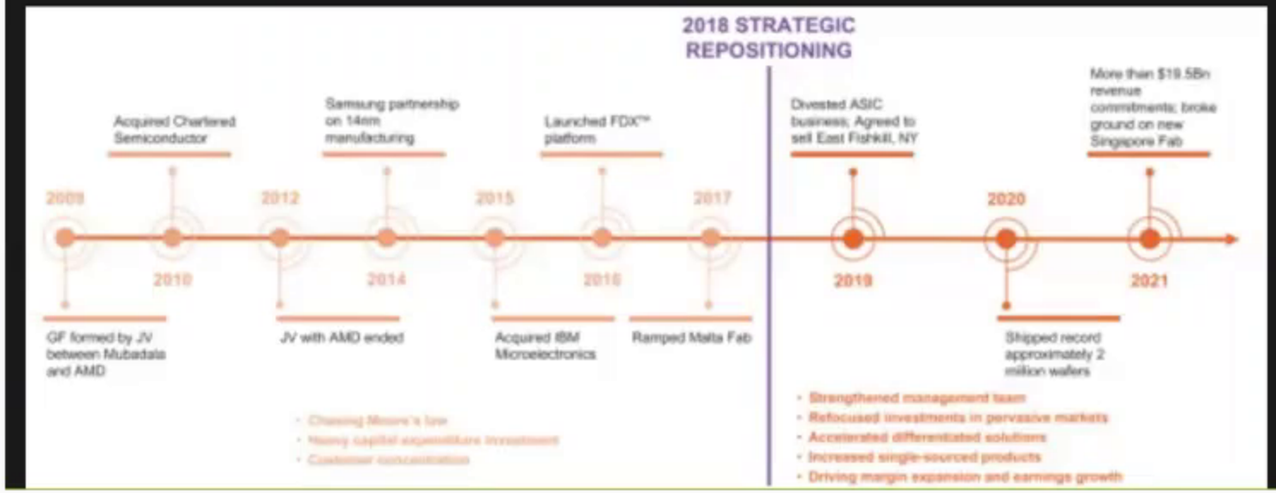

AMD Moves All 7nm CPU, GPU Production to TSMC

By Joel Hruska on August 27, 2018 at 4:00 pm | Comments

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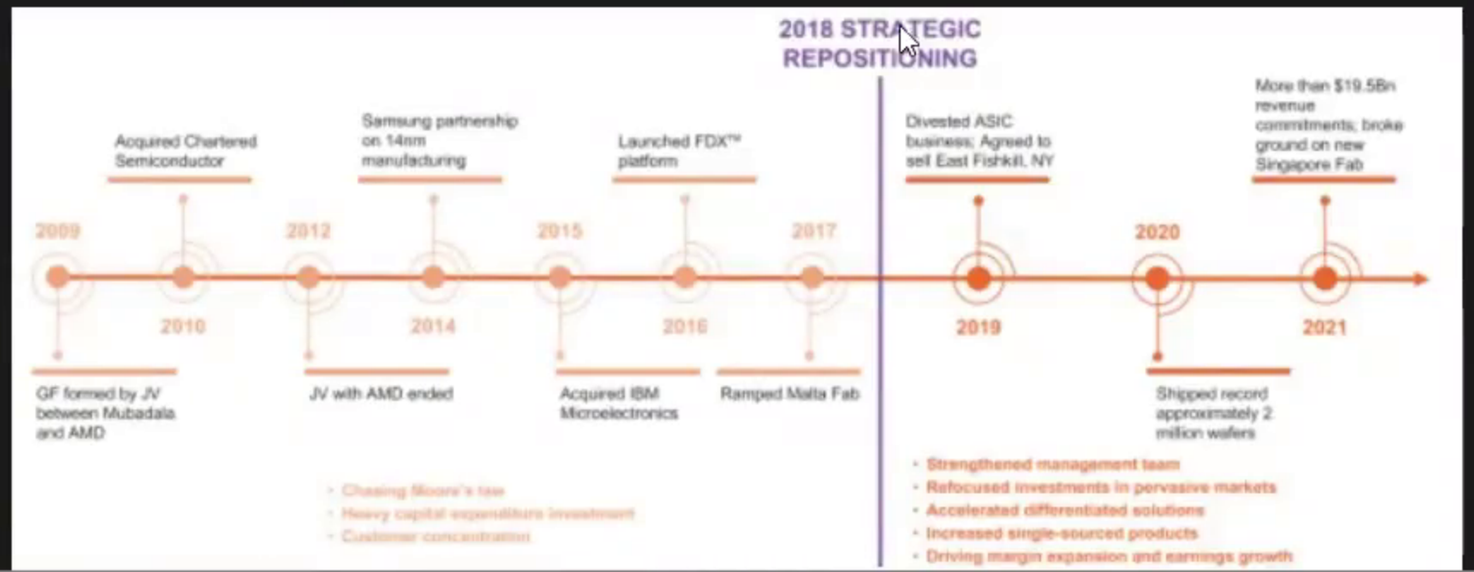

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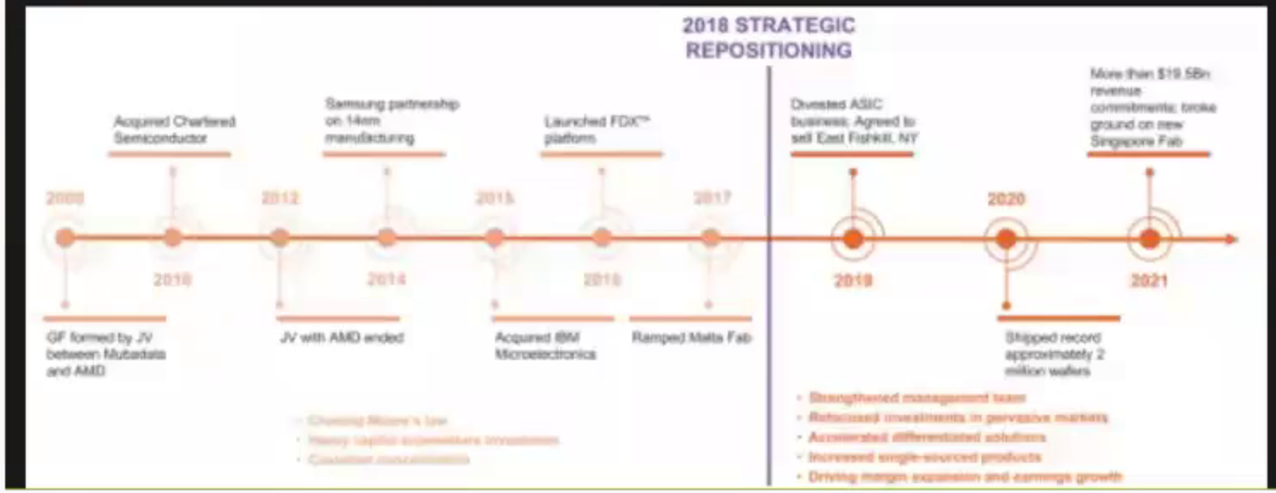

限制良率的罪魁禍首?

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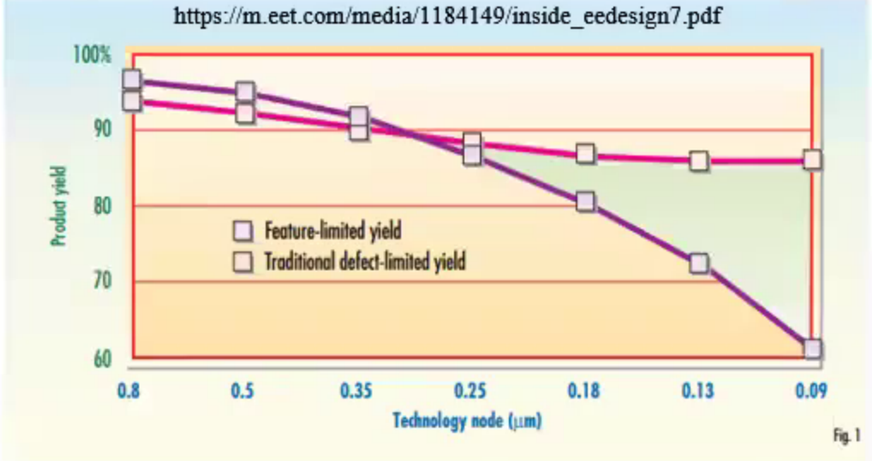
  - 顧客與代工工廠共同合作設計產生的 **PDK/Mask design 出了問題 (x星的軟肋)**

https://m.eet.com/media/1184149/inside_eedesign7.pdf



The modeled trends with defect-limited versus feature-limited yield with successive IC technology nodes. The defect-limited yield trend assumes constant failure rates for each successive technology node. The feature limited yield trend assumes a 50% improvement for each successive technology node, while the number of features grows >50% per node.

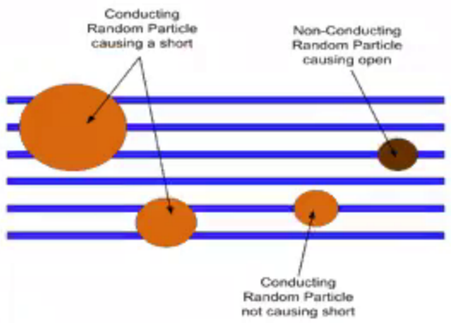


Figure 6. Particulate defects

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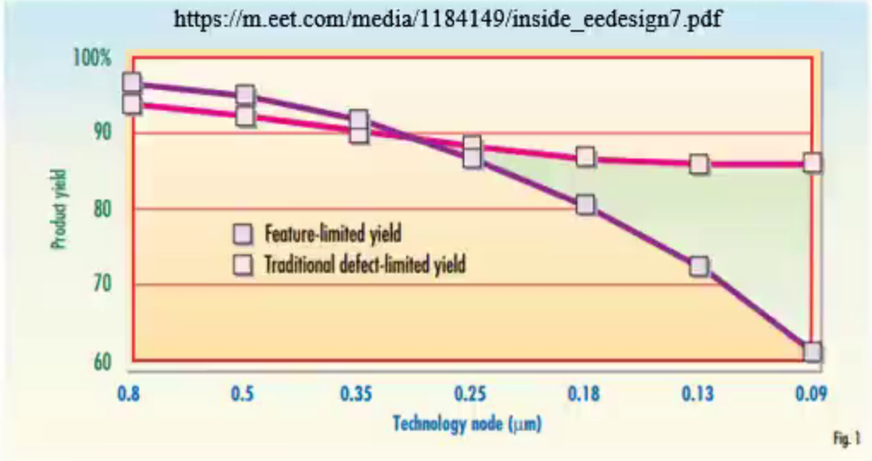

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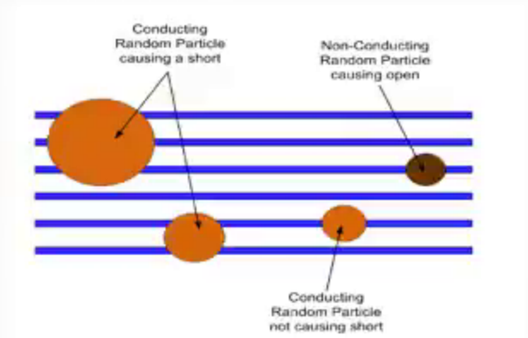

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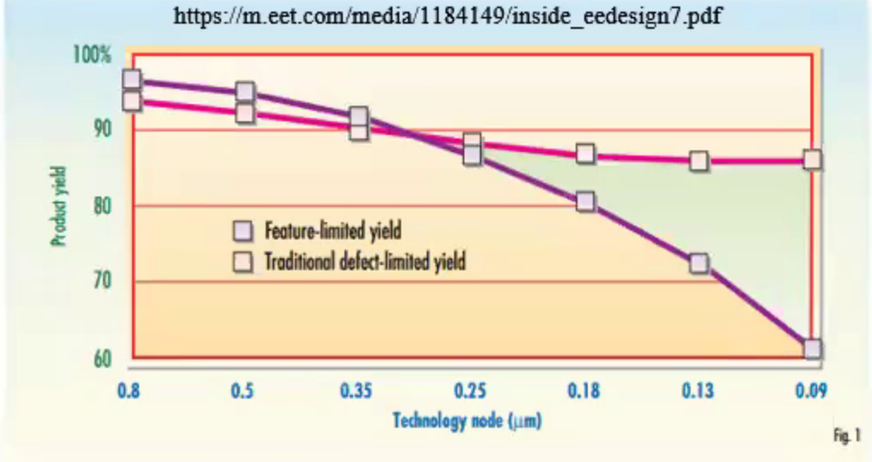

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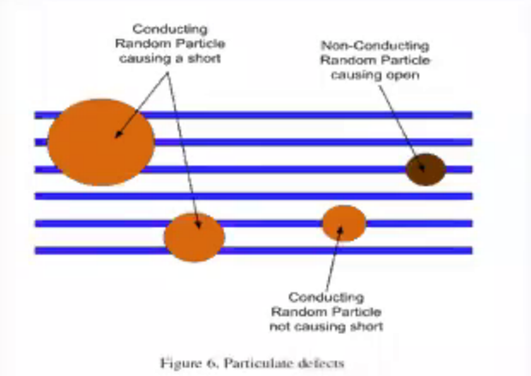

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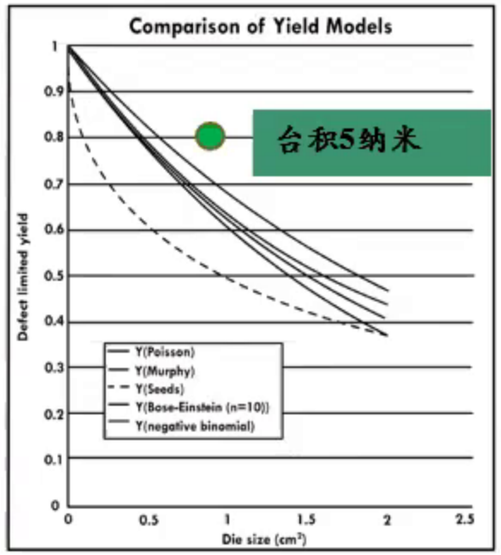
  - 目前教課書上所有的良率公式，皆不適用了 (見下圖，台積良率竟在理論估計值之上)



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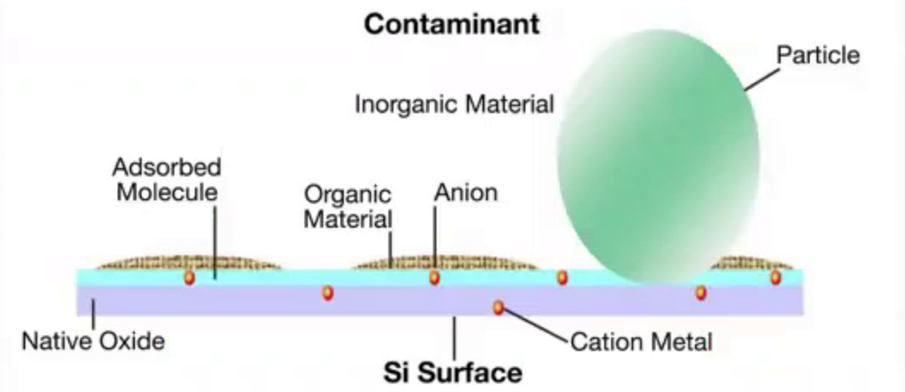
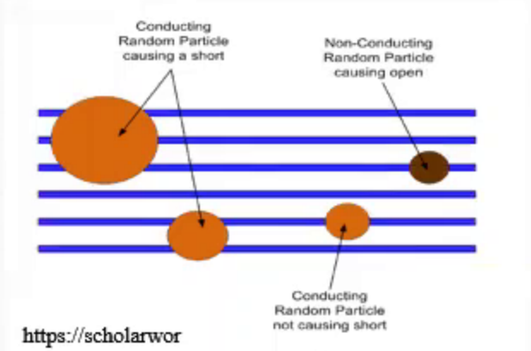
https://www.mksinst.com/n/wafer-surface-cleaning





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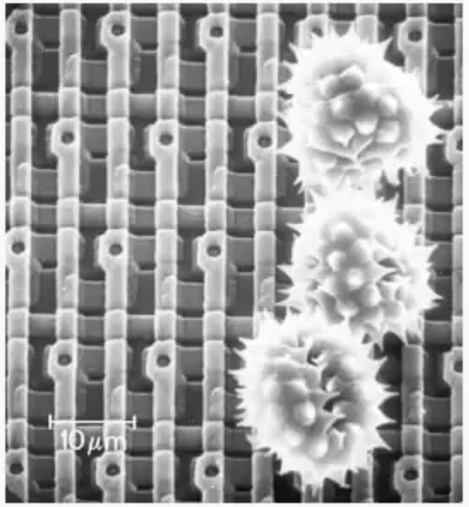

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    - **Process margin issue?**
  - 英x爾 invented this process but failed to deliver yield performance in HVM
    - **Lost 10/7NM markets (CEO was kicked out)**
  - TSMC, as a copycat, did a better job
    - **Become world No.1**

2015 IEEE International Interconnect Technology Conference and 2015 IEEE Materials for Advanced Metallization Conference (IITC/MAM)

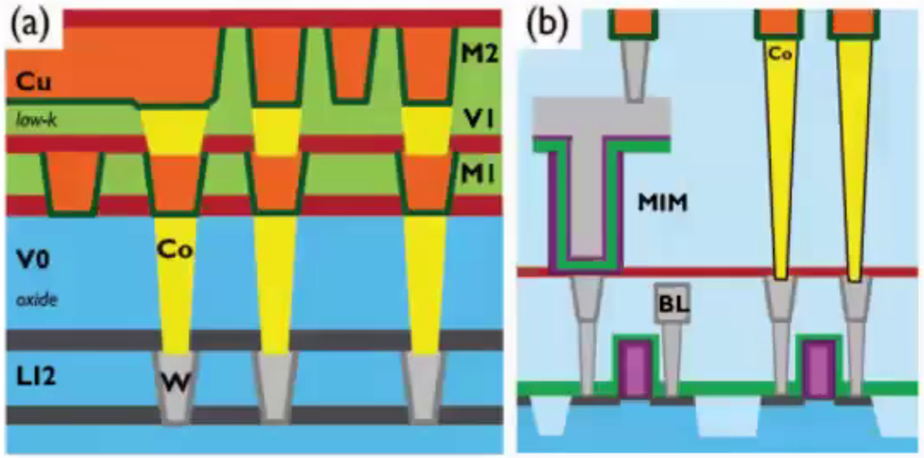

Fig. 1. Cross-sectional schematic of the Co bottom-up contact fill and via prefill for (a) logic and (b) Co in high AR ratio (AR 10) contacts in a DRAM memory bitcell. Co electroless can be used for fill on W or on Cu.

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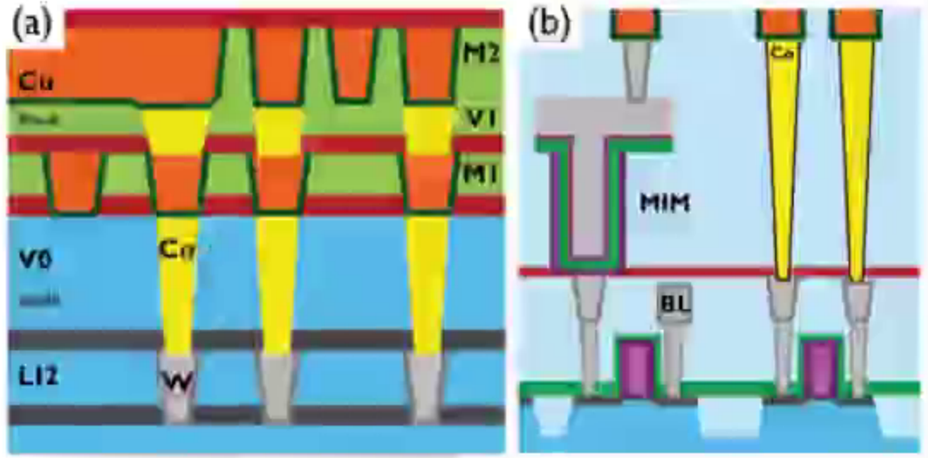

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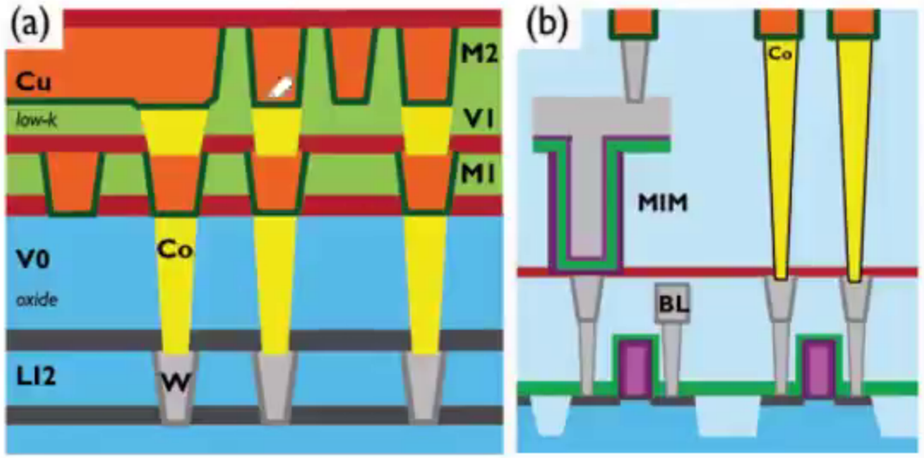

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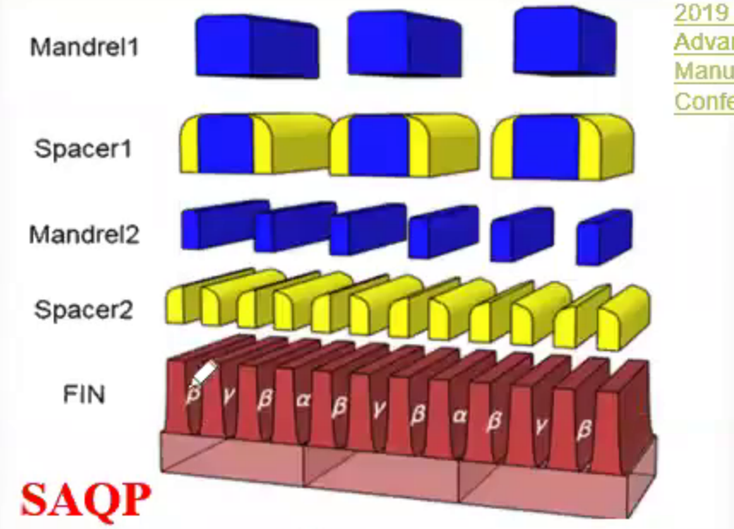
- Multi-patterning (x星/英x爾的軟肋??)
- 多重图形（Multiple patterning）是指一种在半导体制造过程中的技术，使用了多重图形曝光增强鰭電晶體密度(右圖SAQP)
  - SQDP 製程產生缺陷的概率(例如 pitch walk) >> EUV
- 台積大量應用了EUV，使得他的對SAQP 的需求，比其他對手要少得多，所以他的良率為第一



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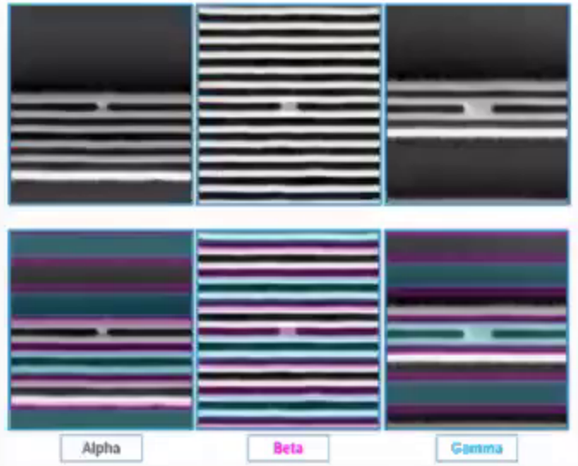

回味: Pitch Walk issues in SAQP

- **Pitch Walk:** 硅鰭最後形成的位置竟然不是在預定的位置，而是位移了數納米(如右圖所示)
- 不要小看這小小位移，不小心良率就玩完了(因為以後的製程都會受到嚴重打擊)

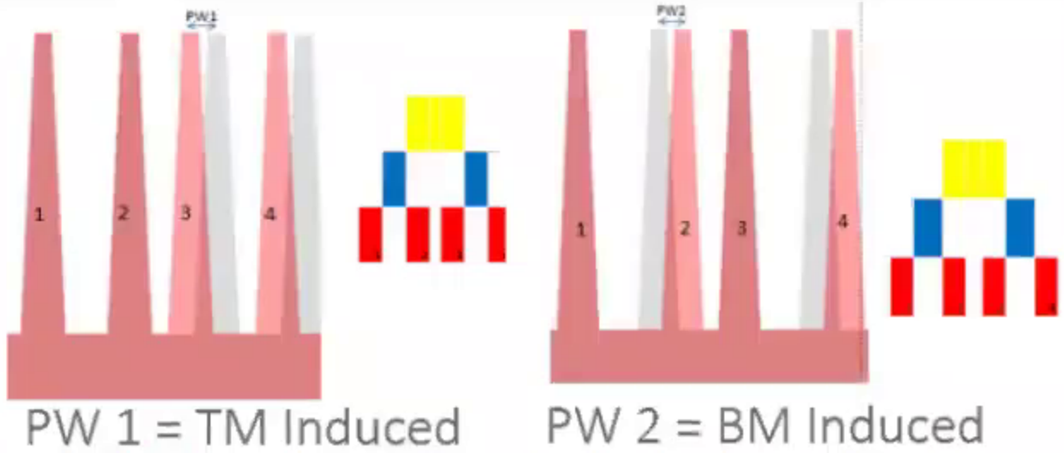

Figure 8 Pitch walk 1 and 2 are referenced to fins 1 and 2, and 1 and 3, respectively

Advanced in-line metrology strategy for self-aligned quadruple patterning, Chao et al,
Proceedings Volume 9778, Metrology, Inspection, and Process Control for Microlithography 2016

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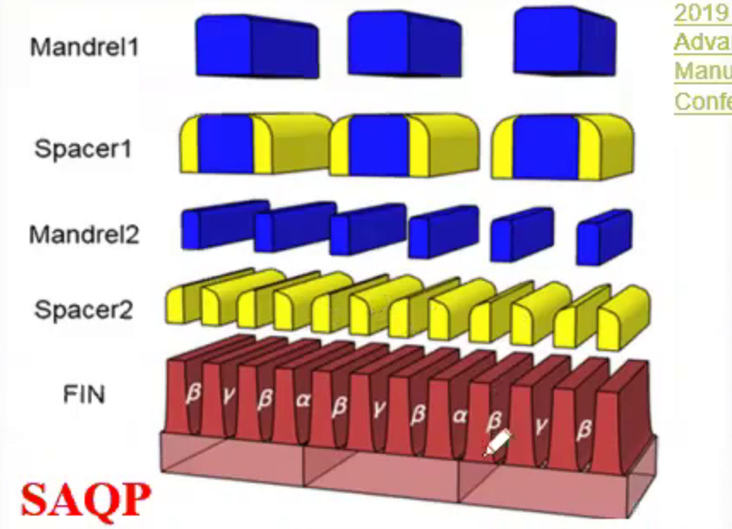

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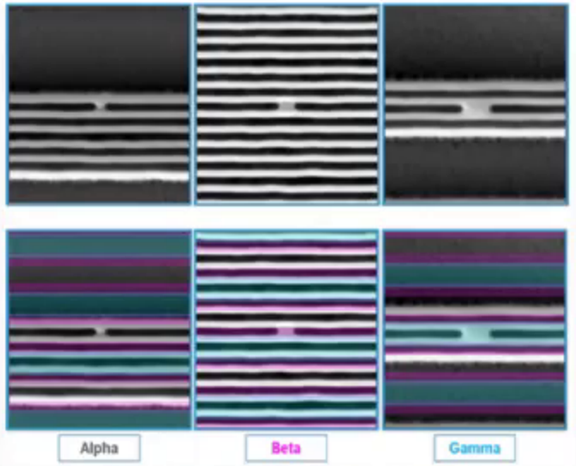
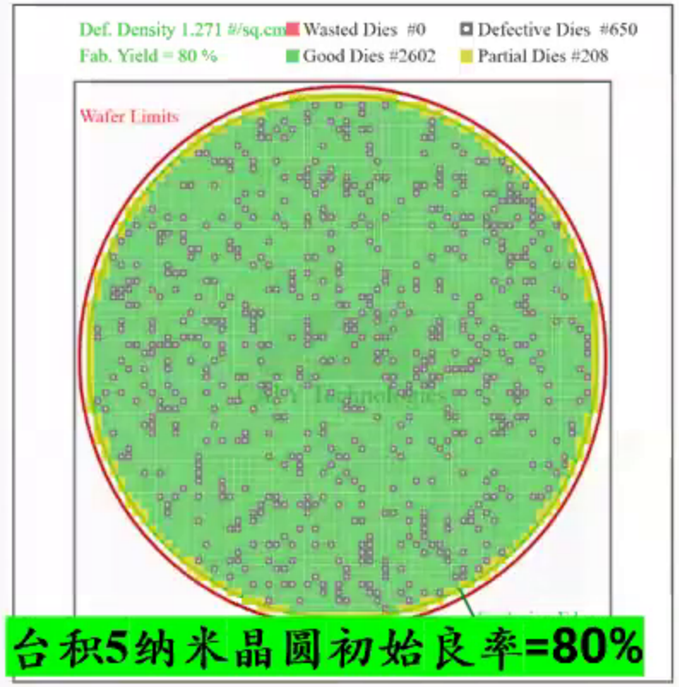


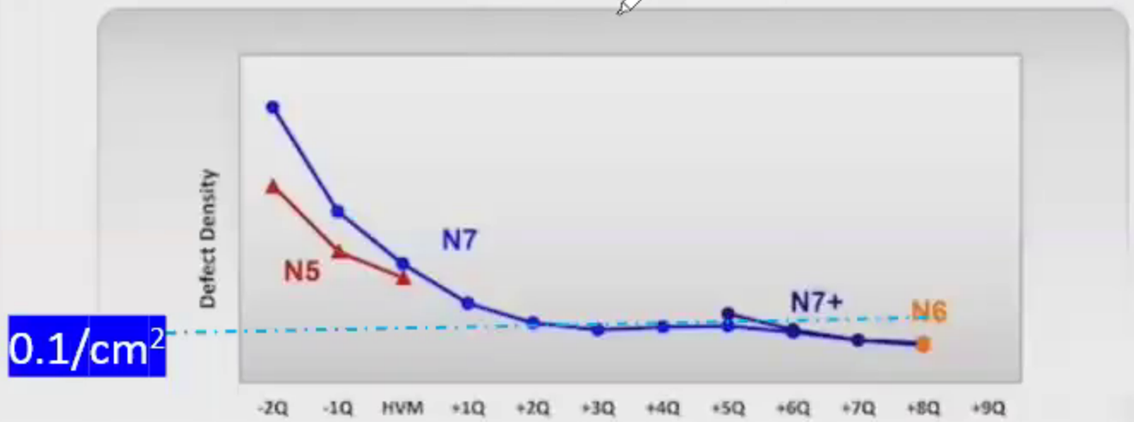
台积5纳米晶圆初始良率嚇嚇叫

- 世界級 DD (defect density) = 0.5/cm^2
  - 台积量產時 DD ~ 0.1/cm^2
    - NVidia 10: ~**80%** Yield
      Zen2 Chiplet: ~**94%** Yield



台积5纳米晶圆初始良率=80%

- N5 offers 15% faster speed, 30% less power and 1.8X logic density over N7
- N5 product D0 performance is progressing ahead of N7
- N5P extends additional 5% speed gain and 10% power enhancement over N5



https://www.anandtech.com/show/16028/better-yield-on-5nm-than-7nm-tsmc-update-on-defect-rates-for-n5

Anything below 0.5/cm^2 is usually a good metric, and we've seen TSMC pull some interesting numbers, such as 0.09 / cm^2 on its N7 process node only three quarters after high volume manufacturing

https://www.anandtech.com/show/15219/early-tsmc-5nm-test-chip-yields-80-hvm-coming-in-h1-2020

教課書良率理論們

- 這只是基本功，是”必要”但"非充分”的

Negative binomial

$$Y_r = \frac{1}{\left(1 + \frac{AD_0}{\alpha}\right)^{\alpha}}$$

Murphy

$$Y_r = \left(\frac{1 - e^{-AD_0}}{AD_0}\right)^2$$

Bose-Einstein

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Seeds

$$Y_r = e^{-\sqrt{AD_0}}$$

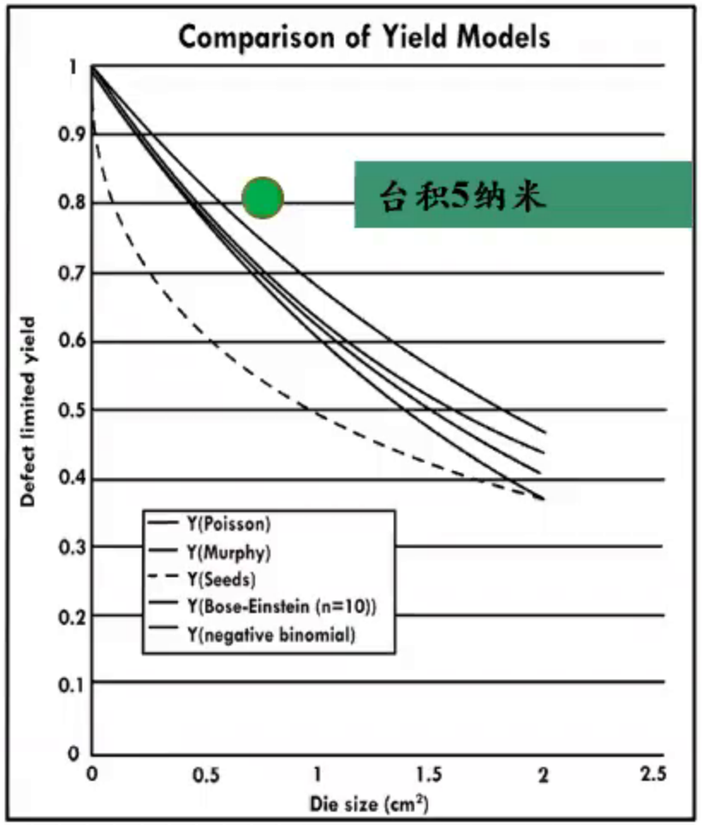
Poisson

$$P(k) = \frac{\lambda^k k e^{-\lambda}}{k!}$$

$$Y_r = P(0) = e^{-\lambda} = e^{-AD_0}$$

$$Y_r = \int_0^{\infty} F(D) e^{-AD} d$$

- **ITRS 建議使用以上Negative-Binomial (NB) distribution 產生的良率公式**



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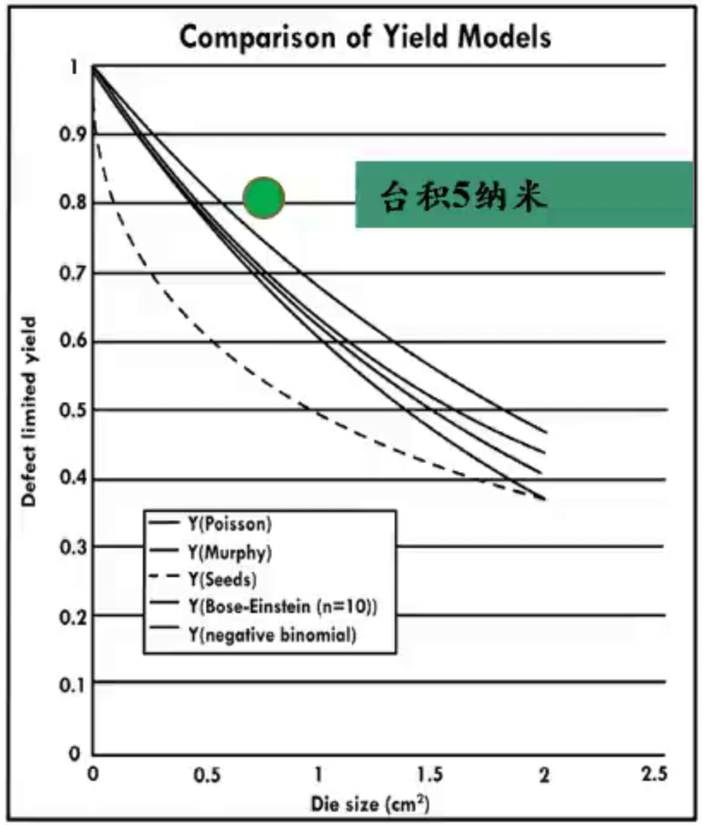

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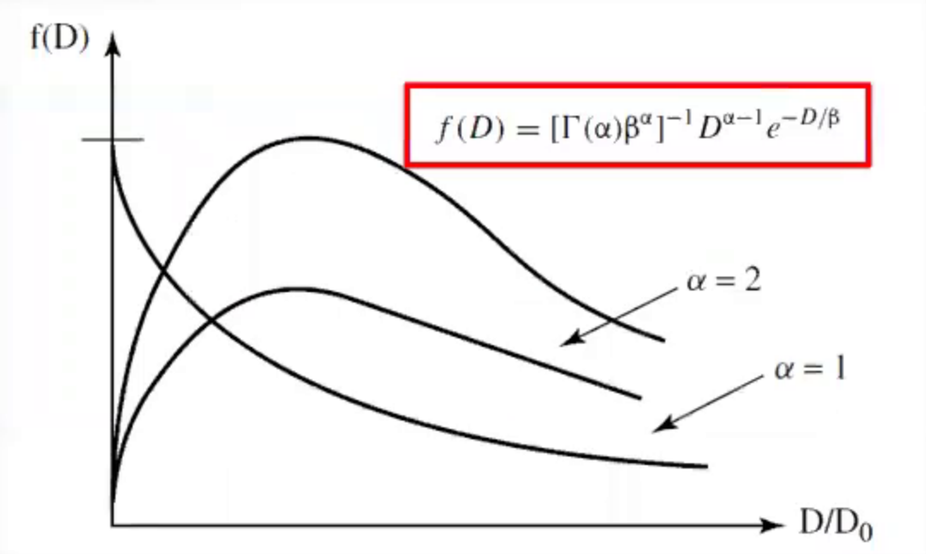
教課書良率理論: NB良率推演

- 良率 $Y = f(A_c, D)$
  - D = defect density
  - Ac = critical area (in which a defect occurring has a high probability of resulting in a fault), "缺陷必殺區" (例如指數分布如下)
  - Murphy 建議良率 Y如下:

$$Y = \int_0^{\infty} e^{-A_c D} f(D) dD$$

  - Okabe建議 f(D)如下:

$$f(D) = [\Gamma(\alpha)\beta^{\alpha}]^{-1} D^{\alpha-1} e^{-D/\beta}$$



Negative binomial

$$Y_r = \frac{1}{\left(1 + \frac{AD_0}{\alpha}\right)^{\alpha}}$$

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  - 0.8 = exp(-1cm*1cm*D_0)
  - ∴ D_0= - ln(0.8) = 0.223/cm^2

- 解答:
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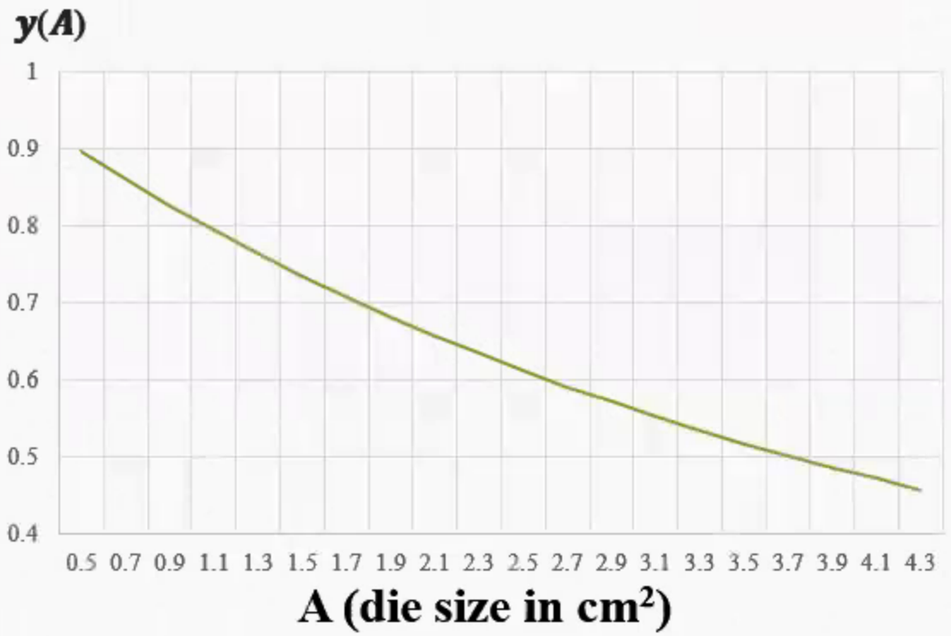

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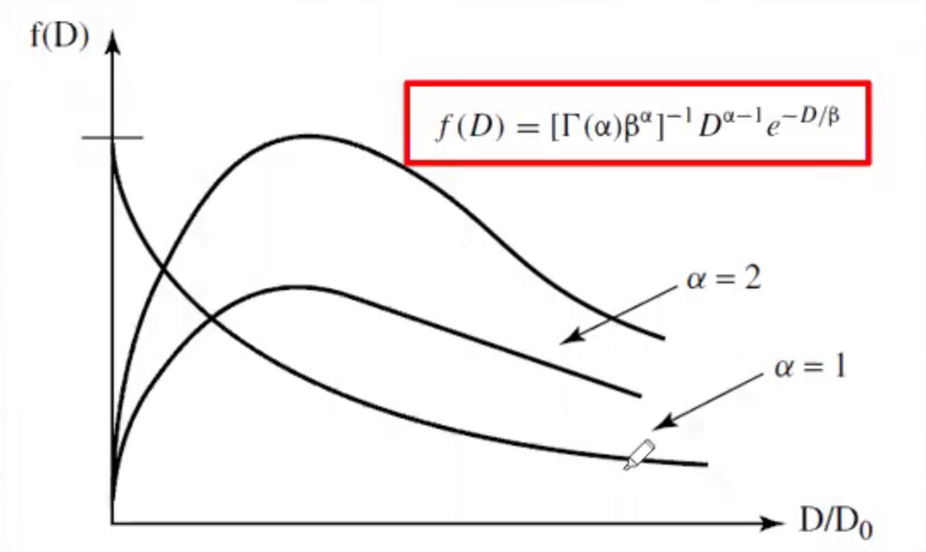

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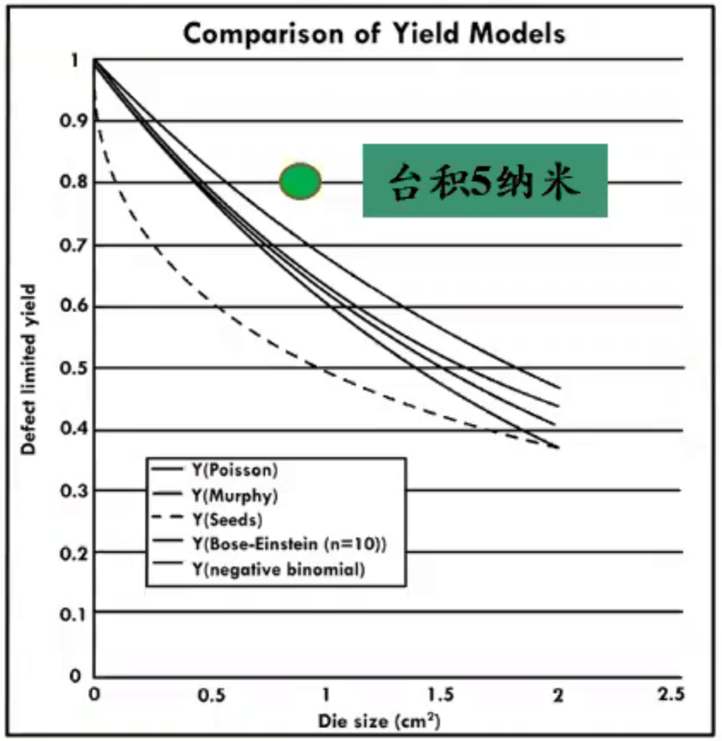
芯片越大，良率越低

芯片尺寸 vs 良率

- FPGA (Xilinx, VU19P)芯片超大 = 9cm²
  - 良率非常低，一個300mm晶圓只能得到一個或數個芯片，所以要價極高
- 有人建議小chiplet 概念，好做，便宜，良率也高
  - 見右圖，die size越小，良率越高
  - 例如magnetic hard drive的晶片極小，所以制程根本就不怕defects，因為良率天生超高



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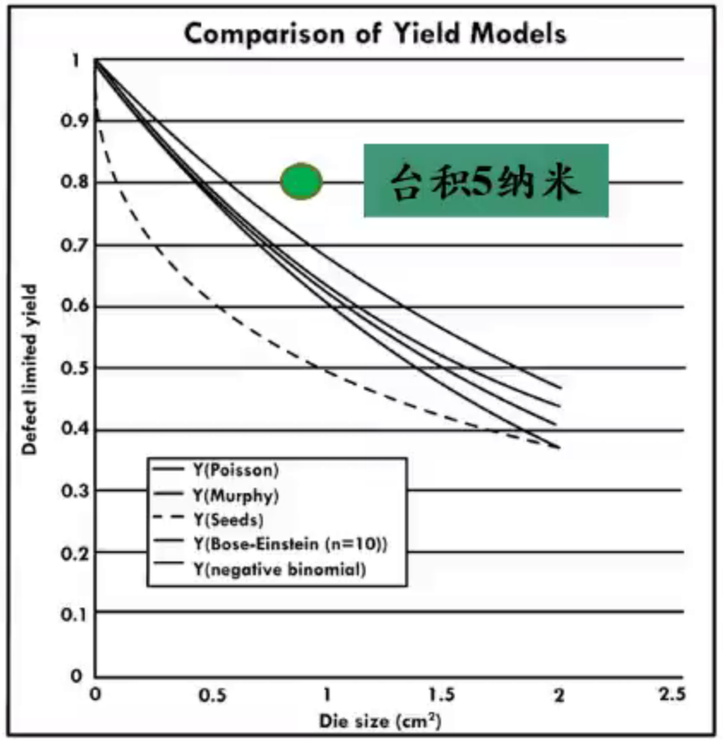

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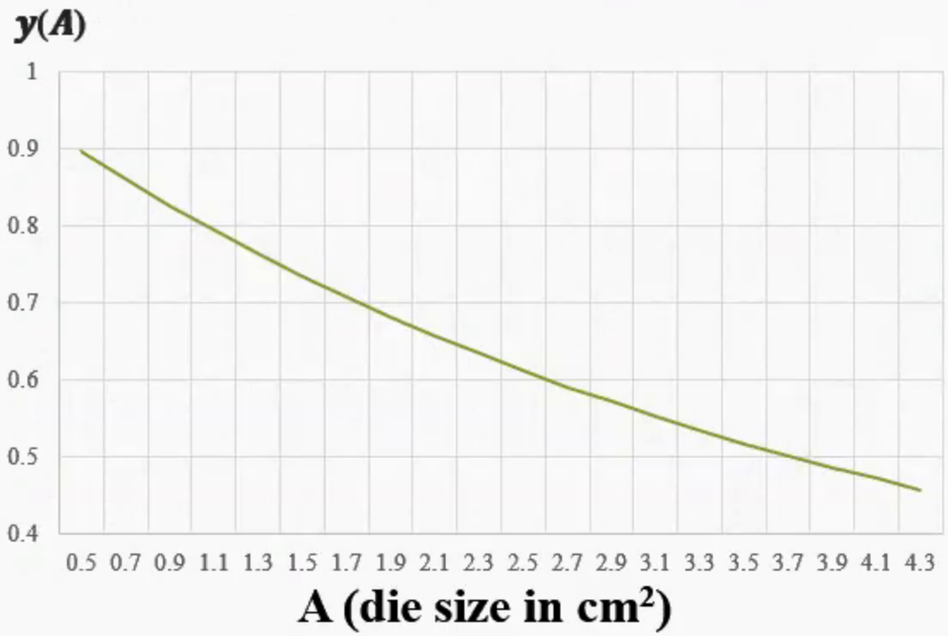
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