

FDSOI

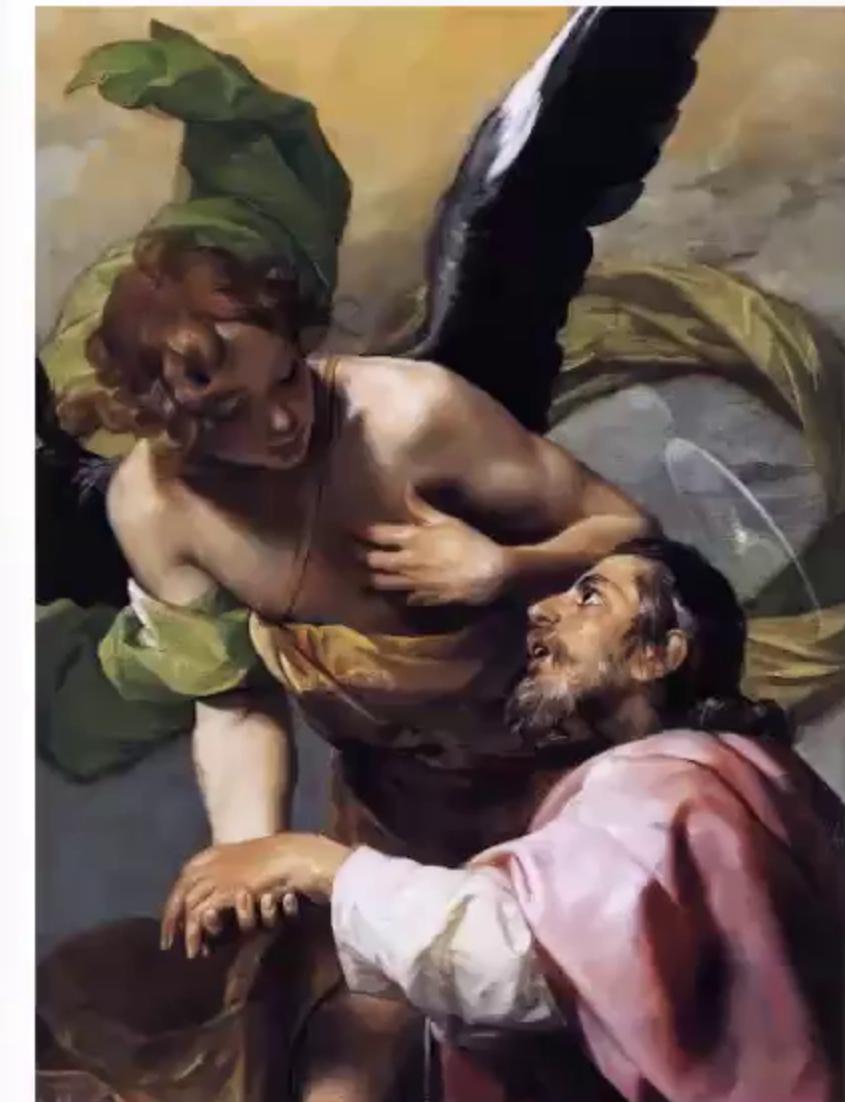
魔鬼制程挑戰之一

Tsi, Lg Limits and sigma Vt

王不老說半导

魔鬼數字χξς與66大順

- <启示錄>有提到所謂的魔鬼數字χξς (666 也，希臘數字 $\chi = 600, \xi = 60$ and $\varsigma = 6$)，其發音為(kai, zai, sigma)
- A=100、B=101，如此類推，希特勒的姓「HITLER」加起來就等於666
- 66大順卻是吉利(粵語「六」同「祿」音)，送36元紅包，取其禮輕意重
 - $1+2+3+4+5+6+\dots+36$ 總和= 666
- 在FDSOI制程的世界哩，又有哪些魔鬼數字呢？



Angel of the Revelation by Alonso Cano

納米魔鬼數字之一：4

試問：當鳍腰圍Dfin太瘦，竟也有不育傾向，此魔鬼數字為何？

解答：4nm也

- Yu發現硅鳍表面電位變化($\Delta\Psi_s$)與鳍腰圍有嚴重親密關係如右
- 此乃因硅原子已很少(見下頁)，量子離散(discrete)效應越來越顯著之故
- 右圖顯示，5nm時， $\Delta\Psi_s$ 已現其獠牙，到了4nm，芯電晶体已經狀似瘋癲，無法正常運作了

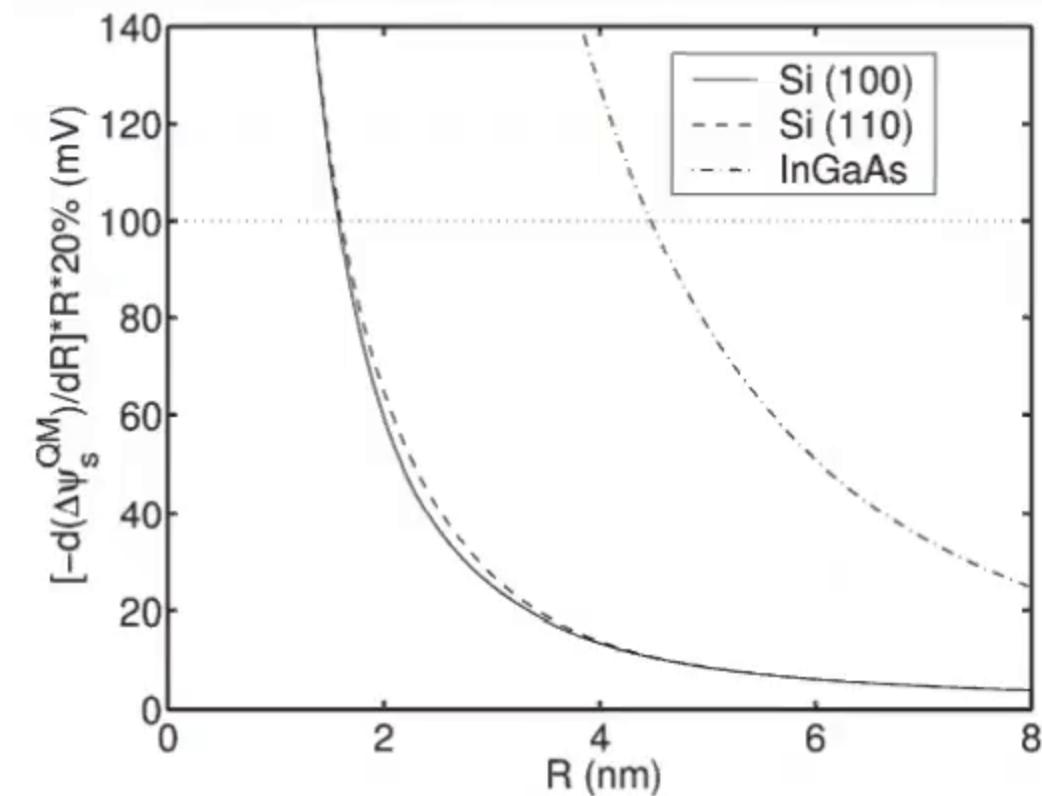


Fig. 7. Model-predicted total variation of $\Delta\psi_s^{QM}$, $[-d(\Delta\psi_s^{QM})/dR] \times (20\% \cdot R)$, for nanowire nMOSFETs as functions of R , based on an assumption of $\pm 10\%$ variation of R . Nanowires with both orientations for silicon and InGaAs are compared.

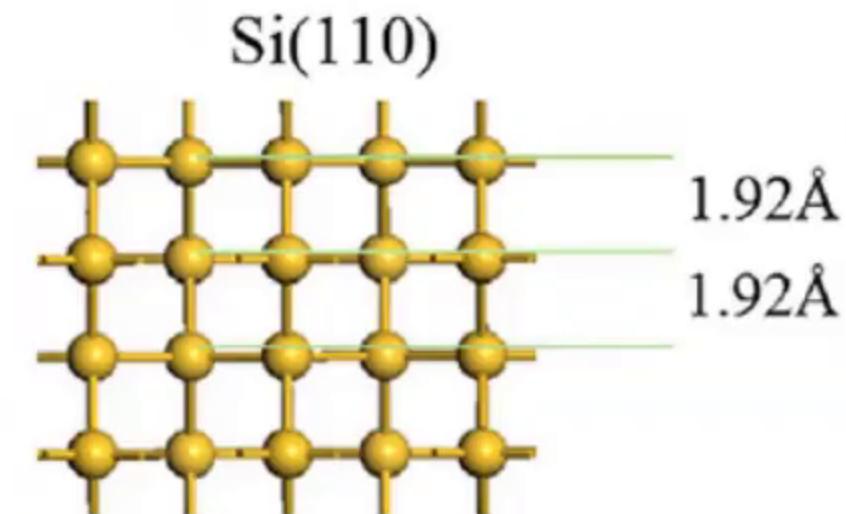
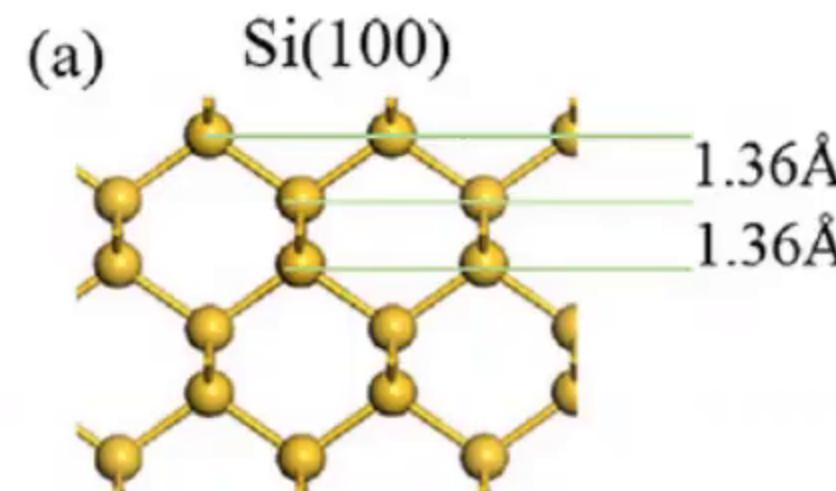
- Yu et al, Scaling of Nanowire Transistors, TED'08, 55(11)11, p.2846-2858,

納米魔鬼數字之一：4

試問：當鍍腰圍 = 4nm，其中含有多少硅原子層？

解答：~ 21 層

- interplanar spacing of Si(100) and Si(110) are 1.36 Å and 1.92 Å
- $40/1.92 \sim 21$ layers



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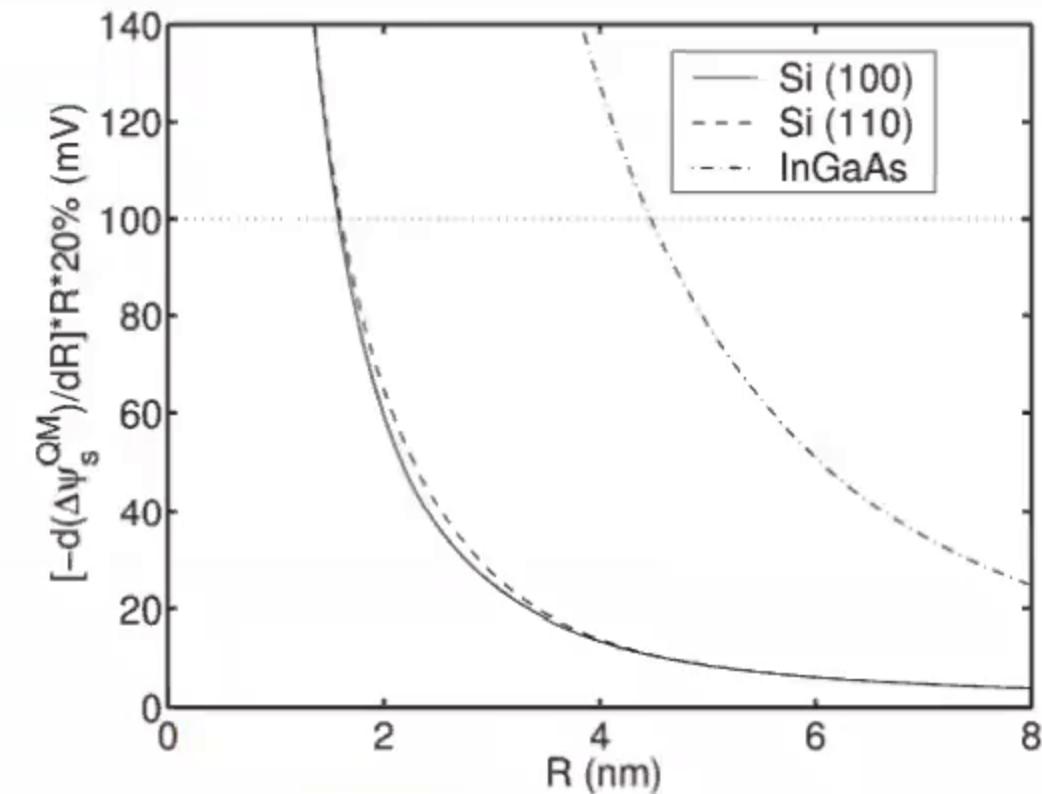


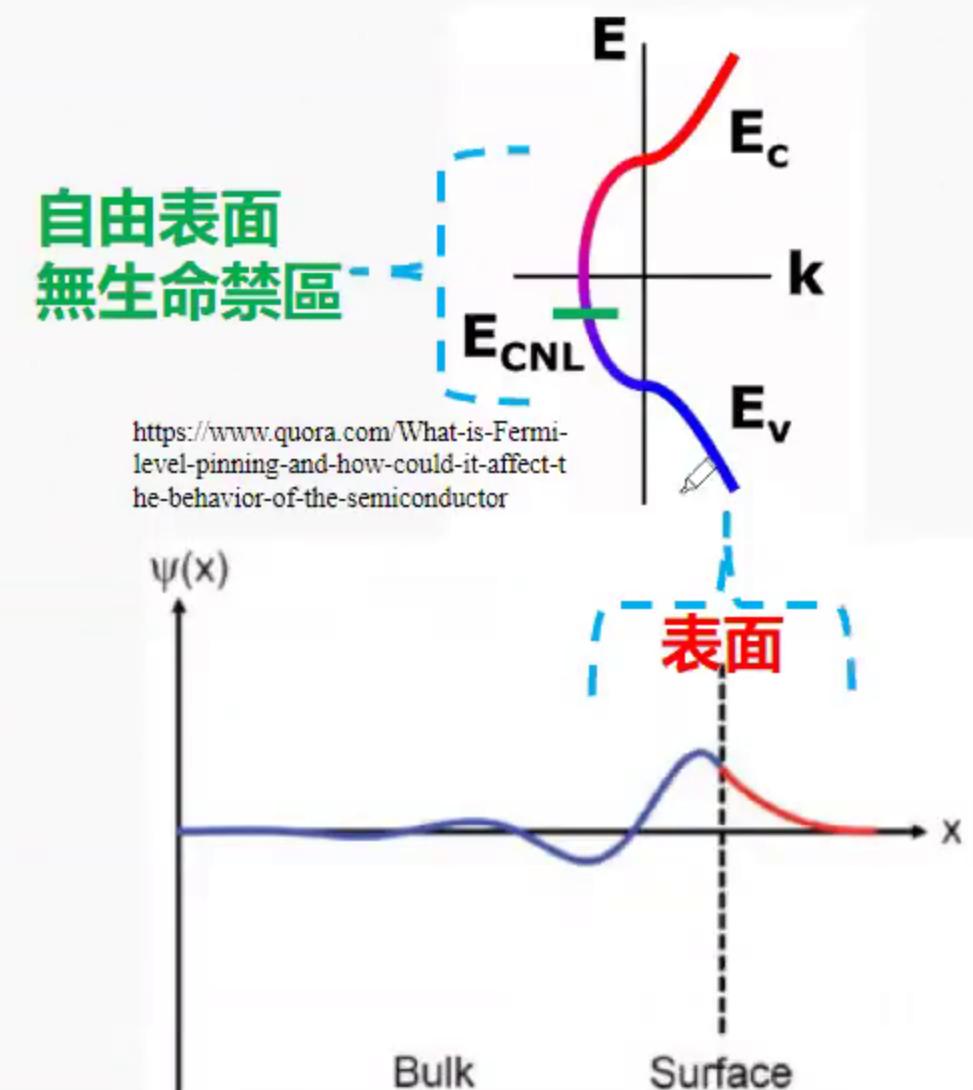
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試問： $k \cdot p$ 之自由表面變異結果為何？

解答：Eg觀念為CNL取代

- **自由表面扭曲了 $k \cdot p$ 天地法則：**當晶格的周期結構在表面終止時，電子必重建特定於表面的電子狀態(以降低系統表面能量)
- 电子波在表面附近达到顶峰，振幅从表面向外真空和晶体內以指數方式衰減(見右下圖)
- 原來電荷不可存活的生命禁區Eg，在半导(甚至絕緣體)的自由表面上，竟有了能階連續概念(如右上圖)，而且有一個新管家叫做馮道CNL



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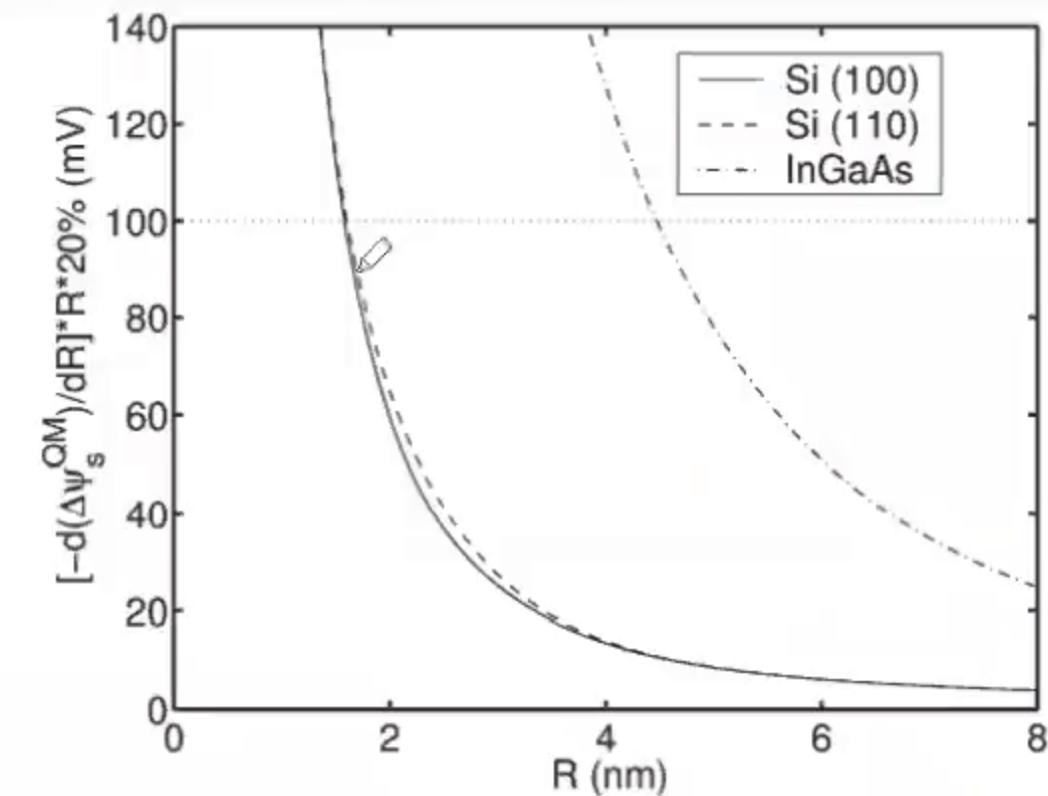
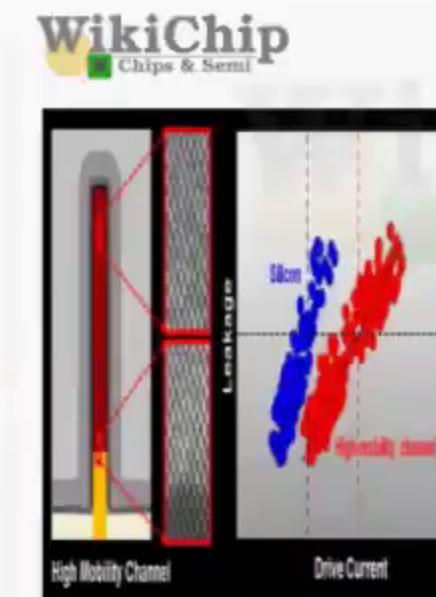
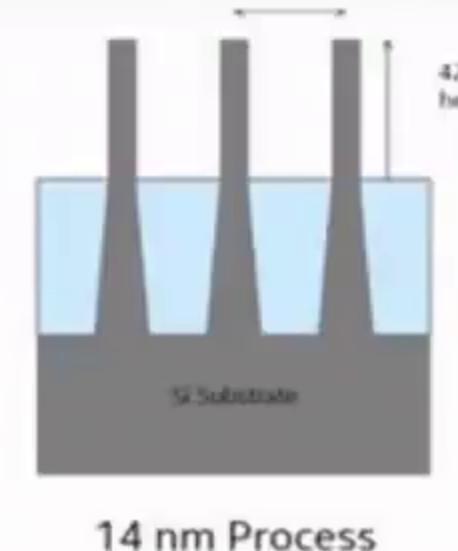
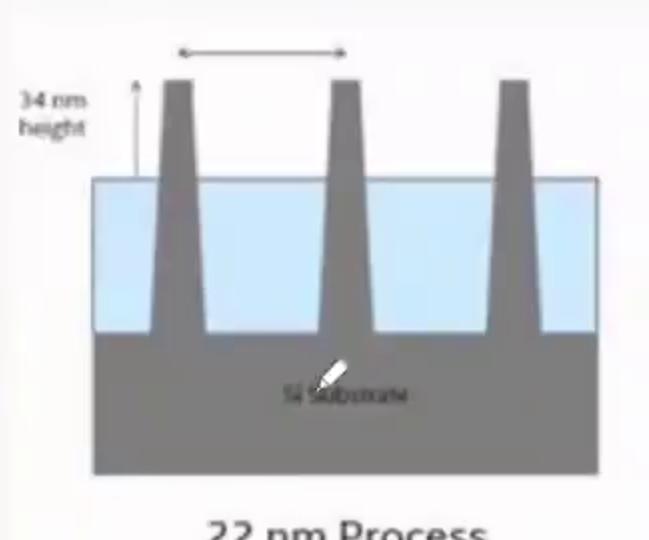


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楚王好细腰，宫中多饿死

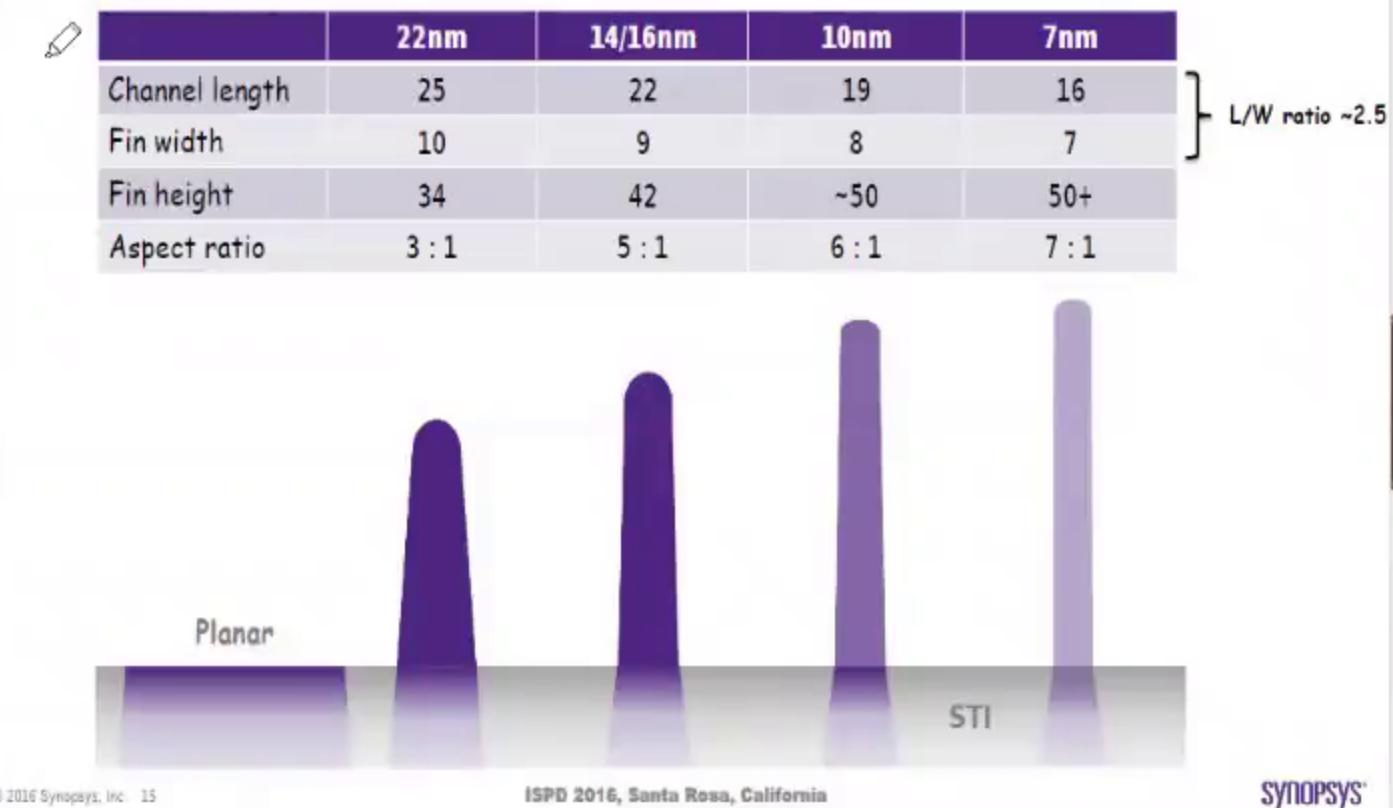
- 汉成帝愛妃赵飞燕瘦不贏骨，但因服用息肌丸減肥太過，竟然絕育
- 在硅納米鳍式场效应晶体管 (FinFET)的世界哩，人人皆是汉成帝，他們對鳍的腰圍(曰之Dfin)有嚴格要求，基本上，當然是越細越好，因為如此可更容易掌控，得以減少所謂的SCE(short channel effect)，例如左下圖所示，硅納米鳍由矮胖必須進步到高瘦，右下圖中為TSMC五納米鳍腰，更是瘦到嚇死人



硅鰭魔鬼數字: 4x90

- 硅鰭的厚度有極限(~4nm)，而且其與電性有效通道長度(**Leff**)的比值 ~ **2.5**
- 電性有效通道長度極限為 $Leff = 2.5 \times 4 = 10\text{nm}$ (硅鰭芯片物理极限之一)
- 然而為了保持电流总面积 (~Fin width x fin height) 相同，Fin height $\sim 350/4 = 90\text{nm}$ (太高會駝背due to fin bending from dummy gate)
- **fin limit = 4nm x 90nm**

Fin Shape Evolution

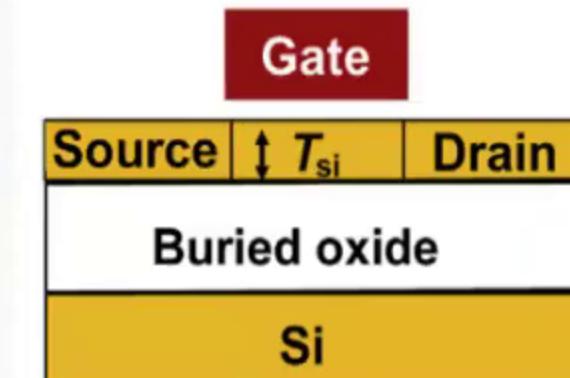


<https://www.fool.com/investing/2016/05/24/a-note-on-intel-corporation-and-manufacturing-tech.aspx>

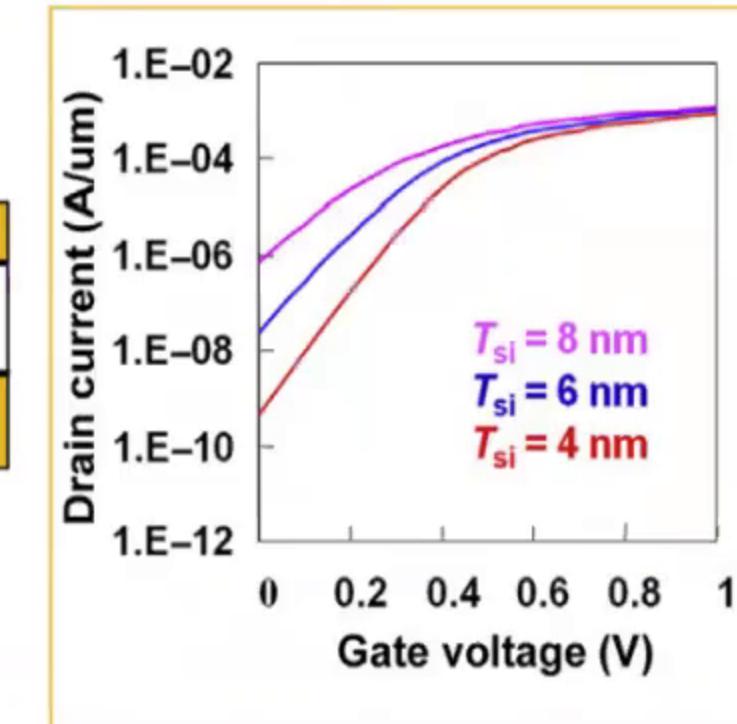
FDSOI的魔鬼數字：4x10

- FDSOI ~ 躺著的FinFET
- 但FDSOI卻有不同的scaling rule如右上公式所示
 - $T_{\text{ox}}(\epsilon_{\text{si}}/\epsilon_{\text{ox}}) \sim 0.5 \text{ nm}$ (極限)
 - 右下图指出 T_{Si} 與 I_{off} 的關係 (彼此之間，相差近百倍)
- $\Rightarrow L_g > 2 + 4T_{\text{Si}} = 10 \text{ nm}$
- 其實 $L_g = 10 \text{ nm}$ 也是FFT的極限

$$T_{\text{si}} + T_{\text{ox}} \left(\frac{\epsilon_{\text{si}}}{\epsilon_{\text{ox}}} \right) < \frac{L_g}{4}$$



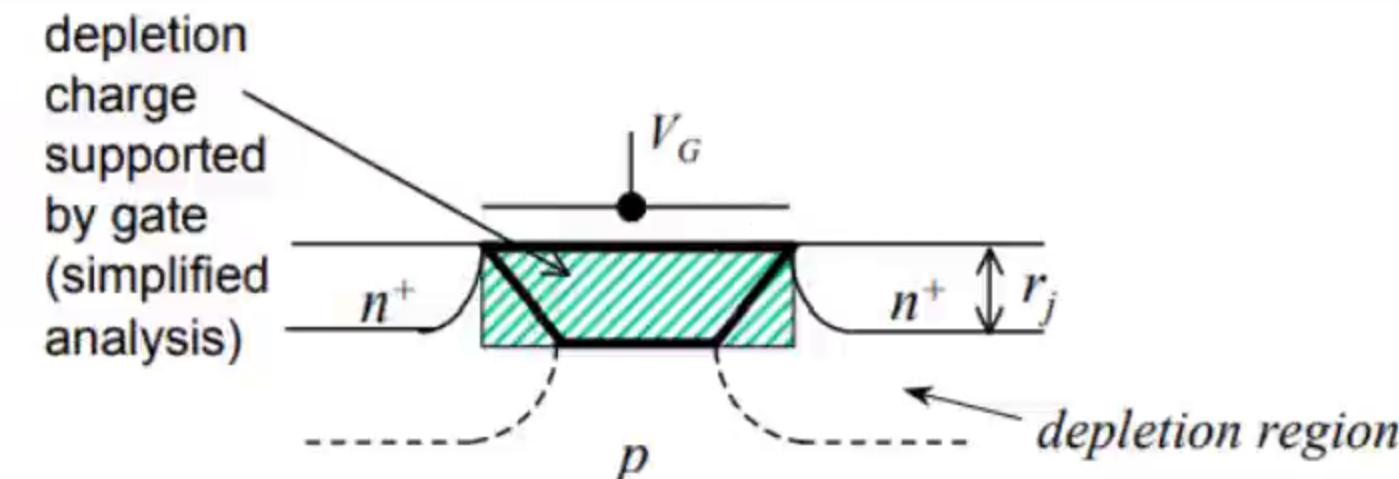
25 nm Lg FDSOI



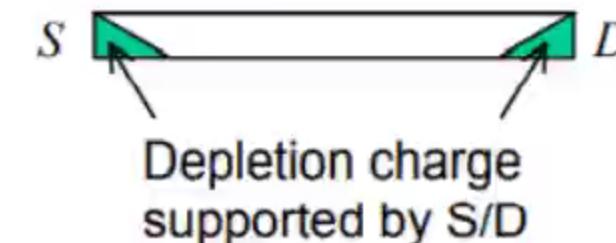
Industry Standard FDSOI Compact Model BSIM-IMG for IC Design,
CHENMING HU et al, 2019

魔鬼一： L_g 越小，S/D燈下黑比例越嚴重

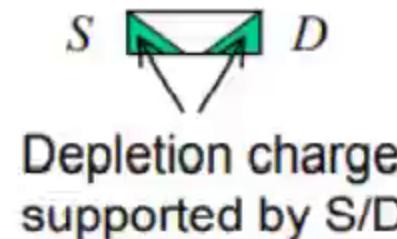
- 簡單的說，MOSFET就是用 Gate來控制硅通道的開關
- 但是S/D是燈下黑(右圖中的綠色部分)，偷偷來搶Gate的控制權
- 當 L_g 大的時候，Gate控制力道還足，但是當 L_g 越小的時候，對S/D的巧取豪奪，就漸有些力有未逮之感了
- SCE = short channel effect



Large L:



Small L:

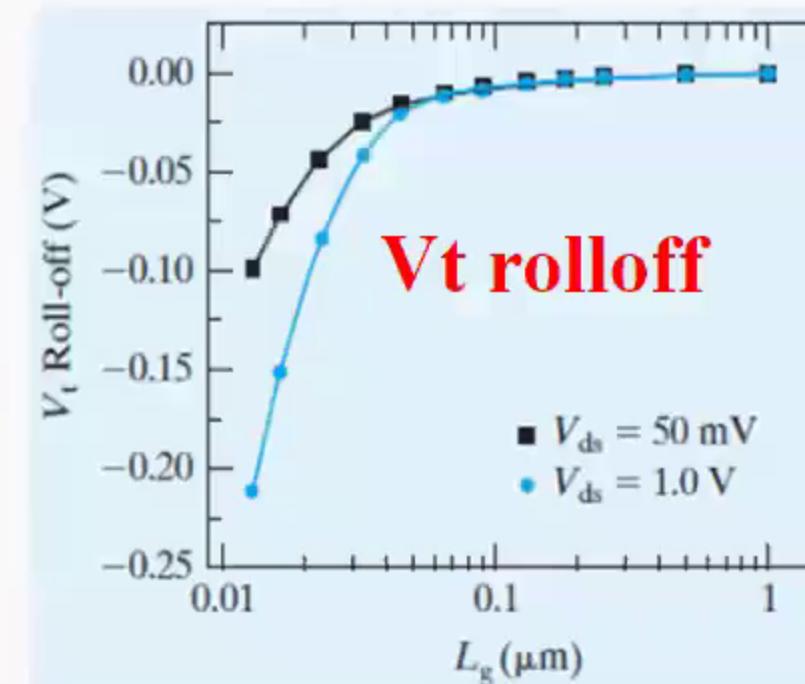


Spring 2003

EE130 Lecture 26, Slide 4

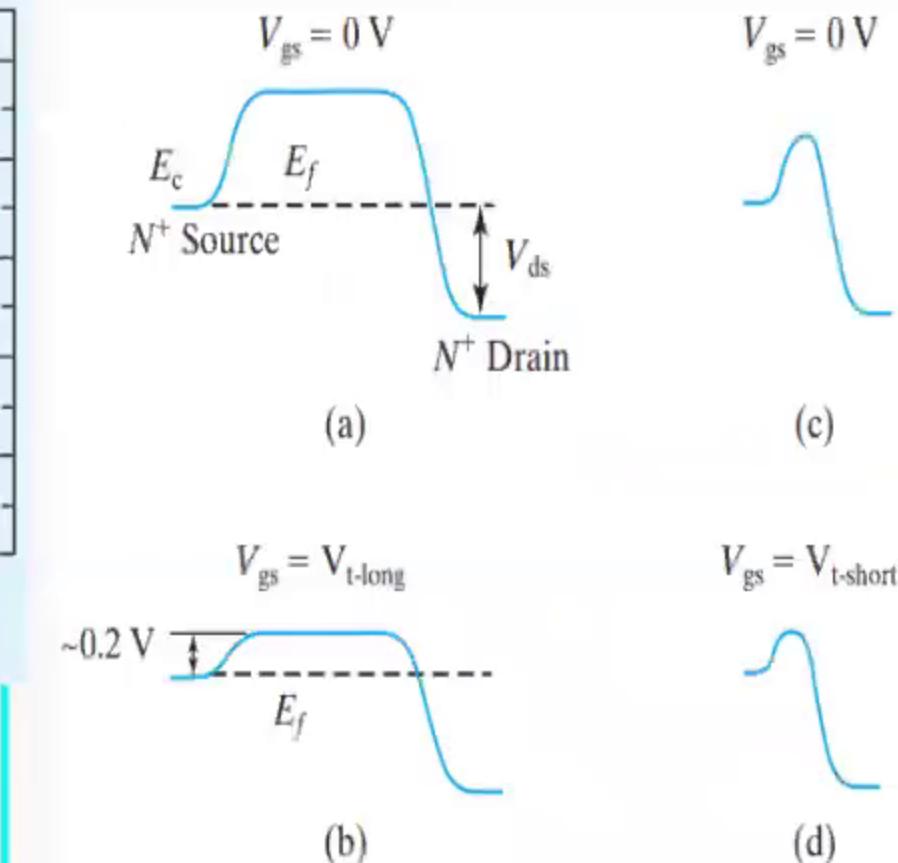
魔鬼二: L_g 越小，被D扯後腿也越嚴重

- V_{gs} 控制硅通道，但 D 却愛扯後腿， V_{ds} 明目張膽來搶 V_{gs} 的控制权
- 當 L_g 大的時候， V_{gs} 控制力道還足，但是當 L_g 越小的時候，對 V_{ds} 的巧取豪奪，有未逮之感
- V_t 受衝擊而变小，向零趨近 → **Vt rolloff**



$$V_t = V_{t-long} - (V_{ds} + 0.4 \text{ V}) \cdot e^{-L/l_d}$$

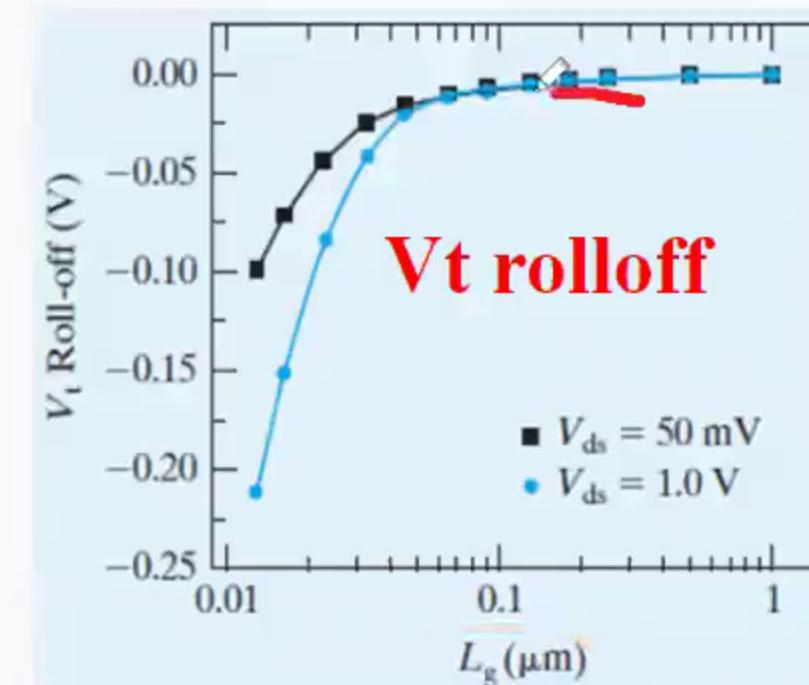
$$l_d \propto \sqrt[3]{T_{oxe} W_{dep} X_j}$$



Modern Semiconductor Devices for Integrated Circuits
 by Chenming Hu

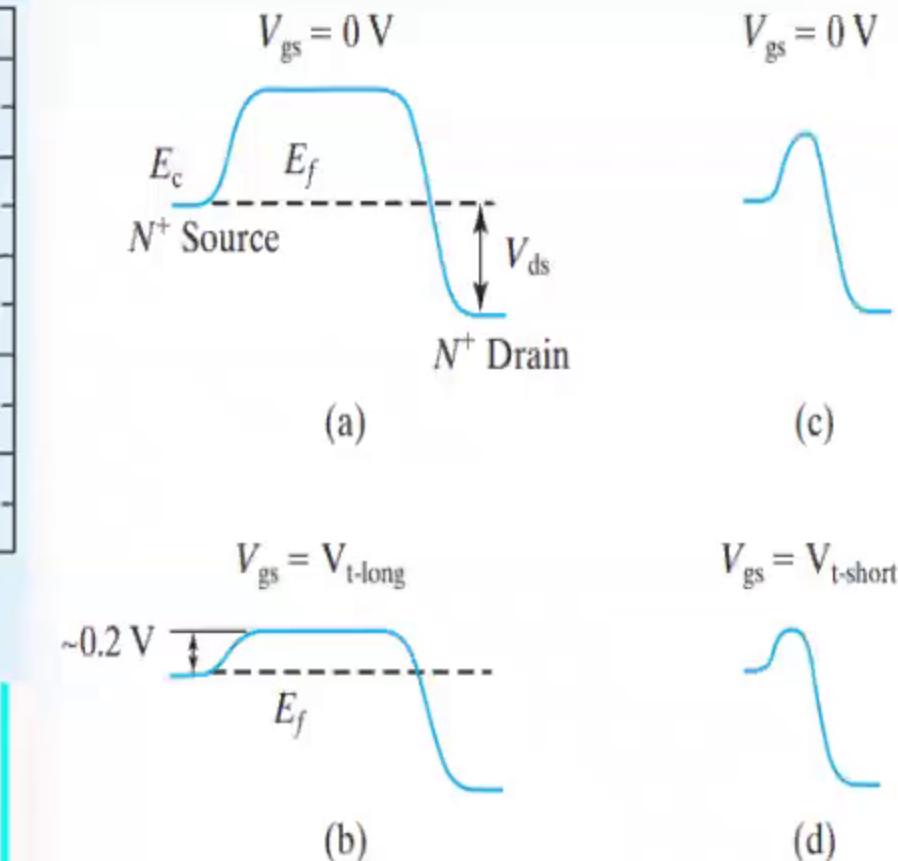
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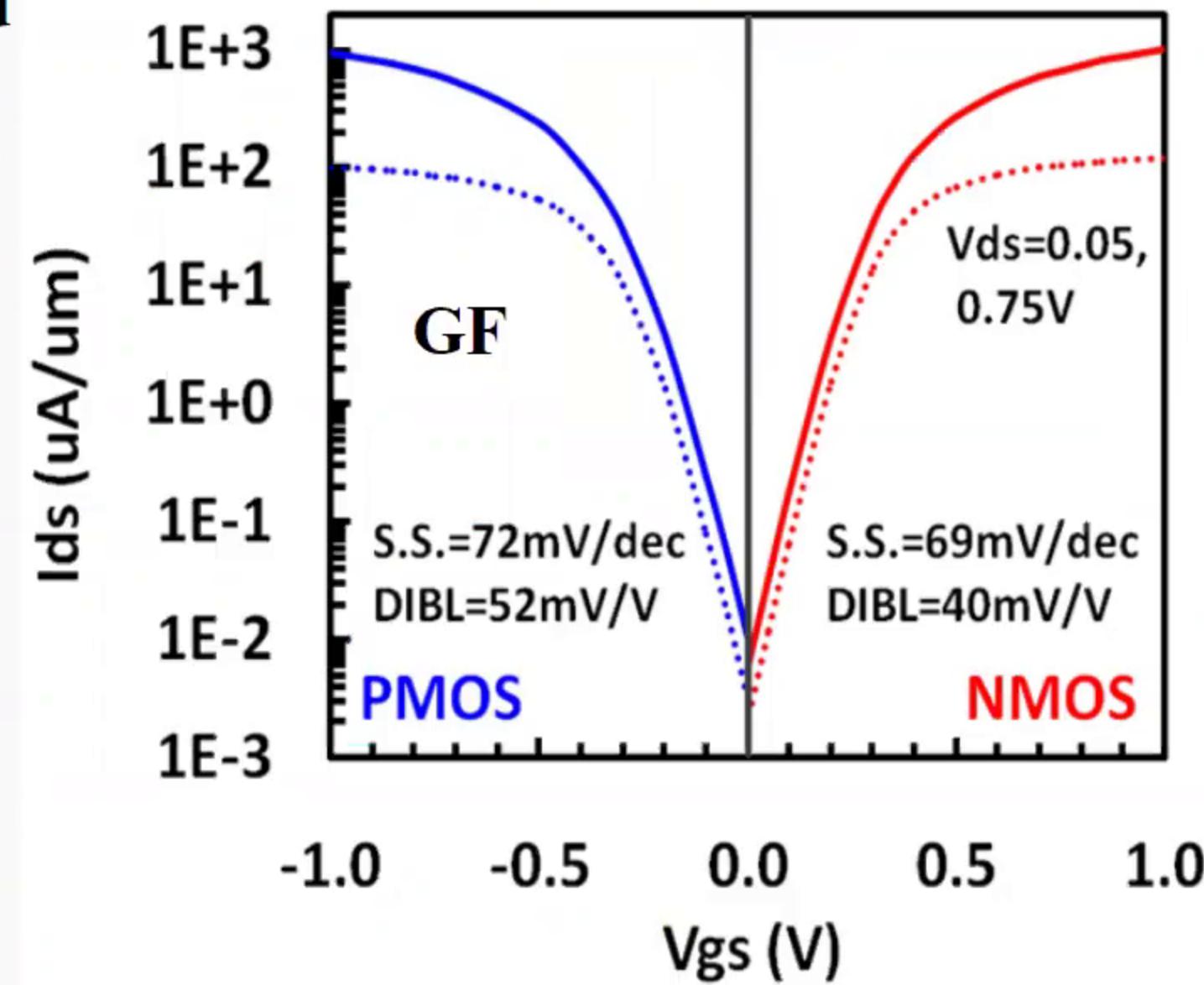
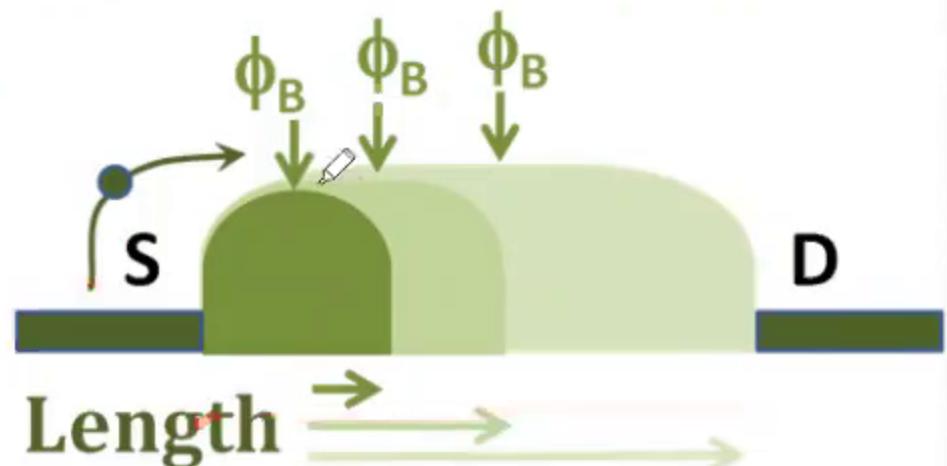
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Modern Semiconductor Devices for Integrated Circuits
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魔鬼二：看圖作文DIBL

- DIBL= 相對於小Vd，被大Vd 拉開的程度
- = 在小Vg~0區中，實線與虛線的間距 / (大Vd-小Vd)
- = $36\text{mV}/(0.75-0.05)\text{V} = 52\text{mV/V}$



https://en.wikipedia.org/wiki/Drain-induced_barrier_lowering

魔鬼二：不過Tsi越小，竟越難被D扯後腿

- DIBL(drain induced barrier lowering) 與芯片架構有關，比較右表中 FDSOI與FinFet，與Tsi與 $T^2\text{si}$ 相關，值得注意的是：

DIBL(FFT) < DIBL(FDSOI)

- DIBL也會直接影響芯

$$\frac{\Delta f}{f} = -\frac{2\text{DIBL}}{V_{DD} - V_{Th}}$$

$$\begin{aligned}\text{Conventional DIBL} &= 0.8 \frac{\epsilon_{Si}}{\epsilon_{ox}} \left(1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{ds} \\ \text{FDSOI DIBL} &= 0.8 \frac{\epsilon_{Si}}{\epsilon_{ox}} \left(1 + \frac{T_{Si}^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{Si}}{L_{el}} V_{ds} \\ \text{FinFET DIBL} &= 0.8 \frac{\epsilon_{Si}}{\epsilon_{ox}} \left(1 + \frac{T_{Si}^2/4}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{Si}/2}{L_{el}} V_{ds}\end{aligned}$$

Doris et al, *Fully Depleted Devices FDSOI and FinFET*, in Micro And Nanoelectronics Emerging Device Challenges and Solutions, Tomasz Brozek, 2015,

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- DIBL也會直接影響芯速度如下：

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魔鬼二：而Tbox越小，也越難被D扯後腿

- DIBL也與FDSOI的Box厚度(Tbox)有關，值得注意：
- Tbox越薄，DIBL也越小
- 目前Tbox約為15-25nm

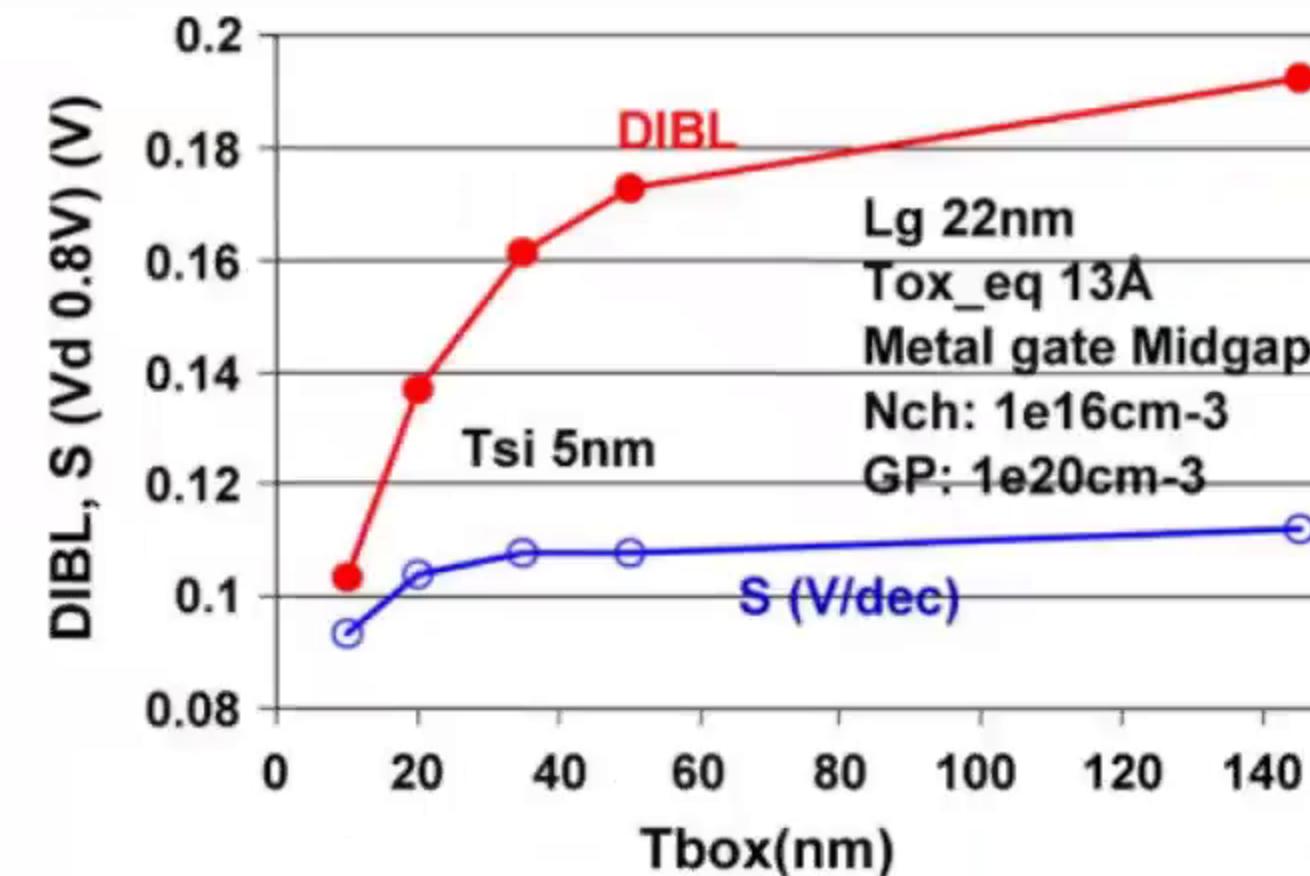
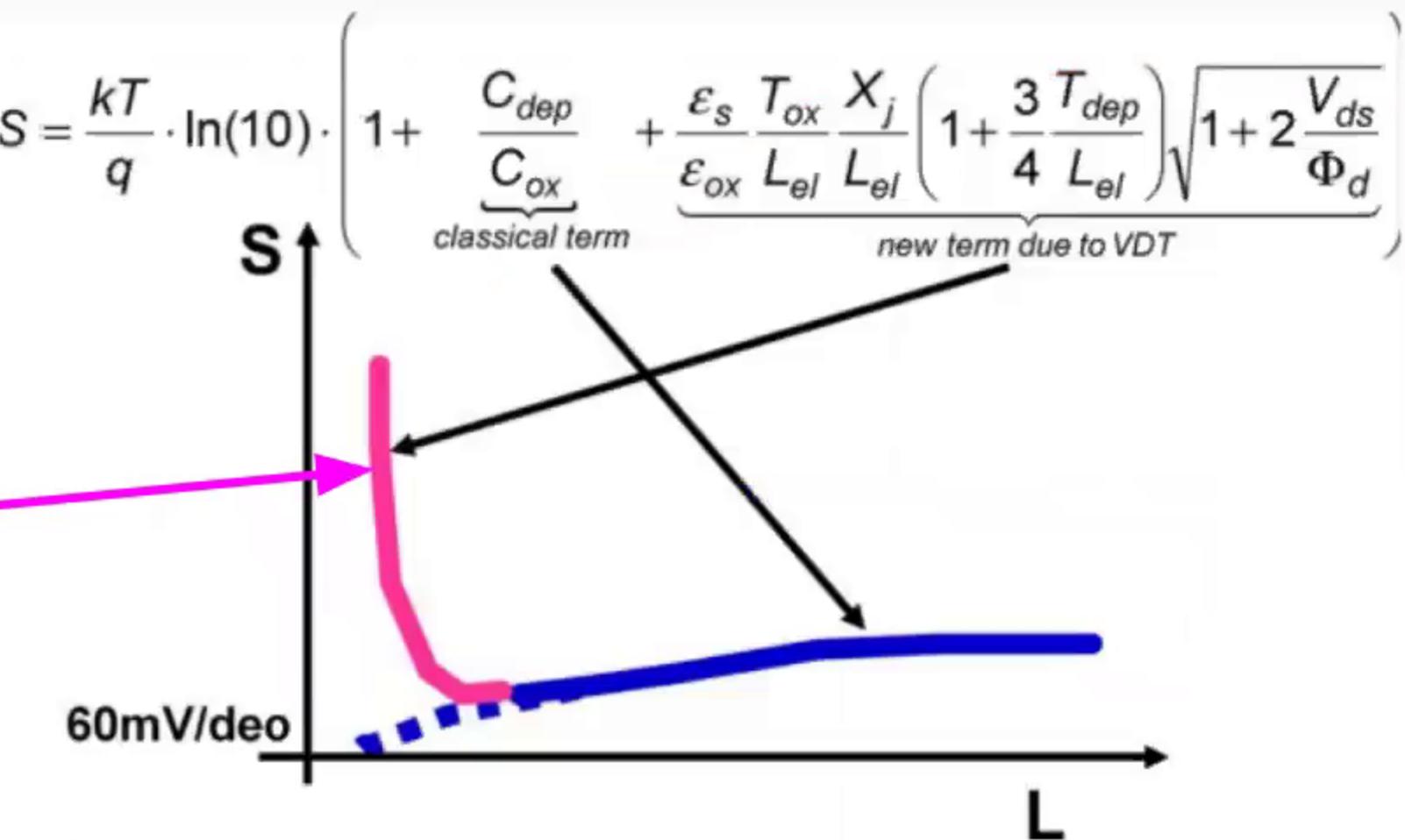
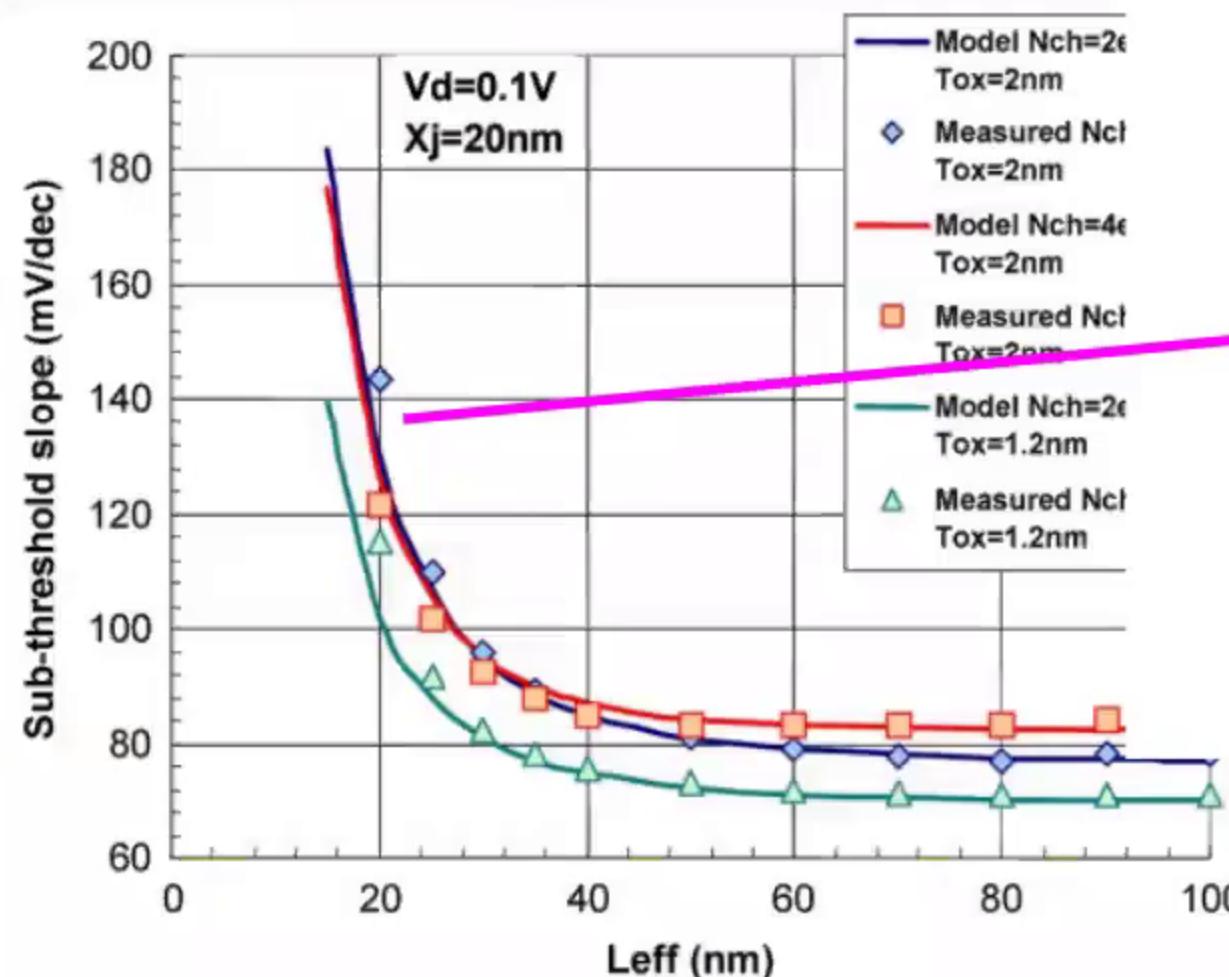


Fig. 31. Dependence of DIBL and S on BOX thickness in UTB devices, as

Skotnicki et al, Innovative Materials, Devices, and CMOS Technologies for Low-Power Mobile Multimedia, TED'08, 55(1)96-130

魔鬼三： L_g 越小，SS會越瘋狂上翹

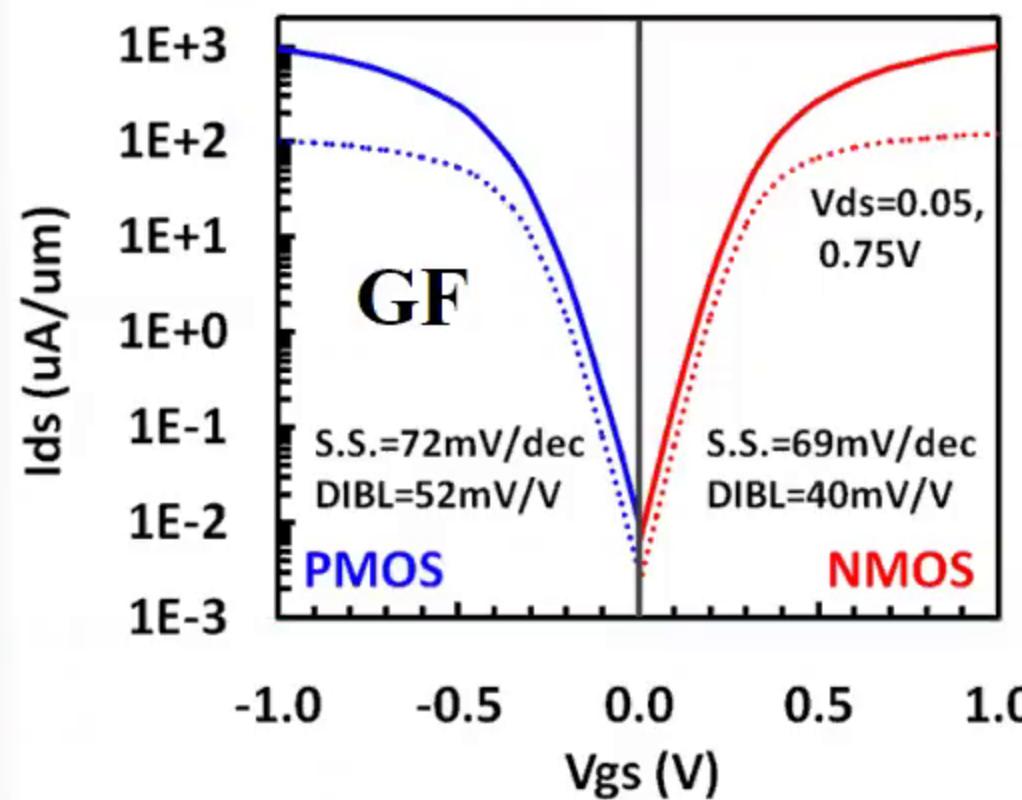
- 當 L_g 越小的時候，如右圖所示，SS突然往上翹



Skotnicki et al, Innovative Materials, Devices, and CMOS Technologies for Low-Power Mobile Multimedia, TED'08, 55(1)96

三魔鬼的綜合影响→ $I_{off} \uparrow$

- L_g 越小的時候，漏电流 I_{off} 大幅增加
- 右图顯示，DIBL比SCE嚴重，所以一般報導芯片表現時，都以DIBL與SS為主



$$EI = \left(1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox_el}}{L_{el}} \frac{T_{dep}}{L_{el}}$$

$$EIS = \frac{T_{ox_el}}{L_{el}} \frac{X_j}{L_{el}} \left(1 + \frac{3}{4} \frac{T_{dep}}{L_{el}} \right)$$

$$DIBL = 0.80 \frac{\epsilon_s}{\epsilon_{ox}} EI \times V_{ds}$$

$$SCE = 0.64 \frac{\epsilon_s}{\epsilon_{ox}} EI \times \Phi_d$$

$$\text{Log } I_{off}[A] = \log I_{th}[A] - (V_{th\infty} - SCE - DIBL)/S$$

魔鬼死舞：FFT/NS/NW/FDSOI

- 對 L_g 的極限，有以下共識：

FFT:

$$\frac{F_{si}}{2} + T_{ox} \left(\frac{\varepsilon_{si}}{\varepsilon_{ox}} \right) < \frac{L_g}{4}$$

FDSOI:

$$T_{si} + T_{ox} \left(\frac{\varepsilon_{si}}{\varepsilon_{ox}} \right) < \frac{L_g}{4}$$

- 但其實以上二者都差不多，真正決定 L_g 的極限其實是 σV_t
- 右圖顯示， $L_g < 12\text{nm}$ 時， σV_t 已經大的受不了

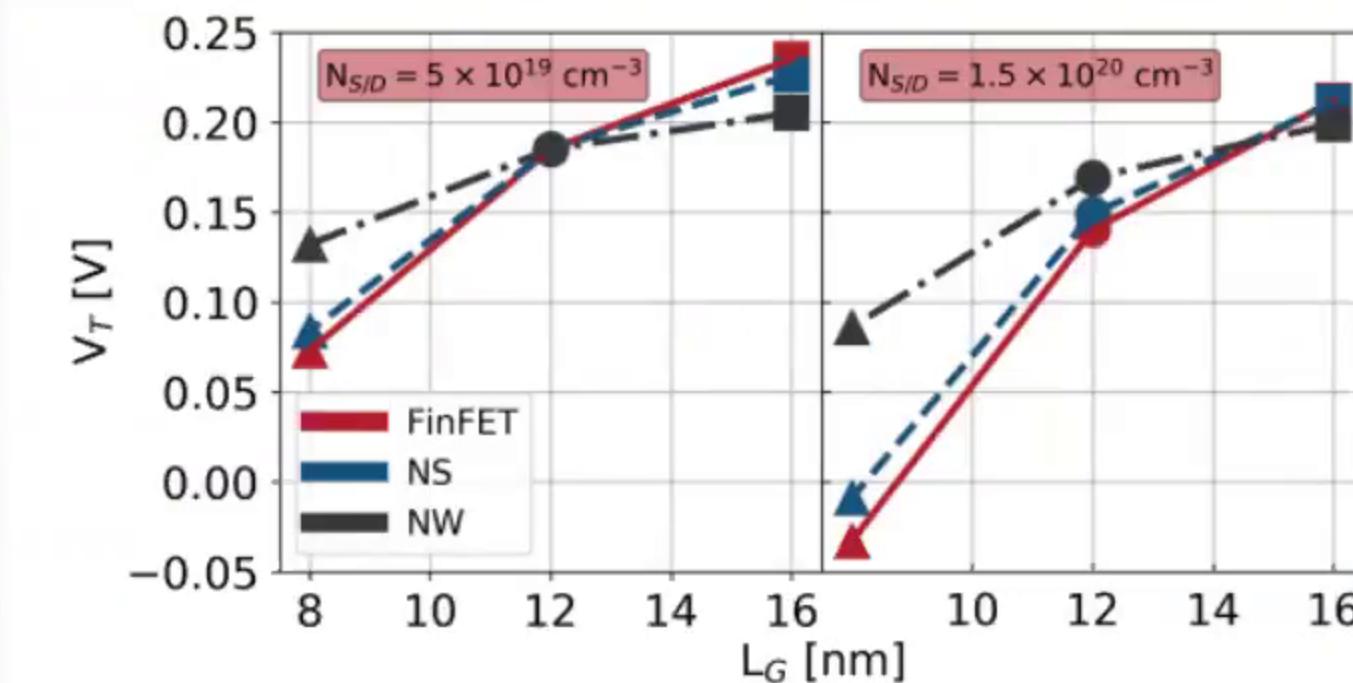
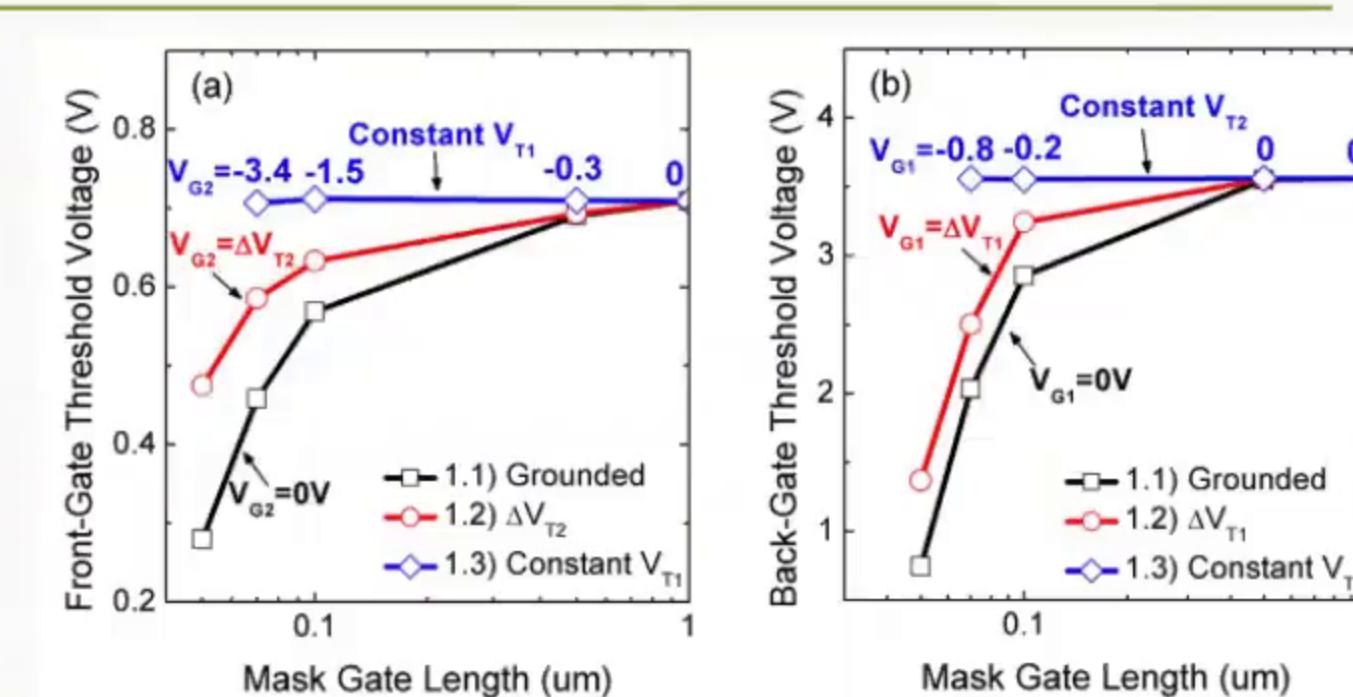


FIGURE 7: Threshold voltage (V_T) vs. gate length (L_G) for the Fin, NS and NW FETs at fixed gate metal workfunctions. The gate metal workfunctions of the three transistors are adjusted to provide the same V_T at the 12 nm gate length with $N_{S/D} = 5 \times 10^{19} \text{ cm}^{-3}$. The results are for $N_{S/D} = 5 \times 10^{19} \text{ cm}^{-3}$ (left) and $N_{S/D} = 1.5 \times 10^{20} \text{ cm}^{-3}$ (right).

FDSOI是个双面人

- FDSOI的box有上下兩個介面，此二介面(front and backside interfaces)有暗渡陳倉的額外耦合
- SCE(short channel effect)看起來會比較嚴重
- 所幸以制程與結構優化(SOA)，加上backside bias絕招，可以反敗為勝(如右图所示)



STRUCTURAL PARAMETERS OF EXPERIMENTAL DEVICES

Device	$N_A (cm^{-3})$	$t_{ox} (nm)$	$t_{Si} (nm)$	$t_{BOX} (nm)$
Non-optimized	$2 \cdot 10^{17}$	4	26	25
State-of-the-art (SOA)	10^{15}	1.12	7.8	25

The state-of-the-art transistors featured a highly doped N-type ground plane under the BOX. N_A = body doping concentration, t_{ox} = front-gate oxide thickness, t_{Si} = Si-film thickness and t_{BOX} = buried oxide thickness.

魔鬼死舞：FFT/NS/NW/FDSOI

- 對 L_g 的極限，有以下共識：

FFT:

$$\frac{F_{si}}{2} + T_{ox} \left(\frac{\varepsilon_{si}}{\varepsilon_{ox}} \right) < \frac{L_g}{4}$$

FDSOI:

$$T_{si} + T_{ox} \left(\frac{\varepsilon_{si}}{\varepsilon_{ox}} \right) < \frac{L_g}{4}$$

- 但其實以上二者都差不多，真正決定 L_g 的極限其實是 σV_t
- 右圖顯示， $L_g < 12\text{nm}$ 時， σV_t 已經大的受不了

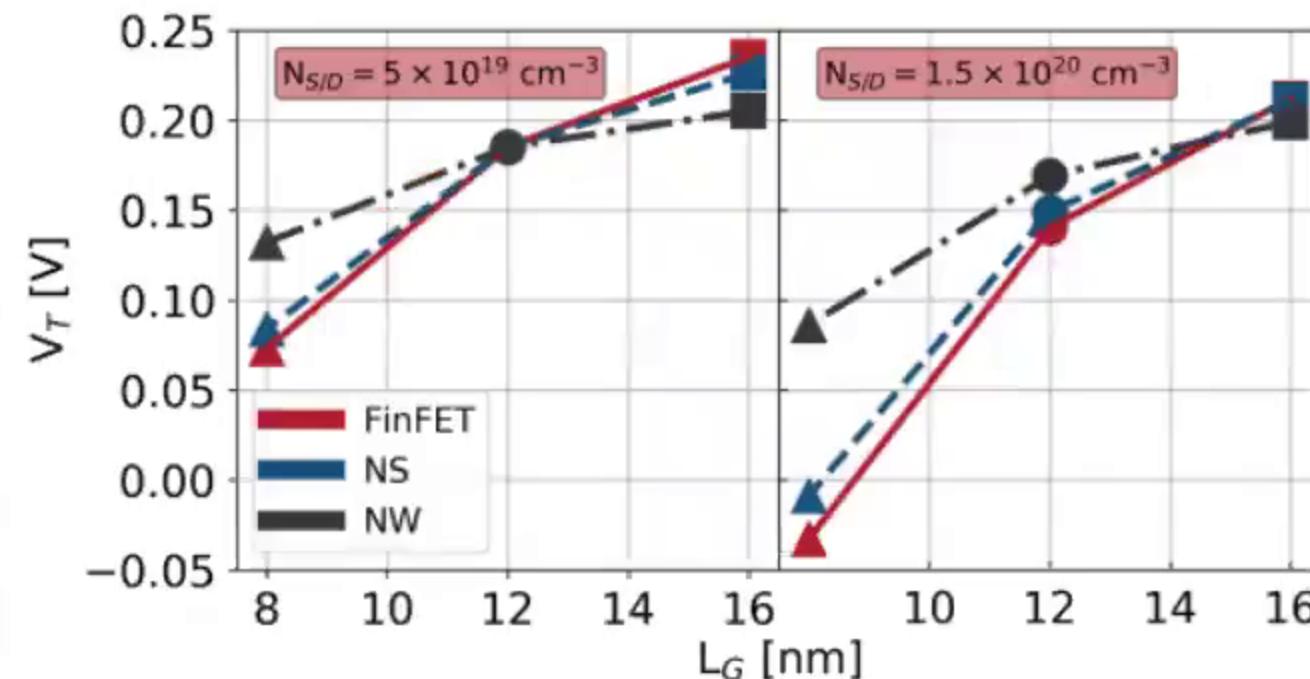


FIGURE 7: Threshold voltage (V_T) vs. gate length (L_G) for the Fin, NS and NW FETs at fixed gate metal workfunctions. The gate metal workfunctions of the three transistors are adjusted to provide the same V_T at the 12 nm gate length with $N_{S/D} = 5 \times 10^{19} \text{ cm}^{-3}$. The results are for $N_{S/D} = 5 \times 10^{19} \text{ cm}^{-3}$ (left) and $N_{S/D} = 1.5 \times 10^{20} \text{ cm}^{-3}$ (right).

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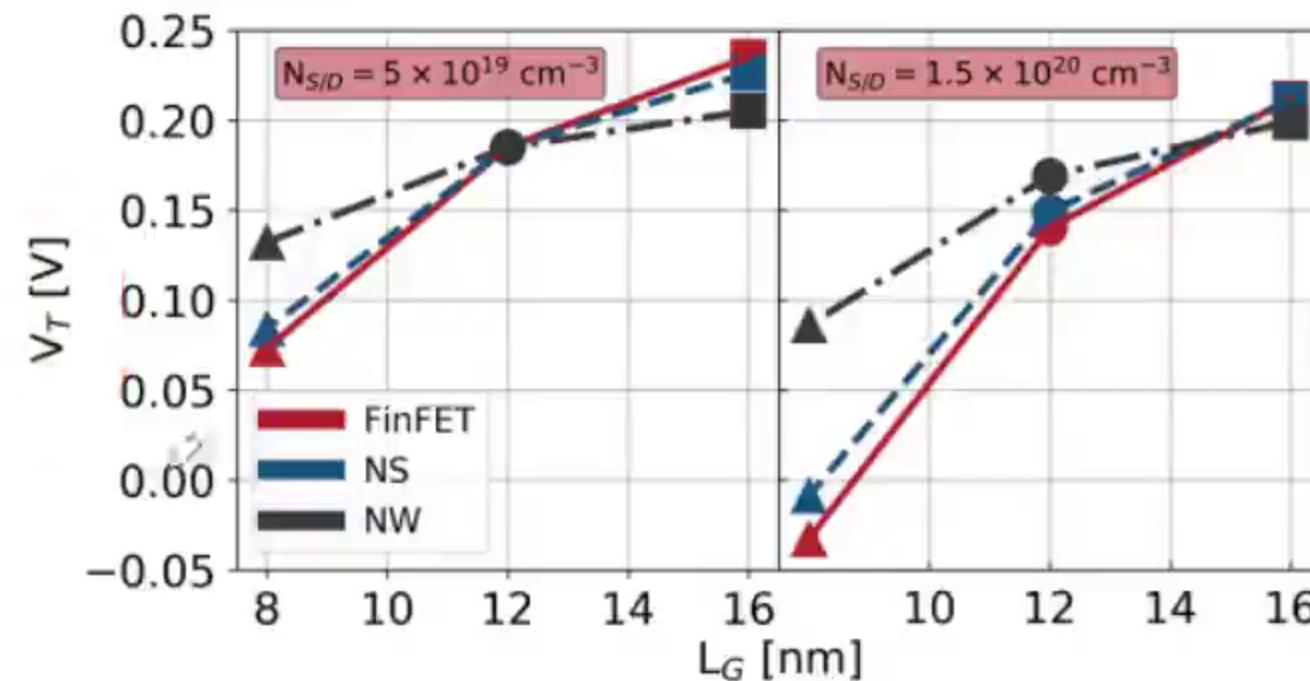


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魔鬼死舞:Sigma Vt

- 芯片設計需要”包含制程的變化”，而制程的變化的指標為 σV_t (V_t 的斜率)
- σV_t 不應超過50mV(見右)， σV_t 趨勢越來越糟，此值已是35mV於32nm世代了，若非22nm世代推出了新鰭狀電晶體(FFT)，CMOS scaling大概就GG了，
- 那麼為何鰭狀電晶體(22nm)橫空出世就能逆轉 σV_t 趨勢呢？
 - 因為沒有了RDF(random dopant fluctuation)也

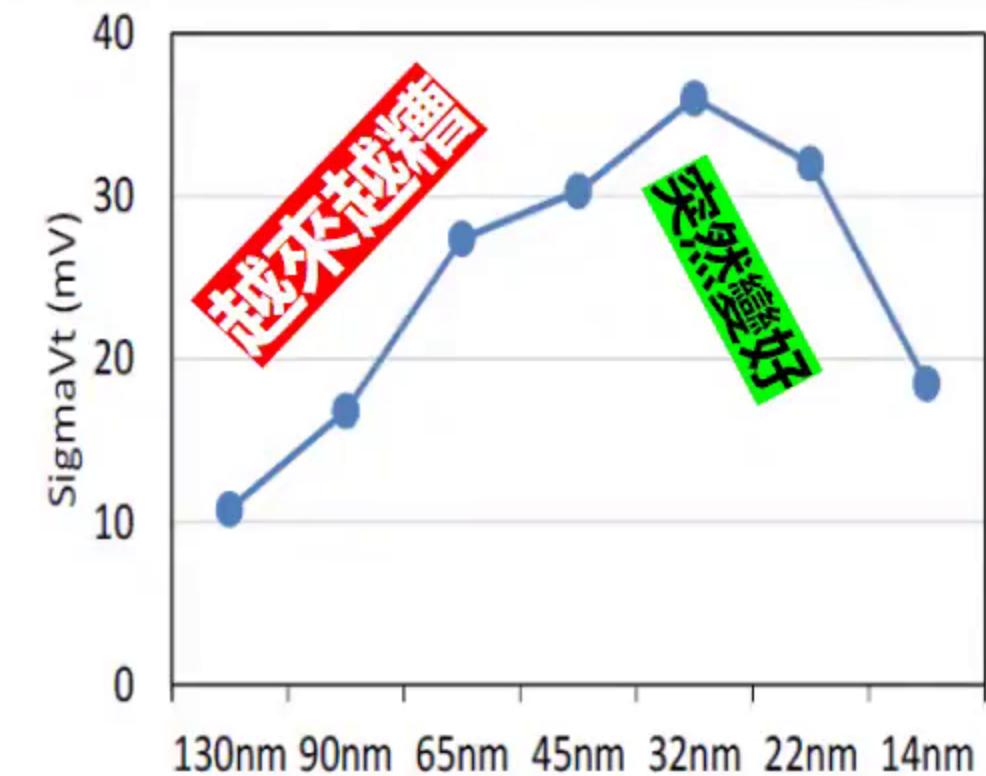


Figure 7: Random Variation Trend (σV_t)

S Natarajan, Intel IEDM'14

FDSOI 被 Tsi 與 Tbox 的魔鬼死舞困住

- WIWNU impacts ($\sigma V_t \sim 25 \text{mV/nm}$ for early FDSOI devices)

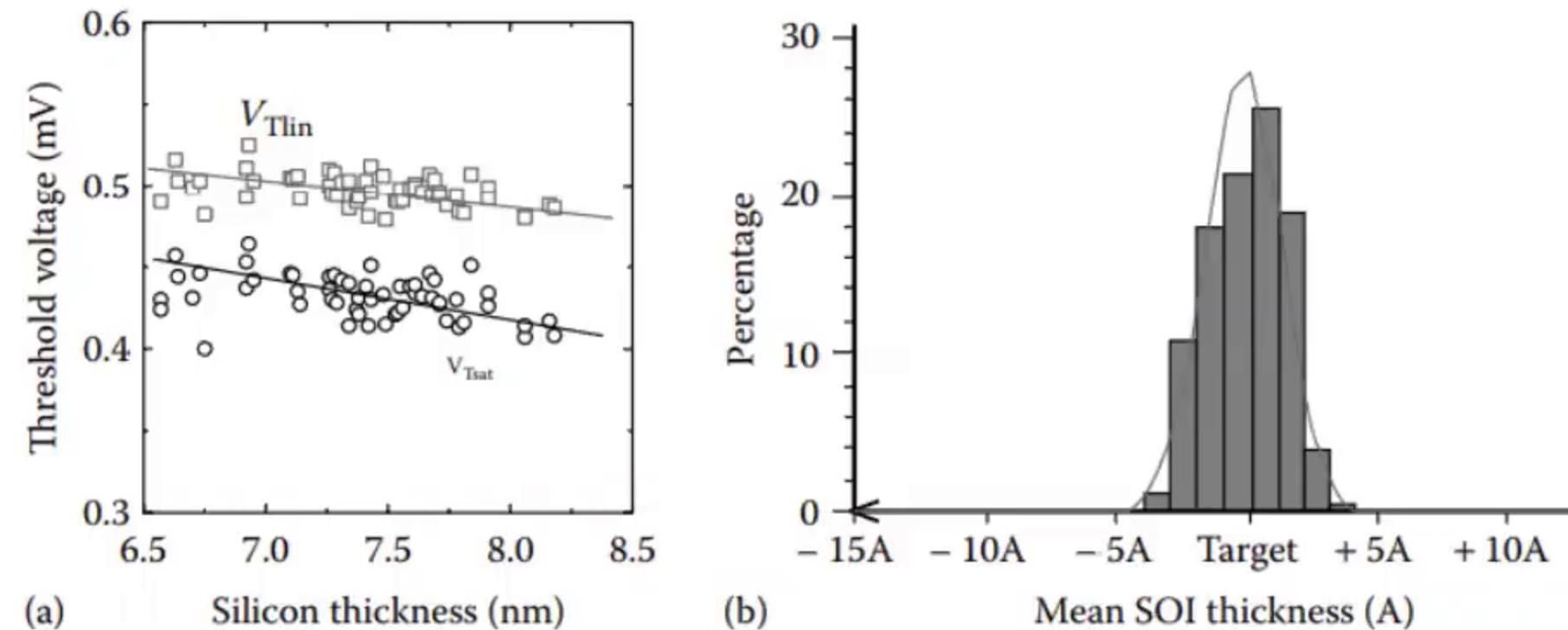
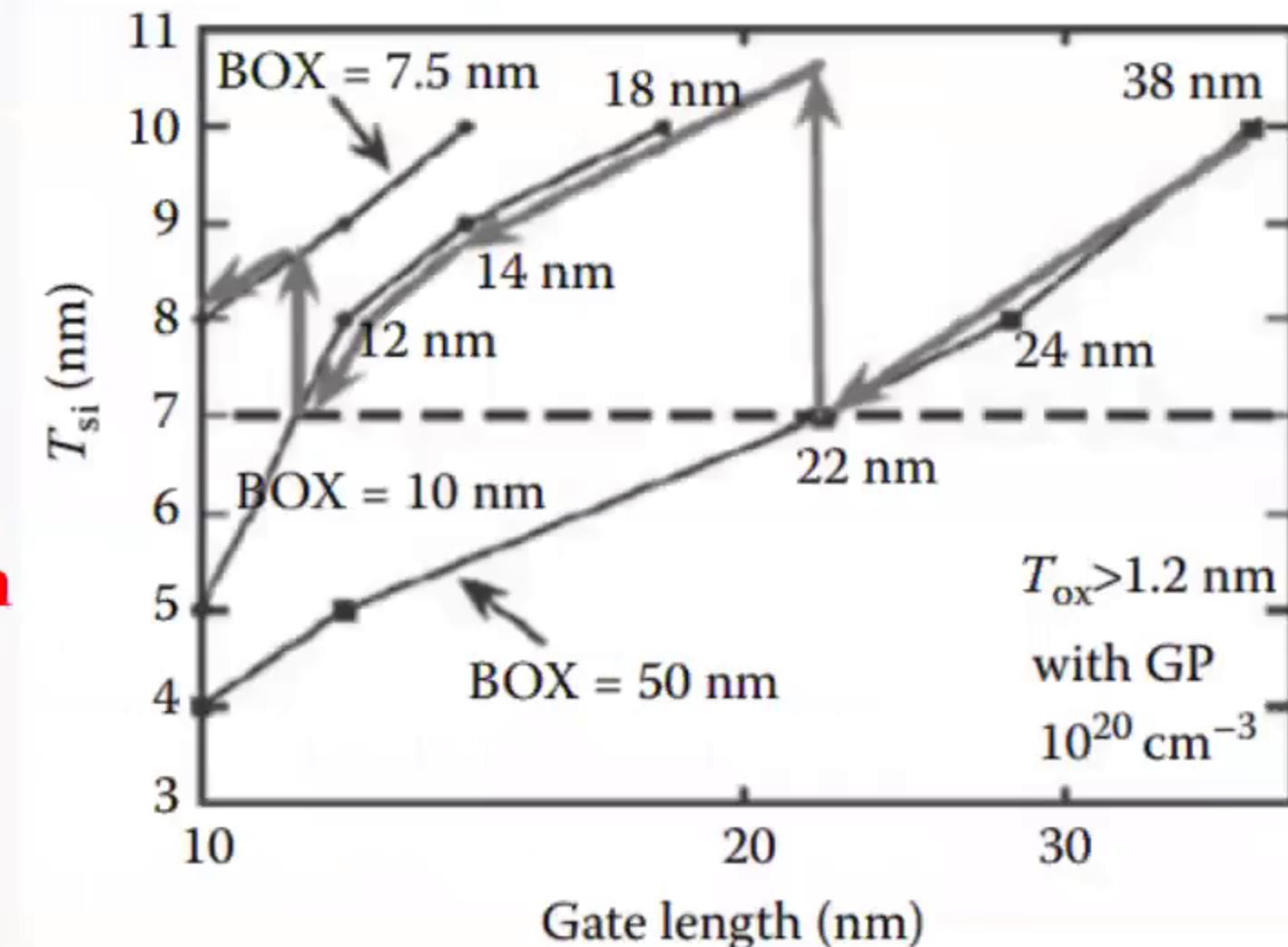
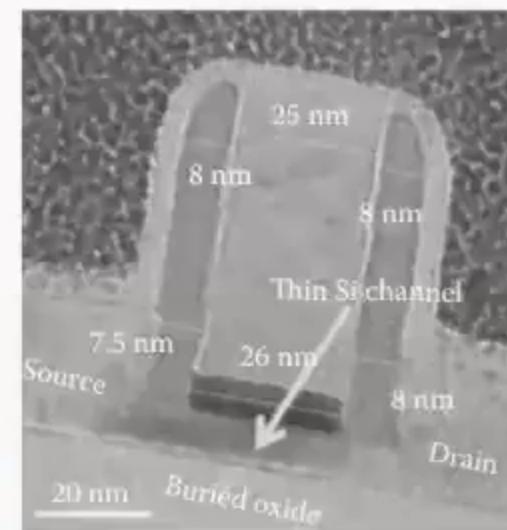


FIGURE 4.9 (a) Threshold voltage as a function of silicon thickness, indicating that the V_t sensitivity is about 25 mV/nm. (From Khakifirooz, A. et al., *International Symposium on*

Challenges and Opportunities of Extremely Thin SOI (ETSOI) CMOS Technology for Future Low Power and General Purpose System-on-Chip Applications, Khakifirooz et al, 2010 IEDM

FDSOI 被 Tsi 與 Tbox 的魔鬼死舞困住

- Rule of Thumb ($T_{si} \sim L_g / 3$):
 - $32/22\text{nm} \rightarrow T_{si} \sim 10/7\text{nm}$
- IBM 14/10 nm FD SOI (FFT)
 - $14/10\text{nm} \rightarrow T_{si} = 5\text{ nm}$,
 - $T_{box} = 10\text{-}20\text{nm}$
- 22nm FDSOI, $4\text{nm} < T_{si} < 7\text{nm}$



Nguyen et al, Fully depleted DOI Technology Overview,
in Micro- and Nanoelectronics, CRC press, 2015