

納米武林基本功

— 土四鬼月系列之六

σV_t , GIDL, DIBL(vs wimpy), Id(mA/um)

王不老說半导

納米武林基本功

— 土四鬼月系列之六 —

σVt, GIDL, DIBL(vs wimpy), Id(mA/um)

王不老說半导

太刀與肋差武士刀

- 日本武士有用許多不同尺寸的刀(如右圖)，而其腰間配有一長一短兩把刀，長刀就是我們所常見的武士刀叫「太刀」，而短的刀叫「肋差」
- 當然，日本武士打架自然以長刀為主，「肋差」適用於偷襲或其他次要用途
- 但在硅納米世界哩，卻剛好相反，所謂的**長通道**(long channel)主要是用來調適芯片參數用，手機與電腦裏頭真正用來工作的，卻是**短通道**(short channel)的电晶体



Scaling Trending gone flat?

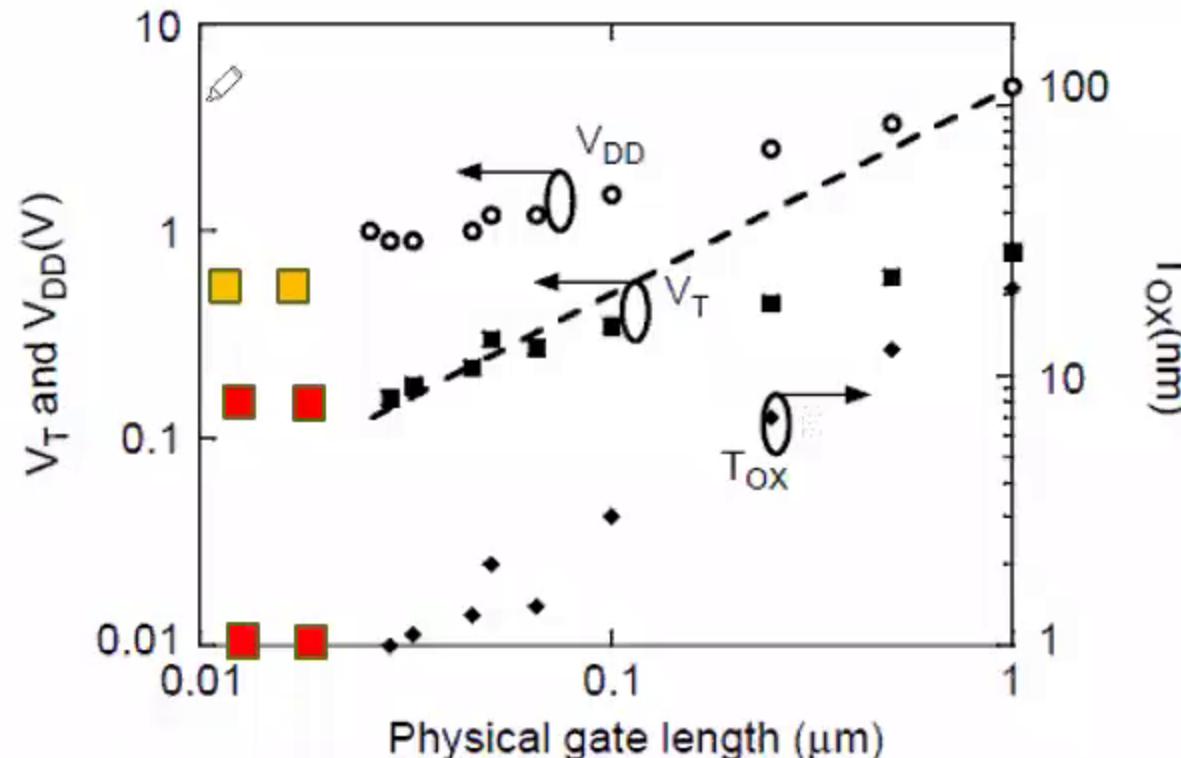
Key parameters scaling trends
gone flat/stopped for extreme
nodes

- $V_{dd} \sim 0.7V$, $V_t > 0.15V$, $L_g > 10nm$, $HKIL \sim 3nm$

What about variability?

$$\sigma Tpd \approx \frac{\sigma VT}{(Vdd - VT)^{2.5}}$$

- $V_{dd} = 1.8V$ and $V_T = 0.3V$, $\sigma Tpd = 0.44 \times \sigma VT$, while for $V_{dd} = 1.6V$, $\sigma Tpd = 0.59 \times \sigma VT$.
- $\rightarrow \sim 25\% \uparrow$ in σTpd as V_{dd} reduced from 1.8V to 1.6V (分母效應也)



Supply voltage, threshold voltage, and gate oxide evolutions vs. gate length.

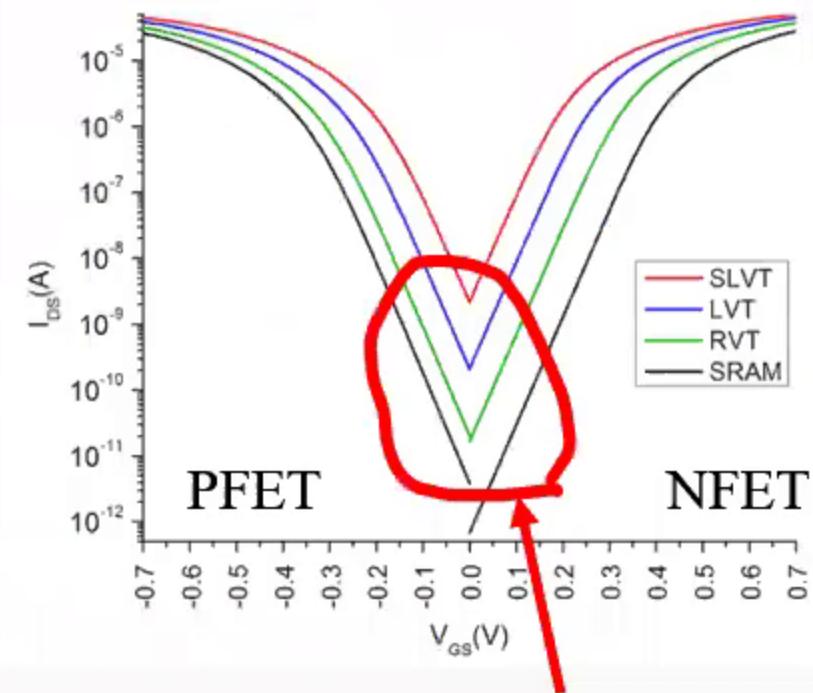
舉例: 7納米顧客的IdVg要求_ASAP7 PDK

右图(及以下)就是某7纳米顾客的需求:

internal MOS devices and layers. Four threshold options, namely high-Vt (HVT), regular Vt (RVT), low Vt (LVT) and Super low VT (SLVT) are usually proposed [Clark2016]:

- HVT – High Threshold Voltage causes less power consumption, but switching is slow. HVT are used in power critical functions. I_{off} is around $0.1 \text{ nA}/\mu\text{m}$, I_{dsat} around $1.2 \text{ mA}/\mu\text{m}$.
- RVT – Regular Threshold Voltage (sometimes called Standard VT or SVT) offers trade-off between HVT and LVT i.e., moderate delay and moderate power consumption. I_{off} is around $1 \text{ nA}/\mu\text{m}$, I_{dsat} around $1.4 \text{ mA}/\mu\text{m}$.
- LVT – Low Threshold Voltage causes more power consumption and switching timing is optimized. LVT are used in time critical functions. I_{off} is around $10 \text{ nA}/\mu\text{m}$, I_{dsat} around $1.6 \text{ mA}/\mu\text{m}$.
- SLVT – Super Low Threshold Voltage causes even more power consumption but switch at the highest speed. SLVT are used in time-critical functions without consideration of leakage currents. I_{off} is around $100 \text{ nA}/\mu\text{m}$, I_{dsat} around $1.8 \text{ mA}/\mu\text{m}$.

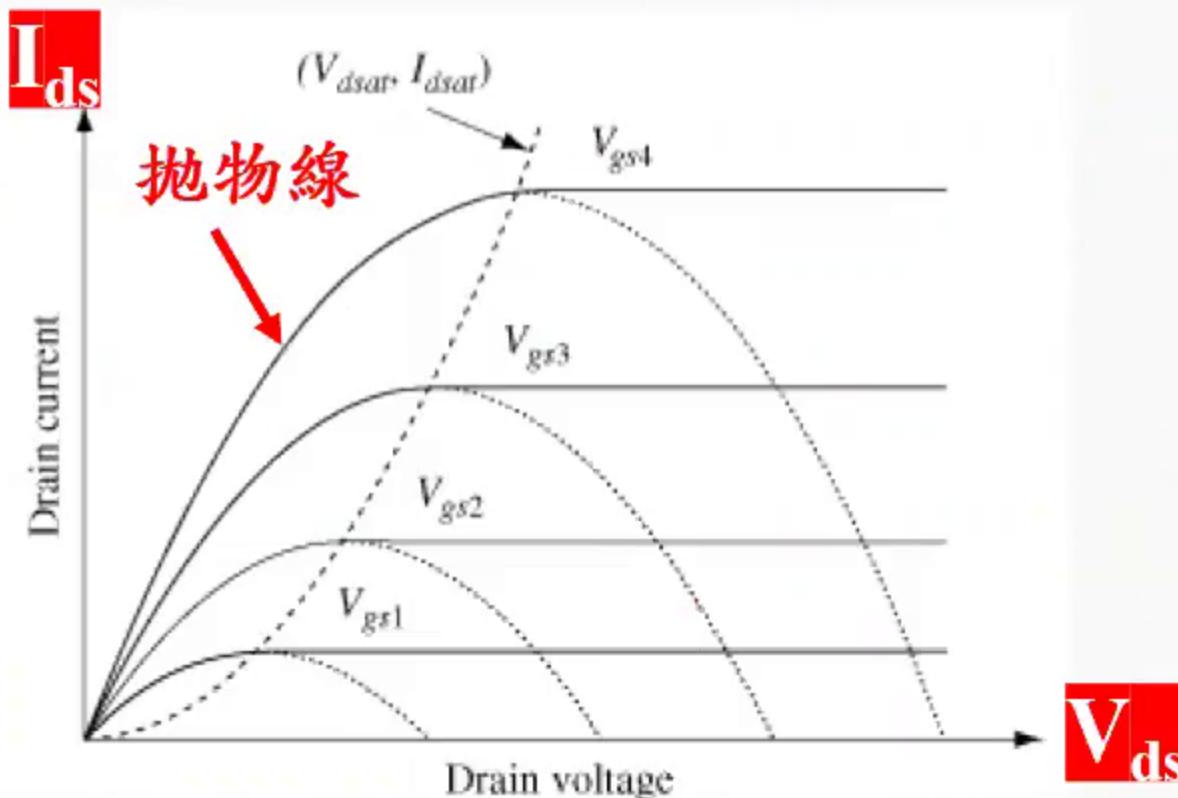
• Microelectronics Journal 53:105-115, 2016
ASAP7: A 7-nm finFET predictive process design kit



制程優化的挑
戰在屁股區乎?

試問: long channel 的電流長甚麼樣子?

- 解答: 飽和之前, 長得像支拋物線(我們愛稱之為IdVd curve), 其公式在右下角
- 其中的L就是本章的重點(channel的長短)有關, 顯而易見, $L \propto I_{ds}$ ~只與電壓有關, 所以我們在優化製程時, 可以調整的所謂”**製造參數**“ (見下頁), 希望能在調整製程後, I_{ds} 能變得更厲害



$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} \left((V_{gs} - V_t) V_{ds} - \frac{m}{2} V_{ds}^2 \right),$$

試問: I_{ds} 的製造參數為何?

解答: I_{ds} 真正公式蠻複雜的(如下圖), 所謂”製造參數 (manufacturing parameters)”有 K_N , a 與 λ 等, 例如:

- $K_N = \frac{\mu \varepsilon_{ox}}{t_{ox}}$, a 與dopants有關, 這些都是製程可以改變的材料參數
- 不過說實在話, 現在真正影響制程良率地的反而是其他東西(leakages and defects vs Yields等), 然而基本功還是要練的

$$I_{DS} = \frac{W}{L} \cdot K_N \cdot \begin{cases} 0 & \text{if } V_{GS} \leq V_{TH} \\ \left(V_{GS} - V_{TH} - \frac{(1+a)}{2} V_{DS} \right) V_{DS} (1 + \lambda V_{DS}) & \text{if } V_{DS} \leq \frac{(V_{GS} - V_{TH})}{(1+a)} \\ \frac{(V_{GS} - V_{TH})^2}{2(1+a)} (1 + \lambda V_{DS}) & \text{if } V_{DS} \geq \frac{(V_{GS} - V_{TH})}{(1+a)} \end{cases}$$

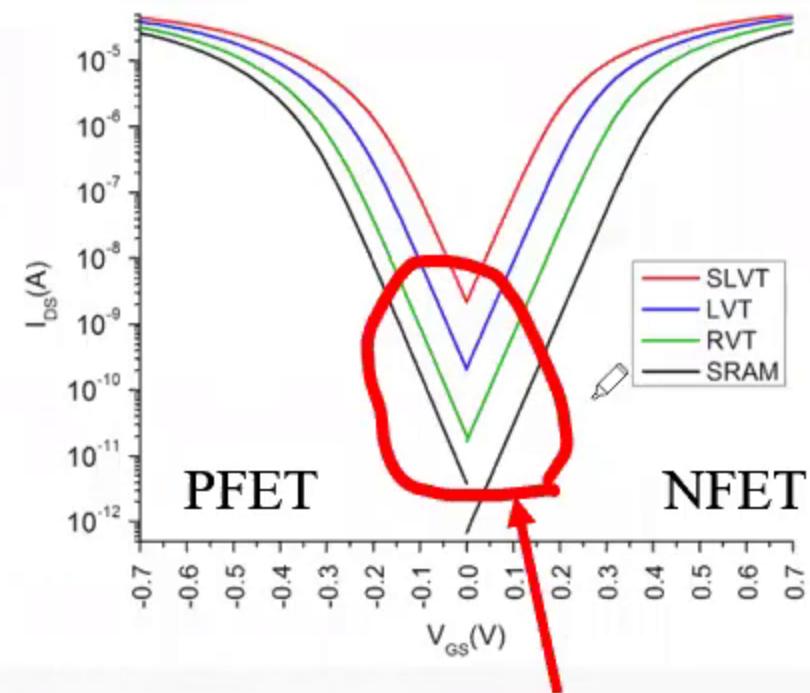
舉例: 7納米顧客的IdVg要求_ASAP7 PDK

右图(及以下)就是某7纳米顾客的需求:

internal MOS devices and layers. Four threshold options, namely high-Vt (HVT), regular Vt (RVT), low Vt (LVT) and Super low VT (SLVT) are usually proposed [Clark2016]:

- HVT – High Threshold Voltage causes less power consumption, but switching is slow. HVT are used in power critical functions. I_{off} is around $0.1 \text{ nA}/\mu\text{m}$, I_{dsat} around $1.2 \text{ mA}/\mu\text{m}$.
- RVT – Regular Threshold Voltage (sometimes called Standard VT or SVT) offers trade-off between HVT and LVT i.e., moderate delay and moderate power consumption. I_{off} is around $1 \text{ nA}/\mu\text{m}$, I_{dsat} around $1.4 \text{ mA}/\mu\text{m}$.
- LVT – Low Threshold Voltage causes more power consumption and switching timing is optimized. LVT are used in time critical functions. I_{off} is around $10 \text{ nA}/\mu\text{m}$, I_{dsat} around $1.6 \text{ mA}/\mu\text{m}$.
- SLVT – Super Low Threshold Voltage causes even more power consumption but switch at the highest speed. SLVT are used in time-critical functions without consideration of leakage currents. I_{off} is around $100 \text{ nA}/\mu\text{m}$, I_{dsat} around $1.8 \text{ mA}/\mu\text{m}$.

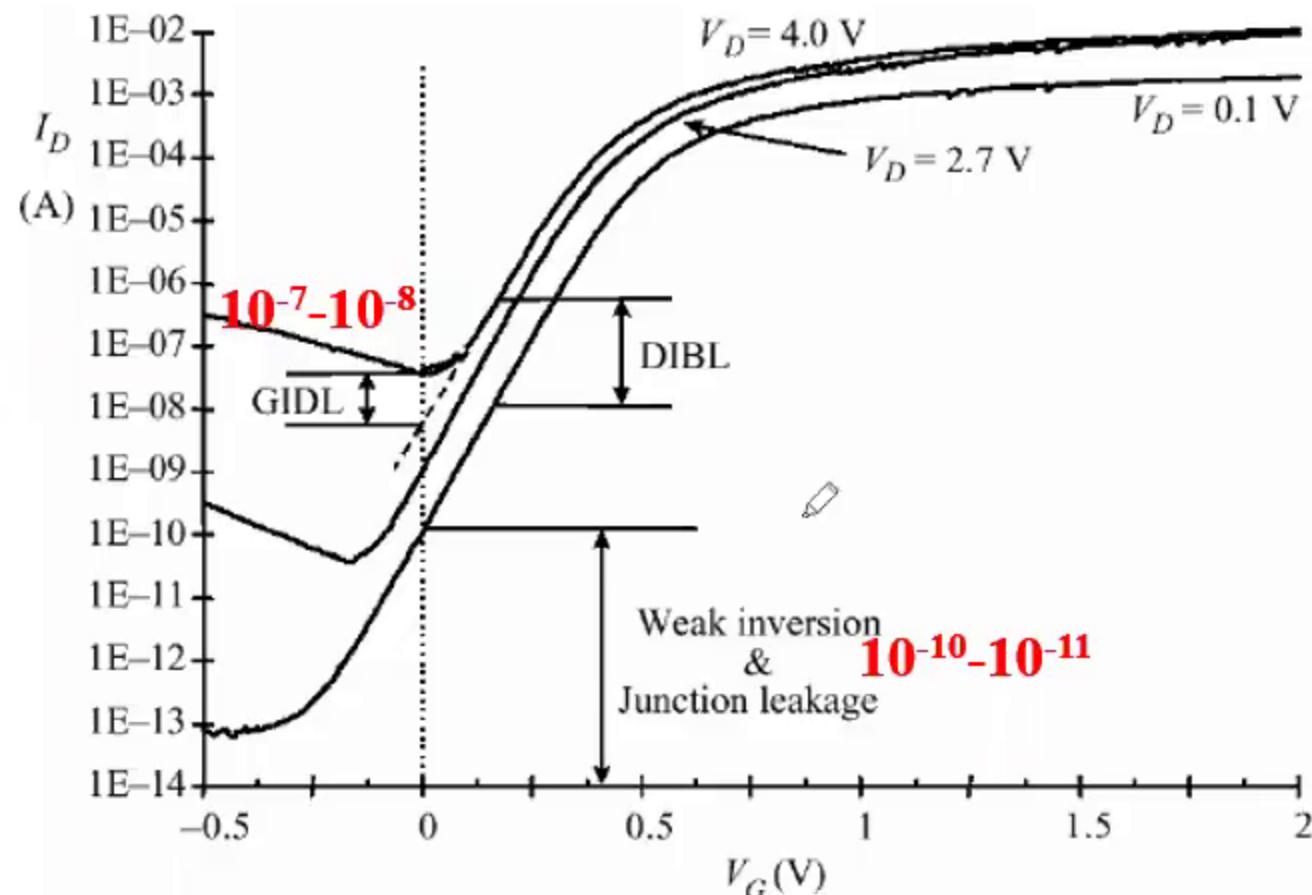
• Microelectronics Journal 53:105-115, 2016
ASAP7: A 7-nm finFET predictive process design kit



制程優化的挑
戰在屁股區乎?

制程優化的挑戰在屁股區

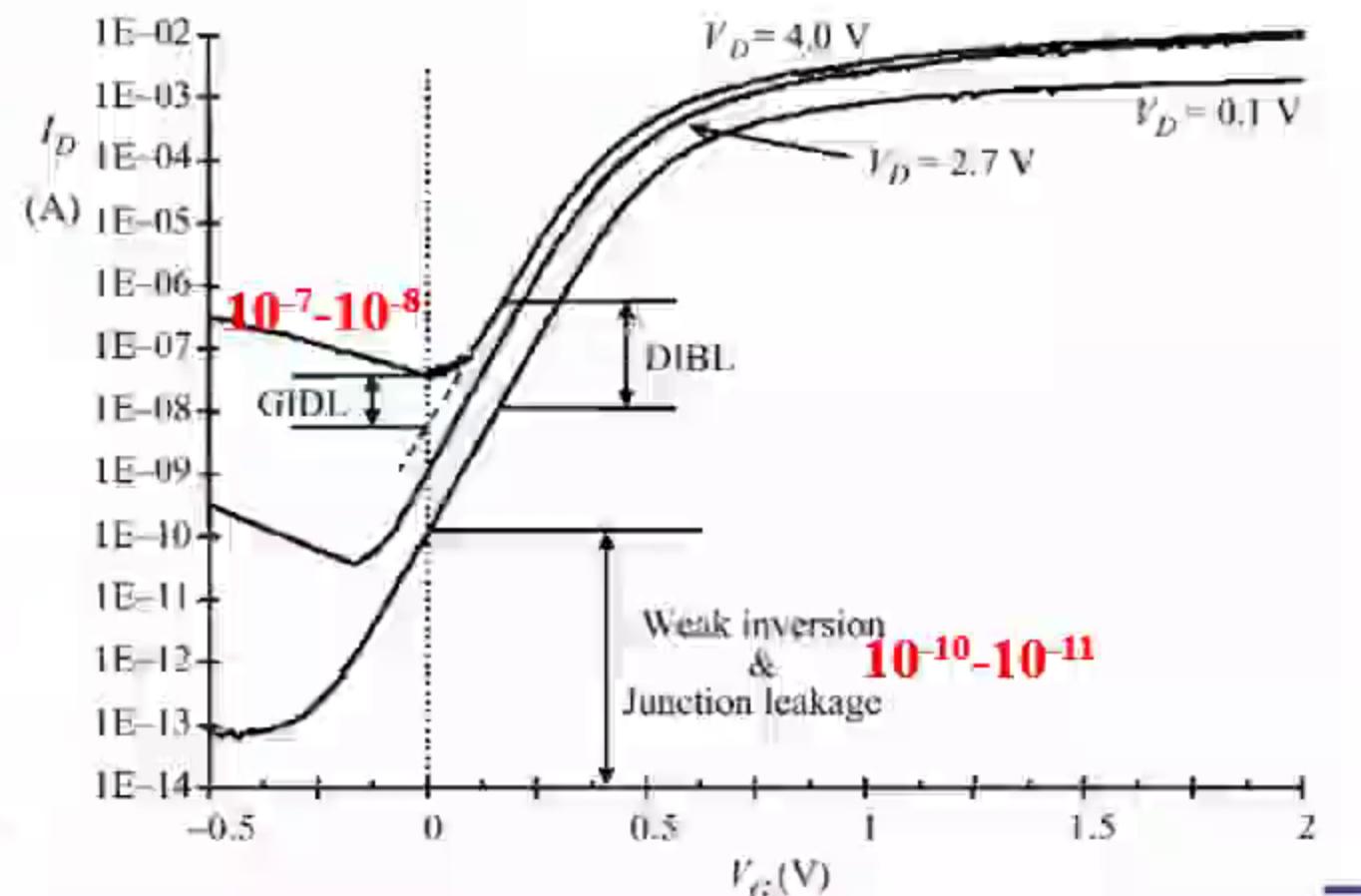
- Scaling的目的:面積少一半,但重要防漏參數(SS, DIBL, GIDL, gate leakage等)與可靠性BTI不惡化,而電流 I_D 大一些就OK了(知易行難也)
- 右圖的(junction leakage and weak inversion, DIBL and GIDL)設計時就知道的漏電流,制程工程師其實管不了
- 但是制程工程師必須優化制程,使得量產結果與理論估計值(設計時就知道了)相差不大



GIDL在最新製程(7/5/3NM)不太重要了,因為 V_{dd} 只有約0.7V

制程優化的挑戰在屁股區

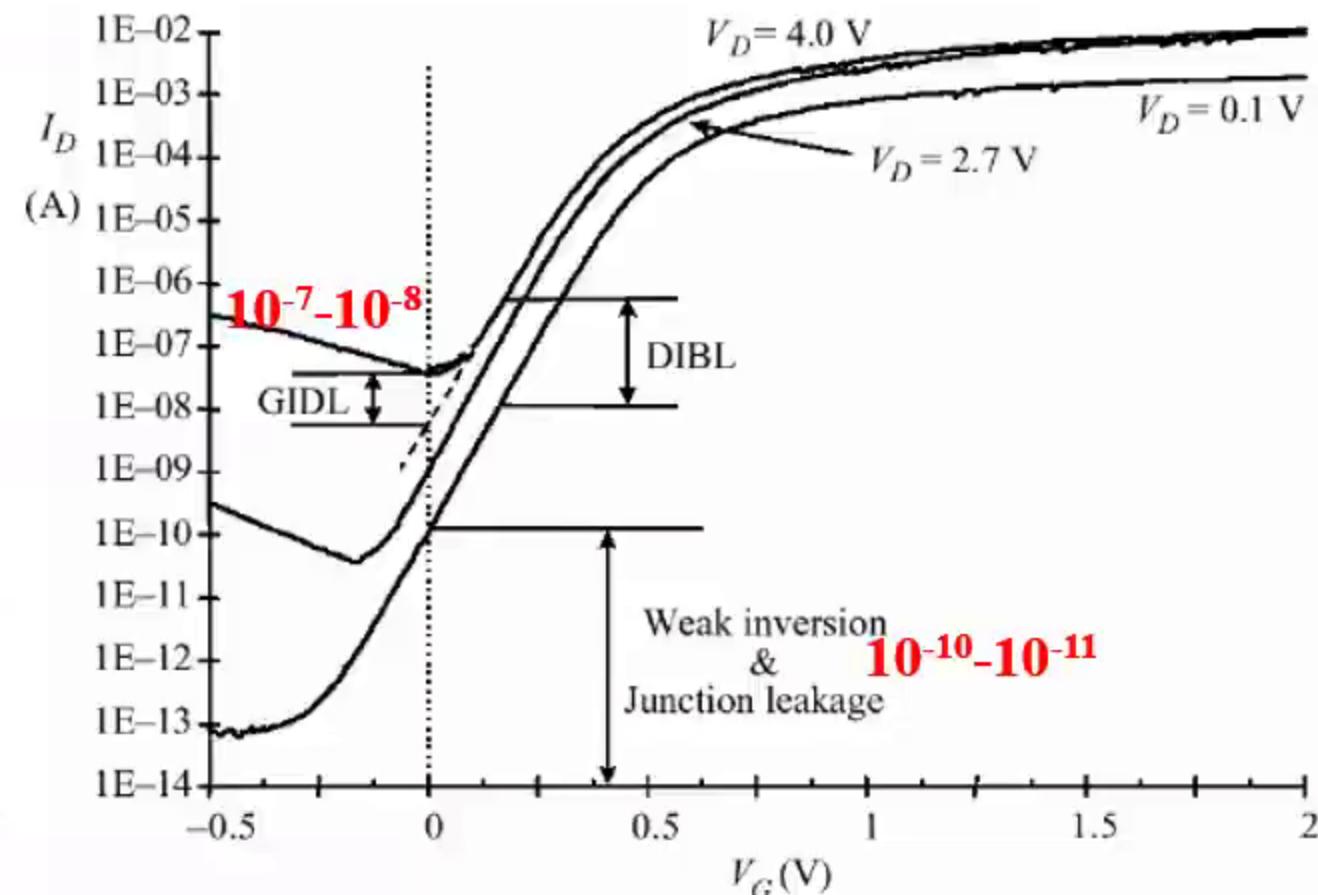
- Scaling的目的:面積少一半,但重要防漏參數(SS, DIBL, GIDL, gate leakage等)與可靠性BTI不惡化,而電流 I_D 大一些就OK了(知易行難也)
- 右圖的(junction leakage and weak inversion, DIBL and GIDL)設計時就知道的漏電流,制程工程師其實管不了
- 但是制程工程師必須優化制程,使得量產結果與理論估計值(設計時就知道了)相差不大



GIDL在最新製程(7/5/3NM)不太重要了,因為 V_{dd} 只有約0.7V

制程優化的挑戰在屁股區

- Scaling的目的:面積少一半,但重要防漏參數(SS, DIBL, GIDL, gate leakage等)與可靠性BTI不惡化,而電流 I_D 大一些就OK了(知易行難也)
- 右圖的(junction leakage and weak inversion, DIBL and GIDL)設計時就知道的漏電流,制程工程師其實管不了
- 但是制程工程師必須優化制程,使得量產結果與理論估計值(設計時就知道了)相差不大

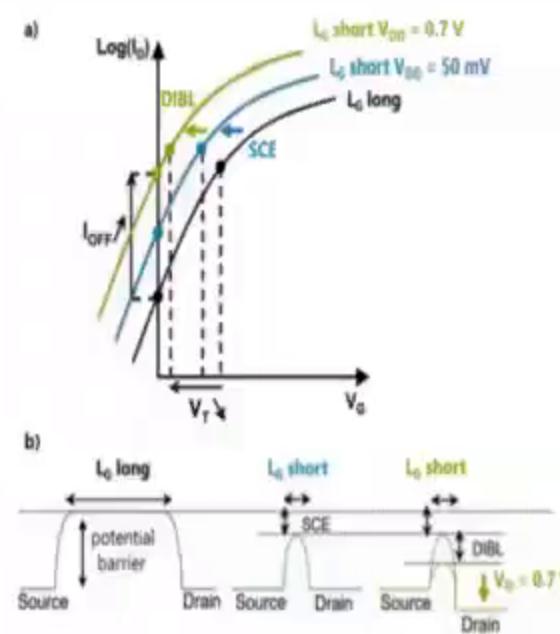


GIDL在最新製程(7/5/3NM)不太重要了,因為 V_{dd} 只有約0.7V

試問：為何DIBL必須越小越好？

解答：因為她對V_t影響深遠

- $V_t(SC) = V_t(LC) - SCE - DIBL$
 $V_t(SC) \sim V_t(LC) - DIBL$
 - V_t 之太刀 = **long channel** $V_t = V_t(LC)$
 - V_t 之肋差 = **short channel** $V_t = V_t(SC)$
- DIBL都與通道(L)大小，有巨大相關，若L越小則以上二者越大，所謂優化的製程就是指**DIBL要比對手小**
- 下一頁我們比較TSMC的5nm與GF的7nm製程的DIBL



SCE and drain induced barrier lowering (DIBL) can be computed in various devices geometry by introducing the Electrostatic Integrity factor (EI):

$$SCE \sim 0.64 \frac{\epsilon_{Si}}{\epsilon_{ox}} \cdot EI \cdot V_{bi} \quad (\text{Eq. 1-1})$$

$$DIBL \sim 0.80 \frac{\epsilon_{Si}}{\epsilon_{ox}} \cdot EI \cdot V_{DS} \quad (\text{Eq. 1-2})$$

with V_{bi} the source to drain built-in potential and V_{DS} the source to drain potential.

Figure 1.3 – DIBL and SCE displayed on (a) a transistor I-V characteristic and (b) on a band diagram.

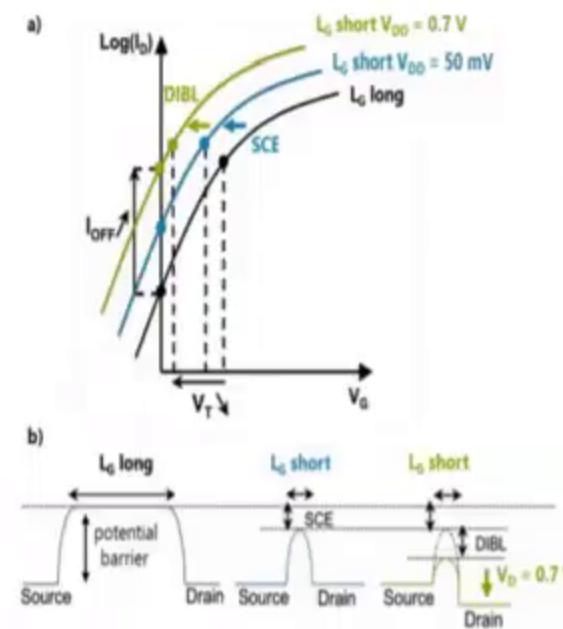
This gives the threshold voltage roll-off in between a long channel device ($V_{th\infty}$) and its short channel counterpart (V_{th}):

$$V_{th} = V_{th\infty} - SCE - DIBL \quad (\text{Eq. 1-3})$$

試問：為何DIBL必須越小越好？

解答：因為她對V_t影響深遠

- $V_t(SC) = V_t(LC) - SCE - DIBL$
- $V_t(SC) \sim V_t(LC) - DIBL$
 - V_t 之太刀 = **long channel** $V_t = V_t(LC)$
 - V_t 之肋差 = **short channel** $V_t = V_t(SC)$
- DIBL都與通道(L)大小，有巨大相關，若L越小則以上二者越大，所謂優化的製程就是指**DIBL要比對手小**
- 下一頁我們比較TSMC的5nm與GF的7nm製程的DIBL



SCE and drain induced barrier lowering (DIBL) can be computed in various devices geometry by introducing the Electrostatic Integrity factor (EI):

$$SCE \sim 0.64 \frac{\epsilon_{Si}}{\epsilon_{ox}} \cdot EI \cdot V_{bi} \quad (Eq. 1-1)$$

$$DIBL \sim 0.80 \frac{\epsilon_{Si}}{\epsilon_{ox}} \cdot EI \cdot V_{DS} \quad (Eq. 1-2)$$

with V_{bi} the source to drain built-in potential and V_{DS} the source to drain potential.

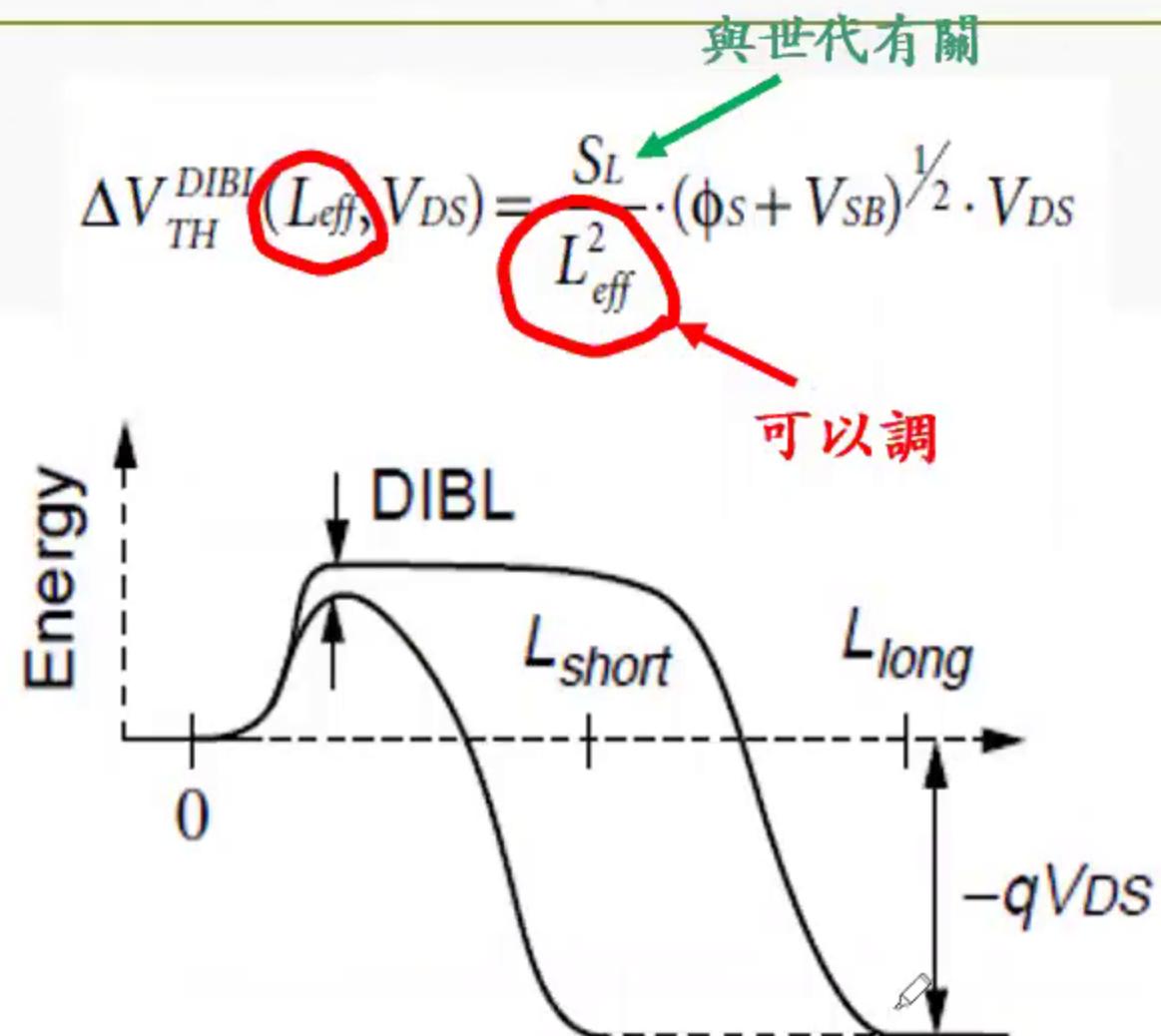
Figure 1.3 – DIBL and SCE displayed on (a) a transistor I-V characteristic and (b) on a band diagram.

This gives the threshold voltage roll-off in between a long channel device ($V_{th\infty}$) and its short channel counterpart (V_{th}):

$$V_{th} = V_{th\infty} - SCE - DIBL \quad (Eq. 1-3)$$

一石二鳥：DIBL的缺點變優點

- Drain-induced barrier lowering (DIBL): voltage at the drain lowers the source potential barrier lowers V_t (no change on SS)
- 右圖顯示，DIBL將臨界電壓 V_t 下降了，(因為所需能量減少了，電晶體更易高潮)，而且他只與 L_{eff} and V_{DS} 有關



試問：為何DIBL必須越小越好？

解答：因為她對V_t影響深遠

- $V_t(SC) = V_t(LC) - SCE - DIBL$
→ $V_t(SC) \sim V_t(LC) - DIBL$
 - V_t 之太刀 = **long channel** $V_t = V_t(LC)$
 - V_t 之肋差 = **short channel** $V_t = V_t(SC)$
- DIBL都與通道(L)大小，有巨大相關，若L越小則以上二者越大，所謂優化的製程就是指**DIBL要比對手小**
- 下一頁我們比較TSMC的5nm與GF的7nm製程的DIBL

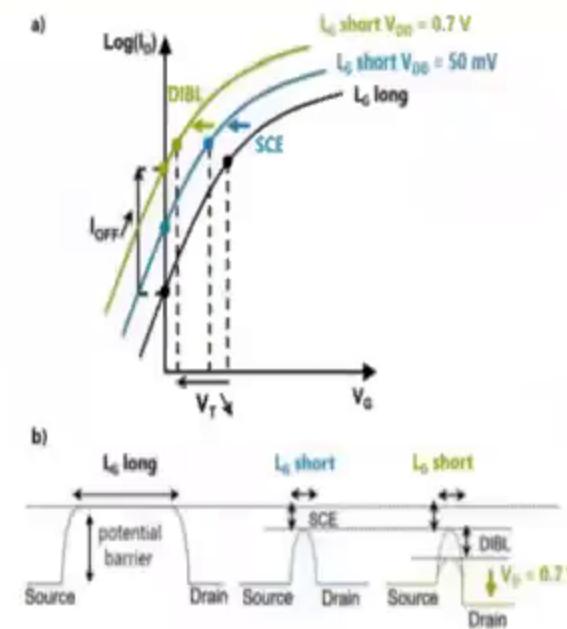


Figure 1.3 – DIBL and SCE displayed on (a) a transistor I-V characteristic and (b) on a band diagram.

This gives the threshold voltage roll-off in between a long channel device ($V_{th\infty}$) and its short channel counterpart (V_{th}):

$$V_{th} = V_{th\infty} - SCE - DIBL \quad (Eq. 1-3)$$

Fabrication and Characterization of Gate-All-Around Stacked-Nanowire/Nanosheet MOS transistors realized by a Gate-Last approach for sub-7 nm technology nodes. Loic Gaben

SCE and drain induced barrier lowering (DIBL) can be computed in various devices geometry by introducing the Electrostatic Integrity factor (EI):

$$SCE \sim 0.64 \frac{\epsilon_{Si}}{\epsilon_{ox}} \cdot EI \cdot V_{bi} \quad (Eq. 1-1)$$

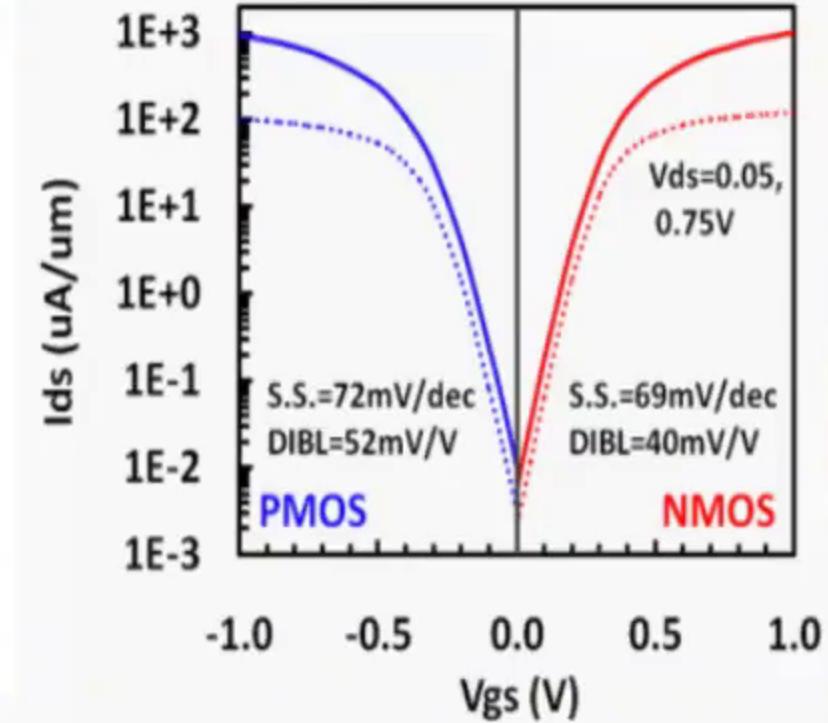
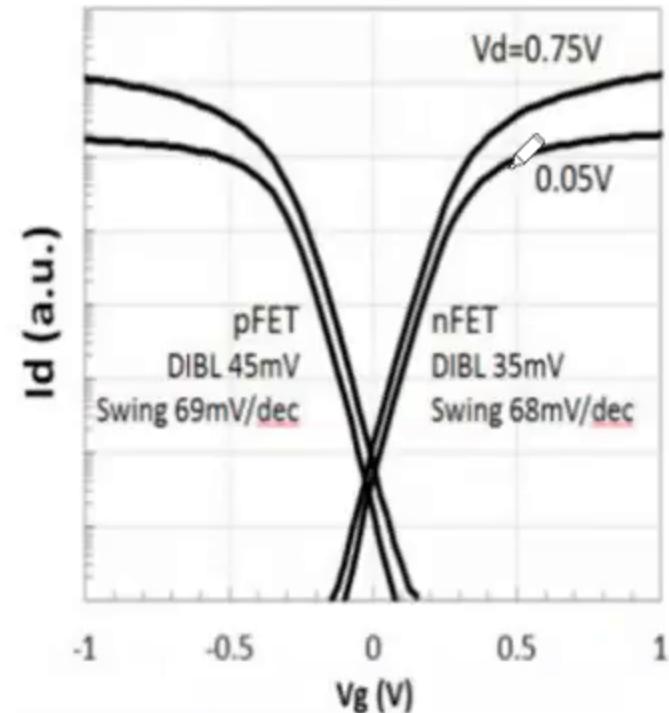
$$DIBL \sim 0.80 \frac{\epsilon_{Si}}{\epsilon_{ox}} \cdot EI \cdot V_{DS} \quad (Eq. 1-2)$$

with V_{bi} the source to drain built-in potential and V_{DS} the source to drain potential.

比較: TSMC 5nm vs GF 7nm

結果:如右圖所示，TSMC完勝

- DIBL: 與 L_g 及相關製程有關，越小越好 (5nm比7nm難多了)，
 - TSMC 5nm = 35mV per V
 - GF 7nm = 40mV per V
- SS (swing): 與介面缺陷有關，所以也是越小越好
 - TSMC 5nm = 68/69 mV/dec
 - GF 7nm = 69/72 mV/dec
- 看來差異彷彿不是太大。然而結果是GF輸得脫褲子，最後宣告7nm徹底失敗，退出<10nm晶圓代工戰場，差一點就被賣掉



<https://semiwiki.com/semiconductor-manufacturers/tsmc/282339-tsmc-unveils-details-of-5nm-cmos-production-technology-platform-featuring-euv-and-high-mobility-channel-finfets-at-iedm2019/>

<https://moepc.net/iedm-2017-gf-7nm-further-details-cobalt-and-euv-wikichip/>

GIDL在最新製程(7/5/3NM)不太重要了，因為 V_{dd} 只有約0.7V

DIBL: FinFET的天生麗質

- 注意: 就DIBL而言, FDSOI竟然比DG大得多
- 又 $L_{eff} < 30nm$ 時(現在約15nm了??), 仍必須要求 $DIBL \sim 35 mV/dec$
- Note: L_{eff} is defined to be the lateral separation between the locations at which the S/D doping falls $1 \times 10^{19}/cm^3$

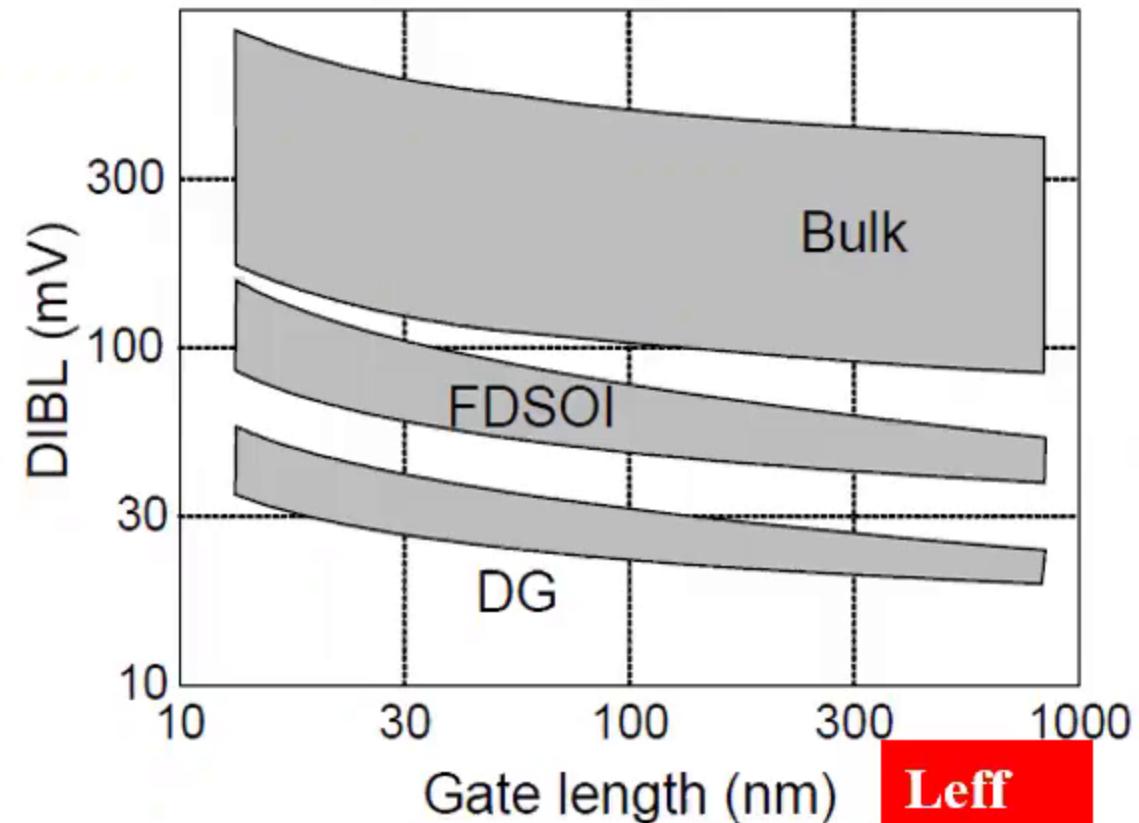


Fig. 1.4. Typical drain-induced barrier lowering in bulk, fully depleted SOI (FDSOI) and double-gate (DG) MOSFETs calculated by MASTAR.

DIBL: FinFET的天生麗質

- 注意: 就DIBL而言, FDSOI竟然比DG大得多
- 又Leff < 30nm時(現在約15nm了??), 仍必須要求DIBL ~ 35 mV/dec
 - Note: Leff is defined to be the lateral separation between the locations at which the S/D doping falls $1 \times 10^{19}/\text{cm}^3$

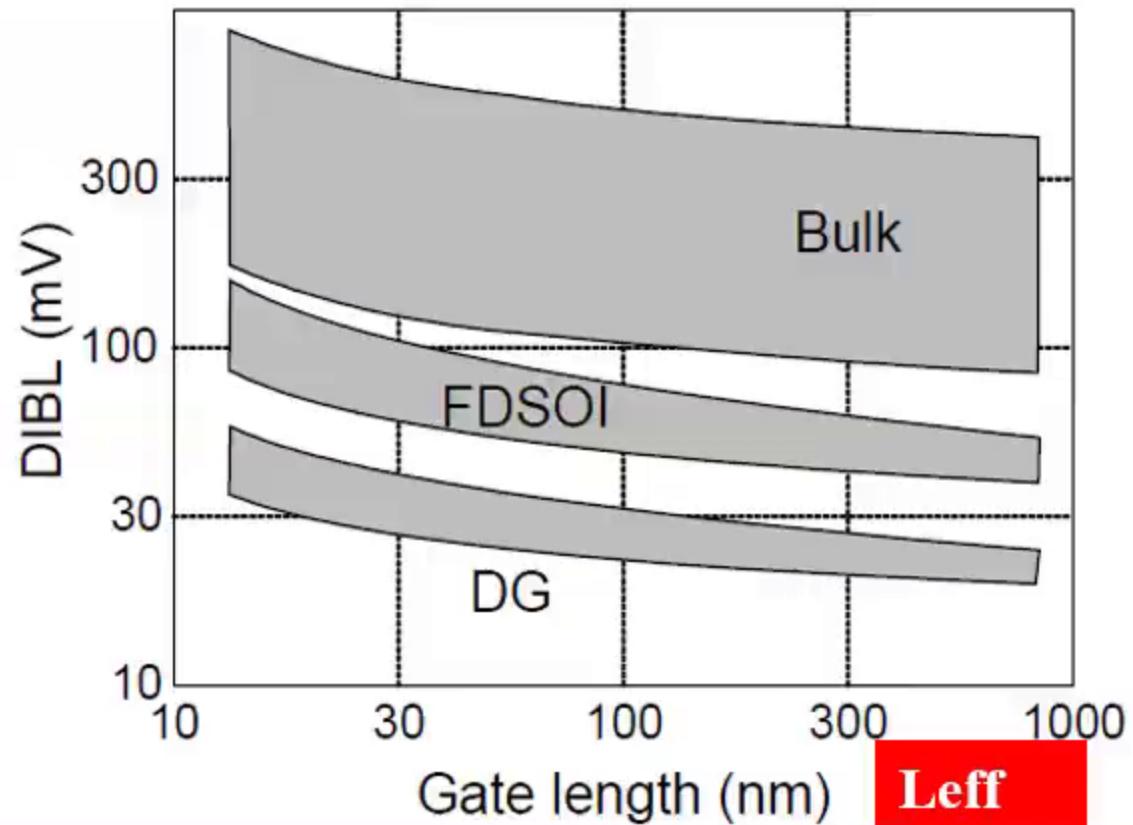
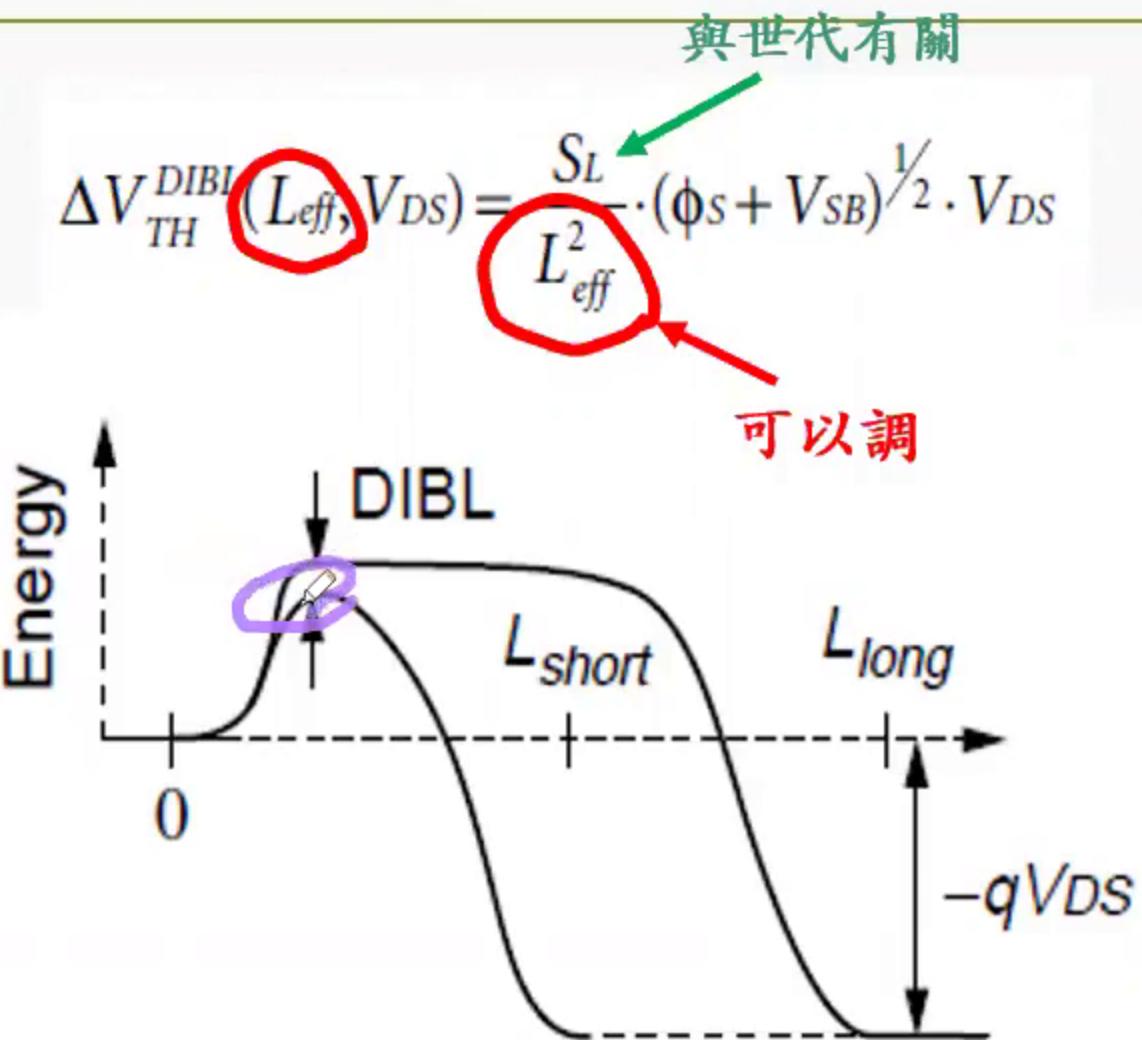


Fig. 1.4. Typical drain-induced barrier lowering in bulk, fully depleted SOI (FDSOI) and double-gate (DG) MOSFETs calculated by MASTAR.

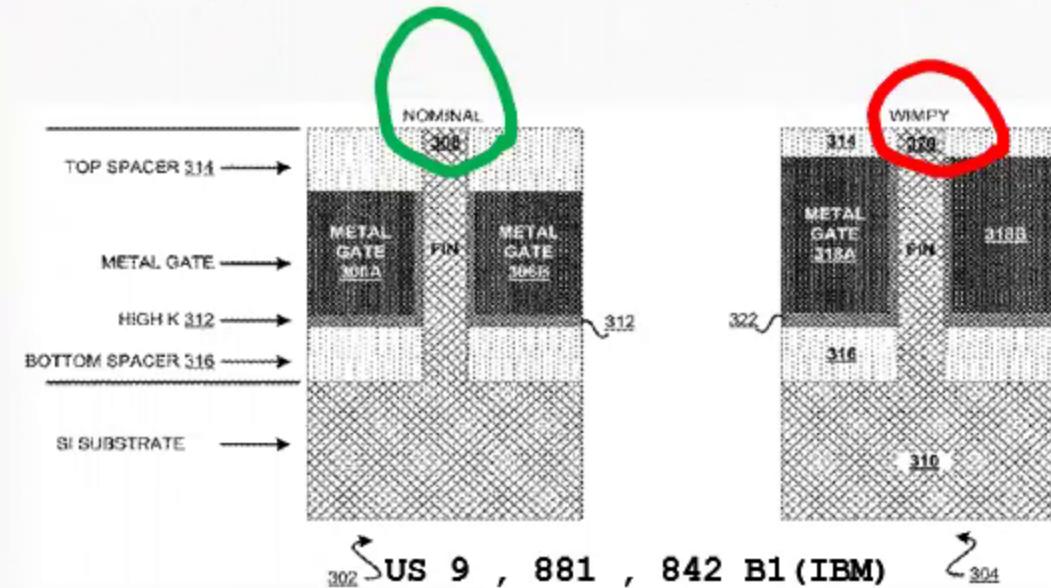
一石二鳥：DIBL的缺點變優點

- Drain-induced barrier lowering (DIBL): voltage at the drain lowers the source potential barrier lowers V_t (no change on SS)
- 右圖顯示，DIBL將臨界電壓 V_t 下降了，(因為所需能量減少了，電晶體更易高潮)，而且他只與 L_{eff} and V_{DS} 有關

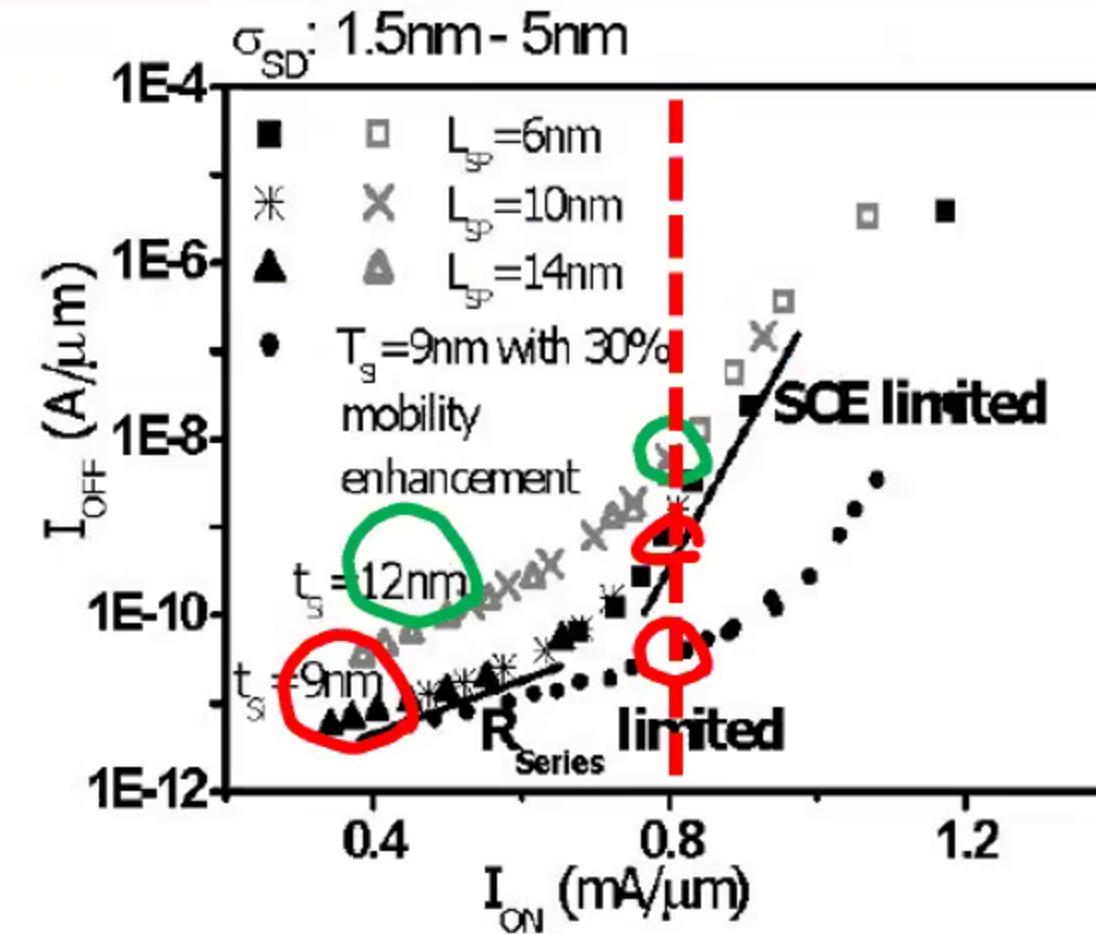


一石二鳥：DIBL的缺點變優點

- 所以有聰明人建議：用不同的Leff來調整Vt(幾乎是免費的，因為使用同一個mask，**一石二鳥也**)，此曰之wimpy
- 右圖顯示，同一Ion之下，可以有兩個Ioff(二者唯一差別是L大小)



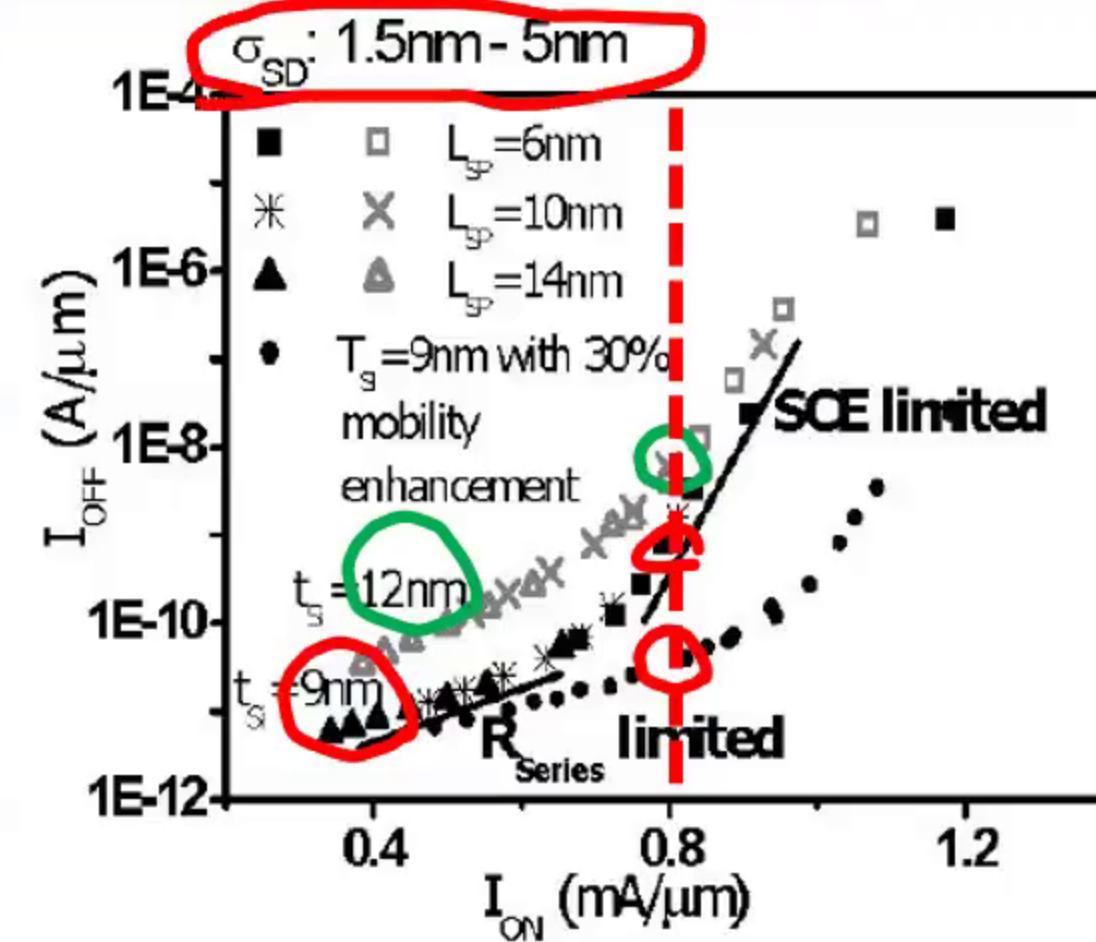
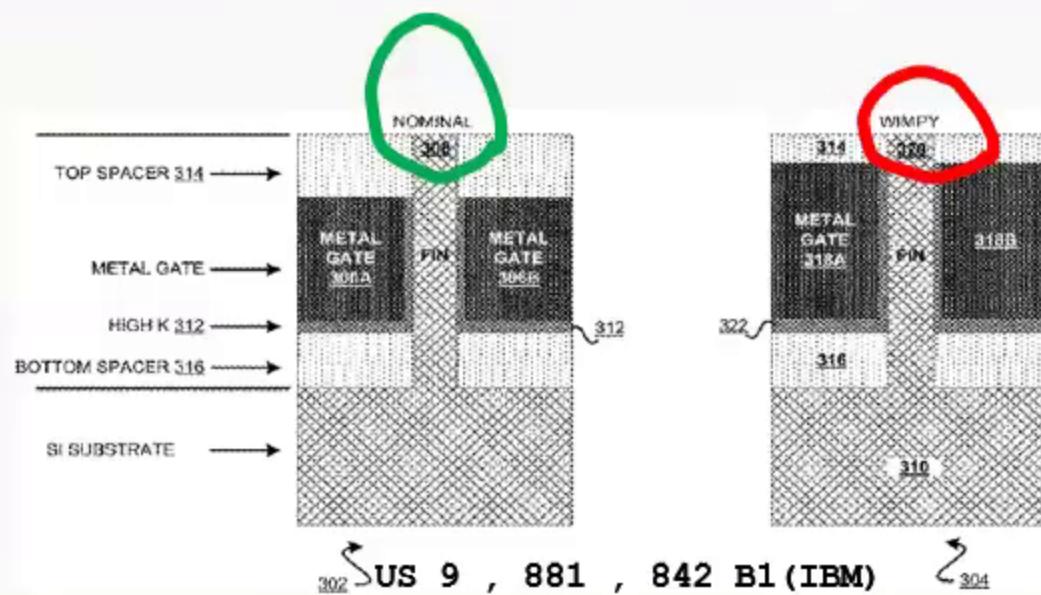
當Leff變得太小時，此招還能用嗎？



VT Adjustment by Leff Engineering for LSTP Single Gate Work-function CMOS
FinFET Technology Varadarajan et al, DOI: [10.1109/UGIM.2006.4286372](https://doi.org/10.1109/UGIM.2006.4286372)

一石二鳥：DIBL的缺點變優點

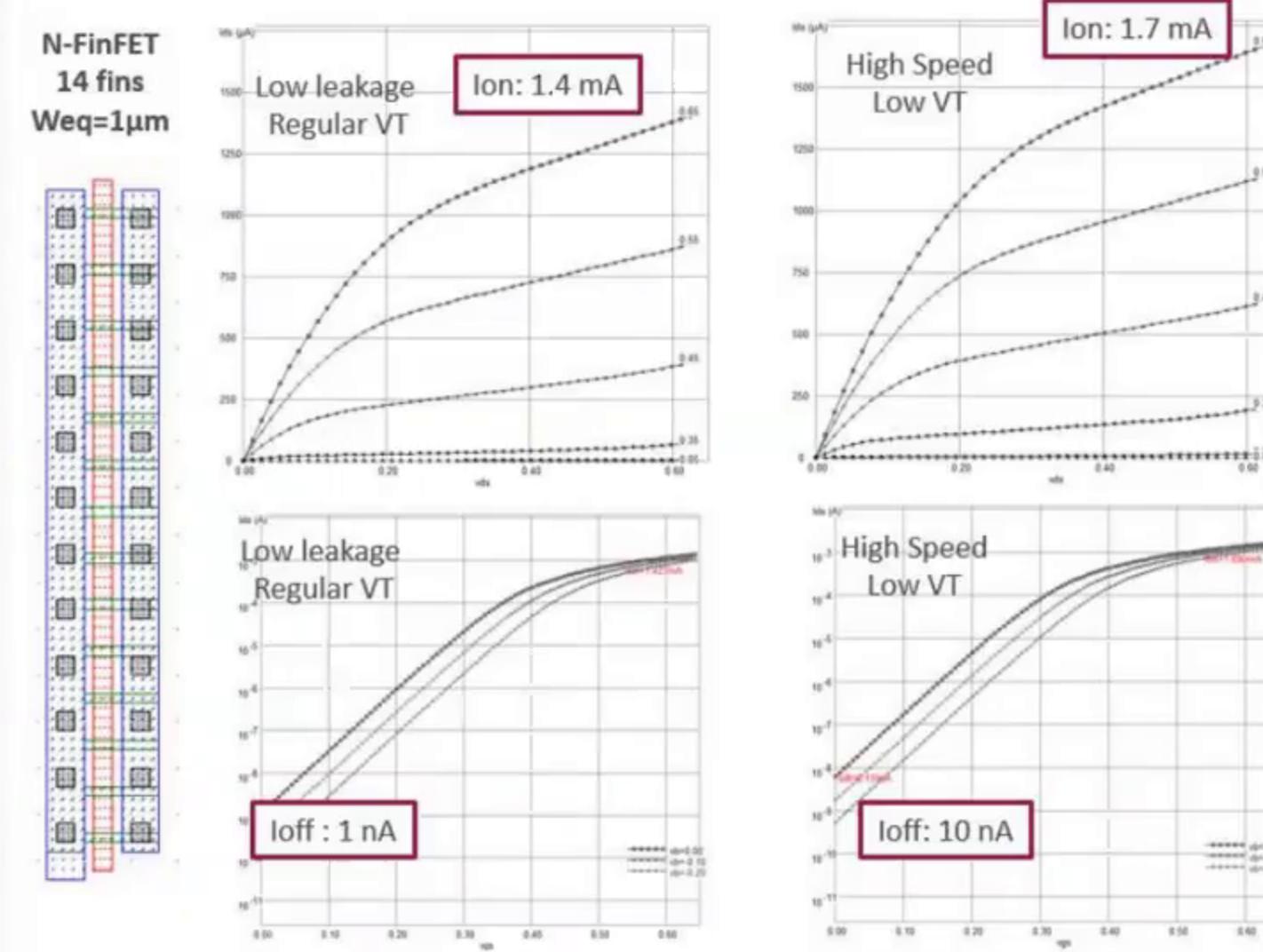
- 當 L_{eff} 變得太小時，此招還能用嗎？
 - 難矣哉！(因為 σ 太大了)



VT Adjustment by Leff Engineering for LSTP Single Gate Work-function CMOS
FinFET Technology Varadarajan et al, DOI: [10.1109/UGIM.2006.4286372](https://doi.org/10.1109/UGIM.2006.4286372)

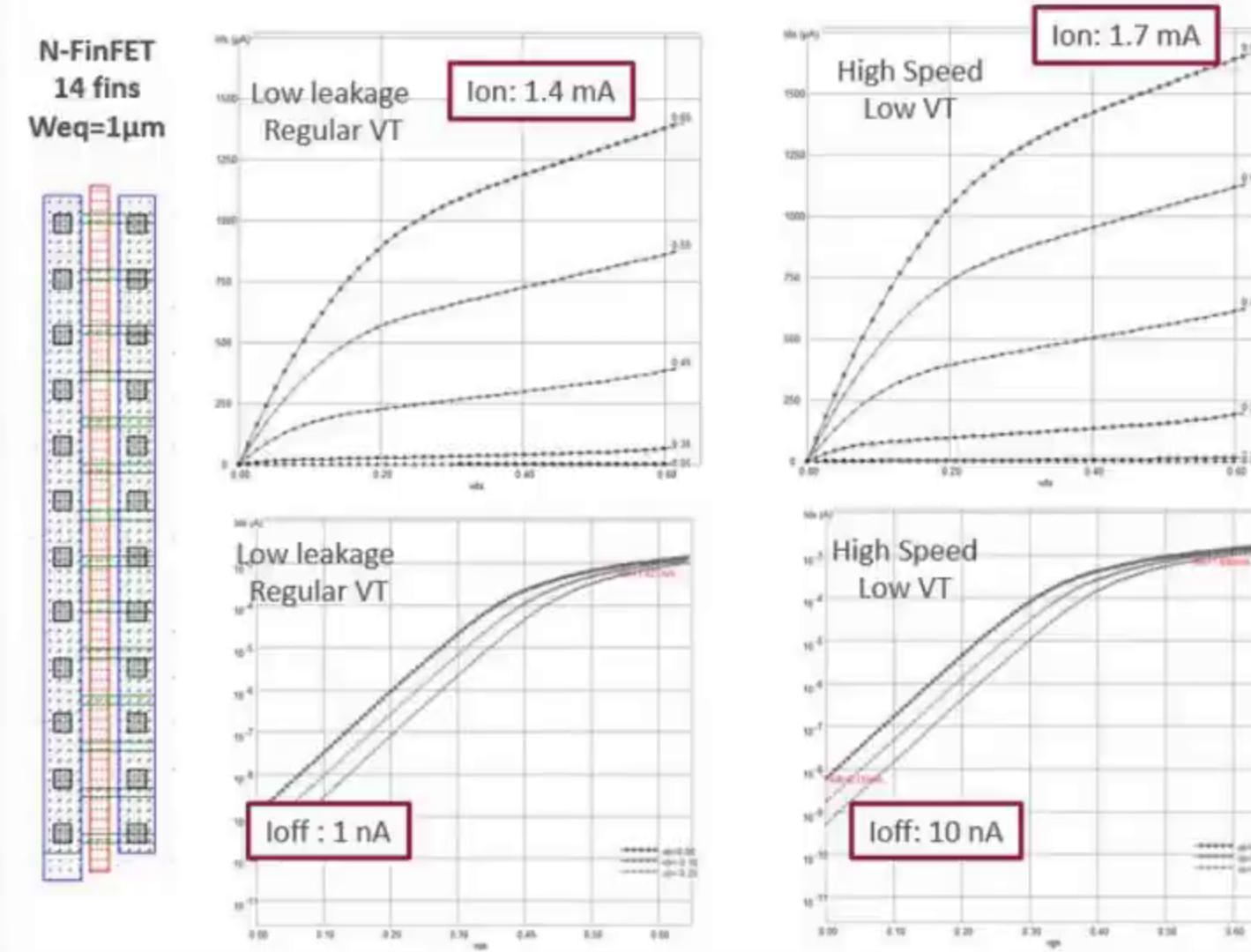
舉例: 7納米顧客的IdVg要求 ASAP7 PDK

- 從顧客的角度來看，他根本不管代工廠如何做到，例如他要所有**短通道**的RVT的漏電流(無外加電壓 $V_{gs}=0$)必須只能有**1nA/ μm** ，然而他還要求在外加電壓只有區區**0.7V**的時候，電流必須是**1.4mA/ μm** ，這是漏電流**1nA**的**140萬倍**
- 然而，他的下一個要求(使手機加速)，卻是漏電流可以有**10nA/ μm** ，而電流必須是**1.7mA/ μm**
 - 注意：電流只增加了**20%**，但是漏電流卻增加了**10倍**，還真有些划不來，因此你手機裡的RVT線路最多(**60-80%**)



舉例: 7納米顧客的IdVg要求 ASAP7 PDK

- 從顧客的角度來看，他根本不管代工廠如何做到，例如他要所有**短通道**的RVT的漏電流(無外加電壓 $V_{gs}=0$)必須只能有**1nA/ μm** ，然而他還要求在外加電壓只有區區**0.7V**的時候，電流必須是**1.4mA/ μm** ，這是漏電流**1nA**的**140萬倍**
- 然而，他的下一個要求(使手機加速)，卻是漏電流可以有**10nA/ μm** ，而電流必須是**1.7mA/ μm**
 - 注意：電流只增加了**20%**，但是漏電流卻增加了**10倍**，還真有些划不來，因此你手機裡的RVT線路最多(**60-80%**)



舉例：TSMC對7納米顧客要求的反應

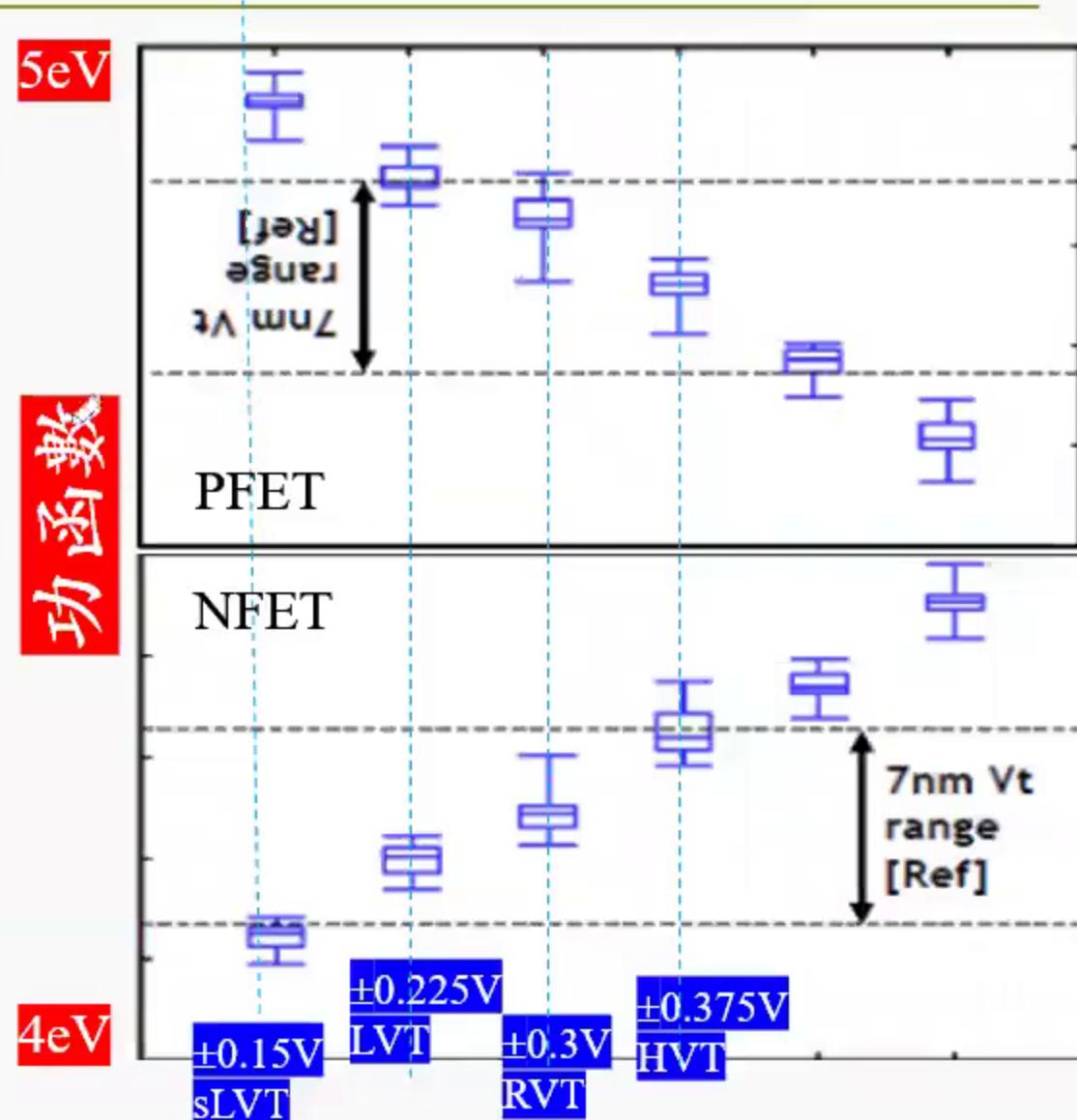
重點：TSMC宣稱其7nm製程滿足顧客要求

5eV

- 右圖所示為功函數與V_t的直接關係，此圖乃是晶圓代工成王敗寇的關鍵之一
- 製程之重要性體現於其”定位 (positioning) ”與”西格瑪 (sigma)：制程變化控制”
- “定位”由所選擇的金屬與其流程所決定 (見金屬閨密篇)
- ”西格瑪σ”全靠製程控制的精密程度(此乃各家不傳之密，而且其中甚至包含許多不為人知的“人為因素”)
- 下頁我們舉個簡單的例子來看

功函數

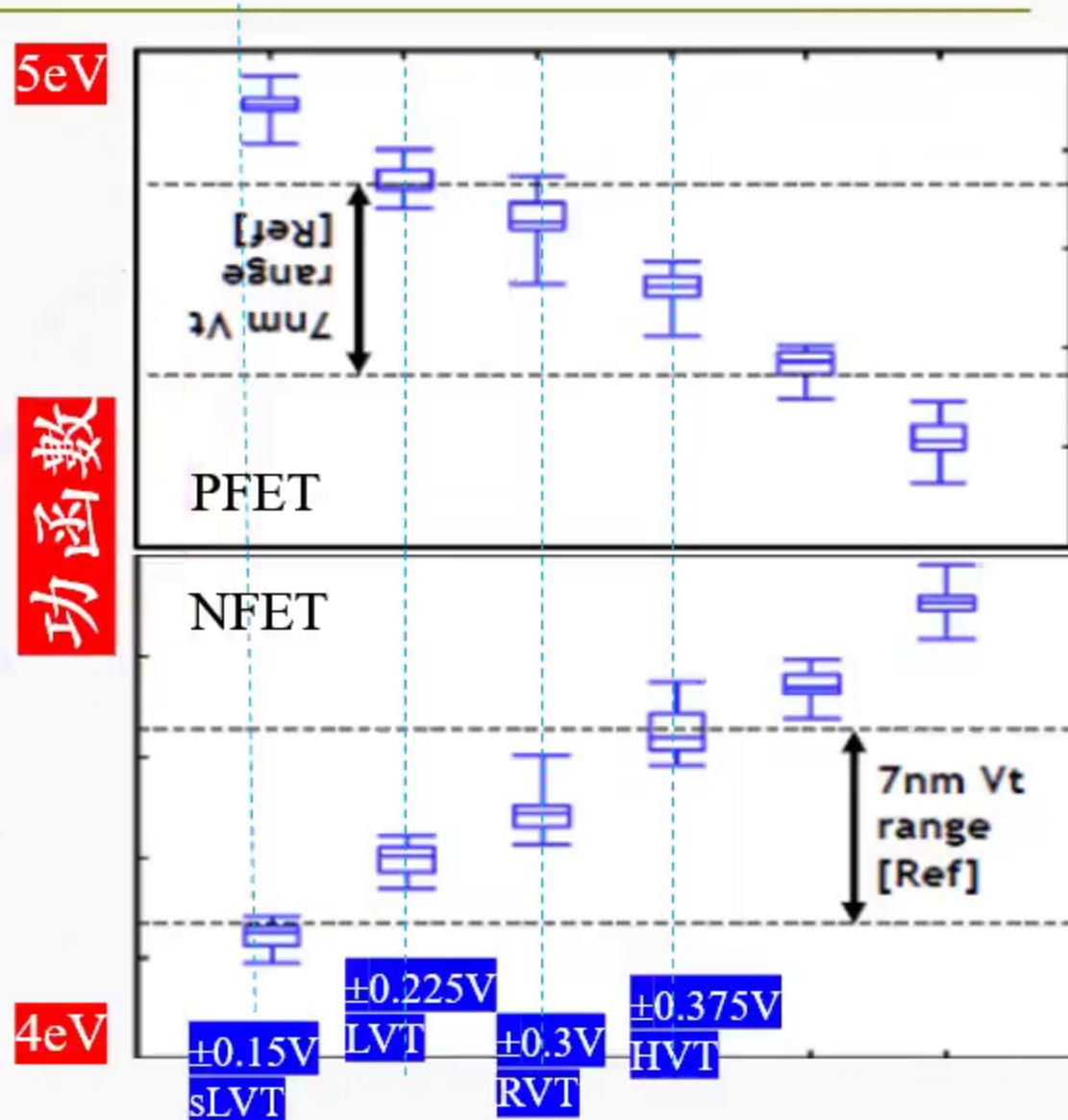
4eV



舉例：TSMC對7納米顧客要求的反應

重點：TSMC宣稱其7nm製程滿足顧客要求

- 右圖所示為功函數與V_t的直接關係，此圖乃是晶圓代工成王敗寇的關鍵之一
- 製程之重要性體現於其”定位 (positioning) ”與”西格瑪 (sigma)：制程變化控制”
- “定位”由所選擇的金屬與其流程所決定 (見金屬閨密篇)
- ”西格瑪σ”全靠製程控制的精密程度(此乃各家不傳之密，而且其中甚至包含許多不為人知的“人為因素”)
- 下頁我們舉個簡單的例子來看



試問: $\sigma V_t \sim 30\text{mV}$ 還好嗎?

解答: 大概要完蛋了

- 我們看前頁x-axis, 即之各 V_t 之間的間隔其實很小, 約只有75mV
- 若某製程有個很小很小的問題, 使得其 $\sigma V_t \sim 33\text{mV}$ (如右圖所示), 表示製程正態分布3 σ 為 $\pm 99\text{mV}$, 此值已經 $>> 75\text{mV}$
- 表示無法區分 V_t 之間的間隔(完了)

再問: 那麼多少個原子缺陷就會產生這麼大的 σV_t 呢?

解答: 平均只需要一兩個就夠了
(Mamamia!!)

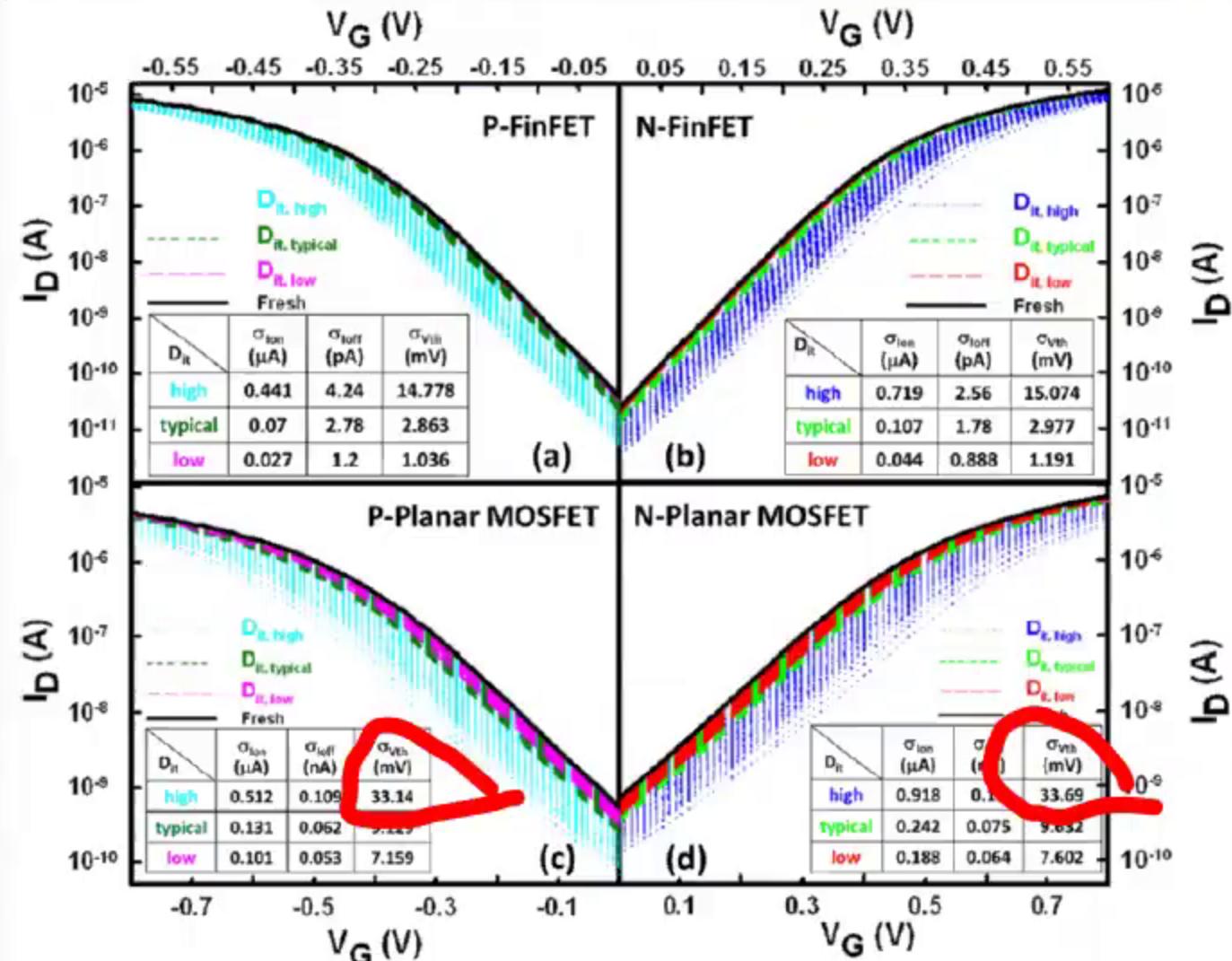


Figure 2 I_D - V_G curves of the studied devices with different D_k levels. The line indicates the I_D - V_G of a fresh sample. (a, b) n-/p-type bulk FinFET and (c, d) n-/p-type planar MOSFET devices.

試問: $\sigma V_t \sim 30\text{mV}$ 還好嗎?

解答: 大概要完蛋了

- 我們看前頁x-axis, 即之各 V_t 之間的間隔其實很小, 約只有75mV
- 若某製程有個很小很小的問題, 使得其 $\sigma V_t \sim 33\text{mV}$ (如右圖所示), 表示製程正態分布3 σ 為 $\pm 99\text{mV}$, 此值已經 $>> 75\text{mV}$
- 表示無法區分 V_t 之間的間隔(完了)

再問: 那麼多少個原子缺陷就會產生這麼大的 σV_t 呢?

解答: 平均只需要一兩個就夠了
(Mamamia!!)

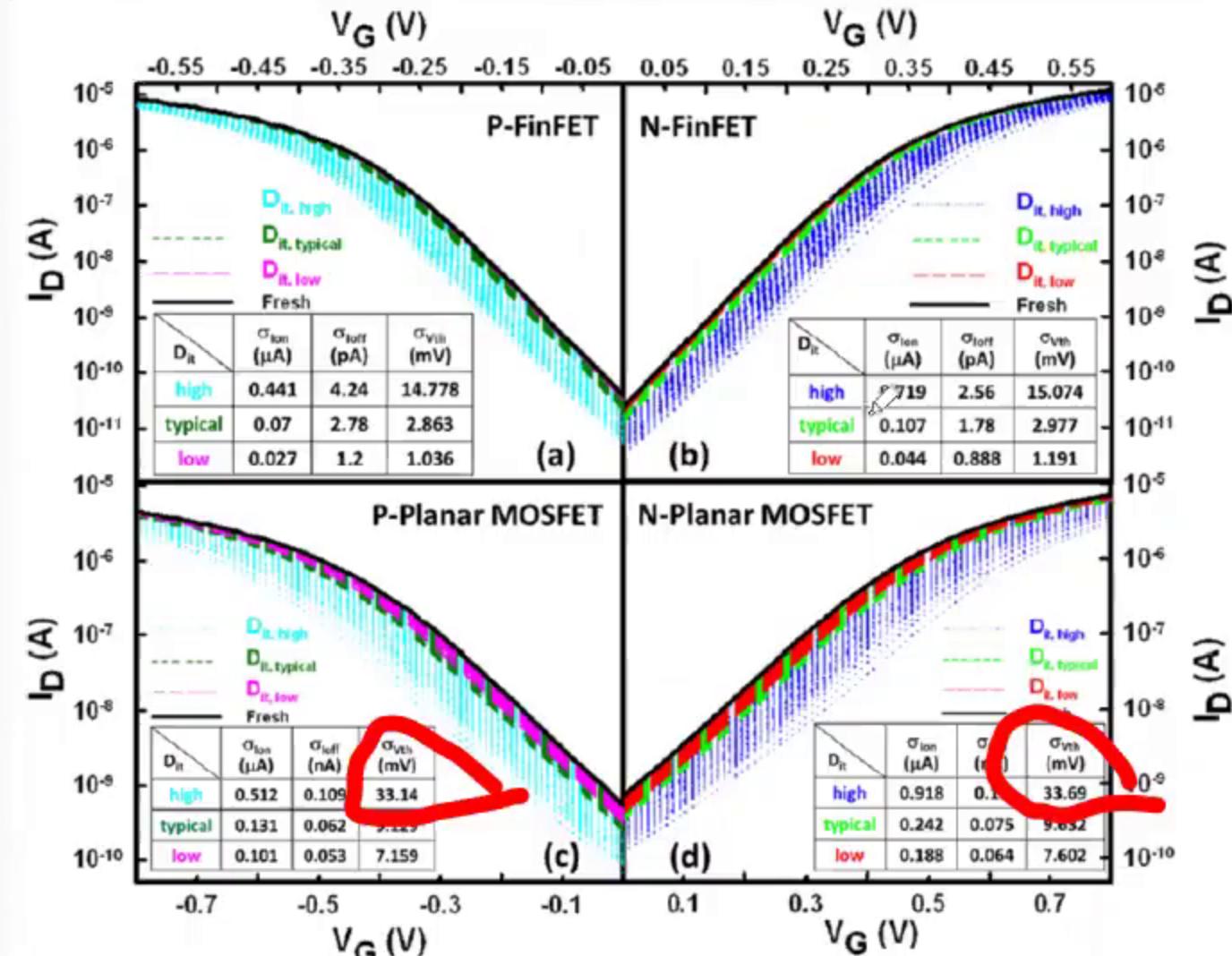
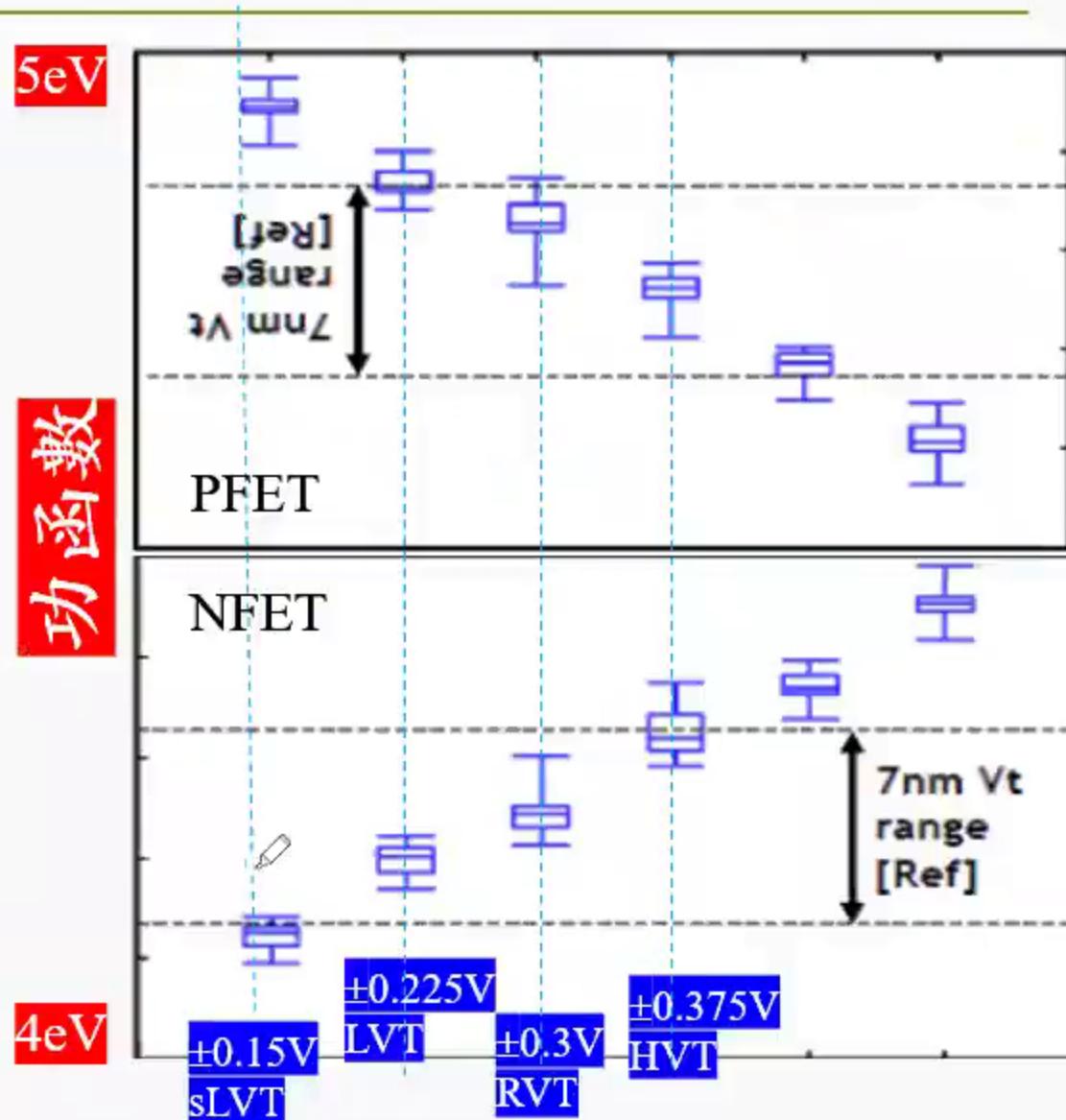


Figure 2 I_D - V_G curves of the studied devices with different D_k levels. The line indicates the I_D - V_G of a fresh sample. (a, b) n-/p-type bulk FinFET and (c, d) n-/p-type planar MOSFET devices.

舉例：TSMC對7納米顧客要求的反應

重點：TSMC宣稱其7nm製程滿足顧客要求

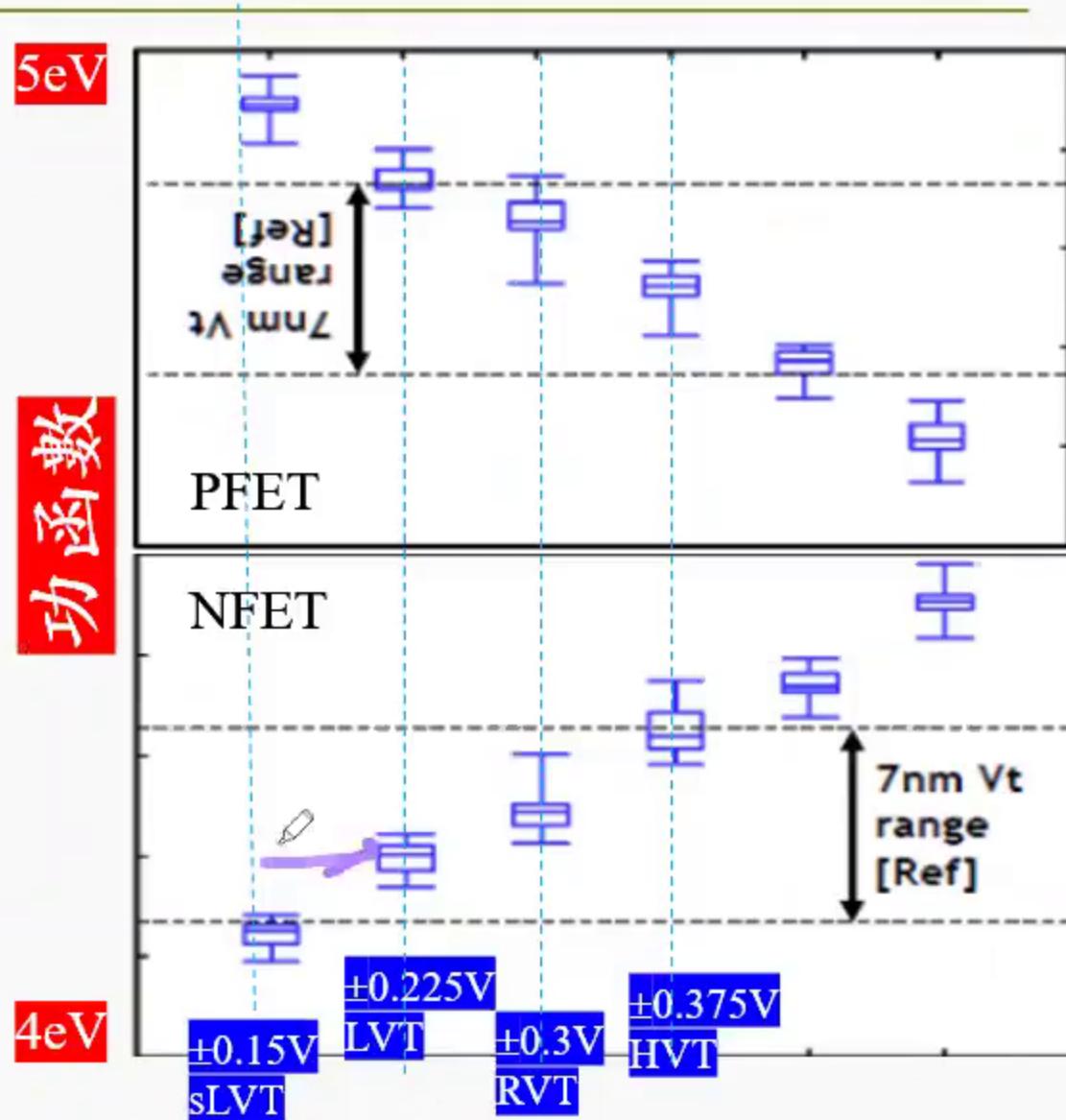
- 右圖所示為功函數與V_t的直接關係，此圖乃是晶圓代工成王敗寇的關鍵之一
- 製程之重要性體現於其”定位 (positioning) ”與”西格瑪 (sigma)：制程變化控制”
- “定位”由所選擇的金屬與其流程所決定 (見金屬閨密篇)
- ”西格瑪σ”全靠製程控制的精密程度(此乃各家不傳之密，而且其中甚至包含許多不為人知的“人為因素”)
- 下頁我們舉個簡單的例子來看



舉例：TSMC對7納米顧客要求的反應

重點：TSMC宣稱其7nm製程滿足顧客要求

- 右圖所示為功函數與V_t的直接關係，此圖乃是晶圓代工成王敗寇的關鍵之一
- 製程之重要性體現於其”定位 (positioning) ”與”西格瑪 (sigma)：制程變化控制”
- “定位”由所選擇的金屬與其流程所決定 (見金屬閨密篇)
- ”西格瑪σ”全靠製程控制的精密程度(此乃各家不傳之密，而且其中甚至包含許多不為人知的“人為因素”)
- 下頁我們舉個簡單的例子來看



附錄：為何 I_d 的單位是mA/ μm ？



解答：因為要公平！

- 由右上圖即知每一個新世代的鰭都是不同的，基本上是越來越約高瘦(高/瘦比約為2.5)，因此每根鰭產生的電流也因此必有不同

再問：如何讓各世代之間的電流(I_d)能相互公平比較呢？

解答：業界同意以 $1\mu m$ (即之Weq)內所生所有電流為共同標準

- 例如右下圖某7nm所示，若鰭高 $H = 40nm$ ，鰭瘦 $W = 6nm$ ，則 $1\mu m$ 內所含的鰭晶體為 $1\mu m/(2 \times 40nm + 6nm) \sim 12$ 根

Fin Shape Evolution

	22nm	14/16nm	10nm	7nm	L/W ratio ~2.5
Channel length	25	22	19	16	
Fin width	10	9	8	7	
Fin height	34	42	~50	50+	
Aspect ratio	3 : 1	5 : 1	6 : 1	7 : 1	

