Introducing 7-nm FinFET technology in Microwind

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This paper describes the implementation of a high performance FinFET-based 7-nm CMOS Technology in Microwind. New concepts related to the design of FinFET and design for manufacturing are also described. The performances of a ring oscillator layout and a 6-transistor RAM memory layout are also analyzed.

1. Technology Roadmap

Several companies and research centers have released details on the 7-nm CMOS technology, as a major step for improved integration and performances, with the target of 4-nm process by 2025. We recall in table 1 the main innovations over the past recent years.

Technology node	Year of introduction	Key Innovations	Application note
180nm	2000	Cu interconnect, MOS options, 6 metal layers	
130nm	2002	Low-k dielectric, 8 metal layers	
90nm	2003	SOI substrate	[Sicard2005]
65nm	2004	Strain silicon	[Sicard2006]
45nm	2008	2nd generation strain, 10 metal layers	[Sicard2008]
32nm	2010	High-K metal gate	[Sicard2010]
20nm	2013	Replacement metal gate, Double patterning, 12 metal layers	[Sicard2014]
14nm	2015	FinFET	[Sicard2017]
10nm	2017	FinFET, double patterning	[Sicard2017]
7nm	2019	FinFET, quadruple patterning	This application note
5nm	2021	Multi-bridge FET	

Table 1: Most significant technology nodes over the past 15 years

Improved performances

The power, performance and area gains are an important metric for justifying a shift from older technology nodes to new ones.

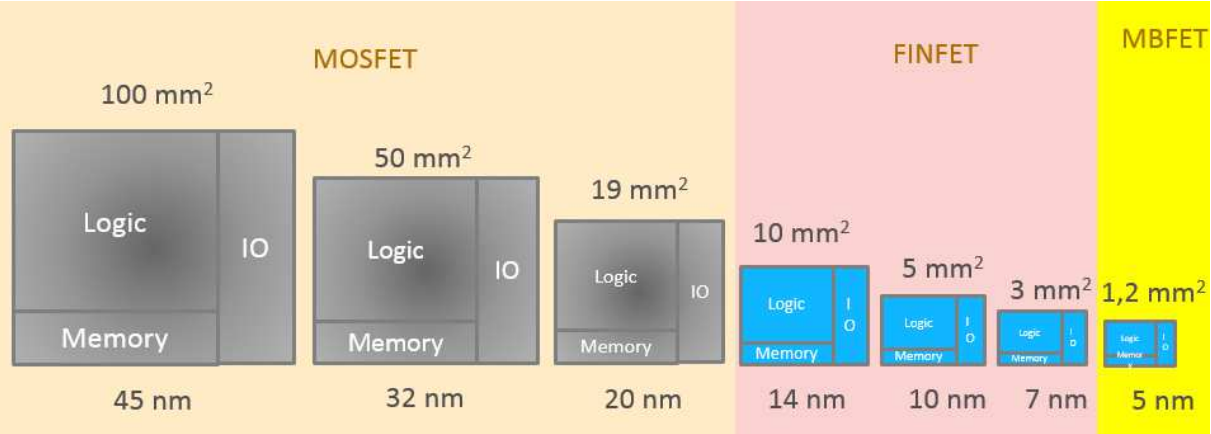


Figure 1: The spectacular reduction of feature sizes from 45 to 7nm (adapted from [Mistry2017])

As compared to 14-nm technology node, the 7-nm technology offers [Brain2017, Mistry2017]:

- More than 50 % less power consumption. This is a key feature for mobile industry for which the battery life is the top one problem.
- 20 to 50 % increase in switching performance. This is equally important in server applications and smartphones, which use faster processors and higher resolution screens.
- 4 times higher density. This is a key advantage to produce the lightest and thinnest possible smartphones.

The giant cost of fab and IC design in 7-nm

The movement from node to node has been observed every 2 years, at a regular rate. In 2017, the IC manufacturing was getting into 7nm, but the transition to 5nm was predicted to appear in more that 2 years. The reason for this potential slowing down is because profitability is jeopardized by design and manufacturing costs. Until the 28-nm node, the design cost was below 100 M$. Economic gain could be ensured by high IC unit costs and high volumes, which is the case for SoC for smartphones and laptops.

Company	Logo	Technology name
Intel	intel	10nm, 10nm+, 10nm++
Samsung	SAMSUNG	10nm, 8nm, 7nm, 6nm, 5nm, 4nm
TSMC	tsmc	10nm, 7nm, 5nm
GlobalFoudries	GLOBALFOUNDRIES	7nm
IBM	IBM	7nm, 5nm

Table 2: 5 major players in the 10/7/5-nm chip manufacturing

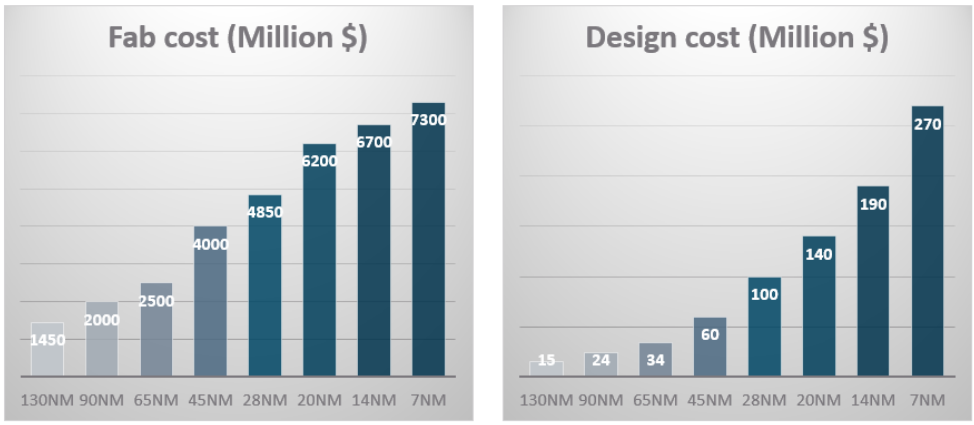


Figure 2: The extraordinary increase of the fab cost: more than 7 billion $ for a 10-7-nm process, and associated chip design cost as high as 270 M$ for a run in 7-nm.

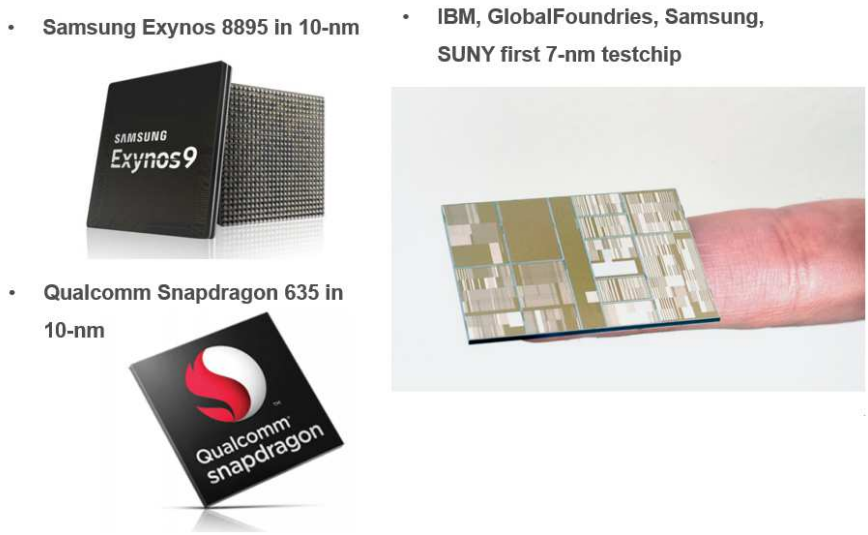


Figure 3: Examples of 10-nm processors and prototype 7-nm circuit by IBM

The consequences of the fab and chip design cost explosion have been the drastic decrease of foundries. While more than 20 foundries existed for 130nm technology, only 5 major companies are providing the 10-7nm processes (Table 2). One reason is the extraordinary fab and IC design cost on nano-CMOS designs, as illustrated in Figure 2.

In 2017, no commercial processor was yet fabricated in 7nm. IBM, GlobalFoundries, Samsung and SUNY announced the first 7-nm test chip (Fig. 3). A continuous increase in switching performance has been made possible thanks to several innovations, as shown in Figure 6. Starting 14-nm, the MosFET is replaced by the FinFET, for improved current capabilities. According to Samsung and IBM, the 7-nm technology could be the last one to use Fin-FETs, which has reached its physical limits, and could be replaced starting 5-nm node by multi-bridge FETs with gate all around stacked fins, which consume far less power, according to IBM researchers.

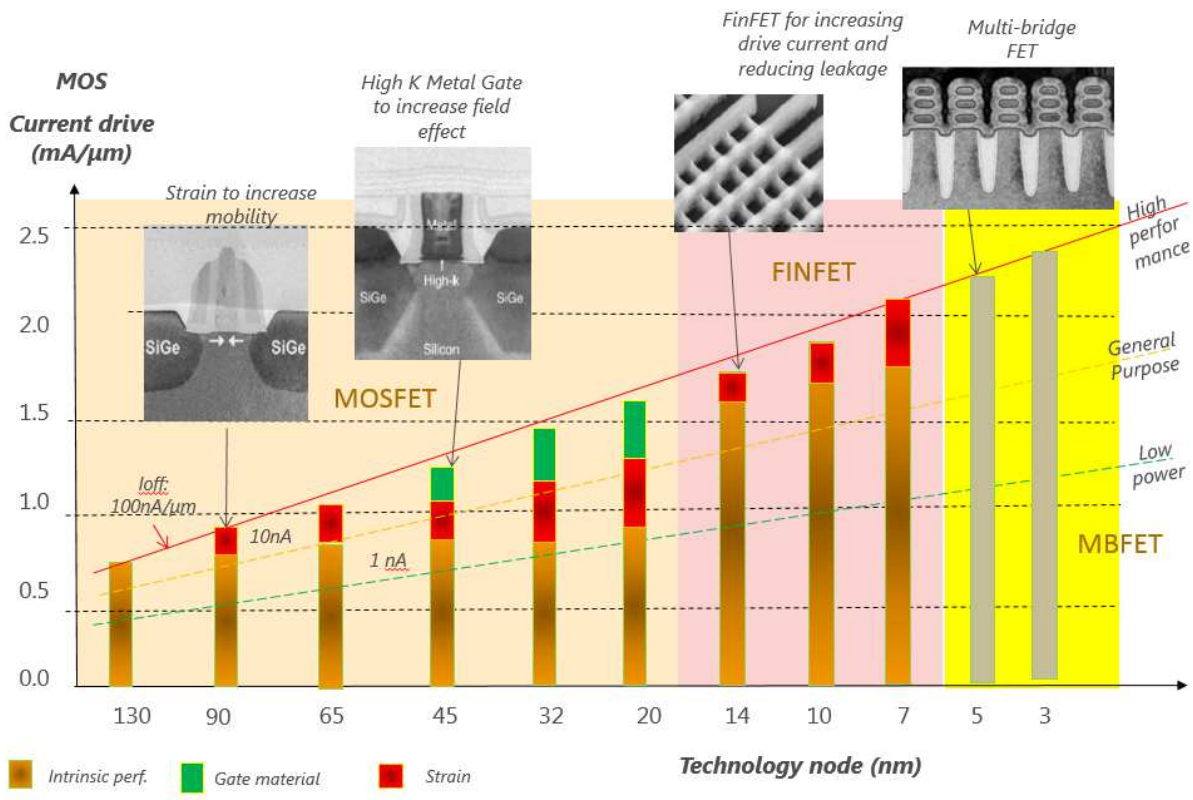


Figure 4: Increased switching speed capabilities over technology nodes

Power supply operation

The supply voltage, both internal to the cores and the external I/O supply have been continuously decreased due to the thinning of the gate oxide and faster switching rates thanks to reduced voltage swings. The 7-nm technology operates around 0.6 V, while I/Os are supplied at 1.0, 1.2, 1.5 V (Fig. 5).

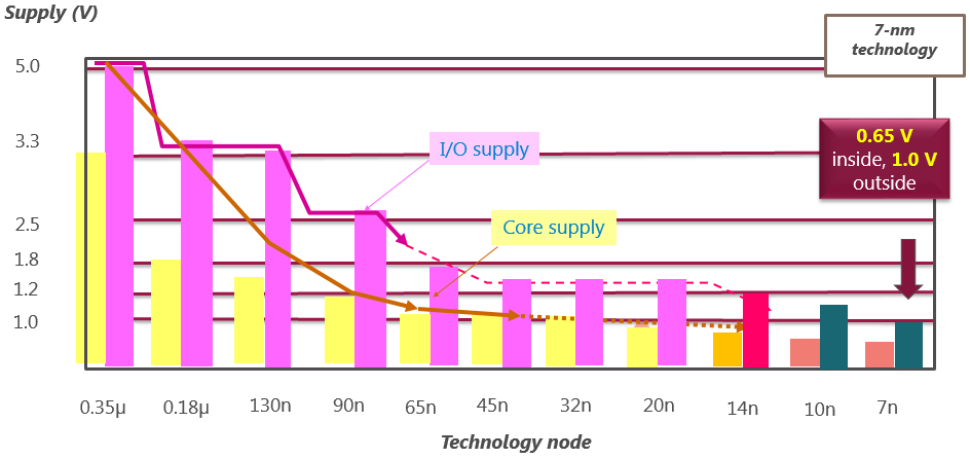


Figure 5: The core supply voltage in 7nm technology is 0.65 V, with typical IO voltage of 1.0 V

2. Key features of the 7-nm technology

Equivalent Gate oxide

The FinFET switch is made of titanium nitride gate (TiN) with a combined hafnium oxide (HfO_2) and silicon oxide (SiO_2) for insulator. Hafnium-based oxides were introduced as a replacement for silicon oxide for improved field-effect in the transistor channel. The dielectric constant of HfO2 is near 20, more than 5 times the dielectric constant of SiO2 (around 4). The distances between the O atoms and the Hf-atom range between 0.21 and 0.24 nm, the Si-Si distance is 0.23 nm, while the O-O distance is 0.26 nm. The formulation of the equvalent oxide thickness (EOT) if all the oxide was SiO2 is as follows:

$$\mathrm{EOT} = \mathrm{n.d_{SiO2}} + \mathrm{Th} \times \epsilon_{\mathrm{SiO2}}/\epsilon_{\mathrm{HfO2}}$$

- EOT is around 0.65 nm for 7-nm technology [Hashemi2016], as seen in Table 3.
- $\mathrm{d_{SiO2}}$ is the distance between 2 SiO_2 atoms = 0.2 nm
- n is the number of SiO_2 atoms (2 or 3)
- T_h is the thickness of HfO_2 (3 nm in 14-nm, 1.4 nm in 7-nm)
- ϵ_{SiO2} = 4, ϵ_{HfO2}= 20

EOT 7nm	Low leakage RVT	High speed HS	High Voltage HVT
Parameter in RUL file	b4t2ox	b4t2ox	b4t3ox
n-Channel FinFET (nm)	0.65	0.65	2.0
p-Channel FinFET (nm)	0.65	0.65	2.0

Table 3: Equivalent oxide thickness of 7-nm devices in Microwind

2D view at atomic scale

In Microwind, the 2D view of the process may be turned to an atomic scale view of the layers. As the distance between 2 Si atoms is 0.235 nm, a 7-nm fin is equivalent to 20 atoms.

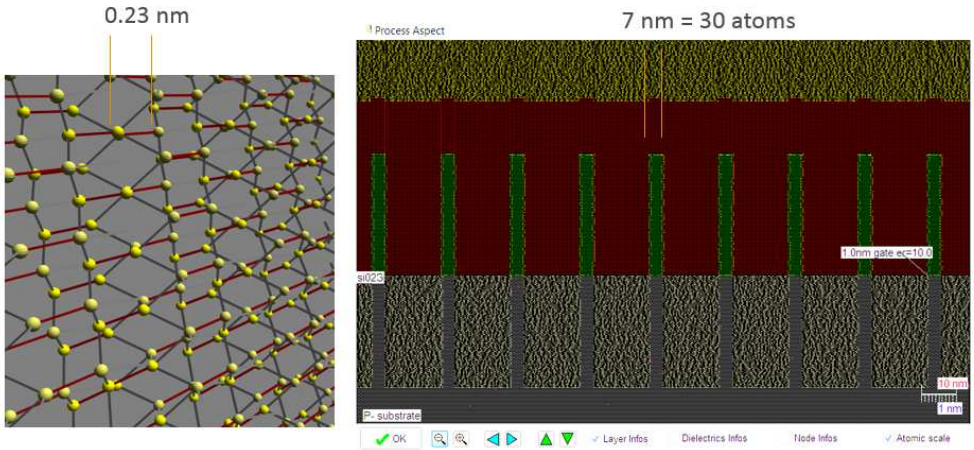


Figure 6: View of the silicon lattice and atomic scale view of the fin-FET in 7-nm

Still the FinFET

The FinFET device has a different layout style than the MOS device. Instead of a continuous channel, the FinFET uses fins (Figure 7), which provide the same current at size more than 3 times smaller (Fig. 8). FinFET also provides a lower leakage current (Ioff) at the same (Ion). High density (HD) designs use 2 fins, high performance (HP) designs 4 fins or more.

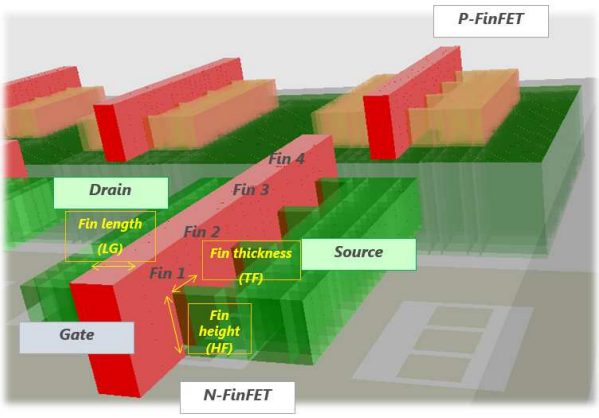


Figure 7: 3D view of the 4-fin FinFET and illustrations of the Fin height (HF), Fin Thickness (TF) and Fin Length (LG).

Lambda

In Microwind, we use an integer unit for drawing, called λ ("lambda") which is fixed to 4 nm for 7-nm CMOS process (Table 4).

- The drawn gate length is 2 λ that is 8 nm.
- The fin width is 1 λ that is 4 nm.
- The lower metal pitch is 24 nm.

Microwind parameter	Unit	Code	Name in rule file	7-nm process
Lambda	nm	λ	lambda	4
Core supply	V	VDD	Vdd	0.65
Fin Width	λ	WF	R301	1
Fin pitch	λ	FP	R308	6
Fin Height	nm	HF	thdn	35
Gate height	nm	GH	thpoly	50
Gate length	λ	GL	R302	2
Gate pitch	λ	GP		6
Contact size	λ	CS	R401	2
EOT	Nm	EOT	b4toxe	0.65
M1 pitch	λ		R501+R502	6

Table 4: key parameters of the 7-nm processes used to configure Microwind rule file Cmos7n.RUL

Core MOS devices

Publications from foundries regarding 7-nm technology rarely give detailed numbers regarding precise currents & voltages, and usually refer to "arbitrary units" (A. U.) [Wu2016, Xie2016, Steegen2015]. Another approach proposed by [Clark2016] consists in proposing a set of parameters interpolated from previous technology nodes, and tuned to available experimental data. We follow a similar approach and try to propose numbers close to average performances.

Table 4 gives an overview of the key parameters for the 7-nm technological node concerning the internal MOS devices and layers. Four threshold options, namely high-Vt (HVT), regular Vt (RVT), low Vt (LVT) and Super low VT (SLVT) are usually proposed [Clark2016]:

- HVT – High Threshold Voltage causes less power consumption, but switching is slow. HVT are used in power critical functions. Ioff is around 0.1 nA/µm, Idsat around 1.2 mA/µm.
- RVT – Regular Threshold Voltage (sometimes called Standard VT or SVT) offers trade-off between HVT and LVT i.e., moderate delay and moderate power consumption. Ioff is around 1 nA/µm, Idsat around 1.4 mA/µm.
- LVT – Low Threshold Voltage causes more power consumption and switching timing is optimized. LVT are used in time critical functions. Ioff is around 10 nA/µm, Idsat around 1.6 mA/µm.
- SLVT – Super Low Threshold Voltage causes even more power consumption but switch at the highest speed. SLVT are used in time-critical functions without consideration of leakage currents. Ioff is around 100 nA/µm, Idsat around 1.8 mA/µm.

The *Idsat* current for p-channel devices is almost simulare to the n-channel device. In Microwind, we only propose 2 types of devices :

- Low leakage MOS (LL), close to RVT
- High Speed MOS (HS), close to LVT

Parameter	In Microwind
V_{DD} core (V)	0.65
Effective gate length (nm)	12
MOS variants	2
Ion N (mA/µm) at 0.6 V	1.4 (LL) 1.7 (HS)
Ion P (mA/µm) at 0.6 V	1.3 (LL) 1.6 (HS)
Ioff N (nA/µm)	1 (LL) 10 (HS)
Ioff P (nA/µm)	1 (LL) 10 (HS)
Gate dielectric	SiO_2, HfO_2
Gate stack	Al/TiN
Equivalent oxide thickness (nm)	0.65

Table 5: Key features of the core devices proposed in the 7-nm technology

IO MOS devices

Table 6 gives an overview of the key parameters for the 7-nm technological concerning the Input/output MOS devices and associated supply voltage. In Microwind, we only consider 1.0 V I/O supply and tune the "High-Voltage" (HV) MOS device on the median performances.

Parameter	High Voltage (HV) MOS in Microwind
VDD IOs (V)	1.0
Effective gate length (nm)	100
Ion N (mA/µm)	0.5
IonP (mA/µm)	0.4
Ioff N (nA/µm)	0.1
Ioff P (nA/µm)	**0.1**

Table 6: Key features of the I/O devices proposed in the 7-nm technology and corresponding values in Microwind

3. Transistor performances in 7-nm technology

Designing a 1µm-width FinFET

The evaluation of the equivalent FinFET channel width corresponds to the following formulation (Eq. 1). The evaluation of the current is usually expressed in mA/µm, meaning that a 1-µm equivalent width FinFET design is needed to evaluate the current. In the proposed 7-nm technology, HFIN is 35 nm, WFIN 4 nm, so one fin has an equivalent width of 74 nm (Figure 8).

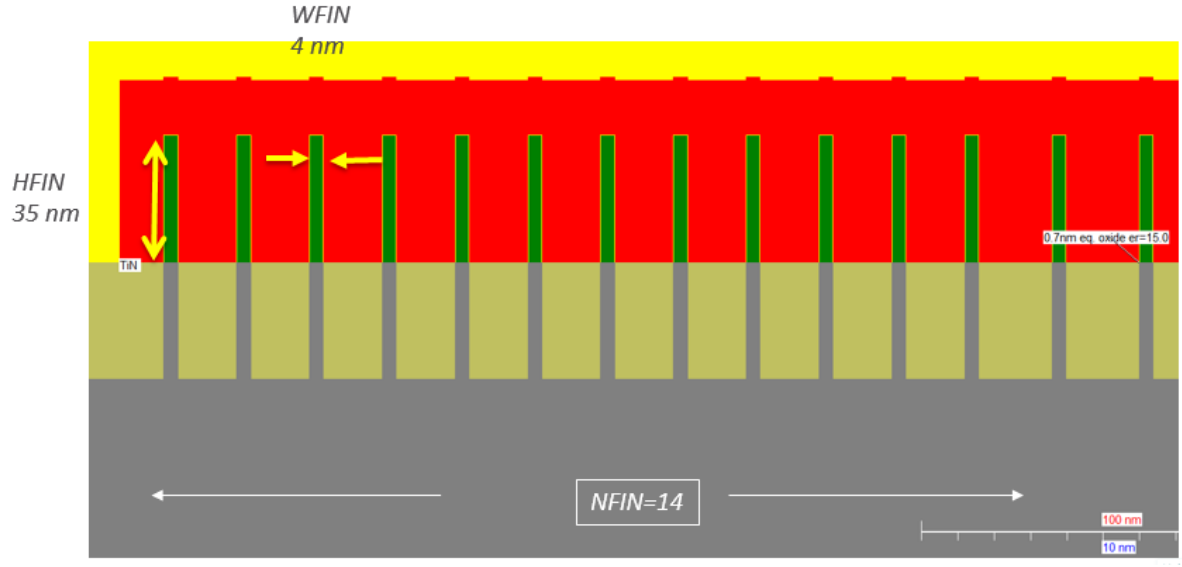


Figure 8: The equivalent width of a multi-fin FET

$$Weq = (2 \times H_{FIN} + W_{FIN}) \times N_{FIN} \quad \text{Eq. 1}$$

$$Weq = (2 \times 35 + 4) \times 14 = 1036\,nm \approx 1\,\mu m \quad \text{Eq. 2}$$

An equivalent width of 1µm, as it would be designed using MosFET's, corresponds to around 14 fins in 7-nm technology. As seen in Fig. 9, the FinFET with a 1-µm width is 3 times smaller than a MosFET with the same width. We get the following I/V characteristics (Fig. 19) for n-channel FinFET and p-channel FinFET.

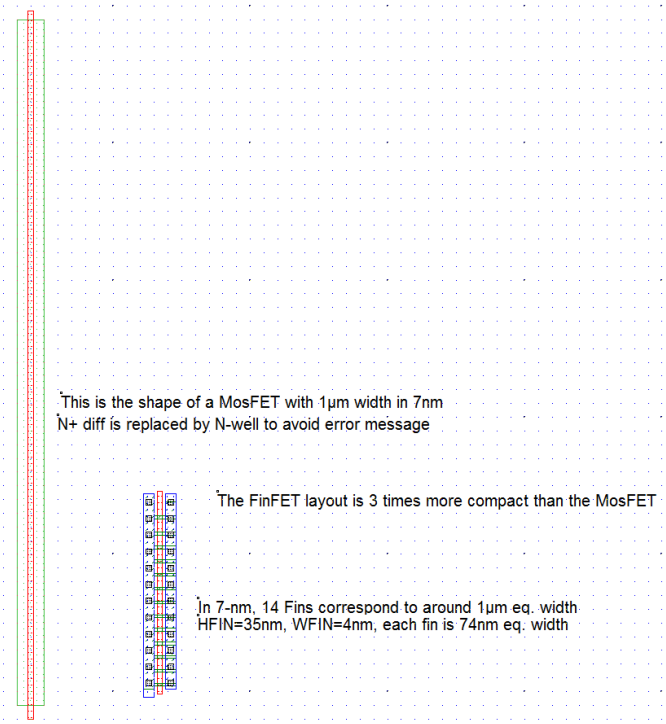


Figure 9: The 7-nm multi-fin FET with an equivalent width of 1 µm is three times more compact than the MosFET traditional design

n-FinFET characteristics

The I/V characteristics of the low-leakage and high-speed FinFET devices (Fig. xxx) are obtained using the MOS model BSIM4. As shown in the figures, the low-leakage NMOS has a drive current capability of around 1.4 mA with 14 fins (equivalent to W=1.0 µm) at a voltage supply of 0.65 V. For the high speed NMOS, the drive current rises to 1.7 mA/µm.

The drawback associated with this high current drive is the leakage current which rises from 1 nA/µm (low leakage NMOS) to 10 nA/µm (high speed NMOS), as seen in the Id/Vg curve at the X axis location corresponding to Vg= 0 V. From a design view-point, the "option" menu in the MOS generator enables to switch from low leakage to high-speed. In terms of layout, the only difference is the option layer that contains the MOS option information which can be Low leakage (Regular Vt), High Speed (Low VT), or High Voltage.

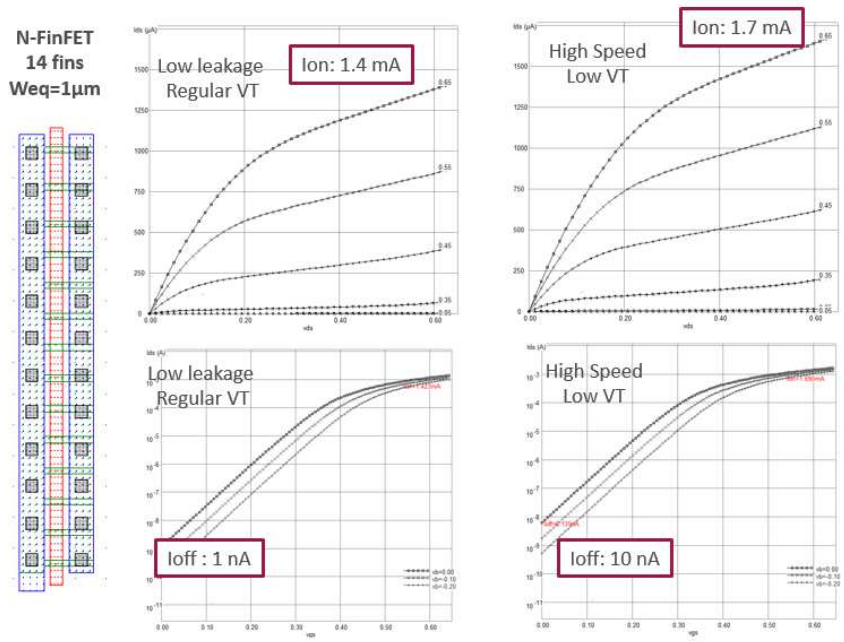


Figure 10: Id/Vd characteristics of the low leakage and high speed n-channel FinFET devices.

P-channel MOS device characteristics

The p-FinFET drive current in 7-nm technology is quite similar to the n-FinFET thanks to the strain engineering for p-channel that nearly compensates the intrinsic mobility degradation of holes (P-channel) vs. electrons (N-channel). The leakage current is around 1 nA/µm for the low-leakage device and nearly 10 nA/µm for the high-speed device (Fig. 11).

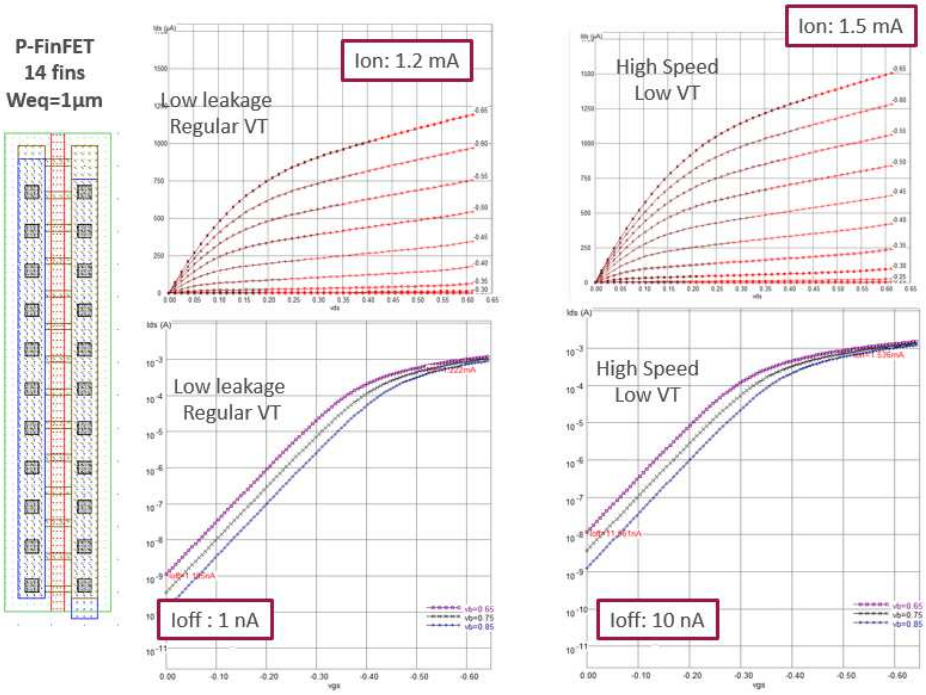


Figure 11: Id/Vg characteristics of the low leakage and high-speed p-FinFET devices

Subthreshold slope

The sub-threshold slope (SS) is measured for Vgs significantly lower than the threshold voltage VTO. It consists in evaluating the mV per decade of current Ids. The SS is around 70 mV/decade when measured from 10^{-7} A to 10^{-6} A. The SS is controlled in BSIM4 model by parameter NFACT (Fig. 12). It is expected that new devices such as Gate-All-Around FET will have SS around 65 mV/decade or less [Huang2015].

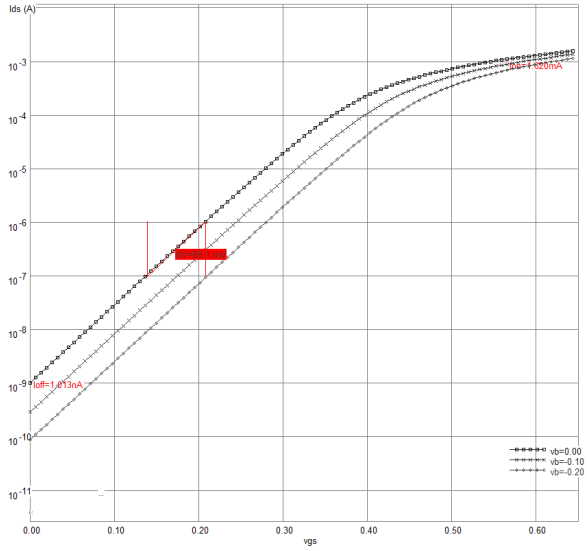


Figure 12: Evaluation of the sub-threshold slope for a LL device: around 70mV/decade

Difference between Ion, Idsat and Ieffective

The terms *Ion* and *Idsat* correspond to the same metrics that reflect or represent the performance of a transistor. *Ion* is the current delivered by the device at nominal supply voltage *VDD* for the drain/source voltage *Vds* and *VDD* also for the gate/source voltage *Vgs*. *Ion* is often compared to *Ioff*, the *Ids* current for *Vgs*=*VDD* and *Vds*=0. Publications either refer to *Idsat* or to *Ion*. When comparing transistor metrics, a transistor with *Ion* =1,5 mA/µm for a given 7-nm technology at a given *Ioff*= 10 nA/µm, is better than the one with *Ion*=1,2 mA/µm with the same *Ioff*.

However, *Ion* is not the best metrics to estimate the circuit delay because, in most logic cells, the current through the n-device and p-device never really reach Ion (Fig. 13). The average current I_{eff} reached during switching operation may be approximated as the average of I_{high} and I_{low}, with the following expressions. The effective current *Ieff* is shown in Fig. 13. *Ieff* is around half of *Ion*.

- $I_{On} = I_{DSAT} = I_{DS}(V_{GS} = V_{DD}, V_{DS} = V_{DD})$
- $I_{eff} = \frac{I_{high}+I_{low}}{2}$
- $I_{low} = I_{DS}(V_{GS} = \frac{V_{DD}}{2}, V_{DS} = V_{DD})$
- $I_{high} = I_{DS}(V_{GS} = V_{DD}, V_{DS} = \frac{V_{DD}}{2})$

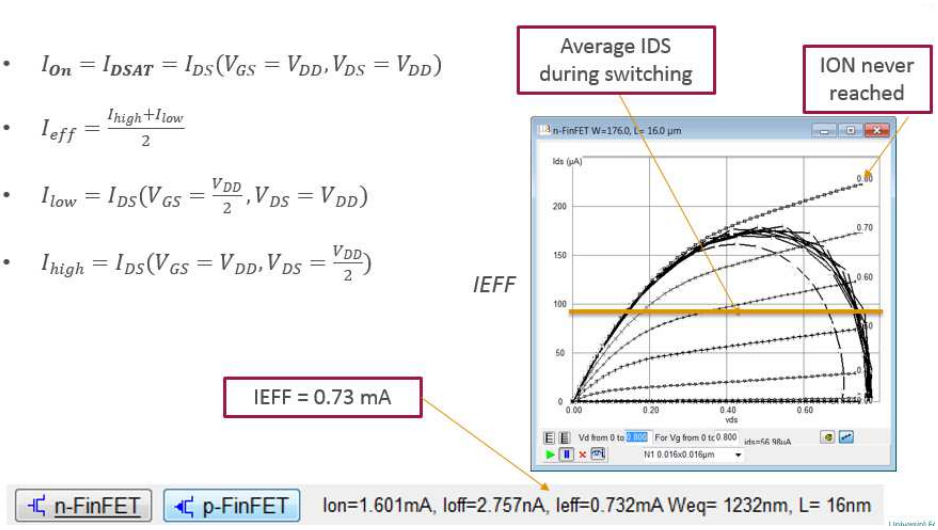


Figure 13: Difference between Ion and Ieff. The inverter switching is shown on the I/V curves.

Threshold voltage dependence on gate length

As can be seen in Fig. 14, the threshold voltage decreases when the channel length tends to its minimum value 2 λ, which is equivalent 8 nm in Microwind's 7-nm technology. Note that the minimum length for high-voltage device is 4 λ, which is 16 nm in 7-nm technology. This effect is also named threshold voltage roll-off. It is anticipated that stacked nano-wires such as Gate-All-Around (GAA) FET devices will show the least amount of VT roll-off due to their superior electrostatic integrity [Zheng2016].

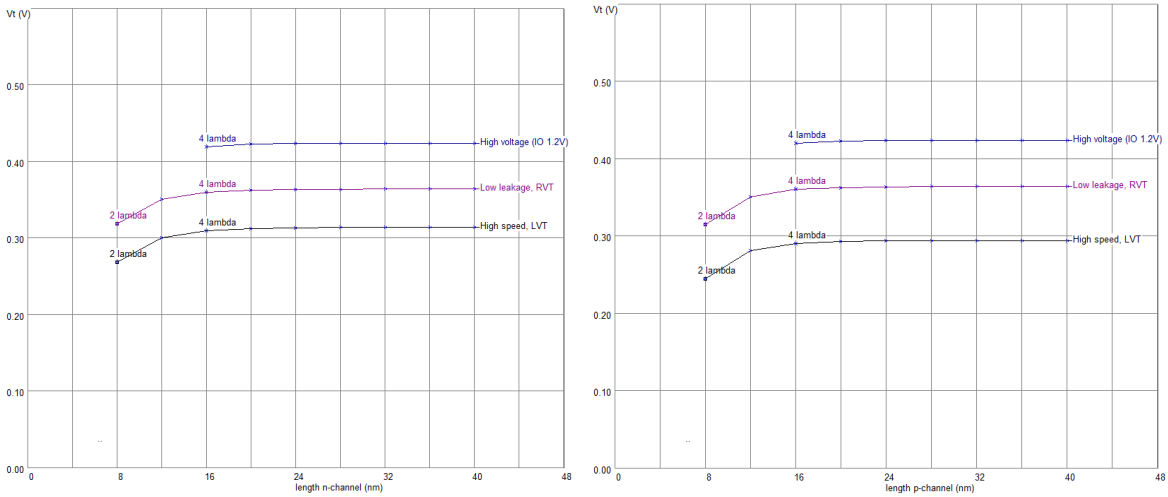
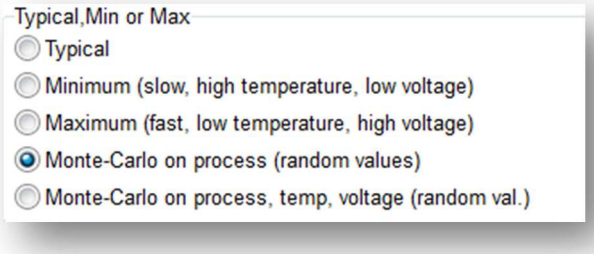


Figure 14: The threshold voltage decreases with short-channel effects (n-channel FinFET at left, p-channel FinFET at right)

Process Variability

One important challenge in nano-CMOS technology is process variability. The fabrication of billions of devices at nano-scale induces a spreading in switching performances in the same IC. The effects of process variability on the device characteristics such as Ids/Vds (Fig. 15), Ids/Vgs (Fig. 16) and Ioff/Ion (Fig. 17) may be observed by selecting the option “Monte-Carlo on process” in the Simulate > Simulation Options menu.



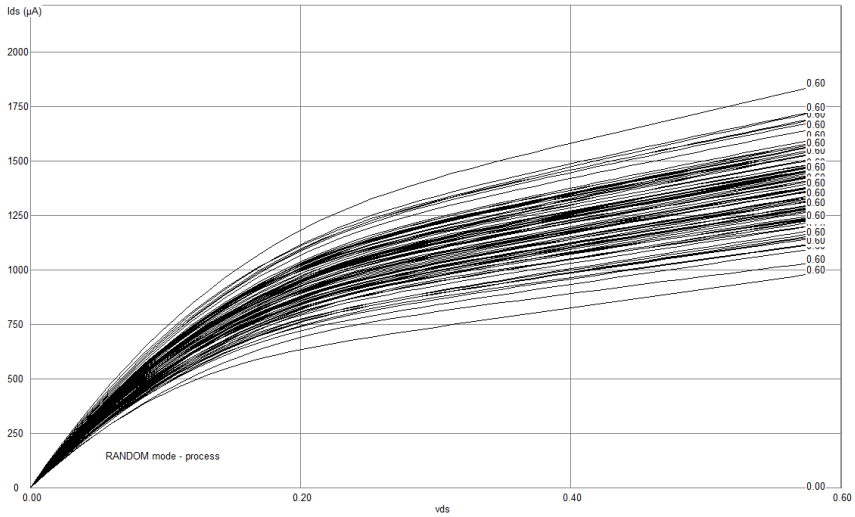


Figure 15: Ids vs Vds calculated on 100 samples of n-FinFET with random distribution of VT and U0, with a Gaussian distribution around the nominal value.

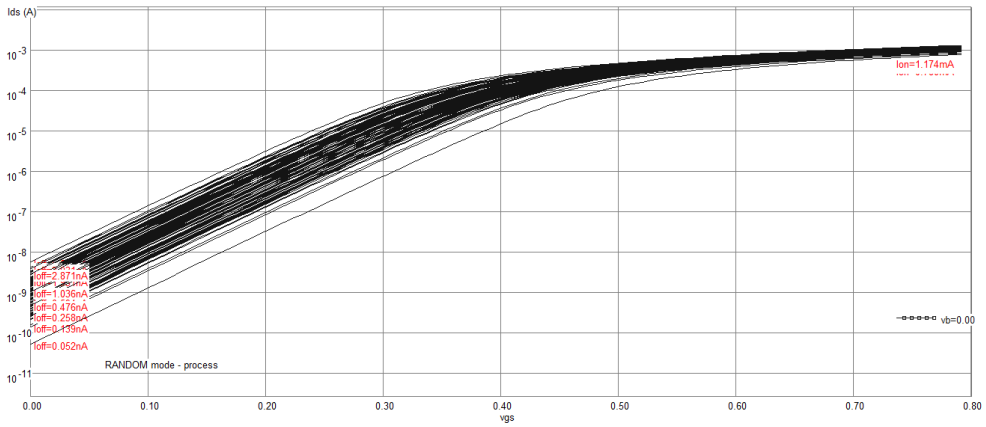


Figure 16: log(Ids) vs Vgs calculated on 100 samples of n-FinFET with random distribution of VT and U0, with a Gaussian distribution around the nominal value.

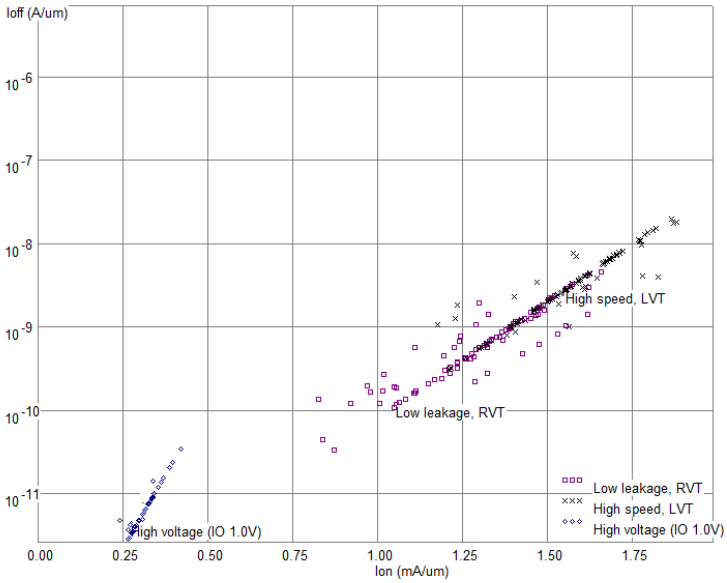


Figure 17: Ioff/Ion calculated on 100 samples of n-FinFET with random distribution of VT and U0, with a Gaussian distribution around the nominal value

4. Basic gates

The cell compiler proposed in Microwind converts into layout basic cells such as inverters, AND/OR, NAND, NOR or combinations of AND/OR gates. A very regular drawing of gates and dummy gates on both sides is required for manufacturability. The fins must also be aligned from one cell to another.

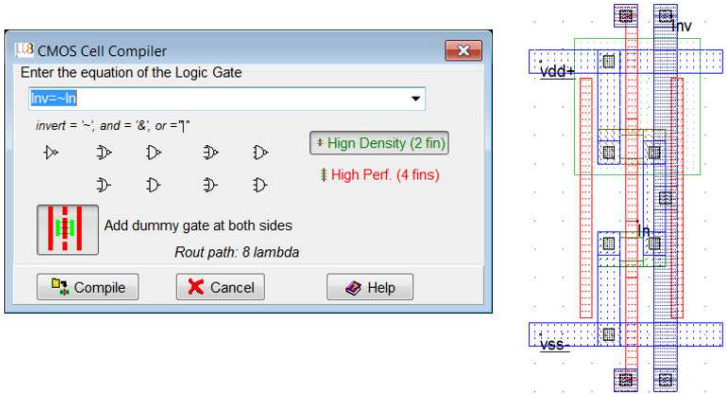


Figure 18: Compilation of a 2-fin inverter (High density option) with Microwind

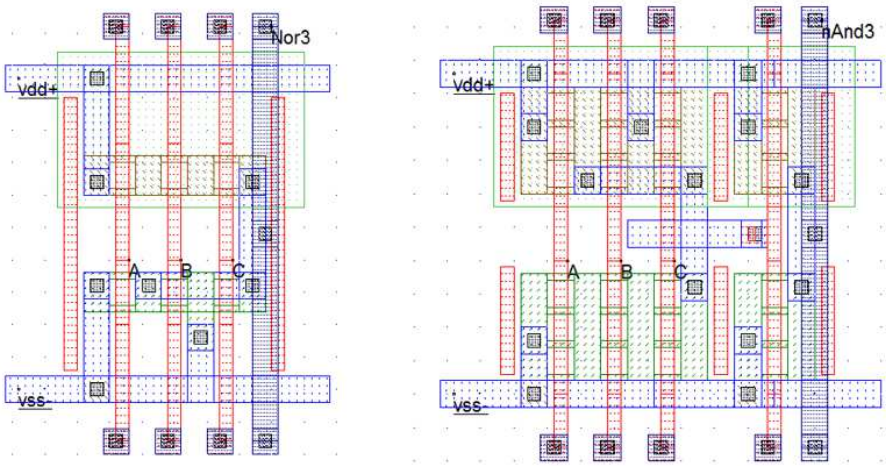


Figure 19: Compilation of a 2-fin NOR3 cell (High density) and a 4-fin AND3

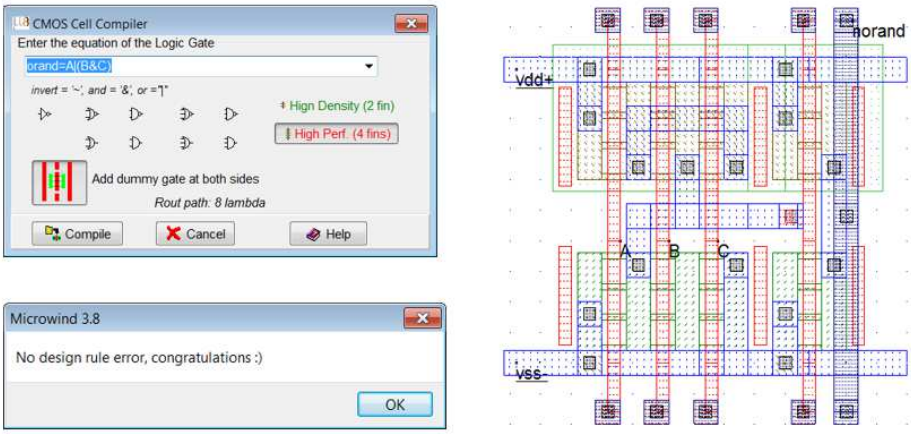


Figure 20: Compilation of a combination of AND and OR cells, with verification of the design rules

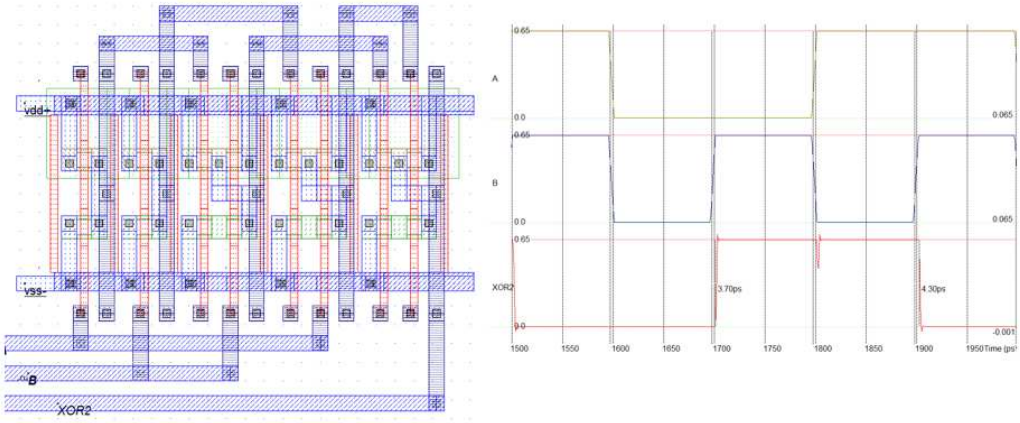


Figure 21: Design and simulation of a 14-transistor XOR gate, with switching speed 4.5 ps, 30% faster than in 14-nm

5. Interconnects

Metal Layers

The number of metal layers in nano-CMOS technology usually ranges from 8 to 15, with a trade-off between integration and cost. In Microwind, only 8 metal layers are considered, according to table 7.

-

Parameter	Pitch (nm)	Pitch (λ)	Rules	Thickness (nm)	Thickness parameter	Purpose
M1	24	6	R501, R502	30	Thme	Short routing
M2	24	6	R701, R702	30	Thm2	Short routing
M3	32	8	R901, R902	60	Thm3	Medium routing
M4	32	8	RB01, RB02	60	Thm4	Medium routing
M5	64	16	RD01, RD02	100	Thm5	Long routing
M6	64	16	RF01, RF02	100	Thm6	Long routing
M7	184	46	RH01, RH02	300	Thm7	Supply, very long routing
M8	300	75	RJ01, RJ02	500	Thm8	Supply, Coil inductance

Table 7: Key features of interconnects in the 7-nm technology implemented in Microwind

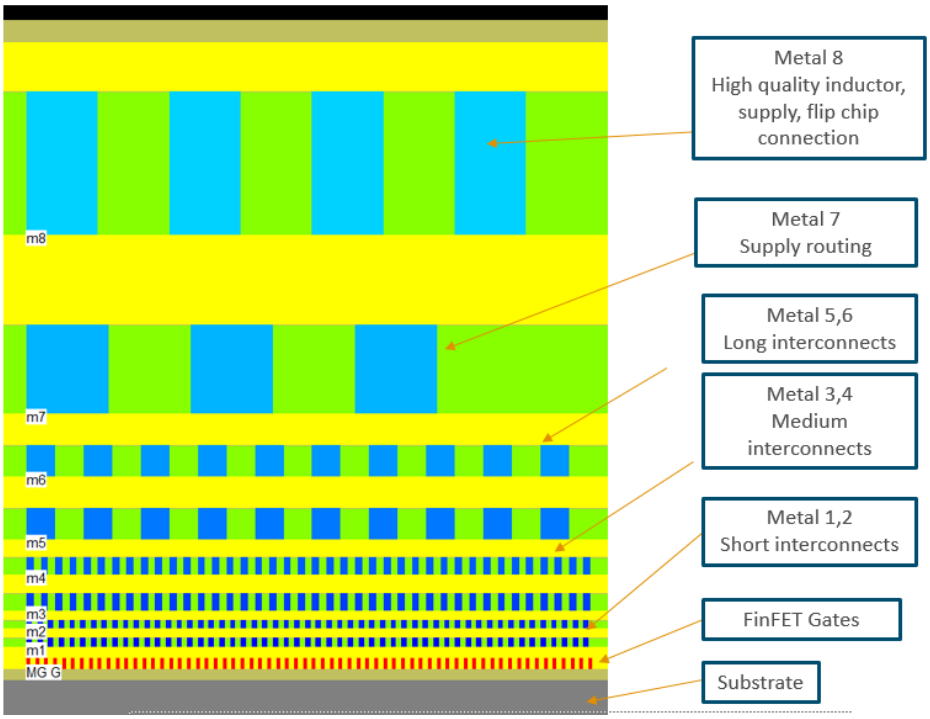


Figure 22: The 8 metal layers proposed in Microwind's implementation of the 7-nm technology

Layers *metal5* and *metal6* are a little thicker and wider, while layers *metal7* and *metal8* are significantly thicker and wider, to drive high currents for power supplies (Fig. 22).

Double & quadruple Patterning

The quadruple patterning is required for metal layers with a pitch smaller than 40-nm, which is the case of M1 & M2 (Fig. 23). One quarter of the patterns go on the first patterning, the second pattern

to the 2nd process iteration, etc. The double patterning is required for metal layers as the pitch between tracks is smaller than 80 nm that is M3 to M6. Half the patterns go on the first patterning and half go on the second patterning. In order to ensure an easy selection of metal tracks for the first and second patterning, regular structures with straightforward orientation such as M1 east-west, and M2 south-north are requested. The other solution is to relax the pitch constraints for an improved manufacturability, at the cost of an extended silicon area. M3-M8 with pitch of 80-nm and higher are still fabricated using simple patterning.

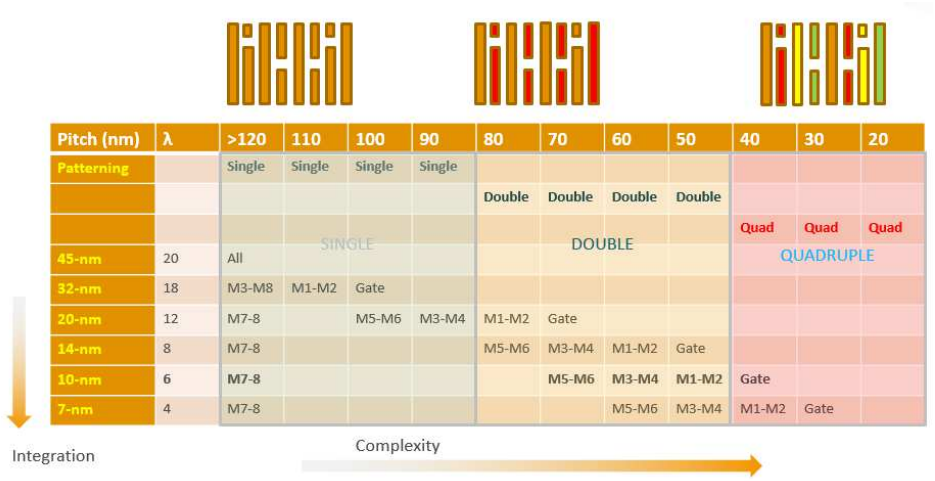


Figure 23: Single, double and quadruple patterning as a function of interconnect pitch [Brain2017]

6. Ring Inverter Simulation

Introducing FO3 AND FO4

The acronyms FO3 and FO4 [Wikipedia] are often found in publications presenting the technology details, as a metric of switching performances. The figure 24 [Collaert2016] describes the performances of a ring oscillator (RO) based on inverters with design D1 (INVD1) with "FO3", meaning a fan-out of 3.

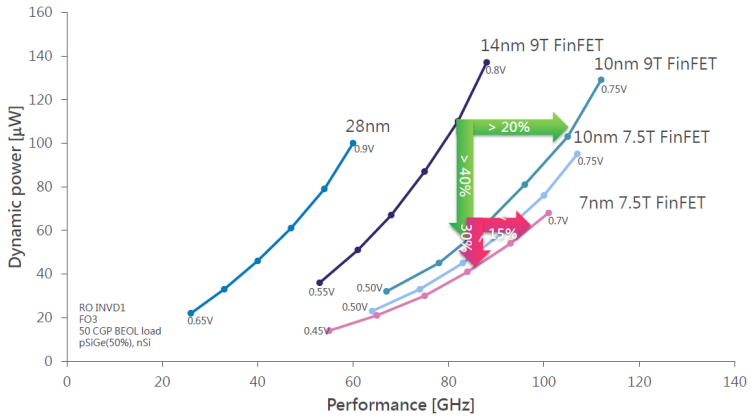


Figure 24: Ring oscillator performance comparison proposed by [Collaert2016] on technologies ranging from 28-nm to 7-nm

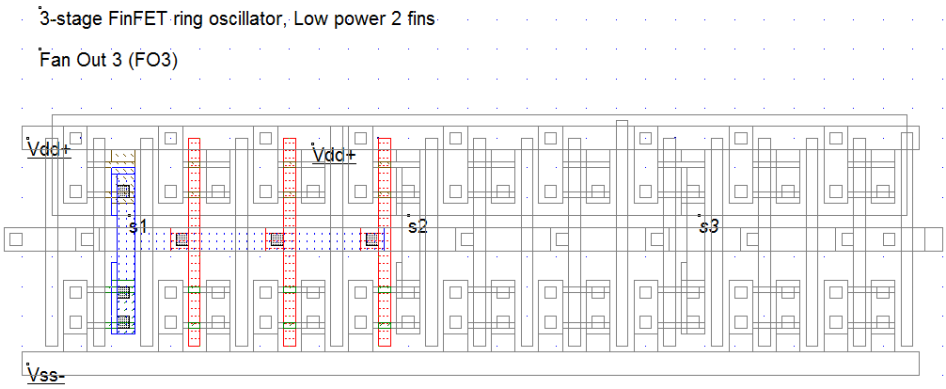


Figure 25: Ring oscillator with fan-out of 3, 3 stages, 2 fins. The node extraction shows 3 gates connected to each inverter output

The Fan-Out may be expressed by:

$$FanOut = \frac{C_{Load}}{C_{in}}$$

where

C_{load} = total gate capacitance driven by the logic gate under consideration

C_{in} = the gate capacitance of the logic gate under consideration

Most often, inverters are used in the delay chain. However, NAND4 designs may also be found in the literature. In FO3 configuration (Fig. 25), each inverter of the ring oscillator is connect to the next-stage inverter (FO1) plus 2 inverter gates that have no action on the ring oscillator, but charge the inverter with 2 supplementary gate capacitances. FO4 consists in connecting the inverter output to 4 inverter inputs.

Performances

An improvement of switching performances close to a factor of 2 is observed between 14-nm and 7-nm designs, although VDD is reduced from 0.85 V to 0.65 V. The performance estimation is based on the simulation of a 3-inverter ring oscillator (RO) with FO3. The tool **Analysis -> Parametric Analysis** of Microwind is used to monitor the oscillating frequency for varying supply voltage VDD (Fig. 26). We choose s3 as monitoring signal, and select VDD as varying parameter, from 0.3 V to nominal voltage. We observe an oscillation starting 0.55V in 14-nm (VDD=0.85 V). For 7-nm, the oscillation starts at 0.50 V (VDD=0.65V).

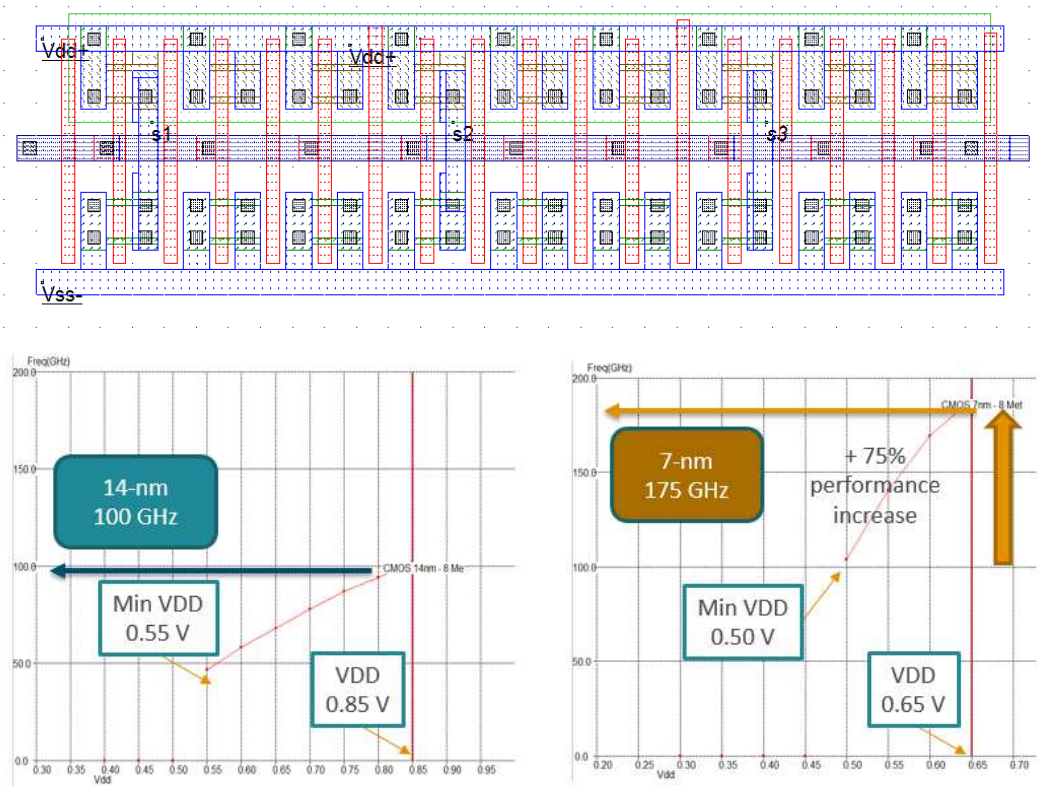


Figure 26: A speed improvement close to a factor of 2 is observed between 14-nm 3-stage ring oscillator and 7-nm (RO3, FO3).

Simulation of Process Variations (PVT)

Considerable differences may be observed in terms of performances, depending on the process, voltage and temperature conditions. The usual temperature range is [-50°C..+125°C], the voltage variation VDD+/- 10%, and the process may also vary +/-15% for some key parameters such as the threshold voltage and mobility. Microwind gives access to "Process-Voltage-Temperature" (PVT) simulation through the command **Simulate → Simulation Parameters → Process Variations**. Direct access from the simulation waveform window is also possible using the button **"Process Variations".** The most usual simulation consists of simulating extreme situations (Min and Max), as compared to typical conditions (Table 8).

- In *Min* situation, VT is high and the mobility U0 is low. The supply is minimum and the temperature is maximum. The ring oscillating is around 100 GHz.
- In *Max* situation, VT is low, mobility U0 is high and the channel is short (LINT<0). The supply is maximum and the temperature is minimum. The ring oscillation is around 250 GHz.

Parameter class	Parameter	Symbol (BSIM4)	Unit	Min (7-nm)	Typ (7-nm)	Max (7-nm)
Process	Threshold Voltage	VT	V	0.46	0.39	0.34
	Mobility	U0	m2/V.s	0.023	0.027	0.031
Voltage	Supply	VDD	V	0.55	0.65	0.75
Temperature	Temperature	TEMP	°C	125	25	-50
Oscillating frequency						

Table 8: Variation of process parameters and effects on the oscillating frequency

7. 6-transistor static RAM

One of the most representative designs for comparing technology nodes is the static RAM cell designed using 6 transistors (6T-SRAM). High performance SRAM use 2 fins for internal inverters while high density SRAM use 1 fin.

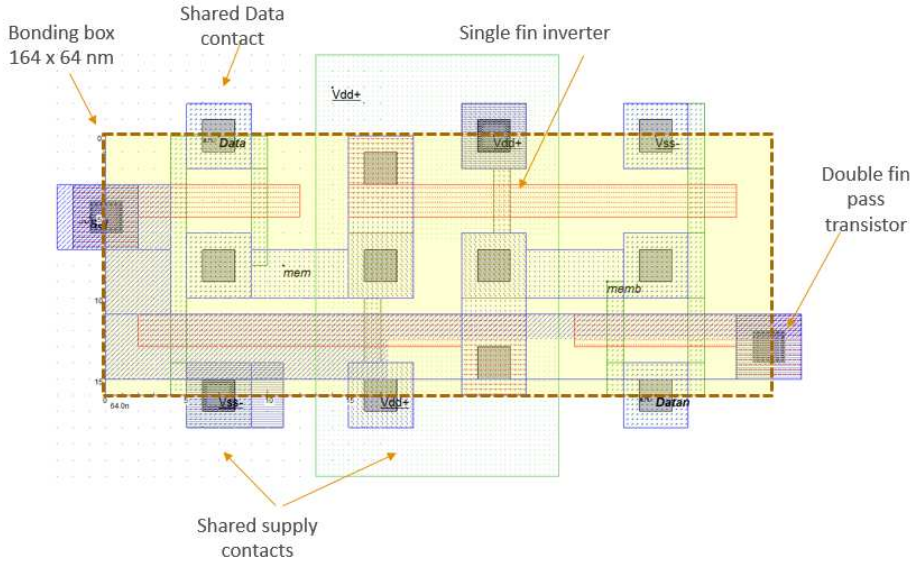


Figure 27: 6T-SRAM implementation in FinFET (SRAM-6T-7nm.MSK)

In our implementation in Microwind (see Fig. 27), the layout size is 164 x 64 nm, with a surface area of 0.010 µm^2. The layout obeys the basic design rules. Most contacts are shared with neighboring cells: the VSS, VDD contacts, the Select and Data lines. It is usual to find more aggressive layout design rules in RAM cell designs, in order to further decrease the cell area.

8. Compare technologies

A quick access to technology is proposed in **Simulation Parameters** (Fig. 28). MosFET technologies range from 0.18µm to 20nm, FinFET technologies range from 14nm to 7nm. MosFET and FinFET designs are not compatible.

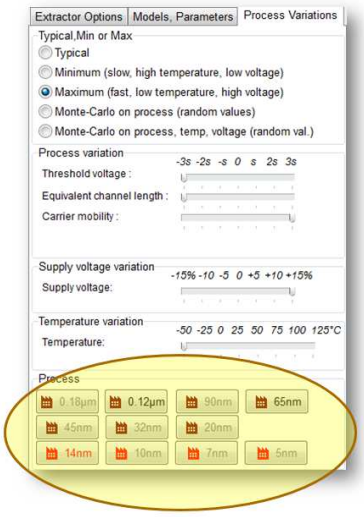


Figure 28: Quick access to MosFET and FinFET technologies

In Microwind 3.8, the command **Edit > Convert into FinFET** creates fins from N-diffusion. Only works for vertical gates. The command generates fins according to the fin pitch as described in the design rule file (r308). An example of fin generation from a MosFET layout is reported in Fig. 29.

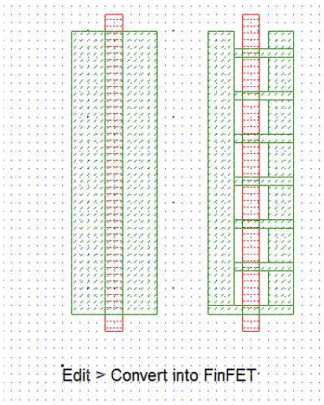


Figure 29: Convert MosFET design into FinFET. Only vertical gates are considered.

9. Conclusions

This application note has illustrated the trends in nano-CMOS technology and introduced the 7-nm technology generation, based on technology information available from manufacturers. The key features of the 7-nm CMOS technology have been illustrated, including the FinFET, design for manufacturing and double patterning. A 3-stage ring, FinFETs wih 1-µm equivalent width as well as interconnects with 1-µm length have been used for comparison purpose.

Acknowledgements

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