LITHOSCALE®

Maskless Exposure Lithography System

Introduction

LITHOSCALE® is a revolutionary, highly versatile maskless exposure lithography product platform geared for a variety of microfabrication applications accommodating wafers up to 300 mm.

The LITHOSCALE system featuring EV Group's MLE™ maskless exposure technology tackles legacy bottlenecks by combining powerful digital processing that enables real-time data transfer and immediate exposure, high structuring resolution and throughput scalability. Its mask-free approach eliminates mask-related consumables, while the exposure system with its tunable solid-state laser source is designed for high redundancy and long life-time stability with unique auto-calibration capabilities that eliminate maintenance. Powerful real-time digital processing enables immediate exposure from the design-file to the substrate – thereby avoiding hours of conversion time for each digital mask layout. LITHOSCALE features high-resolution (< 2 µm L/S), dynamically die-level addressable exposure of the entire substrate surface, which enables agile consumable-free processing and low cost of ownership (CoO). The LITHOSCALE system integrates full-wafer top-and-backside alignment utilizing dedicated objectives with visible to near-IR capability and proprietary chuck designs accommodating wafer sizes up to 300 mm. The system features dynamic alignment modes with an automatic focus, in order to adapt to the substrate material and surface variations. The ability to finely control focus level position keeps sidewalls steep as well as desired 3D contour of the resist, while preventing edge topping and footing. Large working distance and automatic adaptive focus ensures patterning uniformity across the exposure surface. It also offers individualized die processing, while fast full-field positioning and dynamic alignment enable high scalability for a range of substrate sizes and shapes.

Features

- Resolution capability < 2 µm L/S
- Regularly monitored & auto-calibrated solid-state light source securing its long life-time stability and high redundancy
- Advanced alignment modes supporting top-side and bottom-side VIS & IR alignment capability
- Consumables-free technology
- Advanced software features:
  - Dynamic die level annotation
  - Autofocus function
  - Advanced distortion compensation function
  - Mask-file transfer & recipe execution via host/flexible per each wafer
  - Layout transformation function
  - Alternative format files support: Gerber, ODB++, OASIS
- Design freedom and data confidentiality thanks to digital programmable layouts
- Scalable solution accommodating R&D and HVM needs in one system without adding to footprint

Contact

EV Group Europe & Asia/Pacific GmbH
DI Erich Thallner Strasse 1
4782 St. Florian am Inn
Austria
+43 7712 5311 0

Contact@EVGroup.com

Technical Specification Sheet

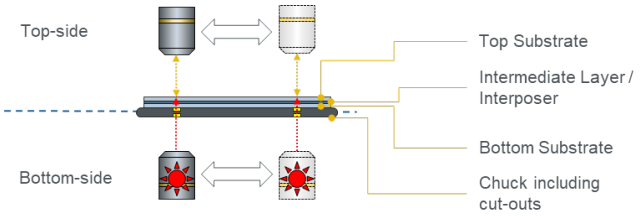
LITHOSCALE®

Maskless Exposure Lithography System

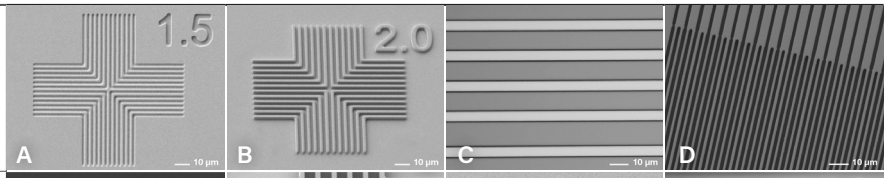
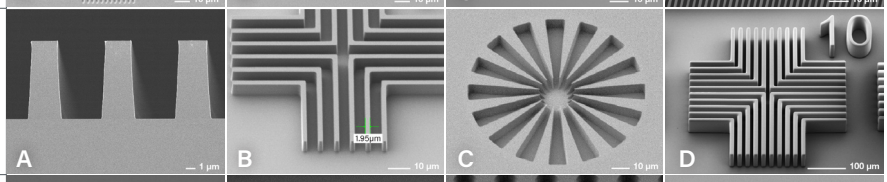
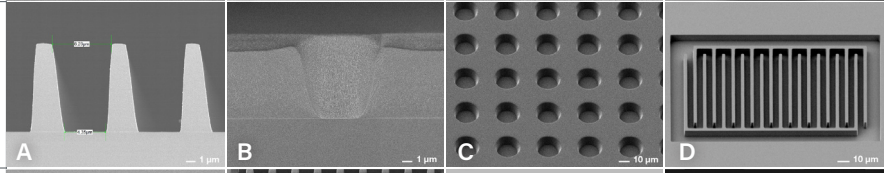
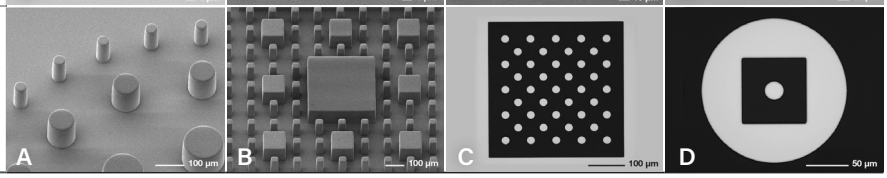
Substrate - Wafer Dimensions	
Substrate / Wafer Size	up to 300 mm
Wafer Thickness	up to 10 mm
Automation Loading	2 FOUP load ports
Robot Module	Dual-end effector Pre-aligner Bar-code reader

Alignment Modes	
Top-side Alignment Accuracy	≤ ± 1 µm
Bottom-side Alignment Accuracy	≤ ± 2 µm
IR Alignment	≤ ± 1.5 µm
Dynamic Alignment Modes [DAM]	Global Alignment Multi-point Alignment

Exposure Module	
Exposure Source	HP UV - Laser Diode (LD)
Exposure Spectrum (single, broad-band or any kind of mixture)	375 nm 405 nm
Depth of Focus range	± 12 µm
Autofocus range	100 µm
Critical Dimension L/S	< 2 µm



Software Features			
	Dynamic Annotation Function		GDS File Transfer & Recipe Execution via Host / Flexible per each Wafer
	Autofocus Function		Layout Transformation Function
	Advanced Distortion Function		Gerber, ODB++ and OASIS File Format Support

Applications & Process Results	
Thin Resists **Fine-line RDL structuring, Lift-off applications** - Pos. AZ MIR 701, LT: 1 µm (A) - Neg. AZ nLOF, LT: 2 µm (B) - Pos. AZ 12XT, LT: 10 µm (C) - Pos. Sumitomo, AR 4.5:1, 7:1 (D)	
Thick Resists **Bumping, core-line RDL structuring, high AR** - Pos. TOK P-W1000T, LT 8 µm, AR: 4:1 sidewall angle: 87° (A, B, C) - Neg. JSR THB 151N, LT 50 µm, AR 5:1 (D)	
Dielectrics **Buffer layer for stress & thermal optimisation** - Pos. JSR WPR5100, LT 7 µm, AR: 2:1 sidewall angle: 82° (A, C, D) - Neg. FUJIFILM LTC Series, LT 7.5 µm, AR: 2:1 (B)	
ORDL, Photonics, MEMS Applications **Photonics packaging, MEMS, coloured resists** - NEG. SU-8 GM1075, LT 100 - 600 µm (A, B) - NEG. Black resist (FFEM), LT 1 - 6 µm (C, D)	

Get in touch:

Contact@EVGroup.com