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FULL PAPER

# Photolithographic Route to the Fabrication of Micro/Nanowires of III–V Semiconductors**

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Nano/microwires of semiconducting materials (e.g., GaAs and InP) with triangular cross-sections can be fabricated by "top–down" approaches that combine lithography of high-quality bulk wafers (using either traditional photolithography or phase-shift optical lithography) with anisotropic chemical etching. This method gives good control over the lateral dimensions, lengths, and morphologies of free-standing wires. The behaviors of many different resist layers and etching chemistries are presented. It is shown how wire arrays with highly ordered alignments can be transfer printed onto plastic substrates. This "top–down" approach provides a simple, effective, and versatile way of generating high-quality single-crystalline wires of various compound semiconductors. The resultant wires and wire arrays have potential applications in electronics, optics, optoelectronics, and sensing.

## 1. Introduction

One-dimensional (1D) structures (such as wires, rods, ribbons, and tubes) of inorganic semiconducting materials on the nanometer and micrometer scale have intrigued more and more scientists and engineers in the last several decades due to their novel properties and interesting potential applications when compared with their bulk counterparts.[1,2] For instance, semiconductor nanowires/nanorods with diameters less than 15 nm exhibit strong quantum-confinement effects and possess bandgaps in the spectral range of solar emission.[3] These unique optical properties make them good candidates to serve as inorganic dopants for polymer-based solar cells with high power-conversion efficiency.[4] With regard to electronic applications, the ribbons and wires of single-crystalline inorganic semiconductors can be assembled on any insulating substrate, including low-cost plastics and even paper, to generate a thin film of active components for building devices with performance higher than devices made of organic semiconducting materials.[5]

Compound III–V semiconductors are of particular importance for modern electronics and optics (e.g., high-speed digital circuits and high-performance optoelectronic devices), because of their high electron mobility, high saturated drift velocity, wide direct bandgap, and wide range of working temperatures.[6,7] A large number of approaches have been developed to synthesize nanowires or microfibers of these materials (e.g., GaAs and InP) in both gaseous and liquid media. For the vapor-based methods, the vapor–liquid–solid (VLS) process originally developed by Wagner and Ellis seems to be the most successful for generating single-crystalline 1D structures.[8] A typical VLS process starts with the dissolution of vapors of target materials, which are generated by laser ablation[9] and/or thermal decomposition of corresponding compounds,[10] into nanosized liquid droplets of a metal catalyst (e.g., Au, Ag, or Cu), followed by nucleation and growth of single-crystalline rods and then wires. The liquid droplets are generated from the corresponding metal nanoparticles at high temperatures, and their size determines the diameter of wires. The vapor determines the composition of the wires, but the doping uniformity and dopant concentration are difficult to control. An analog of the VLS process performed in the liquid phase, the so-called solution–liquid–solid (SLS) process, has been pioneered by Buhro and co-workers to synthesize nanowires using nanoparticles made of metals (e.g., In and Ga) with low melting points as catalysts.[11] Nanowires of GaAs and InP with small diameters (e.g., 3–17 nm) and narrow-diameter distributions were synthesized by refluxing 1,3-diisopropylbenzene solutions of the corresponding precursors (i.e., $(t\text{-Bu})_3Ga$ and $As(SiMe_3)_3$ for GaAs, and $[Me_2InP(SiMe_3)_2]_2$ for InP) in the presence of In nanoparticles. By employing a liquid with a high boiling temperature, such as supercritical hexane, metal nanoparticles (i.e., Au) with high melting points could catalyze the growth of nanowires of GaAs.[12] The as-synthesized wires always have

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[**] This work was supported by the DARPA-funded AFRL-managed Macroelectronics Program (FA8650-04-C-7101). It was also partially supported by the U.S. Department of Energy under grant DEFG02-91-ER45439 and by the National Science Foundation under grant NSF-DMII 03-28162. The fabrication and measurements were carried out using the facilities located in the Microfabrication Laboratory and Center for Microanalysis of Materials of the Frederick Seitz Materials Research Laboratory, which are supported by Department of Energy. Y. S. thanks Prof. Younan Xia in the Department of Chemistry at the University of Washington for his useful suggestions on the anisotropic etching.

  DOI: 10.1002/adfm.200400411 

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broad distributions in wire diameter and length, and their lengths rarely exceed 100 μm. Although the wires are single crystalline and doped in most cases, their surface crystallinity, compositional purity, doping uniformity, and dopant concentration remain unclear compared with bulk single-crystal wafers used in the semiconductor industry.

Developing "top–down" methods (i.e., strategies for preparing small objects on the nanometer or micrometer scale by carving, slicing, or etching the materials on the macroscale) for generating free-standing nano- and microwires of semiconductors from bulk high-quality wafers can produce high-quality wires with well-controlled doping levels, dimensions, and crystallinities, which fit the requirements of modern industry and research. To date, nanowires of Si and GaN have been fabricated from multi-layered wafers (i.e., silicon-on-insulator (SOI) wafers for Si, and 6H-SiC wafers covered with an epitaxial GaN film for GaN) by near-field optical lithography and diffraction-mask projection laser ablation, respectively.[13] The use of wafers with epitaxial layers for generating wires increases the cost of fabrication because of the high price associated with these kinds of wafers.

We report, in this article, a versatile "top–down" approach to the fabrication of nano- and microwires of GaAs and InP with well-controlled morphologies that combines various optical-lithographic techniques (e.g., conventional photolithography and phase-shift optical lithography using the soft-phase masks of polydimethylsiloxane) and anisotropic chemical etching with high-quality bulk single-crystal wafers of GaAs or InP. Interestingly, wire arrays with degrees of order similar to that of the mask patterns can be generated by surrounding the patterned mask stripes with unpatterned bulk mask film, which can then be dry-transfer printed onto plastic substrates with good retention of order and crystallographic orientation. This "top–down" fabrication process associated with the dry-transfer printing process might be important for future large-area, high-performance "macroelectronic" systems and other devices that require integration of vastly different material types.

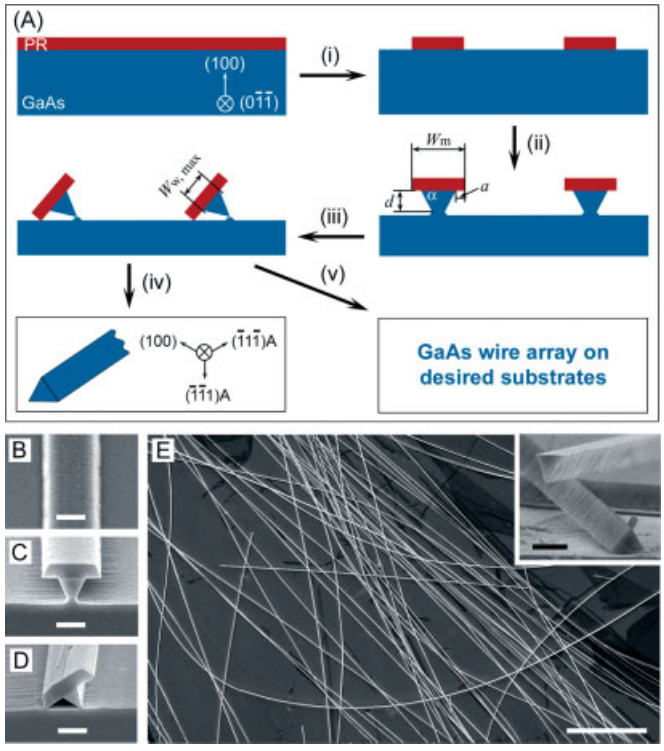


**Figure 1.** A) Schematic illustration of the process for generating GaAs wires from a high-quality bulk single-crystal GaAs wafer. The major steps include: i) defining of patterned PR stripes on a GaAs wafer; ii) anisotropic chemical etching of GaAs wafer using PR stripes as an etch mask; iii) continuous etching of GaAs wafer, with the formation of released GaAs wires; iv) removing PR using acetone and/or $O_2$ plasma; and v) transferring GaAs-wire arrays from the mother substrate to other desired substrates. B–E) Scanning electron microscopy (SEM) images of the samples formed at different stages of the fabrication process: B) PR stripes on GaAs wafer before etching; C) cross-section of a reverse-mesa capped with a PR stripe; D) cross-section of a released GaAs wire resting on the mother substrate against the bottom edge of the GaAs wire and one edge of the PR stripe; and E) a random assembly of the GaAs wires after removal of PR stripes. The inset in (E) is an SEM image taken from the same sample as (E), clearly showing the triangular cross-section. The scale bars in (B–D) and in the inset of (E) represent 1 μm, and the scale bar in (E) represents 50 μm. The etchant consisted of 4 mL of $H_3PO_4$ (85 wt.-%), 52 mL of $H_2O_2$ (30 wt.-%), and 48 mL of $H_2O$, and was cooled in an ice-water bath during the etching process.

## 2. Results and Discussion

### 2.1. Fabrication of GaAs Wires and Etching Chemistry

The fabrication process of GaAs wires includes two major steps: defining photoresist (PR) patterns on a (100) GaAs wafer using photolithography, and chemically etching the GaAs wafer through the PR-patterned mask. Figure 1A depicts the detailed procedure for generating GaAs micro/nanowires from a high-quality bulk GaAs wafer. Spin-casting the PR on the GaAs wafer forms a uniform thin film. Parallel PR lines are defined by standard photolithographic methods: aligning the patterned lines of the photomask along the (0$\bar{1}\bar{1}$) crystalline direction of the GaAs wafer; contacting the photomask with the PR film; exposing the PR film through the photomask; and developing the exposed regions of the PR (step i). The patterned PR lines can directly serve as an etching mask in the anisotropic chemical-etching step when the etchant is acidic.[14] The etchants for GaAs are generally prepared by mixing acids (e.g., $H_3PO_4$, $H_2SO_4$, HCl, or HF) and oxidants (e.g., $H_2O_2$) in water. Specifically, we chose the aqueous solution of $H_3PO_4$ and $H_2O_2$ in a ratio of $H_3PO_4$ (85 wt.-%)/$H_2O_2$ (30 wt.-%)/$H_2O$ = 1:13:12 by volume, which was cooled in an ice-water bath and used to etch the GaAs wafer by the reaction

$$GaAs + H_3PO_4 + 4H_2O_2 \rightarrow GaPO_4 + H_3AsO_4 + 4H_2O \quad (1)$$

This etching process includes the oxidation of GaAs with $H_2O_2$ and subsequent dissolution of the oxidized products by $H_3PO_4$. In this fashion, the chemical etching generates GaAs structures with high anisotropy, i.e., sharply defined reverse-mesa-shaped profiles under the PR-mask stripes (step ii). For

  

sufficient etching times, the two side walls of each reverse-mesa intersect, resulting in the release of a wire with triangular cross-section from the mother wafer (step iii). The maximum width of released wires, $W_{w,max}$, is determined by the width of the PR-mask stripes, $W_m$, the angle of each side wall relative to the top surface, $\alpha$, and the ratio between the etching rates parallel and perpendicular to the wafer surface, ($a/t$) ($d/t$), where $a$ and $d$ represent the undercutting distance and the depth of the reverse-mesa, respectively, and $t$ denotes the etching time. According to the geometry, the value of $W_{w,max}$ can be calculated from

$$W_{w,max} = Wm \Big/ \left[1 + \frac{a/t}{d/t} \times \tan(\alpha)\right] = Wm \Big/ \left[1 + \frac{a}{d} \times \tan(\alpha)\right] \quad (2)$$

Rinsing the wires with acetone and/or exposing them to $O_2$ plasma completely removes the PR, leaving clean GaAs wires (step iv). The ends of each GaAs wire remain connected to the mother wafer when the patterned PR lines are surrounded by a bulk PR film. This connection confines the wires and preserves the spatial orientation and layout defined by the pattern of the PR. The wire array can be transferred to any desired substrate (e.g., plastics, paper) through a dry-transfer technique described in Section 2.5 (step v).

Figures 1B–E show scanning electron microscopy (SEM) images of samples obtained at different stages of the fabrication process illustrated in Figure 1A. Figure 1B presents an SEM image of a section of a 2 μm wide PR line on a GaAs substrate, indicating its straightness and uniform width along its longitudinal axis. (Unless specified otherwise, Shipley 1805 was used as the PR material in our reported results.) The SEM image shown in Figure 1C displays the mushroom-like morphology of the cross-section of a reverse-mesa capped with the PR stripe, indicating the occurrence of lateral undercutting along with the vertical etching. Under this specific etching condition, the values of $a/d$ and $\alpha$ are around 0.68 and 60.7°, respectively. Note that this undercutting allows us to prepare GaAs wires with widths on the nanometer scale by prolonged etching, even when the PR-mask stripes have micrometer-scale widths.[15] Etching for sufficient time releases the GaAs wires, each of which sits on the substrate against its bottom edge and one edge of the PR stripe (a typical SEM image of such a wire is shown in Fig. 1D). PR stripes can be removed by rinsing with acetone. Figure 1E shows an SEM image of such GaAs wires randomly assembled on a GaAs substrate. The wires exhibit uniformity and straightness along their longitudinal axis, while the formation of curved structures indicates that the wires are flexible. The inset is a higher magnification SEM image recorded from the same sample, clearly showing the triangular cross-section of each wire, the roughness of the side walls, and the flatness of the top surface protected with the PR. These wires have an average width of 840 nm.

The anisotropy of etching originates from the difference of etching rates along the different crystallographic axes. The crystal planes with the lowest energy and highest chemical resistance have the slowest etching rate. Since GaAs is crystallized in the form of a zinc-blende face-centered cubic (fcc) lattice, the {111} planes are the most stable.[16] The Ga-rich {111} surface, also called {111}A, is deficient in electron density compared with the As-rich {111} surface (the {111}B surface). This difference makes the {111}A surface resistant to chemical oxidation and generally difficult to etch. According to the crystallographic geometry of the GaAs wires, the side walls of each wire are indexed to the $(\bar{1}\bar{1}1)$A and $(\bar{1}1\bar{1})$A planes. The left rendering in Figure 2A illustrates the three-dimensional arrangement of Ga and As in an GaAs wire with a triangular cross-section. Both the side walls and the top surface are enclosed by Ga-rich planes. The angle of the side wall relative to

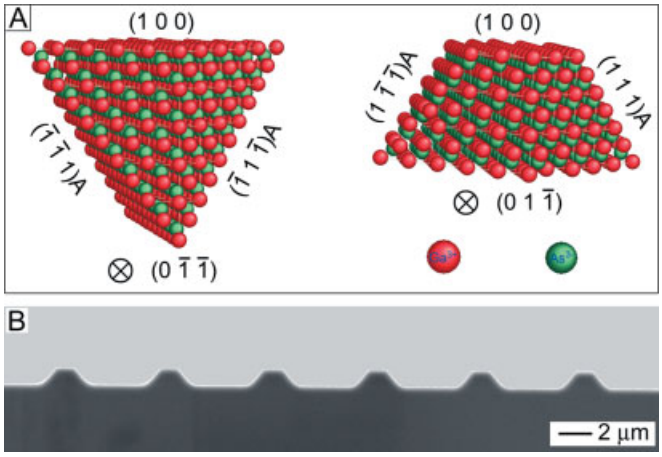


**Figure 2.** A) Illustration of the three-dimensional arrangement of Ga and As in the reverse-mesa (left) and normal-mesa (right) geometries. B) SEM image of the cross-section of mesas formed by etching the GaAs wafer masked with patterned PR stripes along the $(01\bar{1})$ direction. Etching conditions were similar to that of Figure 1.

the top surface is 54.74°, which is very close to the angle observed from the resultant GaAs wires shown in Figure 1 (60.7°). In principle, the anisotropic chemical etching is highly dependent on the crystallographic orientation of mask lines. Etching of GaAs crystals with the PR stripes oriented in the $(01\bar{1})$ plane results in a mesa-shaped profile with side walls bounded by $(1\bar{1}\bar{1})$A and (111)A planes (Fig. 2A, right). Figure 2B shows an SEM image taken from the cross-section of a sample produced by etching with the PR-mask lines oriented in the $(01\bar{1})$ direction, confirming the formation of mesa-like profiles. The angle of the side wall relative to the top surface is 126.7°, which is similar to the theoretical angle of 125.26°. The agreement between the observed etch profiles and the crystallographic models implies that the Shipley 1805 PR can effectively protect the top surface of GaAs during the etching process.

### 2.2. Variation in the Dimensions of GaAs Wires

The values of $\alpha$ and $a/d$ are independent of the width of the mask lines for a given combination of mask material and etchant composition. In this case, the maximum lateral dimension of the GaAs wires ($W_{m,max}$) can be easily changed by control-

  

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ling the width of the PR-mask stripes because of their proportional relationship. Figures 3A,B show SEM images of the GaAs wires prepared using the PR-mask lines (defined by conventional contact photolithography) with widths of ~10 μm and ~3 μm. Both samples exhibit triangular cross-sections, and their corresponding average widths are 3.84 μm and 1.19 μm, respectively. Because contact photolithography can only define PR lines with widths larger than 1 μm, we employed phase-shift optical lithography to generate patterned PR lines with submicrometer widths.[17] In this process, a transparent elastomeric polydimethylsiloxane (PDMS) stamp with narrow lines was prepared by replica molding of the relief structures of a master fabricated via e-beam lithography.[18] The phase-shift of light and conformal contact between PDMS and the PR film enable the PR to be patterned into lines with widths of 50–300 nm, depending on the conditions and the design of the mask. Figure 3C shows an SEM image of the GaAs nanowires with widths of ~65 nm, which were prepared from the GaAs wafer masked with ~200 nm wide PR lines defined via phase-shift lithography. Combining these two kinds of lithographic techniques enables the preparation of GaAs wires with widths ranging from tens of nanometers to several hundred micrometers. Figure 3D plots the dependence of the maximum wire width ($W_{w,max}$) on the width of mask lines ($W_m$), showing the linear relationship. The slope is 0.40, which is close to the predicted value (0.45) from Equation 2 by substituting 0.68 and 60.7° for $a/d$ and $\alpha$, respectively. The high anisotropy of etching remains, even for free-standing wires capped with PR stripes. As a result, wires with nanometer-scale widths can also be obtained by increasing the etching time with PR lines that have micrometer widths.

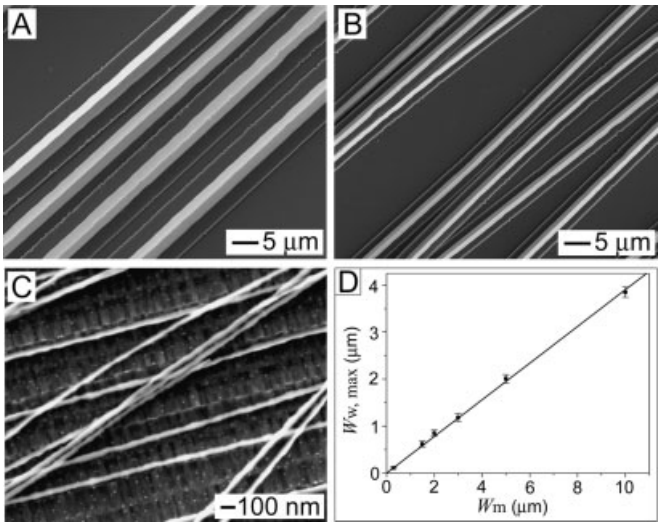


**Figure 3.** A–C) SEM images of GaAs wires with different widths: A) 3.84 μm, B) 1.19 μm, and C) 65 nm. These wires were fabricated from GaAs wafers using PR-mask stripes with widths of 10 μm, 3 μm, and 200 nm, respectively. The wires shown in (A,B) were transferred to the PDMS stamps before images were taken. The wires shown in (C) were on the rough mother substrate after removing the PR stripes. D) Plot of the dependence of the maximum width of GaAs wires ($W_{w,max}$) on the width of PR-mask stripes ($W_m$). Etching conditions were similar to that of Figure 1.

The lengths of the GaAs wires can also be easily tuned by controlling the length of the PR-mask stripes. Figure 4 shows SEM images of GaAs rods with different lengths; they are somewhat shorter than the lengths of their corresponding PR stripes. The shortening is attributed to the undercutting along the longitudinal axis of each PR stripe, i.e., in the $(0\bar{1}\bar{1})$ direction. Since the $(0\bar{1}\bar{1})$ planes have higher surface energy than {100} planes for fcc crystals,[16] the undercut etching exposes the {100} planes, resulting in the formation of sharp ends. The SEM image (Fig. 4A) of the unreleased GaAs rods shows the generation of sharp ends on each rod and the preservation of a flat top surface. The illustration shown in Figure 4A (inset) clearly depicts the geometry and crystallographic surfaces of an individual rod. Figures 4B–D show SEM images of GaAs rods with average lengths of 6.4 μm, 15.5 μm, and 40 μm, which were prepared by using the PR-mask stripes with lengths of 10 μm, 20 μm, and 50 μm, respectively. In principle, we can prepare wires with lengths up to tens of centimeters, i.e., the diameter of the original wafer. The high uniformity in the lengths of the as-prepared GaAs rods/wires shown in Figure 4 is very difficult—or impossible—to generate through chemically synthetic, "bottom–up" approaches.

In addition to easy control over the dimensions and uniformity of the GaAs wires, the "top–down" approach described in this article can also prepare complex structures other than free-standing straight lines using specifically designed masks. For example, each GaAs wire with lateral dimensions on the sub-micrometer scale tethers one end to the mother substrate when one end of each PR-mask stripe is connected to the bulk PR film and the other end of the stripe is free. Figure 5 shows a typical SEM image of such GaAs wires on the mother sub-

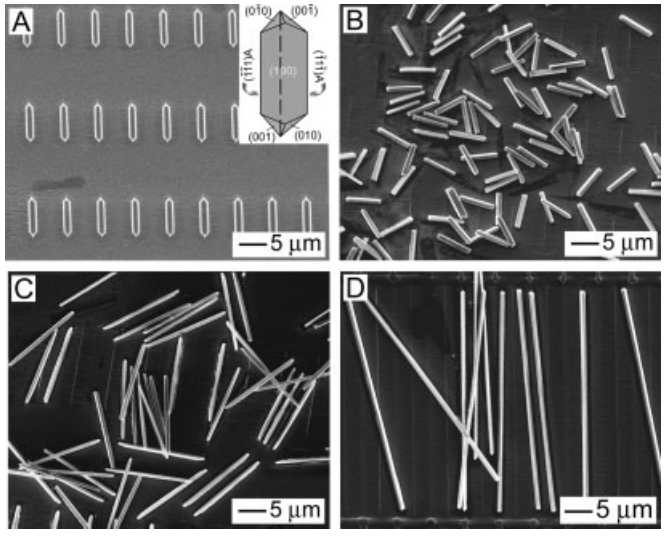


**Figure 4.** A) SEM image of an array of unreleased reverse-mesas. The inset presents an illustration of an individual GaAs rod with all the crystallographic planes specified. SEM images of GaAs wires with different lengths: B) 6.4 μm, C) 15.5 μm, and D) 40 μm. The widths of PR stripes for all samples were 2 μm. Etching conditions were similar to that of Figure 1.

  

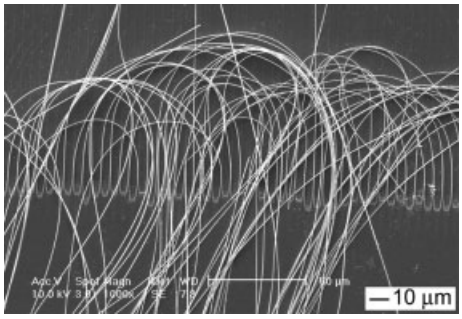


**Figure 5.** SEM image of the GaAs wires with one end of each wire tethered to the mother substrate and the other untethered. Etching conditions were similar to that of Figure 1.

strate. The anchored ends of the wires preserve the spatial order of the PR pattern, while the opposite ends move freely, allowing the wires to bend into curved structures.

### 2.3. Influence of Etchant and Mask Materials on the Morphology of GaAs Wires

Wet-chemical systems that anisotropically etch GaAs can be classified into three categories: aqueous solutions of acids and hydrogen peroxide ($H_2O_2$),[19] aqueous solutions of bases and $H_2O_2$,[20] and solutions of bromine ($Br_2$) in methanol.[21] Acidic solutions of $H_2O_2$ are commonly used in anisotropic etching of GaAs due to their low toxicity (relative to $Br_2$ solutions) and their compatibility with PR materials. We selected $H_3PO_4$–$H_2O_2$–$H_2O$ as the etchant in this work because of the high purity (i.e., availability as electronic-grade) and non-volatility of $H_3PO_4$. Previous studies indicated that the molar ratio of $H_2O_2$ to $H_3PO_4$ significantly affected the anisotropy of etching of GaAs single crystals. In our experiments, the molar ratio of $H_2O_2$ to $H_3PO_4$ was fixed at 7.8:1, a value where high anisotropy was previously obtained,[22] and the influence of concentration of $H_2O_2$ on the etching rates and profile of cross-sections was investigated. Figure 6 shows the dependencies of the undercutting-etching rate and the vertical-etching rate on the concentration of $H_2O_2$, indicating that the more concentrated solution etches the crystals faster along both directions. Analysis of SEM images taken from cross-sections of reverse-mesas reveals that the angles between the top surfaces and side walls of reverse-mesas are independent of the concentration of $H_2O_2$, and that the values are around 60.5°. According to Equation 2, the maximum width of released wires prepared using PR-mask stripes with the same width is determined mainly by the ratio of etching rates along the different directions. The inset in Figure 6 plots the ratio of the undercut-etching rate to the vertical-etching rate versus the concentration of $H_2O_2$. The results show that the etchant with a $H_2O_2$ concentration of 4.2 M (i.e., a solution consisting of $H_3PO_4$ (85 wt.-%)/$H_2O_2$ (30 wt.-%)/$H_2O$ = 1:13:12 by volume) generates the lowest ratio of etching rates ($r_u/r_v$). In this case, the etching process generates the highest anisotropy and largest wire width. Having GaAs wires with a relatively large width is

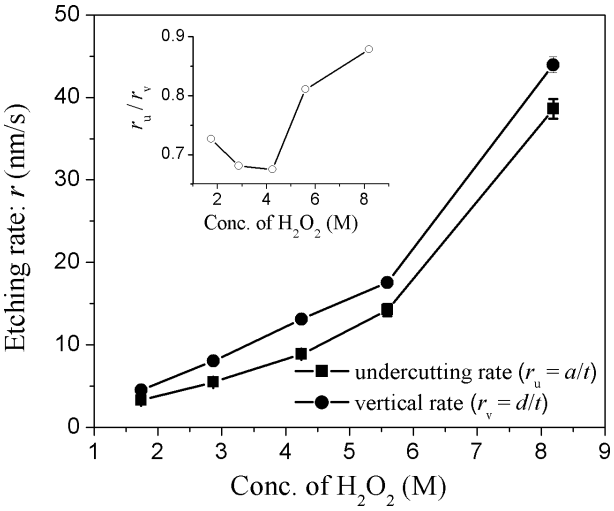


**Figure 6.** Dependence of the etching rates on the concentration of $H_2O_2$ in the etchant solution. The molar ratio of $H_2O_2$ to $H_3PO_4$ was fixed at 7.8:1 for all etchants. The GaAs wafers were patterned with 2 µm width PR stripes.

important in some cases, e.g., electronic devices, in order to generate a large cross-sectional area for carrier transport. In the following studies, the etchant solution was fixed, with the recipe consisting of 4 mL of $H_3PO_4$, 52 mL of $H_2O_2$, and 48 mL of deionized water.

In addition to the composition of the etchant, the composition of the etching mask also significantly affects the profile of resultant GaAs wires. Table 1 lists the etching results obtained using different PR materials (spin-cast on GaAs wafers) and e-beam-evaporated thin films of dielectrics (e.g., $SiO_2$) or metals (e.g., Pd, Au, Ti/Au). The GaAs wafer masked with Shipley 1805 PR generated the smallest $r_u/r_v$ and $\alpha$, and the largest $W_{w,max}/W_m$, while all the e-beam-evaporated masks led to increases in both $r_u/r_v$ and $\alpha$, and thus to decreases in $W_{w,max}/W_m$. The difference in the ratios of the etching rates parallel to and perpendicular to the top surface ($r_u/r_v$) might be attributed to the stronger reducing ability of novolac-based PRs (e.g., Shipley 1805) compared with GaAs, which reduces the oxidation rate of GaAs near the interface of GaAs and PR,

**Table 1.** Results of GaAs with different mask materials etched with a solution consisting of $H_3PO_4$ (85 wt.-%)/$H_2O_2$ (30 wt.-%)/$H_2O$ = 1:13:12 by volume.

| Mask material | $r_u = a/t$ [nm s$^{-1}$] | $r_v = d/t$ [nm s$^{-1}$] | $r_u / r_v$ | $\alpha$ [deg] | $W_{w,max}/W_m$ |
|---|---|---|---|---|---|
| Shipley 1805 PR | 8.86 ± 0.38 | 13.13 ± 0.25 | 0.68 | 60.7 ± 1.8 | 0.45 |
| PMMA PR | 9.57 ± 0.35 | 10.60 ± 0.12 | 0.90 | 63.1 ± 0.7 | 0.36 |
| AZ5214 PR | 11.16 ± 0.42 | 10.42 ± 0.28 | 1.07 | 69.8 ± 0.9 | 0.26 |
| 50 nm $SiO_2$ [a] | 12.68 ± 0.62 | 11.79 ± 0.25 | 1.08 | 70.1 ± 1.7 | 0.25 |
| 50 nm Pd [a] | 11.17 ± 0.33 | 10.92 ± 0.20 | 1.02 | 71.7 ± 0.9 | 0.25 |
| 50 nm Au [a] | 10.89 ± 0.20 | 9.79 ± 0.20 | 1.11 | 70.8 ± 0.1 | 0.24 |
| 5 nm Ti/50 nm Au [a] | 10.76 ± 0.29 | 9.31 ± 0.19 | 1.16 | 72.2 ± 0.5 | 0.22 |

[a] The mask stripes were formed by depositing the corresponding materials using e-beam evaporation on the PR-patterned GaAs wafer, followed by a lift-off process in acetone.

  

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**Table 2.** Etching results of GaAs in different acid solutions.

| Volume ratio [a] | Mask | $r_u = a/t$ [nm s$^{-1}$] | $r_v = d/t$ [nm s$^{-1}$] | $r_u / r_v$ | $\alpha$ [deg] | $W_{w,max}/W_m$ |
|---|---|---|---|---|---|---|
| 1:2:8 $H_2SO_4/H_2O_2/H_2O$ | Shipley 1805 PR | 10.93 ± 0.40 | 15.57 ± 0.28 | 0.70 | 65.6 ± 0.5 | 0.39 |
| 1:2:8 $H_2SO_4/H_2O_2/H_2O$ | 50 nm $SiO_2$ | 10.43 ± 0.52 | 10.78 ± 0.76 | 0.96 | 71.9 ± 1.3 | 0.25 |
| 1:4:40 $HCl/H_2O_2/H_2O$ | Shipley 1805 PR | 1.89 ± 0.08 | 1.69 ± 0.04 | 1.12 | 75.3 ± 0.8 | 0.19 |
| 1:4:40 $HCl/H_2O_2/H_2O$ | 50 nm $SiO_2$ | 2.18 ± 0.09 | 1.57 ± 0.04 | 1.39 | 80.6 ± 1.3 | 0.11 |

[a] Solution concentrations: $H_2SO_2$ 98 wt.-%; HCl 37 wt.-%; $H_2O_2$ 30 wt.-%.

thus decreasing the undercut-etching rate. The differences between different PRs is still unclear, due to uncertainties over their exact compositions. As shown in Table 2, GaAs masked with e-beam-evaporated $SiO_2$ stripes always generated larger values of $r_u/r_v$ and $\alpha$ than GaAs masked with PR stripes, whatever the etchant composition. To our knowledge, this study represents the first demonstration that the composition of the etching mask has significant effects on the morphology of GaAs wires. As a result, tuning the etching-mask composition could provide an alternative to changing etchant composition in order to modify the morphology of GaAs wires.

Statistical analysis of tens of etching experiments reveals that the value of $\alpha$ is strongly related to the ratio of $r_u/r_v$; i.e., these two parameters cannot be tuned independently. Figure 7 shows their relationship: the etching processes that generate high $r_u/r_v$ ratios result in structures with high angles ($\alpha$). The formation of relatively large angles (i.e., $\alpha > 65°$) indicates that the etching process generates side walls bounded by high-index planes (e.g., {332}) rather than {111}A.[19] Therefore, we can control the morphology and crystallographic surfaces (e.g., cross-section) of the released GaAs wires by selecting appropriate mask materials and etchants. For example, GaAs wires with equilateral triangular cross-sections can be prepared by etching GaAs wafer masked with PR stripes of Shipley 1805 in $H_3PO_4$–$H_2O_2$–$H_2O$, while etching GaAs wafers masked with e-beam-evaporated $SiO_2$ stripes in HCl–$H_2O_2$–$H_2O$ can generate GaAs wires with very thin, wedge-like morphologies (Fig. 8). Figure 8A presents the SEM image of the cross-section of the wires before they were released. This result indicates that the undercutting-etching rate was larger than the etching rate along the direction perpendicular to the top surface of the GaAs wafer, and that the angle of the side wall relative to the top surface was ~80.6°. The lateral dimensions of the mesa-shaped neck is larger than that of the reverse-mesa (~750 nm versus ~250 nm). After the GaAs wires were released, the surface of the mother substrate was patterned with the parallel necks left behind (the parallel bright lines shown in Fig. 8B). This image also shows some GaAs wires randomly assembled on the surface of the mother substrate. These GaAs wires exhibit much shorter lengths than the $SiO_2$ mask stripes, indicating that the resultant wires broke into small pieces due to their fragility. The SEM image of the cross-section of an individual GaAs wire clearly shows its sharp wedge-like profile, rough side walls, and saw-like bottom edge (Fig. 8B, inset). The formation of saw-like edges (i.e., the bottom edge formed by the intersection of the side walls of the reverse-mesas) can be attributed to roughness (i.e., the existence of ridge/valley stripes) on the side walls of GaAs wires. The sections with ridges on the side walls detach from the mother substrate at greater depths than those with valleys. The difference is apparent for GaAs wires with narrow widths (compare Fig. 8B, inset with Fig. 1E, inset). Mechanical effects caused by vibration of the solution during etching might also contribute to these saw-like edges.

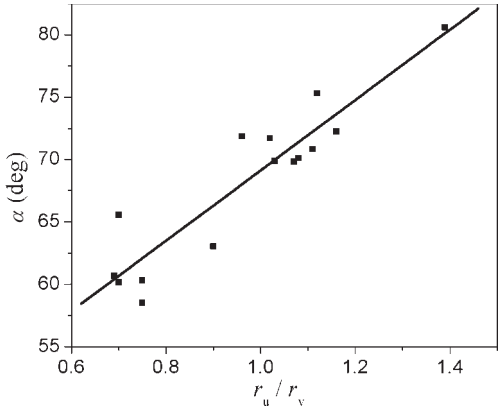


**Figure 7.** Dependence of the angle of the side wall relative to the top surface ($\alpha$) on the ratio of the undercutting rate to the vertical-etching rate ($r_u/r_v$). The etchant was composed of a ratio of $H_3PO_4$ (85 wt.-%)/$H_2O_2$ (30 wt.-%)/$H_2O$ = 1:13:12 by volume.

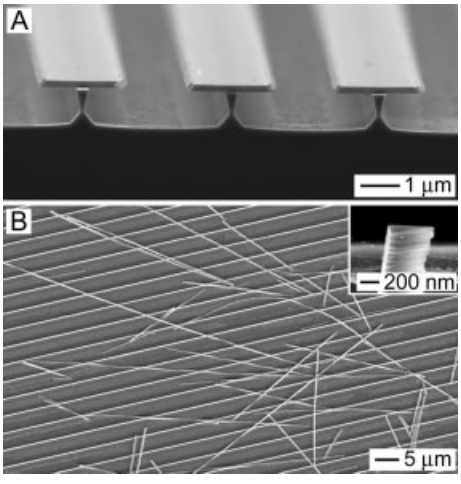


**Figure 8.** SEM images of the GaAs wires A) before and B) after release from the mother substrate for the $SiO_2$-masked GaAs wafer etched in the solution consisting of 1 mL HCl (37 wt.-%), 4 mL $H_2O_2$ (30 wt.-%), and 40 mL $H_2O$.

  

### 2.4. Characterization of Surface Roughness

Anisotropic etching usually generates a small mesa-shaped neck between each reverse-mesa and mother substrate (Fig. 1C). The neck is left as a ridge on the mother substrate after the GaAs wire is released. Figure 9A shows an atomic force microscopy (AFM) image of the surface of the left-behind GaAs wafer, clearly showing the formation of a ridge where the PR stripe was located. Polishing the GaAs wafer using well-established approaches can smoothen its surface.[23] Figure 9B presents an AFM image of the surface of the GaAs wafer shown in Figure 9A after it was polished with 20 nm silica beads and chemical polishing agents. The ridges completely disappear and the surface roughness is significantly decreased. The small spots on the polished surface is attributed to the relatively large size of the silica beads that we used in our demonstration. It is likely that better-controlled polishing procedures, similar to those used in the semiconductor industry, can generate surfaces with quality similar to that of the original wafer. The polished wafer shown in Figure 9B can be reused to generate GaAs wires via the procedure depicted in Figure 1A. Uniform GaAs wires were indeed prepared using the "top-down" fabrication process and a recycled wafer, with a typical SEM image of the resultant wires shown in Figure 9C. Apparently, the combination of "top–down" fabrication and a polishing process enables the production of a large number of wires from a single bulk GaAs wafer, thus significantly reducing the cost per wire.

Close observations of the side walls of GaAs wires and reverse-mesas reveal that their surfaces are rough with ridge/valley stripes parallel to the $(0\bar{1}\bar{1})$ plane, i.e., the surface of the cross-section. The SEM image in Figure 10A was taken from one reverse-mesa before it was released from the mother sub-

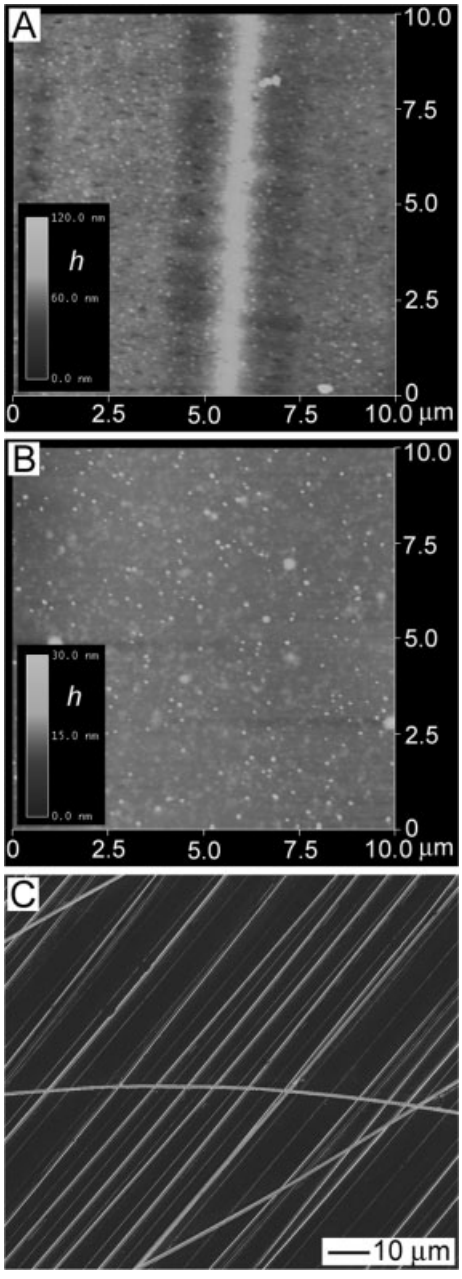


**Figure 9.** AFM images of the remaining GaAs mother wafer A) before and B) after it was polished with 20 nm silica colloids and chemical polishing agents. C) SEM image of GaAs wires fabricated from the polished GaAs wafer (B) using the procedure depicted in Figure 1A. Etching conditions were similar to that of Figure 1.

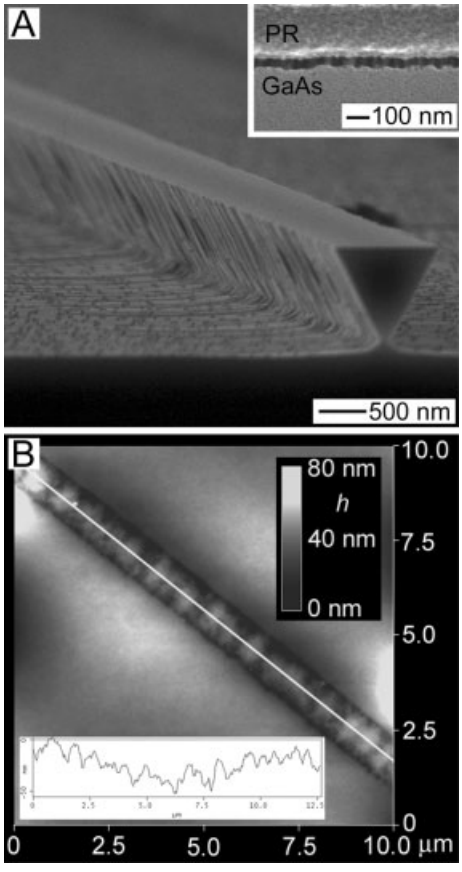


**Figure 10.** A) SEM image of an individual reverse-mesa generated by etching a GaAs wafer masked by a PR stripe. The inset is an SEM image of a GaAs wafer with a PR stripe after etching for 5 s. B) AFM image of the side wall of a single GaAs wire. Etching conditions were similar to that of Figure 1.

  

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strate. The ridge/valley stripes on the side wall continue to extend to the mother substrate. The continuity of ridge/valley reliefs on the side wall of the reverse-mesa and the mother substrate suggests that they originate from the same source. The inset in Figure 10A shows the SEM image of the GaAs masked with PR after it was etched for a very short time (5 s). The image clearly shows that the edge of the PR stripe is rough and that the chemical etching initiates at the boundary of PR edge and GaAs. The ridge/valley stripes on the side walls of GaAs wires therefore likely originate from the roughness of the edge of the PR-mask lines. An AFM analysis (Fig. 10B) of the side wall of an individual GaAs wire confirms the formation of a ridge/valley relief structure, with peak-to-valley distances ranging from several to tens of nanometers (Fig. 10B, inset). Decreasing the roughness of the edges of the PR-mask lines will likely decrease the roughness of the wires.

### 2.5. Transfer Printing of GaAs-Wire Arrays onto Plastic Substrates

The surface roughness of GaAs wires could have adverse effects on certain device applications, but this disadvantage could be eliminated by transferring the GaAs-wire arrays to desired substrates with their top, flat surfaces facing up for device fabrication. When the PR-mask lines are surrounded by bulk PR film, both ends of each GaAs wire are connected to the mother wafer, resulting in the approximate preservation of the spatial orientation defined by lithography. The resultant GaAs-wire array can be transfer printed onto plastic substrates using the procedure illustrated in Figures 11A,B. The first step is to place a transfer element (i.e., a flat piece of PDMS) on the GaAs wafer covered with released GaAs wires. The low modulus of PDMS promotes the formation of a conformal contact between PDMS and the surface of the PR-mask stripes (step i). The surfaces of the PDMS and PR stripes can be bonded together by hydrophobic–hydrophobic interactions[24] because the fresh PDMS surface, covered with –Si–H and –Si–$CH_3$ groups, is highly hydrophobic.[25] This force is strong enough to break the connections between the ends of wires and mother substrate. Peeling the PDMS stamp from the GaAs substrate lifts off all of the wires (step ii). Placing the PDMS stamp with GaAs wires against an adhesive layer, such as polyurethane (PU), spin-coated onto a plastic substrate, such as a sheet of poly(ethylene terephthalate) (PET), forms a conformal contact due to flow of the liquid PU (step iii). Curing the PU with illumination of a UV lamp (with an intensity of 14.5 mW $cm^{-2}$) for 1 h solidifies the PU layer and bonds the GaAs wire and PET substrate together. Peeling away the PDMS stamp leaves the GaAs wires and PR-mask stripes embedded in the matrix of cured PU, with preservation of the order and crystallographic orientation of the wires prior to lift-off from the mother substrate (step iv). Figures 11C,D are SEM images of the GaAs wires (with PR) on the flat PDMS stamp, showing the preservation of the order of wires and the triangular cross-section of each wire. The SEM image shown in Figure 11E shows the GaAs wires embedded in PU/PET, indicating that the surface of the cured PU layer is as smooth as the PDMS surface. In the transfer process, the PR-mask stripes serve as a buffer layer to protect the surfaces of the GaAs wires from being contaminated with other materials, such as PU. By using inorganic dielectric materials, e.g., $SiO_2$, as etching masks, it is possible to completely avoid organic contaminants. The resultant wire arrays can also be transfer printed onto plastic substrates through a scheme similar to that in Figures 11A,B.[15]

This technique has the capability of transferring GaAs-wire arrays onto plastic substrates with large areas. Figure 12A presents an optical-microscopy image of a PU/PET substrate with

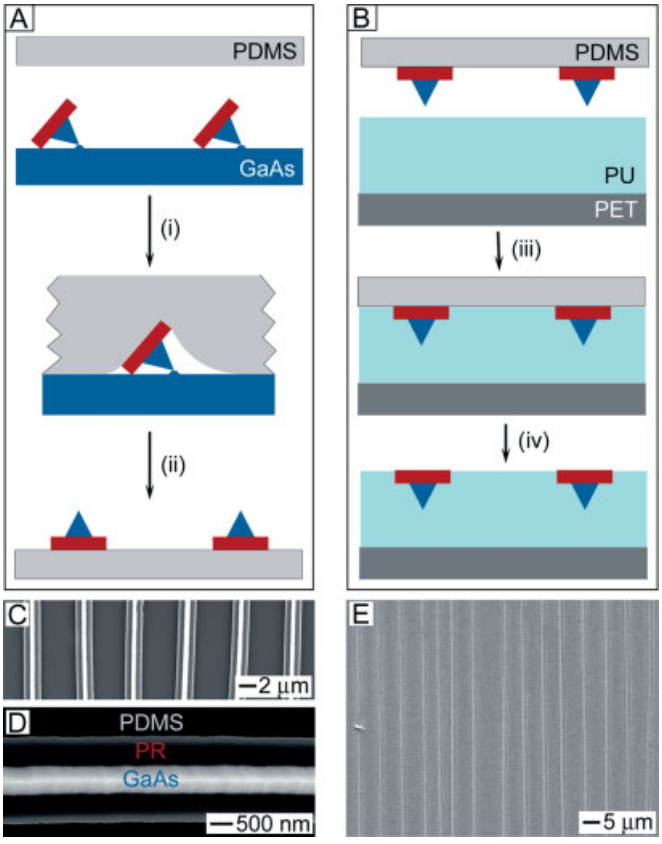


**Figure 11.** Schematic illustration of the process of transfer printing GaAs-wire arrays onto plastic substrates. A) The steps involved in the transfer of GaAs-wire arrays to a PDMS stamp: i) placing a PDMS stamp on a GaAs wafer with wires leads to the formation of a conformal contact and hydrophobic–hydrophobic interaction between PDMS and the surface of PR stripes; ii) peeling the PDMS stamp from the GaAs substrate lifts off the wires. B) The steps involved in the transfer process of GaAs-wire arrays from PDMS stamp to poly(ethylene terephthalate) (PET) substrate coated with a thin layer of polyurethane (PU): iii) placing the PDMS stamp (with wires) on a liquid PU layer spin cast on PET sheet causes the PU to flow and conform to the wires; iv) solidifying PU with UV light bonds the wires to the PET sheet such that peeling off the PDMS stamp leaves the wires embedded in PU. C,D) SEM images of a GaAs-wire array bonded to PDMS stamp via the PR stripes. E) SEM image of a GaAs-wire array on a PU/PET sheet. Etching conditions were similar to that of Figure 1.

  

embedded GaAs wires, indicating that large-area wire arrays can be routinely printed on the PU/PET substrate using the approach depicted in Figure 11. Illuminating the GaAs wires with a laser beam perpendicular to the surface of PU/PET substrate generates a diffraction pattern consisting of only one straight line (with diffraction spots) perpendicular to the orientation of GaAs wires (Fig. 12A, inset), further confirming that the GaAs wires embedded in a PU/PET substrate maintain their uniform alignment defined by lithography. (However, the periodic ordering is somewhat degraded.) The transfer process could be repeated to print multiple layers of GaAs-wire arrays on the same PET substrate by spin-coating a new layer of PU. Figure 12B shows a typical image of a sample with two layers of GaAs-wire arrays, obtained by rotating the second layer by ~90° relative to the first layer. Accordingly, illuminating this sample with a laser beam generates a diffraction pattern with two perpendicularly-crossed lines (Fig. 12B, upper-right inset). The bottom-left inset of Figure 12B presents an SEM image of the cross-section of the sample shown in Figure 12B, clearly showing that the GaAs wires are embedded in the cured PU, and that the two individual layers of GaAs-wire arrays are separated by PU. The thickness of the PU layer, which can be controlled by tuning the spin-coating speed, controls the spacing between the wire arrays. For various applications, the PU can insulate the GaAs arrays located in different levels.

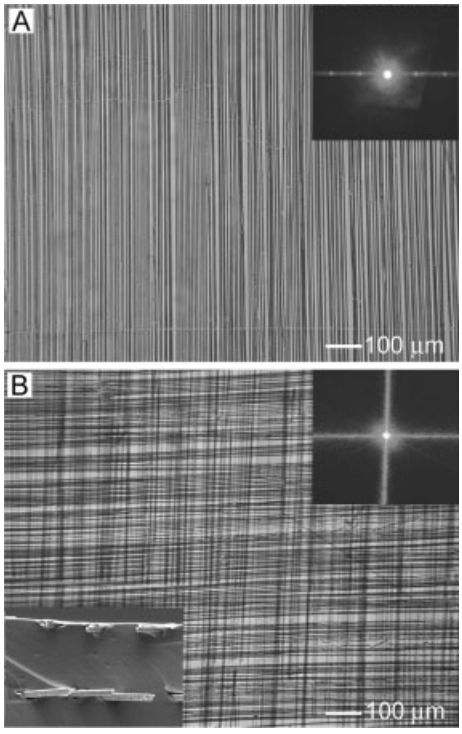


**Figure 12.** Optical micrographs of GaAs-wire arrays on PU/PET substrates with different numbers of layers of wires: A) single layer; B) double layers with cross angle of ~90°. The upper-right insets are the diffraction patterns generated from a laser beam perpendicularly passing through the PU/PET sheets with GaAs-wire arrays. The bottom-left inset of (B) is the SEM image taken from the cross-section of the sample in (B) with double layers of GaAs wires.

### 2.6. Extension of the Fabrication Process to Other Materials

This "top–down" approach can be used to generate wires or wire arrays of other semiconductor materials by judicial selection of anisotropic etchants. For example, InP wires with triangular cross-sections have been fabricated by etching a (100) InP wafer with $SiO_2$-mask lines along the $(0\bar{1}\bar{1})$ direction in a 1 vol.-% solution of $Br_2$ in methanol. In this case, $SiO_2$ replaced PR as an etching mask because methanol dissolves the PR. Figures 13A,B show typical SEM images of the InP wires before and after lift off from the mother substrate, respectively. The degree of undercutting for InP etching is less than that of GaAs, implying that InP wires with small widths (less than 500 nm) might be more easily prepared by using narrow $SiO_2$ stripes rather than by controlling the etching time. It is of note that the side walls of InP wires are much smoother than those of GaAs wires (compare Fig. 13B (inset) with Fig. 1E (inset)). The difference implies that the etching of InP does not initiate from the boundaries of the edges of the $SiO_2$-mask lines and the InP substrate. The arc-shaped surface of the remaining mother substrate with deep positions located at the areas without the $SiO_2$ mask (indicated by the arrows in Fig. 13A) indicates that the etching of InP starts from the cen-

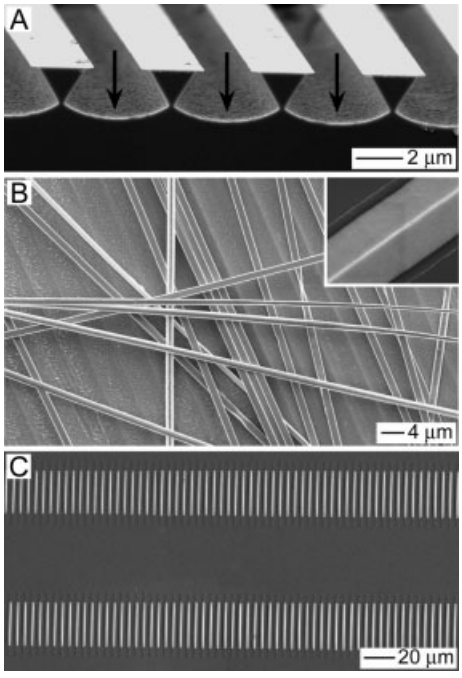


**Figure 13.** A) SEM image of the reverse-mesas of InP generated by etching InP wafer with $SiO_2$-mask stripes in a 1 vol.-% solution of $Br_2$ in methanol. B) SEM image of a random assembly of released InP wires on the mother substrate. C) SEM image of InP-wire arrays bonded to a PDMS stamp via $SiO_2$ stripes.

  

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tral portions of uncovered InP. In this case, the roughness of the side walls of the InP wires is mainly determined by the etching process rather than by the roughness of the edges of the $SiO_2$-mask stripes. The lengths of the InP wires can also be changed by controlling the length of the $SiO_2$-mask stripes, and the resultant wire arrays can be transfer printed onto plastic substrates (e.g., PU/PET) using a PDMS stamp.[15] Figure 13C shows an SEM image of two rows of InP-wire arrays attached to a PMDS stamp via the $SiO_2$-mask stripes. The formation of covalent siloxane (Si–O–Si) bonds between PDMS and $SiO_2$ enables us to pick up InP wires from the mother substrate.[26] These wires were fabricated from an InP wafer patterned with $SiO_2$ lines of 50 μm length and 2 μm width. The wires had lengths and widths of ~35 μm and ~1.7 μm, respectively. The InP wires on PDMS can then be printed onto PU/PET substrates using the procedure in Figure 11B.

## 3. Conclusions

A simple "top–down" approach was developed for fabricating micro/nanowires of GaAs and InP with triangular cross-sections from the bulk high-quality single-crystal wafers of these materials. The process is based on the combination of a photolithographic technique (i.e., traditional photolithography using a photomask or phase-shift lithography using a soft PDMS phase mask) and anisotropic chemical etching. The lateral dimensions of the resultant wires can be controlled by tuning the width of the mask stripes and the etching time, while their lengths are mainly dependent on the length of the mask stripes. The morphologies of the cross-sections (i.e., the relative length of each edge, and the angle $\alpha$) of GaAs wires is strongly dependent on the composition of the etchant system as well as the composition of the etching mask. Therefore, this "top–down" process with various tunable parameters generates better control over the dimensions, crystallinity, doping level, doping uniformity, and morphology of resultant wires than "bottom–up" synthetic approaches. Importantly, the left-behind mother wafer can be reused after polishing, so large numbers of wires can be generated from a single wafer, significantly decreasing fabrication costs.

Defining mask stripes surrounded by bulk film generates wire arrays with order and spatial orientations similar to that of the mask stripes. The as-obtained wire arrays on the mother substrates can be transfer printed with high fidelity onto plastic substrates coated with a thin layer of adhesive, in which the wires become embedded. This "dry" printing of "top–down" nano/microwires represents a new class of transfer processes that could be easily scaled up to larger areas and higher speeds because liquid solvents and complex instrumentation are not required in the process. The main disadvantage of this transfer process is that the edge roughness of the mask stripes, resulting from the lithography, limits the smoothness of the side walls and the uniformity in the widths of the wires. It is likely that these "top–down" fabrication and transfer printing processes can be extended to other materials by carefully selecting the composition of the anisotropic etchant. Wire arrays of semiconductors transfer printed onto plastic substrates could find immediate applications in various fields, such as high-performance flexible electronic devices.

## 4. Experimental

*Fabrication of GaAs Wires*: A layer of photoresist (Shipley 1805, Shipley Company LLC, Marlborough, MA) was spin-coated on a (100) GaAs wafer at a speed of 3000 rpm for 30 s, followed by soft-baking at 115 °C for 60 s. Exposing the wafer to UV light (12.5 mW cm$^{-2}$ in intensity, Karl Suss MJB3 mask aligner, Suss Microtec Inc., Waterbury Center, VT) for 6 s through the proper Cr photomask defined the patterned lines parallel to the $(0\bar{1}\bar{1})$ direction of the GaAs crystal. Developing the exposed wafer (MF-26 A developer, Rohm and Haas Electronics Materials LLC, Marlborough, MA) for 6 s generated photoresist patterns. A similar procedure was used to define line patterns of other photoresists (i.e., AZ5214 or poly(methyl methacrylate)) on the (100) GaAs wafer. For the line patterns of e-beam-evaporated materials, the GaAs wafers with patterned lines of photoresist (Shipley 1805) were placed in the chamber of an e-beam evaporator (Temescal, Berkeley, CA), and the desired materials were deposited on the wafers at high vacuum. Lifting off the photoresist in acetone left the mask lines made of dielectric (i.e., $SiO_2$) or metals (i.e., Au, Pd, and Ti/Au) on the GaAs wafer. For soft lithography using a phase mask, a polydimethylsiloxane (PDMS) stamp with patterned lines of several hundred nanometers width was first prepared from a master fabricated via e-beam lithography. In this step, the master was placed in a vacuum desiccator along with ~100 μL of (tridecafluoro-1,1,2,2-tetrahydrooctyl)-1-trichlorosilane (United Chemical Technologies Inc., Bristol, PA) for 2 h. The silanized master was covered with a thin film of high-modulus PDMS (Gelest Inc., Morrisville, PA) by spin-casting a mixture of 3.4 g (7–8 % vinylmethylsiloxane)–dimethylsiloxane copolymer, 100 μg of 1,3,5,7-tetravinyl-1,3,5,7-tetramethylcyclotetrasiloxane, 50 μg of platinum catalyst, and 1 g (25–30 % methylhydrosiloxane)–dimethylsiloxane copolymer, followed by pouring the low-modulus PDMS (component ratio A/B = 1:10, Sylgard 184, Dow Corning Corp., Midland, MI) onto the master. Baking at 65 °C for 2 h completed the curing of the polymers. Peeling away the composite PDMS formed the soft phase mask. The phase mask was then placed on the (100) GaAs wafer covered with photoresist film (Shipley 1805, spin-cast at 5000 rpm for 60 s), with the lines on PDMS aligned parallel along the $(0\bar{1}\bar{1})$ direction of the GaAs crystal. Exposing and developing generated the patterned lines of photoresist with widths of ~200 nm. The etchant was prepared by mixing 4 mL of $H_3PO_4$ (85 wt.-%), 52 mL of $H_2O_2$ (30 wt.-%), and 48 mL of deionized water in an ice-water bath. Immersion of GaAs wafers with various etching masks in the etchant generated GaAs wires through anisotropic etching. The resultant samples were rinsed with deionized water or acetone, dried, and prepared for taking images and transfer printing.

*Fabrication of InP Wires*: The $SiO_2$ mask was defined via the same procedure as that used for GaAs. The etchant was prepared by mixing 1 mL of $Br_2$ liquid and 100 mL of methanol at room temperature. Immersion of InP wafers with $SiO_2$ masks in the etchant for appropriate times generated InP wires through chemical etching. Caution: This operation must be performed in a well-ventilated hood because $Br_2$ is highly volatile and toxic.

*Transfer Printing of Wire Arrays on Plastic Substrates*: The transfer element, i.e., a flat PDMS sheet, was prepared by pouring the mixture of low-modulus PDMS (A/B = 1:10, Sylgard 184, Dow Corning) onto a piece of silicon wafer pre-modified with a monolayer of (tridecafluoro-1,1,2,2-tetrahydrooctyl)-1-trichlorosilane, followed by baking at 65 °C for 2 h. Rinsing the PDMS stamp with ethanol generates a clean and hydrophobic surface after it was peeled off from the Si wafer. Placing the PDMS stamp against the surface of a GaAs wafer with a wire array resulted in conformal contact between PDMS and the surface of the PR stripes. Leaving the system in contact for 10 h generated strong hydrophobic–hydrophobic interactions between PDMS and the PR. Peeling the PDMS stamp from the GaAs wafer lifted off all the GaAs wires

  

(with the PR-mask stripes). The GaAs wires on the PDMS stamp can be transferred to a poly(ethylene terephthalate) (PET) substrate via an adhesive layer, i.e., polyurethane (PU). In this process, the PDMS stamp was placed against a thin layer of liquid PU (NOA 73, Norland Products, Cranbury, NJ) spin-coated onto a plastic PET substrate with a thickness of ~175 μm (Mylar film, Southwall Technologies, Palo Alto, CA). Illuminating the sample with an UV lamp (Model B 100 AP, Black-Ray, Upland, CA) for 1 h cured the PU layer and formed a strong bond between the cured PU and the GaAs wires, and between the cured PU and the PET sheet. Peeling away the PDMS stamp left the GaAs wires and PR stripes embedded in the matrix of cured PU.

Received: September 8, 2004
Final version: September 30, 2004
Published online: December 20, 2004

[1] a) Y. Xia, P. Yang, Y. Sun, Y. Wu, B. Mayers, B. Gates, Y. Yin, F. Kim, H. Yan, *Adv. Mater.* **2003**, *15*, 353. b) A. P. Alivisatos, P. F. Barbara, A. W. Castleman, J. Chang, D. A. Dixon, M. L. Kline, G. L. Melendon, J. S. Miller, M. A. Ratner, P. J. Rossky, S. I. Stupp, M. I. Thompson, *Adv. Mater.* **1998**, *10*, 1297. c) M. Nirmal, L. Brus, *Acc. Chem. Res.* **1999**, *32*, 407. d) G. Markovich, C. P. Collier, S. E. Henrichs, F. Remacle, R. D. Levine, J. R. Heath, *Acc. Chem. Res.* **1999**, *32*, 415. e) J. Hu, T. W. Odom, C. M. Lieber, *Acc. Chem. Res.* **1999**, *32*, 435.

[2] a) M. H. Huang, S. Mao, H. Feick, H. Yan, Y. Wu, H. Kind, E. Weber, R. Russo, P. Yang, *Science* **2001**, *292*, 1897. b) M. Law, D. J. Sirbuly, J. C. Johnson, J. Goldberger, R. J. Saykally, P. Yang, *Science* **2004**, *305*, 1269. c) Z. W. Pan, Z. R. Dai, Z. L. Wang, *Science* **2001**, *291*, 1947. d) X. Y. Kong, Y. Ding, R. Yang, Z. L. Wang, *Science* **2004**, *303*, 1348. e) Y. Wang, X. Jiang, Y. Xia, *J. Am. Chem. Soc.* **2003**, *125*, 16176. f) D. Battaglia, J. J. Li, Y. Wang, X. Peng, *Angew. Chem. Int. Ed.* **2003**, *42*, 5035. g) D. J. Milliron, S. M. Hughes, Y. Cui, L. Manna, J. Li, L.-W. Wang, A. P. Alivisatos, *Nature* **2004**, *430*, 190.

[3] A. D. Yoffe, *Adv. Phys.* **1993**, *42*, 173.

[4] W. U. Huynh, J. J. Dittmer, A. P. Alivisator, *Science* **2002**, *295*, 2425.

[5] a) E. Menard, K. J. Lee, D.-Y. Khang, R. G. Nuzzo, J. A. Rogers, *Appl. Phys. Lett.* **2004**, *84*, 5398. b) X. Duan, C. Niu, V. Sahl, J. Chen, J. W. Parce, S. Empedocles, J. L. Goldman, *Nature* **2003**, *425*, 274. c) B. A. Ridley, B. Nivi, J. M. Jacobson, *Science* **1999**, *286*, 746.

[6] a) P. P. Jenkins, A. N. Macinnes, M. Tabibazar, A. R. Barron, *Science* **1994**, *263*, 1751. b) A. L. Robinson, *Science* **1983**, *219*, 275. c) H. Morkoc, S. N. Mohammad, *Science* **1995**, *267*, 51. d) M. Razeghi, *Nature* **1994**, *369*, 631. e) N. Matsunaga, M. Yamamoto, Y. Hatta, H. Masuda, *IEEE Trans. Electron Devices* **2003**, *50*, 1194. f) J. L. Leclercq, R. P. Ribas, J. M. Karam, P. Viktorovitch, *Microelectron. J.* **1998**, *29*, 613.

[7] a) *Semiconductor Sensors* (Ed: S. M. Sze), Wiley, New York **1994**. b) C. Y. Chang, R. Kai, *GaAs High-Speed Devices: Physics, Technology, and Circuit Applications*, Wiley, New York **1994**.

[8] R. S. Wagner, W. C. Ellis, *Appl. Phys. Lett.* **1964**, *4*, 89.

[9] X. Duan, C. M. Lieber, *Adv. Mater.* **2000**, *12*, 298.

[10] a) Z. H. Wu, X. Mei, D. Kim, M. Blumin, H. E. Ruda, *Appl. Phys. Lett.* **2003**, *83*, 3368. b) N. Panev, A. I. Persson, N. Sköld, L. Samuelson, *Appl. Phys. Lett.* **2003**, *83*, 2238. c) T. Martensson, P. Carlberg, M. Borgström, L. Montelius, W. Seifert, L. Samuelson, *Nano Lett.* **2004**, *4*, 699. d) Z. H. Wu, X. Y. Mei, D. Kim, M. Blumin, H. E. Ruda, *Appl. Phys. Lett.* **2002**, *81*, 5177. e) S. Bhunia, T. Kawamura, S. Fujikawa, K. Tokushima, Y. Watanabe, *Phys. E (Amsterdam, Neth.)* **2004**, *21*, 583.

[11] a) T. J. Trentler, K. M. Hickman, H. Subhash, C. Goel, A. M. Viano, P. C. Gibbons, W. E. Buhro, *Science* **1995**, *270*, 1791. b) H. Yu, W. E. Buhro, *Adv. Mater.* **2003**, *15*, 416. c) H. Yu, J. Li, R. A. Loomis, L.-W. Wang, W. E. Buhro, *Nat. Mater.* **2003**, *2*, 517.

[12] F. M. Davidson III, A. D. Schricker, R. J. Wiacek, B. A. Korgel, *Adv. Mater.* **2004**, *16*, 646.

[13] a) Y. Yin, B. Gates, Y. Xia, *Adv. Mater.* **2000**, *12*, 1426. b) T. Höche, R. Böhme, J. W. Gerlach, F. Frost, K. Zimmer, B. Rauschenbach, *Nano Lett.* **2004**, *4*, 895.

[14] *Handbook of Semiconductor Manufacturing Technology* (Eds: Y. Nishi, R. Doering), Marcel Dekker, New York **2000**, Ch. 17.

[15] Y. Sun, J. A. Rogers, *Nano Lett.* **2004**, *4*, 1953.

[16] Z. L. Wang, *J. Phys. Chem. B* **2000**, *104*, 1153.

[17] a) J. A. Rogers, K. E. Paul, R. J. Jackman, G. M. Whitesides, *J. Vac. Sci. Technol., B: Microelectron. Nanometer Struct.—Process., Meas., Phenom.* **1998**, *16*, 59. b) J. A. Rogers, K. E. Paul, R. J. Jackman, G. M. Whitesides, *Appl. Phys. Lett.* **1997**, *70*, 2658.

[18] S. Jeon, E. Menard, J.-U. Park, J. Maria, M. Meitl, J. Zaumseil, J. A. Rogers, *Adv. Mater.* **2004**, *16*, 1369.

[19] D. W. Shaw, *J. Electrochem. Soc.* **1981**, *128*, 874.

[20] a) J. J. Gannon, C. J. Nuese, *J. Electrochem. Soc.* **1974**, *121*, 1215. b) K. Kenefick, *J. Electrochem. Soc.* **1982**, *129*, 2380. c) S. H. Jones, D. K. Walker, *J. Electrochem. Soc.* **1990**, *137*, 1653. d) D. G. Hill, K. L. Lear, J. S. Harris, Jr., *J. Electrochem. Soc.* **1990**, *137*, 2912.

[21] Y. Tarui, Y. Komiya, Y. Harada, *J. Electrochem. Soc.* **1971**, *118*, 118.

[22] Y. Mori, N. Watanabe, *J. Electrochem. Soc.* **1978**, *125*, 1510.

[23] S. Adachi, K. Qe, *J. Electrochem. Soc.* **1983**, *130*, 2427.

[24] F. Zhou, Z. Liu, B. Yu, M. Chen, J. Hao, W. Liu, Q. Xue, *Surf. Sci.* **2004**, *561*, 1.

[25] a) M. Morra, E. Occhiello, R. Marola, F. Garbassi, P. Humphrey, D. Johnson, *J. Colloid Interface Sci.* **1990**, *137*, 11. b) K. M. Choi, J. A. Rogers, *J. Am. Chem. Soc.* **2003**, *125*, 4060.

[26] D. C. Duffy, C. McDonald, O. J. A. Schueller, G. M. Whitesides, *Anal. Chem.* **1998**, *70*, 4974.

  