高頻高压半导世界

_GaN可靠嗎?找歪伯理論

Reliability of GaN Power Devices

王不老說半导

4/24/2022

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- 1939年他更发表了Weibull Distribution
  - 当时瑞典军部及武器制造商(Bofors)就是用他發明的品管方式来保证瑞士武器制造精良(當時世界第一流)

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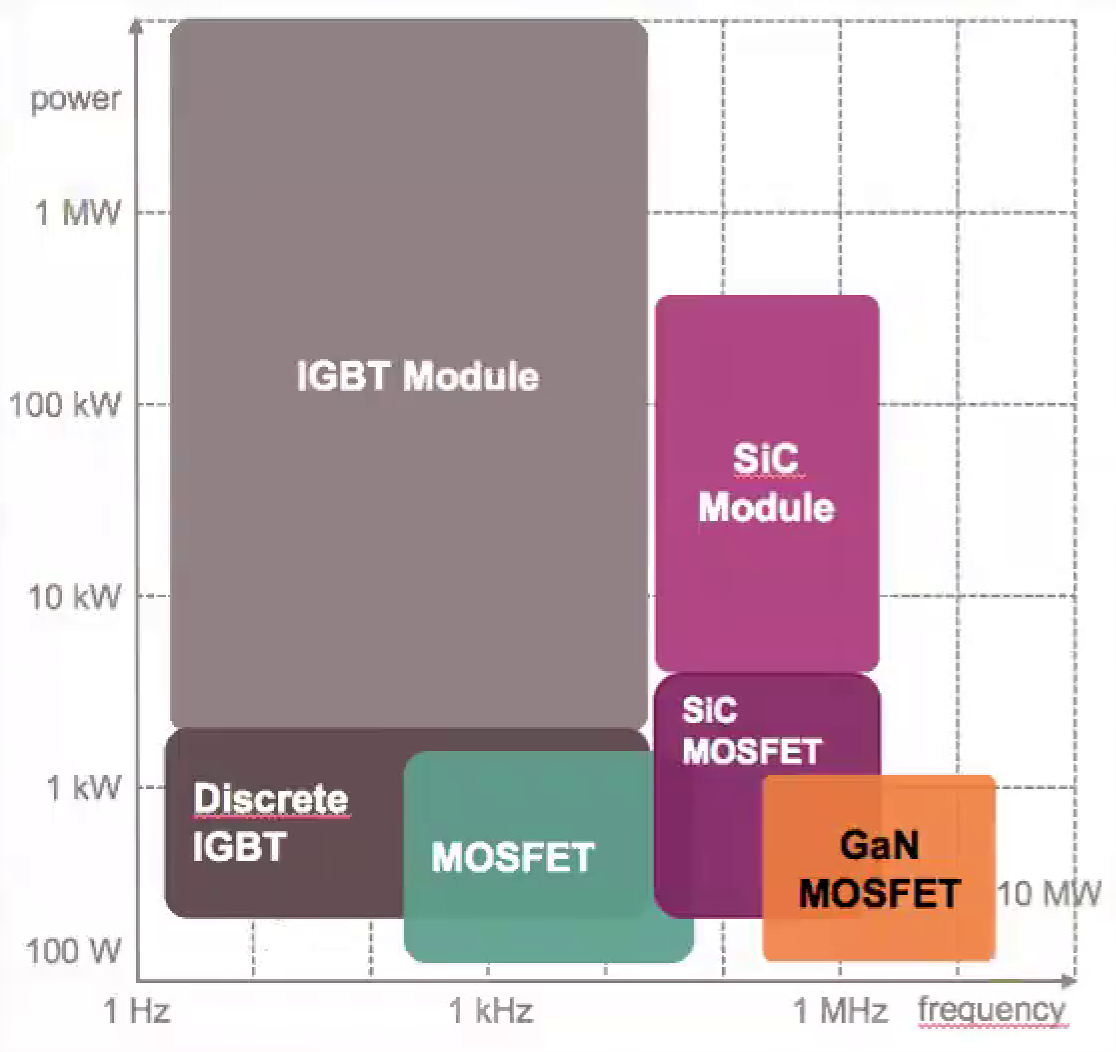
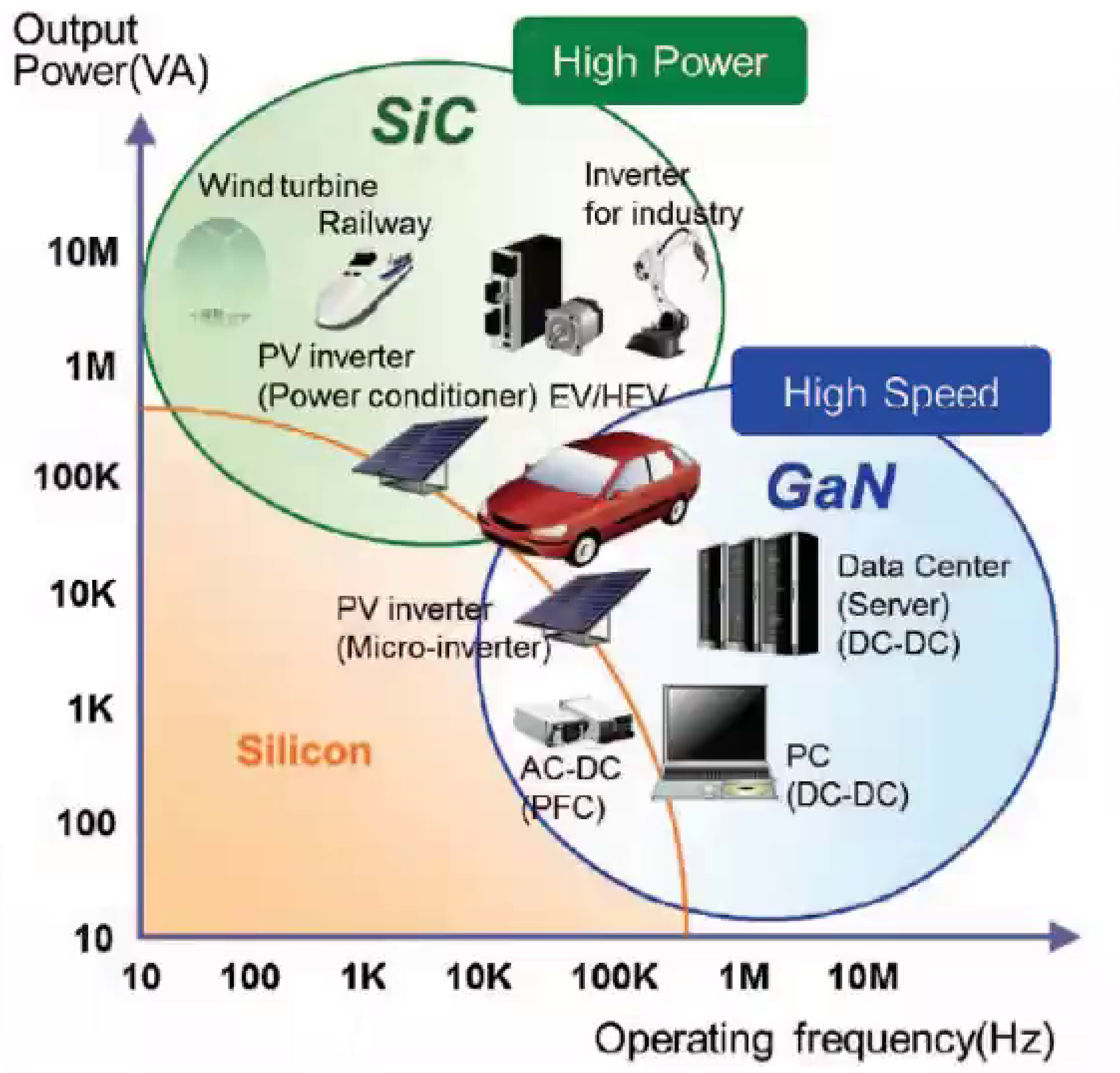
GaN拔劍四顧心不茫



https://semiengineering.com/improving-reliability-for-gan-and-sic/



T. Ueda, "Reliability issues in GaN and SiC power devices," 2014 IEEE IRPS'14, pp. 3D.4.1-3D.4.6

歪伯愛洗澡: 产品可靠性澡盆曲线

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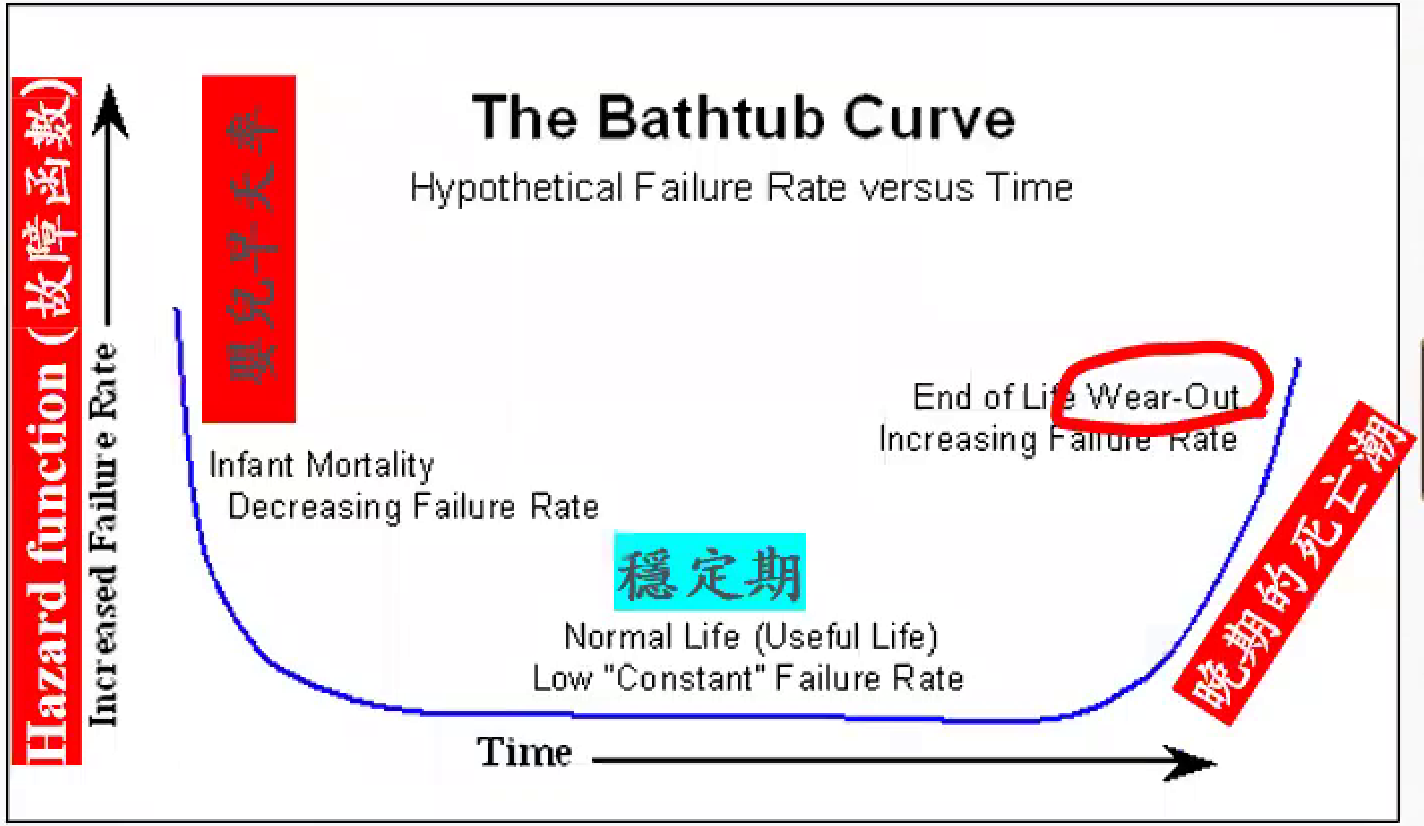

https://www.weibull.com/hotwire/issue21/hottopics21.htm

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Weibull Distribution:可靠性分析很給力

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  - $f(T) = \frac{\beta}{\eta}\left(\frac{T-\gamma}{\eta}\right)^{\beta-1} e^{-\left(\frac{T-\gamma}{\eta}\right)^{\beta}}$
    - β = shape parameter (形狀參數)
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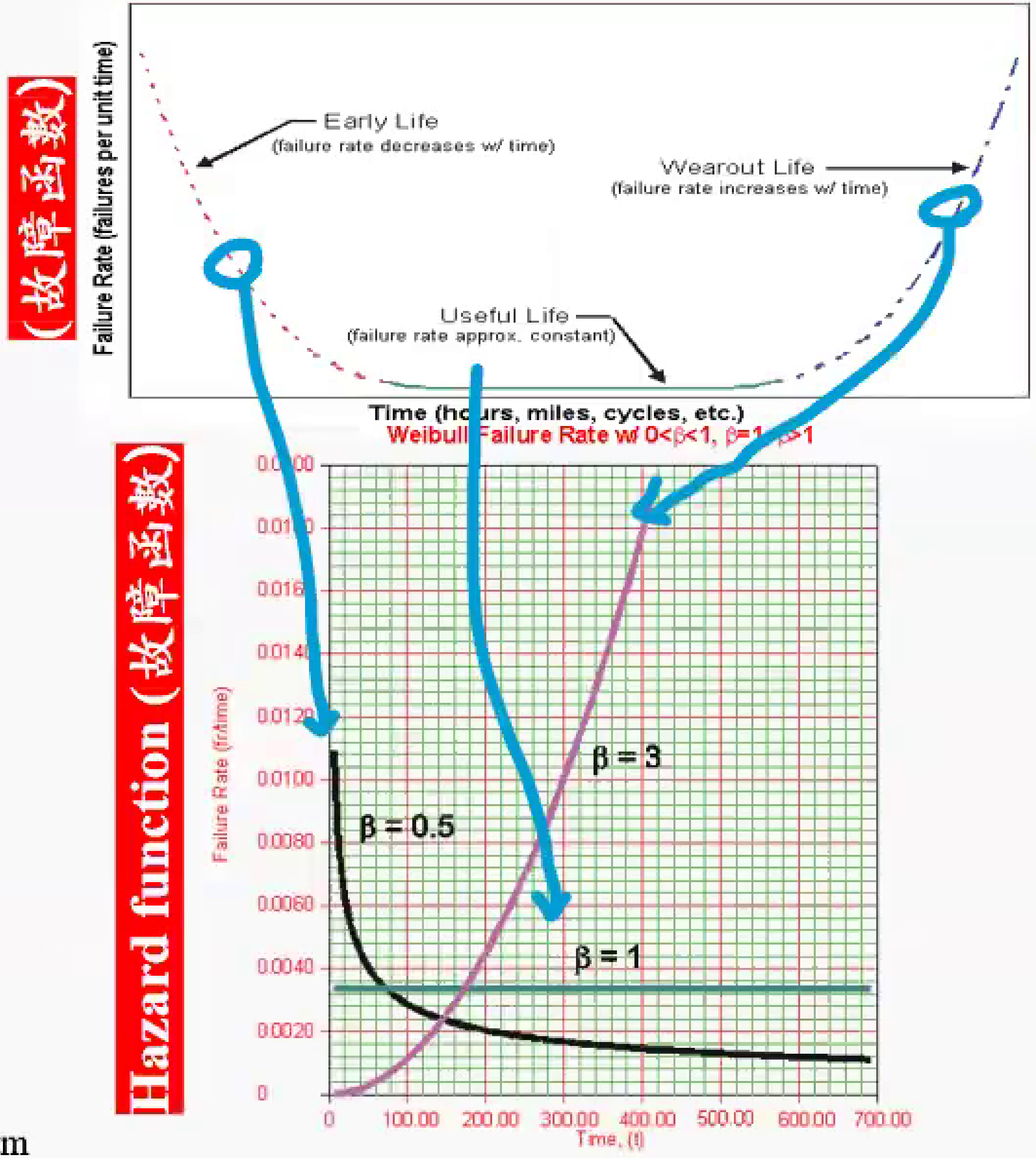
  - γ = location parameter (thresh in Minitab)
- 歪伯厲害的地方就是用他以他發明的概率密度函數(PDF)推导出適當的**故障函數**，竟能解釋产品可靠性澡盆曲线所有部分



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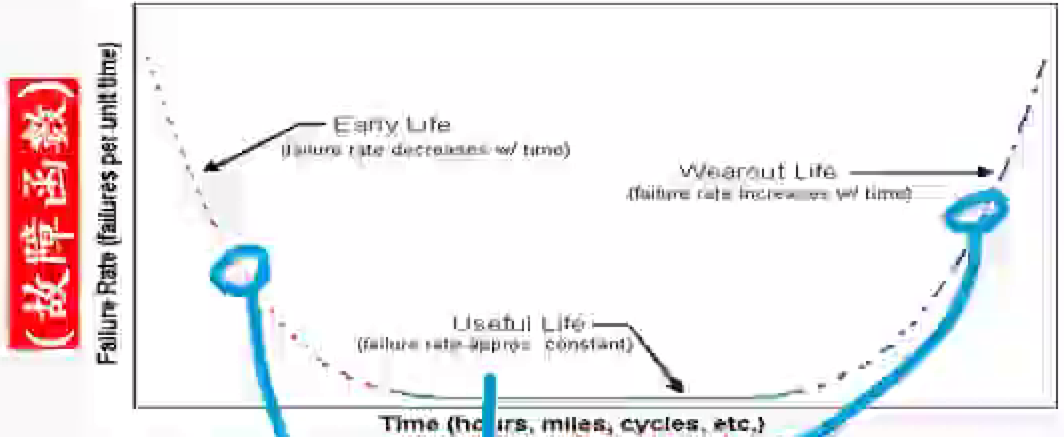

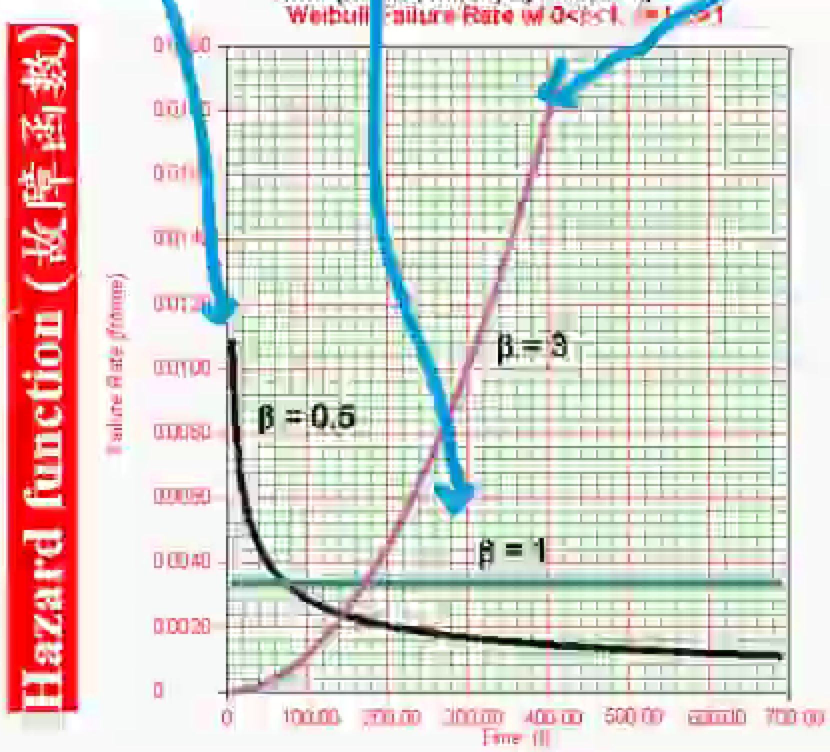

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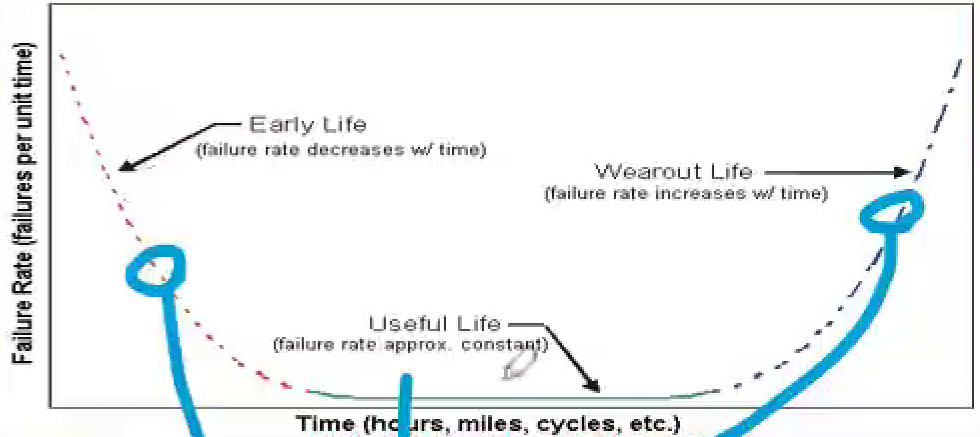
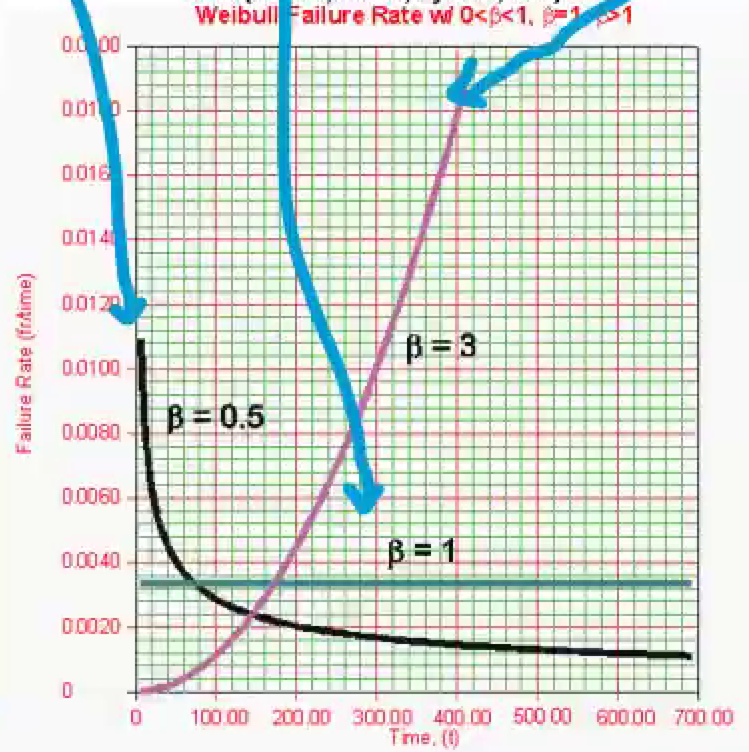


Hazard function (故障函數)



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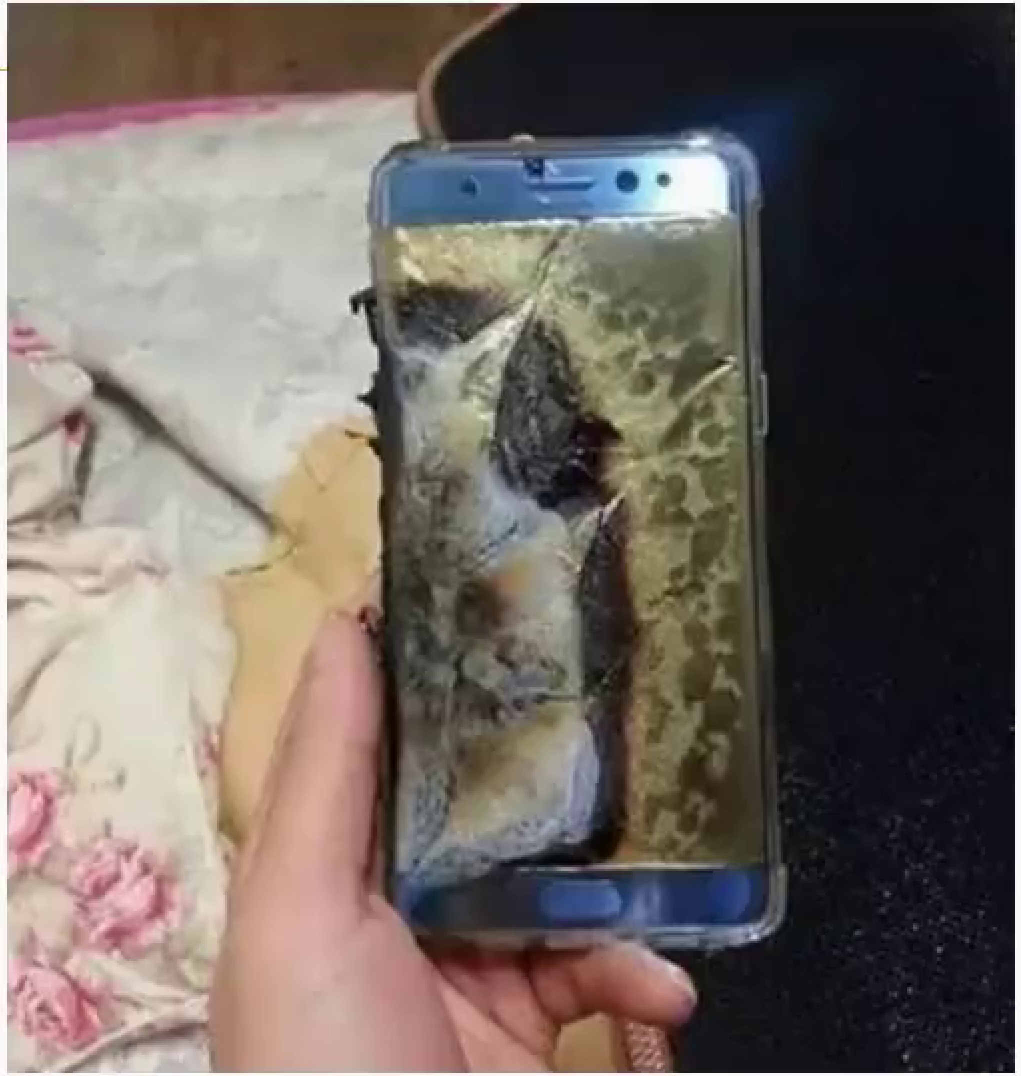
β < 1(夭折死): 2016 三星 Note 7

三星终向中国消费者低头Note7全面召回!

- 8月2日，三星Note7欧美地区开售
- 8月24日，全球首炸(早夭)
- 10月11日，三星终于宣布也在中國召回全部Note7手机，共计190984台，中国消费者也得到了与全球一样的待遇

Note7手機下架共損失54億美元

- 三星想要赶在iPhone之前，匆忙出货



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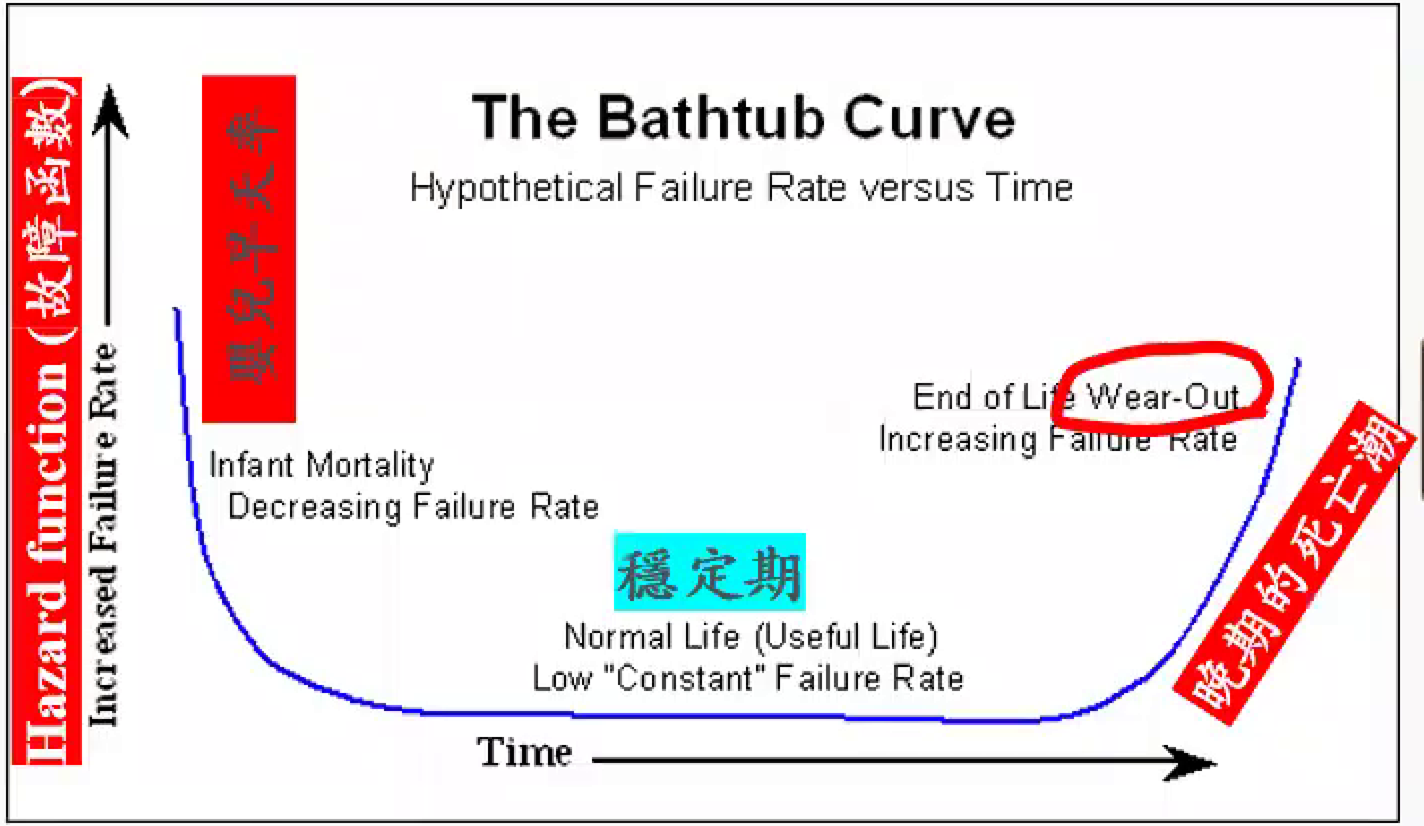

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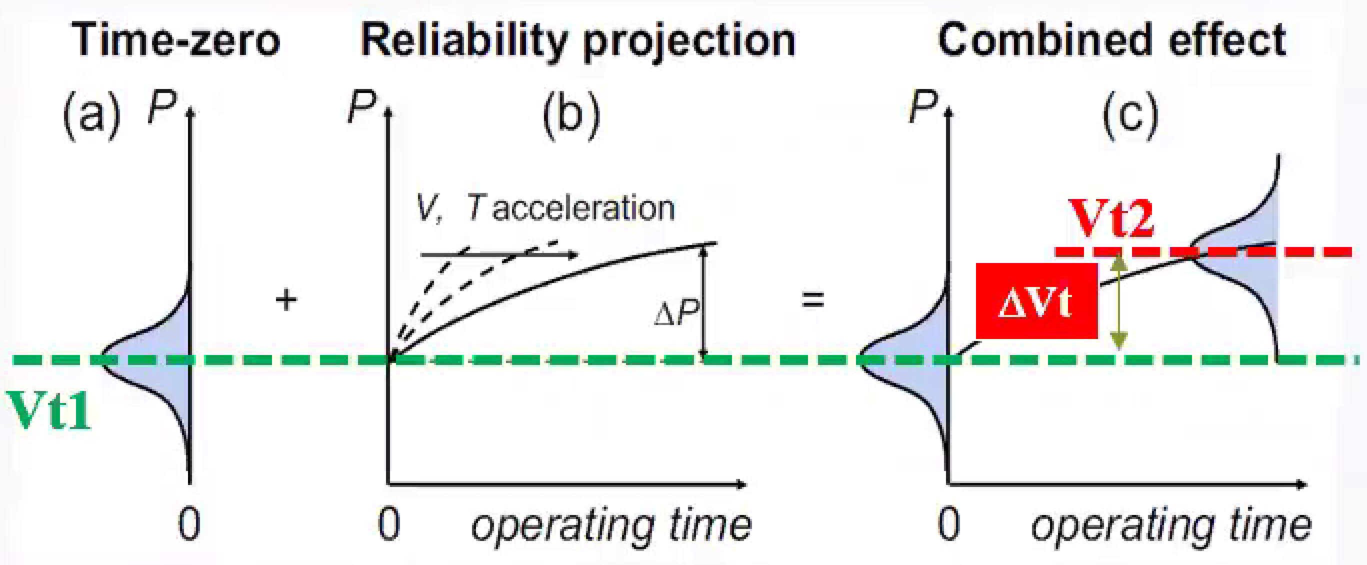
Si-CMOS的可靠性分析參數

- Si-CMOS內某重要电性參數(P)因時間及使用，就如同輪胎一般，開始有老化漂移現象，例如P = Vt， Vt shift = ΔVt
- 我們知道$I_d \propto (Vg\text{-}Vt)^2$，若Vg = 0.7V，Vt1 = 0.3V，老化漂移後Vt2 = 0.35V， ΔVt =50mV，I_{d2}= 0.765I_{d1}，元件就算拜拜了
- 基本上，我們要求电子元10年內，只能容許ΔVt = 50mV
  - 但我們卻沒有10年可以等啊!



The defect-centric perspective of device and circuit reliability—From gate oxide defects to circuits, B. Kaczer et al., Solid-State Electronics 125 (2016) 52–62

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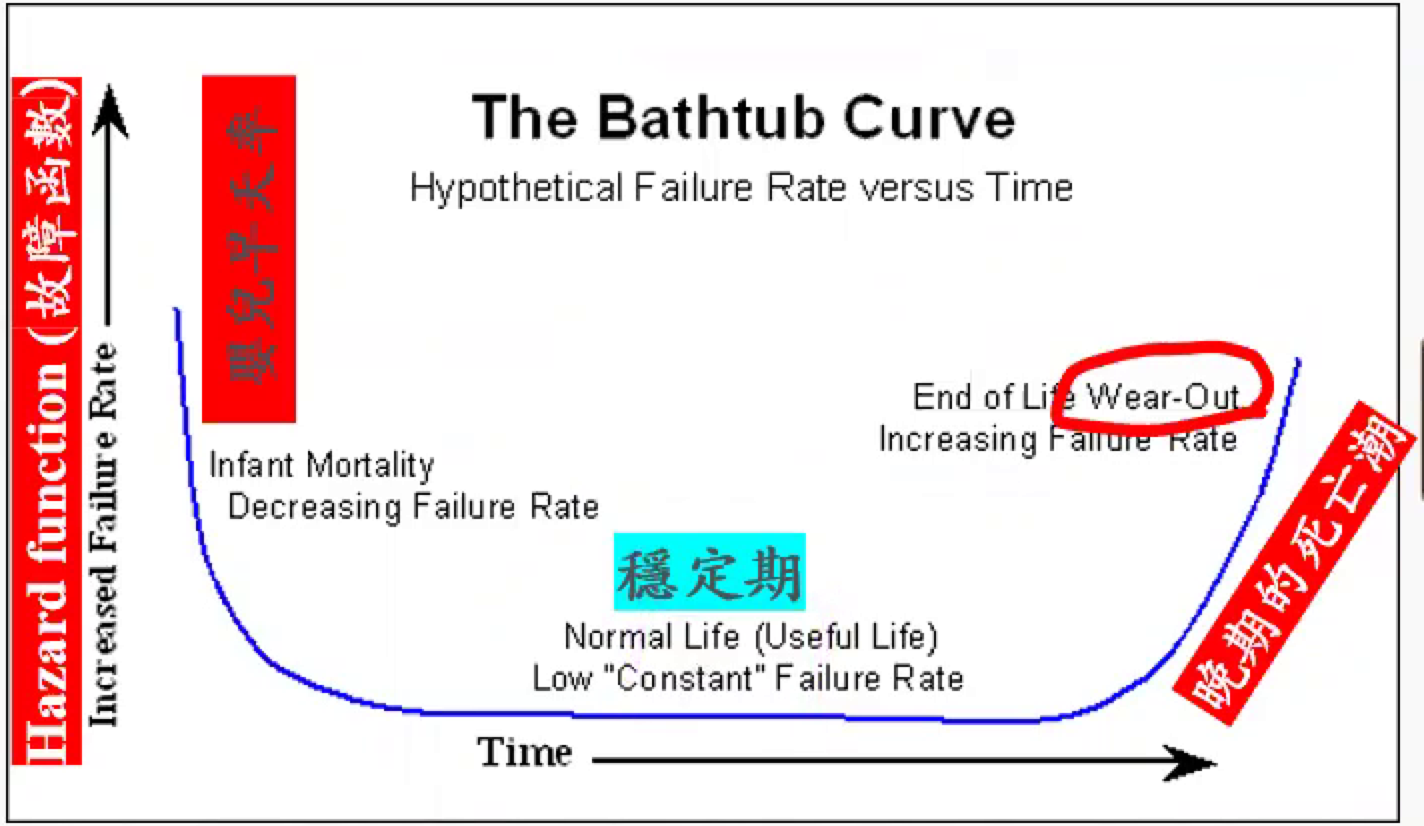

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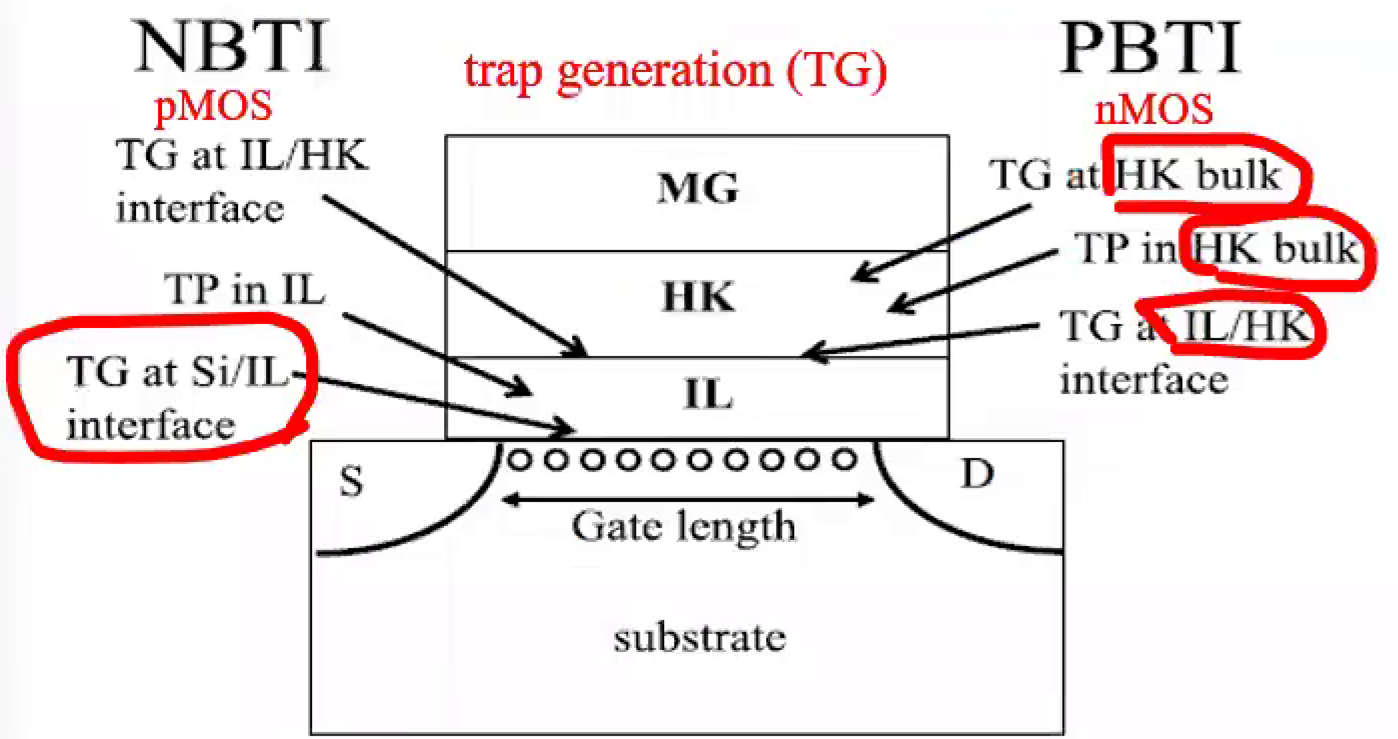
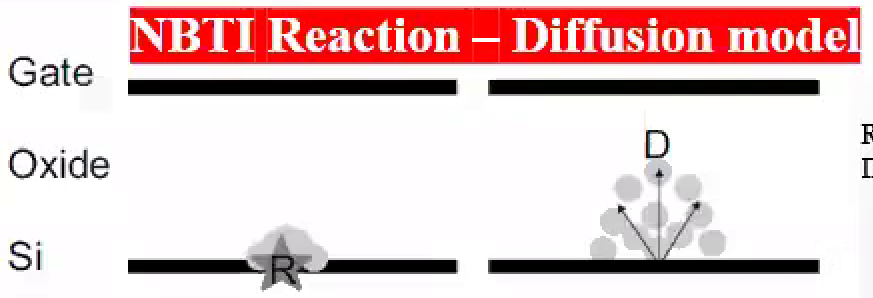
Si-CMOS的可靠性分析參數

- 电子老化漂移當然由內部最脆弱的地方開始，例如
- **Negative-bias temperature instability(NBTI)**负偏置温度不稳定性是影响阈值电压Vt的偏移，其乃因Silicon IL介面太脆弱(dangling bonds)，解決方法為以重氫(D_2)重拳出擊(high temperature deuterium anneal，~1000C)，介面得以強化也(這制程之优化，竟耗費Intel/IBM數年)

Mukhopadhyay et al, "A Comparative Study of NBTI and PBTI Using Different Experimental Techniques," in TED, 63(10)4038-4045, 2016





RELIABILITY ENGINEERING IN RF CMOS, Guido T. Sasse

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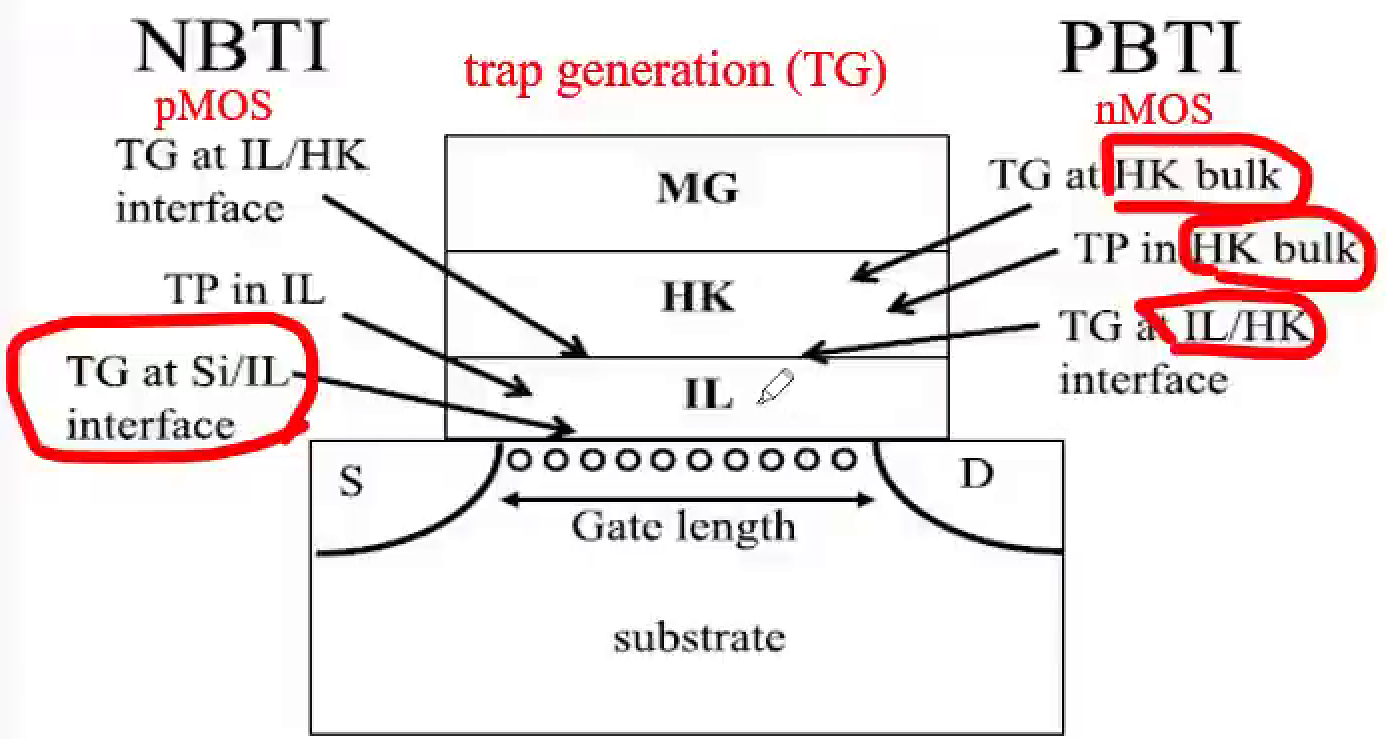

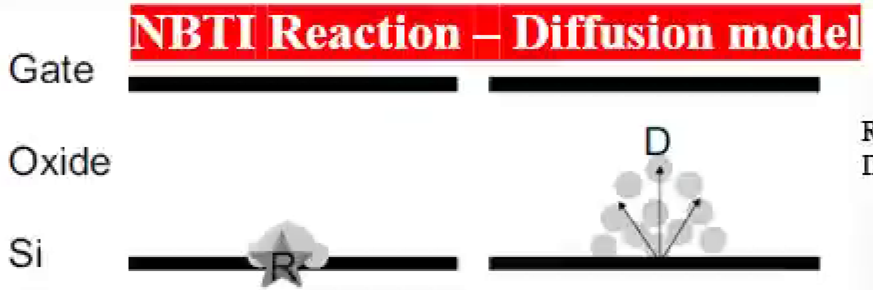

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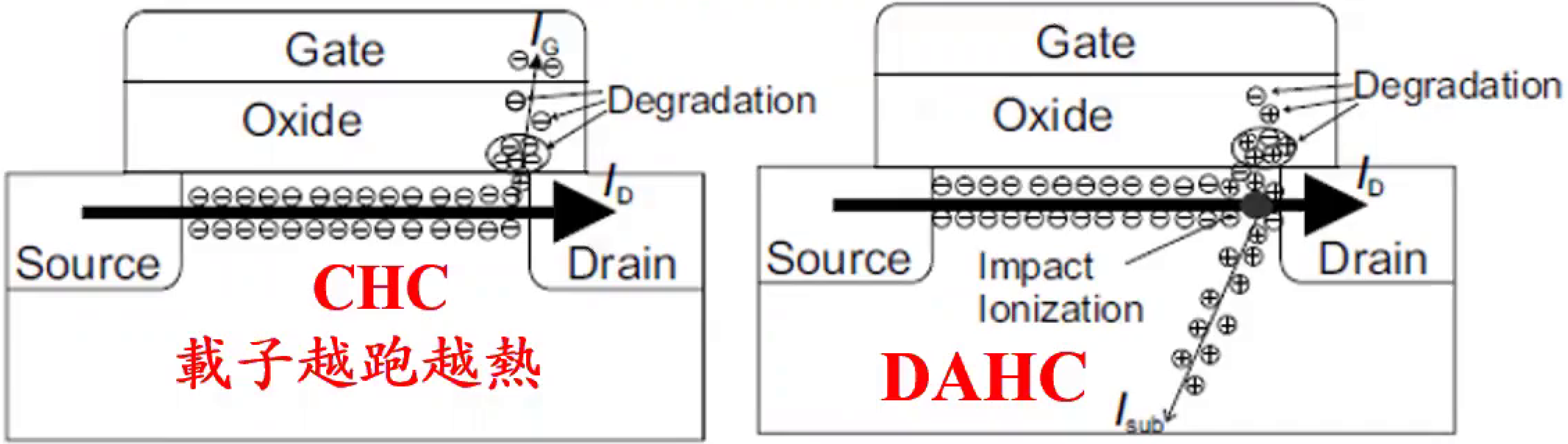
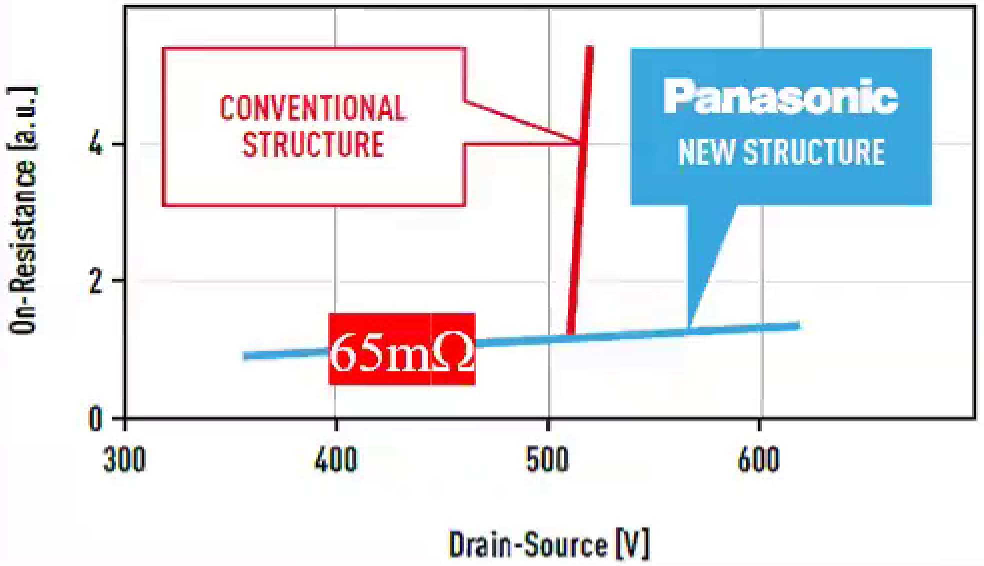
被加速到自爆: Channel Hot Carriers (CHC)

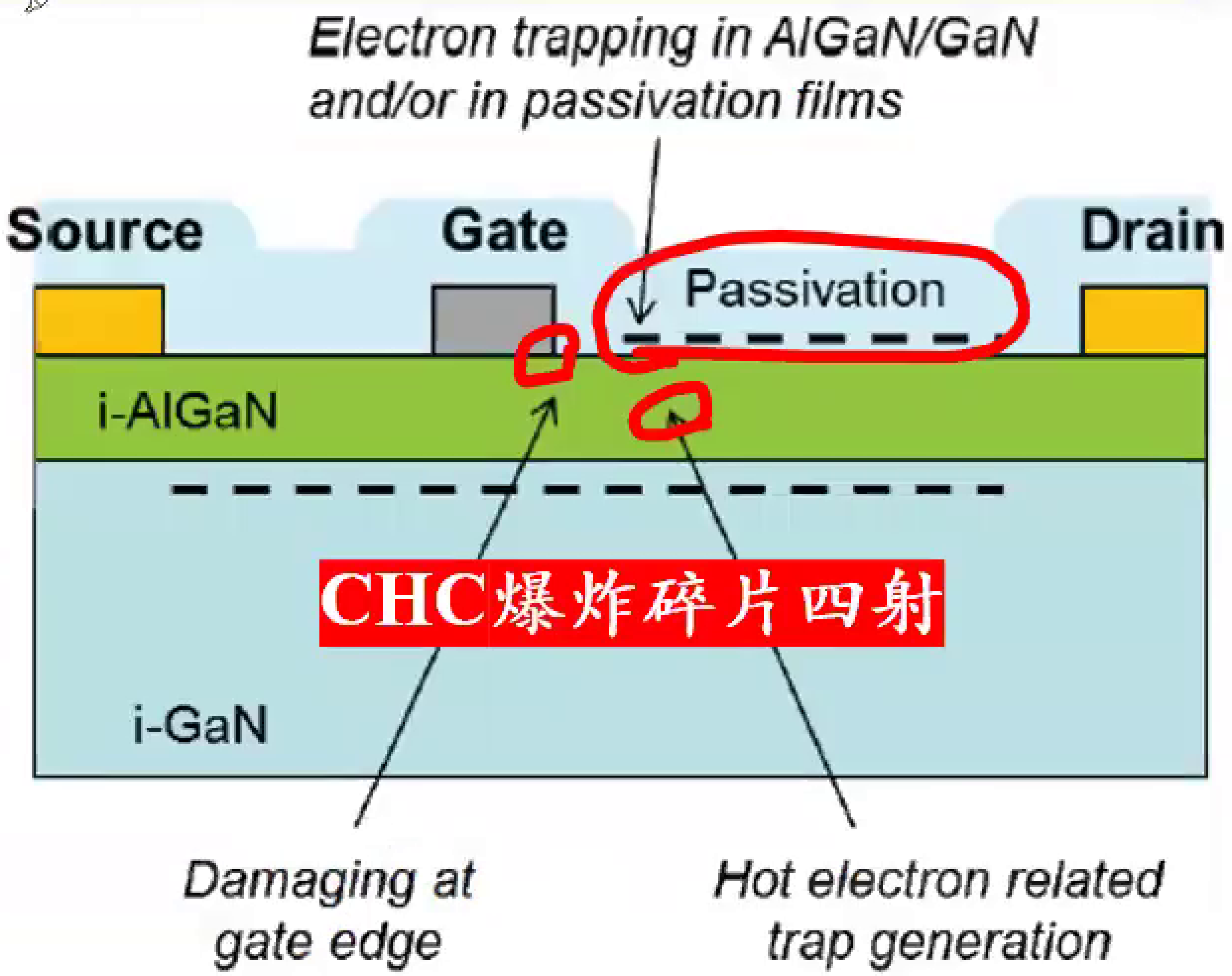
- 电子見到V_{DS}立馬興奮从Source衝向Drain，越跑越快(故動能分布好似溫度越來越高，所以曰之Hot)，在近終点處竟翻車爆炸了(Drain的电場太強)
- 爆炸碎片四射，傷及一堆池魚，包括oxide, gate，Interfaces , 及Drain漏电雪崩 (Drain Avalanche Hot Carriers，DAHC)等



Reliability Issues in GaN Power Devices

- 前面Si-CMOS，我們舉了個P=Vt的例子，但在GaN power devices, P = On-Resistance (current collapse),
- 左下图所示，电阻突然在$V_D > 500V$時，瞬間拔高(电流消失了)，怎麼回事?原來是一個CHC效應(右图)，





https://eu.industrial.panasonic.com/sites/default/pidseu/files/pan_18047_whitepaper_gan_web.pdf

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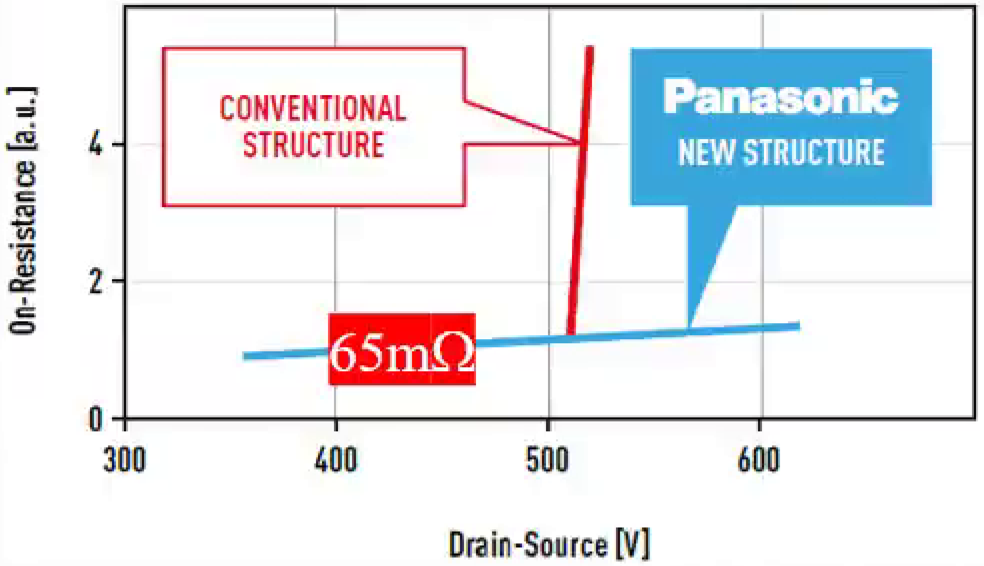

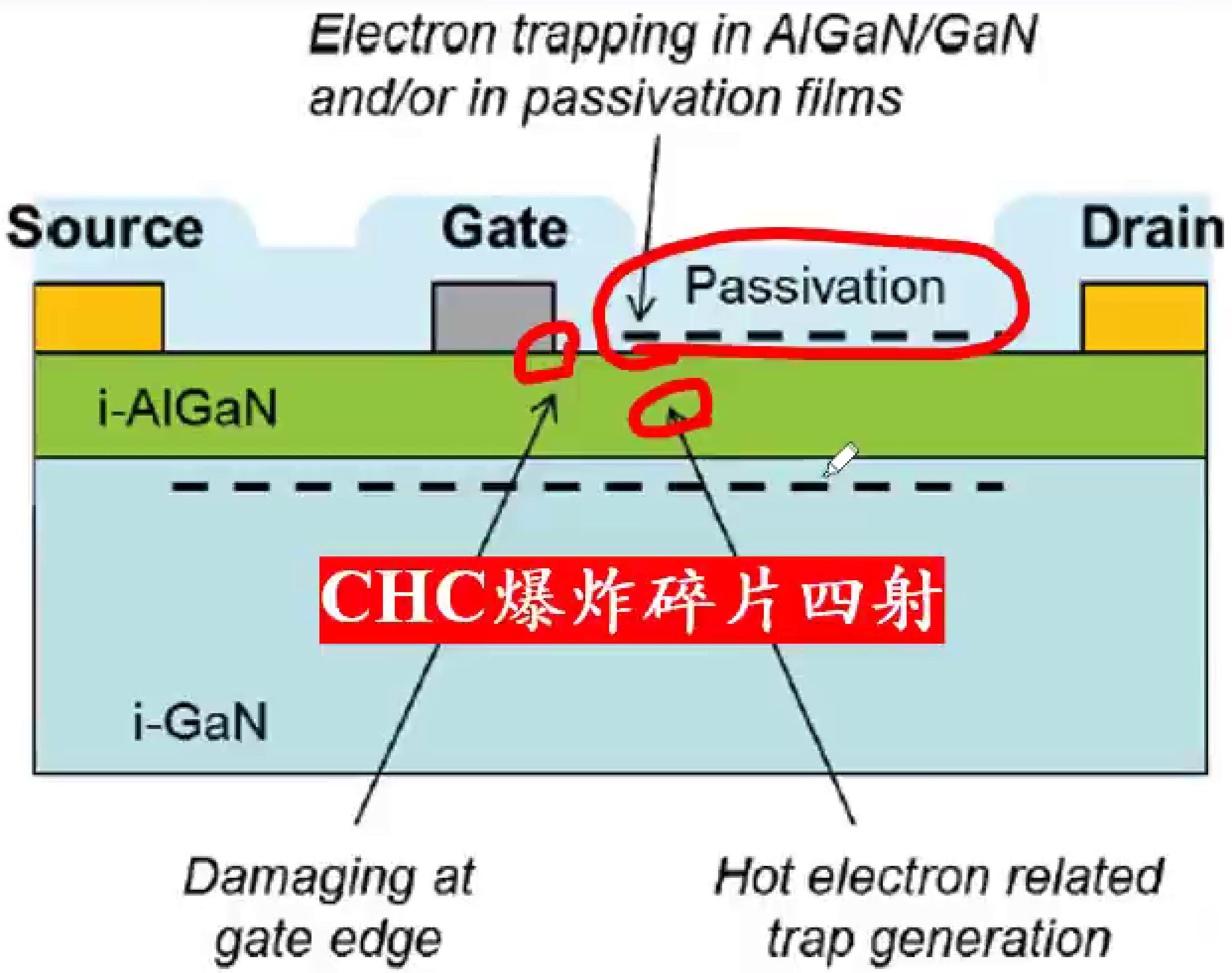

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業界可靠性測試標準 JEDEC: JEP180.01

- **GUIDELINE FOR SWITCHING RELIABILITY EVALUATION PROCEDURES FOR GALLIUM NITRIDE POWER CONVERSION DEVICES**

https://www.jedec.org/standards-documents/docs/jep18001

Table 2 — DHTOL recommendations

Stress name	Abbrev.	Conditions	Requirements	
			# Lots / units per lot	Duration / Acceptance
Dynamic High Temperature Operating Life	DHTOL	Maximum recommended switching conditions 1) (Table 3)	3 Lots X ≥ 8 test beds of core-cells. (2)	1000h 1) / 0 Fails

1) Test conditions can exceed the maximum recommended ones to increase the equivalent application runtime at customer-use conditions. Until industry confidence is built in the model, durations shorter than 1000h would need agreement of the user.
2) A core cell is defined as the basic switching cell, clause 4.6

Table 3 — Best-practice DHTOL conditions

Stress parameter	Conditions	Example
DC bus voltage	Maximum recommended V_{DS} or 80% of absolute maximum V_{DS} per datasheet	480V (600V abs. max.)
Operating junction temperature	Worst case temperature, T_J, within datasheet operating limits	80 °C ≤ T_J ≤ 125 °C represents the typical expected temperature range in application. In case of supporting data T_J shall be set to be the worst case for the technology
Peak current	Corresponding to the maximum power condition	Technology/product dependent Test chamber dependent (in particular cooling limited)
Switching frequency	Max allowable for the desired operating junction temperature	e.g., 100kHz for hard-switching application.
Gate driving conditions	As recommended by manufacturer in datasheet and application note	Technology/product dependent

業界可靠性測試標準 JEDEC的歪伯精神

- 當然我們也希望GaN产品的生命週期像個很長的澡盆(如右)
- 意思是說，將制程優化改進，使得wear Out能越晚來到越好
- 又除了JEDEC，還有AEC
    - http://www.aecouncil.com/AECDocuments.html

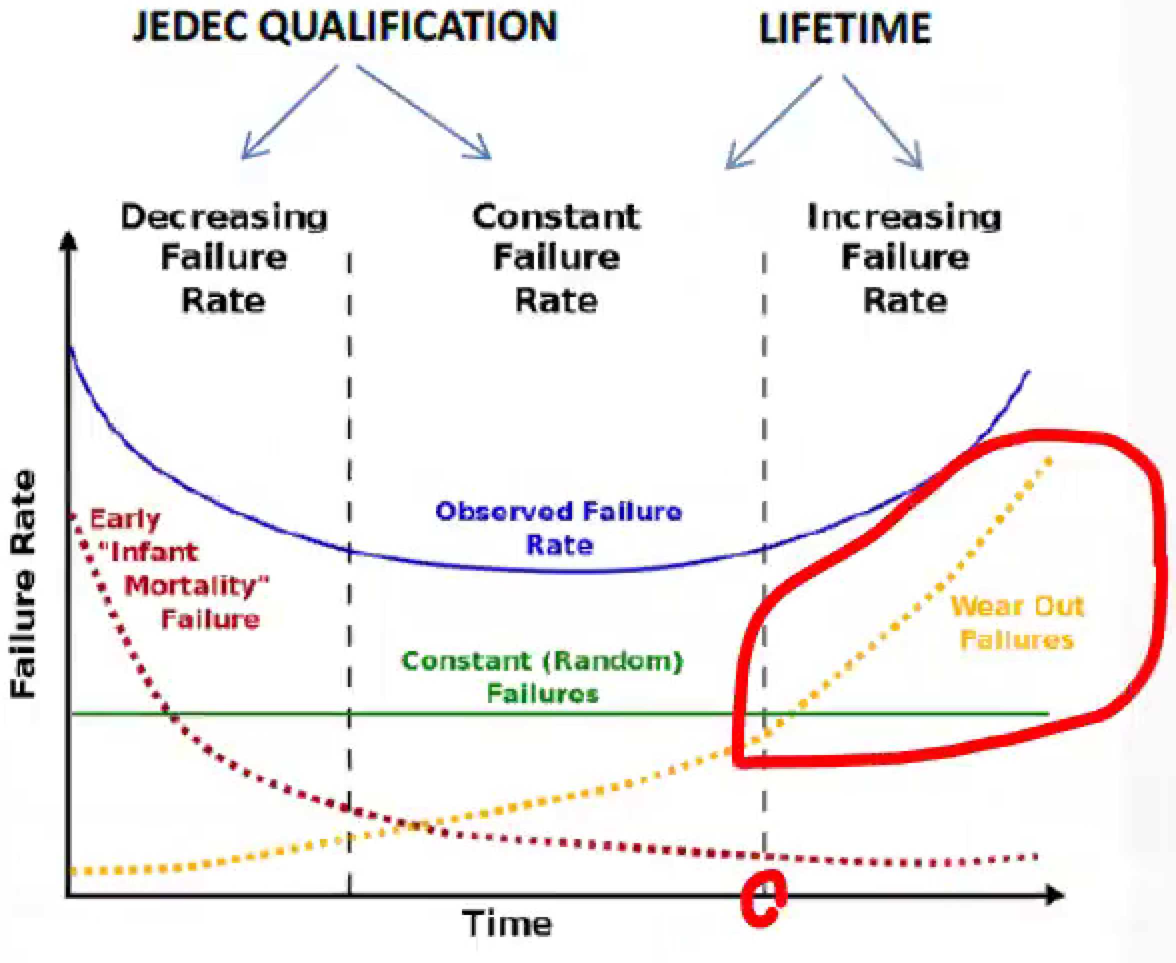

Figure 1. Reliability lifecycle illustrated using a "bathtub curve"

Reliability Lifecycle of GaN Power Devices Kurt Smith , Ronald Barr 2017

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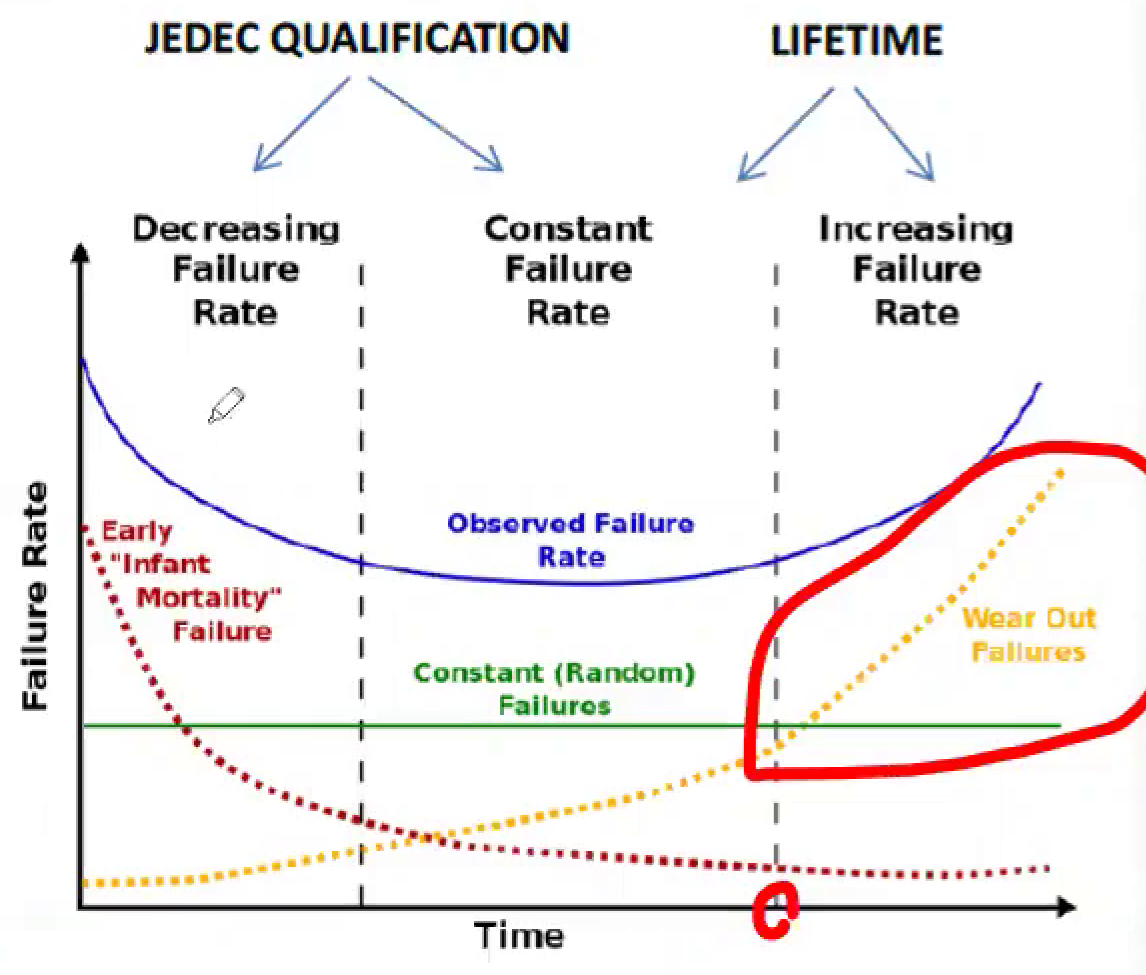

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JEP180.01之實戰演例

Table 1. JEDEC qualification test results for Transphorm's products

Test	Symbol	Conditions	Sample	Pass Criteria
High Temperature Reverse Bias	HTRB	TJ=150°C VDS = 480V 1000 Hrs	3 lots 77 parts per lot 231 total parts	0 Fails
Highly Accelerated Temp and Humidity Test	HAST	130°C 85% RH 33.3 PSI Bias = 100V 96 Hrs	3 lots 77 parts per lot 231 total parts	0 Fails
Temperature Cycle	TC	-55°C / 150°C 2 Cycles / HR 1000 Cycles	3 lots 77 parts per lot 231 total parts	0 Fails
Power Cycle	PC	25°C / 150°C ΔT = 100°C 7500 Cycles	3 lots 77 parts per lot 231 total parts	0 Fails
High Temperature Storage Life	HTSL	150°C 1000 Hrs	3 lots 77 parts per lot 231 total parts	0 Fails

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HTRB: High Temperature Reverse Bias

- 但我們卻沒有**10年**可以等啊!所以加熱加电壓**加速**測試 (HTRB)
  - 加熱(125C-150C)
  - 加电壓(指的是加高电壓Vds，而Vgs必須為零)，
  - 看的是GaN元件漏电流的澡盆曲線(如右图所示)

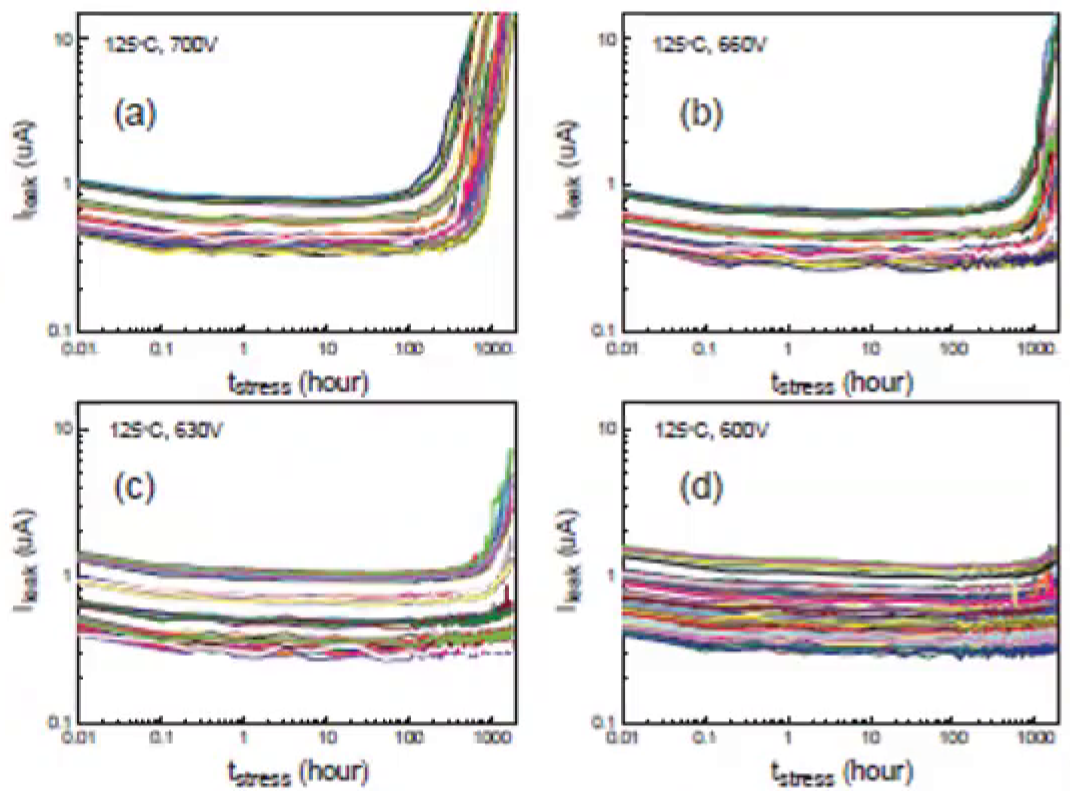
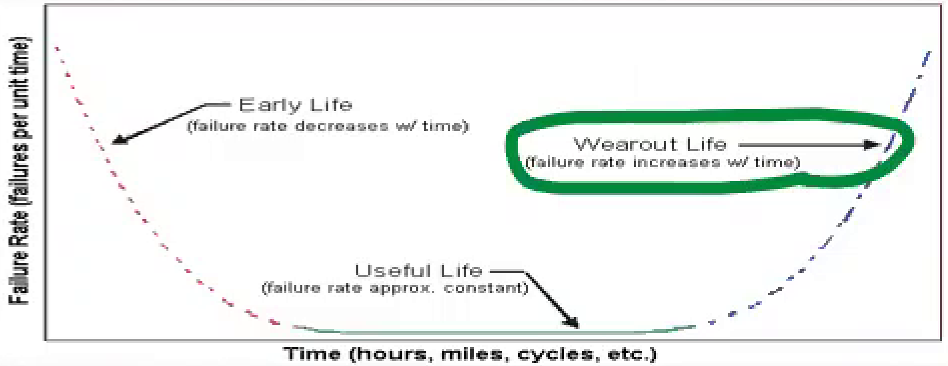


Fig. 2: OFF-state (V_{GS}=0V) drain leakage current of HD-GIT at V_{DS} of 600V (I_{leak}) as a function of the total stress time t_{stress}. The stress bias voltage: (a) V_{DS}=700V, (b) V_{DS}=660V (c) V_{DS}=630V, and (d) V_{DS}=600V.



K. Tanaka et al., "Reliability of hybrid-drain-embedded gate injection transistor," IRPS'17, pp. 4B-2.1-4B-2.10,

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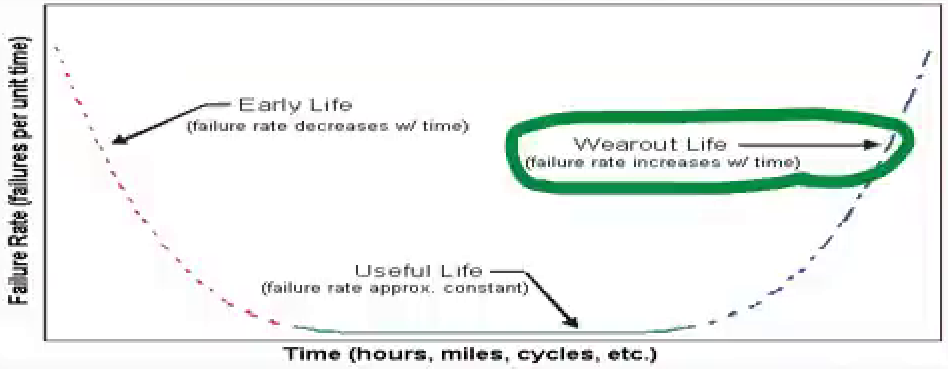

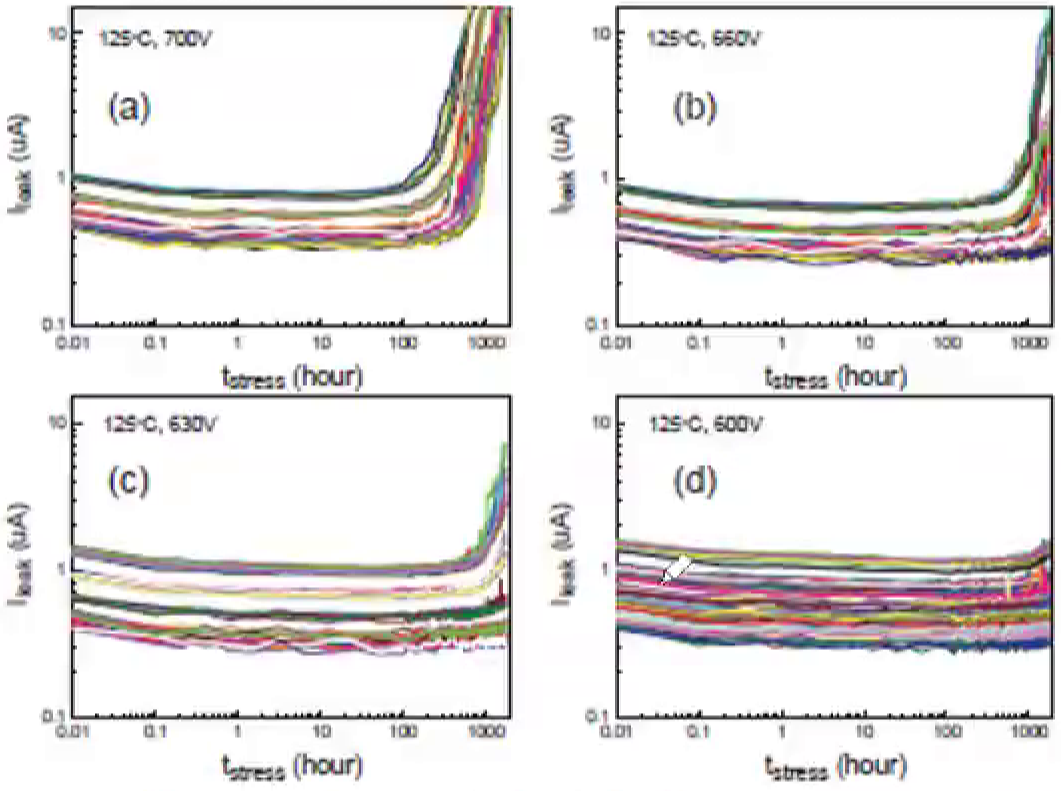

Fig. 2: OFF-state (V_{GS}=0V) drain leakage current of HD-GIT at V_{DS} of 600V (I_{leak}) as a function of the total stress time t_{stress}. The stress bias voltage: (a) V_{DS}=700V, (b) V_{DS}=660V (c) V_{DS}=630V, and (d) V_{DS}=600V.

K. Tanaka et al., "Reliability of hybrid-drain-embedded gate injection transistor," IRPS'17, pp. 4B-2.1-4B-2.10,

JEP180.01夠不夠勁?

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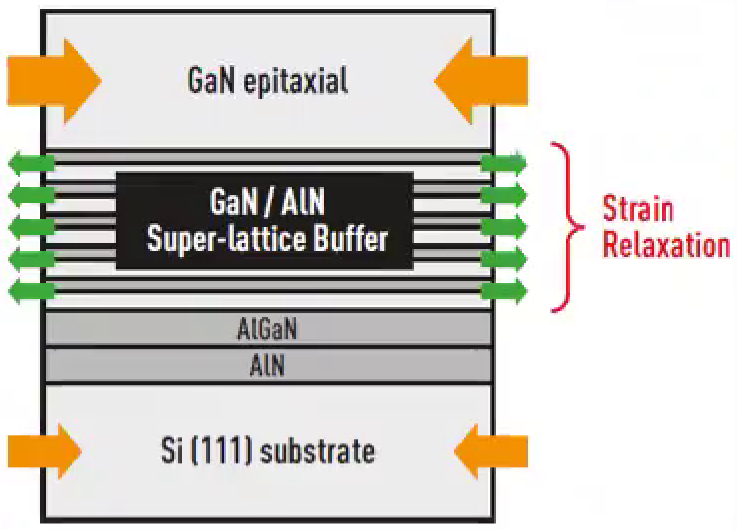

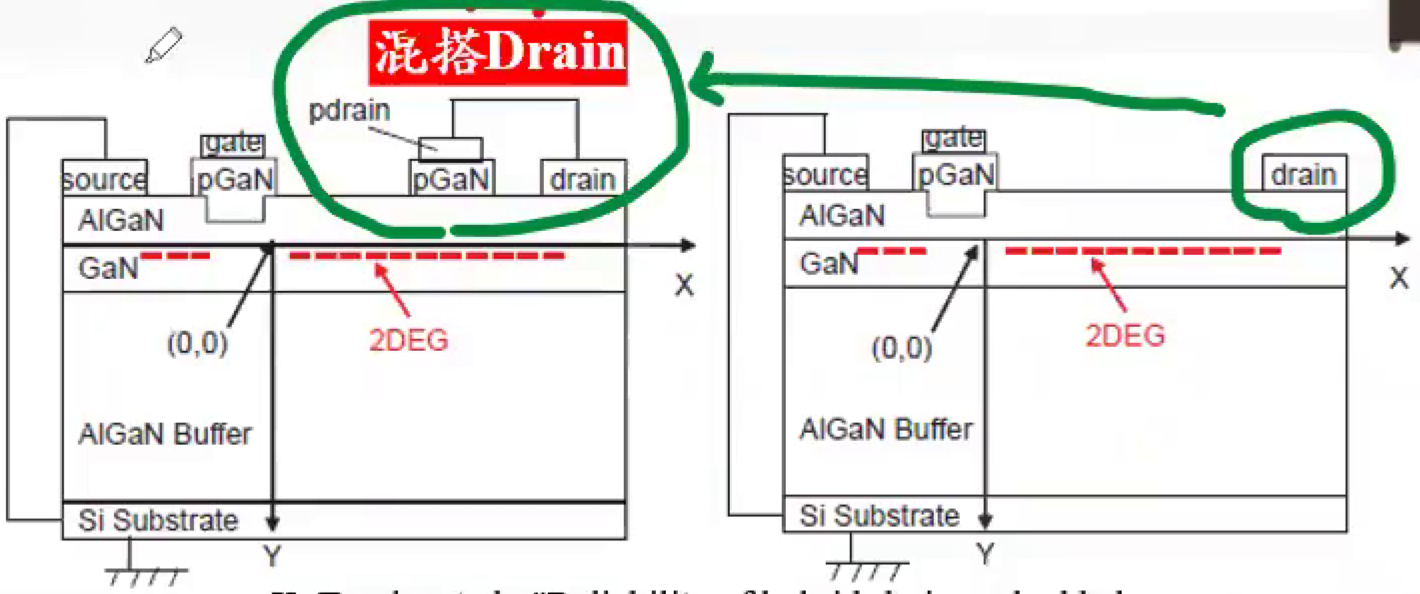

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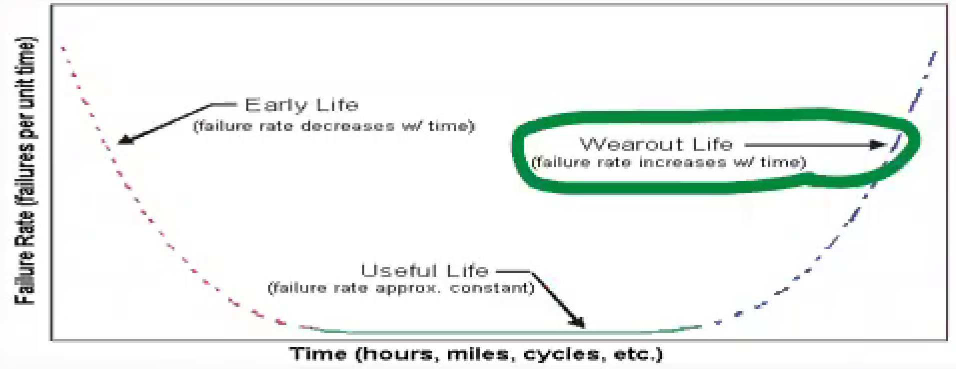
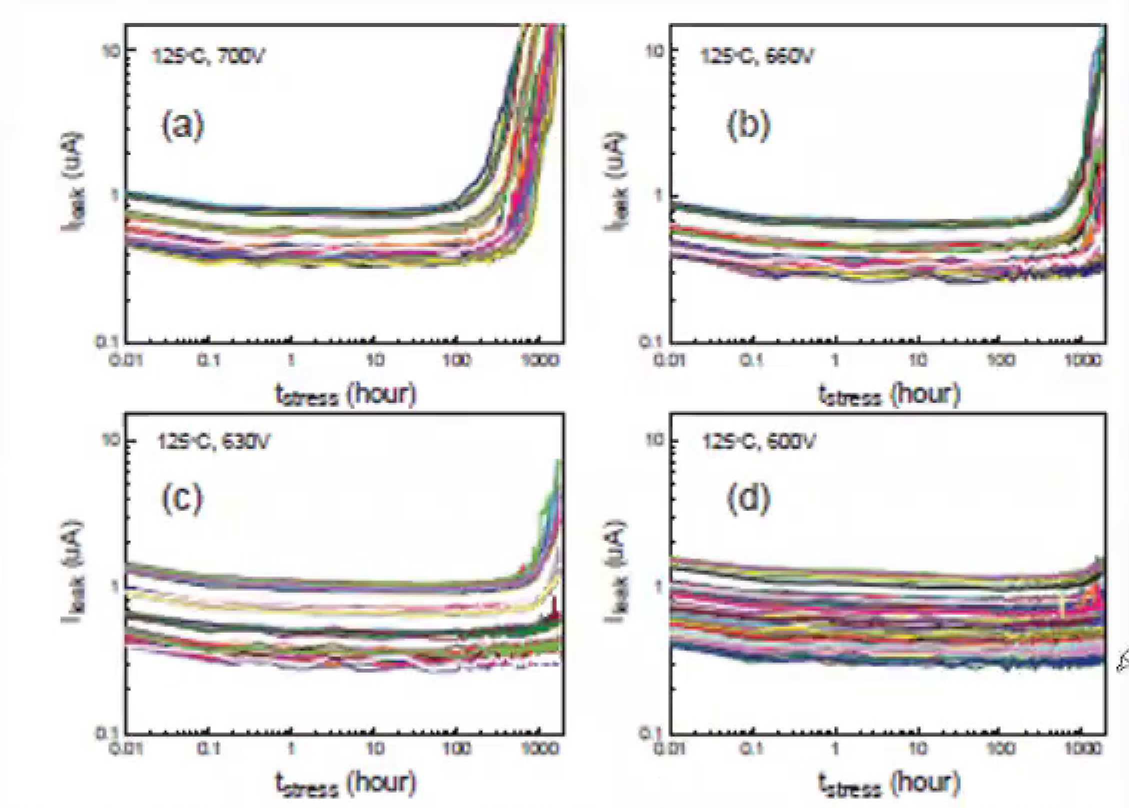
https://eu.industrial.panasonic.com/sites/default/pidseu/files/pan_18047_whitepaper_gan_web.pdf

HTRB: High Temperature Reverse Bias

- 但我們卻沒有**10年**可以等啊!所以加熱加电壓**加速**測試 (HTRB)
  - 加熱(125C-150C)
  - 加电壓(指的是加高电壓Vds，而Vgs必須為零)，
  - 看的是GaN元件漏电流的澡盆曲線(如右图所示)





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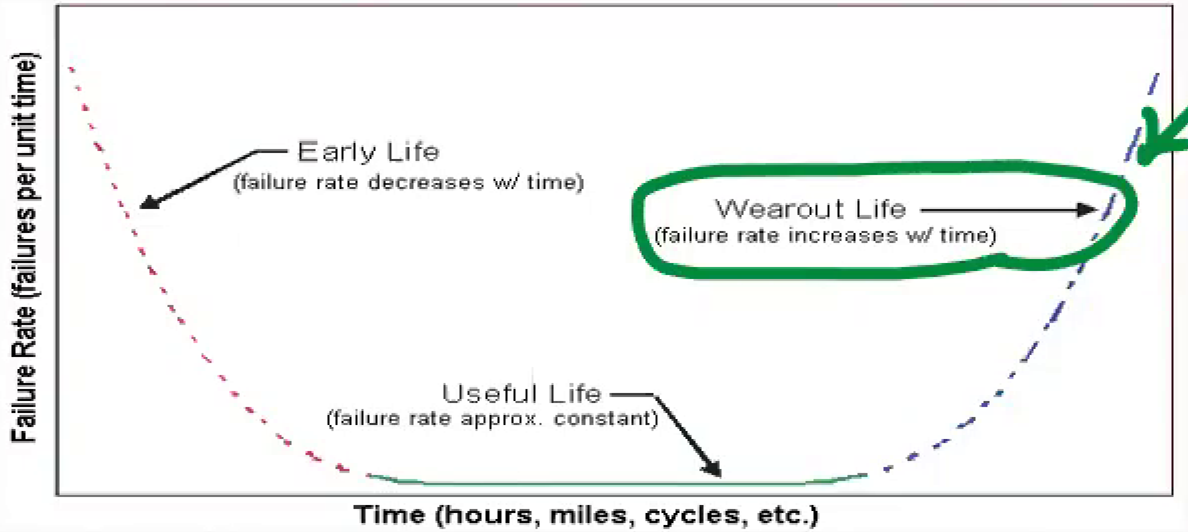
Hybrid-Drain GiT的歪伯分布

- 歪伯分析發現，其β (= m) >> 1，此明顯的是wear out (叫做慢慢累死，乃正常的現象，沒有surprise，好耶!)



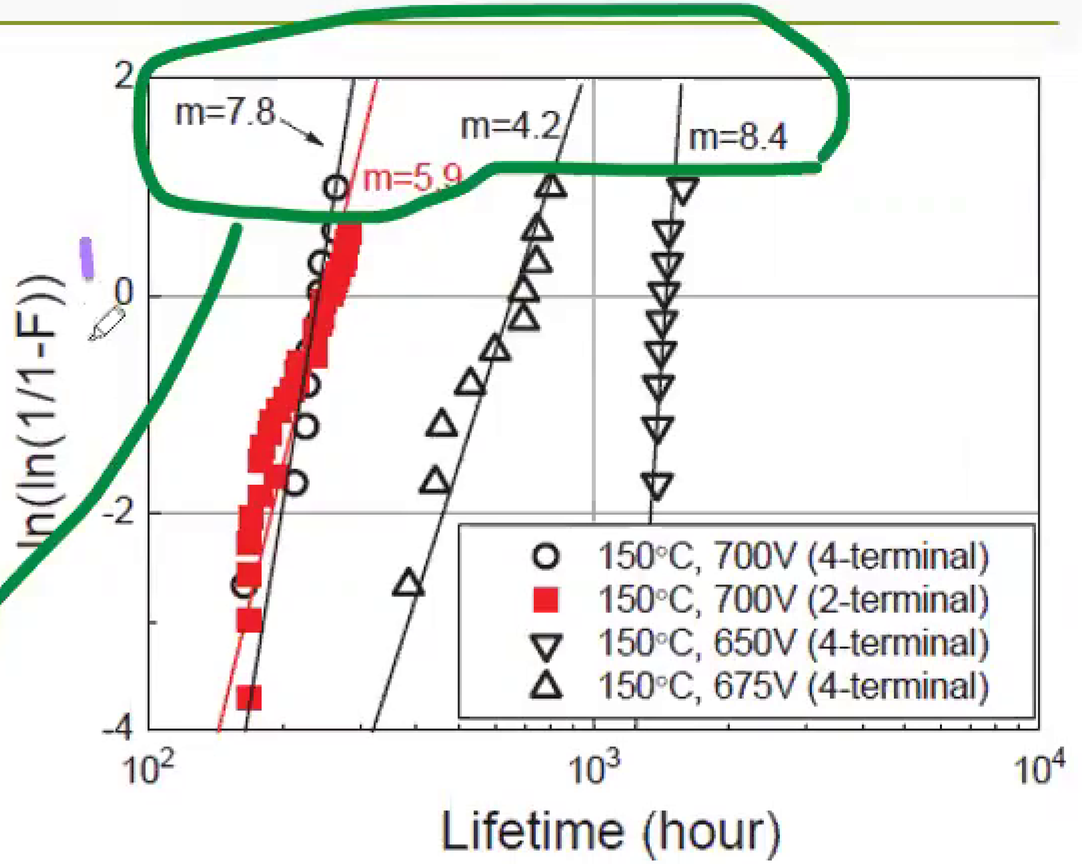


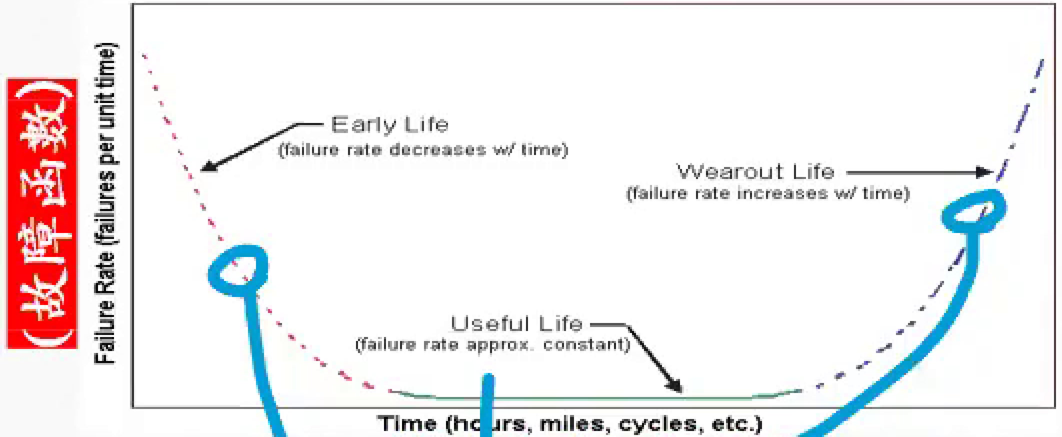
Fig. 4: Weibull plot under stress voltage in the 4- and 2-terminal configurations at 150°C.

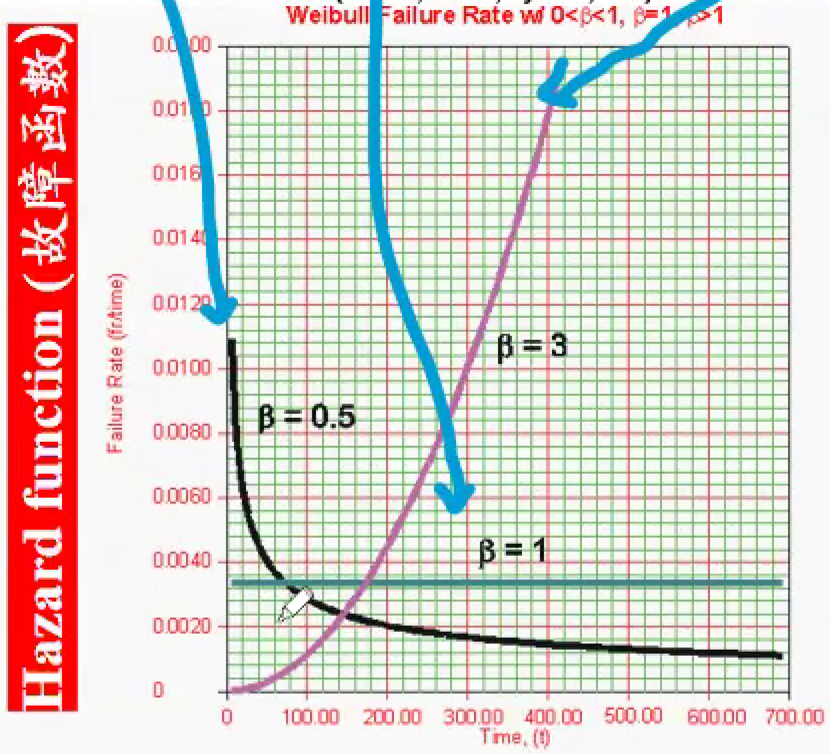
K. Tanaka et al., "Reliability of hybrid-drain-embedded gate injection transistor," IRPS'17, pp. 4B-2.1-4B-2.10,

歪伯愛洗澡: 产品可靠性澡盆曲线

Weibull Distribution:可靠性分析很給力

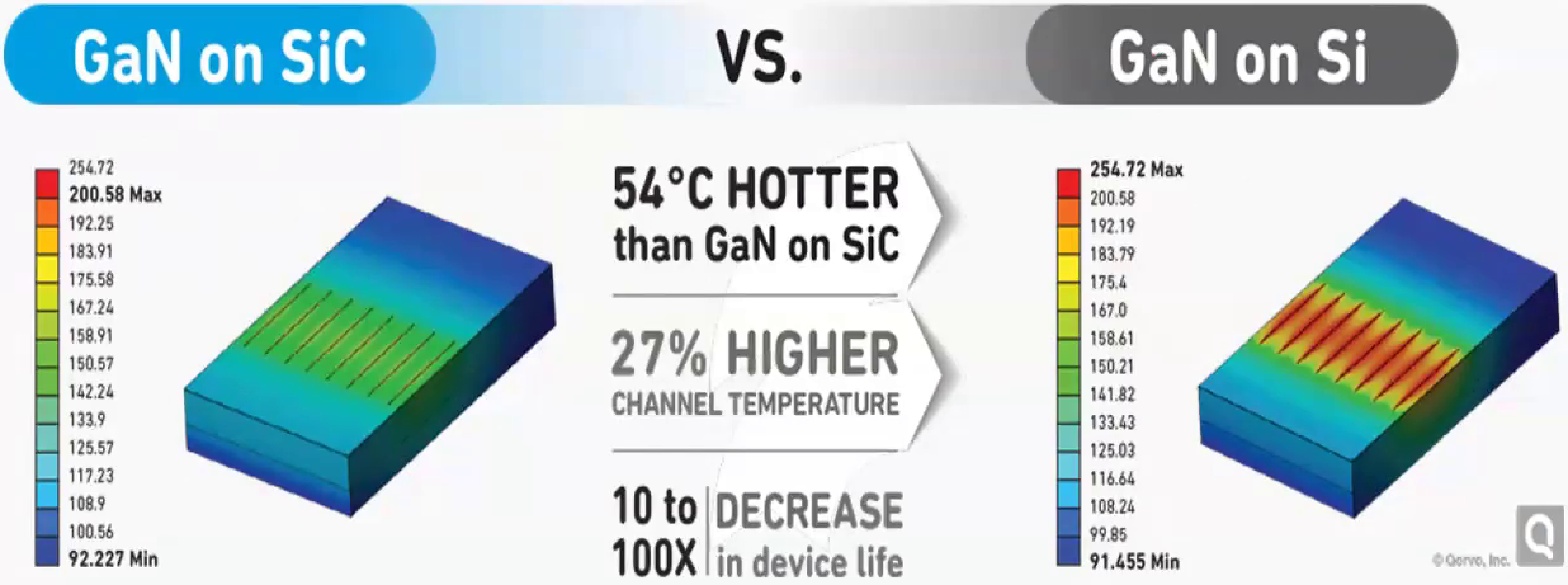
- 所屬PDF (probability density distribution)
  - $f(T) = \frac{\beta}{\eta}\left(\frac{T-\gamma}{\eta}\right)^{\beta-1} e^{-\left(\frac{T-\gamma}{\eta}\right)^{\beta}}$
    - β = shape parameter (形狀參數)
    - η = scale parameter (比例參數)
    - γ = location parameter (thresh in Minitab)
- 歪伯厲害的地方就是用他以他發明的概率密度函數(PDF)推导出適當的故障函數，竟能解釋产品可靠性澡盆曲线所有部分





https://www.weibull.com/hotwire/issue14/relbasics14.htm

GaN on SiC更可靠，當然也更貴了



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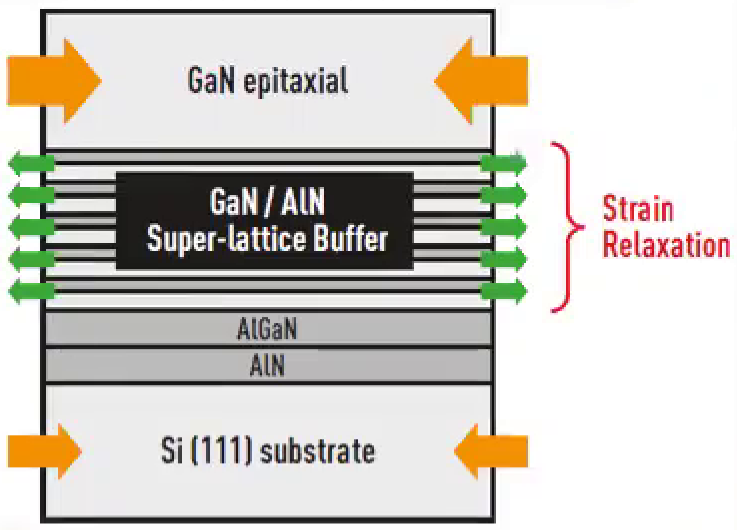

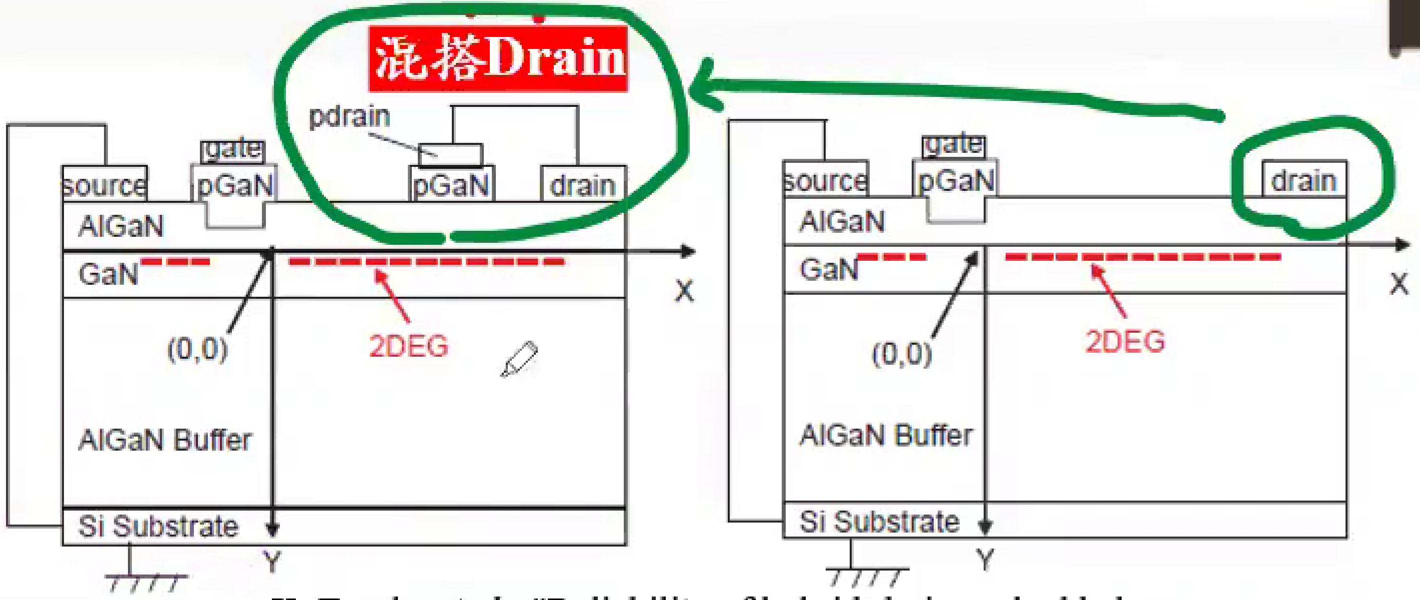

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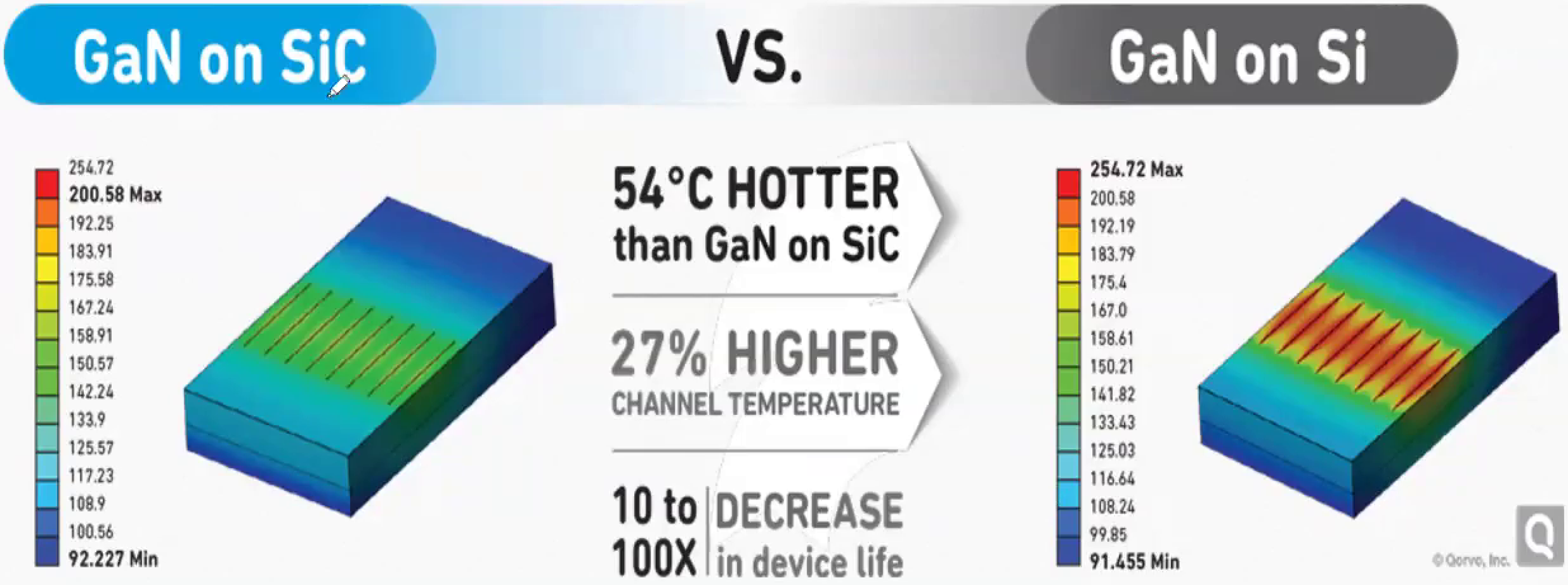

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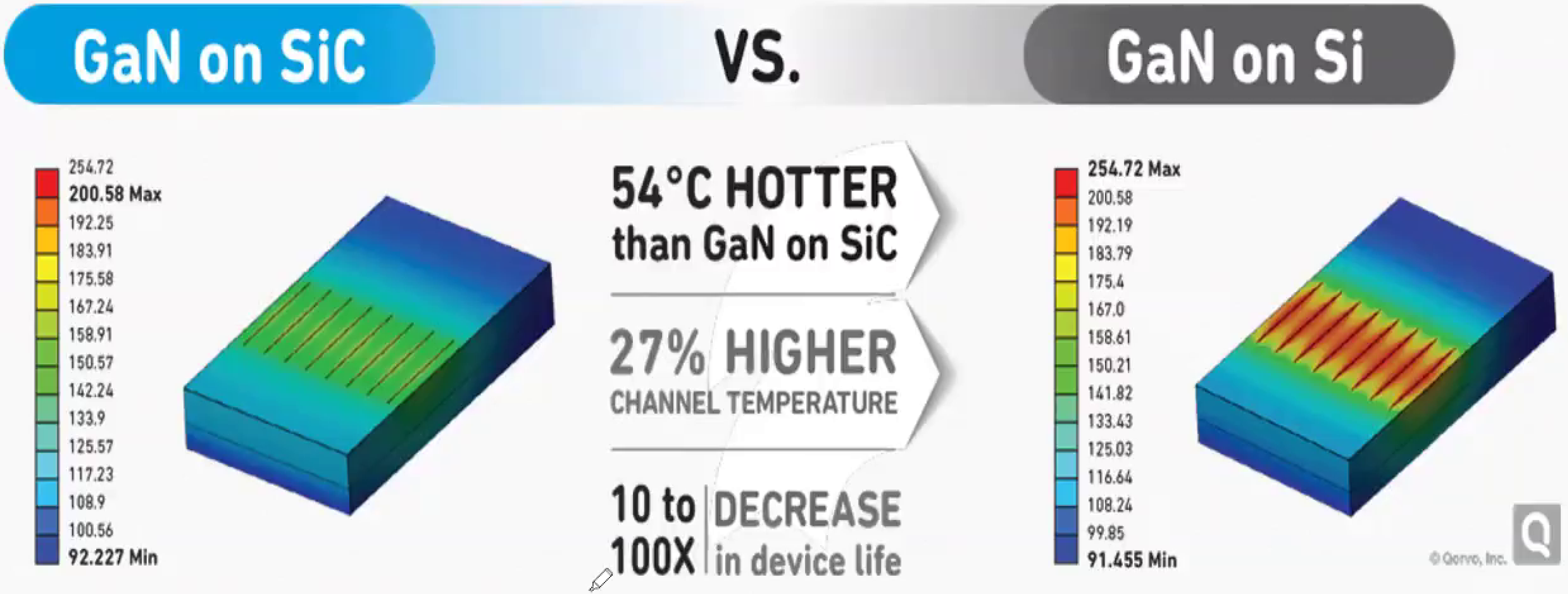

https://cn.qorvo.com/

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_GaN可靠嗎?找歪伯理論

Reliability of GaN Power Devices

王不老說半导