芯片良率難搞篇
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HKIL

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王不老說半导

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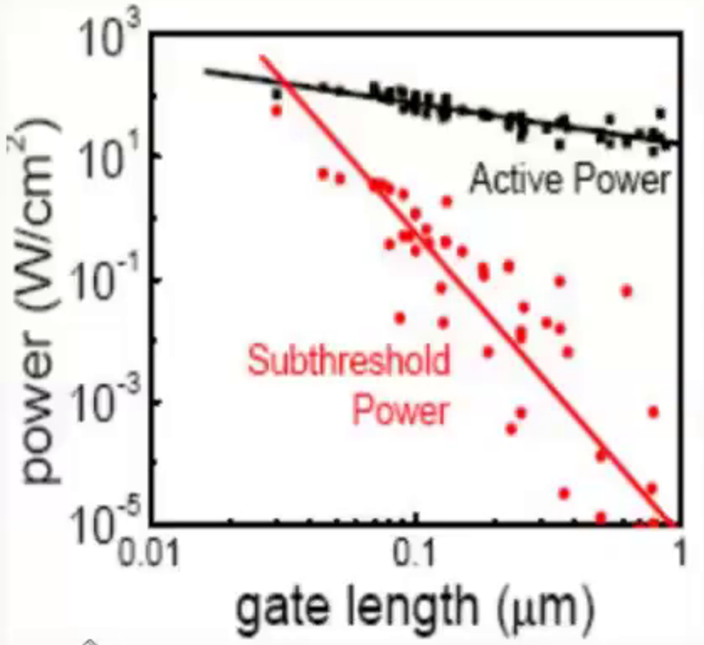
静态漏电所佔比例已經越來越不像話



Source: IBM, T.C. Chen, ISSCC 2006

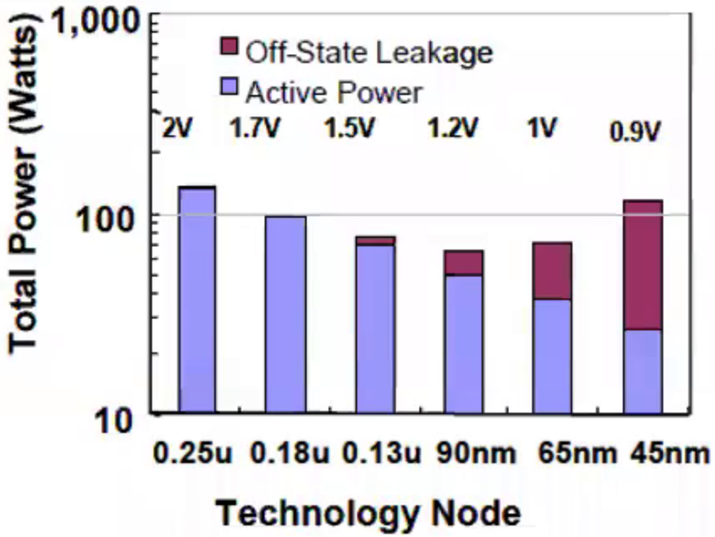
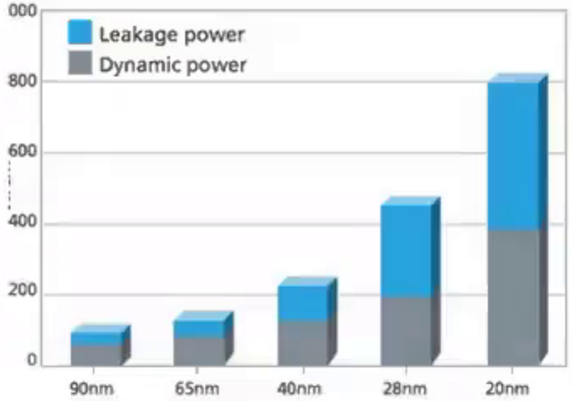


Figure 20: Total power as a function of technology node, for a fixed (30m) total transistor width, showing the increasing importance of off-state current as technology scales

Transistor Elements for 30nm Physical Gate Lengths and Beyond, Brian Doyle, Intel Technology Journal Vol. 6 Issue 2,



Source: IBS

所以减少漏电已經比增加速度更重要了

Intel Gate Leakage data

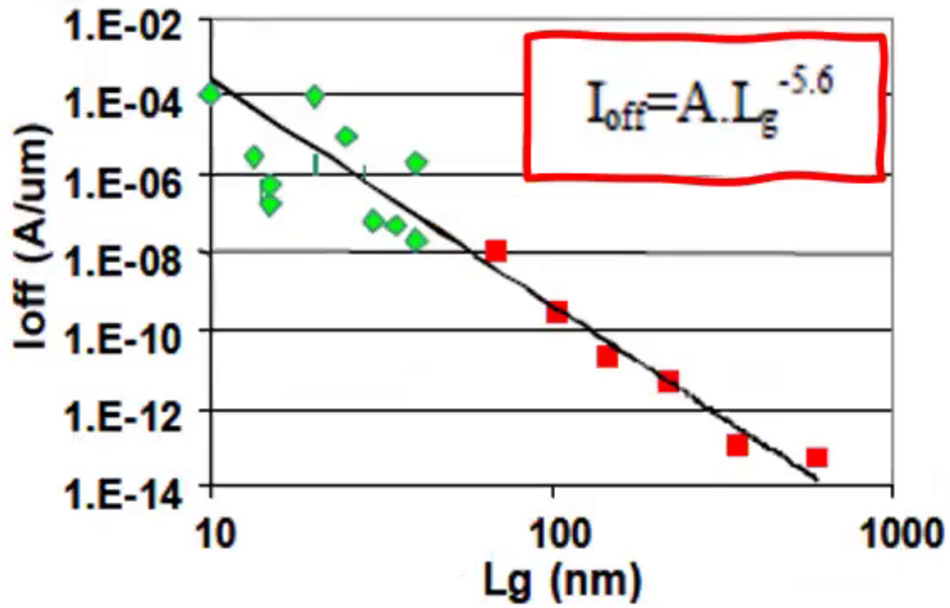


Figure 19: Transistor off-state leakage vs gate length
Red squares indicate pre-production transistors
Green diamonds indicate research devices

Transistor Elements for 30nm Physical Gate Lengths and Beyond, Brian Doyle et al. , Intel

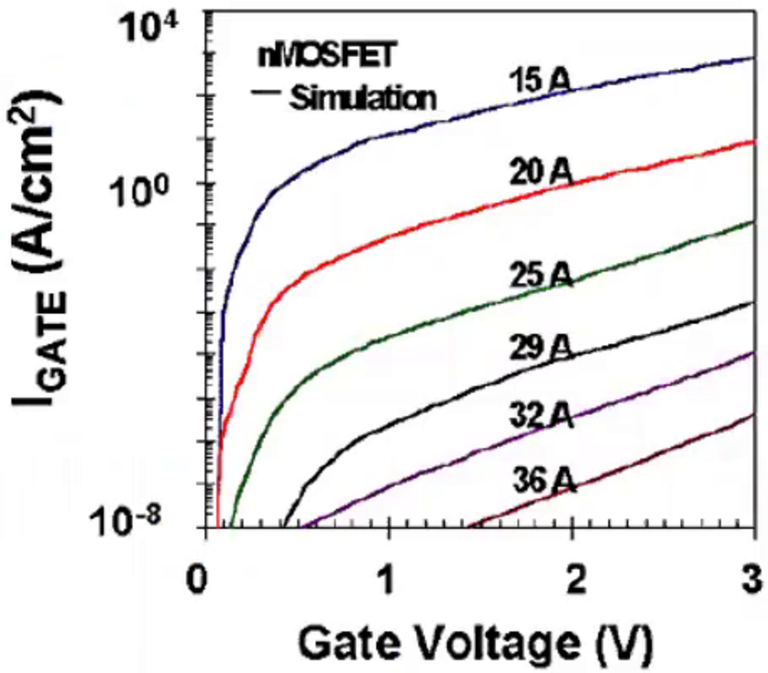


Figure 5 Gate leakage vs. oxide thickness and voltage

Test Challenges in Nanometer Technologies,
Sandip Kundu et al., Intel

HfO_2確能大幅降漏電

HKIL = HfO_2 (HK) + SiOx (IL)

- HfO_2的實際厚度 = 1.5-2.5nm (nominal ~ 2nm)，大幅降漏電5-6數量級，其中IL SiOx (IL)真實厚度 = 0.6-1nm (nominal ~ 0.8nm)
  - EOT = $t_{HfO_2}\frac{k_{SiO_2}}{k_{HfO_2}} \sim t_{HfO_2}\frac{3.9}{15}$
  - EOT(2nmHK) = $20\frac{3.9}{15} \sim 5$Å
- 意思是說，實際2nm (k=15) HfO_2的厚度，其實等於~0.5nm的SiO_2電容厚度

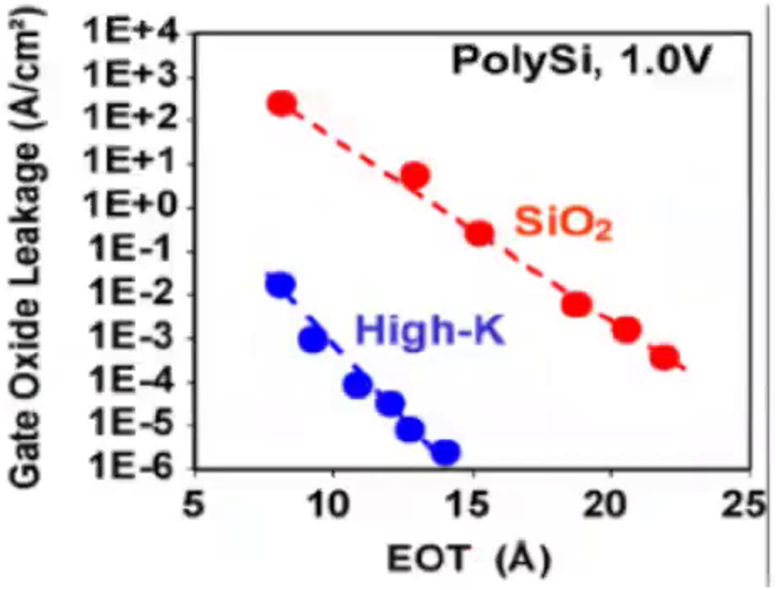


Figure 18: Comparison of gate leakage between SiO_2 and high-K dielectrics

Transistor Elements for 30nm Physical Gate Lengths and Beyond，Brian Doyle， et al.

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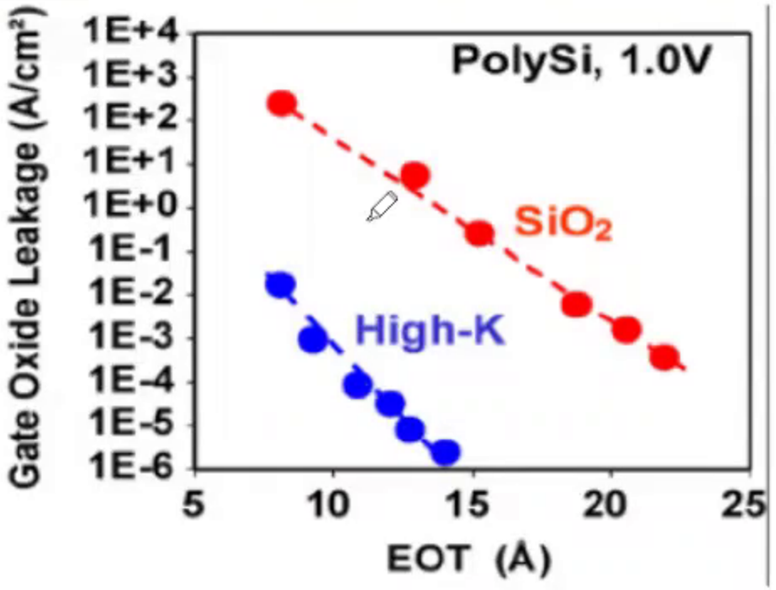

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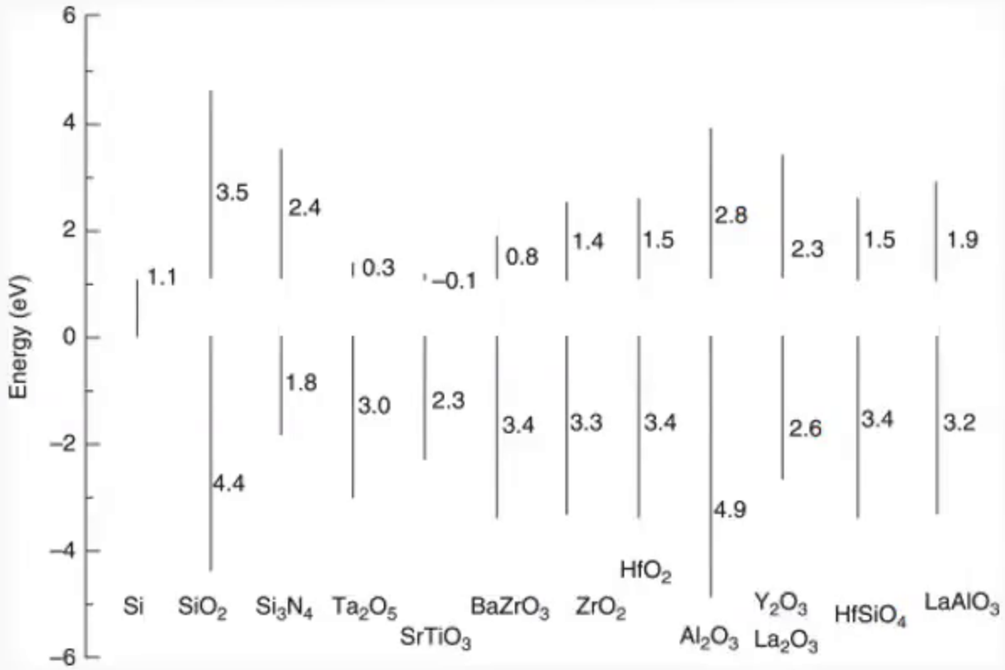

P.R. Berger, A. Ramesh, in Comprehensive Semiconductor Science and Technology, 2011

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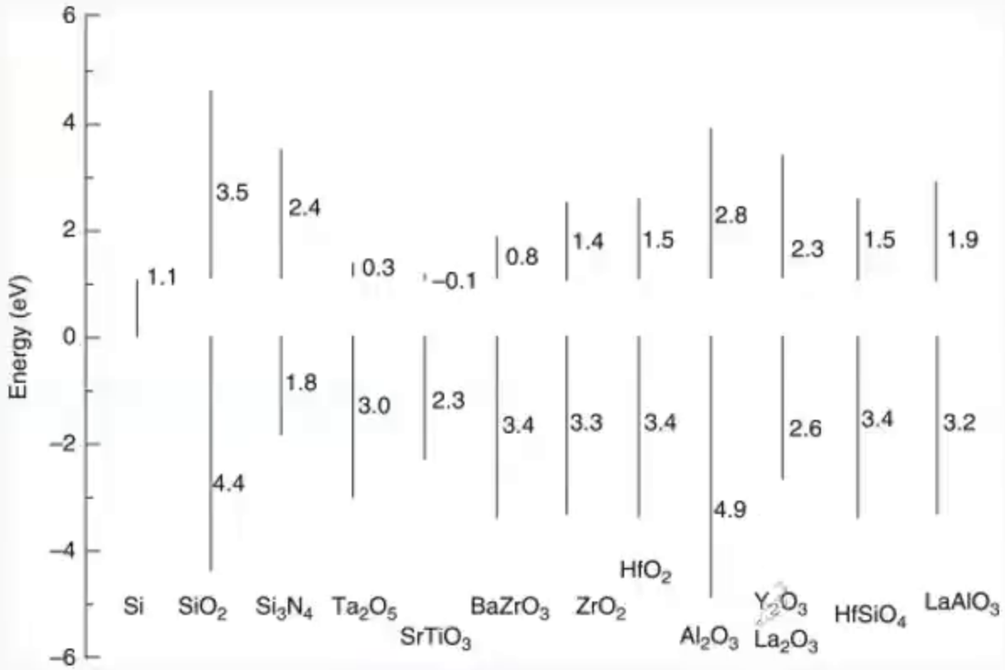
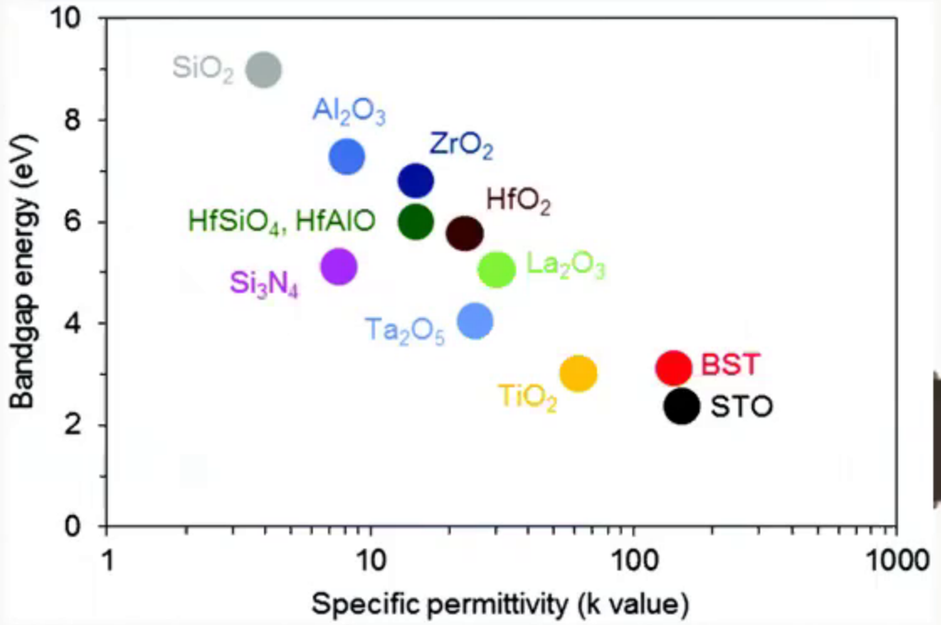


P.R. Berger, A. Ramesh, in Comprehensive Semiconductor Science and Technology, 2011

為何只HK有HfO_2能雀屏中選?

- 增加絕緣材料的厚度是減少漏電的最佳方法，但是電容卻不能減少，所以只有選擇某high k，
- HfO_2中選原因很多，例如他與SiOx如同水油不相容(immiscible)是優點，若相容則其各自的天生缺陷必因相容而相加，必大幅增加可靠性(reliability)的困難度
- HfO_2 K值15-20之間(amorphous)，雖不高，還夠用



J. Mater. Chem. C, 2017, **5**, 8000-8013

HKIL內部缺陷的細部分解

- 世界上所有材料皆有天生的缺陷，右圖所示為HKIL的內部缺陷圖
- 這些缺陷對載子(电子與电洞)有強烈吸引力，載子臉皮薄竟受其影響，飄移速度減慢，電流減少，壞了大事
- 缺陷還會因為芯片使用自動增加(材料勞損)，最後導致硅芯片無法正常工作(臨界電壓改變太多)
- 這些缺陷可用許多方法減少(但要 < $10^{10\text{-}11}/cm^2$)，目前只有HfO_2 + SiOx的搭配才能真正降得下來，而且穩定多年(Intel前後共花了15年才做出來)

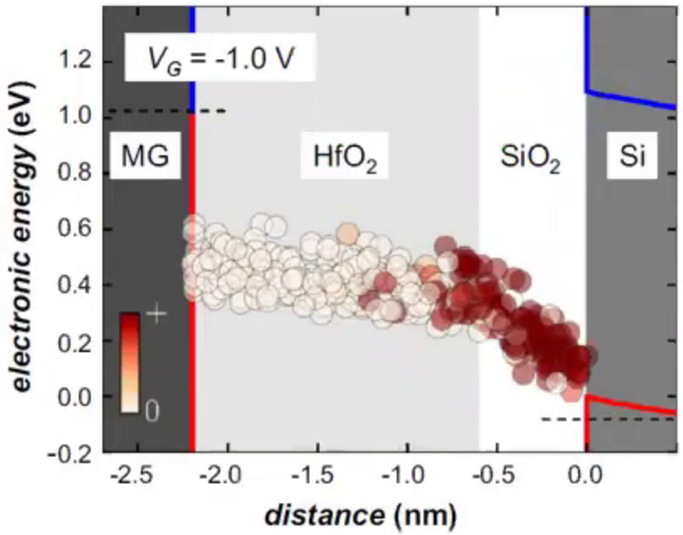


Fig. 5. A simulation of pFET device with a high-k/metal gate stack assuming a defect band. Large-area device is simulated to obtain average behavior. Capture and emission to/from both the substrate and the gate are considered [35,36].

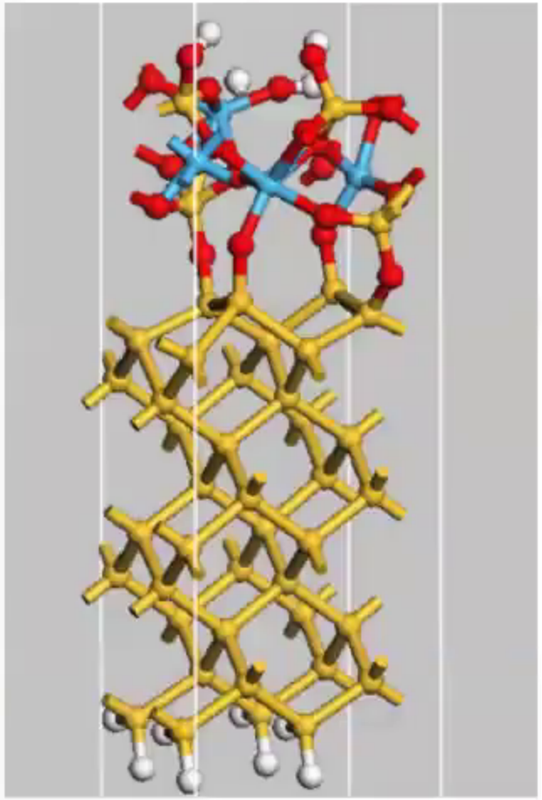
The defect-centric perspective of device and circuit reliability—From gate oxide defects to circuits，B. Kaczer，Solid-State Electronics 125 (2016) 52–62

HK(HfO_2)的缺點需要SiOx彌補

HKIL = HfO2 (HK) + SiOx (IL)

- 若HK沒有IL的保護，硅芯片基本上將死於pFET的可靠性(NBTI)不足身上
- 剛剛形成IL(SiOx)的厚度與晶格表面有關，(100)上的約為0.8-1nm，然而在(110)上的要更厚一些，將SiOx變薄可是一門大學問，但也不能太薄，理論上SiOx只能薄到0.4nm (to be defect free，如右圖所示)
- 太薄也讓SiOx失去對HK的保護效果，电洞因此可見到HK內部缺陷，竟然走不動路了

PHYSICAL REVIEW B 75, 245304 (2007)



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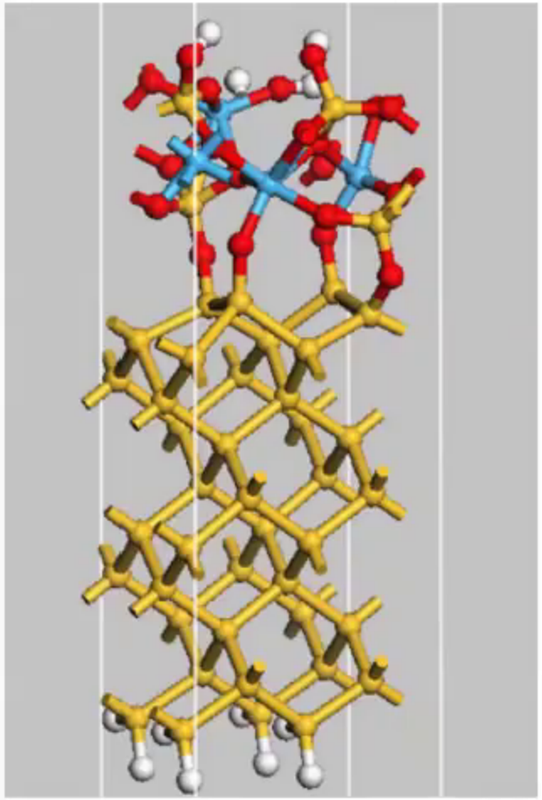
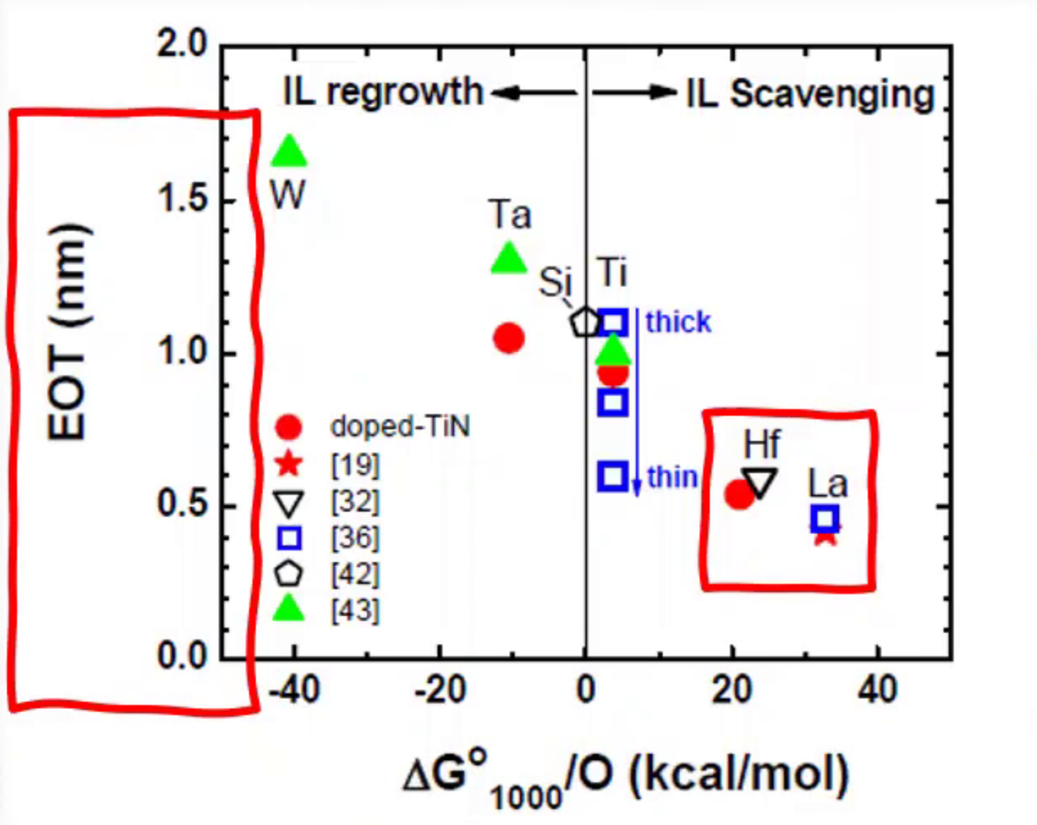


調整IL厚度的方法: IL scavenging

- IBM(T. Ando)證實可調整IL的厚度
- 將超愛吃氧的(Hf and La等)放在HK(HFO_2)的上方，經然可用“隔山打牛”方式，強行掠奪(scavenging) HK下面可憐瘦弱(<1nm)的IL裡面的氧，使它變薄(有夠殘忍)
- **此日: IL scavenging**

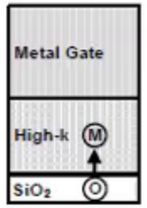
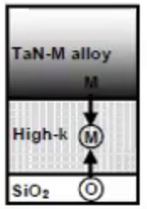
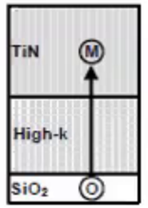


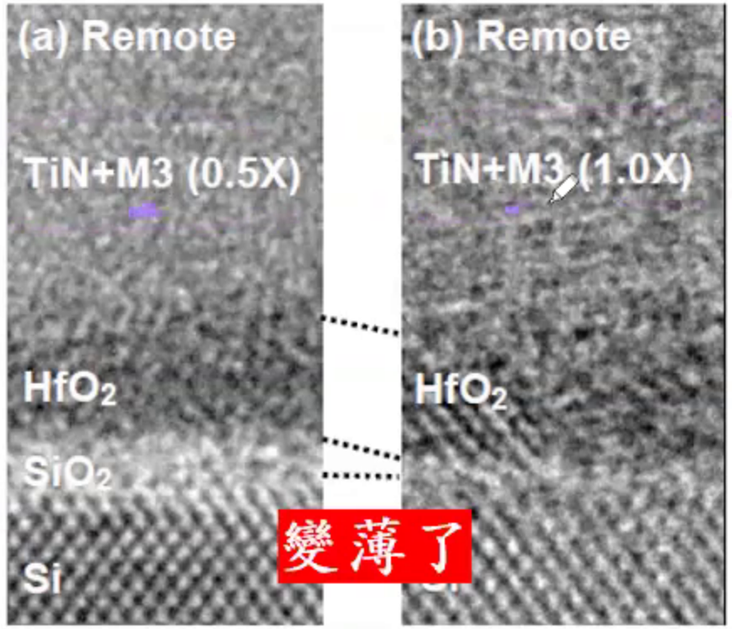
Ultimate Scaling of High-κ Gate Dielectrics: Higher-κ or Interfacial Layer Scavenging? Materials 2012, 5, 478-500; T. Ando

IL scavenging = “隔山打牛”神功?

- 如右圖所示，HK下面可憐瘦弱(<1nm)的IL裡面的氧，好像誰都可依欺負她，硬搶她體內的氧，使它變薄(因為SiOx → Si)
- 此制程曰之"IL Scavenging“

Figure 3. Schematics of direct- and remote- scavenging techniques in the literature.

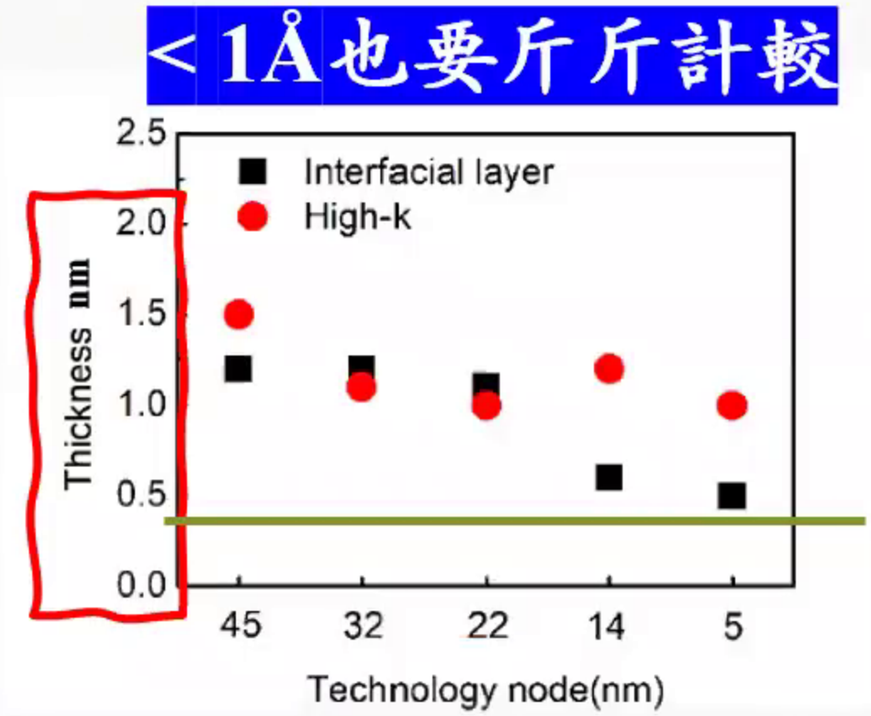
Type	Direct		Remote
Scavenging element (M)	Within High-k		Isolated from High-k
Schematics			
Ref.	[29, 30, 32]	[33]	[19, 35]



Ultimate Scaling of High-κ Gate Dielectrics: Higher-κ or Interfacial Layer Scavenging? Materials 2012, 5, 478-500; T. Ando

附錄: Si Fin (110) → ~1.34nm SiO_xH_y (110)

- 右圖所示，IL(SiO_xH_y)可是越來越薄(HK厚度卻不動如山)
- SiOxHy的增加直接增加EOT(→CET)，而且是1:1的比例，每1Å約相當於10%CET(or Tinv)，也就是可能影響近~10%電流也
  - 註: 1nm CET = 3.4μF/cm²
- 理論上，FinFET的 sidewall native oxide (SiO_xH_y) 太厚，所以必須優化變薄一些，但卻也不能太薄



State of the Art and Future Perspectives in Advanced CMOS Technology, Henry H. Radamson, *Nanomaterials* 2020, *10*(8), 1555

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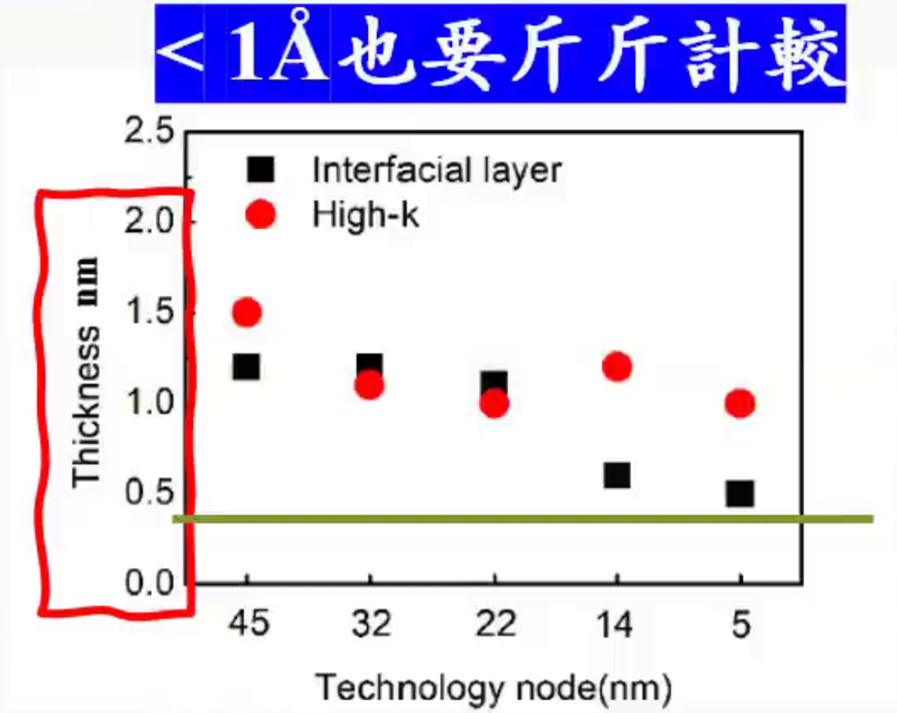
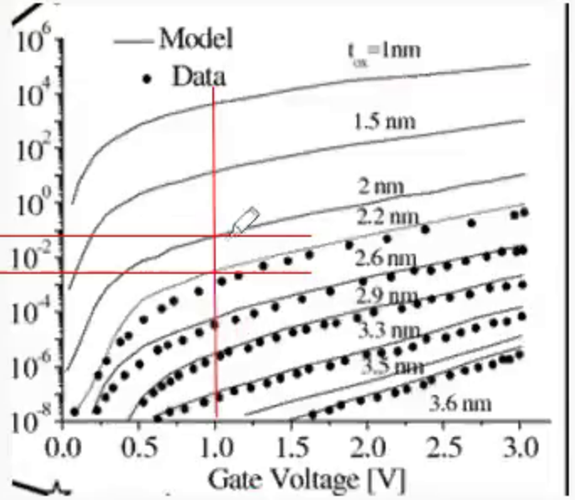


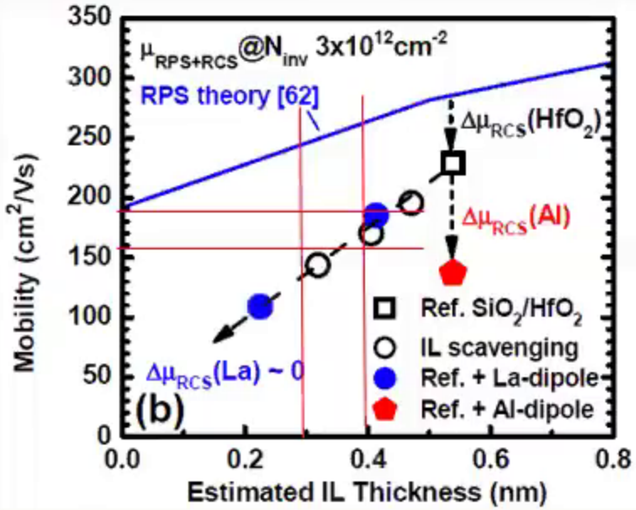
State of the Art and Future Perspectives in Advanced CMOS Technology, Henry H. Radamson, *Nanomaterials* 2020, *10*(8), 1555

少了1Å 的 $SiH(O_3)$ IL又如何?

- **已知**:在先進的芯片製程(HKMG)中，HK = HfO_2，但其下須墊著一纳米厚天然的氫氧化合物$SiH(O_3)$ = 介面層(Interfacial layer or IL)
- **試問**: 若此介面層(IL)減少了1Å，芯片会受到多大的打击，請由漏电流(Ig)，電子遷移率(mobility，μ)度及可靠性(reliability)三方向簡單分析
- **解答**:
  1. 右上圖顯示，當IL降2Å時，漏电流(Ig)↑約十倍，
     → IL減少1Å，漏电流(Ig) ↑約3-5倍
  2. 右下圖顯示，當IL下降1Å時，電子遷移率(μ)↓15%
     - Note: 2020 TSMC claimed its N5 process offered 15% speed improvement over N7



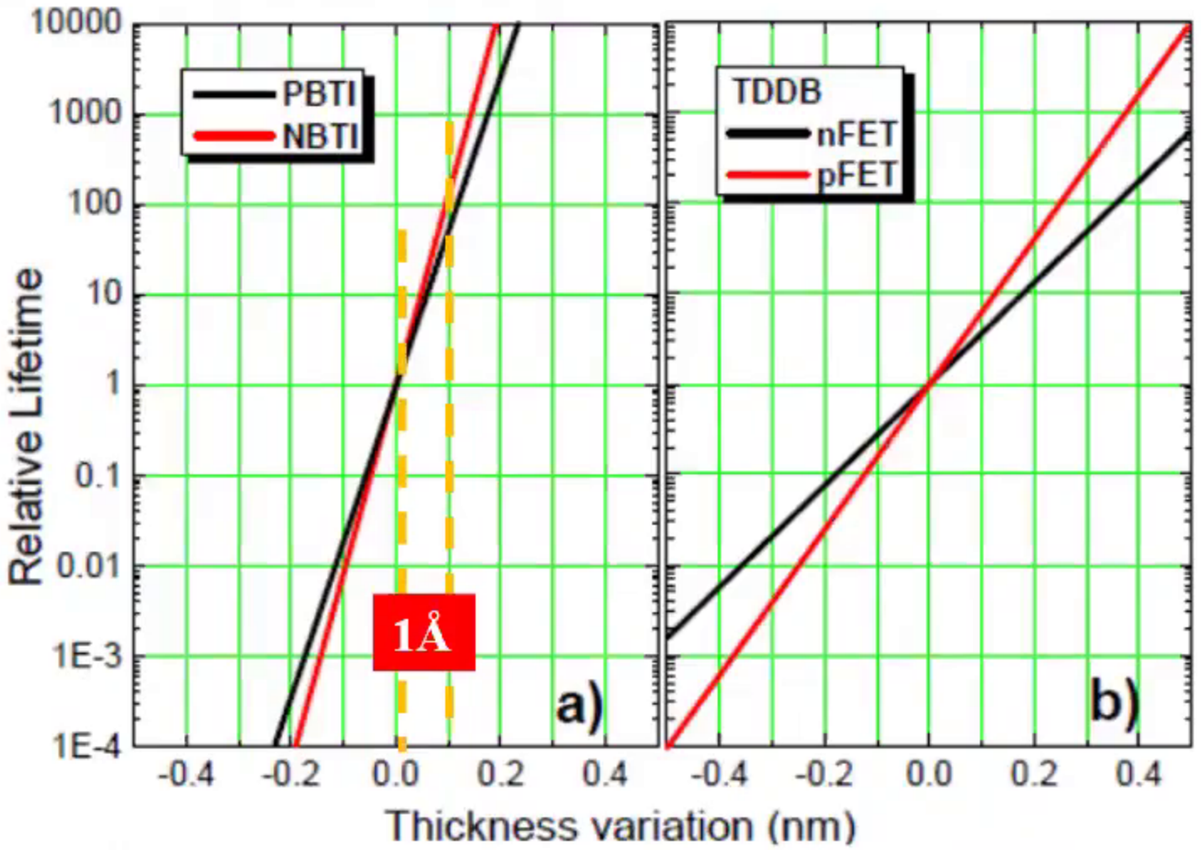
http://userweb.eng.gla.ac.uk/fikru.ada mu-lema/Chapter_02.pdf



Materials 2012, 5, 478-500; T. Ando

少了1Å 的 SiH(O_3) IL又如何?

- 解答:
  - 而且可靠性(reliability，or Lifetime)可能大幅下降～1-2數量級(見右圖)



Ultimate Scaling of High-κ Gate Dielectrics: Higher-κ or Interfacial Layer Scavenging? Materials 2012, 5, 478-500; T. Ando

IL竟是HK的遮羞布: BTI vs EOT

- EOT對硅芯片可靠性有決定性影響
  - EOT< 5Å, 竟彷彿變成透明，露出在其後醜陋的坑坑洼洼HK嘴臉，活活嚇死膽小的电洞載子，此曰見光死，有Medusa的味道
  - NBTI(for pFET)在EOT~5Å時 lifetime = 0→ 即刻死亡
  - 原來，IL竟是HK的遮羞布
  - EOT~7-8Å，可靠性OK，但是電容卻會減少(電流會下降)，EOT優化是HKIL的重要課題

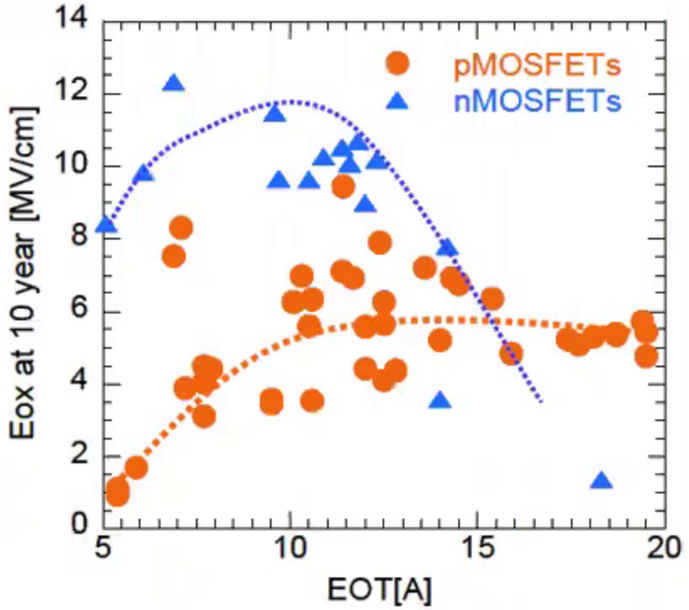
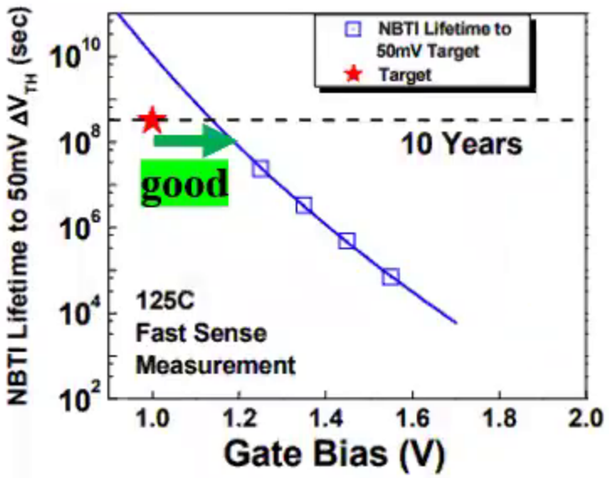


Figure 10. Electric field at 10 years after P/NBTI vs EOT. Considering *iso*-electric field can decrease the concern.

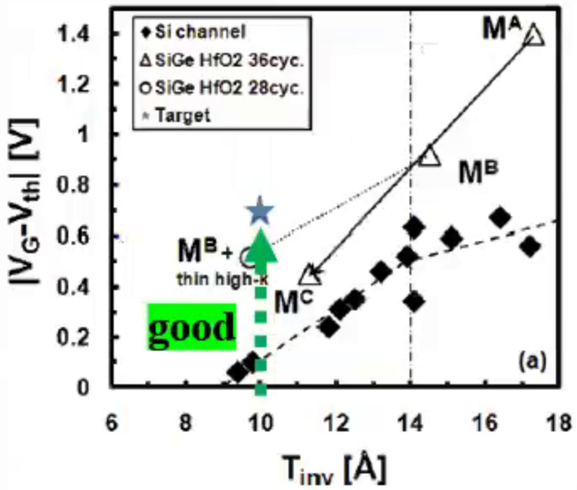
POSITIVE AND NEGATIVE BIAS TEMPERATURE INSTABILITY ON SUB-NANOMETER EOT HIGH-K MOSFETS， Moonju Cho, imec， IRPS10-1095

鍺來救命: NBTI vs EOT

- 右圖顯示，Tinv = 9-10Å (EOT = 5-6Å)時，(V_G-V_{th} = 0，也是指life time~0)，可靠性～0
- 但若以硅鍺為新材料(SiGe channel)，則可靠性(NBTI)可如火箭般上升
  - IBM/IMEC 研發結果證實如右
- 據稱TSMC 5nm pFET 就是用SiGe channel (Samsung/Intel 並沒有如是說)



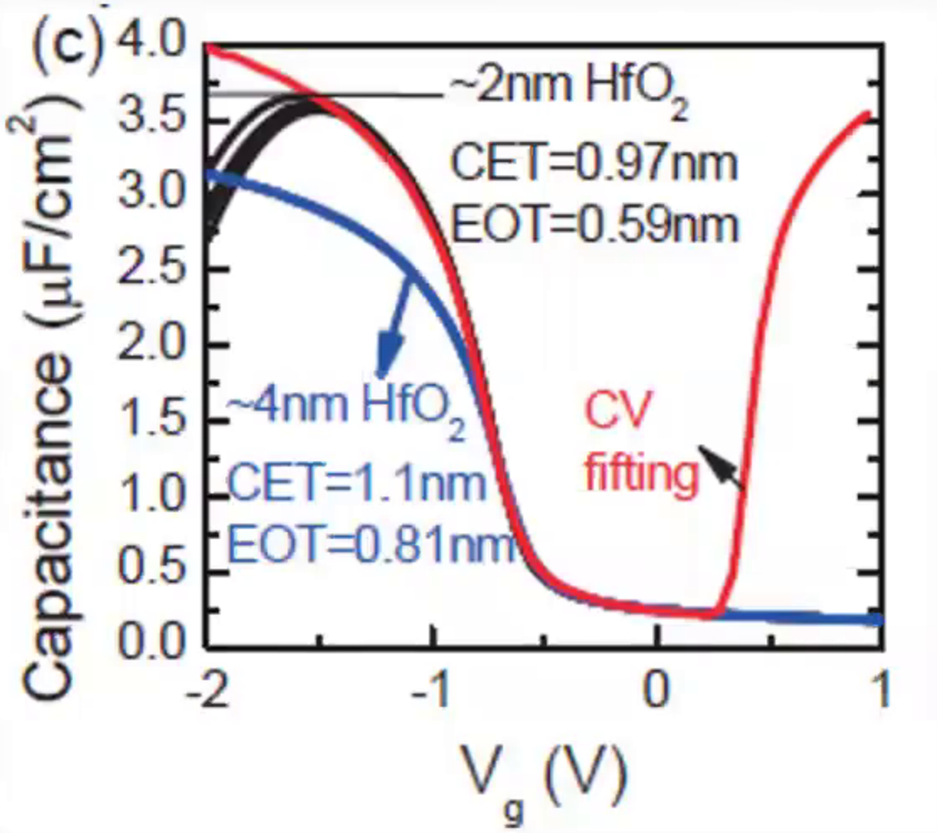
S. Krishnan (IBM) IEDM'11



6Å EOT $Si_{0.45}Ge_{0.55}$ pMOSFET with Optimized Reliability (V_{DD}=1V): Meeting the NBTI Lifetime Target at Ultra-Thin EOT J. Franco et al, imec, IEDM'10

HKIL 整體电性厚度: T_{inv} = EOT + 4Å

- 就芯片運作电性而言，電容才是真正的考量，電容越大則電流越大，電容相對應的厚度叫做CET (capacitance equivalent thickness)
  - 反型層(inversion) 的CET曰之Tinv
- CET = 1nm 時的電容 = 3.4uF/cm2
- CET無法知道其組成(HK與IL)各自的厚度，必須用TEM查看並驗證
- 右圖中為例，CET (= 3.4/3.1)=1.1nnm
  - EOT of HKIL is obtained from TEM with an assumed k value of HfO_2



Gate First High-k/Metal Gate Stacks with Zero SiO_x Interface Achieving EOT=0.59nm for 16nm Application, J. Huang VLSI'09

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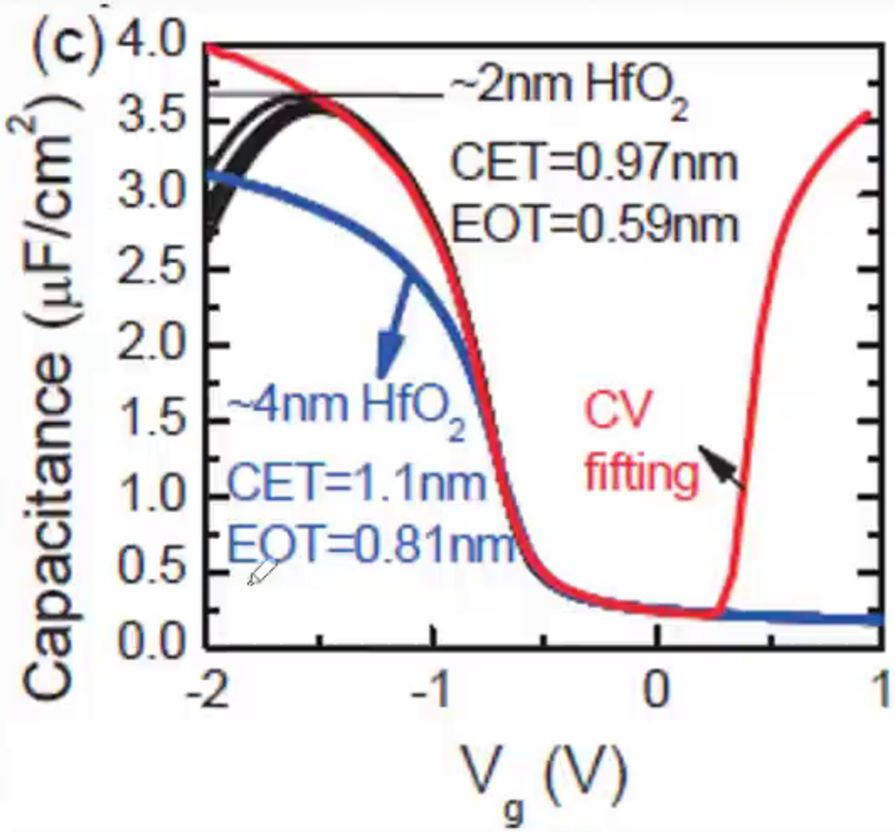
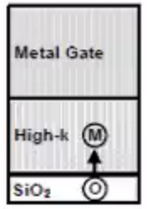
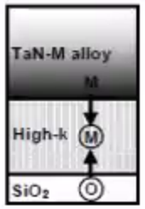
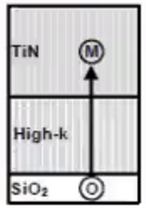


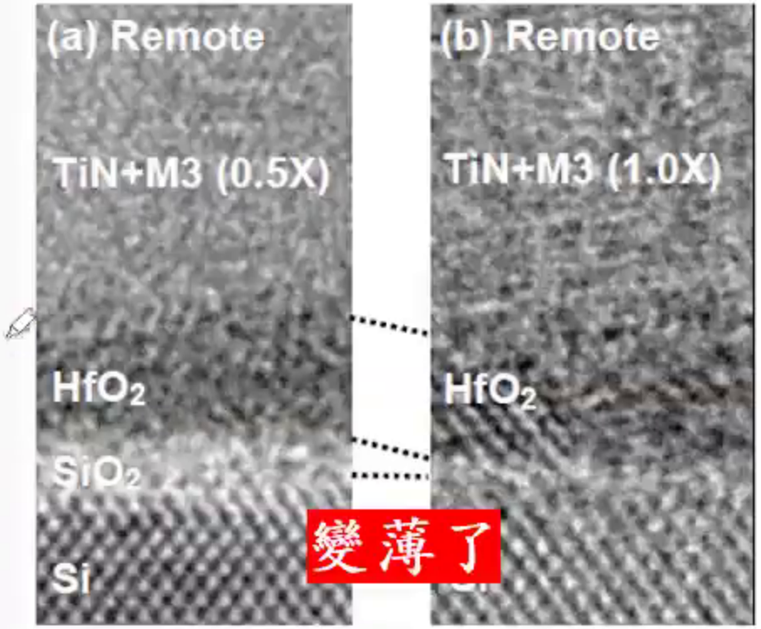
Gate First High-k/Metal Gate Stacks with Zero SiO_x Interface Achieving EOT=0.59nm for 16nm Application, J. Huang VLSI'09

IL scavenging = “隔山打牛”神功?

- 如右圖所示，HK下面可憐瘦弱(<1nm)的IL裡面的氧，好像誰都可依欺負她，硬搶她體內的氧，使它變薄(因為SiOx → Si)
- 此制程曰之"IL Scavenging“

Figure 3. Schematics of direct- and remote- scavenging techniques in the literature.

Type	Direct		Remote
Scavenging element (M)	Within High-k		Isolated from High-k
Schematics			
Ref.	[29, 30, 32]	[33]	[19, 35]



Ultimate Scaling of High-κ Gate Dielectrics: Higher-κ or Interfacial Layer Scavenging? Materials 2012, 5, 478-500; T. Ando

HKIL整體电性厚度: T_{inv} = EOT + 4Å

- 目前業界(IBM，IMEC)等所出版論文皆假設:
- T_{inv} = EOT + 4Å

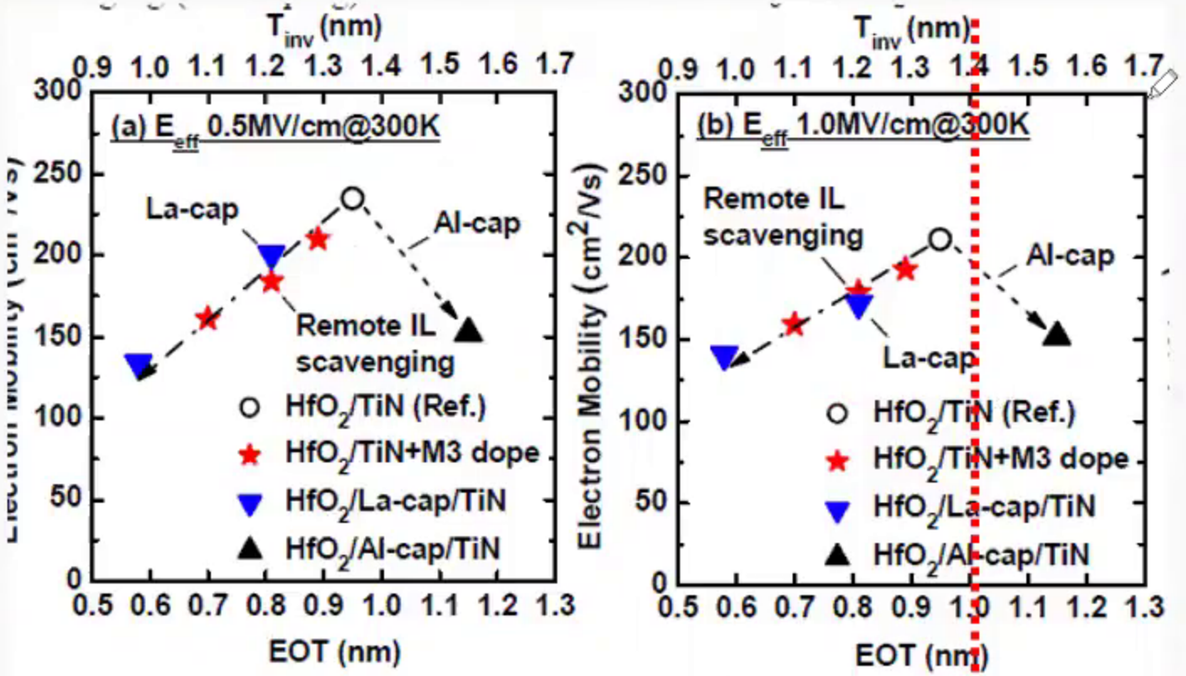
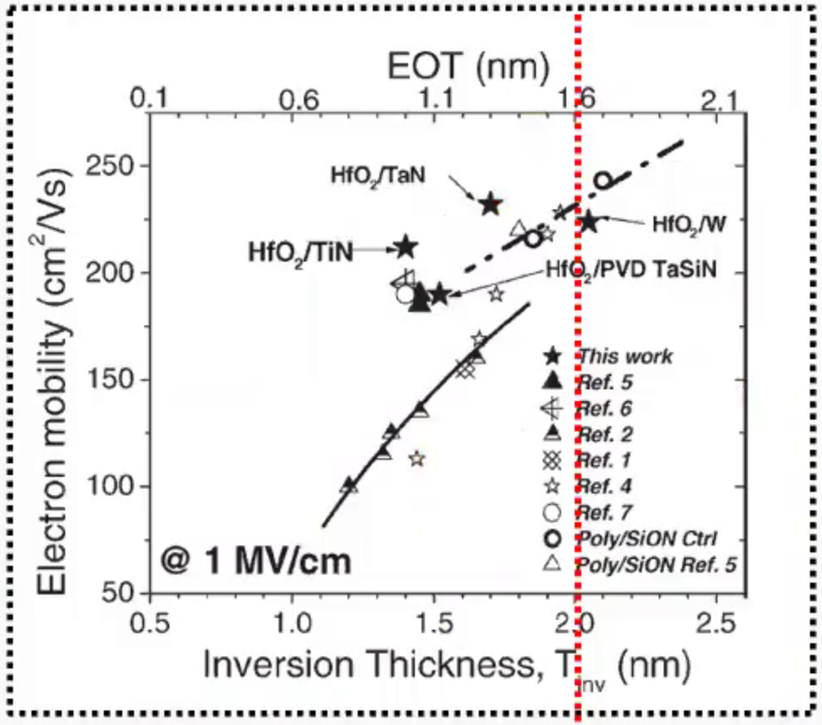


Fig. 13: Electron mobility (E_{eff} (a) 0.5 MV/cm (b) 1.0 MV/cm) vs. EOT plot for TiN gate w/ and w/o cap layers (La, Al) and TiN+M3 dope gate.

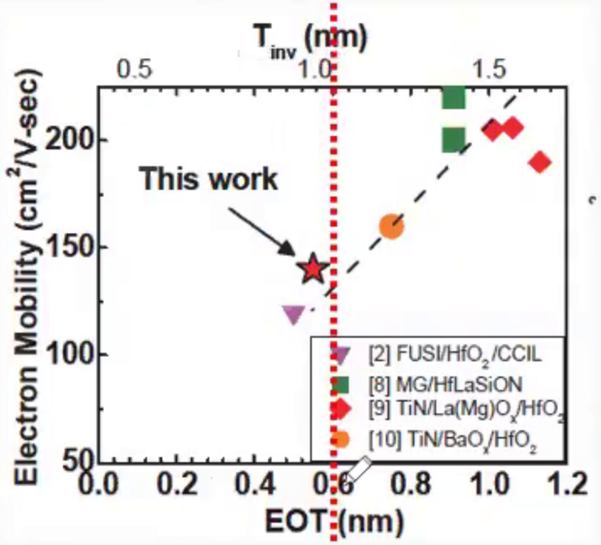
Understanding Mobility Mechanisms in Extremely Scaled HfO_2(EOT 0.42 nm) Using Remote Interfacial Layer Scavenging Technique and V_t-tuning Dipoles with Gate-First Process T. Ando (IBM), IEDM'09

HKIL整體电性厚度: T_{inv} = EOT + 4Å

- 目前業界公認
  T_{inv} = EOT + 4Å



Process Optimization for High Electron Mobility in nMOSFETs With Aggressively Scaled HfO2/Metal Stacks, V. Narayanan et al (IBM), TED, 2006, p.591



Extremely scaled gate-first high-k/metal gate stack with EOT of 0.55 nm using novel interfacial layer scavenging techniques for 22nm technology node and beyond, K. Choi et al, VLSI'09

附錄:一層Si有多厚?

- **Lattice constant of silicon**
  - a_{Si}= 5.43Å
- **Interplanar spacing $d_{(100)}$ and $d_{(110)}$ of Si(100) and Si(110) are 1.36 Å and 1.92 Å**
  - $d_{(100)} = a_{Si}/4 = 5.43/4 = 1.36$ Å
  - $d_{(110)} = \frac{a_{Si}}{2\sqrt{2}} = \frac{5.43}{2\sqrt{2}} = 1.92$ Å

Table 1.2. The major characteristics of the crystalline structure of the elements of the diamond group.

Element	Lattice constant [Å]	Interatomic spacing in axial direction [Å]			Interplanar spacing [Å]		
		⟨100⟩	⟨110⟩	⟨111⟩	(100)	(110)	(111)
C	3.56	3.56	2.52	1.54 4.59	0.89	1.26	0.51 1.54
Si	5.43	5.43	3.85	2.35 6.99	1.36	1.92	0.78 2.35
Ge	5.65	5.65	4.00	2.45 7.29	1.41	2.00	0.81 2.45

Table 1.1. The basic data for the structure of cubic crystals (spacings are given in the units of the lattice constant a).

Structure	Atoms per unit cell	Interatomic spacing in axial direction			Interplanar spacing		
		⟨100⟩	⟨110⟩	⟨111⟩	(100)	(110)	(111)
simple	1	1	$\sqrt{2}$	$\sqrt{3}$	1	$1/\sqrt{2}$	$1/\sqrt{3}$
bcc	2	1	$\sqrt{2}$	$\sqrt{3}/2$	1/2	$1/\sqrt{2}$	$1/2\sqrt{3}$
fcc	4	1	$1/\sqrt{2}$	$\sqrt{3}$	1/2	$1/2\sqrt{2}$	$1/\sqrt{3}$

Crystal Channeling and Its Application at High-Energy Accelerators, V. Biryukov et al

試問:鰭4nm腰圍含有多少硅原子層?

解答: ~ 21 層for Si(100)/<110>

- **$d_{(110)}$ is 1.92 Å, therefore 40/1.92 ~ 21 layers**

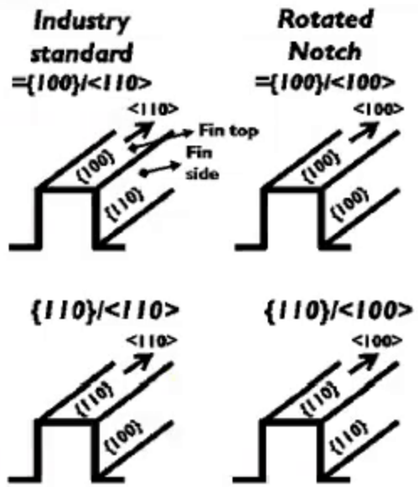
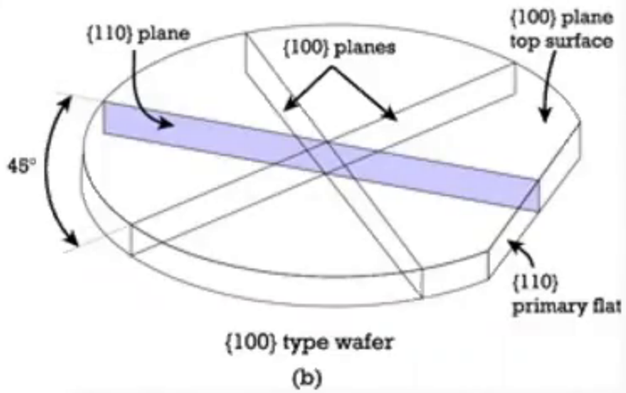
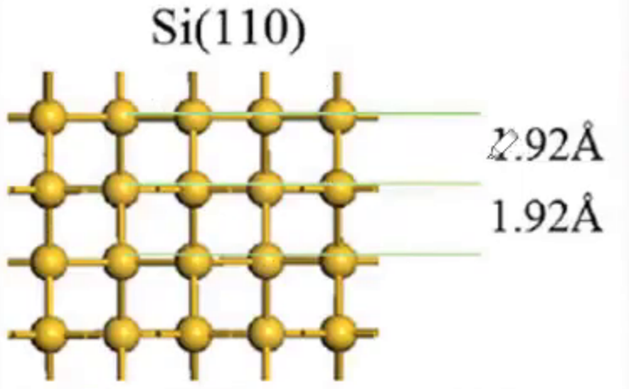


Figure 2. Overview of the FinFET orientations, defined by *{mnp}/<ijk>*, where *{mnp}* is the wafer orientation and *<ijk>* is the channel direction.



X-ray diffraction applications in thin films and (100) silicon substrate stress analysis James D. Rachwal



Effect of crystal plane orientation on tribochemical removal of monocrystalline silicon, Xiao et al, www.nature.com/scientificreports/

FinFET Stressor Efficiency on Alternative Wafer and Channel Orientations for the 14 nm Node and Below, G. Eneman, 2015 International Conference on IC Design & Technology (ICICDT)

附錄: 蘿蔔腿斜著跑竟變成超級飛毛腿

試問: 為何电洞妻的蘿蔔腿(hole mobility)在fin sidewall surface (110)上竟跑得比电子夫的飛毛腿快?

- 如右圖所示

解答: 因為(110)原子密度比較大也

- 如右圖所示，(110)晶格的面相與(110)很不相同，乍看之下，好像(110)比較寬鬆，然而屈指一算，竟然發現
  - Ns(110) = 9.6/nm^2 > Ns(111) = 7.8/nm^2 > Ns(100) = 6.8/nm^2
- 电洞跑的方式與电子很不同，她的蘿蔔腿在(100)/ <110>上竟變成超級飛毛腿

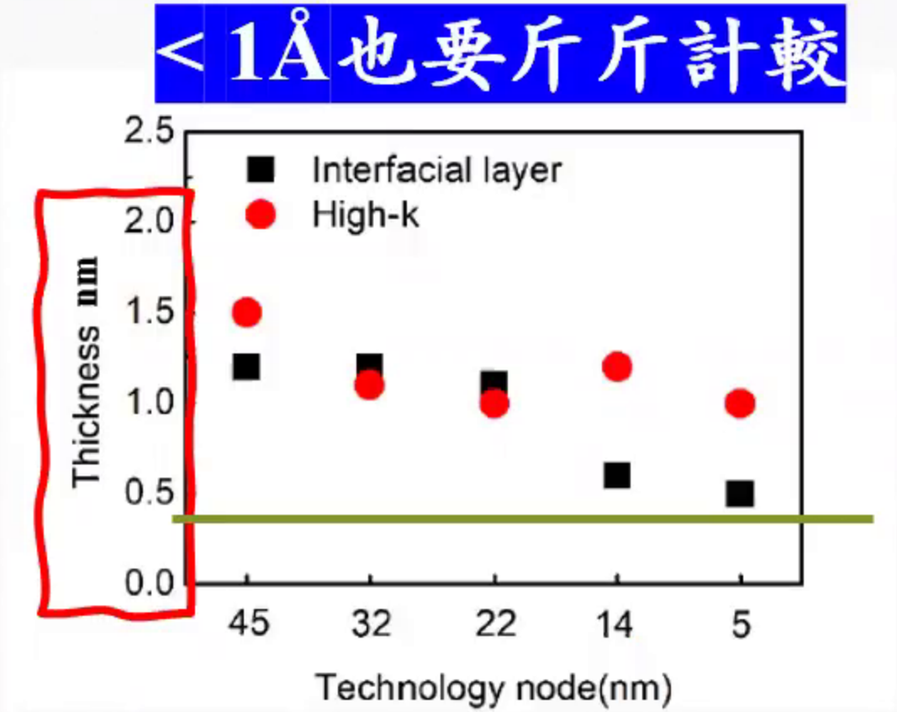
Table II. Summary of the mobility values of the top and facet surfaces for the various fin structure types. The unit of electron and hole mobility is $cm^2 \cdot V^{-1} \cdot s^{-1}$. The values of electron mobility and hole mobility were taken at E_{eff} of 1.0 and 0.6 MV/cm, respectively.

		Type				
		1	2	3	4	5
Channel direction		⟨110⟩		⟨100⟩	⟨110⟩	⟨100⟩
Top surface orientation		(100)		(110)		
Facet surface orientation		(110)	(551)	(100)	(100)	(110)
Top surface	electron mobility	253		253	79	96
	hole mobility	81		81	206	128
Facet surface	electron mobility	79	88	253	253	96
	hole mobility	206	210	81	81	128

Carrier mobility characteristics of (100), (110), and (551) oriented atomically flattened Si surfaces for fin structure design of multi-gate metal–insulator–silicon field-effect transistors R. Kuroda et al 2014 Jpn. J. Appl. Phys. 53 04EC0

附錄: Si Fin (110) → ~1.34nm SiO_xH_y (110)

- 右圖所示，IL(SiO_xH_y)可是越來越薄(HK厚度卻不動如山)
- SiOxHy的增加直接增加EOT(→CET)，而且是1:1的比例，每1Å約相當於10%CET(or Tinv)，也就是可能影響近~10%電流也
  - 註: 1nm CET = 3.4μF/cm²
- 理論上，FinFET的 sidewall native oxide (SiO_xH_y) 太厚，所以必須優化變薄一些，但卻也不能太薄



State of the Art and Future Perspectives in Advanced CMOS Technology, Henry H. Radamson, *Nanomaterials* 2020, *10*(8), 1555

芯片良率難搞篇
-原來你是我的遮羞布

HKIL

Tinv = EOT (TEM) + 4Å (QM)

王不老說半导