Handbook of Materials Structures, Properties, Processing and Performance
DOI 10.1007/978-3-319-01905-5_34-1

Photolithography Applied to Integrated Circuit (IC) Microfabrication

Lawrence E. Murr*
Metallurgical and Materials Engineering, University of Texas at El Paso, El Paso, TX, USA

Abstract

Photolithography as it relates to lithography fundamentals is described and applied to the lithography process utilized in producing integrated circuits (ICs) and layered electronic device structures. These structures have some thickness or layering restrictions but are nonetheless layer-manufactured structures on an electronic landscape, usually a silicon wafer substrate.

Introduction: Photolithography Fundamentals

Additive manufacturing or 3D printing technologies employ a layer-by-layer building process to fabricate 3D, monolithic structures using computer-aided design (CAD) strategies or models. These technologies are also known as optical fabrication, photo-solidification, or solid freeform fabrication (SFF). More generally these technologies are referred to as *stereolithography* (SLA), a term coined by Charles Hull in 1986. However, stereolithography can be conceptually related to a lineage of lithographic processes.

Lithography, a method for printing using limestone (or other flat stones; from the Greek lithos, meaning stone, and graphein, meaning to write), was invented by Alois Senefelder around 1797 and used by artists to produce prints of their work. In this process, the artist drew a picture on the surface of a flat or flattened stone (primarily limestone) with a mixture of wax, soap, lampblack (the ink), and rainwater. This image would repel water, while the surrounding, uncoated stone surface would retain the water, selective hydrophobic/hydrophilic surface regimes. The hydrophobic (image) regions could be recoated with ink in the greasy (wax) matrix to allow continuous printing or transfer of the inked image to paper or other suitable medium. However, the image in normal lithography is reversed, but could be offset by transferring the image to a flexible sheet such as rubber and then printed from the offset (reversed) image. This is the standard printing format today except the image is made of a polymer coating applied to a flexible aluminum plate affixed to a roller-plate system as illustrated in Fig. 1. This modern offset lithography or high-volume lithography used to produce newspapers, magazines, books, posters, and other paper image formats depends on photography or a photographic process. In the original photolithography process, images were photographically transferred to a stone surface or the more efficient, flexible aluminum plate. This process led to breaking down the original photograph into dots of varying sizes suitable to press reproduction which became known as the halftone process for reproduction.

Color printing of multicolor prints or chromolithography used separate stones or aluminum plates for each color, and the paper or medium to be printed upon must pass through the printing press for each color in the final print. Precise registry is required to assure that each color is placed in the precise position in each print. These are also broken down in the halftone process producing printable color dots, with image resolution determined by the number of dots printed in a unit

*Email: lemurr@utep.edu

DOI 10.1007/978-3-319-01905-5_34-1

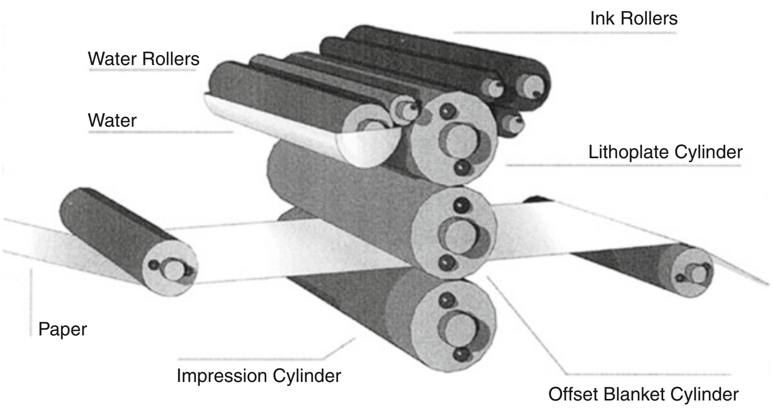

Fig. 1 Offset lithography schematic view

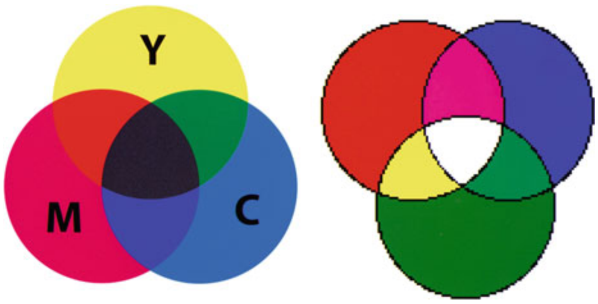

Fig. 2 Color addition. (a) Standard offset *cyan* (*C*), *magenta* (*M*), and *yellow* (*Y*). *Red–green–blue* addition characteristic of display color

area: usually dots per inch (dpi) in an area one inch on a side. In the preparation of the lithographic plates, the polymer coating is photosensitive and resistant to acids or other etching compounds. This material is referred to as a photoresist, which when exposed to the photographic negative hardens where the negative image allows light to pass. The photoresist is developed by rinsing in a solvent which removes the unhardened areas. The image area on the prepared plate takes up ink as noted previously. In offset printing (or lithography) as illustrated in Fig. 1, each color of ink is applied separately – one for each plate. However, color dots of four inks – cyan (blue), magenta, yellow, and black – are deposited in specific patterns, creating color addition which produces a wide range of perceived colors. This is referred to as four-color printing or four-color process lithography. Figure 2 illustrates these color fundamentals, which in various ways can be applied to color image formation or projection, including three-phosphor dot image screens or flat screen arrays involving LCD or LED color dots (or areas). Correspondingly, inkjet printing can print color dots in similar patterns to create full color, or the perception of a wide range of color hues when more than four colors are printed. It will be observed later that inkjet arrays can be used to print in three-dimensions as illustrated conceptually in Fig. 96 of chapter "► Chemical Forces: Nanoparticles" for 3D-cell printing or bioprinting.

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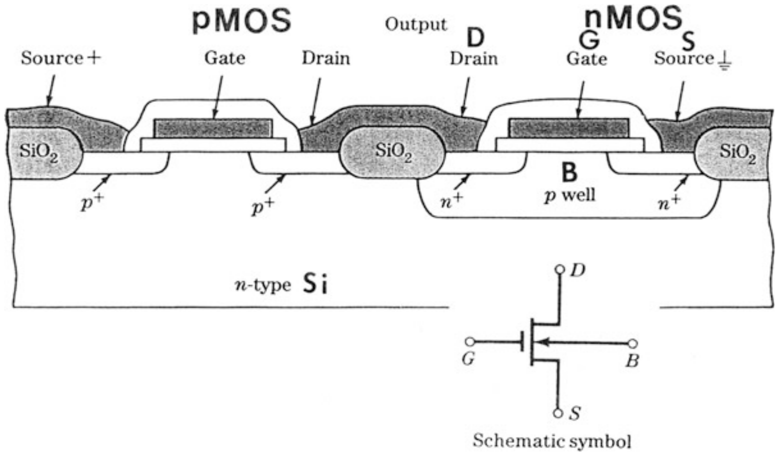

Fig. 3 CMOS (n- and p-type) field-effect transistors fabricated on the same silicon wafer substrate

Microfabrication Fundamentals

Integrated circuits, monolithic integrated circuits (ICs), or what are commonly referred to as microchips are fabricated by multiple, overlapping, functional, patterned layers defined by photolithography. Patterns are created on flat semiconductor surfaces, usually silicon similar to the photoresist sensitization in offset lithography, although color (image) sequences represent electronic functions or functional regions of conductors, insulators, or doping sequences to create memory devices. These are often complementary metal–oxide–semiconductor (CMOS) field-effect transistors which are formed whenever the gate layer (polysilicon or metal) crosses a diffusion layer creating n- or p-type semiconduction region as illustrated schematically in Fig. 3 (Baker 2010).

This process begins by spin coating a silicon wafer with a photoresist similar to the offset lithography plate. A photomask characterizing the circuitry or circuit elements in a small feature image is projected onto the wafer photoresist using intense light, usually ultraviolet (UV) light. In modern IC fabrication, deep UV excimer lasers (krypton fluoride (KrF)) having a wavelength of 248 nm or argon fluoride (ArF) at a wavelength of 193 nm are used. The light source wavelength (λ) is a controlling factor in the minimum feature size that the projection system can print:

$$CD = K\lambda/NA, \tag{1}$$

where CD is the critical dimension or minimum feature size, λ is the wavelength, K is a process factor commonly assumed to have a value of ~0.4, and NA is the numerical aperture of the lens relative to the wafer surface. While this characterizes a design role for lateral dimensions of features in the plane of the IC (or the silicon wafer), the depth of focus (DF) presents a competing constraint since it restricts the thickness of the photoresist and the wafer topography or functional layer thickness:

$$DF = K'\lambda/(NA)^2, \tag{2}$$

where K' is another process-related parameter.

Generally, CD in Eq. 1 of chapter "▶ 3D Printing: Printed Electronics" is connected with circuit size or the number of transistors (or memory elements) on an IC chip, which has followed the doubling law or Moore's law. In 1965, Gordon Moore, cofounder of Intel, noted that the number of

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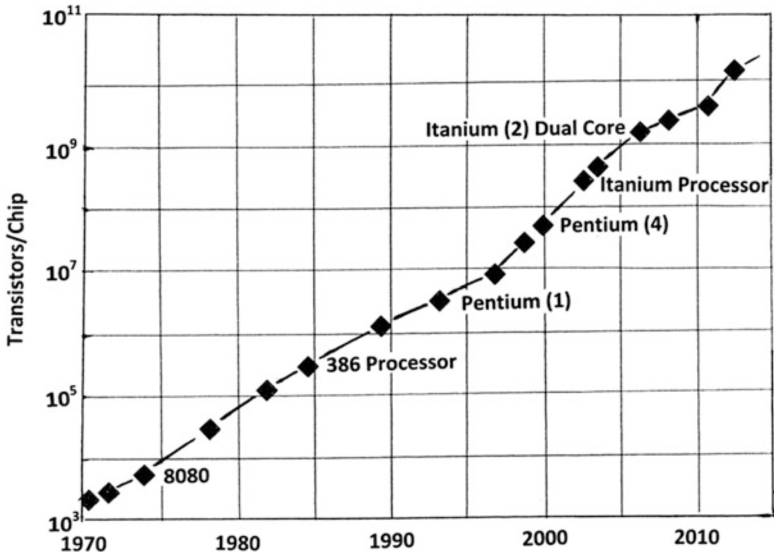

Fig. 4 Moore's law: transistors per chip by production year (Intel data). Only a few types of processor chips are noted

transistors on an IC chip would double every 18–24 months. This law has been generally followed up to the present time (2013), where the Intel chip density exceeds 10 billion transistors as illustrated in Fig. 4. Correspondingly, minimum feature sizes in chip manufacturing (Eq. 1 of chapter "▶ 3D Printing: Printed Electronics") have decreased from 500 nm in 1990 to below 45 nm in 2010, with CD (Eq. 1 of chapter "▶ 3D Printing: Printed Electronics") approaching ~10 nm by 2020. The ultimate limit of downsizing will be roughly the distance between silicon substrate atoms, ~0.3 nm. Operating frequency (or clock speed) trends for Intel processors have also increased from ~50 MHz in 1990 to ~3 GHz in 2010. IC circuit size classification also changed from small-scale integration (SSI) in 1963 to medium-scale integration in 1970 (Fig. 4), large-scale integration (LSI) in 1975, very-large-scale integration (VLSI) in 1980, ultra-large-scale integration (ULSI) in 1990, and to giga-scale integration (GSI) after 2010 (Fig. 4). The VLSI revolution began in large part as epitomized by the classic text by Carver Meade and Lynn Conway, "Introduction to VLSI Systems" published in 1980 (Meade and Conway 1980).

Figure 5 illustrates an example of a cross-sectional view of a fabricated chip with a reversed, p-type Si substrate, in contrast to Fig. 9.3, showing an nMOS and pMOS transistor. A modern CMOS wafer chip will go through the photolithographic cycle as many as 50 times. While this represents a feature of layer-by-layer fabrication, the integrated circuit has come to be known as a monolithic integrated circuit or single, functional chip. A truly 3D lithographed electronic monolith could be constructed by stacking chips and interconnecting them by vertical, conducting vias. This is a difficult feature to achieve in a unitized production process.

Photolithography (or optical lithography) as illustrated in the context of UV excimer laser lithography implicit in Eqs. 1 and 2 of chapter "▶ Tissue Engineering Scaffolds and Scaffold Materials" and as applied to Fig. 5 shares some fundamental principles with offset color lithography printing (Fig. 1) in that a photographic (mask) pattern is created in a photoresist or etching resist through UV excimer laser exposures with the design feature of each layer function characterized by a color: green, n-diffusion; red, polysilicon; blue, metallizational; yellow/brown, p-diffusion; and magenta (purple) and cyan (light blue), metallizations 2 and 3, respectively. However, this exposure can be accomplished by direct writing of the pattern by the laser or by an electron beam, and the subsequent stages in the lithography process have more in common with etching than lithographic

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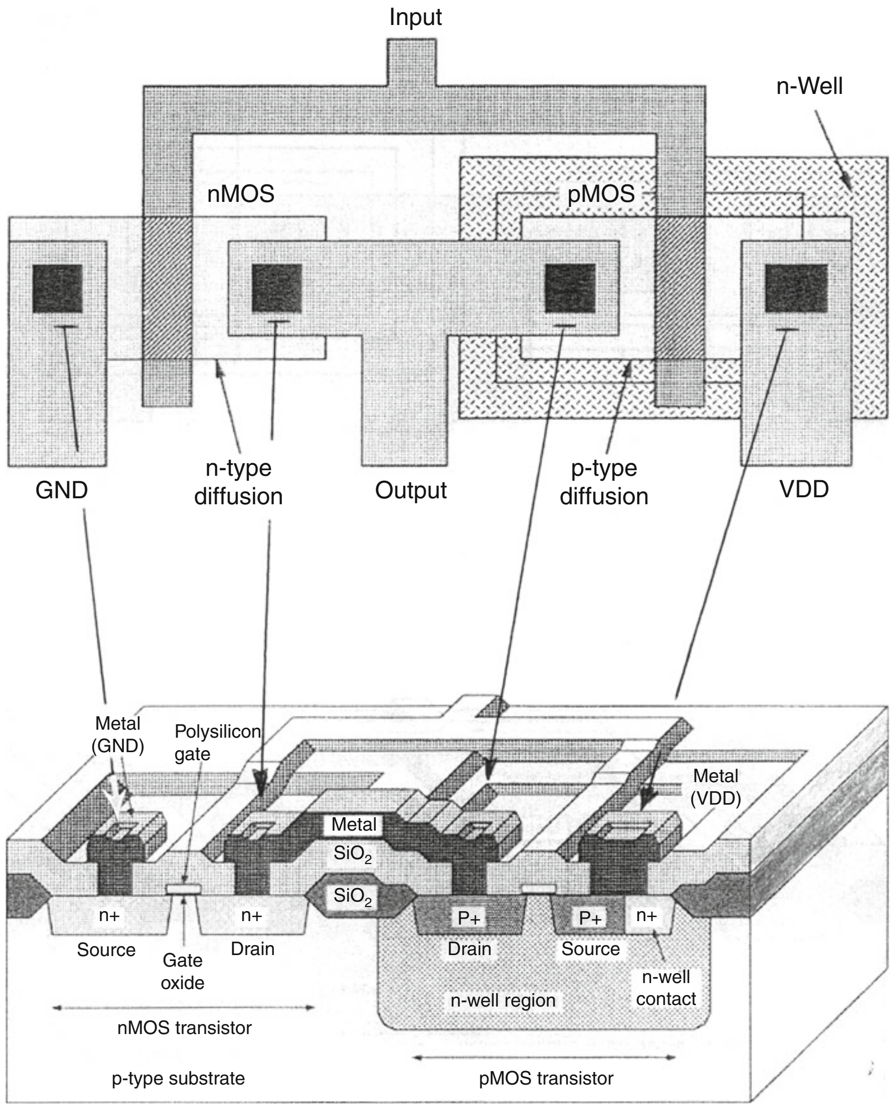

Fig. 5 Cross-sectional view showing CMOS transistor on chip composite layout. GND and VDD denote ground and above ground voltage contacts (Adapted from Maly 1987)

printing (Fig. 1). The photoresist can be positive (preferred) or negative relative to the solubility in the developer of exposed areas.

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Index Terms: