WSL - 3



Calibration Techniques for Wireless SoCs

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Outline

- Why Calibrate?
- Calibration Techniques



- Resistor Calibration
- RC Time Constant Calibration
- VCO Calibration
- Automatic Frequency Control (Agile Frequency Offset Calibration)
- Quadrature Error and LO Feedthrough Calibration
- LO Generation Amplitude Control System and Calibration
- Other Calibrations
 - Process Sensing and Calibration
 - Temperature Sensing and Calibration
 - Power Detector Calibration



Calibrations & "Support" Circuitry

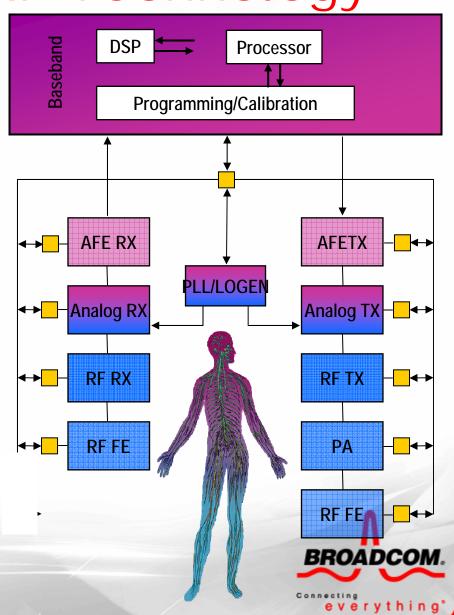
- Radio self-calibrations used to be considered as "nice to have". Today radio self-calibrations have been recognized as absolutely essential.
- Design of the calibration algorithms and methodology is an integral part of the radio design, and not an after-thought
- Chip level and system level auto-calibration is required for overcoming difficulties of integrated radio design, increasing chip and system yield and improving performance.
- Some examples:
 - VCO tuning
 - Tx and Rx IO Calibration
 - R-Calibration on bandgap blocks
 - RC time constant calibration
 - RSSIs
 - Agile center frequency correction

- Integrated temperature sensor
- Transmit LO feedthrough cancellation
- TSSI
- Rx DC Offsets & High-Pass Corners
- Process sensing



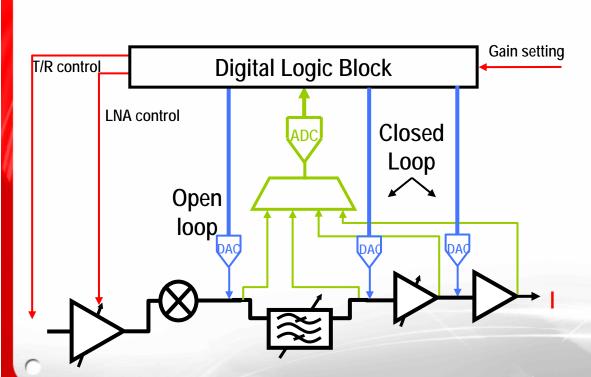
Today's Radio/RF Technology

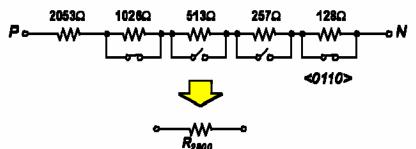
- Multiple Frequency Bands, Simultaneous Operation for multiple standards & Applications (WLAN, Bluetooth, RFID, ...)
- Rapid Real Time configuration/ calibration:
 - Optimum Performances
 - Max/Best Yields
 - Multiple Fab/Process, Package
 - No Factory Cal or Pre-Stored Cal data needed, No Flash or SRAM
 - Reduce RF test time
 - Compensate over temperature (which factory-cal does not allow for)

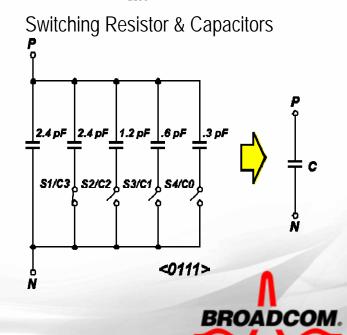


Radio Calibration Technology

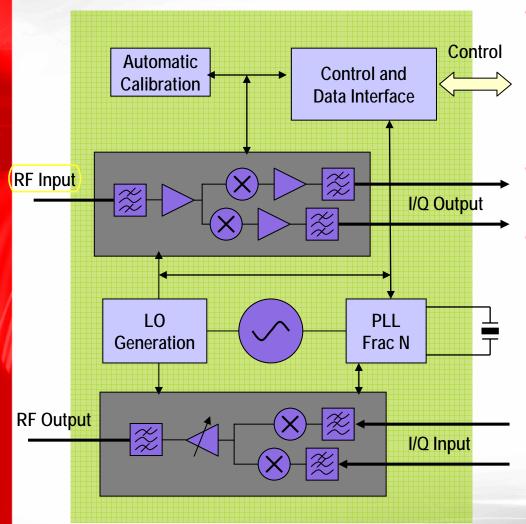
- Radio Blocks are developed using a digitally controllable matrix of
 - Passive devices (R, L, C)
 - Actives devices
 - ADCs & DACs
 - Small Controllers/DSPs







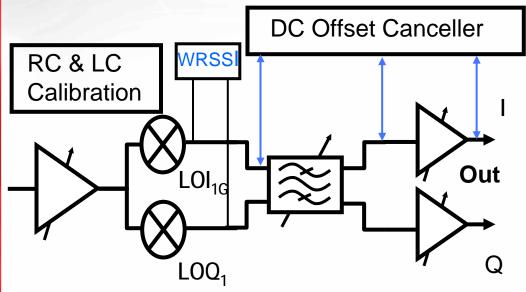
Integrated Smart Radio Technology



- Radio Blocks are developed using a digitally controllable matrix of Passive devices, Actives devices, ADCs & DACs & Small Controllers/DSPs
 - These units can be digitally programmed/ calibrated by local calibration Engines
 - These units can be digitally programmed/ calibrated through JTAG by baseband
- Long Term Agile/Real Time calibration
 - Optimizes overall performances over many frames or Packets
- Short Term Cal, Optimizes overall performances over a frame or packet
 - Accurate frequency response, center frequency, gain
 - Maximum dynamic range
 - Minimizing non-idealities, such as DC offsets, I/Q mismatches, feed-through, coupling...

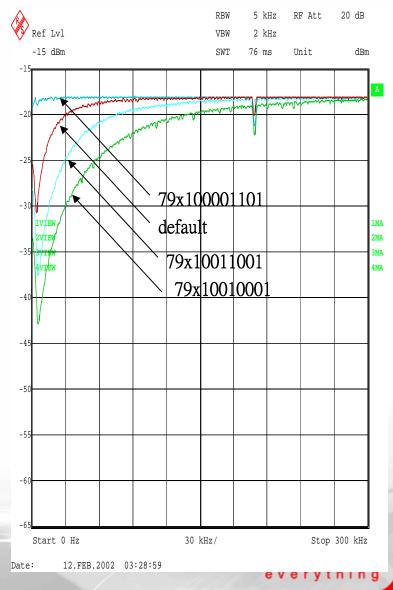


Receiver Architecture w/Calibration



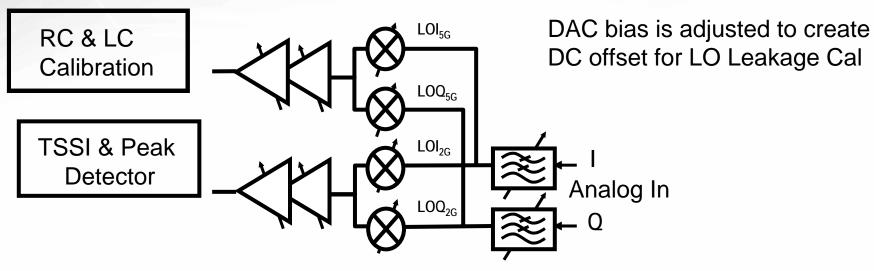
 Bandwidth and frequency response are set by programming R*C

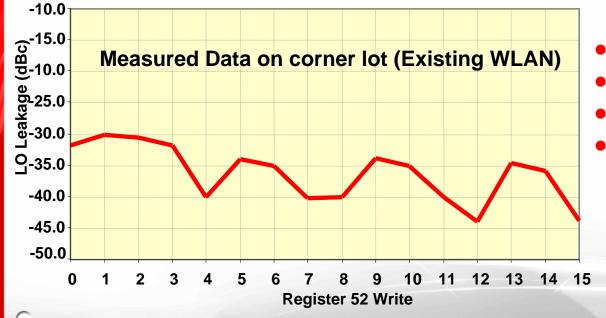
- Gain and current consumption are set by programming I*R
- RX DC offset and blocking can be calibrated globally and locally



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Multi-Band Transmitter w/Calibration

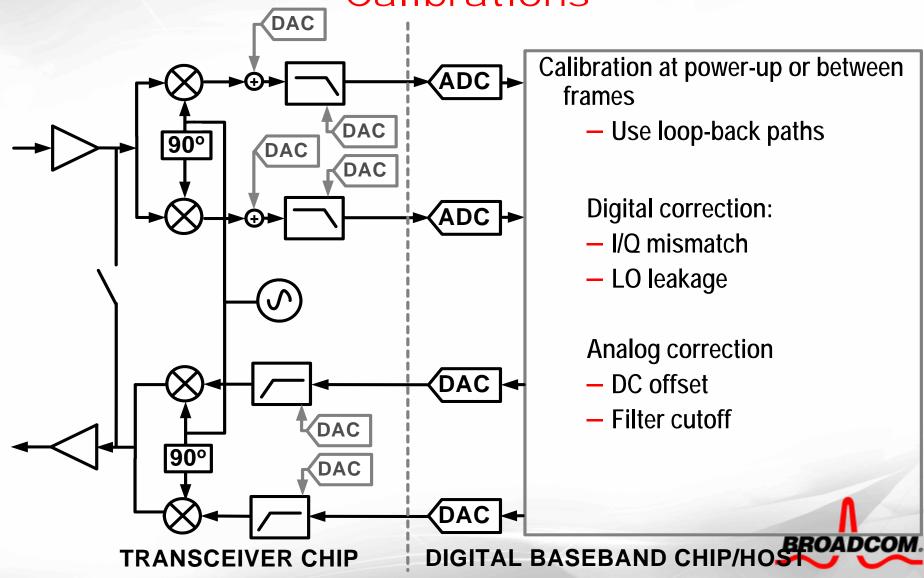




- Output level calibration
- LO Leakage Calibration
- Gain calibration
- Bandwidth & frequency calibration/programming



Example of Transceiver with Multiple Calibrations



Ref: I. Bouras, et al, ISSCC 2003

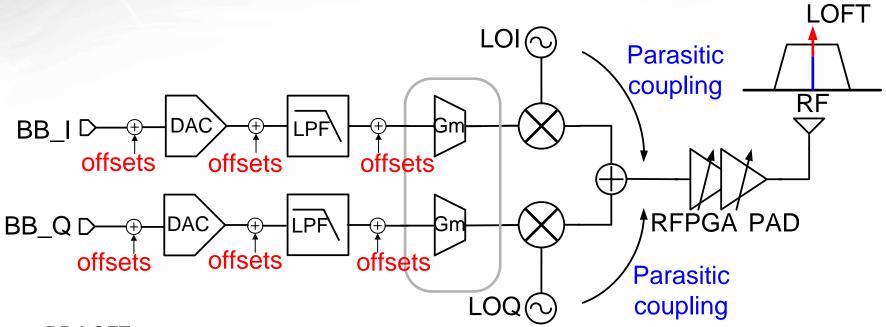
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Requirements for WLAN Transmitters

- Low transmit error vector magnitude (EVM).
 - High linearity.
 - Small I/Q imbalance.
 - Low local oscillator (LO) phase noise.
- Low local oscillator feed-through (LOFT).
 - <-15dBr for IEEE 802.11a standard.
- Wide and accurate gain-control range.
 - Rate dependent power control.



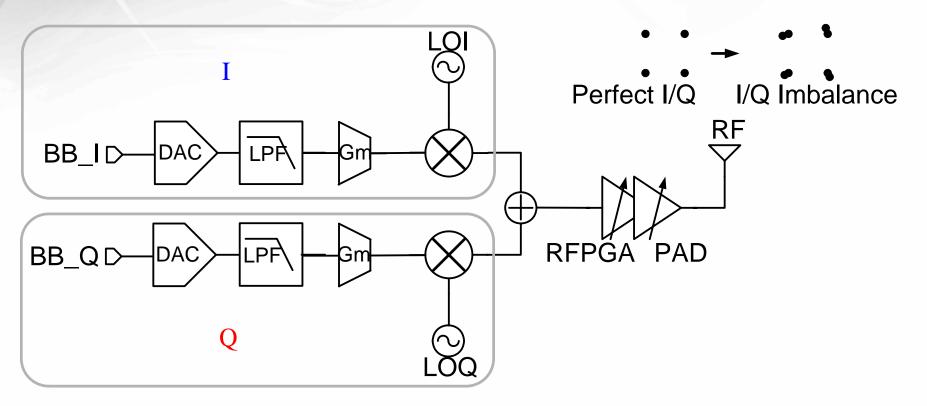
Sources of LOFT in Tx



- BB LOFT
 - Device offsets up-converted to RF.
- RF LOFT
 - Mismatch in the Gilbert cell mixer switching quads.
 - Parasitic capacitance coupling.
 - Mutual inductance coupling.



Sources of I/Q Imbalance in Tx

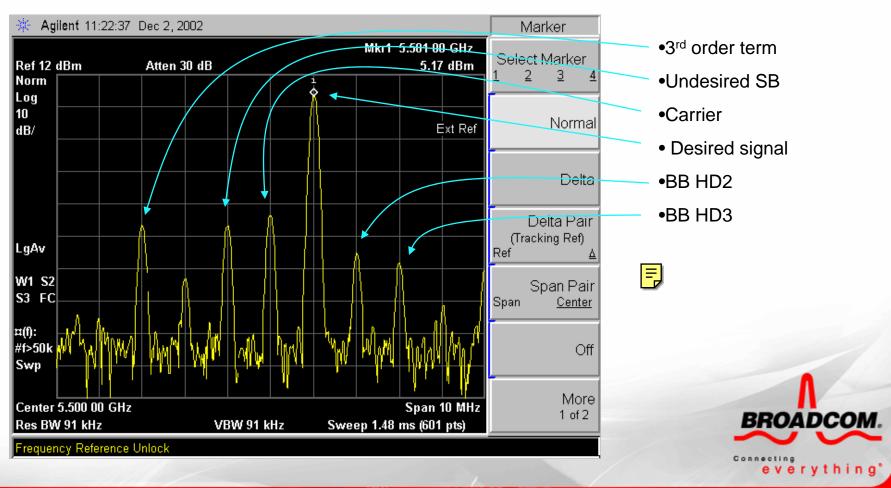


- Baseband I/Q imbalance
 - Device and bias mismatches between I and Q paths.
- RF I/Q imbalance
 - LO I/Q mismatch.
 - Mixer I/Q mismatch.



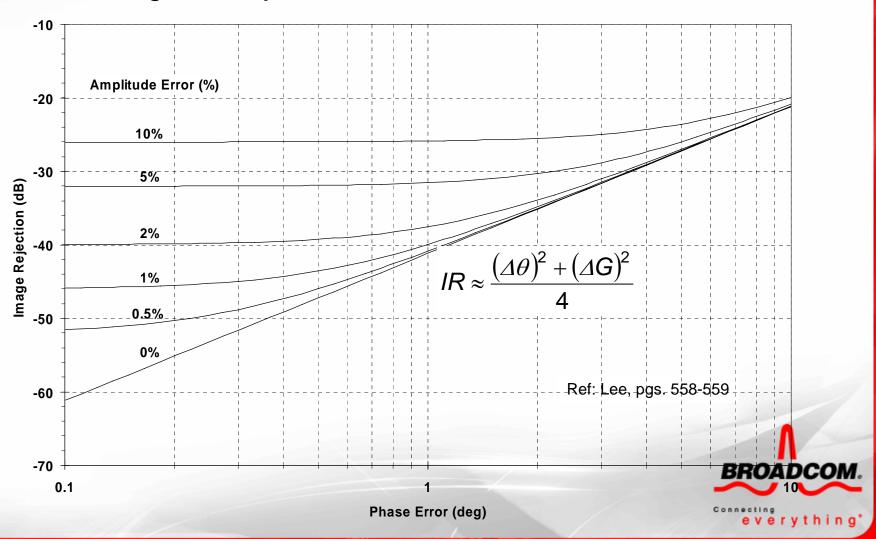
Tx: IQ modulator impairments

- Example output spectrum
 - BB input is single tone in quadrature at 1MHz; LO is 5.500GHz



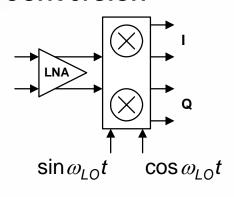
Rx & Tx: IQ Balance & Image Rejection

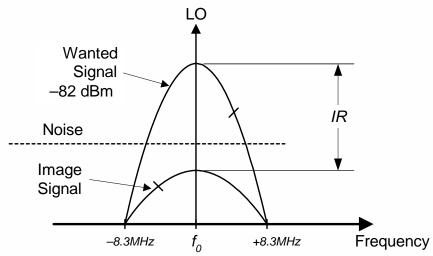
• Quadrature gain and phase errors:



Rx: Image Rejection: Direct Conversion

Direct Conversion

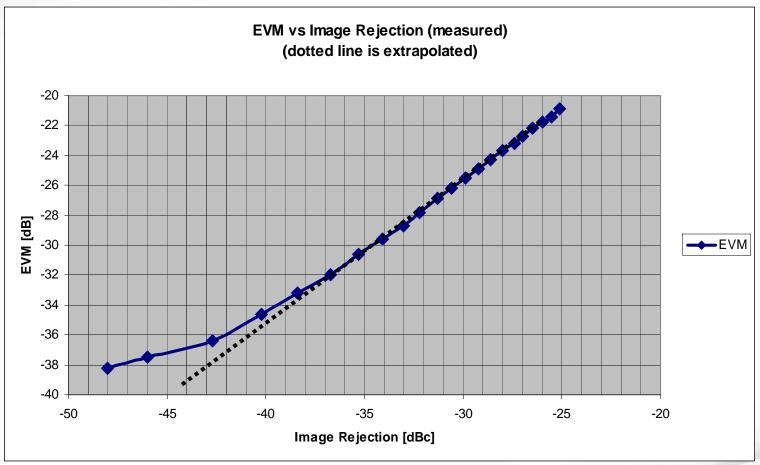




- Image rejection achieved through quadrature matching
 - Image is wanted signal itself
 - Since subcarriers are mostly uncorrelated image adds to noise floor (distorts OFDM constellation)
 - Image also causes orthogonality to suffer
- Requirement set by reference sensitivity / EVM test:
 - Most challenging for 64-QAM



Rx & Tx: EVM and Image Rejection

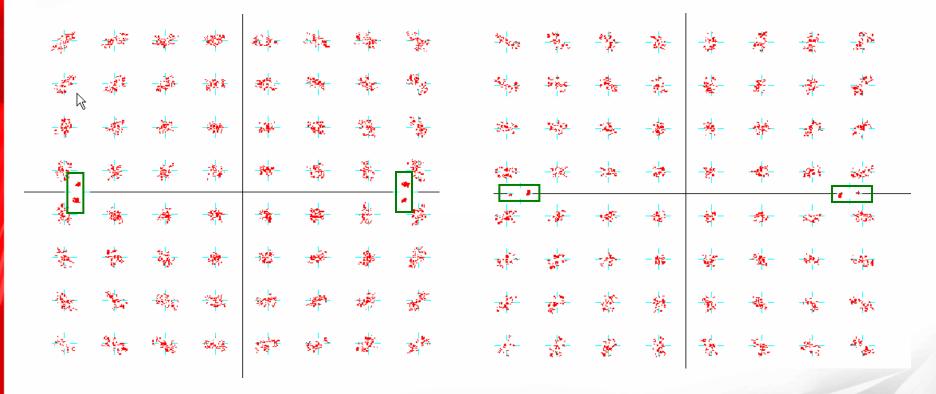




Impact of IQ Imbalance on Constellation

4° Phase error

0.5dB Amplitude error



Channel estimation based on preamble only

(a)

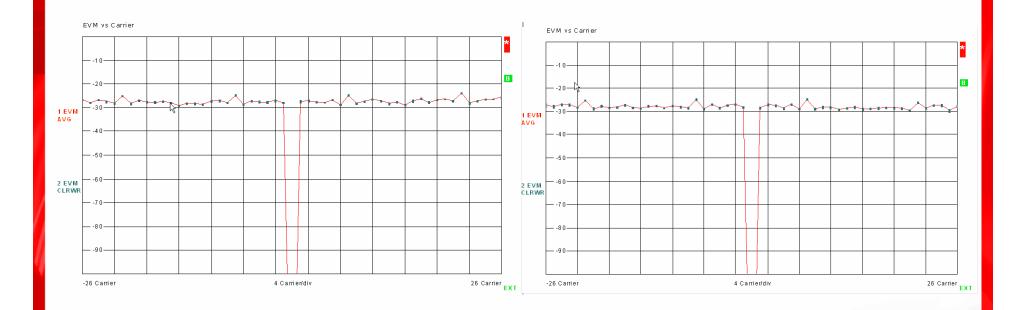
(b)



Impact of IQ Imbalance on EVM

4° Phase error

0.5dB Amplitude error



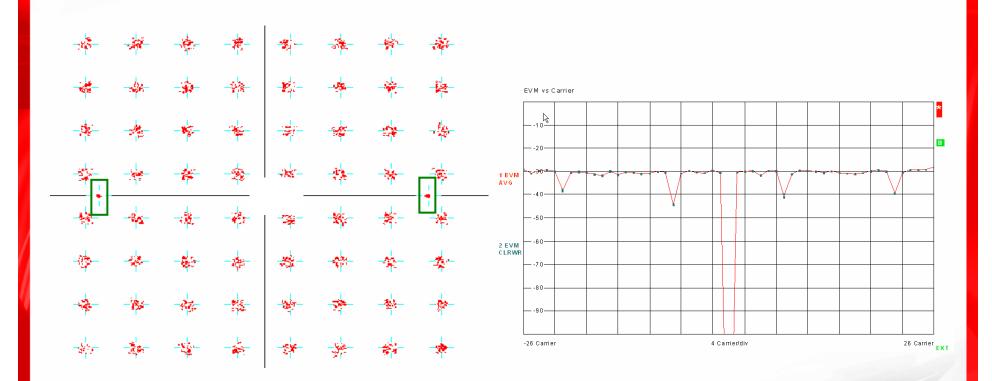
Channel estimation based on preamble only

(a)

(b)



Impact of IQ Imbalance on Constellation & EVM



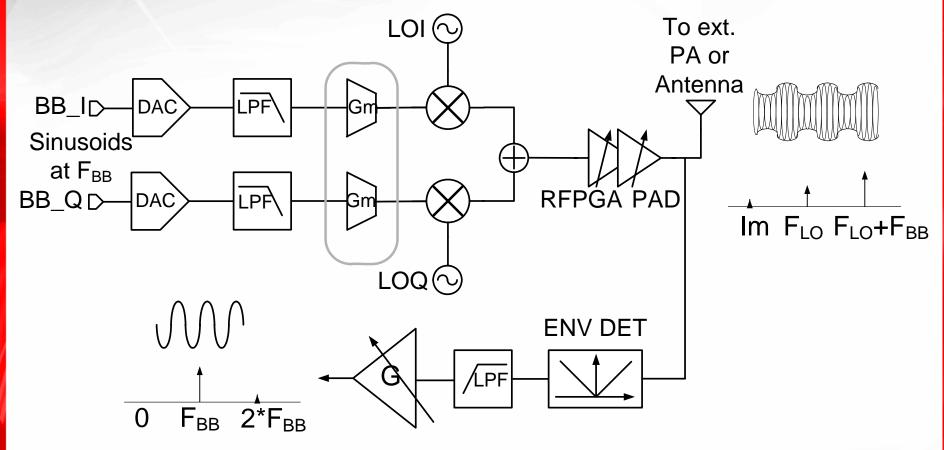
Channel estimation based on preamble & Payload

(a)

(b)



Detecting LOFT and I/Q imbalance



- Only LOFT shown for simplicity.
- Inject Sinusoid at F_{BB.}
- ADC+FFT to detect F_{BB} or 2*F_{BB}.
- LOFT at F_{BB}, I/Q imbalance at 2*F_{BB}.



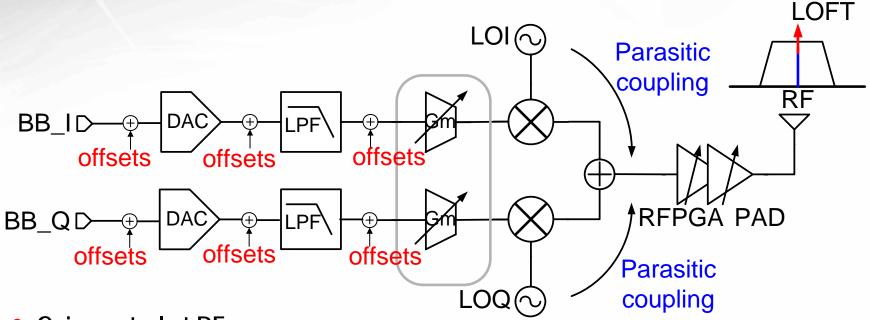
Ref: C. P. Lee et al, ISSCC 2006

Reducing LOFT and I/Q imbalance

- LOFT can be reduced by introducing DC offsets at baseband.
 - IDAC currents.
 - Affects bias points → Causes I/Q imbalance.
- I/Q imbalance can be corrected by pre-distorting the baseband data.
 - Need to come up with the correct pre-distorting coefficients.



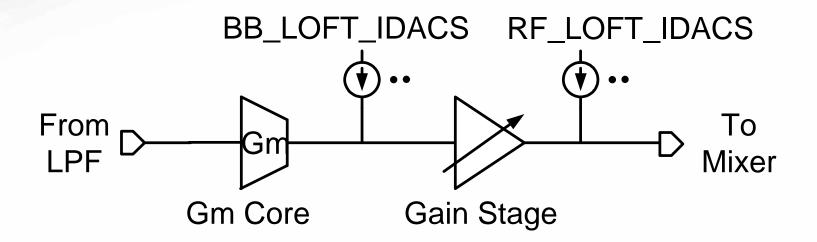
Gain Control



- Gain control at RF
 - BB and RF LOFT are scaled by gain.
 - Accuracy and range issues.
- Gain control at BB
 - Right before mixer to affect all BB offsets.
 - BB LOFT is scaled by gain.
 - RF LOFT is not scaled by gain.
 - LOFT will become a problem at low gains.



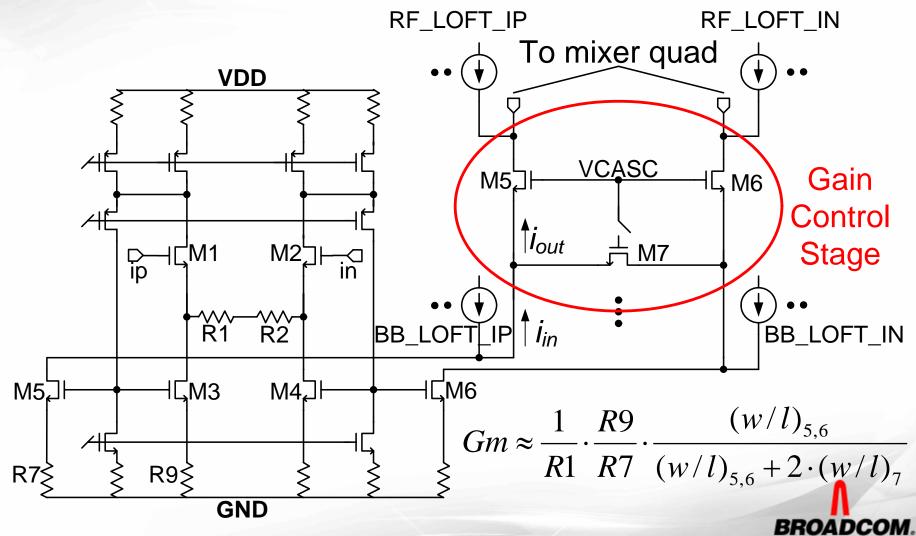
Conceptualized Gm Stage



- To cancel RF LOFT and BB LOFT independently,
 - High-Linearity Gm Core.
 - BB_LOFT IDACS to cancel baseband DC offsets.
 - Very low offset and highly linear Gain Stage.
 - RF_LOFT IDACS to cancel RF LOFT.

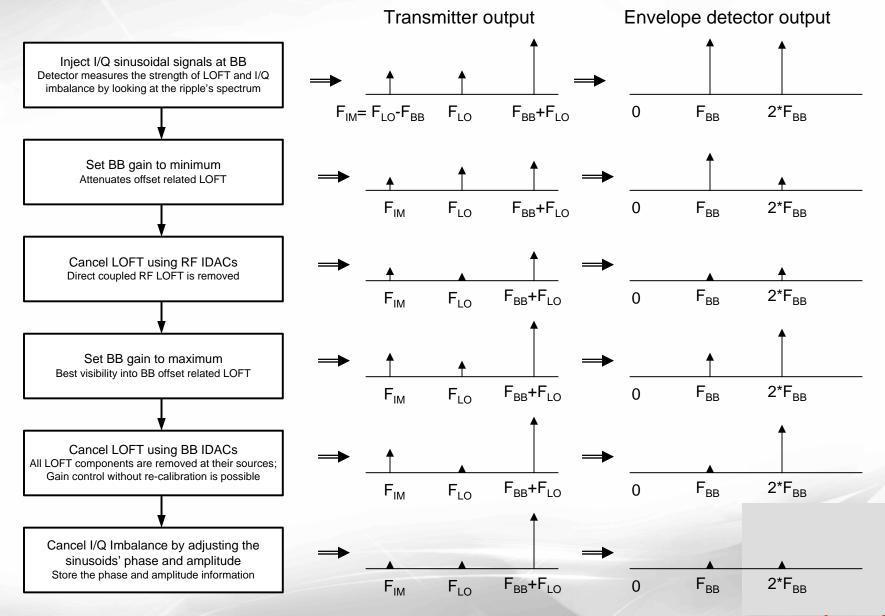


Proposed Gm Stage Implementation

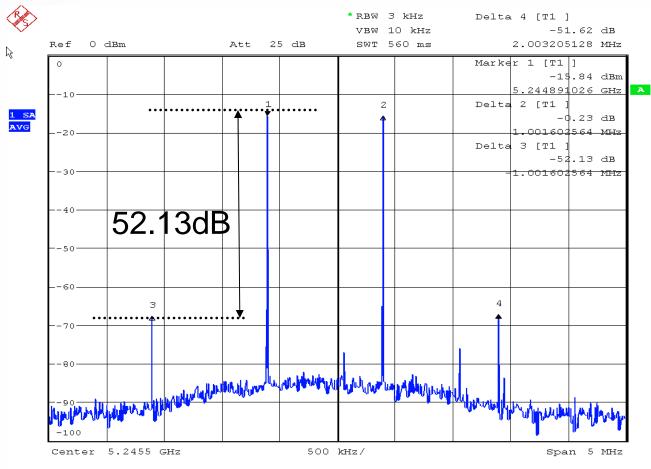


High-Linearity Gm Core

LOFT/IQ Calibration Algorithm



2-tone Linearity Test Entire Tx-Chain



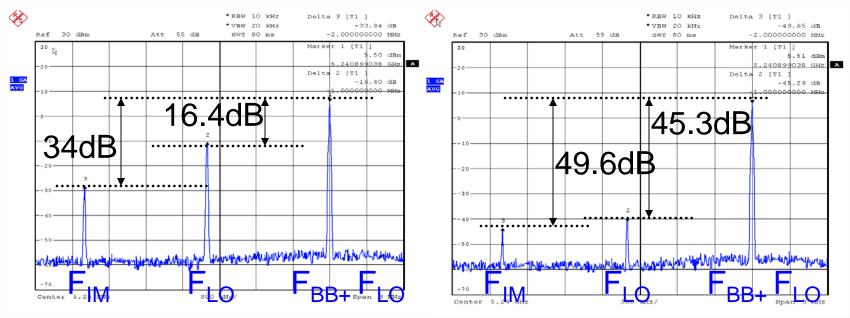
F_{LO}=5.24GHz, F2-F1=1MHz, Vin=1Vppd



Calibration - Maximum BB Gain



After Cal.



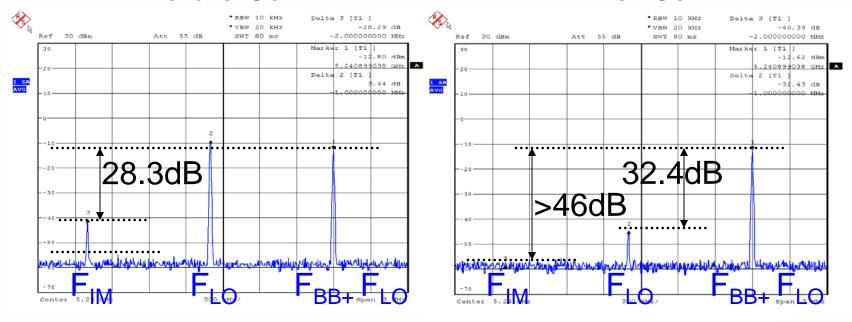
F_{LO}=5.24GHz, F_{BB}=1MHz, Vin=1Vppd



Calibration - Minimum BB Gain

Before Cal.

After Cal.



Fc=5.24GHz, F_{BB}=1MHz, Vin=1Vppd

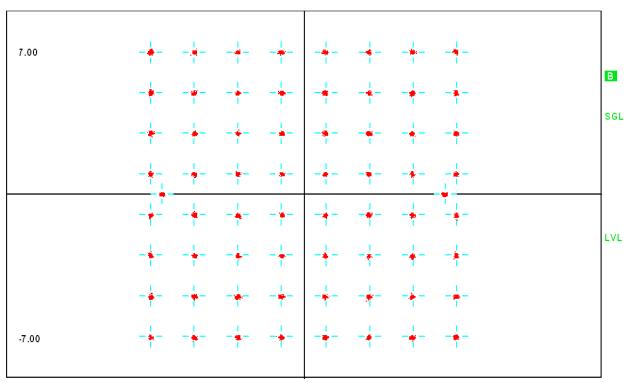


Constellation Diagram

Entire Tx Chain After Calibration

IEEE 802.11a					
Frequency:	5.24 GHz	Signal Level:	-9.8 dBm	External Att:	6 dB
စ်weep Mode:	Single	Trigger Mode:	Free Run	Trigger O ffset:	-10 µs
Burst Type:	Direct Link Burst	Modulation:	54 Mbps 64 QAM	No Of Data Symbols:	1/1366

Constellation vs Symbol



-7.00

7.00

Measurement Complete

Date: 30.AUG.2005 00:11:48

Fc=5.24GHz Po= -5dBm EVM < -40dB

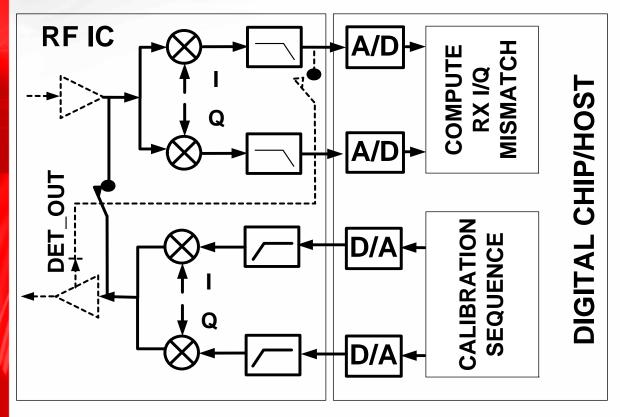


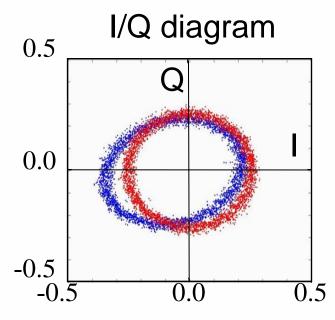
Summary: Tx IQ & LOFT Calibration

- Highly linear Transconductance stage.
 - IM3 rejection > 52dBc.
 - Gain range of 17.5dB in 2.5dB/step.
- LOFT and I/Q imbalance Cancellation.
 - Calibration algorithm to separate RF and BB LOFT.
 - LOFT better than 32dBc for all gain settings.
 - Image better than 46dBc for all gain settings.
- EVM better than -40dB in A-band and -41dB in G-band with -5dBm output power.



Rx IQ Calibration



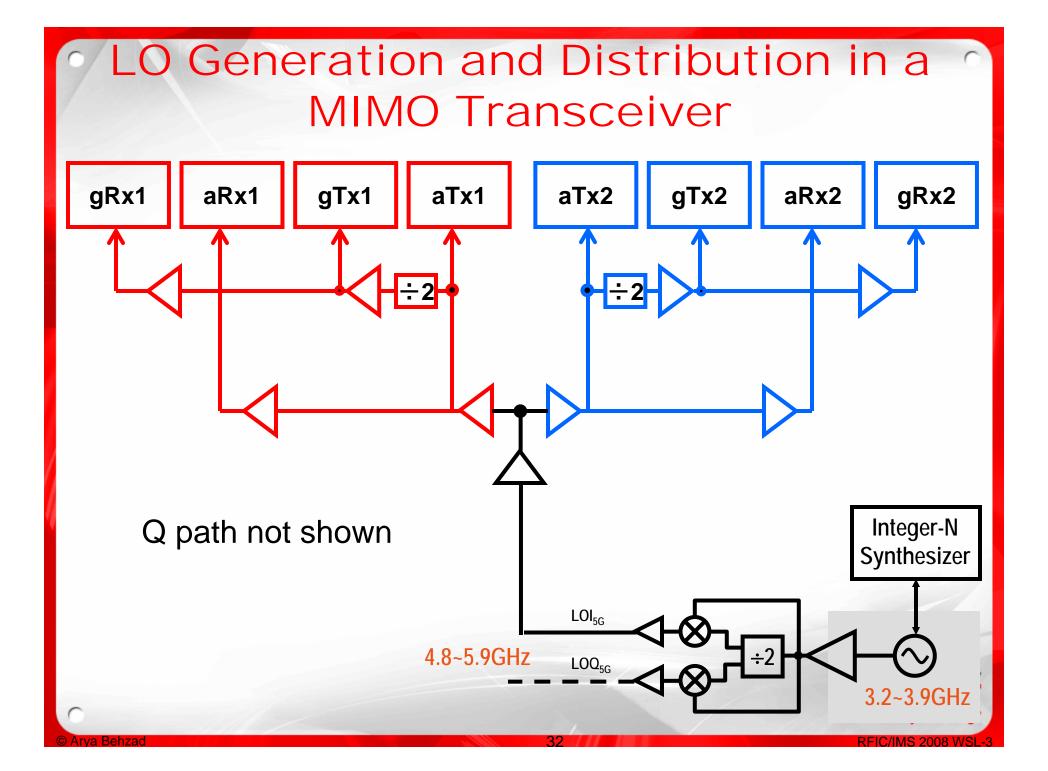


Before calibration

After calibration

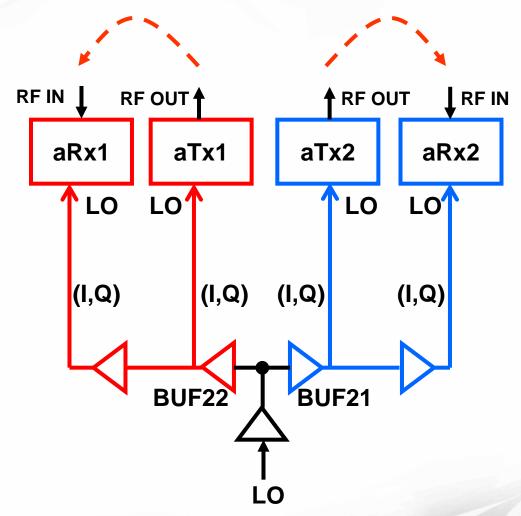
Ref: I. Bouras, et al, ISSCC 2003





Rx IQ Calibration—Same Core Method

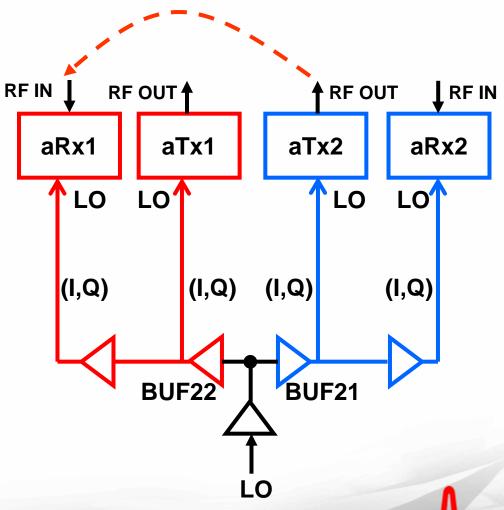
- After Tx IQ has been calibrated, a SSB test tone is transmitted and coupled to the Rx input
- The downconverted I and Q signals at Rx BB are used to calibrate the Rx LO I and Q in digital BB
- Tx1 output is used to calibrate Rx1 and Tx2 output is used to calibrate Rx2



- The problem is that the loading of BUF21 (BUF22) is different during calibration with normal Rx operation
- Post-calibration image rejection can be limited to ~-35dBc

Rx IQ Calibration—Cross Core Method

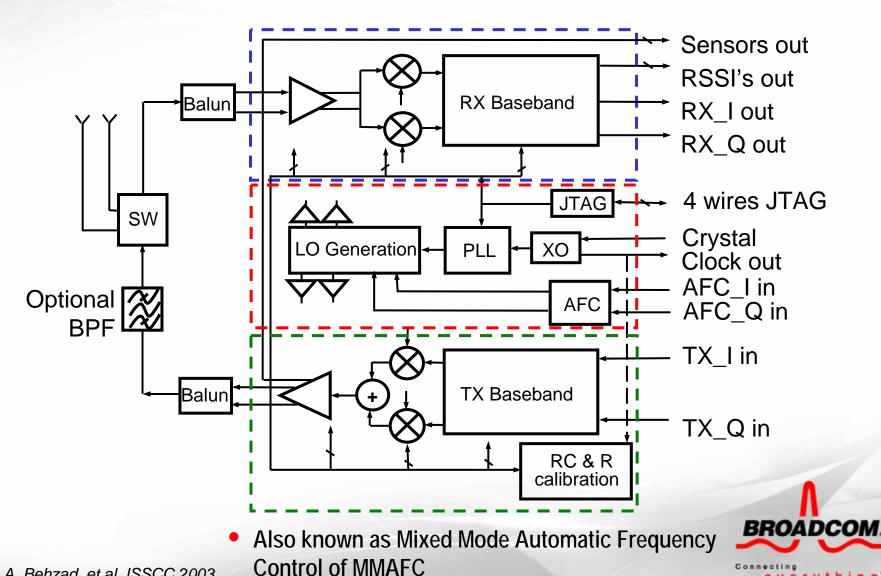
- Instead, couple calibrated Tx2 output to Rx1 input, with Tx1 OFF during calibration
- Loading of BUF22 is now the same during calibration and normal Rx operation
- Repeat the procedure with Tx1 and Rx2 when done with (Tx2,Rx1)
- Post-calibration image rejection is better than < -50dBc



Ref: A. Behzad, et al, ISSCC 2007, JSSC 2007

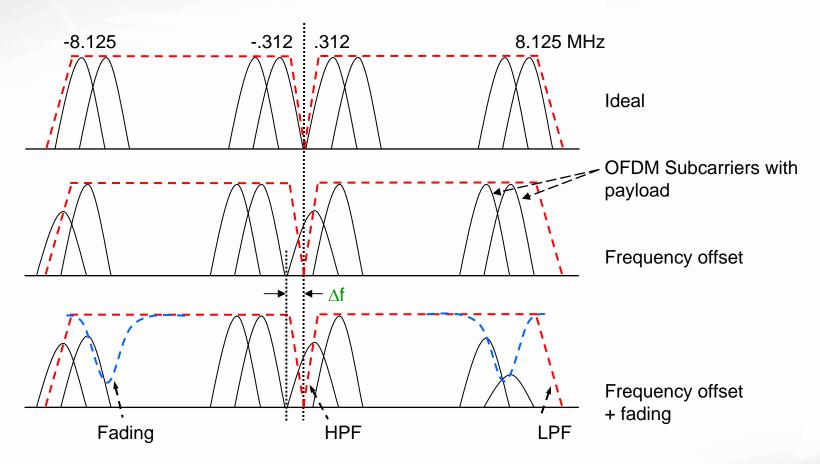


Transceiver with Agile Center Frequency Offset Correction (MMAFC)



Ref: A. Behzad, et al, ISSCC 2003

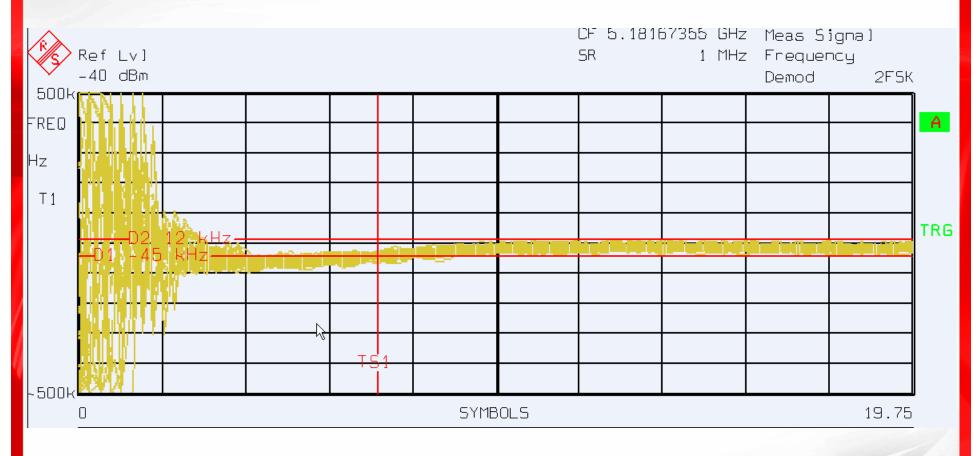
Need for Center Frequency Offset Correction



Standard requirement of 20PPM: 214KHz of frequency offset at 5.35GHz



PLL Frequency Adjustment



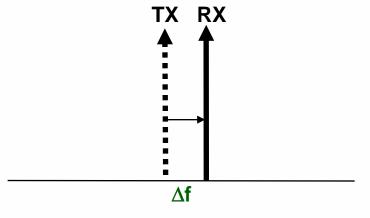
 Adjusting PLL frequency to correct for Crystal frequency error is not viable as the settling time would be too slow

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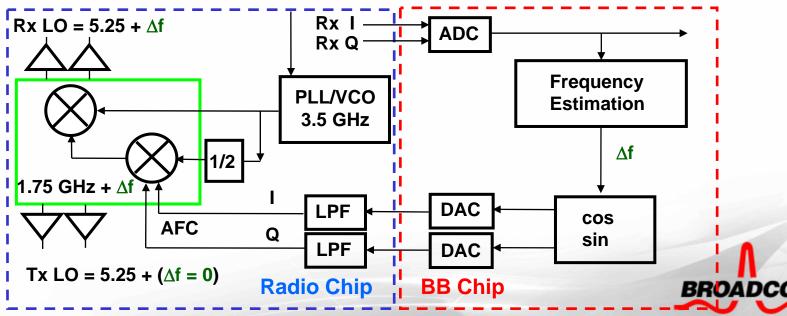
MMAFC Block Diagram

$$f_{LO_TX} = \frac{3}{2} \cdot f_{vco}$$

$$f_{LO_{-RX}} = \frac{3}{2} \cdot f_{vco} + \Delta f_{afc}$$



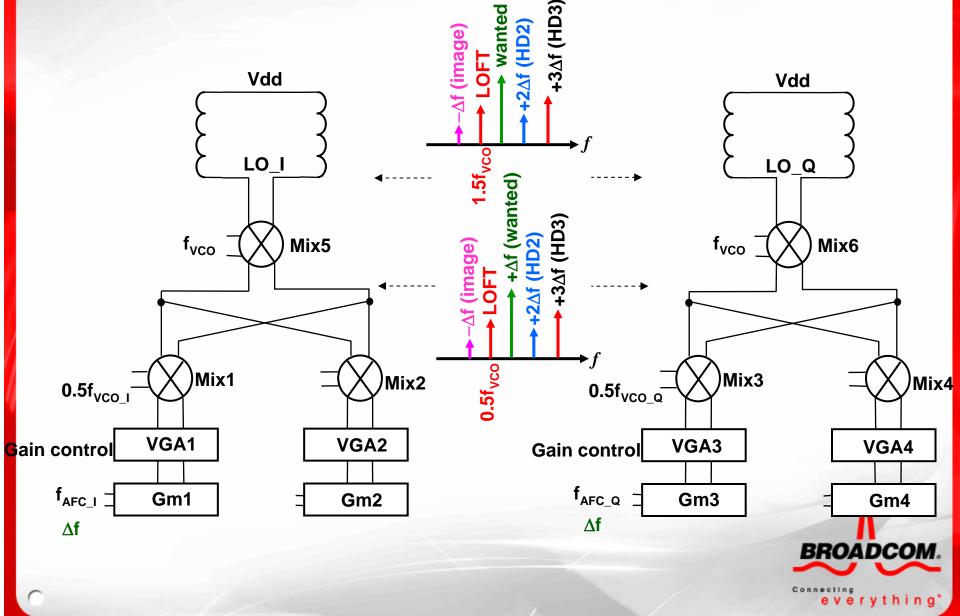
20 MHz Xtal



Ref: A. Behzad, et al, ISSCC 2003

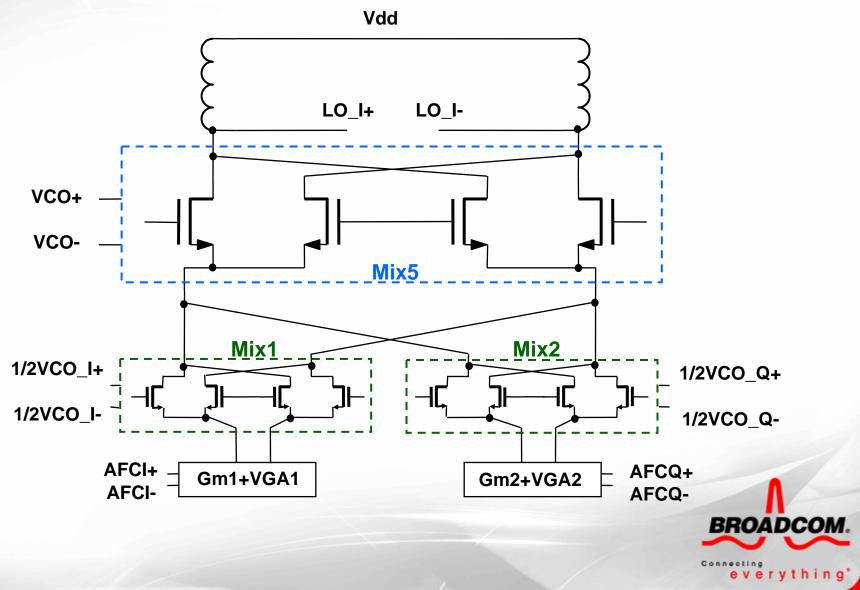
everything*

Block Diagram of LO Generation Mixers

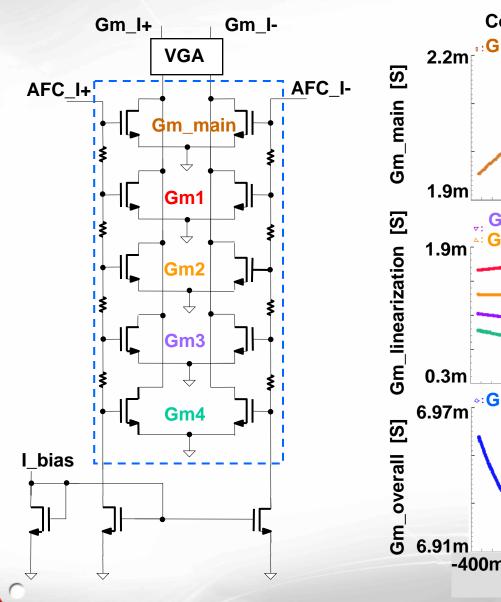


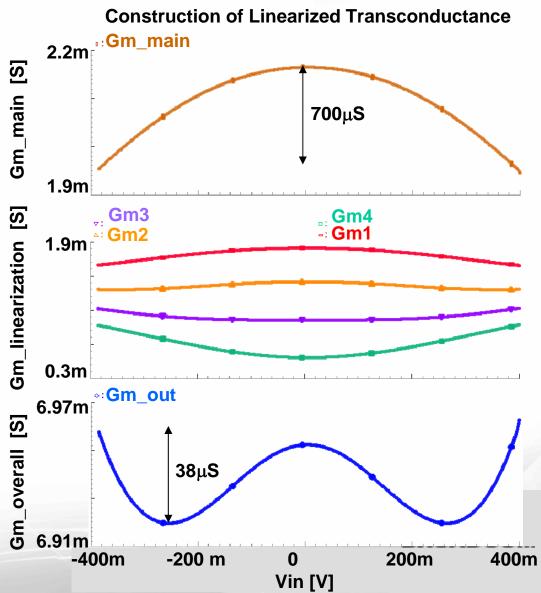
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Simplified Schematic of LO Generation Mixers

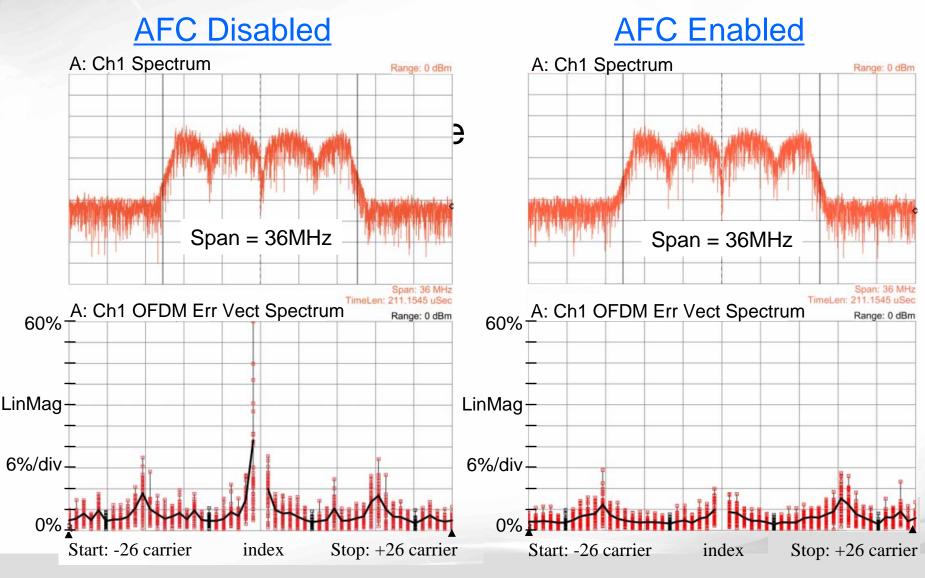


Multi-section Class AB Offset-Gm of MMAFC Mixer





MMAFC Performance

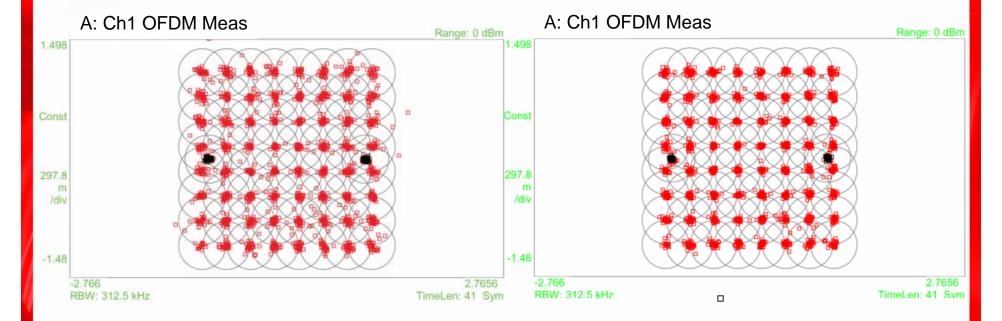


Multipath: 200ns, -2dB, 180deg; Frequency Offset: 200kHz

MMAFC Performance

AFC Disabled

AFC Enabled



Rx EVM Improved by 4.1dB

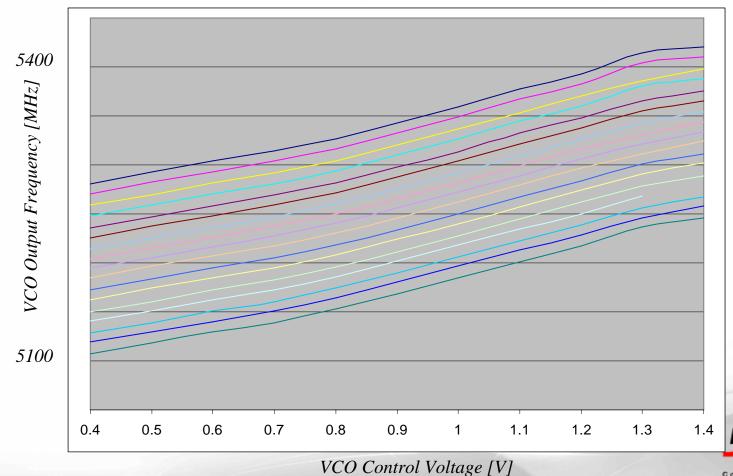


VCO Calibration

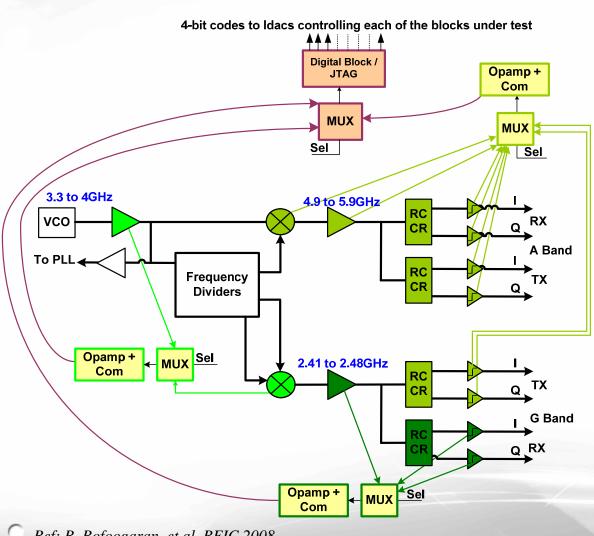
- Coverage over a wide frequency range is required for many standards
 - One way to achieve this is to design a VCO with a high gain factor (Kvco)
 - The problem with a high gain VCO is the sensitivity of the VCO to noise on the control line and the supplies, and hence often a poor phase noise
- An alternate method to achieve a wide tuning range while maintaining a low Kvco is to use banks of switch capacitors in the VCO
 - The switch capacitor setting sets the VCO to a frequency that is "close enough" and then the varactor is used in conjunction with the PLL to set the exact frequency
- Due to process, temperature and supply variations, it is not sufficient to set the switch capacitor banks for a required channel based on a a-priori programmed lookup table
 - It is essential to use an auto-calibration loop to ensure proper operation over PVT and to ensure the operation of the charge pump over a compliant voltage range
- The auto-calibration can be done wit the PLL in open-loop mode, closed-loop mode, or a combination of the two
 - Tradeoffs of calibration accuracy against calibration time need to be accounted for BROADCON

VCO Tuning Curves

VCO switch capacitor tuning curves covering the lower U.S. 802.11a band. The
calibration algorithm selects the optimal curve such that the VCO can operate at a
voltage around the middle of the charge pump compliance range.



Compact & Power Efficient LOGEN

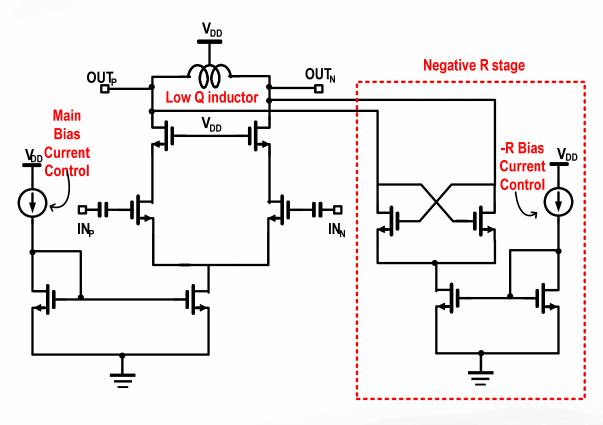


- Extensive calibrations are utilized in this compact and powerefficient LO generation subsystem
- Simplified block diagram shown



Ref: R. Rofoogaran, et al, RFIC 2008

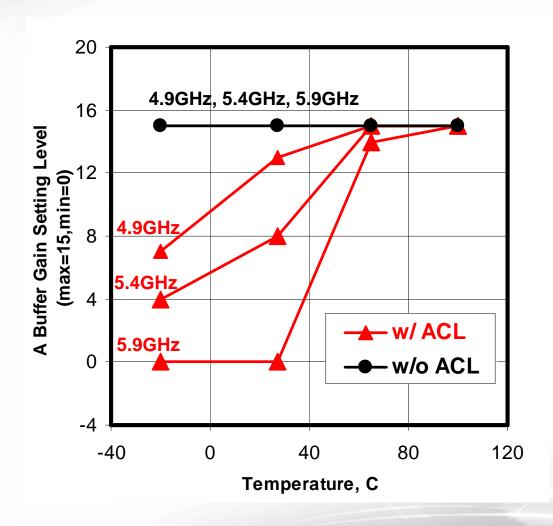
Gain-Boosted Inductively Loaded Stage



- Utilized in the various sections of the calibrated LOGEN sub-system
- Simplified schematic shown



Calibrated LOGEN Gain Setting Output



- Gain setting of a representative buffer with and without the amplitude control loop calibration
- With ACL, lower settings are achieved at colder temperatures corresponding to lower power consumption

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Resistor Calibration

- Often a constant on-chip current is required, where the current varies minimally with process parameters
- A fairly accurate and process independent voltage can be easily synthesized on chip by using a bandgap circuit. A constant current can be synthesized if this voltage is applied to a process-independent resistor
- Often the resistors utilized in a vanilla CMOS process have high variation
 - A calibration circuit is needed to compensate for this variation
- One method would be to generate the required current by applying the bandgap voltage on an external low tolerance resistor
 - This method would require one external resistor and one pin for each on chip calibrated current and is not efficient
- A better alternative is to use a state machine to equalize an on chip generated current (with a particular type of resistor) against the externally generated one, obtain the code, and then apply this code to all currents that require a constant current (and use the same type of resistor) on chip
 - Since the sheet resistance of a resistor is the primary contributor to the resistance variation, and since sheet resistance is fairly constant across the chip, this method obtains the desired outcome with one external resistor and one extra pin

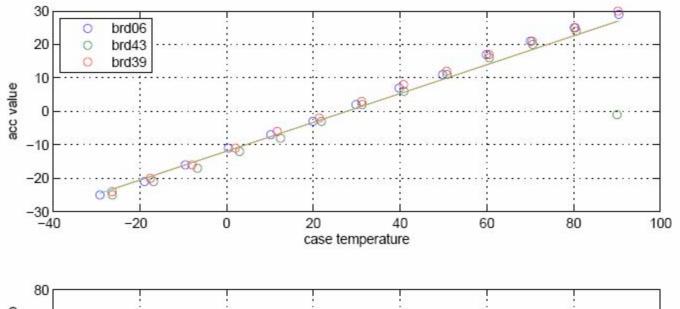
Filter Bandwidth Calibration

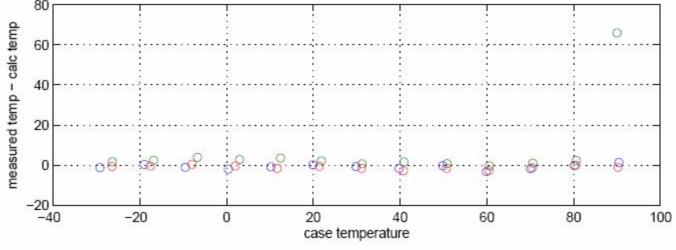
- Often a constant filter bandwidth is required for optimal pass-band response while providing proper ACI
- If we consider a opamp-RC type filter, for example, the bandwidth would vary with varying on chip R and on chip C values
- One (off-line) method to calibrate the bandwidth is to utilize a master-slave approach
 - An on-chip relaxation type RC-based oscillator synthesizes an approximate frequency
 - The counts from this oscillator are compared against that of a known accurate oscillator (such as a crystal oscillator)
 - The Rs or Cs of the relaxation oscillator are adjusted to achieve the desired count
 - The code for the adjusted R or C is obtained and then applied the filters which utilize the same type of Rs and Cs in their construction
- Other more sophisticated techniques also exist for filter calibrations



Highly Accurate Integrated Temp Sense

Can be utilized to adjust parameters that are subject to temperature variations



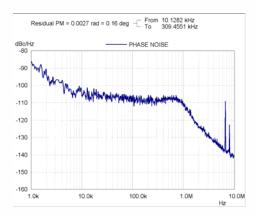


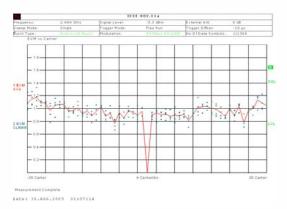


Calibrations Help Achieve Best-of-class Radio Performance

- Radio phase noise density and TX EVM is best of class (for all process technologies, not just CMOS)
 - Digital calibration is key!

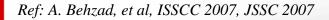
Measured PN at transmitter output (5.24GHz) Measured Tx EVM (Po=-2dBm; -41dB @ 2.484GHz)





TX Constellation (Po=-5dBm; EVM= -40dB @ 5.24GHz)

		1666.0	02.11a			
5.24 GHz Bignal Level:			-9.8 dBm Free Run			+ 45
Single	Trigger Mode					-10 pt
	Modulatio	on:			ta Symbols :	
rs Symbol				20.000	A1856115	
-	4-	+ +	+ +	-	+-	
-+-		+ +	+ +	+	+-	
+		+ +	+ +	+-	+	
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Conclusion

- We have only touched upon a few calibration techniques that are utilized today to achieve transceivers with outstanding performance, low cost, and high yield
- Many, many additional calibrations are possible and being applied to various transceivers
 - Transmit power calibrations
 - Temperature sensor based calibrations
 - Power amplifier linearizations and calibrations
 - LINC Amplifier based calibrations
 - Receiver IP3 and IP2 based calibrations
 - Polar transmitter one-point and two-point based calibrations
 - SWC/MRC based calibrations
 - Beam-former based calibrations
 - Pipeline ADC digital background calibrations



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