

EPITAXIAL SILICON TECHNOLOGY

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1986



ACADEMIC PRESS, INC.

Harcourt Brace Jovanovich, Publishers

Orlando San Diego New York Austin
Boston London Sydney Tokyo Toronto

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ACADEMIC PRESS, INC.

Orlando, Florida 32887

United Kingdom Edition published by
ACADEMIC PRESS INC. (LONDON) LTD.
24-28 Oval Road, London NW1 7DX

Library of Congress Cataloging in Publication Data

Epitaxial silicon technology.

Includes bibliographies and index.

Contents: Silicon vapor phase epitaxy / H. M. Liaw
and J. W. Rose — Silicon molecular beam epitaxy /
B. Jayant Baliga — [etc.]

1. Semiconductors—Design and construction.
2. Silicon crystals—Growth. 3. Epitaxy. I. Baliga,
B. Jayant, Date .

TK7871.85.E65 1986 621.3815'2 86-3524
ISBN 0-12-077120-9 (alk. paper)

PRINTED IN THE UNITED STATES OF AMERICA

86 87 88 89 9 8 7 6 5 4 3 2 1

PREFACE

Among process technologies, epitaxial growth of silicon represents a cornerstone upon which many device structures have been developed. Epitaxial layers have been used for the fabrication of integrated circuits and discrete devices. In the case of integrated circuits, although bulk CMOS became popular, the most recent trend is to return to epitaxial material to improve latch-up performance. In the case of discrete power devices, there has been a steady increase in the use of epitaxial material. In this case, when the device breakdown voltage falls below 2000 V, the thickness of the drift layer, and hence the wafer, becomes smaller than that which can be handled during manufacturing without breakage. This problem can be circumvented by growing the drift layer epitaxially on a thick substrate designed to meet the wafer handling requirements. As the demand for power devices grows due to new applications, an increase in the consumption of epitaxial silicon can clearly be foreseen.

The growth of epitaxial layers of silicon has been treated previously in books that deal with general process technology. In these cases, the focus is primarily upon vapor-phase epitaxy. The epitaxial growth of silicon by other techniques is relegated to reviews specializing in growth techniques, which include other semiconductor materials. The purpose of this book on silicon epitaxial technologies is to provide in a single volume an in-depth review of all the silicon epitaxial growth techniques.

The growth of epitaxial layers of silicon began over 20 years ago by employing chemical vapor deposition at atmospheric pressure using chlorosilanes. This technology has now diversified due to the development of molecular-beam and liquid-phase epitaxial techniques. In addition, even conventional vapor-phase epitaxy has been revolutionized by recently developed low-pressure deposition techniques. Further, this technology is being extended to the growth of epitaxial layers on insulating substrates by means of a variety of lateral seeding approaches. In spite of the widespread use of this technology and its vital importance to the semiconductor industry, no single book that provides an in-depth review of this subject has been published previously.

This book is organized into five chapters. In the first chapter, the growth of silicon layers by vapor-phase epitaxy is discussed. Both atmospheric and low-pressure growth are considered. This is the most widespread technology in use today by the semiconductor industry. The second chapter discusses molecular-beam epitaxial growth of silicon. Although molecular-beam epitaxy has been used extensively for the growth of compound semiconductors, its application to the growth of silicon layers is more recent. This approach provides a unique ability to grow very thin layers with precisely controlled doping characteristics. In the third chapter, the reader is introduced to silicon liquid-phase epitaxy. Again, this approach to epitaxial growth was originally developed for compound semiconductors. The incentives to apply liquid-phase epitaxy to the growth of silicon layers arose from a desire to decrease the growth temperature and to suppress autodoping. The fourth chapter addresses the growth of silicon on sapphire. This technology has been pursued for improving the radiation hardness of CMOS integrated circuits. In the fifth chapter, the most recent and novel advances in the application of silicon epitaxial growth are discussed. This chapter deals with the formation of epitaxial layers of silicon on insulators, such as silicon dioxide, which do not provide a natural single crystal surface for growth.

In the preparation of the book, a special effort has been made to provide a uniform treatment by maintaining a common format among the chapters. Each chapter begins with a discussion of the fundamental transport mechanisms and the kinetics governing the growth rate. Since the quality of the silicon surface is crucial to device fabrication, the importance of the influence of the growth conditions upon epitaxial layer morphology is also treated here. This is followed by a description of the electrical properties that can be achieved in the layers and the restrictions imposed by the growth technique upon the control over its electrical characteristics. Each chapter concludes with a discussion of the applications of the particular growth technique. This is an important segment of the book because, although vapor-phase epitaxial growth is the dominant technology in use today, each of the other growth techniques offers unique features which may be particularly attractive for a specific application.

I would like to take this opportunity to thank each of the authors of the chapters in this volume for the timely preparation of their contributions and for adhering to the guidelines set for them. I am grateful to Dr. J. Pankove for his suggestion to prepare the book. I would also like to acknowledge the generosity of the General Electric Company in conferring upon me the Coolidge Fellowship award, which gave me the time for the preparation of this volume. I hope that the book will be useful not only to process technologists but also to engineers who may need to apply epitaxial growth for device fabrication.

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SILICON VAPOR-PHASE EPITAXY

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1.1 INTRODUCTION

The vapor-phase epitaxial growth of silicon can be classified into two categories: (1) growth by evaporation and (2) growth by chemical vapor deposition (CVD). The former technique involves evaporation of silicon by an electron gun in an "effusion" cell. Silicon vapor is introduced into an ultrahigh-vacuum growth chamber by opening a mechanical shutter. The epitaxial growth occurs when the silicon vapor impinges on the heated silicon substrate. This technique is also referred to as molecular-beam epitaxy and is the subject of a separate chapter of this book. The latter technique involves chemical reactions induced by thermal energy with or without assistance of plasma or photo energies for reaction enhancement. Silicon epitaxial growth by thermally induced CVD has been used by the industry for the production of epitaxial silicon wafers for over two decades. The primary reason for the popularity of this technique is the ease by which it can be scaled. It is also the most versatile technique in terms of the range of epitaxial thicknesses and types of impurity doping obtainable. It seems that this technology is somewhat mature. However, we believe that it will continue to be the most vital epitaxial growth technique in the industry for the next one or two decades by further process innovation and reactor automation.

The CVD method for epitaxial growth is perhaps the most complex when compared to the other techniques. The complexity of this method

arises from the fact that (1) it generally includes multicomponent species in the chemical reactions, (2) the chemical reactions may produce certain intermediate products, (3) the growth process has numerous independent variables, and (4) the deposition process includes many consecutive steps. It is the purpose of this review chapter to provide some insight for understanding CVD growth, to focus on the practical aspects, and to review the key areas of the technology which could affect the properties of epitaxial materials that are used for the fabrication of semiconductor devices.

The CVD epitaxial growth starts with the selection of a silicon-containing gas and its chemical reactions. The conditions under which the silicon deposition will occur can be predicted by thermodynamic analysis of the system. The types of chemical reactions that can lead to silicon epitaxial growth will be reviewed. The thermodynamic data and needed procedures for the calculation of equilibrium partial pressure of gas species in a given silicon system will be illustrated. From the equilibrium partial pressure, the concept of silicon solubility in the gas phase will be presented. The supersaturation similar to that used in liquid-phase epitaxial growth can be derived.

The CVD process involves the transport of chemical species from the gas phase onto the substrate surfaces. In an open tube reactor, in which the gas mixture enters from one end of the reactor and exits at the other end, a boundary layer exists between the gas stream and the substrate surfaces. We will review the boundary layer theory. The thickness of the boundary layer is an important factor determining the mass transfer rate. During the process of mass transport the chemical reactions occur either in the gas phase or on the substrate surface. Where the reactions take place determines if the nucleation is homogeneous or heterogeneous. It will be shown that epitaxial growth requires heterogeneous nucleation. Heterogeneous nucleation may include surface reactions in which the incoming gas species and the intermediate products due to the chemical reactions are adsorbed on the surface and subsequently diffuse to energetically favorable sites for the incorporation of silicon atoms into the crystal lattice. Therefore, the deposition process can be divided into two main steps: (1) gas diffusion through the boundary layer followed by (2) surface reaction. A dimensionless number will be introduced. The magnitude of which can be used to characterize if the overall process is diffusion-controlled or reaction-controlled. The silicon deposition rate equations will be derived based on the rate-limiting step.

The most significant progress that has been made in CVD epitaxial technology over the last two decades is in the areas of reactor evolution and process innovation. A review of these two subjects is also included in this chapter. This progress has resulted in the capability of producing high-

quality epitaxial wafers. The quality standard has been and will be raised as silicon devices continue to evolve to a higher degree of integration.

The surface morphology, crystallographic defects, control of the dopant distribution in the epitaxial layer, and epitaxial layer thickness are some of the important parameters that can affect the device performance and manufacturing yields. Discussion of the causes of poor surface morphology and generation of epitaxial defects will be presented. The techniques for measuring epitaxial thickness and dopant distribution will also be given.

Certain unique features of the CVD epitaxial growth technique will be presented. Examples of such features include the possibility of near-equilibrium growth, reversed growth, and choice of numerous chemical reactions for silicon deposition. Selective area deposition of silicon becomes possible by near-equilibrium growth techniques. The *in-situ* etching of silicon wafers is performed by utilizing the feature of reversed growth. The numerous chemical reactions that are available provide a wide temperature range for epitaxial growth. Utilization of these features can produce specific properties in the epitaxial films for various device applications.

Silicon devices can be built either directly on the silicon substrates or on the epitaxial layers. As it is today, bipolar devices are exclusively built on epitaxial layers while MOS devices primarily use substrates only. High-speed bipolar integrated circuits require a low-resistivity subcollector region which also serves as an electrical isolation from the substrate. This has been accomplished by using a heavily doped *n*-type buried layer either by diffusion or by ion implantation into the *p*-type substrate followed by the epitaxial growth of an *n*-type silicon layer. As scaled-down dimensions in MOS devices continue, the electrical noise generated in the substrate becomes intolerable (Matsunaga *et al.*, 1980), and CMOS devices become very susceptible to latch up. These problems can be easily reduced or eliminated when a thin epitaxial layer is deposited on a heavily doped substrate (Payne *et al.*, 1980). It is predicted that epitaxial silicon will be increasingly used in the MOS devices. Conversion to epitaxial wafers has been resisted due to the increased wafer cost by approximately a factor of two. Furthermore, the substrates are grown from the melt at a higher temperature than the epitaxial growth temperature. This results in superior crystal perfection. Polishing of the substrates also results in fewer surface defects. However, there are other disadvantages that exist in the substrates that are grown by the Czochralski method, in which a silicon ingot is pulled from a melt in a quartz crucible. The Czochralski silicon contains nonintentionally doped impurities such as oxygen and carbon. These impurities are undesirable if they exist in the active regions of the devices, although a limited amount of oxygen in the bulk region of the wafers is beneficial.

for intrinsic gettering. A low oxygen content ($1\text{--}3 \times 10^{16}$ atoms/cm³ as compared to $5\text{--}20 \times 10^{17}$ atoms/cm³ in the Czochralski silicon) at the surface of silicon wafers is desirable and can be easily provided by epitaxial growth (Suzuki *et al.*, 1973). Resistivity of the bulk silicon grown by the Czochralski method is limited to 100 ohm cm or less because of the existence of oxygen donors and other impurities resulting from the erosion of the quartz crucible. Oxygen donors are totally eliminated in epitaxial layers. The upper resistivity of epitaxial silicon is only limited by the autodoping from the epitaxial reactors.

The main advantage of epitaxial wafers over non-epitaxial material is the capability of adjusting the dopant profile in the vertical direction. Ion implantation is also capable of doing that. Recent advances in the high-energy ion implantation technique are in direct competition with epitaxy technology. However, the surface damage and contaminants resulting from a high dosage of ion implantation may limit its ability to produce device-quality n/n^+ or p/p^+ silicon layers.

We foresee that in the next two decades the development of the CVD epitaxial growth technique will continue to focus on reactor design aimed at the improvement of production throughput. A high degree of process automation is one of the key ingredients for cost effectiveness. We also foresee that continued process innovation in epitaxial growth will provide unique material structures which cannot be obtained by other means.

1.2 CHEMICAL VAPOR DEPOSITION

The chemical vapor deposition of epitaxial silicon can be classified into three basic types of reactions: (1) disproportionation, (2) reduction, and (3) pyrolysis. Each method has its advantages and disadvantages.

1.2.1 Growth by Disproportionation

The disproportionation reaction involves the dissociation of divalent halides, SiX_2 , into solid silicon and a four-valence silicon halide, SiX_4 , in vapor form:



Equation (1.2.1) is applicable for SiI_2 , SiCl_2 , SiBr_2 , and SiF_2 , although SiI_2 is most commonly used. Even though SiI_2 cannot exist as an isolated compound, it can be generated by passing iodine vapor over a heated silicon charge (1150°C) placed at the source region of reaction chamber according to the reactions:



The generated SiI_2 is transported to a cooler part of the chamber (900°C), and the reverse reaction of Eq. (1.2.3) will occur. Thus silicon is deposited at the cooler region of the reaction chamber. When a single-crystal silicon substrate is placed in the disproportionation region, a single-crystal epitaxial film will be obtained.

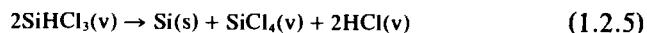
Utilization of this technique for epitaxial silicon growth was reported by May (1965), Glang and Wajda (1963), Taft (1971), Gosch (1980), and Hanssen *et al.*, (1983). Considerable interest has been shown in this technique since epitaxial growth takes place at low temperature, low pressure, and near equilibrium conditions. When the epitaxial growth process occurs at a low temperature and low pressure, a sharp doping transition from a heavily doped substrate to a lightly doped layer can be obtained. The near-equilibrium growth prevents the nucleation of silicon on foreign substrates. Therefore, this technique is ideal for the selective epitaxial growth of silicon. One of the disadvantages of this technique is the necessity of using a closed system. Operation of the closed tube is not flexible for introduction of dopants into the growth system. Therefore, this technique has not been widely used for the production of epitaxial silicon by the industry.

1.2.2 Growth by the Reduction of Chlorosilanes

Reduction of chlorosilanes is characterized by a positive heat of reaction. A high temperature is needed for the reactions to occur. These reactions are reversible. The degree of reversibility increases with the chlorine content in the chlorosilane. Hydrogen is generally used as the reducing agent and the carrier gas. High-purity trichlorosilane is readily available, and thousands of metric tons are produced annually for the semiconductor industry. Its main use is as feedstock for the production of polycrystalline silicon ingots. The polycrystalline silicon ingots are used as raw material for the melt growth of silicon single crystals. Trichlorosilane is also used for epitaxial silicon production. The chemical reaction is identical whether for polycrystalline or for the epitaxial growth. An oversimplification of the reaction is often expressed as



In reality the end products of the reaction are silicon and large quantities of both silicon tetrachloride and HCl. Perhaps the following equation is a more accurate representation of the reaction:



Silicon tetrachloride produced as a by-product of the polysilicon process can be purified and is available in large quantities at low cost. Therefore,

it has been used extensively as the silicon source for the growth of epitaxial silicon. The reduction of silicon tetrachloride can be expressed as



One of the drawbacks of this reaction is that a high temperature (typically 1150–1300°C) is required to produce high-quality layers. Both SiCl_4 and SiHCl_3 are liquids at room temperature. Therefore, a carrier gas is normally used to transport the silicon compound to the reactor. This is done by bubbling a gas such as H_2 through a SiCl_4 or SiHCl_3 reservoir. The temperature and pressure of the reservoir determine the volume ratio of the chlorosilane to the hydrogen carrier gas. To maintain a constant growth rate the volume ratio must remain constant. Table 1 lists the boiling and melting points of silicon compounds normally used to deposit epitaxial silicon. Figure 1 is a plot of vapor pressure for SiHCl_3 and SiCl_4 versus temperature.

One of the problems with using SiCl_4 and SiHCl_3 is maintaining a constant temperature. As hydrogen is bubbled through the liquid, the liquid is cooled by evaporation. This cooling lowers the vapor pressure of the liquid and reduces the volume ratio of silicon source gas to hydrogen. One method of maintaining a constant ratio is to maintain a constant evaporation rate of the silicon source liquid using the principle of the ideal gas law (i.e., $n = PV/RT$). Figure 2 shows the schematic diagram of this control unit (Rose, 1985). This system monitors the temperature of the silicon source liquid and then automatically adjusts the pressure in the bubbler to maintain a constant ratio of P/T . For example, as the temperature of the liquid is cooled, the pressure in the bubbler is decreased. The adjustment of pressure with temperature is to maintain a constant n . Growth rate variations from run to run and during a run are controlled to less than $\pm 2\%$ by using this method.

High-purity SiH_2Cl_2 was not available in large quantities until the early 1970s. Even now it is not extensively used because of its high cost. Since the reduction of SiH_2Cl_2 occurs at a lower temperature than SiHCl_3 or

TABLE 1. Boiling Points and Melting Points of Silane and Chlorosilanes

Compound	Phase	bp (°C)	mp (°C)
SiH_4	Gas	-112	-185
SiH_2Cl_2	Gas	8.3	-122
SiHCl_3	Liquid	31.8	-127
SiCl_4	Liquid	57.6	-68

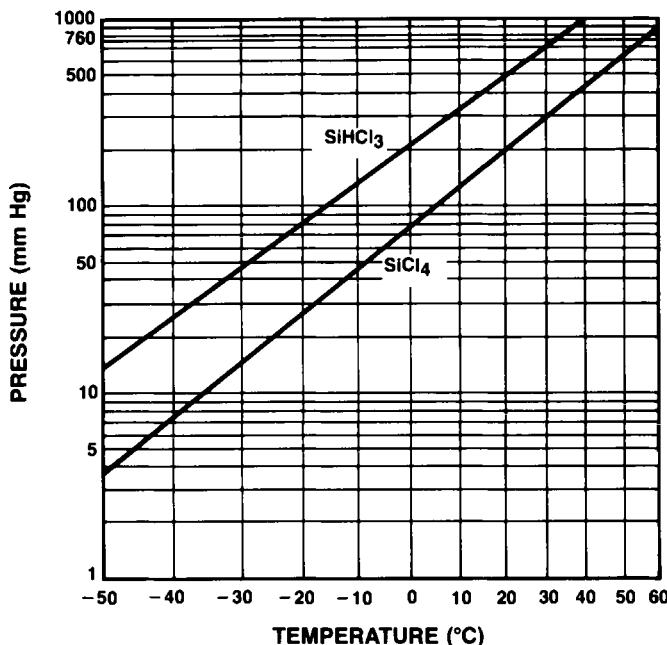


FIG. 1. Vapor pressures of SiHCl_3 and SiCl_4 as a function of temperature. [From Bloem and Giling (1978). Reprinted with permission of North-Holland Publishing Co., Amsterdam.]

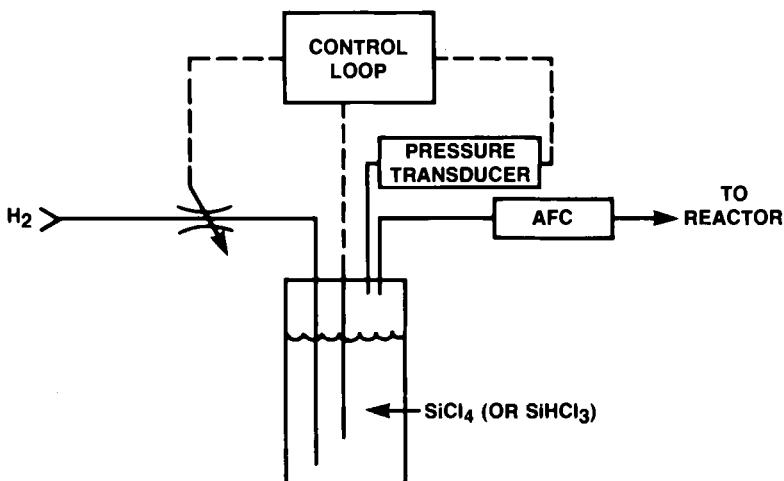
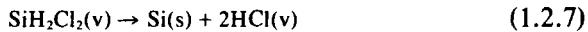


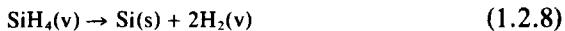
FIG. 2. Block diagram showing a method for maintaining a constant ratio of silicon source gas to hydrogen. [From Rose (1985). Courtesy of Motorola, Inc., Semiconductor Products Sector.]

SiCl_4 , it has gained popularity because impurity outdiffusion can be minimized. Low-temperature processing also minimizes thermally induced slip. Although H_2 is used as a “carrier gas” to dilute SiH_2Cl_2 , the actual reaction does not include H_2 :



1.2.3 Growth by Pyrolytic Decomposition

Deposition of silicon can be obtained by pyrolytic decomposition of SiI_4 or SiH_4 . Herrick and Krieble (1960) have studied the pyrolytic breakdown of SiI_4 for producing semiconductor-grade polycrystalline silicon. The pyrolysis of silane for silicon epitaxial growth was pioneered by Joyce and Bradley (1963). The reaction products are solid silicon together with hydrogen:



The reaction is not reversible and can occur at temperatures as low as 600°C for the polycrystalline silicon deposition and 850°C for the epitaxial silicon growth. Silane is used as a silicon source when low-temperature processing is required. It is also attractive for the high growth rate of polysilicon (>20 $\mu\text{m}/\text{min}$) when the deposition temperature is at 1240°C or higher. High growth rates of silicon epitaxy up to 40 $\mu\text{m}/\text{min}$ can also be obtained by introducing HCl in SiH_4 to suppress Si nucleation in the gas phase (Bloem, 1973). Extensive studies of the pyrolytic decomposition of SiH_4 have been made in the laboratory. Silane is well adapted for heteroepitaxial growth such as silicon on sapphire, where low-temperature growth is required to minimize the outdiffusion of aluminum. Chlorosilanes are still preferable for homoepitaxial growth. The primary reason is that pyrolysis occurs homogeneously in the gas phase when the gas temperatures exceed 400°C. Polycrystalline silicon is also deposited on the reactor walls. This reduces the productivity of the reactors because frequent cleaning is required.

1.2.4 Thermodynamic Consideration

The equilibrium partial pressure is one of the most important thermodynamic parameters for the study of a CVD process. In a simple CVD process, such as pyrolytic decomposition of silane, the process can be described by a single reaction. The equilibrium partial pressure of the system can be easily calculated from the rate constant of the reaction. Reduction of a chlorosilane by hydrogen involves many chemical reactions. Evaluation of the equilibrium partial pressures of the system can provide information on the relative proportion of each species present in an epitaxial system if the system is permitted to reach equilibrium. The

sum of the equilibrium partial pressures of all silicon-containing gases in the system under a given set of conditions (e.g., temperature, pressure, and Cl/H ratio) is referred to as the solubility of silicon in the gas phase (Bloem *et al.*, 1983). The concept of supersaturation which has been widely used in analyzing liquid-phase growth can also be used in CVD growth. The supersaturation is defined as the difference between the partial pressure of the input chlorosilane and silicon solubility in the gas phase. Thus, the equilibrium partial pressures can be used to determine a suitable concentration (or partial pressure) of the input silicon-containing gas to yield the desired results. The amount of supersaturation provides some clues about the kinetics and morphology of deposition. For example, if the supersaturation is high, the deposition rate will be high, and the deposited film will likely be polycrystalline.

Two approaches have been used to calculate the equilibrium partial pressures. The first method uses the approach of minimizing the free energy of a system by a computer iterative technique. Hunt and Sirtl (1972, 1973) have used the computer program described by Cruise (1964) for the calculation of equilibrium partial pressure in the Si-H-Cl, Si-H-Br, and Si-H-I systems. Herrick and Sanchez-Martinez (1984) have used the program provided by Gordon and McBride (1976) to calculate equilibrium partial pressure, equilibrium conversion of the reactions, and silicon deposition yields in the Si-H-Cl system. The method requires the input of all the gas species which may be present in the system, together with the standard enthalpy of formation, standard entropy, and temperature function of the heat capacity for each species in the system. Table 2 lists the

TABLE 2. Equilibrium Partial Pressures of Vapor Species in the Si-H-Cl System^a

Vapor species	1000 K	1200 K	1400 K	1600 K	
H ₂	9.30×10^{-1}	9.38×10^{-1}	9.18×10^{-1}	8.81×10^{-1}	
HCl	1.07×10^{-2}	8.19×10^{-3}	3.97×10^{-2}	8.63×10^{-2}	
SiCl ₄	3.03×10^{-2}	2.43×10^{-2}	2.44×10^{-2}	1.22×10^{-2}	
SiHCl ₃	1.88×10^{-2}	2.76×10^{-2}	1.54×10^{-2}	8.89×10^{-3}	
SiH ₂ Cl ₂	1.43×10^{-3}	8.87×10^{-4}	1.37×10^{-3}	1.03×10^{-3}	
SiH ₃ Cl	5.33×10^{-5}	1.80×10^{-5}	6.23×10^{-5}	5.88×10^{-5}	
SiH ₄	5.70×10^{-7}	3.72×10^{-7}	8.02×10^{-7}	9.77×10^{-7}	
SiCl ₂	6.62×10^{-5}	1.23×10^{-4}	1.53×10^{-3}	1.10×10^{-2}	
SiCl ₃	—	3.53×10^{-4}	—	4.38×10^{-2}	
Reference	Ban and Gilbert (1975)	Herrick and Sanchez-Martinez (1984)	Ban and Gilbert (1975)	Ban and Gilbert (1975)	Herrick and Sanchez-Martinez (1984)

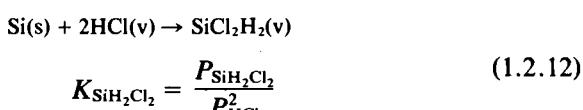
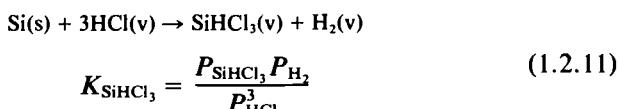
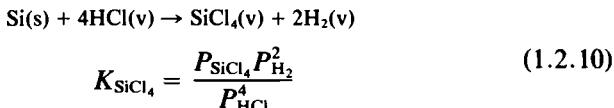
^aPressures given in atmospheres; system total pressure = 1 atm and Cl/H ratio = 0.1.

calculated equilibrium partial pressure of vapor species in the Si–H–Cl system for total pressure of 1 atm and Cl/H ratio of 0.1 (Ban and Gilbert, 1975; Herrick and Sanchez-Martinez, 1984). Notice that at low temperatures when no silicon is deposited, SiCl_4 and SiHCl_3 are the predominant species, and at high temperatures when a large quantity of silicon can be deposited, SiCl_2 and SiCl_3 become predominant species. Hence, the formation of SiCl_2 and SiCl_3 are thought to be important intermediate products for silicon deposition and epitaxial growth.

The second method of calculation requires knowledge of the predominant species in the system. These species are then used for writing a set of chemical equations to describe the system. Equations that relate the equilibrium constant (K) to equilibrium partial pressure of each species occurring in the reaction are formulated. The equilibrium constant of each equation can be calculated from the standard free energy of formation (ΔF):

$$\Delta F = (\Delta H - T \Delta S) = -RT \ln K \quad (1.2.9)$$

where ΔH is enthalpy of formation, T the absolute temperature, ΔS the entropy of formation, and R the gas constant. Ban and Gilbert (1975), and Arizumi (1975) used this method to calculate the equilibrium partial pressures in the Si–H–Cl system. The Si–H–Cl system is applicable for a silicon epitaxial growth process using SiH_2Cl_2 , SiHCl_3 , or SiCl_4 as silicon source gas. The following illustrates the procedures for calculating the equilibrium partial pressures in the Si–H–Cl system. The first step is to identify the most abundant gas-phase species in the system. This can be done experimentally by measuring the gas-phase species by mass spectrometry or other analytical means. The predominant species are H_2 , HCl , SiH_2Cl_2 , SiHCl_3 , SiCl_4 , SiCl_2 , SiH_4 , and SiH_3Cl . The following six equations describe the chemical reactions of these species. Their corresponding equations of the reaction rate constants are also given:

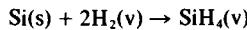




$$K_{\text{SiH}_3\text{Cl}} = \frac{P_{\text{SiH}_3\text{Cl}}}{P_{\text{HCl}} P_{\text{H}_2}} \quad (1.2.13)$$



$$K_{\text{SiCl}_2} = \frac{P_{\text{SiCl}_2} P_{\text{H}_2}}{P_{\text{HCl}}^2} \quad (1.2.14)$$



$$K_{\text{SiH}_4} = \frac{P_{\text{SiH}_4}}{P_{\text{H}_2}^2} \quad (1.2.15)$$

The reaction equilibrium constants of Eqs. (1.2.10)–(1.2.15) can be calculated from ΔF which in turn can be calculated from ΔS and ΔH using Eq. (1.2.9). Figure 3 shows a plot of ΔF versus temperature, which was originally evaluated by Hunt and Sirtl (1972) and plotted by Ban and Gilbert (1975). In order to solve the equilibrium partial pressures of the eight species involved in these six equations [Eqs. (1.2.10)–(1.2.15)], two more equations are needed. We can set the total pressure of the system equal to 1 atm for atmospheric growth. The total pressure is the sum of the partial pressures of all gas components:

$$P_{\text{SiCl}_4} + P_{\text{SiHCl}_3} + P_{\text{SiH}_2\text{Cl}_2} + P_{\text{SiH}_3\text{Cl}} + P_{\text{SiCl}_2} + P_{\text{SiH}_4} + P_{\text{HCl}} + P_{\text{H}_2} = 1 \quad (1.2.16)$$

We can also add the partial pressures of all chlorine compounds and designate the sum as the partial pressure of chlorine (P_{Cl}). By the same token, the partial pressure of hydrogen (P_{H}) is the sum of the partial pressures of pure hydrogen and the hydrogen compounds. Thus the Cl/H ratio can be expressed as

$$\text{Cl/H} = \frac{4P_{\text{SiCl}_4} + 3P_{\text{SiHCl}_3} + 2P_{\text{SiH}_2\text{Cl}_2} + 2P_{\text{SiCl}_2} + P_{\text{SiH}_3\text{Cl}} + P_{\text{HCl}}}{2P_{\text{H}_2} + P_{\text{SiHCl}_3} + 2P_{\text{SiH}_2\text{Cl}_2} + 3P_{\text{SiH}_3\text{Cl}} + P_{\text{HCl}} + 4P_{\text{SiH}_4}} \quad (1.2.17)$$

Equilibrium partial pressures of the vapor species can now be solved numerically using Eqs. (1.2.10)–(1.2.17) for a specific temperature and the Cl/H ratio. Actual equilibrium partial pressures were also measured experimentally by Ban and Gilbert (1975) using SiH_2Cl_2 as an input gas. The measured and calculated results were of the same order of magnitude. The deviations observed in the results are explained by the non-equilibrium nature of the epitaxial system. Nevertheless, the equilibrium calculation provides information on the composition of the vapor phase in the system.

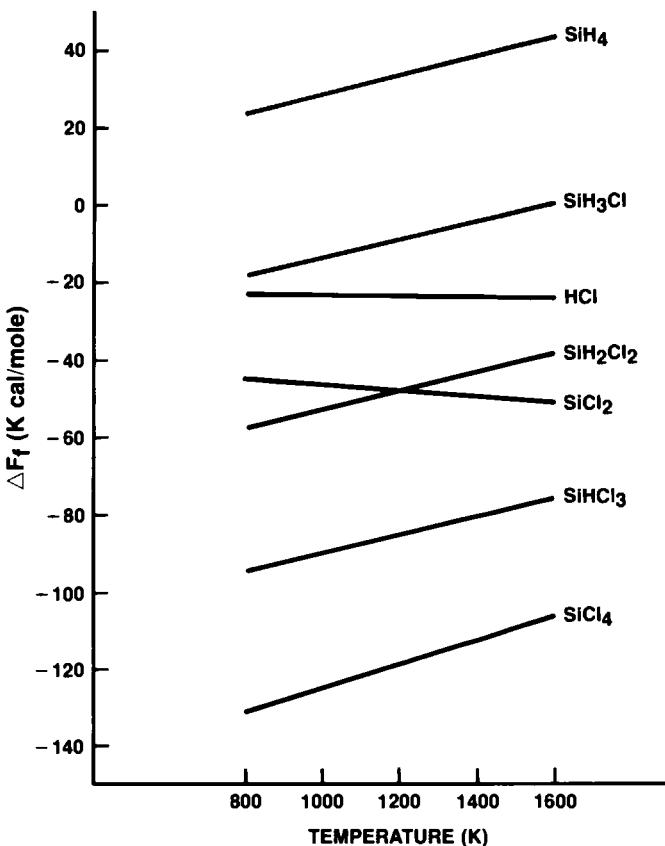


FIG. 3. Free energy of formation of important gas species in the Si-H-Cl system in the temperature range of 800–1600 K. [From Ban and Gilbert (1975). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

The equilibrium partial pressures of the vapor species were also calculated by van der Putte *et al.* (1975) using SiCl_4 as an input gas in the Si-H-Cl system. The 14 vapor-phase species used in their calculation were SiCl , SiCl_2 , SiCl_3 , SiCl_4 , SiH , SiH_4 , SiHCl_3 , SiH_2Cl_2 , SiH_3Cl , Cl , Cl_2 , H , H_2 , and HCl . The results of their calculations are shown in Fig. 4, which plots the equilibrium partial pressures of gas species as a function of the SiCl_4 input concentration at 1500 K. The equilibrium vapor pressures as a function of temperature were given by Bloem *et al.* (1983) and are shown in Fig. 5 for total pressure of 1 atm and the Cl/H ratio of 0.06.

As mentioned earlier, the solubility P_{Si} of silicon in the vapor phase is the sum of equilibrium partial pressures of all silicon containing gas. The general expression of the solubility is (Gilling, 1983)

$$P_{\text{Si}} = \sum_i NP_i(\text{Si}_x\text{H}_y\text{Cl}_z) \quad (1.2.18)$$

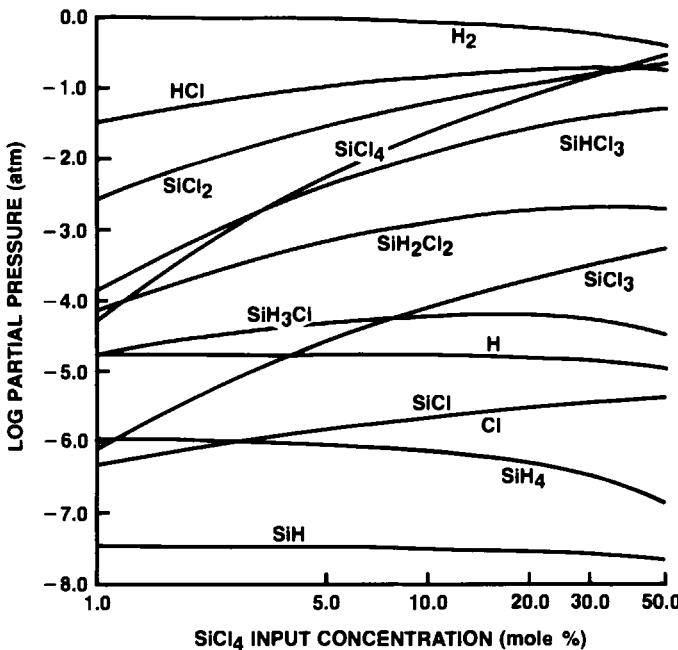


FIG. 4. Computed equilibrium partial pressures (atm) of various components in the Si-H-Cl system as a function of the SiCl_4 input concentration at 1500 K. [From van den Putte *et al.* (1975). Reprinted with permission of North-Holland Publishing Co., Amsterdam.]

where P_i is equilibrium partial pressure of a silicon containing gas, and N is the number of silicon atoms in that component. P_{Si} in the system analyzed by Bloem *et al.* (1983) as illustrated in Fig. 5 can be expressed as

$$P_{\text{Si}} = P_{\text{SiCl}_4} + P_{\text{SiHCl}_3} + P_{\text{SiH}_2\text{Cl}_2} + P_{\text{SiH}_3\text{Cl}} + P_{\text{SiCl}_2} + P_{\text{SiCl}_3} \quad (1.2.19)$$

Figure 6 shows the plot of silicon solubility as a function of temperature for three different total pressures with $\text{Cl}/\text{H} = 0.06$. The solubility of the silicon-bearing gas in the temperature range of 1200 to 1400 K calculated from this figure is 1.8–2.6% of the total pressure. In other words, the partial pressure of the input silicon-bearing gas should be greater than these values in order to have silicon deposition. Figure 6 also shows that the solubility of silicon at atmospheric pressure (i.e., $P_{\text{tot}} = 1.0$ atm) is decreased with the increase in temperature from 1100 to 1400 K. This means that an increase in temperature results in a decrease in solubility (or increase in supersaturation) and therefore results in increase in growth rate. At reduced pressure growth (e.g., 0.1 atm) the silicon solubility is independent of temperature in the range of 1260 to 1400 K. Growth rate will be less dependent on temperature in this range if reduced-pressure growth is used.

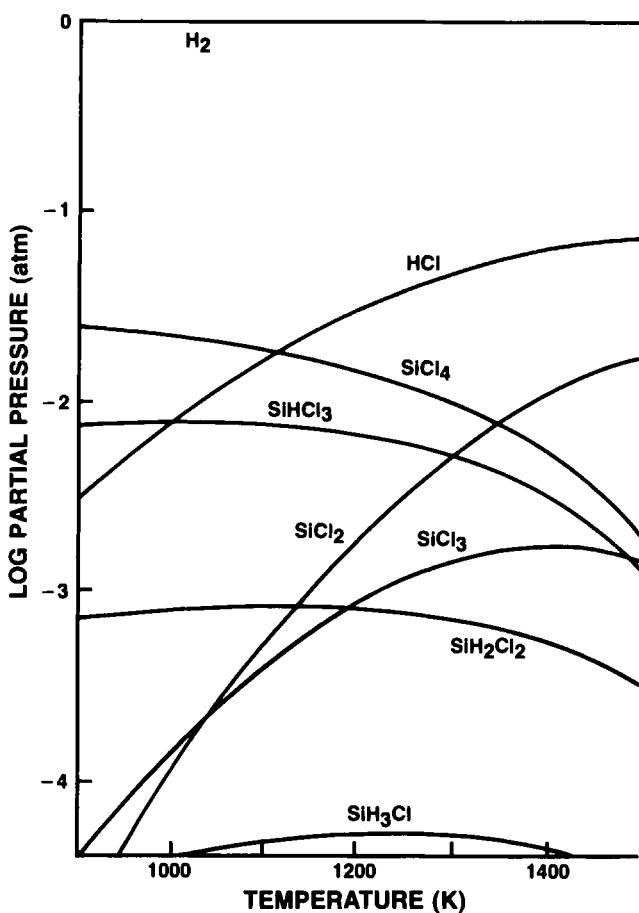


FIG. 5. Calculated equilibrium vapor pressures as a function of temperature at a total pressure of 1 atm and a Cl/H ratio of 0.06. [From Bloem *et al.* (1983). Reprinted with permission of North-Holland Publishing Co., Amsterdam.]

Arizumi (1975) has solved Eqs. (1.2.10)–(1.2.17) for the equilibrium partial pressures of silicon-containing gases as a function of temperature using Cl/H as a parameter. The equilibrium silicon partial pressure was expressed in terms of a silicon to chlorine ratio ($P_{\text{Si}}/P_{\text{Cl}}$). Figure 7 shows the plot of $P_{\text{Cl}}/P_{\text{H}}$ and $P_{\text{Si}}/P_{\text{Cl}}$ as a function of temperature. This figure can also be used to evaluate the degree of supersaturation in the actual epitaxial growth runs. As an example, assume that the entire H_2 carrier gas introduced into the reactor is bubbled through the SiCl_4 tank which was maintained at -20°C . The vapor pressure of SiCl_4 at -20°C is 25 mm Hg (from Fig. 1). The Cl/H ratio of the inlet gas can be calculated as $P_{\text{Cl}}/P_{\text{H}} = 4P/$

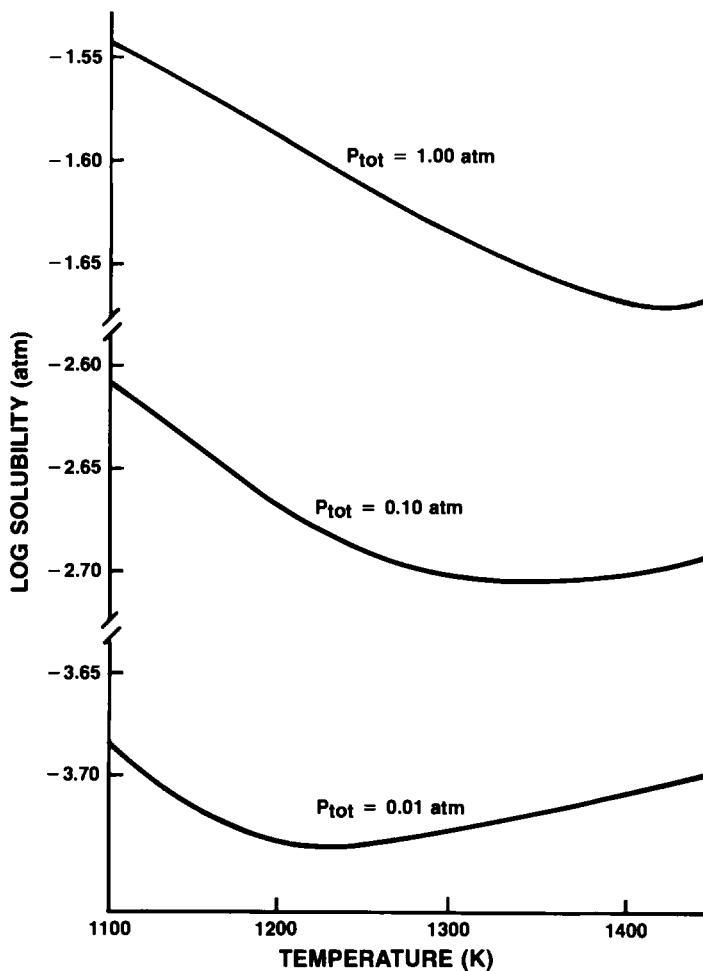


FIG. 6. Plot of the solubility of silicon in the gas phase as a function of temperature for three different total pressures at $\text{Cl}/\text{H} = 0.06$. [From Bloem *et al.* (1983). Reprinted with permission of North-Holland Publishing Co., Amsterdam.]

$2(760 - P) = 4 \times 25/[2 \times (760 - 25)] = 0.068$. Let us assume that the deposition is carried out at 1500 K. Draw a vertical line in Fig. 7 at $T = 1500 \text{ K}$ and a horizontal line at $P_{\text{Cl}}/P_{\text{H}_2} = 0.068$. The intersection of the two lines meets the curve where the $P_{\text{Si}}/P_{\text{Cl}}$ is 0.12. This is the equilibrium value of the ratio of silicon partial pressure to chlorine partial pressure. When SiCl_4 is used as input gas, the ratio of $P_{\text{Si}}/P_{\text{Cl}} = 1/4 = 0.25$. The degree of silicon "supersaturation" (S) in the reactor is

$$S = (P_{\text{Si}}/P_{\text{Cl}})_{\text{enter}} - (P_{\text{Si}}/P_{\text{Cl}})_{\text{equilibrium}} \quad (1.2.20)$$

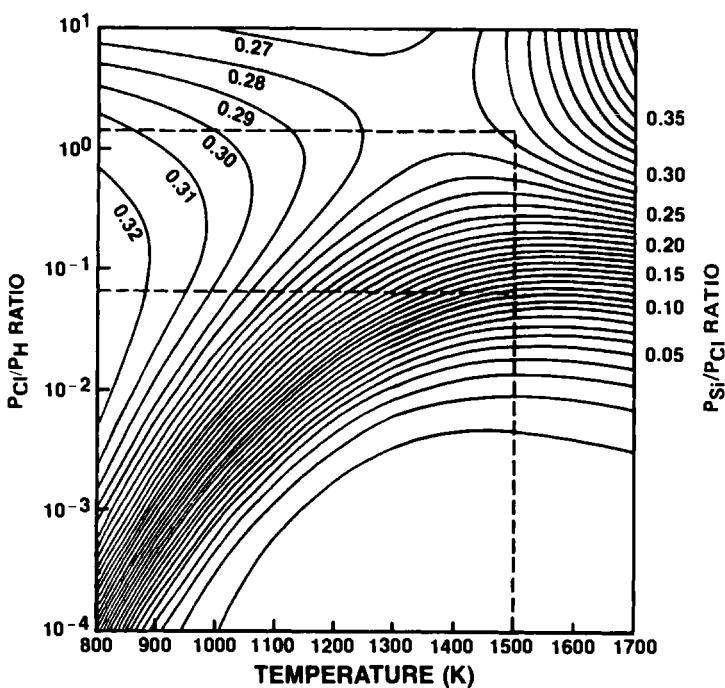


FIG. 7. Plot of $P_{\text{Cl}}/P_{\text{H}}$ and $P_{\text{Si}}/P_{\text{Cl}}$ as a function of temperature. Total pressure = 1 atm. [From Arizumi (1975). Reprinted with permission of North-Holland Publishing Co., Amsterdam.]

In this case $S = 0.25 - 0.12 = 0.13$. Deposition is likely to occur since there is a supersaturation. As another example, let us assume that the SiCl_4 is kept at +30°C. The SiCl_4 vapor pressure of 300 mm Hg is obtained from Fig. 1. The Cl/H ratio of the inlet gas is $P_{\text{Cl}}/P_{\text{H}} = 4P/2(760 - P) = 4 \times 300/[2 \times (760 - 300)] = 1.30$. From Fig. 7 the equilibrium value of $P_{\text{Si}}/P_{\text{H}}$ is 0.285 when the deposition is also carried out at 1500 K. Thus, the degree of supersaturation in the reactor is $0.25 - 0.285 = -0.035$. The negative value implies undersaturation. Thus etching instead of deposition will occur.

The solubility curves are very helpful in predicting the results of an epitaxial process under various deposition parameters. For example, when the composition (i.e., partial pressure) of an input silicon-containing gas is above the solubility curve supersaturation exists, and epitaxial deposition will occur. When the pressure of the input gas is below the solubility curve, etching of silicon will occur. The solubility curves plotted in Figs. 6 and 7 also show that the silicon deposition rates strongly depend upon (1) the Cl/H ratio, (2) temperature, and (3) pressure. For a given input pressure of silicon-containing gas, the higher the Cl/H ratio, the lower is

the supersaturation, and therefore the lower is the growth rate (Fig. 7). In other words the thermodynamic data suggest that under the same deposition conditions a chlorosilane that contains a higher number of chlorine atoms will deposit silicon with a lower rate than one that contains a fewer number of chlorine atoms. Introducing Cl or HCl retards the growth rate because of an increase in the Cl/H ratio.

1.3 GROWTH KINETICS AND MECHANISMS

The mechanism of a CVD process includes two major steps: (1) mass transport from the bulk gas to the substrate surfaces and (2) surface reaction which includes the adsorption and desorption, surface diffusion, and incorporation into the crystal lattice. The boundary layer model has been widely accepted for the description of mass transport from the bulk gas to the substrate surfaces. Figure 8a depicts the formation of a boundary layer above the substrate in a horizontal epitaxial reactor. The velocity of the gas flow is also plotted against the distance above the substrate. As shown in Fig. 8a, the gas velocity is zero at the substrate surface and rapidly increases to a value identical to the velocity of the bulk gas. The distance in which the gas velocity increases from zero to the bulk value is referred to as the thickness of the boundary layer. Figures 8b and 8c depict

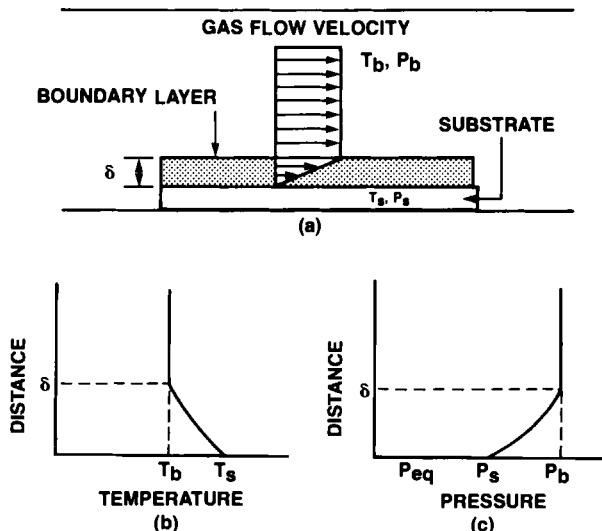


FIG. 8. (a) Schematic representation of the formation of a boundary layer above the substrate in a horizontal epitaxial reactor. Changes of (b) temperature and (c) pressure across the boundary layer.

the changes of temperature and pressure, respectively, across the boundary layer.

The boundary layer thickness affects the mass transport rate through this layer. This layer thickness is determined by the flow dynamics of the gas mixture in the reactor. In open tube reactors, the gas flows by forced convection. Characteristics of the convection flow can be described by the Reynolds number R which is defined as

$$R = \rho v L / \eta \quad (1.3.1)$$

where ρ is the density of gas mixture, v the velocity of gas mixture, L the length of the horizontal reactor, and η the viscosity. The thickness δ of the boundary layer is related to the Reynolds number by

$$\delta = 5L(1/R)^{1/2} \quad (1.3.2)$$

Equations (1.3.1) and (1.3.2) show that high gas flow velocities result in high R values which in turn reduce δ . Physically, large Reynolds numbers imply small viscous effects. When R is less than 5400 the flow pattern in the reactor is laminar, and it becomes turbulent when its value is greater than 5400 (Bloem and Giling, 1978).

The first step of the surface reaction is the adsorption of gas species on the substrate surface. The amount of gas adsorbed depends on its equilibrium partial pressure and temperature. For a given temperature, the mass of gas adsorbed can be calculated according to the theory of Langmuir isotherm, from which the fraction of surface sites occupied (ϕ) can be calculated. Chernov (1977) has used the equilibrium partial pressure of each gas species to calculate ϕ . The results are listed in Table 3. These results show that 83% of the surface sites are occupied by atomic hydrogen

TABLE 3. Equilibrium Coverage of the Adsorbed Molecules on a (111) Surface in the Si-H-Cl System^a

Gas species	P_e (dyne/cm ²)	ϕ
H ₂	10 ⁶	10 ⁻⁴
HCl	2×10^4	10 ⁻⁷
SiCl ₄	4	1.5×10^{-11}
SiHCl ₃	30	1.7×10^{-10}
SiCl ₂	7×10^2	0.16
Si	4×10^{-2}	3.1×10^{-7}
Cl	2×10^{-1}	0.2
H	10	0.63
Vacancies	—	0.015

^aFrom Chernov (1977). Here Cl/H = 0.01 and $T = 1500$ K.

and chlorine. Here SiCl_2 is the only silicon-containing gas species in the Si–Cl–H system that contributes significantly to surface coverage.

Equations for the silicon deposition rate can be derived if the rate-limiting step is known. If mass transfer through the boundary layer is the rate-limiting step, then Fick's First Law can be used to calculate the mass transfer rate:

$$J_d = \frac{D}{RT} \frac{P_b - P_s}{\delta} \quad (1.3.3)$$

where J_d is the mass transfer flux by diffusion through the boundary layer, P_b the partial pressure in the gas stream, P_s the partial pressure at the surface, D the diffusion constant, and δ the thickness of boundary layer.

In surface reactions if the formation of the adsorbed atoms is the rate-limiting step, the mass transfer flux can be calculated using

$$J_s = \frac{K_d}{RT} (P_s - P_{eq}) \quad (1.3.4)$$

where J_s is the mass transfer flux by surface adsorption, K_d the mass transfer coefficient, and P_{eq} the equilibrium partial pressure. Under steady-state conditions J_d is equal to J_s . By equating Eq. (1.3.3) to Eq. (1.3.4) we can rearrange and obtain the following expression for N_{cvd} which is referred to as the CVD number (van den Brekel, 1977):

$$\frac{P_b - P_s}{P_s - P_{eq}} = \frac{K_d \delta}{D} = N_{cvd} \quad (1.3.5)$$

N_{cvd} is a dimensionless number which can be used to characterize the deposition process. When N_{cvd} is much greater than 1 because of a small D/δ , the deposition rate is limited by the diffusion through the boundary layer and is referred to as a diffusion-controlled process. When N_{cvd} is much less than 1 because of a small K_d , the deposition rate is limited by the surface reaction and is referred to as a surface-reaction-controlled process. When N_{cvd} is approximately equal to 1, the process is under the transition between the two rate-controlling steps.

At steady state, P_s can be evaluated by equating the right-hand side of Eqs. (1.3.3) and (1.3.4), P_s is substituted back into Eq. (1.3.3) or (1.3.4) and yields an expression for the mass transfer flux in terms of constants including D and K_d (Bloem and Giling, 1978):

$$J = \frac{P_b - P_{eq}}{RT(\delta/D + 1/K_d)} \quad (1.3.6)$$

This equation shows that the mass transfer rate is mainly a function of partial pressure and temperature. However, the "constants," δ and D , depend on temperature, pressure, and flow rate (Bloem and Giling, 1978):

$$D = D_0 \frac{P_0}{P} \left(\frac{T}{T_0} \right)^{1.75} \quad (1.3.7)$$

$$\delta = 5 \left(\frac{\eta RT}{\rho M v} x \right)^{1/2} \quad (1.3.8)$$

where subscript 0 denotes the reference point, M is the molecular weight of gas mixture, x is the position along the susceptor, and η is the viscosity of gas mixture.

A generalized rate equation which is expressed in terms of temperature, pressure, and flow rate F has been given by Spear (1979) as:

$$J = \frac{K_d(F^{1/2})(T^m)(P_b - P_s)}{P} \quad (1.3.9)$$

where m is an empirical constant and P the total pressure. The effect of temperature on the deposition rate described in Eq. (1.3.9) is perhaps applicable only for the diffusion-controlled process. In this case m is equal to $\frac{3}{2}$ (Bloem and Claassen, 1983). The deposition rate in a reaction-controlled process is exponentially proportional to the temperature following the Arrhenius equation. The effect of F and P_b on the deposition rate shown in Eq. (1.3.9) describes fairly well the deposition of silicon from silane or dichlorosilane. However, the growth rate of silicon deposited from silicon tetrachloride does not increase monotonically with input SiCl_4 concentration. Van der Putte *et al.* (1975) have derived a rate equation for SiCl_4 using a modified model which considers the temperature gradient across the boundary layer and thermal diffusion factors of each gas species. The following will review the kinetics and mechanisms of silicon deposition from specific silicon-containing gases.

1.3.1 Growth from Silane

Early studies of silicon deposited from silane have suggested that the reaction includes only a single step without producing intermediate products. A study by Lee (1984) has proposed that the surface-adsorbed molecules are SiH_2 instead of SiH_4 . He suggests the following sequence of steps for deposition: (1) diffusion of silane from the bulk gas through the boundary layer, (2) dissociation of silane into SiH_2 and H_2 at the silicon surfaces, (3) adsorption of SiH_2 on the surfaces, (4) diffusion of SiH_2 adatoms to surface kink sites, and (5) incorporation of Si into the crystal

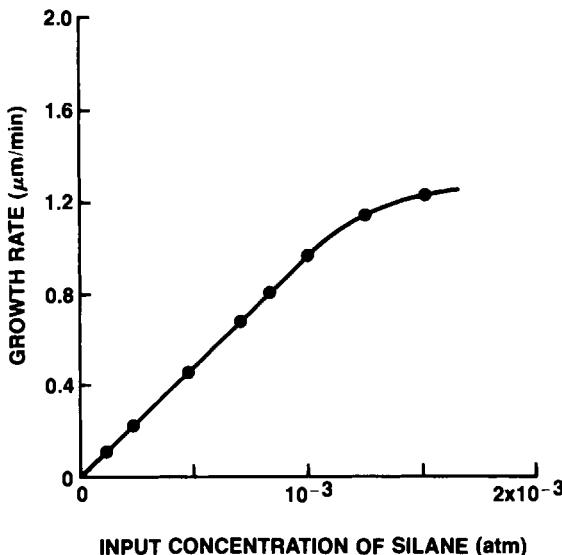


FIG. 9. Measured silicon growth rate from silane at 1150°C as a function of the input concentration of silane. [From Bloem and Giling (1978). Reprinted with permission of North-Holland Publishing Co., Amsterdam.]

lattice accompanied by the desorption of H₂. At high temperatures (>1000°C) and low pressures, steps (2)–(4) proceed rapidly, and step (1) is the rate limiting step. Bloem and Giling (1978) have derived the rate equation which shows that the deposition rate is directly proportional to the silane pressure. When silane is diluted with hydrogen at low pressure, the growth rate is still proportional to the partial pressure of silane but inversely proportional to the square root of the hydrogen partial pressure. Figure 9 shows the measured growth rate at 1150°C as a function of the input concentration of silane.

Studies on growth kinetics at a low temperature have been made by Bloem and Claassen (1980) and by Lee (1984). These studies suggest that at low temperatures, the silicon surface is highly covered with hydrogen adatoms (as shown in Table 3), and, therefore, the surface reaction of silicon-containing species is the rate limiting step. The growth rate G was derived in terms of the reaction rate constants and partial pressure of silane P_0 as

$$G = K_1 P_0 / (1 + K_a P_0) \quad (1.3.10)$$

This equation is similar to the Langmuir adsorption equation. Here, K_1 is the surface diffusion rate constant of SiH₂ adatoms for the reaction SiH₂(surface) → Si(crystal) + H₂, and K_a is the adsorption rate constant

for the reaction $\text{SiH}_2 + \text{surface site} \rightarrow \text{SiH}_2(\text{surface})$. Experimental measurements have shown that the growth rate is directly proportional to P_0 , which suggests that K_a in Eq. (1.3.10) is very small.

The deposition rate can be affected by the type of carrier gas used. When hydrogen is replaced by an inert gas such as helium or argon, the deposition rate is increased (Claassen and Bloem, 1981). It is likely that the surface coverage by He or Ar is not as extensive as by H_2 . Therefore, the surface reaction of the silicon-containing gas is increased. The presence of other gases such as HCl adversely affects the deposition rate. An increase in HCl will decrease $(P_{\text{Si}}/P_{\text{Cl}})_{\text{enter}}$ in Eq. (1.2.20). Therefore, supersaturation of Si is reduced by the addition of HCl. In the temperature range of 800 to 900°C the effect of HCl on the deposition rate G can be expressed as (Bloem and Claassen, 1980; Lee, 1984)

$$G = aP_{\text{SiH}_4} - bP_{\text{HCl}}^2 \quad (1.3.11)$$

where a and b are constants which are temperature dependent.

1.3.2 Growth from Dichlorosilane

The deposition of silicon from dichlorosilane consists of several intermediate steps. Bloem and Claassen (1983) have shown that formation of the intermediate compound, SiCl_2 , plays an important role in determining the deposition rate. Two "rate-limiting steps" are suggested for deposition from dichlorosilane: (1) decomposition of SiH_2Cl_2 to SiCl_2 and H_2 and (2) release of Cl from SiCl_2 by interaction with H_2 . Analyses of the gas species using laser Raman spectroscopy (Sedgwick and Smith, 1976) and mass spectrometer (Ban and Gilbert, 1975; Ban, 1975) have shown that the decomposition of SiH_2Cl_2 into SiCl_2 and H_2 occurs in the gas phase; SiCl_2 , H_2 and other gases are then adsorbed on the substrate surface (see Table 3) to form a monolayer. The adsorbed SiCl_2 then diffuses to the surface steps in accordance with the vacancy mechanism (Chernov and Papkov, 1977). Incorporation of silicon atoms into the crystal lattice is completed by the chemical reaction with H_2 . The reaction by-product, HCl, is then released from the surface.

Claassen and Bloem (1980) have studied the deposition rate as a function of gas-phase composition at 800, 900, and 1000°C. The results show that the deposition rate is linearly proportional to the input concentration of SiH_2Cl_2 only at 1000°C. A parabolic relationship is found at 900 and 800°C. Figure 10a shows the growth rate data obtained from a horizontal reactor by Claassen and Bloem (1980). However, Morosanu *et al.* (1983) reported the linear relationship to exist for temperatures ranging from 800 to 1200°C. Results of growth rate versus mole% experiments performed in barrel reactors by Herring (1979a) and us have also shown a slight deviation from

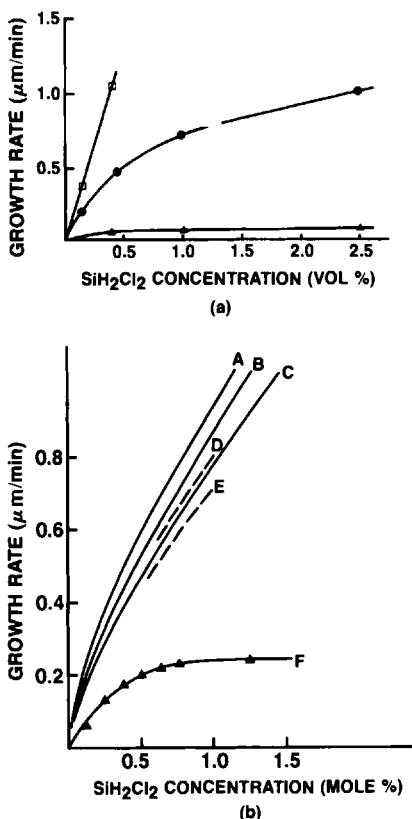


FIG. 10. (a) Growth rate versus input concentration of SiH_2Cl_2 obtained from an rf heated horizontal reactor: \triangle , 800°C ; \bullet , 900°C ; \square , 1000°C . [From Claassen and Bloem (1980). Reprinted with permission of North-Holland Publishing Co., Amsterdam.] (b) Growth rate versus input concentration of SiH_2Cl_2 obtained from radiantly heated barrel reactors. Temperature and pressure parameters are as follows: curve A, 1080°C , 760 torr (Herring, 1979a); curve B, 1080°C , 80 torr (Herring, 1979a); curve C, 1080°C , 40 torr (Herring, 1979a); curve D, 1100°C , 760 torr; curve E, 1100°C , 80 torr; curve F, 950°C , 50 torr, 1.1% HCl.

linearity at $1080\text{--}1100^\circ\text{C}$. The nonlinear relationship is observed at 950°C with addition of 1.1% HCl. Figure 10b shows the results of Herring (1979a) and the authors. The concentration of H_2 in the inlet gas mixture also affects the growth rate. Claassen and Bloem (1980) have found that the growth rate is a linear function of the partial pressure of H_2 . In contrast, Morosanu *et al.* (1983) have found that the growth rate is inversely proportional to the square root of the H_2 partial pressure. The discrepancies could result from the differences in reactors and carrier gases used.

1.3.3 Growth from Trichlorosilane and Silicon Tetrachloride

Growth of silicon from trichlorosilane or silicon tetrachloride is under the same thermodynamic system, (i.e., $\text{Si}-\text{H}-\text{Cl}$) as from dichlorosilane with the exception of a higher input Cl/H ratio for a given input concentration of chlorosilanes. Ban (1975) has analysed the vapor-phase species in the deposition from SiHCl_3 and SiCl_4 and identified the same components as from SiH_2Cl_2 . They are H_2 , HCl , SiCl_2 , SiH_2Cl_2 , SiHCl_3 , and

SiCl_4 . However, the concentration of SiCl_2 in the gas phase is much lower than the equilibrium value when SiCl_4 was used as source gas and deposited at a low temperature. This raises the question of whether SiCl_4 is directly transported to the surface where it is adsorbed and that a heterogeneous reaction occurs on the surface between SiCl_4 and H_2 to form Si and HCl. The reaction product, HCl, can react with the silicon substrate to form a number of volatile compounds such as SiCl_2 , SiH_2Cl_2 , and/or SiHCl_3 . The unreacted HCl molecules can desorb from the substrate. However, Nishizawa and Nihira (1978) have also observed that all the above chlorosilane species existed in the gas phase. Recent studies by Aoyama *et al.* (1981) have found that the reaction mechanism of silicon deposition from SiCl_4 is very dependent on deposition conditions; SiCl_4 is believed to be directly transported to the silicon surface where it is reduced to silicon when high gas flow rates and low substrate temperatures are used.

A simple mass transport equation has failed to describe the rate of silicon deposition as a function of SiCl_4 concentration. Unlike using other silicon source gases in which the deposition rate increases with the concentration of input silicon source gas, the deposition rate increases with the SiCl_4 concentration to a maximum value and then decreases with continued increase in SiCl_4 concentration. Van der Putte *et al.* (1975) have proposed a model that considers the existence of a temperature gradient at the boundary layer. This model includes the thermal diffusion coefficient factor and temperature gradient into the mass transfer rate equation. The equations derived from this model have predicted results that are in agreement with the experimental data provided by various investigators. The recent work by Aoyama *et al.* (1981) has also verified this model.

It should be pointed out at this time that the growth rate maximum for SiCl_4 is seldom reached in commercial epitaxial reactors. These reactors are designed for the high-volume production of epitaxial silicon wafers. The high concentration of silicon tetrachloride required to achieve the maximum growth rate is not easily obtained since only a fraction of the inlet hydrogen is bubbled through SiCl_4 and no heating is applied to the SiCl_4 reservoir. The partial pressure of SiCl_4 in a commercial reactor is therefore relatively low as compared to that in a laboratory reactor. Typical growth rate data obtained from the large commercial reactors are shown in Fig. 11 for the deposition from SiHCl_3 and SiCl_4 .

1.4 NUCLEATION

Nucleation of solid silicon from silicon-containing gases can occur either in the gas phase or on a solid surface. The former is referred to as homogeneous nucleation while the latter is heterogeneous nucleation.

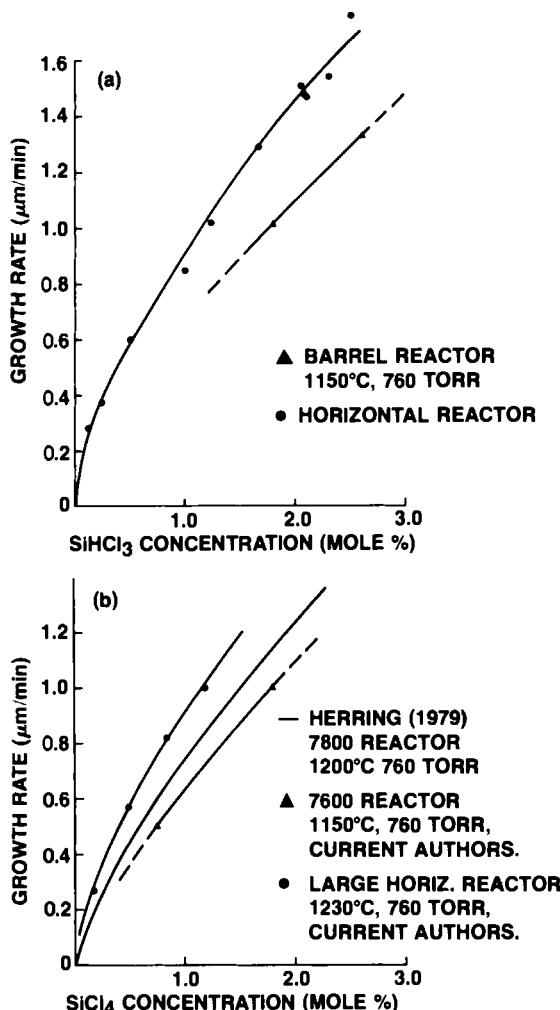


FIG. 11. (a) Growth rate versus input SiHCl_3 concentration: ▲, barrel reactor, 1150°C, 760 torr; ●, horizontal reactor. (b) Growth rate versus input SiCl_4 concentration: —, 7800 reactor, 1200°C, 760 torr (Herring, 1979); ▲, 7600 reactor, 1150°C, 760 torr; ●, large horizontal reactor, 1230°C, 760 torr.

Silicon clusters formed in the gas phase are undesirable for epitaxial growth since they prevent the growth of single-crystal silicon on the substrate. Fortunately, homogeneous nucleation requires a higher degree of supersaturation than heterogeneous nucleation. Therefore, heterogeneous nucleation normally occurs first. Heterogeneous nucleation can occur on the silicon substrate as well as on foreign materials. Silicon is likely to grow epitaxially on its own substrate if the substrate temperature is high enough.

This process is referred to as homoepitaxy. Nucleation on foreign substrates generally leads to polycrystalline growth although specific orientations of certain materials such as sapphire, in which the lattice parameters match with that of silicon, can also lead to single-crystal growth. This combination is referred to as heteroepitaxy and is the subject of another chapter in this book.

1.4.1 Homogeneous Nucleation

In homogeneous nucleation the growth of silicon particles becomes possible only if the nuclei have reached a critical dimension which is referred to as the critical nucleus. When a nucleus is smaller than the critical dimension, its surface energy will be larger than that required for formation of the nucleus and is therefore unstable. Hirth and Pond (1963) have shown that the radius of the critical nucleus, r^* , is a function of specific surface free energy u and supersaturation P/P_{eq} :

$$r^* = \frac{2uv}{KT \ln(P/P_{\text{eq}})} \quad (1.4.1)$$

where v , K and T are the atomic volume, Boltzman constant, and absolute temperature, respectively. Equation (1.4.1) shows that low supersaturation increases the diameter of critical nuclei and makes the growth of silicon in the gas phase less likely. High supersaturation is generally observed in an irreversible reaction such as the pyrolysis of silane. Therefore, homogeneous nucleation is most likely to occur when silicon is deposited from silane. Eversteijn (1971) has evaluated the critical partial pressure of silane above which homogeneous nucleation will occur. Figure 12 shows the critical partial pressure of silane needed for homogeneous nucleation as a function of temperature.

The rate of nucleation is exponentially related to the temperature and free energy of formation of the nuclei, ΔF . Brice (1973) has shown that the nucleation rate dN/dt for homogeneous nucleation can be described as

$$dN/dt = C \exp(-\Delta F/KT) \quad (1.4.2)$$

where C is a constant.

1.4.2 Heterogeneous Nucleation

In heterogeneous nucleation, the concept of critical nuclei is no longer needed since the substrate itself will serve as the nuclei for the growth. The terrace-step-kink growth model is generally accepted for describing the growth of smooth epitaxial surfaces. When the substrate contains steps and kinks on the surface the adsorbed atoms and/or molecules on the

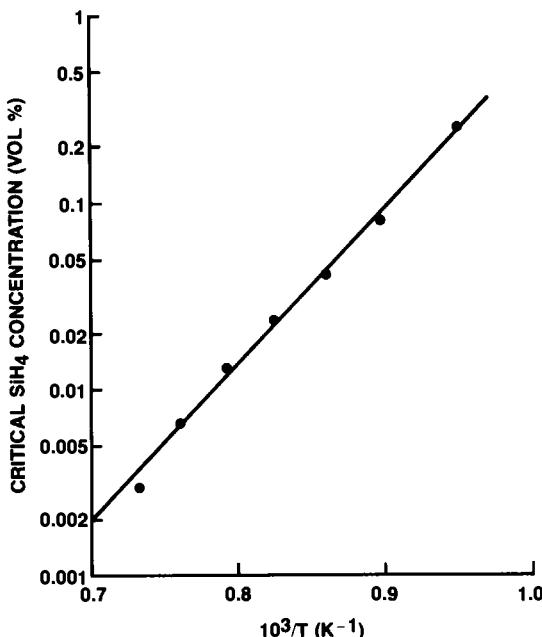


FIG. 12. Critical partial pressure for homogeneous silicon nucleation from silane versus temperature. [From Eversteijn (1974). Reprinted with permission from Phillips Res. Report.]

terrace will migrate (diffuse) to the microscopic (or atomic) surface steps. The steps can result from crystallographic defects such as screw dislocations or misoriented surfaces from low-index planes. The adsorbed atoms and/or molecules will further diffuse along the steps to the kinks and incorporate into the lattice. Silicon surfaces with (111) orientation, which contain no steps, are referred to as singular surfaces. The growth of smooth and flat surfaces is difficult to achieve when the layer is deposited on singular surfaces. This is the so-called singular instability of the surface (Rode *et al.*, 1977). In this case the formation of a two-dimensional nucleus is needed prior to the epitaxial growth. The formation of two-dimensional nuclei is characterized by the formation of tripyramids as shown in Fig. 13. Rode *et al.* (1977) have postulated that the formation of the terraces and pyramids are due to instabilities of the singular surfaces. The surfaces with terraces and pyramids provide a closer spacing of surface steps. The surfaces will then become more stable resulting from the step-step interactions. A slight deviation from the singular orientation provides monoatomic growth steps and the growth of a smooth planar surface becomes possible. Misorientation of 3–5° off the (111) toward the nearest (110)

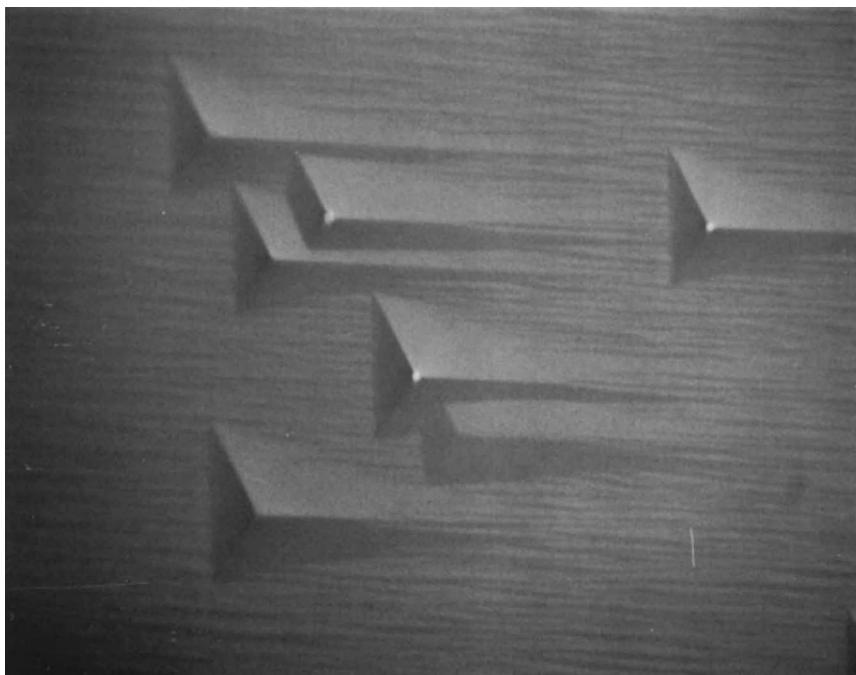


FIG. 13. Photomicrograph of tripyramids on a (111) surface due to singular instability.

plane is commonly used for achieving the growth of stable planar surfaces.

Two-dimensional nucleation of epitaxial layers has been studied by Nishizawa *et al.* (1972). They have found that growth proceeds rapidly in lateral directions. The ratio of lateral to vertical growth rate is at least 2800:1 when Si is deposited from SiCl_4 at 1200°C. Rapid lateral growth does not occur when silicon is deposited using silane. High supersaturation of a chlorosilane inhibits a large ratio of lateral growth. In this case two-dimensional or even homogeneous nucleation can occur and lead to the growth of rough or polycrystalline surfaces.

In heterogeneous nucleation the free energy for the adsorption of adatoms ΔF_{ad} and the free energy for the surface diffusion of adatoms ΔF_{d} need to be considered. The nucleation rate can be expressed as (Hirth and Pond, 1963)

$$\frac{dN}{dt} = C \frac{\log S}{T^{1/2}} P^2 \exp \left[\frac{2 \Delta F_{\text{ad}} - \Delta F_{\text{d}} - \Delta F}{KT} \right] \quad (1.4.3)$$

where C is a constant and S the supersaturation, which in this case is defined as the ratio of input partial pressure to the equilibrium partial pressure of silicon containing gases. Bloem (1979) and Liaw *et al.* (1984)

TABLE 4. Effect of Substrate Materials and Gas Ambient on Silicon Deposition Rate^a

Substrate	SiH ₂ Cl ₂ (1000°C)		SiCl ₄ (1050°C)	
	No HCl	0.88% HCl	No HCl	0.71% HCl
Poly Si	0.270	0.212	0.284	0.200
Si ₃ N ₄	0.245	0.108	some nucleation	no deposition
SiO ₂	0.243	0.042	few nucleation	no deposition
Single-crystal Si	0.307	0.242	0.294	0.202

^aDeposition rates given in micrometers per minute.

have found that the heterogeneous nucleation rate is strongly dependent on the substrate material, which affects ΔF_{ad} and ΔF_d . At a given temperature and partial pressure of silicon-containing gas, the heterogeneous nucleation rate of silicon on various substrates decreases in the following order: single-crystal silicon > polycrystalline silicon > silicon nitride > aluminum oxide > silicon dioxide. The heterogeneous nucleation rate can be qualitatively approximated by measuring the deposition rate using the weight gain method. Table 4 lists the deposition rate of silicon on various substrates from SiH₂Cl₂ and SiCl₄ with and without the addition of HCl.

Equation (1.4.3) is valid only when the supersaturation of the silicon-containing gas exceeds the critical value for the onset of heterogeneous nucleation. The partial pressure of the silicon-containing gas at this critical value is referred to as the critical partial pressure (P^c). For the nucleation of silicon on Si₃N₄ from SiCl₄, P^c has been determined experimentally as well as theoretically by Ogawa *et al.* (1971). The theoretical evaluation is made by letting $dN/dt = 0$ in Eq. (1.4.3) and solving for P . The results have shown that this theoretical calculation is a good approximation to the actual measured values. The critical partial pressure was also found to increase with temperature. For example, when the temperature is changed from 1420 K to 1530 K, P^c increases from 2×10^{-3} to 5×10^{-3} atm.

1.5 DOPANT INCORPORATION

Doping the epitaxial silicon with either a *p*-type or *n*-type impurity is required to obtain the desired electrical characteristic needed for semiconductor device applications. The operation of such devices depend on the precise control of the impurity content as well as its distribution through the layer; AsH₃ and PH₃ are commonly used for *n*-type doping gases while B₂H₆ is used for *p*-type doping. A trace of the doping gas is introduced into the epitaxial reactor along with the silicon-containing compound. At high temperatures in the epitaxial reactor, the doping molecules

decompose into several vapor species. The equilibrium partial pressures of these species can be calculated thermodynamically just as those for the silicon-containing species (see Section 1.2.4). The equilibrium composition of arsenic and phosphorus dopants in the gas phase have been calculated by Rai-Choudhury and Salkovitz (1970b). The equilibrium partial pressures of gas species in the Si-H-P and Si-H-Cl-B systems have been reviewed by Bloem and Giling (1978) and by Giling (1983). These equilibrium data provide information on the dominant dopant species at a given input pressure. For example, at low input PH₃ pressures the main components in the gas phase are PH₃ and PH₂. At high input PH₃ pressures P₂ becomes the dominant species.

The effectiveness of the incorporation of the dopant into the silicon is determined by the segregation coefficient K_{eff} . It is defined as the dopant concentration in the silicon divided by the ratio of partial pressures of dopant-containing gases (P_{dope}^0) to silicon-containing gases (P_{Si}^0):

$$K_{\text{eff}} = \frac{[\text{dope}]_{\text{Si}} / (5 \times 10^{22})}{P_{\text{dope}}^0 / P_{\text{Si}}^0} \quad (1.5.1)$$

When the value of K_{eff} is less than 1, a portion of the dopant atoms are rejected from being incorporated into the epitaxial crystal, and the growth interface accumulates excess dopant atoms. When K_{eff} is equal to 1, the arriving dopant atoms are completely incorporated into the silicon.

1.5.1 Effect of Growth Parameters

The incorporation of dopant into epitaxial silicon can be affected by the input partial pressure of the dopant-containing gas, growth temperature, and growth rate. The input partial pressure is the most significant factor. In general, the dopant concentration of the epitaxial layer increases linearly with the input partial pressure. However, at high input pressures, the dopant concentration in epitaxial layer does not increase linearly with pressure. Figures 14 and 15 show the concentration versus pressure relationship for phosphorus and boron doping, respectively. Figure 14 shows that the concentration of phosphorus incorporated into the silicon is linearly proportional to the input PH₃ partial pressure for partial pressures less than 10⁻⁶ atm and proportional to the square root of the PH₃ partial pressure for the partial pressures greater than 10⁻⁶ atm. These results are primarily due to the fact that for low input pressures, PH₃ and PH₂ are the main gas-phase species in the Si-H-P system. For high input pressures, P₂ is the main gas species. Consequently, the following relationships hold for low and high partial pressures (Giling, 1983)

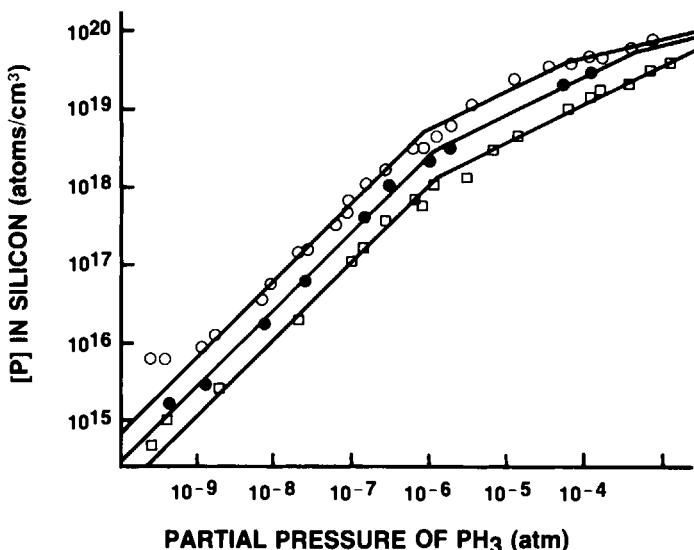


FIG. 14. Incorporation of phosphorus in silicon as a function of the input pressure of phosphine: \circ , 1400 K; \bullet , 1500 K; \square , 1600 K. [From Bloem *et al.* (1974). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

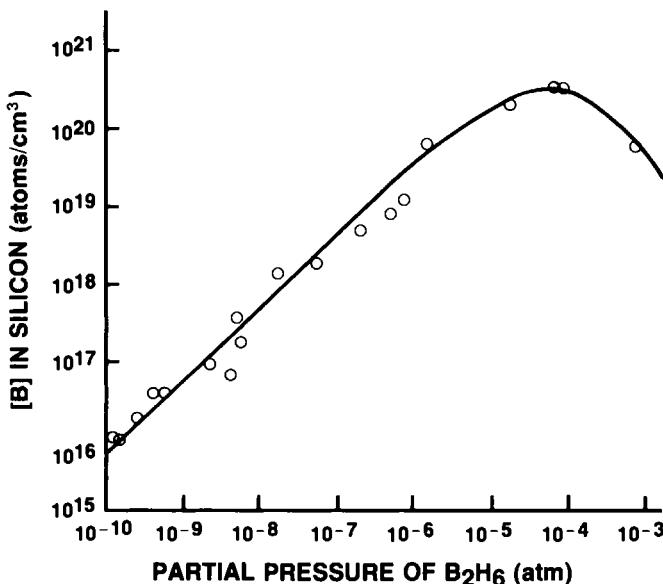


FIG. 15. Incorporation of boron in silicon as a function of input pressure of diborane. [From Rai-Choudhury and Salkovitz (1970a). Reprinted with permission of North-Holland Publishing Co., Amsterdam.]

(a) low input pressure

$$P_{\text{PH}_3}^0 = P_{\text{PH}_3} + P_{\text{PH}_2} \quad (1.5.2)$$

$$[P]_{\text{incorporated}} = P_{\text{PH}_3}^0 \quad (1.5.3)$$

(b) high input pressure

$$P_{\text{PH}_3}^0 = 2P_{\text{P}_2} \quad (1.5.4)$$

$$[P]_{\text{incorporated}} = (P_{\text{PH}_3}^0)^{1/2} \quad (1.5.5)$$

The relationship shown in the region of high input partial pressure of Fig. 15 can also be understood by thermodynamic considerations. The equilibrium partial pressure data show that the boron-containing species start to condense at high input pressures of diborane. The condensed boron does not contribute to the gas-phase doping. This is why the boron incorporation decreases with input partial pressure of diborane.

The preceding thermodynamic considerations of dopant incorporation into the epitaxial silicon assume that the segregation coefficient is equal to one. In fact, the segregation coefficient is a function of the deposition temperature and growth rate. Bloem and Giling (1978) have derived a mathematical expression for the change of K_{eff} with temperature. Rai-Choudhury and Salkovitz (1970a) found experimentally that the incorporation efficiency of *n*-type dopants decreases with an increase in temperature, while that of *p*-type dopants increases with temperature. Figure 16 shows such relationships for B_2H_6 , PH_3 , and AsH_3 .

The effect of growth rate can be divided into two regions. In the region of low growth rate, changes in the growth rate have only a slight effect on the incorporation of dopant in the epitaxial layer. At high growth rates the concentration of dopants incorporated into the layer decreases with an increase in growth rate. Figure 17 shows the plot of phosphorus concentration in silicon versus growth rate for the epitaxial films grown using silane as the silicon source gas and PH_3 as the doping gas. The combined effect of growth rate, growth temperature, and input pressure of phosphine on doping concentration in silicon is shown in Fig. 18.

1.5.2 Distribution of Unintentionally Doped Impurities

Dopants incorporated into the epitaxial layer discussed earlier are intentionally introduced. Portions of the impurities in the epitaxial layers can also be introduced unintentionally, particularly when heavily doped or buried layer diffused substrates are used. The possible sources of these impurities come from (1) the substrate by solid-state diffusion, (2) the substrate by evaporation, and (3) the reactor system such as the reactor wall and susceptor by outgassing. They are referred to as solid-state outdiffusion, gas-phase autodoping, and system autodoping, respectively.

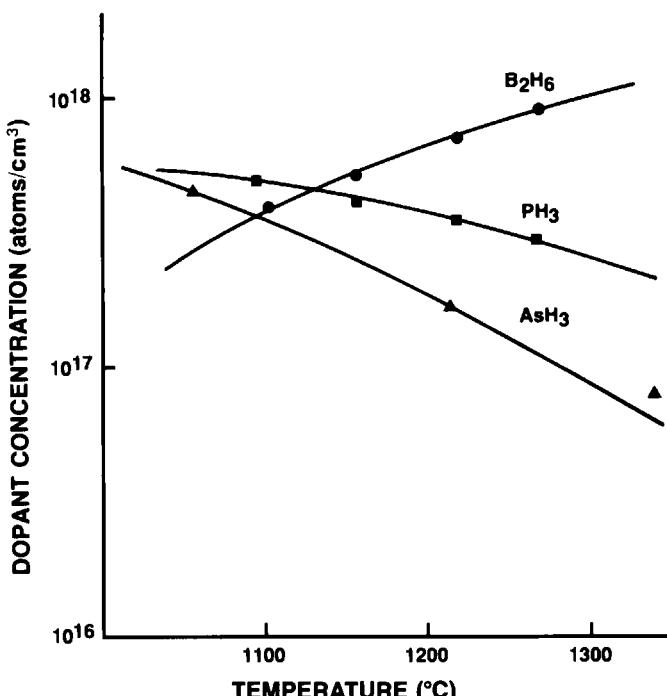


FIG. 16. Dopant incorporation efficiencies into epitaxial silicon as a function of growth temperature. Dopant partial pressure = 1.4×10^{-6} . [From Rai-Choudhury and Salkovitz (1970a). Reprinted with permission of North-Holland Publishing Co., Amsterdam.]

Figure 19 is a sketch that illustrates the doping concentration versus depth from the epitaxial surface. Here C_s^0 is the original surface concentration of the substrate, and C_f^0 is the surface concentration of the epitaxial film. The step profile represents the ideal case in which autodoping and outdiffusion do not occur. The curved profile represents an actual case where unintentional doping impurities have been incorporated into the epitaxial layer. The segment ($X = X_c - X_j$) with the doping profile $C_f(X)$ is the result of the solid-state outdiffusion during the epitaxial process. The next segment ($X_c - X_{ai}$) with the doping profile $C_{ai}(X)$ is the result of the vapor-phase autodoping. A common source of the solid-state outdiffusion and the vapor-phase autodoping is the buried layer. The remaining segment toward the epitaxial surface is doped from the system autodoping and any intentional dopant added during the deposition cycle.

1.5.2.1 Solid-State Outdiffusion

Rice (1964) and Grove *et al.* (1965) developed a model for the impurity redistribution during the epitaxy based on solid-state diffusion. Price and Goldman (1979) have reformulated the diffusion model in terms of easily measured parameters. The concentration profile $C_f(x)$ in the segment

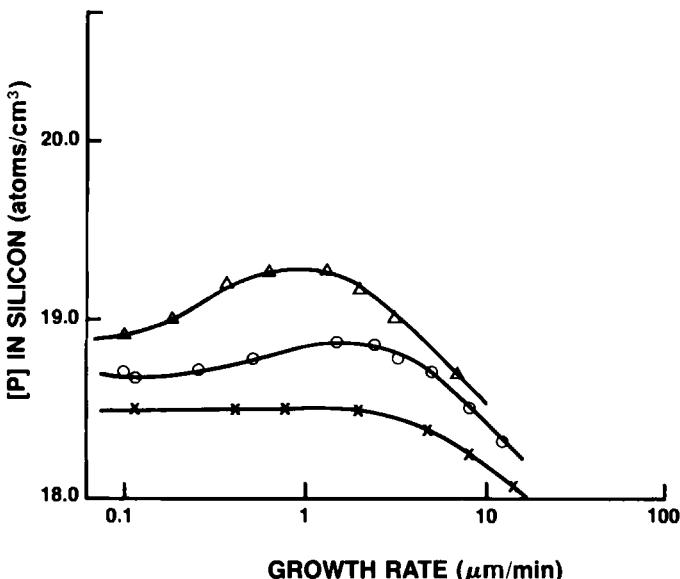


FIG. 17. Phosphorus concentration in silicon versus growth rate for the epitaxial films grown from silane using PH_3 as a dopant: $P_{\text{PH}_3} = 1.2 \times 10^{-6}$ atm; Δ , 1350 K; \circ , 1425 K; \times , 1500 K. [From Bloem (1973). Reprinted by permission of The Electrochemical Society, Inc. This figure was originally presented at the Spring 1973 Meeting of The Electrochemical Society, Inc., held in Chicago, Illinois.]

$X = X_c - X_j$ of Fig. 19 was derived. The profile follows a complementary error function with $K = X/(2(D_f t)^{1/2})$ as a parameter, where D_f and t are the diffusion coefficient and epitaxial growth time, respectively. The distance X_j with respect to the original epitaxial thickness X_c has been formulated with parameters V and t , where V is the growth rate and t is growth time:

$$\frac{X_j}{X_c} = 1 - \frac{2K(D_f t)^{1/2}}{V} \frac{1}{t^{1/2}} \quad (1.5.6)$$

The ratio of X_j/X_c measures the degree of outdiffusion. The smaller the ratio, the greater is the outdiffusion; D_f will increase with temperature, and, therefore, outdiffusion will also be increased. This equation also states that the dopant outdiffusion is inversely proportional to the square root of the growth time and is inversely proportional to the growth rate. The experimental results carried out by Price and Goldman (1979) and also by us have verified this relationship: X_j was measured by the bevel-and-stain technique, and X_c was obtained by the weight-gain method. Figure 20a shows the plot of X_j/X_c versus $1/t^{1/2}$ for different growth rates on phosphorus-doped substrate at 1125°C. Figure 20b shows the same type of plot and compares the outdiffusion between the Sb- and B-doped substrates. A growth pressure of 760 torr was used in both cases.

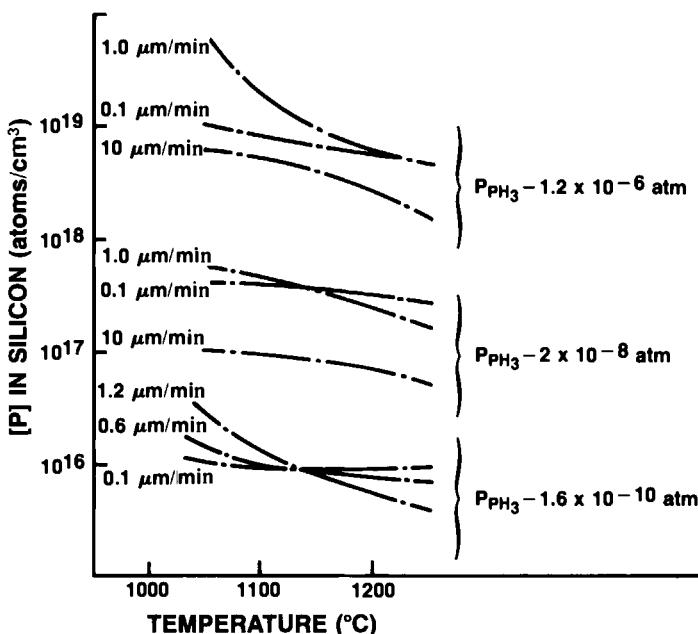


FIG. 18. Plot of doping concentration in silicon as a function of growth rate, growth temperature, and input pressure. [From Bloem (1972). Reprinted with permission of North-Holland Publishing Co., Amsterdam.]

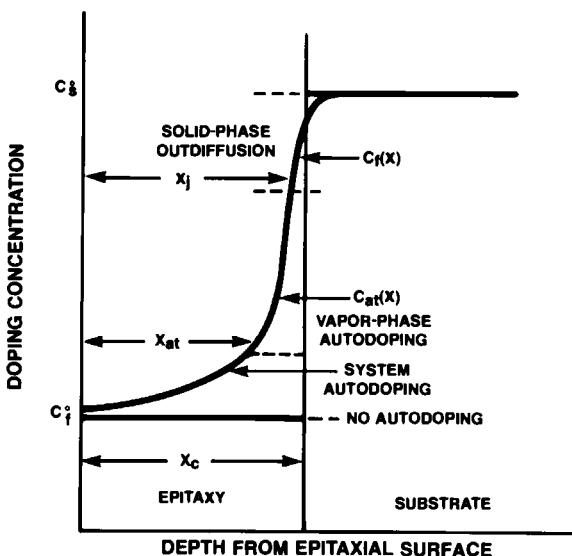


FIG. 19. Sketch of the doping concentration versus depth from the epitaxial surface. The stepwise profile is an ideal case in which autodoping and outdiffusion do not occur. The curved profile is a real case resulting from the incorporation of unintentionally doped impurities.

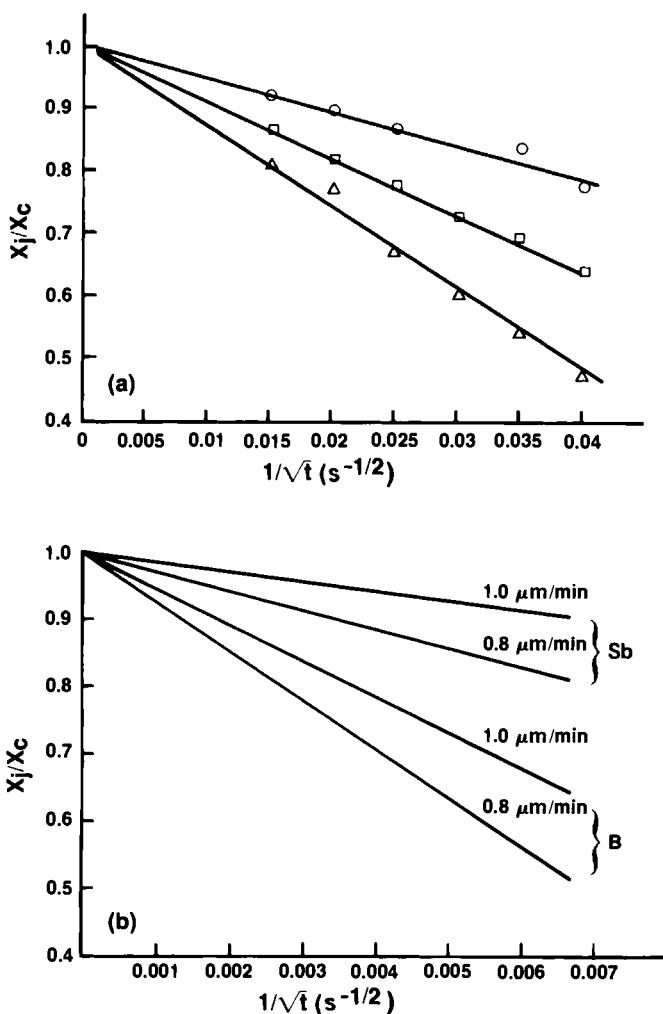


FIG. 20. (a) Plot of X_j/X_c versus $1/t^{1/2}$ for different growth rates on phosphorus-doped substrate: Growth temperature = 1125°C; \circ , 0.5 $\mu\text{m}/\text{min}$; \square , 0.3 $\mu\text{m}/\text{min}$; \triangle , 0.2 $\mu\text{m}/\text{min}$. [From Price and Goldman (1979). Reprinted by permission of The Electrochemical Society, Inc.] (b) Plot of X_j/X_c versus $1/t^{1/2}$ for Sb- and B-doped substrates: Growth temperature = 1150°C.

1.5.2.2 Autodoping

Gas-phase autodoping is the result of impurities being transferred from the substrate to the vapor phase and then being incorporated into the epitaxial films. A great number of models have been proposed in the

literature to describe the autodoping behavior in silicon. Thomas *et al.* (1962) have suggested a model which includes three sequential steps: (1) dopant and silicon atoms are evaporated nonpreferentially from the substrate surfaces; (2) the evaporated elements mix with the input gas and reestablish the gas-phase concentration; and (3) silicon and dopant atoms are deposited on the epitaxial layer with the ratio as that in the gas phase. Grossman (1963) assumed that a dopant atom is reincorporated into the epitaxial layer at a rate proportional to the growth rate and surface concentration. In both cases they predicted that the impurity concentration decreases exponentially from the substrate–epitaxy interface with an increase in epitaxial layer thickness. The model based on the trapping of adsorbed impurities suggested by Wong and Reif (1985) and Wong *et al.* (1985) also predicted the exponential decay of impurity concentration from the interface:

$$C_{at}(X) = fN_A^0 \exp(-X/X_m) \quad (1.5.7)$$

where f is the trapping factor which is a function of growth rate, N_A^0 the surface adsorption density before deposition, X the distance from interface, X_m the transition width which is a function of growth rate and desorption coefficient.

The autodoping from a localized diffused region (e.g., buried layer) includes both vertical and lateral autodoping. Figure 21a shows a schematic drawing of these two types of autodoping. Vertical autodoping is indicated by arrow A in which the dopant is evaporated from the buried layer and incorporated into the epitaxial layer directly above the diffused buried layer. Lateral autodoping is indicated by arrow B in which the dopant is evaporated from the buried layer and spread laterally into the epitaxial layer. Figure 21b shows the plot of doping concentration profiles measured along the dotted lines in Fig. 21a. The measurement of the lateral autodoping is made at a fixed distance away from the buried layer (typically 100 μm). Srinivasan (1980) suggested a model to describe the maximum concentration in the lateral autodoping as

$$C_1 = \text{const } \exp(\beta^2 t_p) \operatorname{erfc}(\beta t_p^{1/2}) \quad (1.5.8)$$

where t_p is the baking time, and $\beta = K/(D)^{1/2}$, where K and D are the evaporation velocity and solid diffusivity, respectively, of the dopant in silicon and are an Arrhenius function of temperature. Equation (1.5.8) shows that the prebake cycle is a critical parameter in determining lateral autodoping. This model has also been used to predict the effect of temperature, growth rate, growth pressure, and gas flow on lateral autodoping (Srinivasan, 1983).

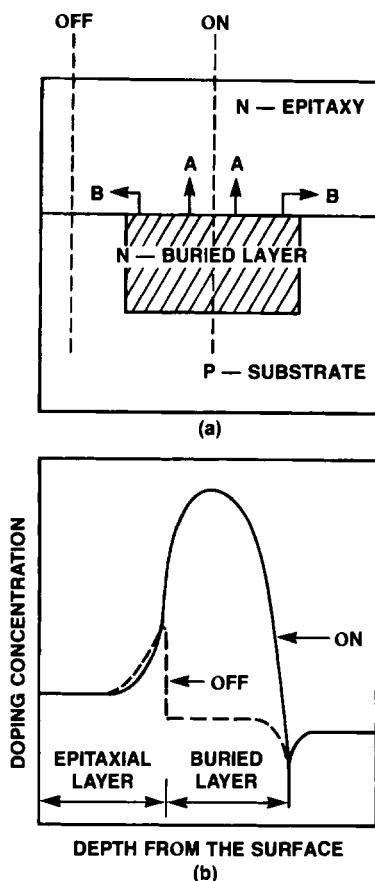


FIG. 21. (a) Schematic representation of vertical and lateral autodoping. (b) Plot of doping concentration profiles measured along the dotted lines in (a).

1.5.3 Calculation of Impurity Redistribution

Several computer models have been devised to calculate the redistribution of impurities in the epitaxial layers. The first comprehensive model was developed by Langer and Goldstein (1974). The method involves numerically solving the diffusion equation of Fick's second law with certain initial and boundary conditions. This model accounts for both front- and back-side autodoping during epitaxial growth as well as impurity redistribution during further high-temperature processing. Later, Antoniadis *et al* (1978) developed a computer program for IC process modeling and simulation, which is referred to as SUPREM, an acronym for the Stanford University process engineering models program. SUPREM includes epitaxy modeling and other processes such as ion implantation,

diffusion, and thermal oxidation. The SUPREM programs are widely used since their softwares are readily available. The epitaxy model used in SUPREM is similar to that of Langer and Goldstein. However, autodoping from both the back and front sides of wafers is omitted. This may account for a slight underestimation of the transition width when the epitaxial layer is deposited on a heavily doped substrate. Figure 22 shows the comparison of measured doping profiles and calculated profiles from SUPREM III, which is a recent version of the SUPREM program.

A new model has been developed by Reif and Dutton (1981). This model considers gas-phase dynamics and physiochemical processes at the growing interface, and can predict the impurity distribution resulting from either a time-dependent or time-varying partial pressure of gas-phase dopant. A computer calculation based on Eq. (1.5.7) has been made by Wong and Reif (1985). The results seem to agree well with the experimental data obtained from three different types of reactors.

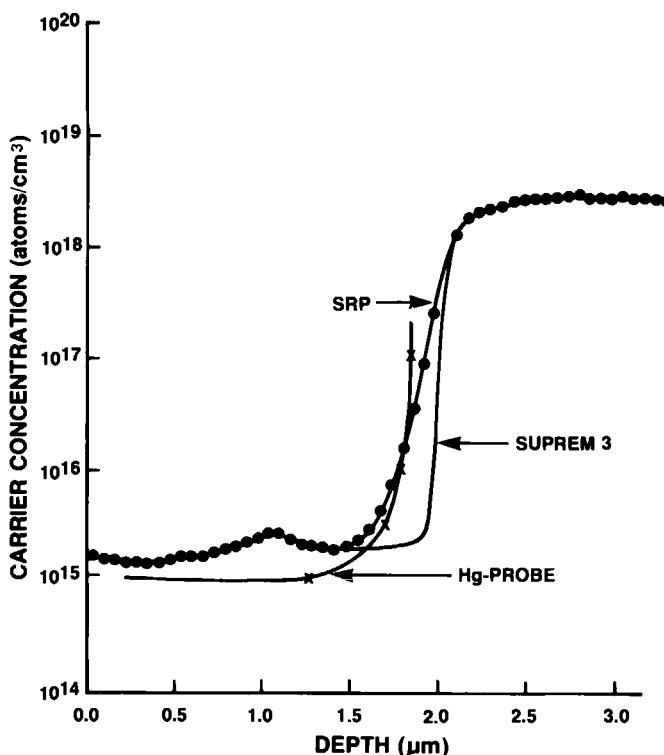


FIG. 22. Measured and calculated (SUPREM) doping profiles in a 2- μm thick epitaxial layer deposited on a boron-doped substrate.

1.6 SURFACE MORPHOLOGY AND EPITAXIAL DEFECTS

The surface morphology of epitaxial layers is strongly affected by the nature of the substrate and the growth parameters. The growth parameters include growth temperature, pressure, and growth rate, which are related to the Cl/H ratio and the supersaturation of silicon-containing gasses. The substrate factors include the orientation, crystallographic defects, and surface contaminants. The substrate cleaning procedure for removal of contaminants prior to the epitaxial growth will be given in a later section. The other factors will be discussed in this section.

The crystallographic orientation of the substrate can affect the surface morphology of the epitaxial films. Growth of smooth planar epitaxial layers on a (100) or (110) surface can be obtained. However, it is very difficult to grow a smooth layer on a (111) surface. As pointed out earlier, silicon (111) surfaces contain no atomic steps. Instability inherent in such singular surfaces always results in the growth of epitaxial layers with morphology containing pyramids or terraces. Misorientation from the (111) by at least 0.5° is required for the growth of smooth planer epitaxial layers [Rode *et al.*, 1977].

Surface contaminants or crystallographic defects in the substrates can cause local deviations from smoothness in the epitaxial surface. Epitaxial stacking faults and spikes are the most commonly observed defects resulting from substrate surface contamination. Epitaxial spikes exhibit local protrusion without any crystallographic pattern. Epitaxial stacking faults are crystallographic in nature and can result from an extra-atomic layer (extrinsic) or missing atomic layer (intrinsic) in the (111) plane. A stacking fault intercepting with a (100) water surface appears as a line, while one intercepting with an off-oriented (111) surface appears as a triangular cone. Figure 23a shows the photomicrograph of a stacking fault intersecting a (111) surface. Figure 23b shows its surface profiles a-d, measured along arrows a-d marked on Fig. 23a. These measurements show that the bottom triangular cone is an elevation, and the center ridge of the cone is a depression. The center ridge is the location where the stacking fault terminates on the surface. This can be more clearly seen by the preferential etching of the surface. Figures 24a-c show the etched surfaces of single, double, and triple stacking faults, while Fig. 24d shows a combination of a spike and a triple stacking fault. These photomicrographs show that a single origin of surface contaminant can generate a single stacking fault, multiple stacking faults, or the combination of stacking faults and an epitaxial spike.

The nature of the surface contaminants which cause the formation of epitaxial stacking faults has been studied extensively. A good review

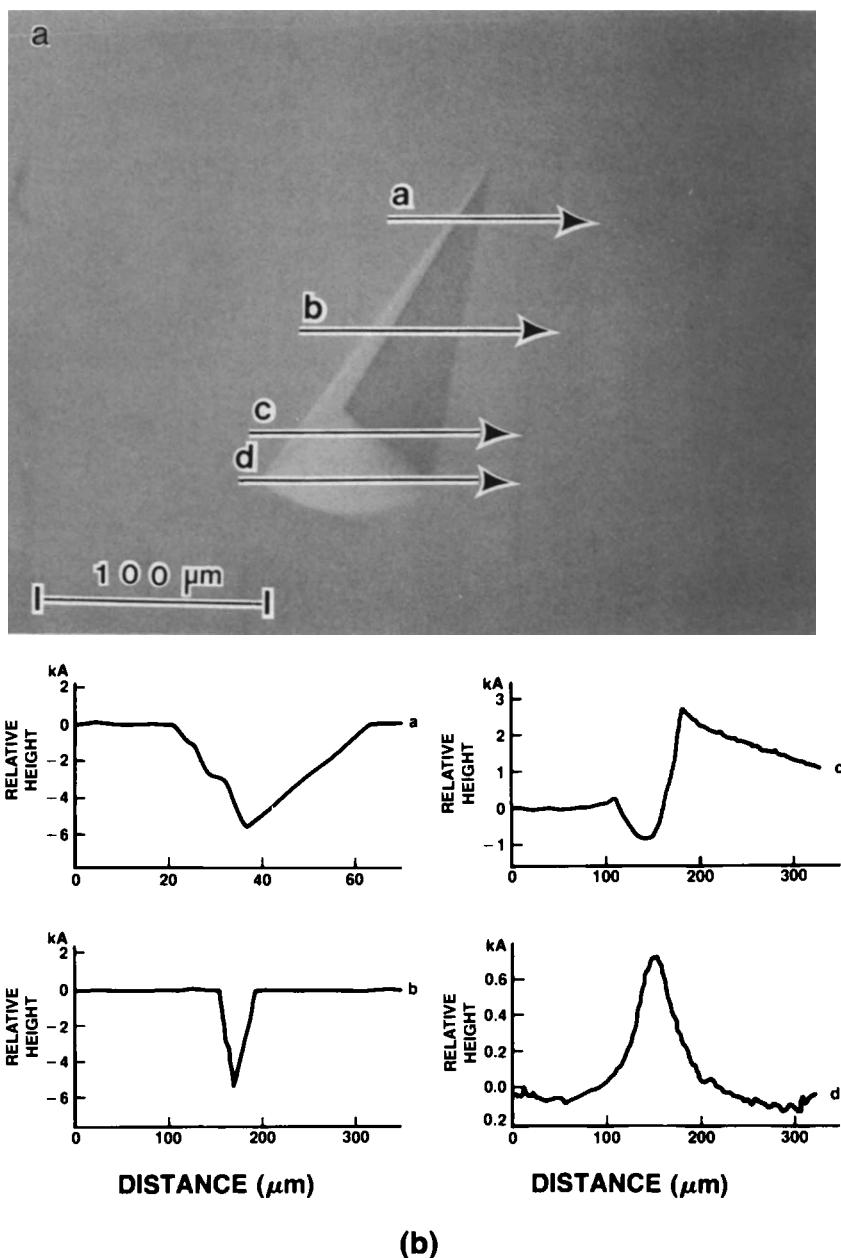


FIG. 23. (a) Photomicrograph of a stacking fault intercepting with the (111) surface. (b) Surface profile of the stacking fault shown in (a). The curves a-d correspond to the measurements along arrows a-d, respectively.

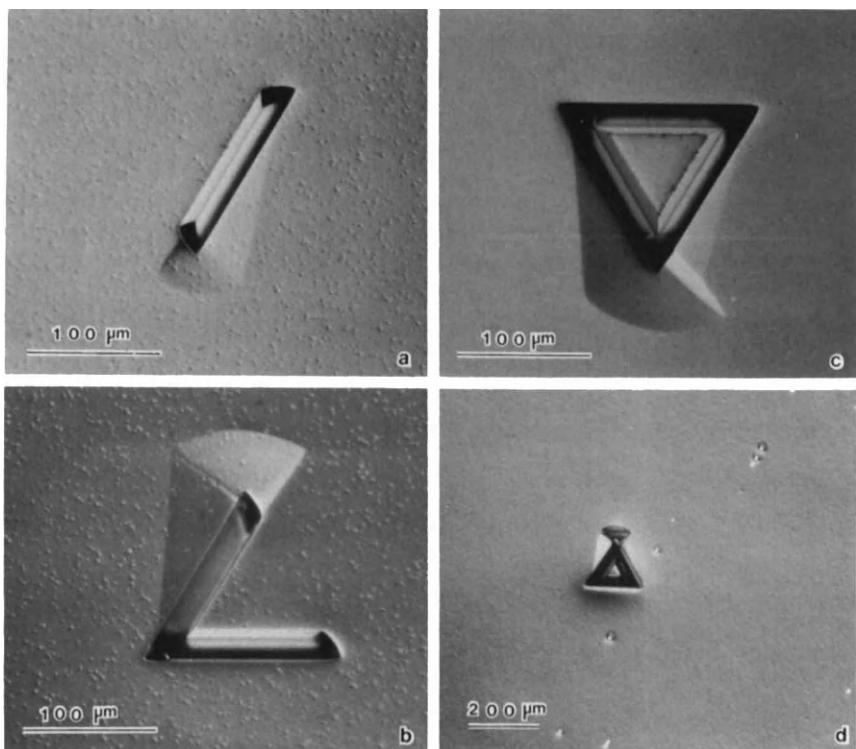


FIG. 24. (a), (b), and (c) Photomicrographs of the etched surfaces revealing single, double, and triple stacking faults respectively. (d) Photomicrograph showing a cluster of defects consisting of a spike and three epitaxial stacking faults originating from a common source.

article of this subject has been given by Stowell (1975). Contamination on the substrate surface can result from either external or internal sources. The internal source is mainly related to the outdiffusion of impurities from the substrate. Examples include oxygen (Finch *et al.*, 1963), metals (Pomerantz, 1967), and segregation and microprecipitation of metallic impurities (Thomas and Franccombe, 1971). This has been verified from the fact that a substrate with a low minority carrier lifetime which contains a higher concentration of metallic impurities has been found to have a higher density of stacking faults (Thomas and Franccombe, 1971). Process-induced defects can also be an origin for epitaxial stacking faults. Figure 25 shows the propagation of an oxidation-induced stacking fault to form an epitaxial stacking fault. Pomerantz (1967) observed a higher epitaxial stacking fault density when the substrate had been oxidized prior to the epitaxy. This results from the formation of oxidation-induced stacking faults in the

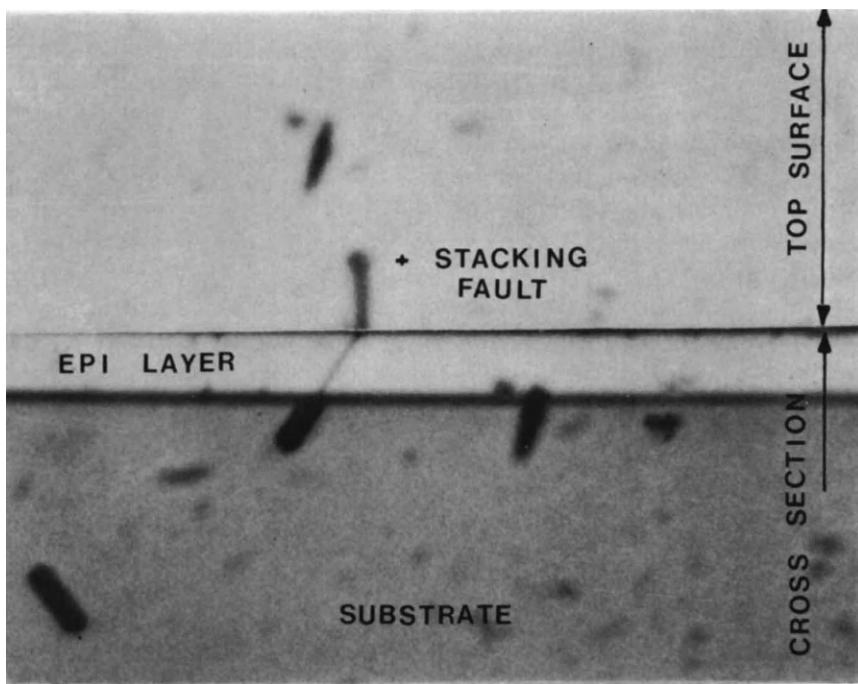


FIG. 25. Beveled and etched surface showing the propagation of an oxidation-induced stacking fault from the substrate into the epitaxial layer to form an epitaxial stacking fault. [From Liaw *et al.* (1984b). Published with permission of Solid State Technology, published by Technical Publishing, a company of Dun and Bradstreet.]

substrate by the thermal oxidation. An obvious external source of surface contamination is the impurity residue resulting from poor surface cleaning. Other external sources include particulate contamination. The particulates may come from the disturbance of the graphite susceptor prior to the epitaxial run. Generation of electrostatic charges in the reactor by its own power source can enhance the affinity of particulates onto the substrate surface.

Epitaxial layer quality is greatly degraded by the formation of hillocks on the surfaces. The formation of hillocks is primarily affected by the growth parameters. Chang and Baliga (1984) reviewed this subject and have shown that the hillock density increases exponentially with growth rate or inverse absolute temperature ($1/T$). Joyce (1968) found that the high temperature (1200°C) growth using SiHCl_3 resulted with smooth and featureless surfaces while a low-temperature growth resulted with rough surfaces. It can be generalized that a continued increase in growth rate or $1/T$ will change the surface morphology from a mirror-finish, to orange

peel, haze, and finally to a polycrystalline film. Chernov (1977) has suggested that formation of hillocks or pyramids is a result of the two-dimensional nucleation growth mechanism. He has developed a model to predict the surface morphology based on this growth mechanism and use of the contours of the chemical potential at the growing interface. This model agrees fairly well with the experimental results which show that the slope of a hillock (or a pyramid as one shown in Fig. 13) is increased by a decrease in temperature, increase in supersaturation, or increase in the Si/Cl ratio.

The surface morphology of polycrystalline silicon deposited on grooved or depressed surfaces is also affected by the deposition parameters. Van den Brekel (1977) has correlated the morphology of the deposited surfaces with N_{cvd} . He has found that spikes or protrusions were observed at the edges of grooves when a high N_{cvd} was used. Uniform coverage over the grooves was found when a low N_{cvd} was used. High N_{cvd} is equivalent to the deposition conditions in which the surface reactions are rapid and the deposition rate is limited by the diffusion through the boundary layer. It can be physically visualized that the concentration gradient of the silicon-containing gas is highest at the edge of the grooves. Once the silicon-containing gas species diffuse through the boundary layer they immediately incorporate into the silicon lattice without surface migration because of the rapid surface reaction.

Surface planarity of the epitaxial growth over selective areas uncovered by an oxide or nitride mask is also affected by the deposition parameters. Deposition using a low N_{cvd} condition resulted in a better planar epitaxial surface. Tanno *et al* (1982) and Voss and Kurten (1983) have used low temperature and/or reduced pressure which are equivalent to lowering N_{cvd} to produce planar surfaces. Figure 26 shows the surface morphologies of epitaxial islands grown at different temperatures and pressures. It can be seen that the surface roughness increases with the growth pressure and temperature.

Dislocations in the epitaxial silicon do not affect the morphology or planarity of the surface. However, the dislocations can affect device performance. Stowell (1975) has reviewed the sources for dislocation propagation into the epitaxial layers. The possible sources include (1) the extension of substrate dislocations, (2) plastic deformation of the film, (3) the accommodation of translational and rotational displacement between the islands that are close to the epitaxial orientation, and (4) the formation of dislocation loops by the aggregation of point defects.

Dislocations in the substrate will extend into the epitaxial layer only when they terminate at the free surface of the substrate. Moreover, after the epitaxial layer has grown to an appropriate critical thickness, the

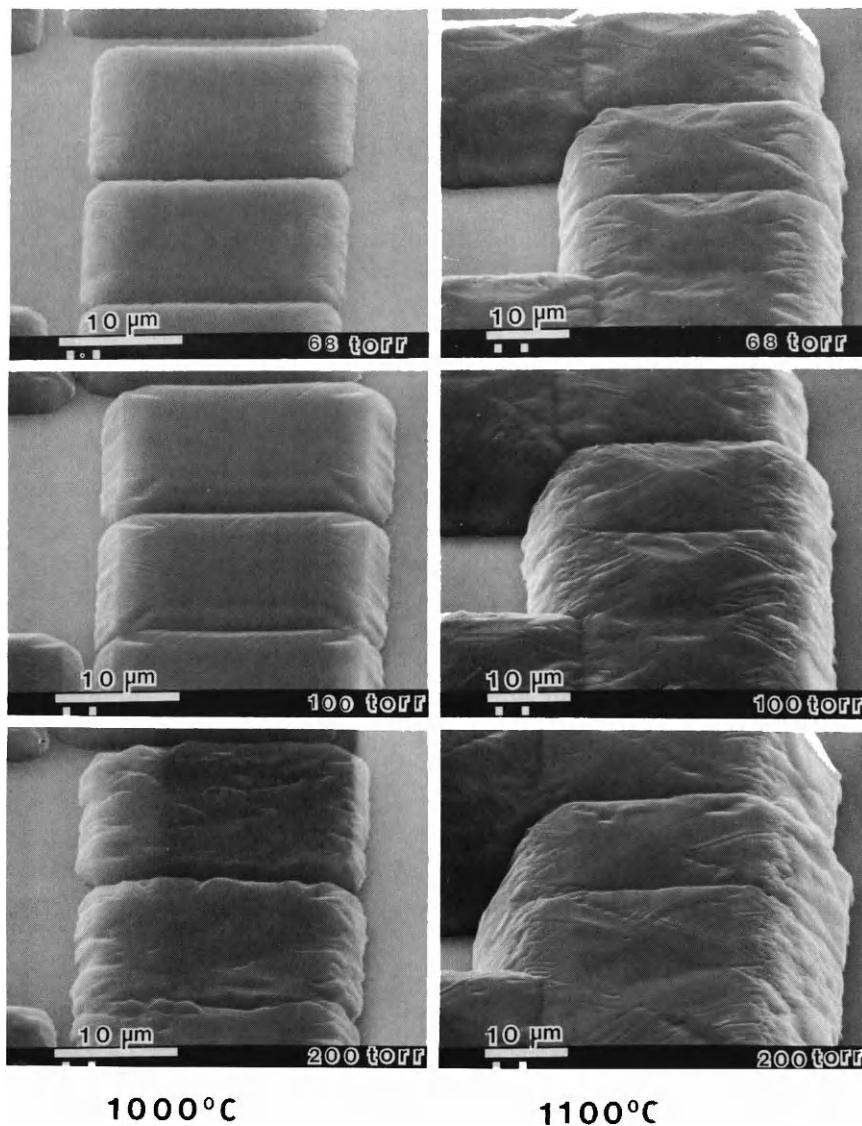


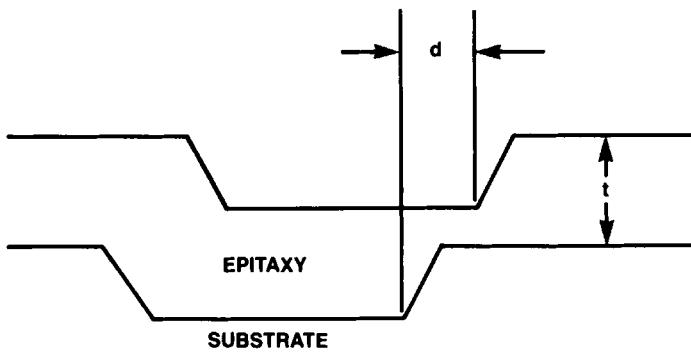
FIG. 26. Effects of temperature and pressure on surface morphology of selective epitaxial islands.

dislocation will tend to bend into the interface to produce misfit relief. At a typical growth rate of a few tenths of micrometer per minute and at a temperature of 1150°C it is expected that the bending of the dislocations should be completed after approximately five min of growth (Blanc, 1978). Dislocations extending from the substrate can be annihilated by adjoining dislocations of the opposite sign. Dislocations can also change their direction of propagation and stop if they terminate at the wafer edge. Overall, since the dislocation density in the state-of-the-art silicon substrate is very low, epitaxial dislocations contributed from this source can be negligible.

Dislocations can be generated by plastic deformation which is induced either by thermal or mechanical stress. Thermal stress is perhaps the most common source of dislocation generation which causes slip in the epitaxial layer. Bloem and Goemans (1972) have shown that the slip is most likely formed when the product of the radial temperature gradient of the epitaxial wafers times the wafer diameter has exceeded a critical value. McDiarmid *et al.* (1984) have confirmed that slip is definitely associated with radial temperature gradients on the order of 25°C or higher when the epitaxial growth is carried out at 1200°C. The stress induced from the lattice mismatch between the substrate and epitaxial layer is relatively small (between 10^{-4} and 10^{-5}) even when the substrate is heavily doped with boron up to 10^{19} atoms/cm³. Therefore, misfit dislocation density should be low, which is confirmed experimentally to be in the range of 30 to 250/cm. On the contrary, when a heavily boron doped ($10^{20}/\text{cm}^3$) layer was grown on an undoped substrate, a much higher density of misfit dislocations (i.e., $>5 \times 10^3/\text{cm}$) was observed (Blanc, 1978).

1.6.1 Pattern Shift

The substrates used for the fabrication of bipolar integrated circuits are diffused or implanted with a dopant in localized regions on the front surface of wafers. The localized diffused regions are referred to as buried layers. The surfaces of the buried layers are generally depressed with a depth of approximately 1000–3000 Å. An epitaxial layer grown on the buried layer will replicate the surface feature of the underlying substrate. It is desirable to obtain a perfect replication. Any lateral displacement of the pattern between the substrate and epitaxial layer is referred to as pattern shift. The primary cause of pattern shift is the anisotropy of the growth rate of the crystallographic planes that bound the bottom and sides of the depressed regions. Figure 27a depicts a pattern shift in which two parallel step-edges of the depression in the epitaxial layer displace toward the right with a distance d . Figure 27b is a photomicrograph in which the pattern shift is revealed by the bevel-and-stain technique. In this case the shift of



(a)

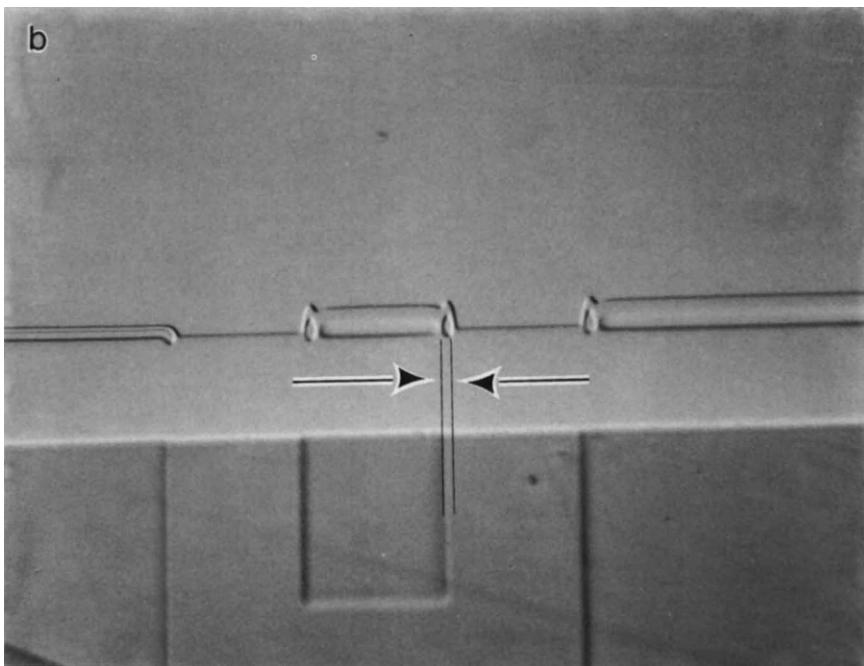


FIG. 27. (a) Pattern shift in which two parallel step-edges of the depression in the epitaxial layer displace toward the right a distance d . (b) Photomicrograph in which the pattern shift is revealed by the bevel-and-stain technique.

the pattern does not change the outline dimensions. However, when two parallel step-edges shift in opposite directions, the outline dimensions will alter. This is referred to as pattern distortion. Examples are shown in Fig. 28 which include the photomicrographs of patterned surfaces together with plots of height versus distance for the depressed regions. These surface profiles were measured along the arrows shown in the photomicrographs. Figure 28a is the original buried layer pattern. Figure 28b shows the increased pattern dimensions in the epitaxial layer resulting from the growth under reduced pressure. Figure 28c shows the decreased pattern

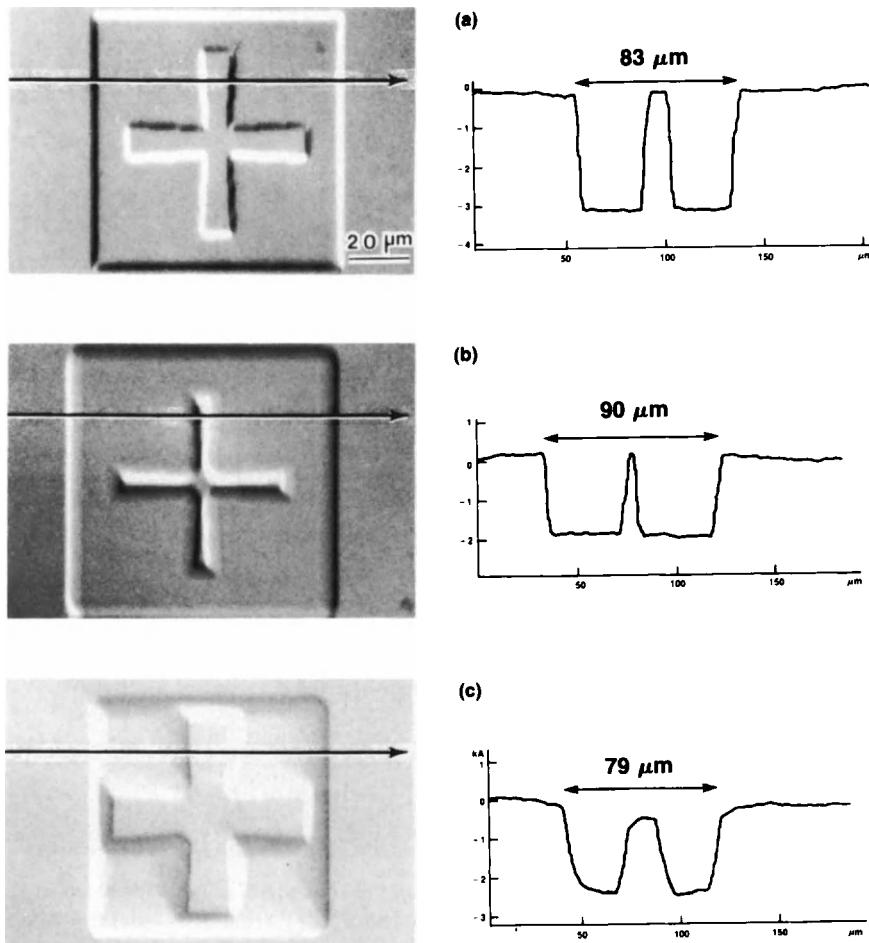


FIG. 28. (a) Photomicrograph showing the original buried layer pattern. (b) Increased pattern dimensions in the epitaxial layer resulting from reduced pressure growth. (c) Decreased pattern dimensions resulting from atmospheric pressure growth.

dimensions resulting from growth at atmospheric pressure. The formation of facets at step edges is also seen in this photomicrograph. The faceting decreases the surface planarity in the epitaxial layer and therefore is not desirable. Another problem that sometimes occurs during epitaxial growth is the obliteration of one or all edge steps. This is referred to as pattern washout. Pattern shift, pattern distortion, and pattern washout are strongly dependent on the substrate orientation as well as growth parameters which include growth pressure, temperature, silicon source gas, and growth rate. Studies on these parameters have been made by Drum and Clark (1968), Lee *et al.* (1977), Weeks (1981), and Boydston *et al.* (1983). The following section summarizes the effect of substrate and growth parameters:

- (1) Pattern shift and distortion are more severe in (111) wafers than in (100) wafers. The pattern shift in (111) wafers generally occurs in a direction opposite to the direction of the 3–5° tilt of the (111) axis. Although the pattern shift in (100) wafers is small, a slight misorientation of the substrates from the (100) plane may lead to a significant shift, particularly when low growth rates and low growth temperatures are used.
- (2) Pattern shift and faceting can be reduced by high growth temperatures. For atmospheric growth, reducing growth temperature causes heavy faceting and an asymmetry in the outline dimensions. A large reduction in the deposition temperature (e.g., to 1150°C using SiCl₄) may obliterate the pattern.
- (3) The facets can be reduced by using low pressure growth (as shown in Fig. 28b). However, this is traded off by the increase in pattern dimensions.
- (4) At atmospheric pressure, low growth rates reduce the pattern shift and faceting.
- (5) Pattern shift can be reduced by the use of the silicon source gas with the least chlorinated silane molecules.

1.6.2 Characterization of Epitaxial Silicon

1.6.2.1 Surface Defect Characterization

Manual inspection of surface defects on the epitaxial wafers by light backscattering is a well-established technique and has been used in the industry. The light source used a high-intensity tungsten lamp. Procedures for the visual inspection of wafers have been given in ASTM standard F523. In essence, the wafer is illuminated by an intense light beam. When the wafer surface is flat and free of surface defects, no light scattering will be observed in the reflected beam. This reflected beam is called the specular beam. The entire surface shows complete darkness when we view

from an angle other than that of the specular beam. The presence of defects on the surface causes a fraction of light to scatter in random directions. An observation of scattered light provides information on the location and size of surface defects. Such information can be recorded by using a photographic camera.

Advances in laser optics and data processing technologies have made automatic wafer scanners available. Automatic wafer scanners use the same principle as the visual inspection with the exception of replacing human eyes (or photographic cameras) with light detectors. Some scanners use only one detector to collect the reflection of a scattered beam. In this case the light collector encompasses a large fraction of reflected solid angle, approximately 70% of 2 sr (Galbraith, 1983). Other scanners use two detectors, one for the scattered beam and the other for the specular beam. The output of the detector signals can be processed and displayed in graphic and/or numerical formats.

We have studied epitaxial surface defects by using an Aeronca WIS 100 laser surface scanner which uses two collectors. The laser beam is incident to the wafer surface at a 15° angle from the normal axis. One collector is used to detect the specular beam and is called the light field collector. The other collector, which is called the dark field collector, detects the scattered beam and is placed at the normal axis. This detector encompasses only 5° of a solid angle of light collection. This type of scanner also provides information on the defects which are detected by the combination of light and dark field collectors. The surface defects detected by the dark field collector are those that reflect light isotropically, and these include particulates, scratch marks, and tweezer damage. Crystallographic defects such as stacking faults which reflect light anisotropically and reduce the intensity of specular beam, are detected by the light field detector. Figure 29 compares the light backscattered photograph and the laser surface defect map of the same wafer. The surface damage along the periphery of the wafer is clearly seen in both figures. Automatic laser wafer scanners can also be used for monitoring defects generated by the epitaxial growth process. This is done simply by counting of each flaw type detected by the laser scanner before and after the silicon epitaxial growth.

Epitaxial surface defects have often been characterized by the chemical etching technique. A preferential etchant which etches at a faster rate at defect sites than on a perfect region can reveal the crystallographic defects. Dislocations, dislocation loops, stacking faults, and swirls are examples of defects that can be revealed by a preferential etchant. Three widely used preferential etchants are the Sirtl, Secco, and Wright etches. The composition of these etchants and the appearances of the defects have been given by Fejes *et al.* (1983).

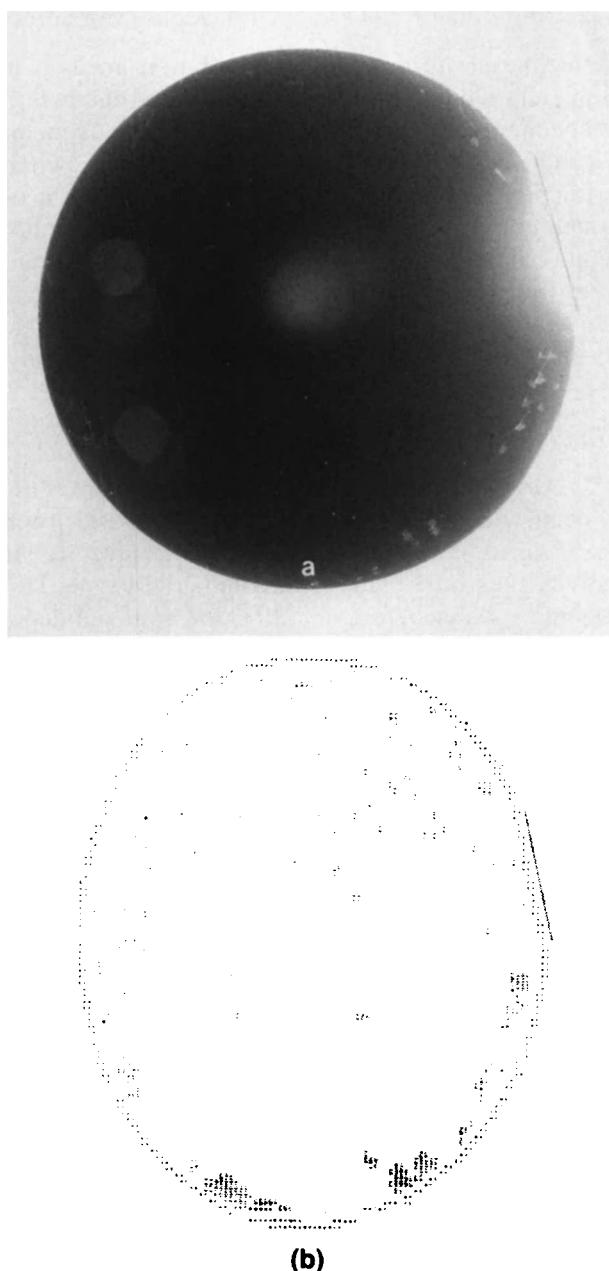


FIG. 29. Comparison of (a) a light backscattered photograph with (b) the laser scanned surface defect map of the same wafer.

1.6.2.2 Measurements of Thickness and Doping Concentration

Epitaxial thickness and doping concentration are two fundamental material parameters which can affect the electrical characteristics of devices. The dependent characteristics in bipolar devices include junction breakdown voltage, capacitance, transistor gain, and switching speed. Capabilities for precise control and accurate measurement of these two material parameters are very critical. The measurements become more difficult as epitaxial layers are reduced in thickness to the micrometer or submicrometer range which is needed for the VLSI technology. An excellent article that reviews the characterization techniques for epitaxial silicon has been given by Kulkarni (1983). Only the commonly used techniques will be briefly presented here.

1.6.2.2.1 Thickness Measurement Techniques

1.6.2.2.1.1 Gravimetric Technique This technique is the most simple and has been widely used. It is particularly useful when the other techniques have failed to measure such an epitaxial layer as one deposited on high-resistivity substrates of the same conductivity type. This technique involves weighing a wafer before and after the epitaxial deposition. The thickness is calculated from the weight gain by knowing the surface area and density of the wafer. Limitations of this technique are: (1) it only measures the average film thickness and cannot provide information on thickness uniformity and (2) its accuracy becomes doubtful when the substrate is etched by HCl in the prebake cycle. The degree of confidence of this technique depends on the accuracy in determining the etch rate of silicon by HCl.

1.6.2.2.1.2 Junction Exposing Technique This technique is applicable to epitaxial layers that are deposited on substrates of opposite conductivity type and a *p-n* junction is formed at the epitaxy-substrate interface. Junction exposing methods include (1) angle lap, (2) wheel grind, and (3) cleavage of the wafers. After the junction is exposed, it can be revealed by a chemical stain. The junction depth in the angle lap samples can also be measured by the spreading resistance probe or merely by optical measurements. The junction depth in the wheel grid samples can be obtained by the trigonometric method. Figure 30 shows a cross-sectional view of a wheel ground sample (McDonald and Goetzberger, 1962). This method is commonly used not only for determining thin epitaxial layers but also for determining the junction depth formed by diffusion or ion implantation. The junction depth or the epitaxial thickness (X_j) is calculated according to

$$X_j = [R^2 - (W_1/2)^2]^{1/2} - [R^2 - (W_2/2)^2]^{1/2} \quad (1.6.1)$$

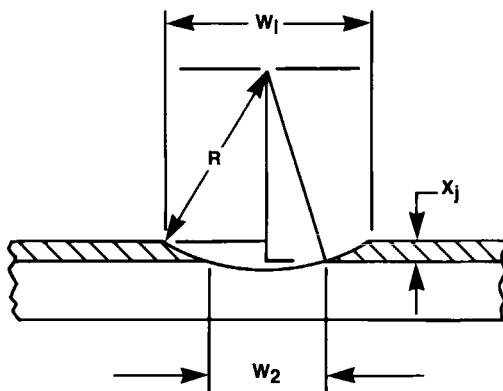


FIG. 30. Cross-sectional view of the parameters used for the epitaxial thickness measurement by the wheel ground technique. [From McDonald and Goetzberger (1962). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

where R is the radius of the grinding wheel, W_1 the width of the epitaxial surface ground, and W_2 the width of the substrate surface ground.

1.6.2.2.1.3 Infrared Spectrometric Techniques The infrared spectrometric technique includes the dispersive and Fourier transform (FTIR) reflective methods. The dispersive reflectance technique is applicable for measuring a layer greater than 2 μm thick. The epitaxial layer must be deposited on substrates of the same conductivity type. The resistivity of the substrate must be less than 0.02 ohm cm and that of the epitaxy must be greater than 0.1 ohm cm. The reflectance of the specimen is measured as a function of wavelength by using a dispersive infrared spectrophotometer. The reflectance spectrum exhibits successive maxima and minima resulting from the interference of the beams reflected from the epitaxial surface and the epitaxy–substrate interface. The thickness of the epitaxial layer is calculated using the wavelengths of the extrema in the reflectance spectrum, optical constants of the layer and the substrate, and the angle of incidence of the infrared beam upon the specimen. The procedure of such calculations has been described in ASTM F-95. In essence, the epitaxial thickness is determined based on

$$T_n = \frac{[(P_n - \frac{1}{2}) + (\phi_2/2\pi)](\lambda_n)}{2(n_i^2 - \sin^2 \theta)^{1/2}} \quad (1.6.2)$$

where T_n is the epitaxial thickness, P_n the orders of the interference fringe associated with λ_n , ϕ_2 the phase at the epitaxy–substrate interface, n_i the index of refraction of the epitaxial layer, θ the angle of incidence of the infrared beam, and λ_n the wavelength of the n th interference fringe.

The order of the interference fringe, P_n , can be calculated by the difference in the orders of the extrema considered and the phase shifts for the wavelengths at the extrema (formula and example of the calculations are given in ASTM F-95). The phase shift as a function of wavelength and resistivity of the substrate has been evaluated by Schumann (1969) and has also been tabulated in ASTM F-95.

The FTIR reflection technique can measure epitaxial film thicknesses smaller than can be measured by the dispersive technique. The FTIR uses a Michelson interferometer to differentiate wavelengths instead of gratings which are used in a dispersive IR. Figure 31 shows an arrangement used for epitaxial film thickness measurement. Collimated radiation from the source is incident on the beamsplitter. Half of the energy is incident on the fixed mirror, while the other half is reflected to the moving mirror. After reflection, the two beams from each arm recombine at the beam-splitter where the beams constructively or destructively interfere, depending on the difference in the optical paths between the two arms of the interferometer. The modulated beam is then directed to the epitaxial sample with an incident angle θ . The light is reflected from the sample and passes on to the detector. The energy detected originates from light reflected from the surface of the epitaxial film and light reflected from the

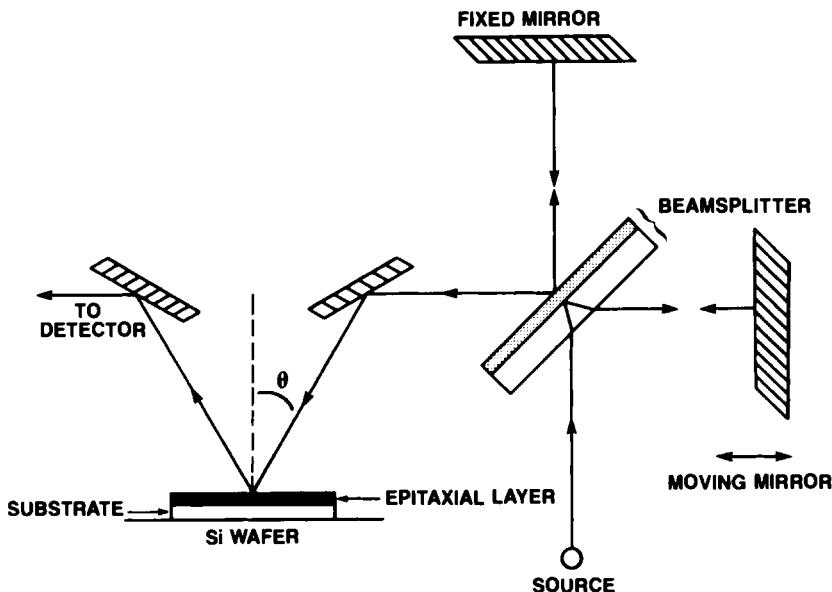


FIG. 31. Arrangement of optics used for the epitaxial layer thickness measurement by the FTIR technique.

epitaxy-substrate interface. The amplitude and phase ϕ of the two beams reaching the detector is a function of the position of the moving mirror. Assuming that the two mirrors are equidistant from the beam splitter, the detector will measure a large signal, since the reflected beams from both mirrors are in phase. This large signal shown in the interferogram is called the zero-order reflection or centerburst. As the moving mirror changes positions, the reflected beams will encounter destructive interference; thus the detector receives little or no signal. However, when the moving mirror is displaced a distance X , which is equal to the beampath distance from the sample surface to the epitaxial-substrate interface, a constructive interference occurs; a strong peak in the interferogram will be detected. This peak is called the first-order reflection or sideburst (Fig. 32). The epitaxial thickness T is related to the displacement distance X in which the sideburst occurs as

$$T = X/(2n_i \cos \theta) \quad (1.6.3)$$

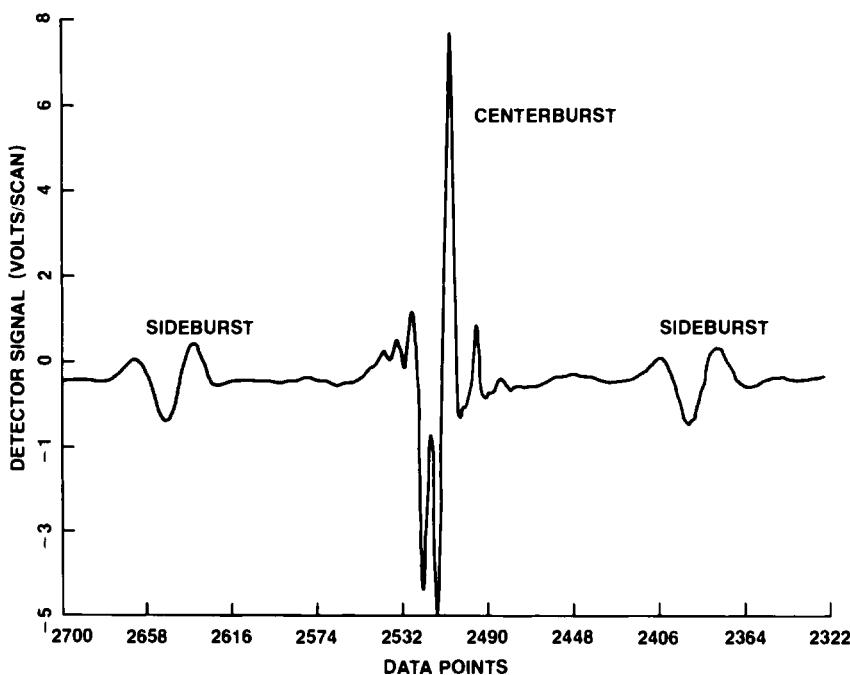


FIG. 32. A reflectance interferogram of a 5.2 micrometer thick epitaxial film measured by the FTIR technique. [Courtesy of R. Boyle, Motorola, Inc. Semiconductor Products Sector.]

This assumes that the phase shift at the epitaxial surface is the same as at the epitaxy–substrate interface ($\phi_s = \phi_{e-s}$). Normally $\phi_s > \phi_{e-s}$, which affects the shape of the peak but not its location in the Fourier domain. Algorithms can be generated to correct for this difference. Since a He-Ne laser is used as a clock for the sampling rate, this displacement of the mirror can be precisely measured. Consequently, this method is able to measure epitaxial layer thicknesses of less than 1 μm . By measuring standard refractive index systems, absolute thicknesses can be determined and correlated with unknown sample thicknesses.

1.6.2.2.2 Measurements of Doping Concentration

1.6.2.2.2.1 Pulsed C–V Technique The vertical doping concentration profiles in the epitaxial layer can be measured by the *C–V* technique using either an MOS capacitor or a Hg-probe, which form a Schottky barrier with silicon. The relationship between the carrier concentration N and the capacitance C resulting from a reverse voltage V can be expressed as

$$N = \frac{2}{q\epsilon A^2 d(1/C^2)/dV} \quad (1.6.4)$$

where q is the electric charge, ϵ the dielectric constant, and A the area of the capacitor. Thus, the carrier concentration can be obtained from the slope of the $1/C^2$ versus V plot. Typically it is preferable to have the plot of N versus depth from the epitaxial surface. This can be obtained using the relationship between the capacitance and depletion depth W as

$$W = \epsilon A/C \quad (1.6.5)$$

When the epitaxial layer is thin and its resistivity is high the depletion width due to the *C–V* reverse bias pulse can extend to the substrate. If the doping concentrations in the substrate and the epitaxial layer are significantly different, their interface can be identified as the location where an abrupt change in carrier concentration occurs. Thus, this technique has also been used for epitaxial layer thickness measurements. The basic circuit used for the *C–V* measurements has been reported by Goetzberger and Nicollian (1967).

The capacitors used for the doping profile evaluation can also be used for minority carrier generation lifetime measurements if the gate of a capacitor includes a guard ring to prevent surface current. For lifetime measurements the capacitor is pulsed into inversion. The minority carrier lifetime is evaluated from the Zerbst plot (Zerbst, 1966). The slope of the straight line portion of the Zerbst plot is proportional to $(1/t_g)$, where t_g is the generation lifetime. Detailed procedures for the lifetime measurements have been described by Heiman (1967).

1.6.2.2.2.2 Spreading Resistance Probe The spreading resistance probe measures the apparent resistance resulting from the point contact between a metal probe and the semiconductor surface. All the potential drop occurs within 1.5 times the effective radius a of the electrical contact. Therefore, the spreading resistance R_s depends mainly on the resistivity of the local material ρ and insignificantly on the Schottky resistance. The relationship between the spreading resistance and resistivity of the material is

$$\rho = 4aR_s/n \quad (1.6.6)$$

where n is the number of current carrying probes across which the potential drop is measured. This relationship is valid under the assumption that the probe is in contact with a semi-infinite material. This assumption does not hold for the measurement of thin epitaxial films. Correction factors have been devised for (1) a shorting boundary and (2) insulating boundary (Gardner *et al.*, 1967; Schumann, Jr. and Gardner, 1969). For epitaxial n/n^+ or p/p^+ structures the former correction factor is used, while p/n or n/p structures require the use of the latter correction factor.

1.7 EPITAXIAL REACTORS

1.7.1 Classification and Evolution

Chemical vapor deposition epitaxial reactors can be classified according to the direction of gas flow with respect to the substrate surface. Those in which gas flow is perpendicular to the main surfaces of the wafers are called vertical reactors. A very early single-wafer vertical reactor is shown in Fig. 33a. The reactors in which the gas flow is parallel to the main surfaces of wafers are called horizontal reactors (Fig. 33b). Reactors can also be classified according to the shape of the susceptor. The reactor shown in Fig. 33a is also called the pedestal reactor. Figure 33c shows a vertical reactor that is also called the pancake reactor. Figure 33d shows a barrel, or cylinder, reactor. However, barrel reactors have never been referred to as horizontal reactor although the gas flow is parallel to main surfaces of the wafers.

The vertical reactor shown in Fig. 33a was first used by Theuerer (1961). The original construction was made of quartz. By the mid 1960s this type of reactor was scaled up to process several wafers per run. This reactor evolved into the pancake type with a rotary susceptor to improve uniformity. Although such reactors were popular during the 1960s, they did not enjoy rapid growth in the market place because of difficulty in scaling up to accommodate larger load sizes. By the early 1980s this type of reactor regained popularity because of its reliability and ability to deposit very uniform layers.

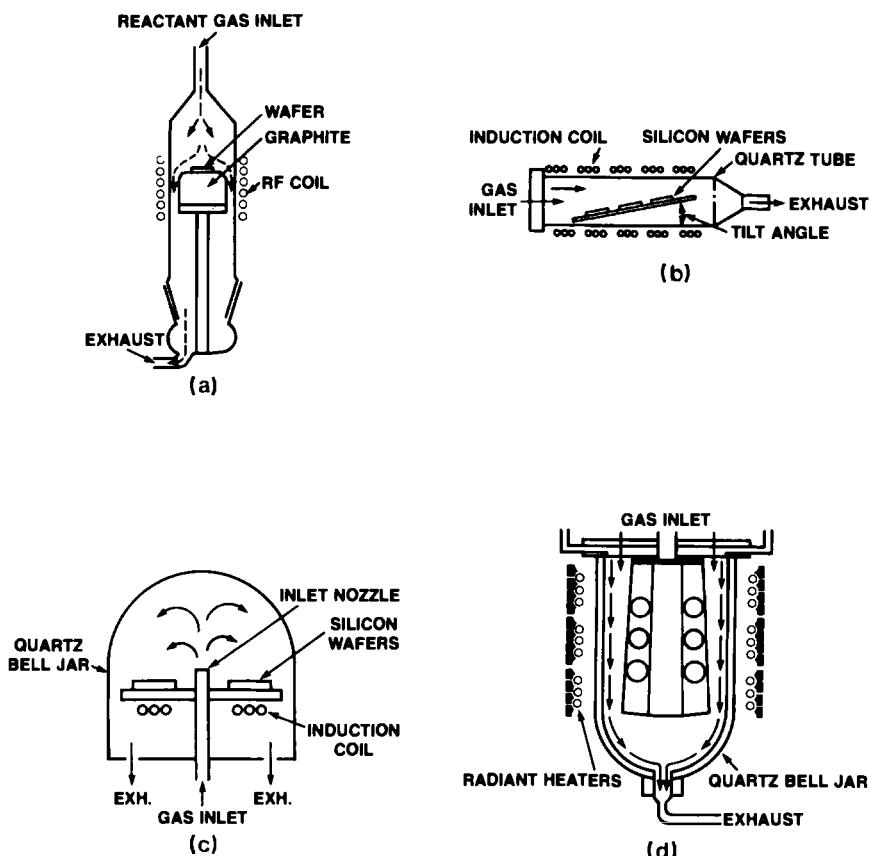


FIG. 33. Classification of epitaxial reactors. (a) Vertical, or pedestal reactor, (b) horizontal reactor, (c) pancake, or vertical, reactor, and (d) barrel reactor.

In the pancake reactors the wafers are loaded near the bottom of the bell jar. The gas mixture enters through the center of the susceptor and flows upward toward the top of bell jar. From there the flow spreads and mixes as it moves downward towards the wafers and the exhaust. The bell jar provides ample space for thorough mixing of the gases prior to reaching the silicon surface. The height-to-width ratio of the bell jar is a critical factor that determines the gas flow pattern in the reactor. In this type of reactor, all wafers are simultaneously exposed to the incoming gas mixture. Good thickness and doping uniformity are easy to obtain. Suzuki *et al.* (1985) further improved the epitaxial thickness uniformity in a laboratory pancake reactor by using a controlled supplemental gas adding system. This system consists of three gas injection nozzles 120° apart, and

gas is injected facing the susceptor to the spots where the concentration of silicon-containing gas from the main stream is lowest. By this technique the thickness variation has been improved to less than $\pm 1\%$. Therefore, it is anticipated that the pancake reactors can increase the load size further and still be able to maintain excellent epitaxial thickness uniformity.

Horizontal reactors were most popular in the 1970s because of the ease in scaling them up. This was accomplished by merely changing the reactor tubes from circular to rectangular in cross section so that they can accommodate a larger susceptor. Figure 34 illustrates the evolution of the load size in the horizontal reactors from the mid-1960s through the 1970s. The throughput can be further improved by stacking multiple reactor tubes in a furnace to share a common induction-heating power source. This type of reactor is simpler for the automatic loading and unloading of wafers. They have been used for automatic epitaxial growth using a central control computer. The backseal of the wafers using the mass transport technique (see Section 1.8.1) is also easy to carry out. Problems associated with this type of reactor are (1) depletion of silicon and dopant source gases towards the downstream end of the reactor, (2) autodoping by impurities carried from the upstream wafers to the downstream wafers, and (3) increase in the boundary layer thickness with distance as shown in Eq. (1.3.8). Some

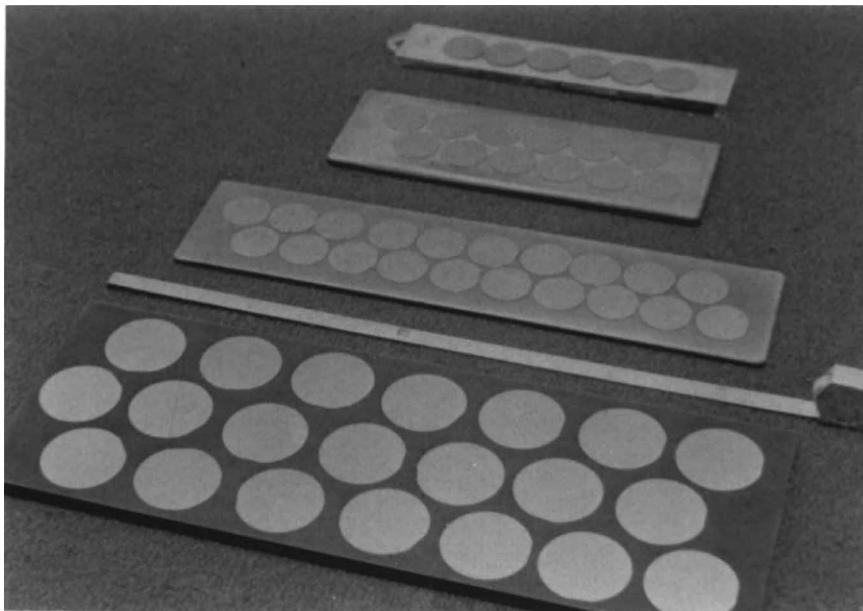


FIG. 34. Evolution of the load size in the horizontal reactors from the mid-1960s through the 1970s. [Courtesy of Motorola, Inc. Semiconductor Products Sector.]

techniques have been developed to overcome these problems. They include tilting of the susceptor, use of high gas flow velocity, and increase in temperature toward the downstream end. However, consistent uniform thickness and dopant concentration are still very difficult to obtain. Therefore, such reactor is gradually being replaced by either the pancake or barrel reactor.

Wafers in the barrel-type reactors are placed nearly vertically against the susceptors. The vertical configuration of wafers is unique for this type of reactor. This greatly reduces the chance of surface contamination resulting from falling particles in the reactor. The load size of the barrel reactors is also comparable with pancake reactors. The barrel reactor uses an inverted bell jar and the gas mixture is injected horizontally by two nozzles at the top of the bell jar. A quartz baffle is used to spread the gas mixture before it flows downward. The wafers placed at the upper position of the barrel are exposed to the up stream of the gas mixture, while those at the bottom of the barrel are exposed to the down stream of the gas mixture. Nevertheless, uniformity of epitaxial wafers, located from top to bottom of the susceptor, almost equivalent to those of vertical reactors has been obtained. This is achieved by (1) adjustment of the direction and flow of gas from two jets, (2) rotation of the barrel, and (3) use of a trapezoidal barrel. Another unique feature is the use of radiant heating and the capability of very low-pressure growth (<80 torr). This reduces the problems of autodoping and slip induced by thermal stress. Therefore, this type of reactor has been very popular since the late 1970s. The barrel reactors are capable of lower-pressure growth (50–60 torr) than can be achieved in rf-heated pancake reactors (100 torr). The lower-pressure capability results from the radiant heating which produces no plasma (arcing). The low pressure capability is a key ingredient for a lower-temperature growth. Studies have shown that device-quality epitaxial silicon can be grown with growth temperatures as low as 850–900°C by using a pressure of 30–50 torr (Nagao *et al.*, 1985; Borland and Drowley, 1985). Table 5 compares the capabilities of the three types of current reactors that currently are available commercially.

One drawback in the radiant heated barrel reactors is the high operational cost. The lamps used for heating require frequent replacement. A new model appeared in 1986 that uses rf heating, which is lower in maintenance cost. The rf coils are encircled horizontally around the upright quartz bell jar, which is cooled by a water jacket. A thin layer of gold film is coated on the outer surface of the bell jar to serve as a heat reflector. The loadsize of the reactor is also increased to 21 150mm-diameter wafers.

There are two more types of epitaxial reactors that have been developed in the laboratories and are not available commercially. One is the contin-

TABLE 5. Capabilities of Three Types of Reactors^a

Type	Reactor load size				Quoted % uniformity ^b		Reduced-pressure capability	Heat source
	75 mm	100 mm	125 mm	150 mm	Thickness	Resistivity		
Horizontal	21	10	6	—	± 10	± 20	No	rf
Pancake I	21	10	7	5	± 4	± 5	Yes	rf
Pancake II	39	22	12	8	± 4	± 5	Yes	rf
							(100–150 torr)	
Barrel A	30	14	12	—	± 5	± 6	No	IR
Barrel B	40	24	12	—	± 4.5	± 6	Yes	IR
							(50–100 torr)	

^aFrom Liaw *et al.* (1984b).^bUniformities quoted here are guaranteed by reactor vendors.

uous chemical vapor-phase reactor (Bean *et al.*, 1985). In this system the wafers pass through the chemical deposition chamber horizontally. The surface to be deposited faces down so that the particulate problem is totally eliminated. Each wafer is enclosed in an individual cell during the etching and deposition. The autodoping problem is also greatly reduced. The other developed by Ban (1978) is called the RCA Rotary Disc Reactor. This reactor consists of a set of parallel, closely spaced susceptor disks which rotate on a common axis in a horizontal reactor tube. Gas mixture is delivered to each space between the susceptors by nozzles. Deposition uniformity of ± 5% has been obtained. Advantages of this reactor include (1) high packing density and (2) low power and gas consumptions. However, no information is available regarding the epitaxial layer quality, such as autodoping and surface defects. The mechanical complexity of this reactor perhaps limits its acceptance for production applications.

Evolution of epitaxial reactors will continue to emphasize the improvement of throughput and quality of epitaxial films. The newer pancake and barrel reactors use dual growth chambers. The reactor's operation efficiency is increased because during the wafer loading/unloading with one chamber the growth can proceed with another chamber. The new type of reactors with increased load size to over 100 25mm-diameter wafers/run are expected to be available by 1986–1987. Automation of the process will also be developed. A current epitaxial reactor is equipped with a microprocessor and automatic growth procedures can be programmed. The robotic handling of wafers for loading and unloading has been incorporated into new rf heated barrel reactors. Computer-controlled automatic epitaxial production has been developed in-house by Motorola. A central computer is used to monitor and control a group of reactors. The recipes or

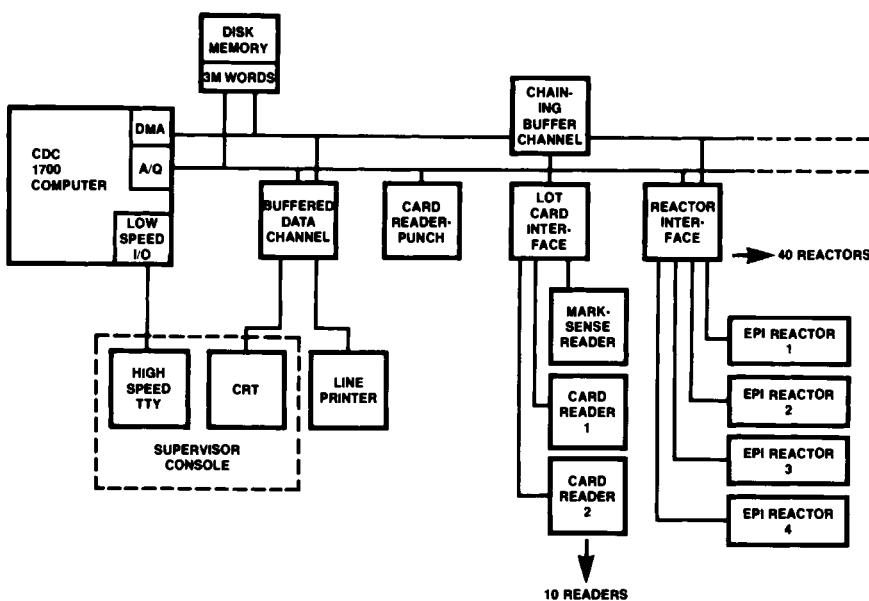


FIG. 35. Schematic layout of the computer-controlled epitaxial reactor system. [Courtesy of Motorola, Inc. Semiconductor Products Sector.]

the process parameters that the reactors will execute are entered through the central computer. Problems such as incorrect temperature or gas flow for the process are monitored and alarms are issued by printed messages on a high-speed teletype. Safety considerations such as hydrogen leaks, cooling system failures, or exhaust failures are also continuously monitored. Failures in any of these systems initiate an emergency shutdown. The computer-controlled system also provides real-time production statistics on an hourly, daily, or monthly basis. This information is used to monitor yields, productivity, and to schedule wafer production. A schematic layout of the computer controlled epitaxial reactor system is shown in Fig. 35. Figure 36 shows the layout of a conceptual automated mini epitaxial factory. [Williams and van Pul, 1978].

1.7.2 Susceptor Design

Temperature uniformity of the wafers (within wafer and from wafer to wafer) is a very important parameter for epitaxial growth. A high radial temperature gradient in the wafers can induce slip during epitaxial growth. It can also affect the thickness and dopant uniformity. The configuration of the heating sources is a major factor affecting the temperature uniformity of wafers. The optimum configuration of the heating source is generally

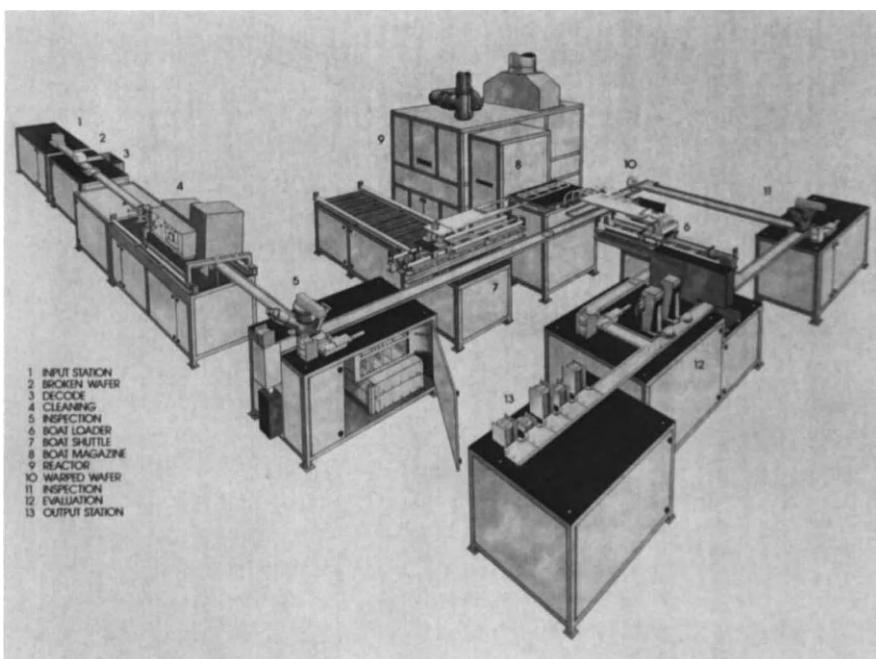


FIG. 36. Conceptual layout of the automated mini epitaxial factory. 1. Input station; 2. broken wafer; 3. decode; 4. cleaning; 5. inspection; 6. boat loader; 7. boat shuttle; 8. boat magazine; 9. reactor; 10. warped wafer; 11. inspection; 12. evaluation; 13. output station. [Courtesy of Motorola, Inc. Semiconductor Products Sector.]

provided by the reactor vendor. We will focus on the discussion of another factor, susceptor configuration.

The susceptors used in most of the epitaxial reactors are made of graphite. In an rf heated reactor the graphite susceptor is directly coupled to the rf energy. The eddy current induced in the graphite susceptor generates heat which in turn heats the wafers from their backside. The front surface of the wafers faces open space and dissipates heat away from the wafers. Thus, the backside of the wafer is hotter than the front side. In a radiantly heated reactor the front surface of the wafers is heated directly by lamps. Thus, the front surface is warmer than the back surface. The temperature difference between front and back surfaces will bow the wafers. Figure 37 sketches the directions of bow in a wafer with respect to the susceptor in the rf and radiantly heated reactors. The radius of curvature R of the bow is directly proportional to the axial temperature gradient (Bloem and Goemans, 1972):

$$1/R = \alpha(dT/dz) \quad (1.7.1)$$

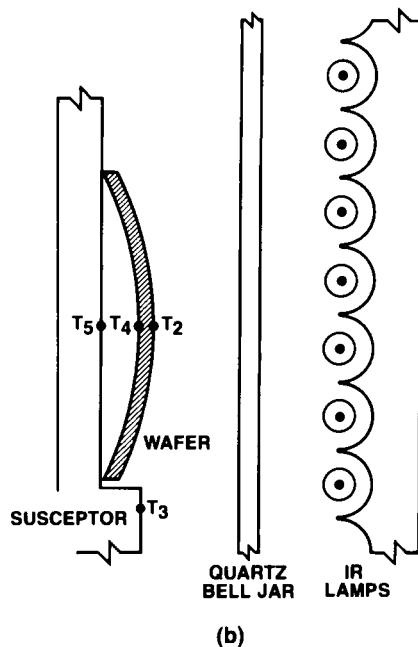
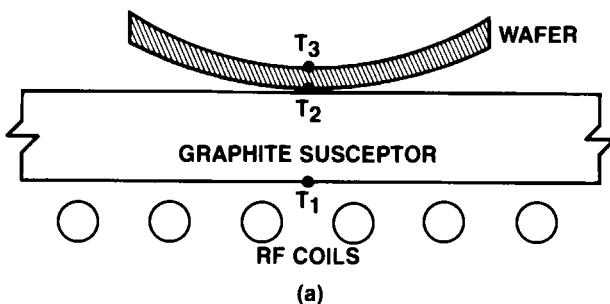


FIG. 37. Directions of bow in a wafer with respect to the susceptor in the (a) rf and (b) radiantly heated reactors.

where α is the expansion coefficient of silicon and dT/dz the axial temperature gradient. Bowing results in poor contact between the wafer and the susceptor. This will increase the radial temperature difference particularly in the rf heated reactor as shown in Fig. 37a. In this case the periphery of the wafer will become cooler than the center region. The radial temperature difference in the wafer will induce an additional curvature to the wafer.

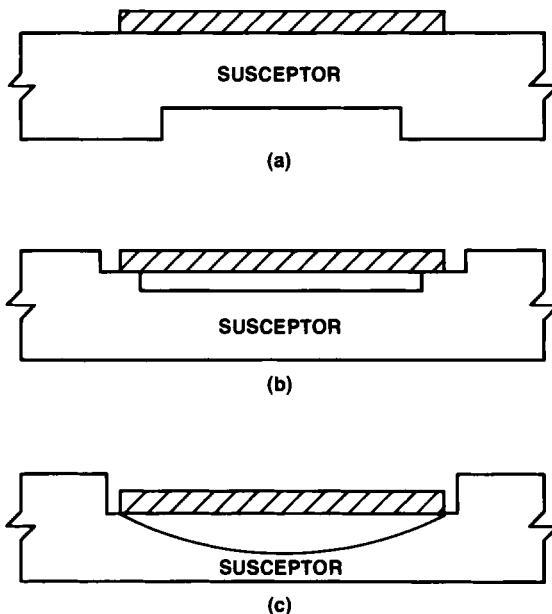


FIG. 38. Types of shaped susceptors for improvement of radial temperature uniformity in the wafer: (a) cut-off pocket, (b) double recess, and (c) saucer dish.

The wafer curvature induced by the radial temperature gradient is proportional to the square root of the temperature difference between the rim and center (Bloem and Goemans, 1972). One method to reduce the radial temperature gradient of the wafer is by shaping the susceptor (Goemans and van Ruyven, 1975; Robinson *et al.*, 1982). Figure 38 shows the shapes of the susceptors which have been suggested for use in an induction heated reactor. Figure 38a shows a pocket underneath the wafer. The diameter of the pocket is slightly smaller than the wafer. Figure 38b shows a double recesses in the front side of the susceptor. Figure 38c shows a curved recess. Shaped susceptors as shown in Figs. 38b and c prevent the wafer from losing contact at the wafer edge. The susceptor shown in Fig. 38c is perhaps the most commonly used. The exact depth of the recess is generally determined empirically. A zero radial temperature gradient can be obtained by optimizing the depth of the recess.

The temperature across the width of the susceptor used in a horizontal reactor is also not uniform, and additional shaping of the susceptor is needed. Again the empirical approach is most oftenly used. Curve A shown in Fig. 39a is a plot of the temperature along the width of the susceptor. The rapid fall-off of temperature at both sides of the width is the result of a greater heat loss in these areas. Figures 39b and c show the

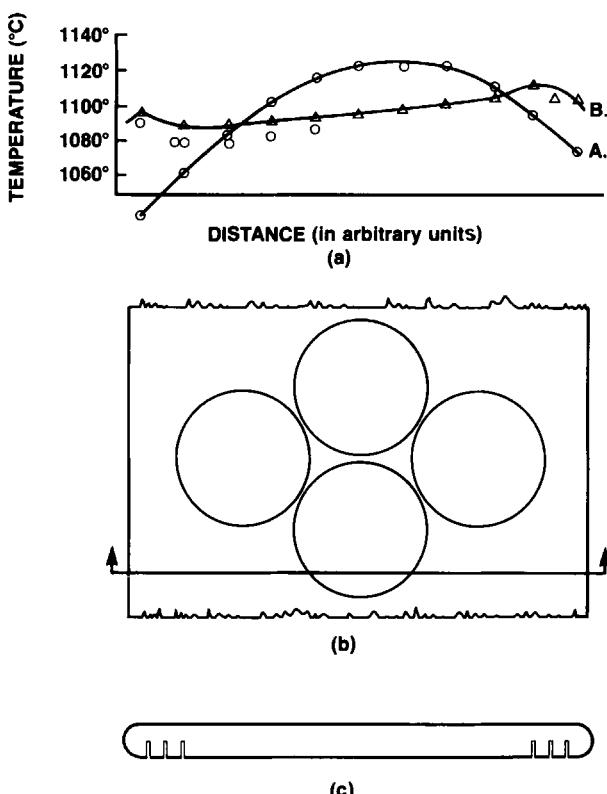


FIG. 39. (a) Plot of temperature profiles along the width for the grooved (curve A) and nongrooved (curve B) susceptors. (b) top and (c) cross-sectional views of the susceptor. [Courtesy of Motorola Inc., Semiconductor Products Sector.]

top and cross-sectional views of the shaped susceptor in which grooves have been cut at both edges along the length. The grooved regions of the susceptor have a higher resistance than nongrooved regions and, therefore, increase the temperature at susceptor edges. Curve B in Fig. 39a plots the temperature across the width of the susceptor after the grooves have been made.

The vertical temperature gradient shown in Eq. (1.7.1) is expected to increase with the susceptor temperature. This results from the fact that the heat loss from the front surface by radiation is proportional to the fourth power of temperature. Indeed our experience has been that slip is very difficult to avoid when the susceptor temperature is greater than 1250°C. Shaping of the susceptor geometry alone may not be the most effective way to flatten the radial temperature gradient and reduce the

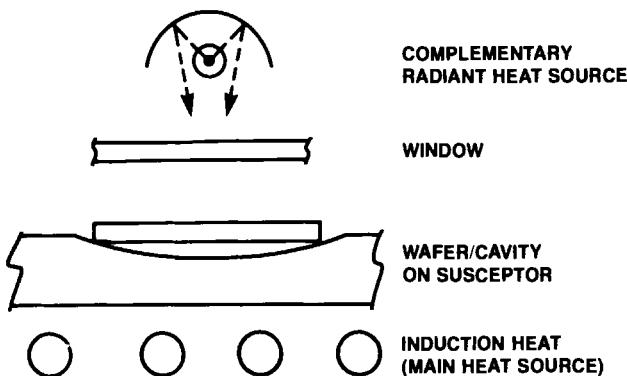


FIG. 40. Arrangement of the two heating sources with respect to the wafer surfaces. Slip-free wafers have been produced from this type of reactor. [From McDiarmid *et al.* (1984). Reprinted by permission of The Electrochemical Society, Inc. This figure was originally presented at Spring 1984 Meeting of The Electrochemical Society, Inc. held in Cincinnati, Ohio.]

vertical temperature gradient. Complementary heating using a radiant heat source has been suggested to add to the rf heat source. Figure 40 shows the arrangement of the two heating sources with respect to the wafer surfaces. Slip-free wafers have been produced from this type of reactor (McDiarmid *et al.*, 1984). A less effective but relatively simple method is the use of a heat reflector. The reactor enclosure such as the bell jar itself can serve as a heat reflector. This is accomplished by either using an opaque quartz bell jar with its inner wall polished to a mirror finish or a transparent quartz bell jar with its outer wall coated with a gold film.

1.8 GROWTH PROCESS

1.8.1 Substrate Preparation

Surface quality of the substrate is a factor determining the quality of epitaxial growth. Current wafer preparation techniques which include slicing, etching, polishing, and cleaning are so advanced that flat ($\pm 2\text{-}\mu\text{m}$), mirror-finished clean substrates are commercially available. The polished wafers are well packaged to protect the surfaces from contamination during shipping and storage. The as-received substrates can be directly used for the epitaxial growth. However, it is a good practice to reclean the substrates when they are stored in an unsealed package and have been exposed to open air. It is also necessary to remove the native oxide when no prebake cycle will be used in the epitaxial growth.

The methods of wafer cleaning vary widely in the industry. Each institution has its own recipe or proprietary solutions which satisfy their specific needs. One of the most well-known cleaning procedure is the so-called RCA clean (Kern, 1970). The procedure includes the cleaning with a hydrogen peroxide solution at high pH (i.e., H₂O₂:H₂O:NH₄OH) followed by a peroxide solution at low pH (i.e., H₂O₂:H₂O:HCl). The first step removes organic contaminants, and the second step removes metal contaminants. Other oxidizing solutions commonly used are H₂SO₄-H₂O₂ and HNO₃-H₂SO₄. Dyer and Padovani (1973) have found that using a HNO₃-H₂SO₄ solution is superior to those based on peroxide solution. Cleaning by the oxidizing solution is performed at an elevated temperature (80–100°C) for 5–10 min. The oxidizing solution not only removes surface contaminants but also forms a thin layer of SiO₂ film on the surfaces. The SiO₂ film causes the silicon surfaces to be hydrophilic which prevents the formation of spotty residues during subsequent cleaning with aqueous solutions. The thickness of the SiO₂ film is approximately 20 Å (Atkinson *et al.*, 1985). This thin SiO₂ film is removed during the prebake cycle (with H₂ or HCl) in the epitaxial reactor.

The presence of an SiO₂ film on the substrate is undesirable if the epitaxial growth does not include the high-temperature prebake cycle. Atkinson *et al.* (1985) have developed a cleaning procedure which removes the native oxide just prior to loading the wafers into the epitaxial reactor. Their procedures include the following steps: (1) H₂SO₄:H₂O (2:1) at 120°C for 5 min followed by a 5-min rinse in deionized H₂O, (2) H₂O:H₂O₂:HCl (5:2:1) at 85°C for 10 min followed by a 5-min rinse and a 30-min rinse in recirculating water, (3) a dip in H₂O:HF (19:1) at 20°C and rinse for 4 min and spin dry. Note that the first two steps use oxidizing cleaning solutions and the last step removes the native oxide. The time between the last step of cleaning and epitaxial growth should be as short as possible to prevent regrowth of the native oxide.

Heavily doped ($>10^{18}$ atoms/cm³ of As, B, or P) substrates require a backseal to prevent doping impurities from outgassing during the epitaxial growth. The substrates backsealed with a layer of SiO₂, Si₃N₄, or polycrystalline Si are available from the substrate suppliers. The growth of the thermal oxide, or the CVD deposition of Si₃N₄, or polycrystalline silicon is applied to the substrates prior to the final wafer polishing. However, updoped silicon can also be deposited to the backside using an epitaxial reactor. The horizontal epitaxial reactors are most suitable for this purpose. This is called the mass transport technique. The undoped polycrystalline silicon is first deposited on the entire surface of the flat graphite susceptor. Silicon substrates are then loaded on the susceptor. Silicon wafers are heated up in the reactor in the absence of the silicon-containing

gas. For the mass transport to occur the wafers must be cooler than the susceptor and HCl must be present. Therefore, the *in-situ* backseal and HCl etch cycles can be carried out simultaneously immediately followed by the epitaxial growth. This technique is not applicable for the wafers placed in a radiantly heated reactor. In this case the backseal and epitaxial growth must be carried out separately in two steps. The first step is to deposit undoped silicon on the backside. The second run is to grow the epitaxial layer on the front side after the reactor has been cooled down to turn over the wafers.

1.8.2 Gettering

Epitaxial quality can be improved by applying a gettering technique to the substrate. The gettering can be classified as extrinsic or intrinsic. Extrinsic gettering includes the creation of damage or stress on the back-side of wafers. The damage can be introduced mechanically such as by sand blasting or by ion implantation of argon. The stress can be introduced by the deposition of a thin material such as Si₃N₄ or polycrystalline silicon. Extrinsic gettering has also been applied to the front surface of the substrate. One technique is to grow Ge–Si strain layers at the interface (Salih *et al.*, 1985). Each strain layer is alternated with a pure silicon layer, and misfit dislocations are created at the interface between the strain and silicon layers. The misfit dislocations serve as sinks for impurities. Intrinsic gettering results from the precipitation of oxygen in the bulk region of wafers. The oxygen precipitation creates dislocations or other crystalline defects. The stress associated with these defects can act as sinks for the gettering of impurities or defects from the front surface.

The extrinsic gettering by backside damage is not very effective since the damage will be annealed out by subsequent heat treatments. For example, Tsuya *et al.* (1980) have found that backside damage gettering can only reduce the density of the oxidation-induced saucer pits in the epitaxial layers from 10⁶ to 10⁴–10⁵/cm². Stress-induced gettering is more effective. Tanno *et al.* (1981) have found that the saucer-pit (or microdefect) density in the epitaxial layer can be reduced to 10²–10³/cm² by deposition of a >250 Å thick Si₃N₄ layer. However, Si₃N₄ deposited on the backside creates bow in wafers. The degree of bow is directly proportional to the Si₃N₄ thickness. When Si₃N₄ is deposited on a mechanically damaged surface, its thickness can be reduced to 200 Å and still has the gettering effectiveness equivalent to a 2500-Å film. Chen and Silvestri (1981) have found that the backside damages introduced by argon implantation reduces the oxidation-induced stacking fault density from 100–1000/cm² to less than 10/cm². However, it did not reduce the epitaxial stacking

fault density. The epitaxial stacking faults can be eliminated only by the combination of the backside and frontside gettering. The frontside gettering in this case uses arsenic implantation which also served to form the subcollector of transistors.

Intrinsic gettering of crystallographic defects in the epitaxial layer by oxygen precipitation in the substrate was reported by Katz and Hill (1978). They have found that the densities of saucer pits and surface stacking faults in the epitaxial silicon were reduced when the substrate contained a high oxygen concentration. The gettering is the result of oxygen precipitation which exceeds the solubility limit at the wafer processing temperature. Oxygen precipitation in the silicon is greatest in the temperature range of 750–850°C. Tsuya *et al.* (1980) have found that a preanneal at 820°C for 16 h is very effective for forcing oxygen precipitation in the substrate. Less oxygen is precipitated when the substrate is preannealed at 1150°C for 16 h.

The oxygen concentration in the substrate has a strong effect on the minority carrier lifetimes in the epitaxial layer (Tsui *et al.*, 1984; Liaw *et al.*, 1984b). Figure 41 shows the plot of lifetime in the epitaxial layer versus

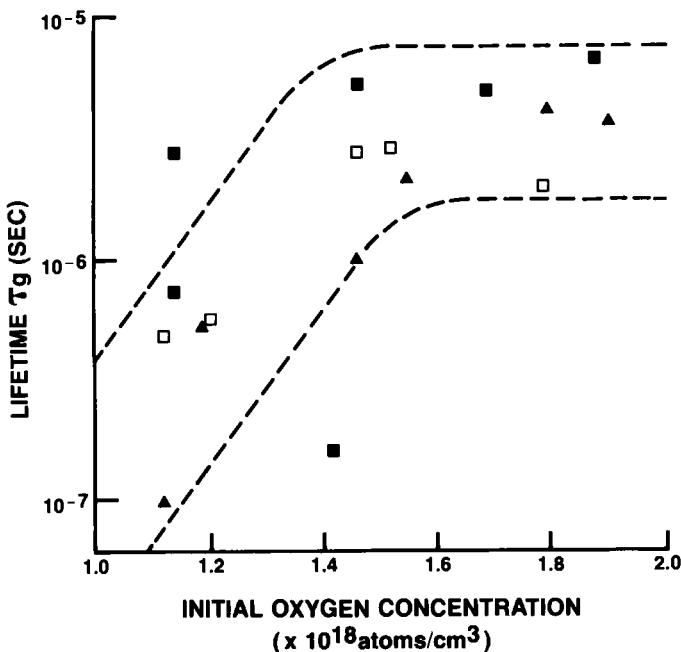


FIG. 41. Plot of lifetime in the epitaxial layer versus initial oxygen concentration in the substrate for wafers which have had different heat treatments for intrinsic gettering: ■, low-high anneal; □, high-low anneal; ▲, no anneal. [From Liaw *et al.* (1984b). Published with permission of Solid State Technology, published by Technical Publishing, a Company of Dun and Bradstreet.]

initial oxygen concentration in the substrate for wafers which have had different heat treatments for intrinsic gettering. The lifetime is seen to increase with oxygen concentration in the substrate, reaching a plateau at the concentration of 1.5×10^{18} atoms/cm³. This plot also shows that preannealing has little affect on lifetime. This is probably due to the fact that the wafers used for this lifetime measurement had an additional heat treatment to simulate the bipolar process heat cycles which include a high-temperature buried layer diffusion. This high-temperature (1200°C) heat treatment may well have dissolved the oxygen precipitation induced by preannealing.

The additional beneficial effect of oxygen precipitation in the substrate is hardening of the crystal lattice (Hu, 1977). This improves the mechanical strength of the wafer and minimizes the chances of slip formation during the epitaxial growth and subsequent high-temperature processing. The adverse effect of oxygen precipitation is the formation of warpage in the wafers, although the warpage is also dependent on the rate of temperature ramping used in the high-temperature processing. The optimum oxygen concentration, therefore, should be determined according to the individual wafer processing needs.

The dopant in the heavily doped substrates can affect the defects in the epitaxial layer. Secco d'Aragona *et al.* (1985) have found that the epitaxial layer deposited on an Sb-doped substrate always contains a higher density of microdefects (saucer pits and oxidation-induced stacking faults). Figure 42 compares the defects in epitaxial layers deposited on Sb-doped and B-doped substrates. Tsuya *et al.* (1985) have found that antimony retards the oxygen incorporation into the silicon during crystal pulling. This suggests that the effectiveness of intrinsic gettering in the Sb-doped substrate is reduced. The epitaxial defect density can be reduced only by a prolonged low-temperature preanneal (Secco d'Aragona *et al.*, 1985).

1.8.3 *In-Situ* HCl Etching and H₂ Prebake

The prebake cycle is an essential part of the epitaxial growth process for obtaining a high-quality film. The prebake can be conducted either in a pure H₂ ambient or with a few percent of HCl in H₂. Prebake in a pure H₂ ambient is used to remove the native oxide which impairs the growth of single-crystal films. It is generally carried out at a temperature between 1150 and 1200°C for about 10 min. The pressure of the prebake has a profound effect on both the prebake temperature and epitaxial growth temperature. Nagao *et al.* (1985) have found that single crystal silicon can be grown from SiH₂Cl₂ at as low as 930°C under atmospheric pressure if the prebake is carried out at a reduced pressure (40 torr). Borland and Drowley (1985) have found that the prebake temperature can be reduced

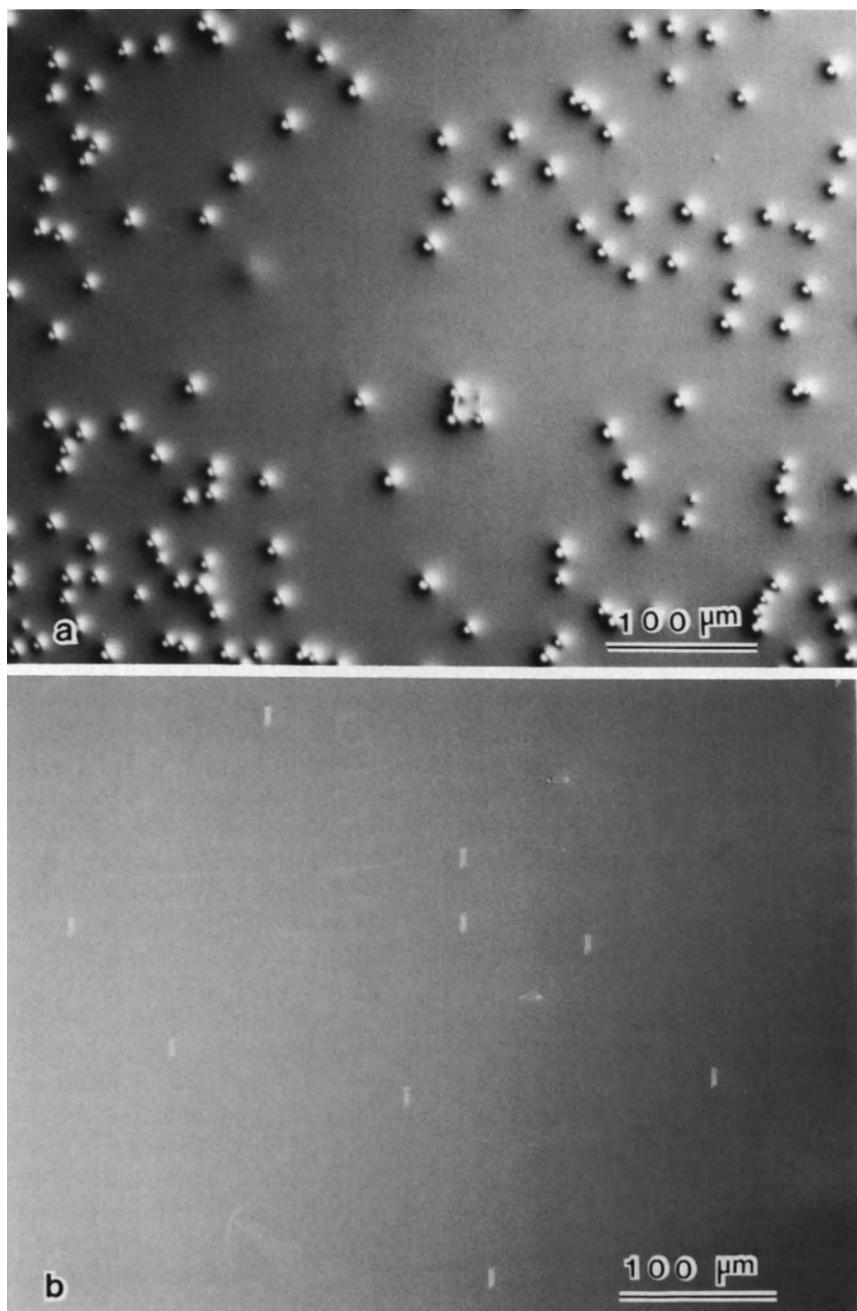


FIG. 42. Comparison of defects in the epitaxial layers deposited on (a) Sb-doped and (b) B-doped substrates. [Courtesy of F. Secco d'Aragona, Motorola, Inc.]

to 950°C and the growth temperature to 825°C when the prebake and growth are carried out at 20 torr.

The prebake cycle using 1–2% HCl in H₂ leads to the nonpreferential etching of silicon. Very clean and damage-free surfaces can be produced if 0.1–0.5 μm of the upper surface has been removed. This *in-situ* etching has been very effective for the elimination of epitaxial stacking faults and spikes. The temperature used for *in-situ* etching is also critical. Chang (1983) has found that etching at 1150°C consistently produced a lower stacking fault density than that at 1050°C independent of the silicon source gas used. However, HCl *in-situ* etching can produce several adverse results. HCl can preferentially remove a dopant over silicon, and the dopant concentration at the substrate surface is reduced. When the substrate contains a buried layer, the sheet resistance of the buried layer is increased which is undesirable for device performance. Parts of the dopant removed by HCl can reincorporate into the epitaxial layer and introduce autodoping. HCl can be a carrier gas for metallic impurities that contaminate the epitaxial layers. The source of metallic impurities can be the HCl container or the piping used in the epitaxial reactor. Scott *et al.* (1984) have found that iron and chromium concentrations in the epitaxial layers are increased by the increase in HCl concentration used during *in-situ* etching.

The choice of H₂ or HCl for prebake requires consideration of many factors: HCl etching is preferred if surface defects in the substrate are a problem; H₂ prebake is preferred when autodoping is a problem. Chang (1983) has found that the choice of H₂ or HCl for prebake also depends on the silicon source gas: HCl etching is superior to the H₂ prebake when SiH₄ is used, H₂ prebake is superior to HCl etching when a chlorosilane is used.

1.8.4 Optimization of Epitaxial Growth Parameters

The epitaxial growth parameters that can be varied include (1) silicon source gas, (2) growth temperature, (3) growth pressure, (4) growth rate, and (5) gas flow rate. The optimization of these parameters is dictated by the specific requirements of the epitaxial films. In general, epitaxial films require a low defect density, a minimum impurity outdiffusion and autodoping, a small pattern shift, and no pattern distortion. However, it is unlikely that a single optimum growth condition exists to meet all these requirements. This is due to the fact that the adjustment of one growth parameter improves certain requirements but worsens the others. The following section reviews the effect of these growth parameters on the epitaxial properties. The optimization of the growth parameters is a matter of trade-off among the requirements of the epitaxial properties.

Silicon source gases that are commonly used for epitaxial growth are

silane, dichlorosilane, trichlorosilane, and silicon tetrachloride. The chlorine content in a silicon source gas determines the temperature range in which epitaxial growth can take place. The growth temperature increases with Cl content in the silicon source gas. When the control of impurity outdiffusion from the substrate is the main concern, the epitaxial growth should be carried out at a temperature as low as possible. Then the choice of silicon source gas should be in this order: SiH_4 , SiH_2Cl_2 , SiHCl_3 , SiCl_4 . If pattern shift is the most critical item of concern, the choice of a silicon source gas should be in the reverse order. The pattern distortion on (100) wafers is also affected by the silicon source gas. The growth from silane gives minimum distortion. No significant difference in pattern distortion has been found whether the films are grown from dichlorosilane or from silicon tetrachloride.

For a given silicon source gas, the growth temperature can also affect epitaxial defects, impurity outdiffusion, and pattern shift. Low growth temperatures can result in a higher defect density. However, the impurity outdiffusion is reduced. The pattern distortion is also decreased with decrease in growth temperature. The effect of the temperature on the pattern shift and pattern distortion occurs only for (111) wafers but not for (100) wafers.

The growth temperature determines whether the epitaxial growth is a diffusion-controlled or a reaction-controlled process. The epitaxial growth at a high temperature is in the regime of diffusion-controlled process. This growth process results in rough and nonplanar morphologies in the selective epitaxial growth islands. The epitaxial growth at a low temperature is in the regime of a reaction-controlled process. This process leads to smooth and planar surfaces.

Growth pressure is a very critical parameter. Low-pressure epitaxial growth has been found to have several advantages over growth at atmospheric pressure (Ogirima *et al.*, 1977; Herring, 1979b; Nagao *et al.*, 1985). They are (1) the reduction of autodoping for the *n*-type dopants, (2) reduction of pattern shift, (3) improvement of epitaxial thickness uniformity, and (4) decrease in the growth temperature. The native oxide on the silicon substrates can be effectively removed at low pressures through the reaction with the deposited silicon and formation of a volatile silicon monoxide. This makes epitaxial growth at a low temperature possible under reduced pressure. However, the reduced pressure growth provides the following adverse effects. The pattern distortion in (100) wafers seems to increase with the decrease in growth pressure, and the autodoping of the *p*-type dopant (boron) is increased with the reduction of growth pressure (Graef *et al.*, 1985).

The growth rate can also affect impurity redistribution, pattern shift,

and pattern distortion. The autodoping of impurities is decreased when the growth rate is increased from 0.1 to 0.5 $\mu\text{m}/\text{min}$. The outdiffusion of impurities is also decreased with the increase in growth rate. Pattern distortion is decreased by the increase in growth rate, whereas pattern shift is increased by the increase in growth rate.

The flow rate of the gas mixtures can affect the thickness uniformity. Poor uniformity may arise from a low flow rate. The effect of the flow rate on other properties has not been reported.

1.8.5 Energy-Enhanced Deposition

Silicon epitaxial growth by the CVD technique is typically carried out at a temperature ranging from 1000 to 1200°C. Growth at this high temperature introduces significant dopant redistribution and causes the abrupt profiles at the epitaxy–substrate interface to become graded. In order to minimize this dopant redistribution, the epitaxial temperature needs to be lowered. A lower deposition temperature can be achieved by using a second energy to supplement the thermal energy for the chemical reactions. The most commonly used supplementary energies are plasma and photon energies. Silicon epitaxial films have been successfully grown by either the plasma-enhanced or photo-enhanced CVD techniques at temperatures as low as 680°C. Although further development is needed for film quality improvement, these techniques seem very attractive for future applications to shallow junction devices.

In plasma-enhanced CVD, glow discharge of the gases can be generated either by a radio frequency electric field or by a dc excitation (Reif, 1984). The growth chamber must be at a reduced pressure of 1 torr or less in order to maintain a glow discharge. Silane is typically used as a silicon source gas for the purpose of low-temperature growth. The procedures for the epitaxial growth by plasma-enhanced CVD also include two steps: (1) prebake and (2) film growth. When the prebake cycle is under the influence of a gas plasma it does not need to be carried out at an elevated temperature higher than that used for growth. Townsend and Uddin (1973) used a hydrogen plasma while Reif (1984) used an argon plasma for the precleaning of the substrate. Townsend and Uddin (1973) have been able to grow epitaxial silicon at 800°C. They found that silicon layers grown by the plasma-enhanced CVD process contain less epitaxial stacking faults than those grown without the plasma. This is interpreted as the result of a better substrate precleaning under the hydrogen plasma during the prebake cycle. Reif (1984) has been able to grow epitaxial silicon at as low as 775°C with specular surfaces. The plasma precleaning of the substrate is considered as the most critical step. It has been found that epitaxial films

with comparable quality can be grown at this temperature without plasma in the reactor as long as the substrates have been precleaned by a gas plasma. An alternate prebake cycle has been used by Suzuki and Itoh (1983). They introduced a small amount of GeH₄ into SiH₄ prior to the onset of the silicon growth. Thus, a Ge-Si alloy film is deposited as a buffer layer at the epitaxy-substrate interface. The existence of this buffer layer has improved the film quality of the silicon layer which is grown subsequent to the buffer layer. This result is attributed to the removal of the native oxide from the substrate by the reaction of Ge + SiO₂ to form volatile GeO.

The plasma-enhanced CVD process can provide two more advantages in addition to the effective surface cleaning during the prebake cycle. They are (1) an enhancement of the growth rate and (2) a decrease in the sensitivity of the growth rate to temperature variation. Townsend and Uddin (1973) have suggested that an enhancement of the growth rate will occur by the presence of plasma in the reactor even though their experimental results were not able to verify it. They had difficulty in measuring their thin epitaxial layers which had thicknesses in the submicron range. Reif (1984) has been able to verify a growth rate enhancement, for example, from 340 Å/min to 450 Å/min. Suzuki and Itoh (1983) have compared the temperature dependence of the growth rate with and without plasma enhancement. They have found that the growth rate is less sensitive to the temperature variation when the glow discharge is present in the reactor. This can be seen from difference in activation energy which was 0.25 eV for the plasma enhanced deposition as compared to 1.6 eV for the deposition without plasma enhancement. They have also found that the temperature dependence of the growth rate is decreased by a lowering of the silane pressure (e.g., from 1×10^{-2} torr to 3×10^{-3} torr). Similar results have also been obtained by Donahue *et al.* (1984).

In the photo-assisted epitaxial growth of silicon, ultraviolet (UV) light is commonly used as an energy source for the enhancement of chemical reactions. Frieser (1968) was the first to report the photo-assisted epitaxial growth of silicon. He used a mercury lamp as the UV light source. The wavelength of the UV lamp was 3160 Å (92 Kcal) which is approximately equivalent to the bonding energy of the Si-Cl bond (91 Kcal/mole). Si₂Cl₆ was chosen as the silicon source gas since it readily decomposes into Si, SiCl₄, and Cl₂ at temperatures as low as 450°C. He has demonstrated that oriented silicon films can be deposited at temperatures as low as 700°C as compared to the polycrystalline deposition without UV irradiation. Work by Yamazaki *et al.* (1984) has demonstrated that single-crystal epitaxial films can be deposited at as low as 630°C using Si₂H₆ as a silicon source gas. Si₂H₆ was chosen because it can be easily decomposed by irradiation

with a high-power Xe–Hg lamp. It is important to note that in both cases of photo-assisted epitaxial growth, the wafers have been preheated at an elevated temperature higher than the epitaxial growth temperature. Nevertheless, abrupt impurity profiles at the epitaxy–substrate interface were still observed.

The combined application of gas plasma and photon energies to the CVD process seems attractive for obtaining the advantages of both energy sources. A CVD deposition apparatus of this type has been built by Hargis, Jr. and Gee (1984). The plasma is generated by applying a 10-kV dc electric field across the reactor, while the photo energy is supplied by a krypton fluoride excimer laser. This apparatus can be used for the etching of insulator substrates as well as for the deposition of silicon films. They have found that single-crystal silicon films can be grown following an initial period of polycrystalline growth when the laser energy density is greater than 0.40 J/cm^2 without heating the substrate externally.

1.8.6 Selective Epitaxial Growth

Epitaxial silicon is typically grown nonselectively over the entire top surface of silicon substrates. The desire for higher device performance has called for the epitaxial silicon to be grown only on selective areas. The early work by Rai-Choudhury and Schroder (1971, 1973), Tsuchimoto *et al.* (1976), and Braun and Kosak (1978) was primarily aimed at discrete devices such as photodiode imagers, high-frequency power transistors, and low-breakdown voltage Zener diodes. No commercial IC devices have as yet used selective epitaxial films.

Recent advances in reactive ion etching technology have allowed the formation of narrow line widths in dielectric films on silicon substrates. This provides the possibility of forming closely spaced epitaxial islands isolated by the dielectric lines. Thus, the selective epitaxial growth (SEG) of silicon became a potential new alternative for IC device isolation (Hine *et al.*, 1982; Endo *et al.*, 1982; Tanno *et al.*, 1982). The development of an alternative device isolation technique is needed due to the fact that the current method, based on the local oxidation of silicon (LOCOS), exhibits an unacceptable lateral oxide encroachment when the isolation line width is reduced. In addition the SEG can potentially be used to form silicon-on-insulator (SOI) structure by lateral overgrowth on the isolating SiO_2 strips (Rathman *et al.*, 1982; Jastrzebski *et al.*, 1983a, b). However, the distance of overgrowth is limited to a very narrow width, typically less than $20 \mu\text{m}$. Selective epitaxial growth has also been used to form retrograded doping profiles for CMOS device applications.

The problem areas associated with SEG are (1) the heterogeneous

nucleation of silicon on the dielectric mask film, (2) the non-planarity across the isolated dielectric and SEG silicon interface, (3) thickness uniformity, and (4) formation of crystallographic defects at the interface. The heterogeneous nucleation rate is affected by many factors as shown in Eq. (1.4.3). This equation shows that one of the methods to suppress heterogeneous nucleation is by reducing the supersaturation. This can be easily accomplished by adding HCl into the reactor. The addition of HCl increases the Cl/H ratio in the reactor. Figure 7 shows that the solubility of silicon in the gas phase is increased by the increase of the Cl/H ratio, and thus the supersaturation is decreased. The dielectric material used for the mask is also a factor determining the heterogeneous nucleation rate. Table 4 shows that the use of SiO_2 is superior to Si_3N_4 for minimizing the heterogeneous nucleation. The nonplanarity across the mask–epitaxy interface results from the formation of facets on the silicon epitaxial islands. The thickness uniformity over the wafer surface is dependent on the variation of the surface area ratio between the mask and epitaxial islands. Ishitani *et al.* (1984) has found that the thickness uniformity of the epitaxial islands can be improved by increasing the HCl flow rate into the reactor. The interfacial defects and facets can be reduced by the alignment of epitaxial islands along the [010] direction instead of the [110] direction (Jastrzebski *et al.*, 1983b, Borland and Drowely, 1985).

1.8.7 Unique Features of CVD Epitaxial Growth

Silicon epitaxial growth by the CVD method has been playing an important role for the semiconductor industry. Many of the current sophisticated devices could not have been fabricated without the CVD epitaxial growth technology. The popularity of the CVD growth over other growth techniques can be attributed to its flexibility and more importantly to its capability for producing high-quality single-crystal films. The diversity of this method includes

- (1) The epitaxial layers can be grown from a variety of silicon-containing gases using different chemical reactions such as pyrolytic decomposition, disproportionation, or reduction of chlorosilanes. Each type of reaction occurs at a certain temperature range. Thus, a wide range of growth temperatures can be chosen. For example, when the epitaxial layers are sensitive to the impurity outdiffusion, a low-temperature growth can be chosen either by pyrolytic decomposition or by disproportionation. When the surface quality and crystal perfection in the epitaxial films are critical, growth by the reduction of a chlorosilane is used. Although the range of growth temperature is far below the melting point of silicon (1412°C), it is higher than some of other growth methods, such as molec-

ular-beam epitaxy (MBE) or liquid-phase epitaxy. However, the CVD growth temperature can be further decreased by using an energy-assisted technique, such as plasma or photo-enhanced deposition.

(2) A variety of compounds are available for either *n*-type or *p*-type doping. A doping concentration ranging from 10^{14} to 10^{18} atoms/cm³ can be obtained. This range meets most of the device application needs. Variations of doping concentration and type can also be easily made within each growth run or from one growth run to another. Thus, the epitaxial films of various properties such as varied resistivity or containing a *p-n* junction can be obtained.

(3) The growth rate can be varied from hundredths of a micrometer to a few micrometers per minute. Thus a wide range of epitaxial thicknesses, typically from submicrometers to 100 μm , can be obtained. Again, this thickness range can meet most of the device needs.

(4) *In-situ* etching or reversed growth can be easily achieved. The *in-situ* etching is a contributing factor to the production of high-surface-quality epitaxial films when the particulate contamination to the substrate surfaces was still not well controlled.

(5) Near-equilibrium growth can be obtained either by the addition of HCl into the chlorosilane or the use of disproportionation of SiI₂. Selective epitaxial growth is possible under the condition of near-equilibrium growth.

(6) It has been demonstrated that this growth technique can be scaled up to accommodate an increase in wafer size without an increase in thickness and doping non-uniformities. The crystal perfection is also not degraded by the scale-up of the batch size.

The crystallographic defects and surface morphology of silicon films grown from the CVD technique are superior to those grown by other techniques. The dislocations induced by the thermal stress have been totally eliminated by minimizing the temperature gradient in the wafers. The density of the other defects such as epitaxial stacking faults and spikes can also be reduced to less than 100/cm². Specular surface can be routinely produced. Recently it has been shown that the epitaxial surface quality is gradually approaching the best quality of silicon substrates which are free of surface defects resulting from the advances in the wafer polishing technique.

The CVD method for epitaxial growth is perhaps the most complex when it is compared to other techniques. Unlike the growth by physical deposition such as MBE, this method requires numerous test runs to reach suitable growth parameters for single-crystal growth. The complexity of this method results from the fact that (1) it generally includes multicomponent species in the chemical reactions, (2) the chemical reactions may

produce certain intermediate products, (3) the CVD growth has numerous independent variables, and (4) the deposition process includes many consecutive steps.

1.9 DEVICE APPLICATIONS

1.9.1 Discrete Devices

Several discrete devices have used epitaxial materials. Each type of device calls for specific requirements of the epitaxial parameters. The first application of epitaxial layers was in the fabrication of bipolar transistors. In this application, the epitaxial layer is p on p^+ or n on n^+ . The epitaxial layer serves as the collector of the transistor and is the determining factor for breakdown voltage of the collector-base junction (BV_{CBO}), saturation resistance, and base-collector junction capacitance characteristics. If the epitaxial layer is too thick, series resistance of the excess material contributes strongly to the collector-to-emitter voltage $V_{CE}(\text{SAT})$. It is feasible to vary the doping level in the epitaxial layer in order to perturb or change the electric field configuration in the collector.

Power devices are characterized by high switching speed, high voltage and high current ratings. High power rating needs high-purity material for reducing device failures. Power transistors can be built either directly on the substrates or on the epitaxial films. Transmutation doped float-zone substrates are typically used for this application. The use of multilayer epitaxial films can improve the device performance (Allan, 1975). The first layer is the collector of the transistor and could be an n on n^+ or p on p^+ substrate. After the thickness of the collector layer has been obtained the dopant type is changed, and a base layer is subsequently grown. The emitter is formed by diffusion into the base layer. One advantage of this technique is that the impurity profiles in both the collector and base can be arbitrarily and independently controlled. A sharp doping transition width of less than 0.2 μm at the junction is needed.

Epitaxial material requirements for power device applications have been discussed by Rai-Choudhury (1973) and Roy (1973). In general, they need to be defect-free over a large area. The epitaxial defects or contamination from the substrate can cause hot spots. Roy has developed the epitaxial procedures for producing hot-spot-free devices. The recommended procedures include a 2–3- μm etch of the substrate with SF_6 and epitaxial growth from SiHCl_3 at 1150°C. Breakdown voltages in excess of 3500 V have been achieved. Some power devices also require high minority carrier lifetime, and a lifetime greater than 100 μsec has been obtained by Rai-Choudhury (1973).

Rai-Choudhury (1973) has also used silicon epitaxial films to build

microwave diodes which can operate at frequencies between 40 and 92 GHz. The material requirements for microwave device applications include thin epitaxial layers (in the submicrometer range), precise control of epitaxial thickness, which relates to the transient time, and a heavily doped surface for good electrical contact.

Epitaxial silicon used for tuning diodes requires graded and hyperabrupt dopant profiles. The specific profile needed is dictated by the $C-V$ characteristics of the diode. In the graded region the dopant concentration N is increased with distance x following a power rule, $N = x^{(1-2m)/m}$, where m is a constant. This kind of dopant distribution is difficult to produce by the conventional growth process. Jackson and DeMassa (1977) have developed a computer controlled doping process and have been able to produce doping profiles for achieving $C = KV^{-n}$ characteristics, where K and n are constants. A doping model by Reif and Dutton (1981) enhances the capability for achieving the desired dopant profiles without extensive trial-and-error epitaxial growth runs.

Diode arrays used for the photo-imaging applications need dielectric isolation between each diode. Selective epitaxial growth was first applied by Engler *et al.* (1970) to fabricate this type of device. The challenge of this application is to prevent polycrystalline silicon nucleation on the surface of the isolation oxide. The formation of a mushroom shape on the tip of each epitaxial silicon island is also preferable.

1.9.2 Bipolar IC

The epitaxial silicon for bipolar IC applications is typically a layer of lightly doped n -type material grown on a p -type substrate which contains a buried layer. The substrate is of high resistivity which provides low capacitance and is opposite to the buried layer in conductivity type which provides $p-n$ junction isolation. The buried layer is heavily doped n -type formed by diffusion or implantation prior to the epitaxial growth. It provides a low-resistivity path to contact the collector of transistors. However, it also provides the source for impurity outdiffusion and autodoping. The regions of the buried layer are slightly depressed from the main substrate surface. An identical pattern of surface depression should be seen on the epitaxial layer if no pattern shift occurs during the epitaxial growth. However, this may not be the case. The main challenges in this type of epitaxial growth are the control of autodoping and outdiffusion from the buried layer, and the control of pattern shift in addition to reduction of epitaxial defects. The control of these parameters have been discussed in the previous sections of this chapter. The typical epitaxial material requirements for the bipolar devices are listed in Table 6 (Liaw *et al.*, 1984).

TABLE 6. Typical Epitaxial Material Requirements for Bipolar Devices

Property	Digital	Linear
Film thickness (μm)	0.75–4.0	4–20
Film thickness uniformity (%)	± 2	± 5
Resistivity (ohm cm)	0.2–5	0.2–15
Resistivity uniformity (%)	5	5
Substrate orientation	(100)	(100) or (111)
Substrate resistivity (ohm cm , B-doped)	5–30	5–25
Buried layer	As or Sb	As or Sb
Pattern shift (μm)	<0.1	0.6–1.1
Transition width (μm)	0.1–0.3	0.2–1.0

The effect of epitaxial doping distribution on bipolar circuit performance has been discussed by Srinivasan (1981). The epitaxial growth process mainly affects the doping profile in the collector, while the subsequent diffusions of dopants affect the doping profiles of the emitter and base. The devices for high-speed operations require a low capacitance in the collector and therefore the collector requires a flat doping profile. The width of the flat doping profile determines the breakdown voltage of the collector-base junction. The graded doping profile, as shown in Fig. 19, resulting from solid-state out diffusion and autodoping must be reduced for good device performance.

1.9.3 MOS Devices

Traditionally MOS devices are built directly on the silicon substrates. Recent advances in lithographic and other wafer processing techniques have reduced the feature size in silicon ICs to the micrometer or submicrometer range. The electric field of electrons is thus increased considerably under the short channel gate. The electrons arriving at the drain with a high electric field cause impact ionization and generate electron-hole pairs. The excess electrons and holes impinge into the substrate bulk region causing secondary impact ionization. The substrate charges caused by the secondary impact ionization can drift back to the active device areas. The flow of the substrate current is referred to as a substrate noise. The number of the substrate charges decreases exponentially with the decrease in minority carrier lifetime in the substrate. The use of epitaxial silicon deposited on a heavily doped substrate, which has low minority carrier lifetime, is one of the methods to reduce the substrate noise.

Scaled CMOS devices built on silicon substrates are highly susceptible to the latchup between the parasitic vertical and horizontal bipolar transistors. Such susceptibility is generally measured by the holding current.

The higher the holding current the greater is the immunity to latchup. The holding current I_h can be expressed as (Manoliu *et al.*, 1983)

$$I_h = \frac{I_{R_w}\beta_n(\beta_p + 1) + I_{R_s}\beta_p(\beta_n + 1)}{\beta_n\beta_p - 1} \quad (1.9.1)$$

where I_{R_w} is the current through the well resistance R_w , I_{R_s} the current through the substrate resistance R_s , and β_n and β_p are vertical and lateral transistor current gains. In order to increase the holding current the substrate resistance R_s and well resistance R_w need to be decreased. Again the use of an epitaxial silicon layer on a heavily doped substrate can achieve this objective.

Epitaxial material has its own drawbacks. In general, the cost of an epitaxial wafer is two to three times that of the substrate. Furthermore, the surface defect density in the epitaxial wafers tends to be higher. We have found that when the surface defects in the substrate are very low, the defect density is always increased by approximately a factor of two after the epitaxial growth. Although we have found insignificant change in the wafer flatness due to epitaxial growth, the question remains on the change in bow and warpage due to the high temperature occurring in epitaxial growth. A detailed comparison between the bulk and epitaxial wafers is listed in Table 7 which includes other parameters such as resistivity limit and oxygen content.

Critical epitaxial parameters for MOS device applications include doping concentration, dopant transition width, defect density, epitaxial thickness, and resistivity of the substrate. The doping concentration affects the depletion widths of the source and drain, which in turn determines the minimum effective channel length for a given thickness of gate oxide. The doping transition width and epitaxial thickness affect the device capacitance and need to be minimized for high-speed operation. Reduction of

TABLE 7. Comparison of Bulk CZ Silicon Wafers with Epitaxial Wafers

	Bulk CZ wafers	Epitaxial wafers
Cost (per cm ²)	A	2-3A
Surface defect density (cm ⁻²)	B	2B
Flatness (μm)	C	C
Warpage (μm)	D	2-3D
Oxygen content (ppm)	10-35	<10
Upper resistivity limit (ohm cm)	100	200
Buried layer	No	Yes
Retrograded doping	Significant lateral outdiffusion (long drive-in time)	Moderated lateral outdiffusion (implant before epi)

the epitaxial thickness also improves latchup immunity in CMOS devices. Epitaxial defects can increase the leakage current of the devices in general and of memory cells in particular. To maintain reasonable refresh rates on the memory parts, the defect density must be controlled. Decrease in the substrate resistivity can reduce the substrate currents and also contributes to latch up immunity. However, this must be traded off with increase in the impurity outdiffusion and autodoping.

In addition to conventional epitaxy, selective epitaxial silicon is also attractive for the MOS device applications. Selective epitaxy can provide the following advantages. The device isolation process via selective epitaxial growth is a relatively simple process. This process can also eliminate the bird beaks which occur in the local oxidation process. Selective epitaxial growth can also be used for the formation of shallow retrograded wells in CMOS (Sabine and Kemhadjian, 1985). This is accomplished by refilling the wells which are implanted with a buried layer. This eliminates the high-energy ion implantation which produces a large lateral outdiffusion because of the necessity for subsequent high-temperature annealing. Thus, shallow and closely spaced well structures can be achieved through the selective epitaxial growth technology.

1.10 CONCLUSIONS

Epitaxial silicon films grown by the CVD techniques have been used by the semiconductor industry for the fabrication of discrete as well as bipolar integrated circuit devices for over the past two decades. Use of epitaxial silicon wafers for high-density MOS devices has been suggested. It is foreseen that the CVD method will continue to be the predominate technique for producing epitaxial silicon wafers for the next decade and beyond.

The trends for the vapor-phase epitaxial growth of silicon by the CVD technique will continue on reactor evolution and process innovation. The future reactors will improve wafer throughput together with process automation such as robotic loading and unloading of wafers. The process innovations include development of low-temperature growth, selective epitaxial growth, energy-assisted deposition, and zero-defect growth. The thick epitaxial layer will continue to be demanded by the high-voltage power devices. However, the major thrust of the process innovation will be geared toward the growth of thin epitaxial layers with precise control of thickness and doping distribution.

A better understanding of the science in CVD will help achieve the aforementioned arts. The science includes thermodynamics, chemical

equilibrium, mass transport, nucleation, and crystal growth theories. Thermodynamics and chemical equilibrium help predict whether silicon (or dopant) can deposit from an input gas mixture. The mass transport can deduce equations for the deposition rate. Nucleation and growth theories provide guidelines for optimizing growth parameters suitable for producing better-quality epitaxial silicon films.

ACKNOWLEDGMENTS

The authors wish to express their appreciation to Dr. K. W. Hansen for his encouragement and support for the writing of this paper and his critical reading of the manuscript. We would also like to thank Dr. R. T. Tsui for his reading and suggestions for the manuscript. We are also indebted to R. Boyle and P. Deal for their input on the FTIR measurement technique. We also wish to thank Mrs. K. Quirke for her typing of this manuscript.

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2

SILICON MOLECULAR-BEAM EPITAXY

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2.1 INTRODUCTION

Silicon molecular-beam epitaxy (MBE) (Allen *et al.*, 1982; Bean, 1981a, b; Kasper and Worner, 1984) has, over the past few years, attracted a growing interest. This interest has no doubt been encouraged by the excellent results obtained in several laboratories and by a realization of the potential capabilities of this technique. In its general sense, silicon MBE refers to silicon-related MBE and includes the epitaxy of those systems that can be grown epitaxially on silicon by this technique. In this chapter, however, our focus will be on the homoepitaxial aspects, and heteroepitaxy will be mentioned only briefly, though we must emphasize that the heteroepitaxial aspects offer much potential leverage for a silicon-based technology (Ishiwara and Asano, 1985; Bean, 1985; Wang, 1984).

In silicon MBE, the growth of silicon (and silicon-related materials) epitaxially on a moderately heated silicon substrate is achieved via the physical deposition of silicon atoms, molecules or ions. The process is depicted schematically in Fig. 1. An important aspect of the method is the relatively low temperature at which the substrate is held. It is also possible to incorporate *n*- or *p*-type dopants simultaneously during growth. Once again, the dopants are transported either via atomic, molecular, or ion beams. This simultaneous incorporation of dopant during growth, combined with the relatively low temperature of growth (typically 700°C but always less than 850°C) permits the generation of stable doping profiles

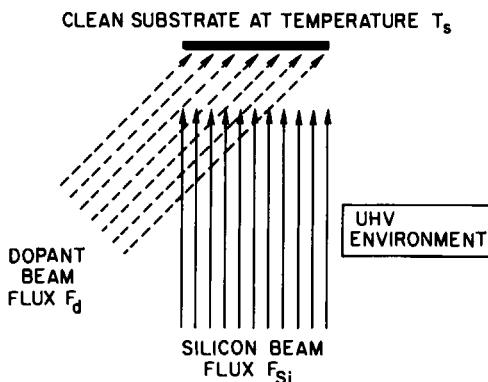


FIG. 1. Schematic representation of the MBE process.

with arbitrarily sharp transitions both in terms of the level of dopant as well as the type of dopant species.

Another distinguishing aspect of silicon MBE is the extremely low vacuum levels [typically a base pressure of 10^{-9} Pa (1 pascal = 1 newton/ $m^2 \sim 0.0075$ torr) and an operating pressure of 10^{-8} Pa] that are employed. The need for such low vacuum levels will be duly pointed out. In addition, silicon MBE requires special attention for the generation of atomically clean starting surfaces.

We shall first present an historical perspective of the development of silicon MBE then review the growth apparatus and growth procedure. The growth mechanism will then be discussed including the details of dopant incorporation using different methods. Crystal quality and the electrical properties of the grown films will then be addressed. The device applications of silicon MBE will be discussed, especially certain novel device concepts that may be realized uniquely by the silicon MBE technique. The chapter will conclude with some thoughts on the development of silicon MBE with respect to system design, process incorporation, and future scope.

2.2 HISTORICAL PERSPECTIVE

Epitaxial silicon films find widespread use in silicon technology. Primarily, high-quality films are deposited by chemical vapor deposition (CVD) (see Chapter 1). This process employs a relatively high temperature ($\sim 1050^\circ\text{C}$). Consequently, if we are attempting to grow a moderately doped film on a highly doped substrate, there is significant outdiffusion of dopant leading to a smeared doping level transition between the substrate and

epitaxial film which may occur over several thousand angstroms, especially when thicker films are to be grown. In addition, CVD techniques also suffer from the disadvantage of autodoping (Srinivasan, 1984), a complicated transport of dopant from the substrate through the vapor phase and back to the growing film, a phenomenon that tends to aggravate the doping transition smear. Efforts to reduce CVD temperatures are still at an exploratory stage (Meyerson, 1985) and use MBE-like conditions.

One simple way to reduce the substrate temperature is the vacuum evaporation of silicon onto a moderately heated silicon substrate such that epitaxial growth results (Unvala, 1962; Thomas and Francombe, 1971). The important criteria for epitaxy are that the incident atoms be sufficiently mobile on the host surface to arrange themselves in single-crystal fashion and that there be few impurities that cause these atoms to be displaced from the epitaxial positions, a condition that influences the crystal quality. Reasonable surface mobility is achieved at surface temperatures of over one-third of the melting point. The impurity level is determined by the vacuum level and the propensity of impurity atoms to stick to the surface and incorporate into the film.

Two principal techniques have been employed to evaporate silicon: (1) Kilgore and Roberts (1963) used flash evaporation from a resistively heated silicon filament and (2) other workers use evaporation from a crucible via electron bombardment (Airco Temescal, 1976). This latter technique is used almost exclusively now. In efforts made in the 1960s, growth was usually performed in pyrex vacuum chambers that were diffusion pumped. The operating pressures were of the order of 10^{-3} - 10^{-4} Pa. At these pressures, contamination of grown films is a major problem. A monolayer of ambient gas, predominantly oxygen and hydrocarbons, is incident on the sample every few seconds. If only a small fraction incorporates, it could lead to formation of crystal faults.

Queisser *et al.* (1963) and Unvala and Booker (1964) determined the effect of oxygen on the number of stacking faults. In order to reduce the impurity content of the films, the growth rate may be increased, but sufficient time needs to be given so that atoms can find their epitaxial positions before they are buried by the next incident layer. The growth rates employed in these studies were typically 1 $\mu\text{m}/\text{min}$. The mobility of the atoms is related to the surface temperature. At higher temperatures, higher growth rates may be established while at the same time reducing the sticking of impurities. Booker and Joyce (1966) found that at background pressure of 10^{-3} Pa, the best films were obtained by growing at 1200°C at a growth rate of 1.5 $\mu\text{m}/\text{min}$. It must be noted however, that no doping control is achievable at these temperatures.

With the advent in the early 1970s of ultrahigh vacuum systems, it was

possible to reduce the background pressure considerably. As a result, growth rates and temperatures could also be reduced, thus leading to greater control of the composition of grown films without compromising film quality. Figure 2 shows the impurity levels achievable at a growth rate of 1 $\mu\text{m}/\text{h}$ at different background pressures. It is seen that to achieve a background impurity concentration of less than $10^{13}/\text{cm}^3$, a background pressure of less than 10^{-10} Pa is required when the impurity sticking coefficient is 10^{-3} , which is typical at about 600°C. At higher temperatures the sticking coefficient drops, and this is shown qualitatively to lower the impurity concentration in the film. Similar effects occur when the background pressure is lowered and the growth rate is increased. It is thus clear why the advent of ultrahigh-vacuum technology in the late 1960s and its refinement in the 1970s, led to a renewed interest in silicon growth by MBE and to its present state of development.

Most of the early workers accomplished doping of the films by using doped silicon sources (Thomas and Francombe, 1971). Bennet and Parrish (1975) proposed a model to explain how the concentration of dopant in the film varied with the source concentration, growth rate, and substrate temperature. The doping level could be expressed in terms of partition and sticking coefficients and individual vapor pressures. Kuznetsov *et al.* (1971, 1979) showed that at a low growth temperature (<500°C) complete transfer of some dopants from the source was possible. They also found anomalous doping of their films using this technique due to the presence of defect centers in the incipient stages of epitaxy.

Tolomasov *et al.* (1971) used a separate antimony evaporation source to dope their silicon films. They also obtained the antimony sticking coefficient as a function of antimony flux and substrate temperature. Most of this work was done at relatively high pressures, and no attempt was made to intentionally obtain a predetermined doping profile. However, Becker and Bean (1977) and Bean (1978) used varying doping fluxes to obtain doping profiles. Ota (1977) used varying substrate temperatures with fixed and varying dopant flux to change the doping level. These probably represent the first systematic efforts to obtain doping profiles of an abrupt nature, utilizing the compositional variation capabilities afforded by MBE.

In the same time frame, other workers also looked into doped MBE films. Konig *et al.* (1979) examined the electrical quality of silicon films at different levels of antimony doping. They concluded that electrical quality deteriorates at high antimony flux values. Iyer *et al.* (1981) investigated the detailed doping mechanisms and determined that doping proceeds by incorporation of dopant atoms from an absorbed phase of dopant that accumulates on the growing surface and that the sharpness of doping profiles obtained was related to how fast the concentration of this absorbed

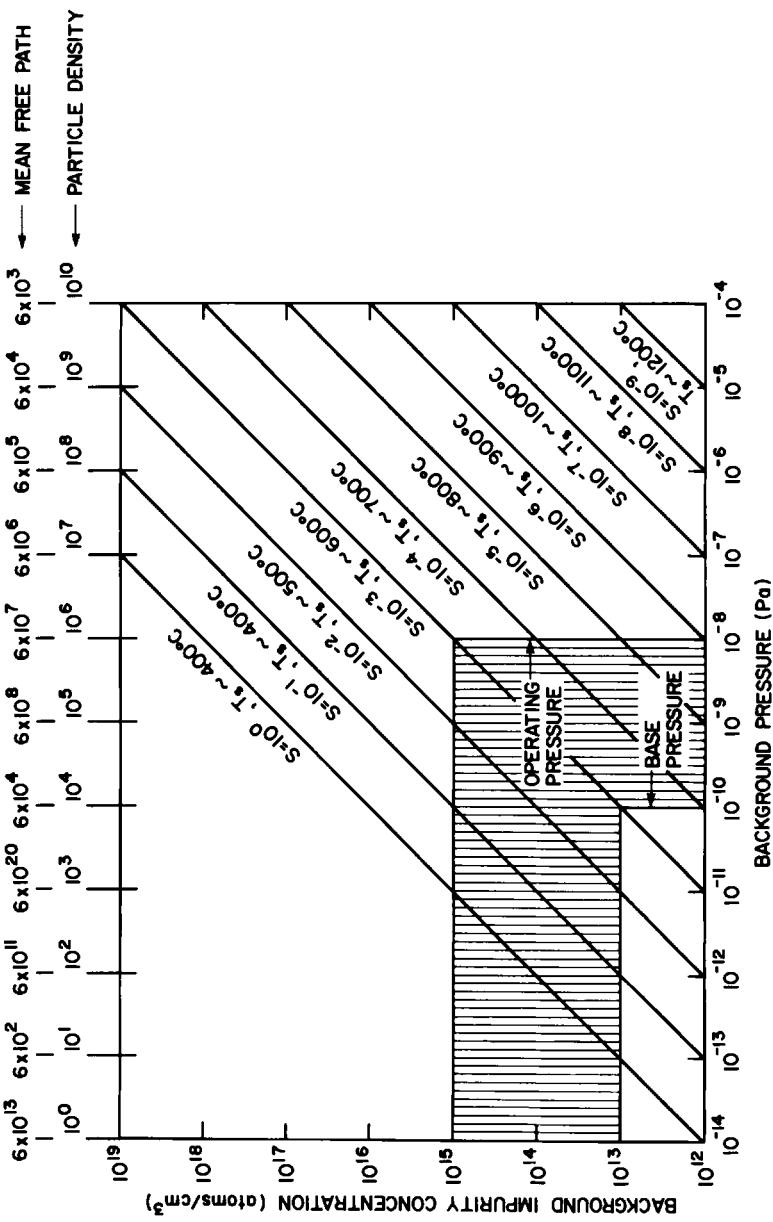


Fig. 2. Impurity levels obtained in growing films as a function of base pressure for different sticking coefficients and growth temperatures. Only active species are assumed to contribute to operating pressure. Also shown are the mean free path (cm) and the particle density. Growth rate $\sim 1 \mu\text{m/h}$. The values of S may vary with electron and ion fluxes.

layer could be changed. Similar results were observed for other dopant species as well. Hypersharp doping profiles were also demonstrated. Low-energy ions were used by Ota (1979) as the source of the dopant species. This method circumvents the complex kinetics of thermally generated dopant incorporation and is intrinsically capable of much greater control. However, bombardment of ions during growth introduces damage, a new complication in the growth process.

Silicon MBE today is an established technique and has even been used in small-scale production since 1984 for certain specialized device technologies (Kasper and Worner, 1984). Commercial silicon MBE processing systems, fully equipped with high-capacity evaporators, ion doping attachments, and a full complement of analysis and preparation facilities are commercially available. High-throughput machines (Konig *et al.*, 1982) with multiwafer capacity (Bean and Butcher, 1985) are also available.

2.3 LEVERAGE OF SILICON MOLECULAR-BEAM EPITAXY

The uniqueness of silicon MBE lies in the fact that it is a low-temperature process carried out in an extremely controlled environment. Thus, impurity concentrations are well controlled with almost atomic-level precision; unintentional impurity concentration may be controlled to values below $3 \times 10^{13}/\text{cm}^3$, and growth may proceed essentially defect free under optimal conditions. In addition, silicon MBE offers a method to integrate silicon homoepitaxy with silicon-related heteroepitaxy, thereby, increasing the leverage of silicon-based technology.

2.4 GROWTH APPARATUS

Considerable progress has been made over the years in the development of reliable, high-performance, versatile MBE equipment. While compound semiconductor MBE systems are well developed and commercially available, machines for elemental semiconductors and metals are still evolving, and several design issues still need to be resolved. Silicon MBE systems share many common characteristics with III-V machines. These include the basic ultrahigh vacuum (UHV) system, analytic tools, and Knudsen cells. However, silicon systems are, in general, much more demanding. First of all, in silicon systems the main growth axis, i.e., the axis along which the beams propagate, needs to be near vertical. This is necessary because, as we shall see, the silicon growth beam is best generated by an electron beam evaporator, and a molten pool is created by electrons impinging on a horizontal surface. That part of the silicon beam not inter-

cepted by the target substrate is deposited on chamber walls, where there is a tendency for it to build up and flake off. While the build-up does contribute to a moderate gettering action, the flaking is hazardous. The flakes contribute to source contamination and also arcing of the high-voltage parts of the system. This leads to growth disruption, beam contamination, and particle deposition on the substrate, all of which result in degraded film quality.

To some extent, this problem may be alleviated by extensive shielding and collimation of the silicon beam. In addition, preconditioning of the exposed surfaces can permit greater buildup before flaking off occurs. Ota (1983a) reports sand blasting exposed surfaces to increase adhesion, though doing so could most likely increase the total outgassing area. An alternative reported by Iyer (1981) is the use of disposable shields at crucial areas. Shields are usually made of refractory metal foil and are inserted after proper cleaning procedures. A modern modular silicon MBE system is shown schematically in Fig. 3.

Pumping packages vary from user to user with oil-free pumps being used almost exclusively. Roughing is done by sorption pumps. Ion pumps, titanium sublimation pumps, and either cryopumps or turbomolecular pumps are also used. In addition, cryoshielding also provides for pumping action. In that case, however, care must be taken to avoid electron-stimulated desorption from the cold stainless steel parts. (Reflected primary electrons and secondary electrons from the evaporators are always present.) Hence, some workers (Kasper, 1985) tend to use water-cooled shields and high-throughput turbomolecular pumps.

Another issue is related to the relatively high temperature seen by some parts of the system in silicon MBE as compared to III-V MBE. First of all, the low vapor pressure of silicon requires high source temperatures for evaporation. The use of Knudsen cells with a wide variety of crucible materials has been tried out extensively and has found limited use. This is because of the extremely corrosive nature of molten silicon and the extremely high temperature of the surrounding parts, both of which result in highly contaminated silicon beams. Graphite crucibles lead to a very high concentration of silicon carbide in the film. The use of resistively heated silicon filaments has also been explored. The problem in this case is the inability to generate a sufficiently intense beam, as well as the fact that a runaway depletion can lead to premature source filament burnout. In addition, beam control is difficult. Some of these problems have been alleviated in a multistrand silicon filament developed by Kirchner (1985), although even this source cannot be used for substantial silicon growth. As a result, electron-beam evaporation remains the most convenient and viable technique for silicon generation. Commercial electron beam evaporators, suitably modified for UHV use, exist. Source pockets holding as

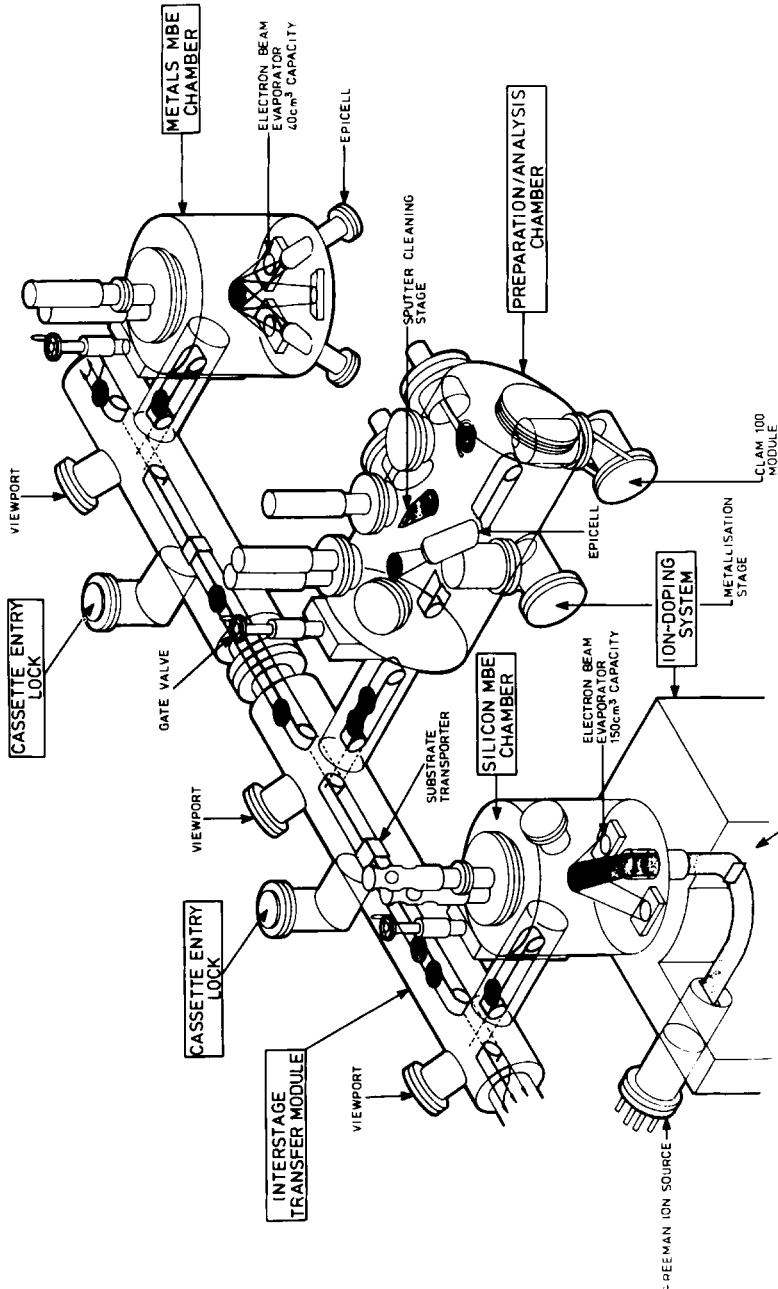


Fig. 3. Schematic of a modern silicon MBE system. It shows a vacuum-interlocked loading chamber, an analysis station with a complement of surface sensitive tools, a substrate preparation station with facilities for ion-sputter cleaning and dry chemical cleaning with optical access, and two growth chambers, which may have a variety of sources of the atomic, molecular, and ion beams employed. Several growth chambers, each dedicated to a particular material system, may be required to prevent cross contamination. [Courtesy of V. G. Semicon Ltd.]

much as 150 cm^3 of silicon charge are available. Both electrostatic and magnetically focused evaporators are used, though the latter are favored. Electron beams that bend 270° are preferred because the hot filament can be shielded from the substrate.

Due to the finite spread of the essentially monoenergetic primary electron beam, a certain small fraction impinges on the metal parts of the hearth. It is important to shield these parts with silicon shields so that metal impurity generation is minimized. A typical scheme reported by Ota (1977) is shown in Fig. 4. In addition, secondary electrons are generated. These electrons may also impinge on chamber walls and other parts. In fact, they are suspected of producing curious artifacts on growth and doping when they intercept the beam. These will be discussed later. In the interest of controllability and reproducibility these secondary electrons must also be shielded. The silicon source itself is a high-purity machined slug that fits snugly in the copper hearth, after allowing for thermal expansion.

During evaporation, the beam parameters, such as its intensity and scan, are controlled so that the molten silicon pool is well confined within the silicon slug. The silicon thus acts as its own high-purity crucible that is cooled from the outside. Because of local changes in the contact with the hearth, instabilities develop in the beam flux. Hence, feedback stabilization using a suitable flux detection scheme is mandatory. With such

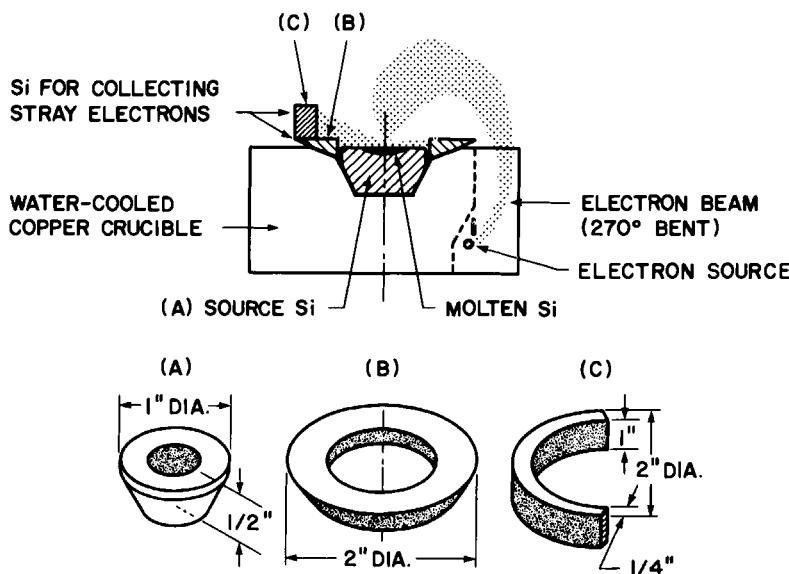


FIG. 4. Shielding of the electron-beam evaporator parts near the hearth to prevent stray electrons from impinging on metal parts and causing metal contamination of growth. [From Ota (1977).]

schemes, temporally and spatially stable beams leading to deposition rates from 0.1 to several micrometers per hour are possible.

Zalm and Beckers (1982) have reported the use of 50–60-eV Si⁺ ions, generated in a plasma chamber attached to a UHV system. Currents of several microamperes were obtained with a spot size of 5 mm. Such current densities are not high enough to sustain an appreciable growth rate, and a different approach is necessary if ion beams are to be used as the silicon source.

Beam detection is possible in a number of ways. Conventionally, quartz-crystal monitors are used. If these are suitably shielded and cooled, they do provide satisfactory beam control. Even so, they are susceptible to instability due to noise. However, after deposition of only a few microns the crystal loses linearity and needs to be changed. The changeover may be delayed by the use of two crystal heads which are exposed one at a time. Even so, changeovers need to be fairly frequent, and modern systems would require the use of a load-locked crystal monitor setup, so that the main system is not vented so frequently. Such a setup is, nevertheless, complex and expensive.

Another attractive scheme is the use of miniature ion gauges which intercept the beam. Since the ion gauges monitor beam pressure rather than flux, background pressure contributes to the overall pressure. This is circumvented by chopping the molecular beam and having lock-in detection systems. Such systems however, suffer from the disadvantage that the parts tend to get coated and lose calibration. A backup calibration scheme using a quartz-crystal monitor is recommended.

A relatively newer scheme that has been successfully employed is the use of electron-stimulated fluorescence of the species to be monitored. In this technique (Bean and Sadowski, 1982; Gogol and Cipro, 1985) a low-energy (<200-eV) electron beam is made to traverse the molecular beam. In the case of atomic species, they are excited and rapidly decay to the ground state, thus fluorescing in the UV, each species with a unique signature. The light is collected by suitable optics. The intensity is proportional to the beam density, and a direct rate is obtained. This technique may be used to feedback control the silicon source and, as demonstrated in Fig. 5, provides better stability, noise immunity, and control than a conventional quartz crystal monitor. Multiple atomic beams may be analyzed simultaneously. Its most important characteristic, however, is that it can be used over very extended periods of time corresponding to up to several hundred micrometers of evaporated material. As in the ion gauge system, periodic quartz crystal calibration is possible. Unfortunately, this technique may be used mainly with atomic species since most molecular species fluoresce in the IR and background radiation causes the signal-to-noise ratio to deteriorate to unusable levels, even when the electron beam is chopped.

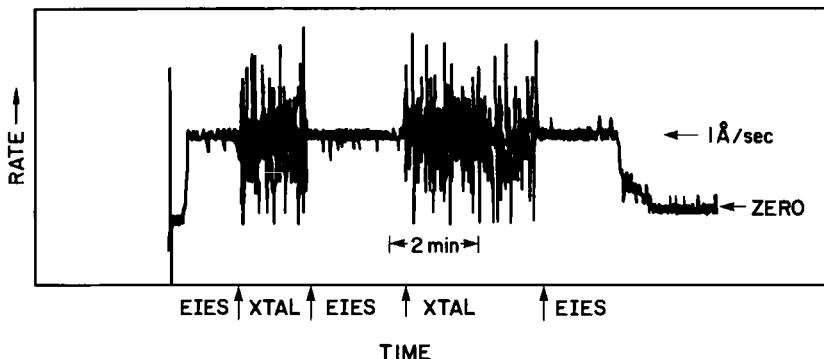


FIG. 5. Silicon rate controlled alternately by the signal from the electron impact emission sensor (EIES) and a quartz crystal sensor. The rate is read off the EIES and is much more stable when the feedback signal is supplied by the EIES. [Courtesy of C. Gogol and C. Cipro, Inficon-Leybold Heraeus.]

Shimuzu et al (1980) have proposed the use atomic absorption spectroscopy to monitor the beam intensities for the dopant beams as well. They report the use of optical radiation at 251.6 nm for silicon monitoring and 294.4 nm for gallium monitoring, using a chopped beam. The absorption of the intensity of the optical beam by the atomic beam, whose path it crosses, is monitored by phase-locked circuitry, and this is translated to beam intensity and the corresponding rate. Figure 6 shows the rise time and overshoot characteristics of such a system.

Another crucial point is the substrate holder. Silicon MBE is a cold-walled process, and heating a silicon wafer to temperatures as high as 1200°C (required in some surface cleaning recipes), without significant heating of the surroundings, presents formidable problems. Moreover, it is absolutely important to ensure a uniform temperature profile over the entire wafer, lest unequal expansion lead to thermal slip and dislocated film growth.

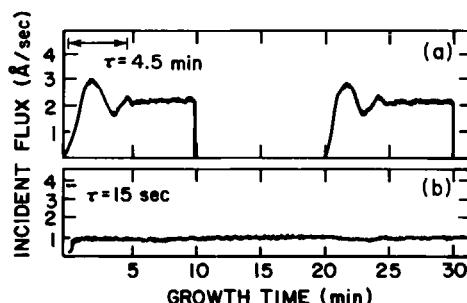


FIG. 6. Transient characteristics of an atomic absorption spectroscopy sensor for (a) gallium and (b) silicon beams (τ is the settling time). [From Shimuzu *et al.* (1980).]

Currently, radiation heating from the rear of the substrate, using a resistively heated refractory metal or graphite filament, is most widely employed. The whole heater assembly may be housed in a liquid-nitrogen-cooled container to minimize unintentional radiation to vacuum chamber parts. In order to compensate for increased edge losses, concentric filaments and filaments with resistance characteristics that increase heat generation near the periphery are used. Substrate rotation is also common both to aid temperature uniformity as well as to ensure deposition uniformity. Furthermore, to enhance doping effects by secondary implantation (to be discussed in more detail later) the substrate should be capable of being independently biased. This also permits electron bombardment of the wafer due to thermionic emission from the filaments and may be used to boost the sample temperature. Figure 7 shows an exploded view of the substrate heater used by Allen and Streit (1983) at UCLA.

Since silicon technology is a very mature technology, and silicon MBE offers potential leverage in enhancing this technology, silicon MBE must be compatible with mainstream silicon technology. Thus, large wafer sizes (6-in. systems are now offered) are essential. Perhaps, most demanding is the excruciatingly good crystal quality and film uniformity both in thickness and doping level that is needed. A very clean system is thus essential.

The dopant beams required for appropriately doping the growing film during growth, are generated by standard Knudsen effusion cells. Generally, these are quite stable and are often not feedback controlled though feedback control can only help.

Modern MBE systems also are equipped with a low-energy ion source for ion-beam doping of the film. In older systems, conventional ion implanters operated at their low-energy limits were employed. Specially designed low-energy implanters in the range of 500 to 1000 eV are available especially for MBE application. These are suitably differentially pumped, possess mass selection capability, and can produce up to 100 μA of current at the substrate. Appropriate scan mechanisms to ensure radial and polar uniformity need to be used. Figure 8 shows such an implantation system. Obtaining adequate current at these low energies with both mass selection and beam scanning is made difficult because of space charge limitations. It must be pointed out that focusing these low-energy beams to dimensions where the beam may be used to write patterns is not feasible at the present time.

It is interesting to note the evolution of silicon MBE equipment. Early systems consisted of just one chamber which combined preparation, analysis, and growth capabilities. The analytic capabilities usually included low-energy electron diffraction (LEED), Auger, and perhaps reflected high-energy electron diffraction (RHEED) to monitor surface structure,

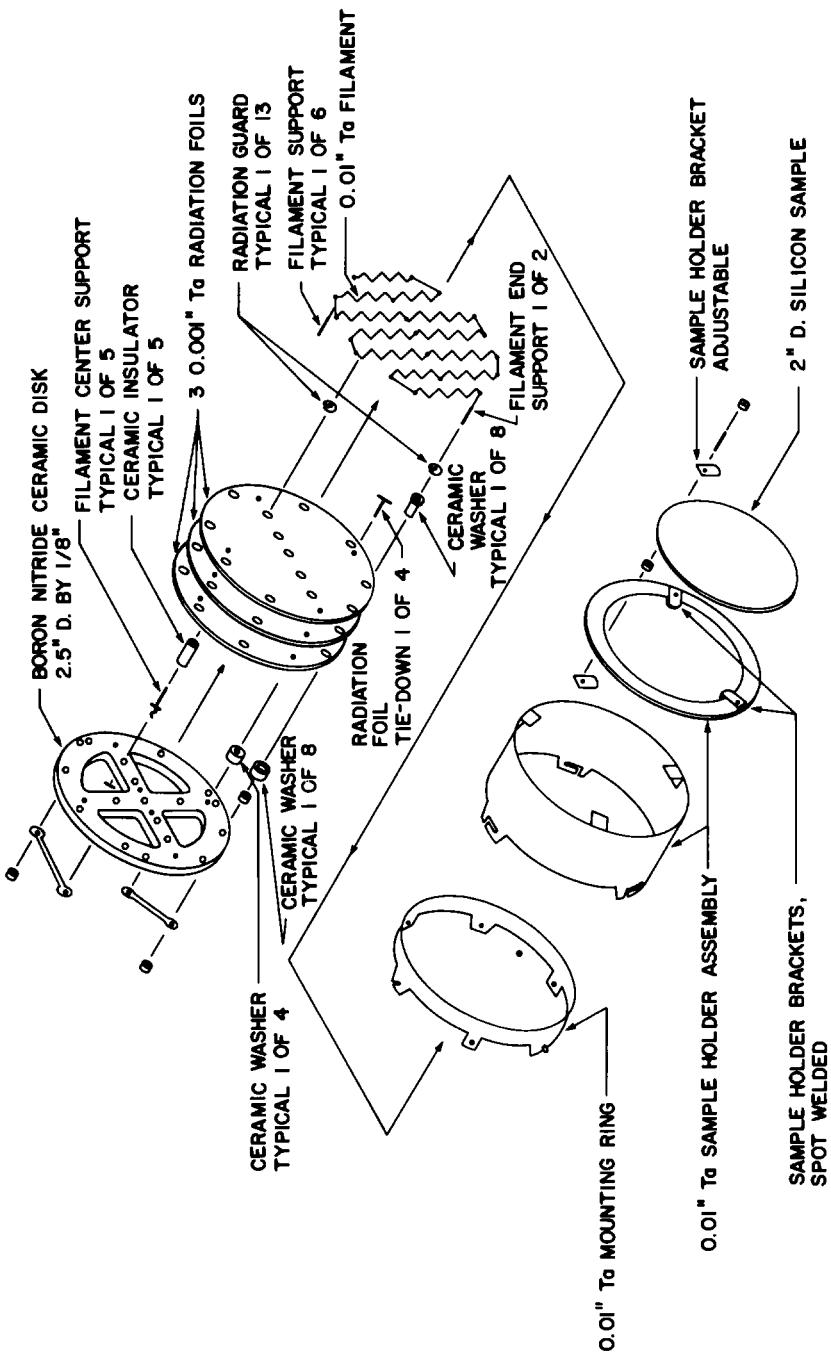


FIG. 7. Exploded view of UCLA 2-in. diameter substrate holder. Radiant heating is used. In addition, electron bombardment of the rear of the wafer is also possible. [From Allen and Streit (1985).]

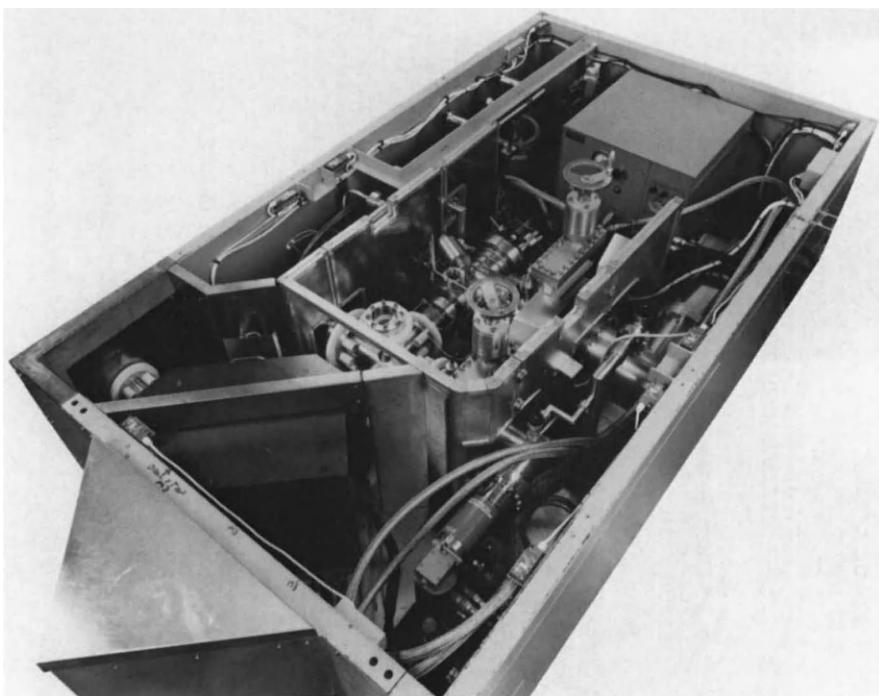


FIG. 8. Low-energy dopant ion implantation system. The Freeman ion source is fed by either solid or gaseous sources (right). The flight tube floats at 10 kV. An analysing magnet (left) performs mass selection. The beam is deflected into the growth chamber (not shown) by electrostatic mirrors. Electrostatic radial scanning is employed. [Courtesy of V. G. Semicon Ltd.]

cleanliness, and growth morphology. These are needed especially in research type systems and during the process development, as well as for process monitoring. Later systems have evolved into multichamber facilities with an efficient wafer transport mechanism between chambers. Surface analysis equipment was contained in one chamber, silicon sample preparation was conducted in another, and growth was performed in a dedicated chamber. Further development has resulted in the development of multiple growth chamber systems especially when both homoepitaxy and heteroepitaxy are contemplated. Such an arrangement is preferred in order to prevent cross contamination and ensure the best film quality. Wafer size has also been continually increasing. Currently vendors offer up to 6-in. wafer diameter systems. Substrates are usually held in ring-like frames, shown in Fig. 9, and the frames are handled during transport and mounting. Frames are made of refractory material, preferably silicon itself. Modern systems now permit cassette loading and unloading (see

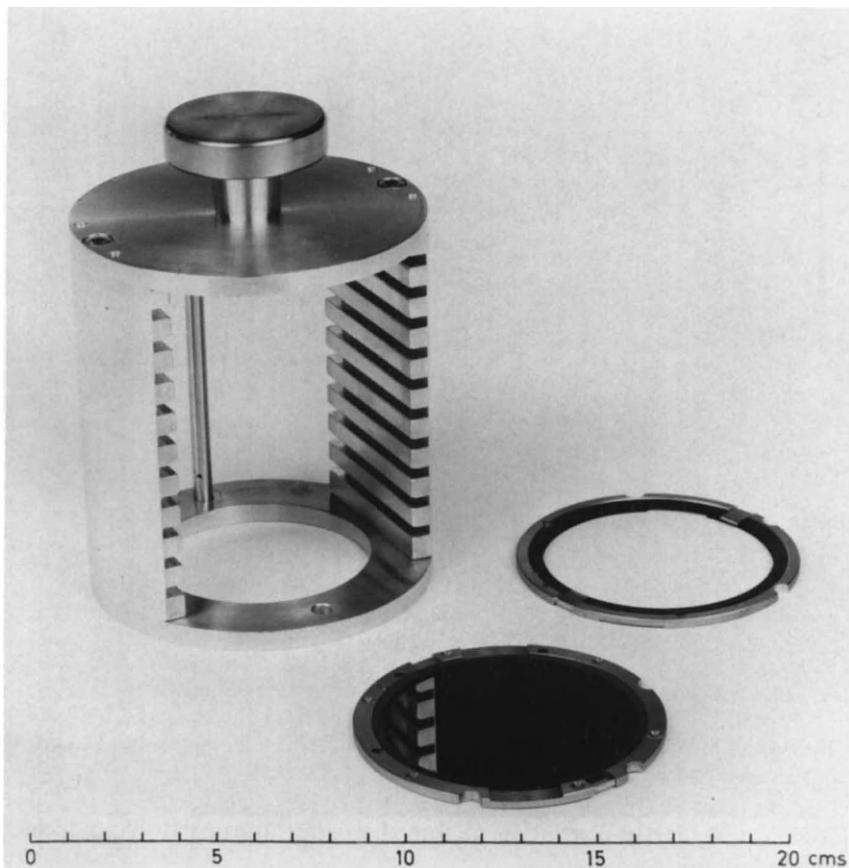


FIG. 9. Annular holder for the substrates. The ring has a lip in which the wafer is placed and is held by retainer clips. Note that the substrate is not held fixed, and thermal expansion may be accommodated. The ring material may be made of silicon or silicon-coated refractory material. A cassette which permits the loading of ten ring-mounted wafers for introduction into an MBE system is also shown. [Courtesy of V.G. Semicon Ltd.]

Fig. 9) via an interlocked loading chamber. Such an arrangement, usually with a cassette parking stage, permits greater flexibility and allows the growth and preparation process to occur simultaneously and protects the system from frequent venting. With large-capacity growth sources, we estimate a few hundred micrometers of growth before routine maintenance. Figure 10 shows a modern silicon MBE system.

Multiwafer processing systems are also being developed. Bean and Butcher (1985) have proposed such a system which utilizes the transport

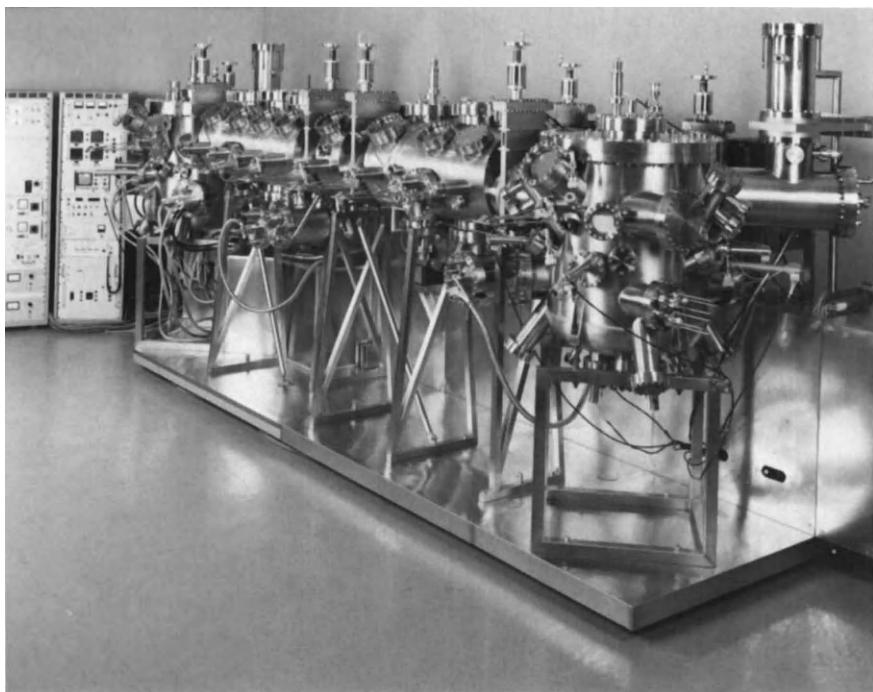


FIG. 10. A multichamber MBE processing system. This 6-in. system has two growth chambers, analytic stations and pre/post processing chambers.

of a platen. A high uniformity is claimed by using appropriately positioned multiple silicon sources.

Silicon MBE today is an established technique and has been used in small-scale production since 1984 for certain specialized device technologies to be discussed later. Commercial silicon MBE processing stations are available and these are fully equipped with high capacity evaporators, ion doping attachments, and a full complement of analysis and preparation facilities, as well as some post-processing capabilities. High-throughput machines with multiwafer capacity are also available.

2.5 SURFACE PREPARATION

MBE film growth occurs at relatively low temperatures by the rearrangement of impinging atoms into epitaxial positions. For this process to occur efficiently the silicon surface must be atomically clean. Once clean, the cleanliness of the surface is maintained by the low vacuum level in the

system. The silicon surface is generally self-passivated by a thin native oxide layer. Furthermore, exposure to air causes adsorption of hydrocarbon layers on the surface. Clearly epitaxial growth cannot proceed in the absence of an atomically clean surface, and these impurities must therefore be removed.

2.5.1 Sputter Cleaning

Farnsworth *et al.* (1958) were perhaps the first to demonstrate that atomically clean surfaces may be prepared by a combination of ion sputtering and annealing of the substrate. Bean *et al.* (1977) studied the process as a function of substrate temperature during sputtering and also varied the presputter treatment. The effect of sputtering species was studied by Hull *et al.* (1985). Generally, sputter cleaning at room temperature or below is preferred. The sputtering process physically removes the first few surface layers. In so doing, however, some lattice damage is created both in the form of displaced silicon atoms and entrapped sputtering species. When inert gas atoms such as argon are used for sputtering, the entrapped gas tends to form inclusions of several argon atoms beneath the surface. An annealing sequence is essential to get rid of the damage and expel the entrapped gas. A good sputter treatment removes about 100–150 Å from the surface layers. This is usually done by sputtering for about 5 min with an argon beam of intensity of about 1 mA/cm² at room temperature. The background pressure of argon during sputtering is about 10⁻³ Pa. The beam voltage is usually between 300 and 1000 V, and the beam is usually arranged to impinge at 45–60° off normal to increase sputter yield. The sputter damage is annealed out typically at 800–900°C for several minutes as soon as the preparation chamber pressure has recovered or better still after transfer to the growth chamber. Growth is commenced soon afterward.

The advantages of sputter cleaning lie in its relative insensitivity to the nature of the surface contaminant and consequently to the exact recipe of the wet chemical preparation of the substrate. Being a physical process it has a wide process window. The disadvantage lies in the residual damage caused by the sputter beam, including roughening of the surface, shown in Fig. 11, incorporation of voids at the interface, and sputtering of impurities onto the surface. Nevertheless, it continues to have wide acceptance, and material with good minority carrier lifetime has been grown by this method. It has also been shown that using heavier inert gas elements to increase sputter yield also leads to an increase in the level of residual damage when the energy is not lowered. Yamada *et al.* (1980) showed that gas inclusion is reduced when a lighter species such as neon is used,

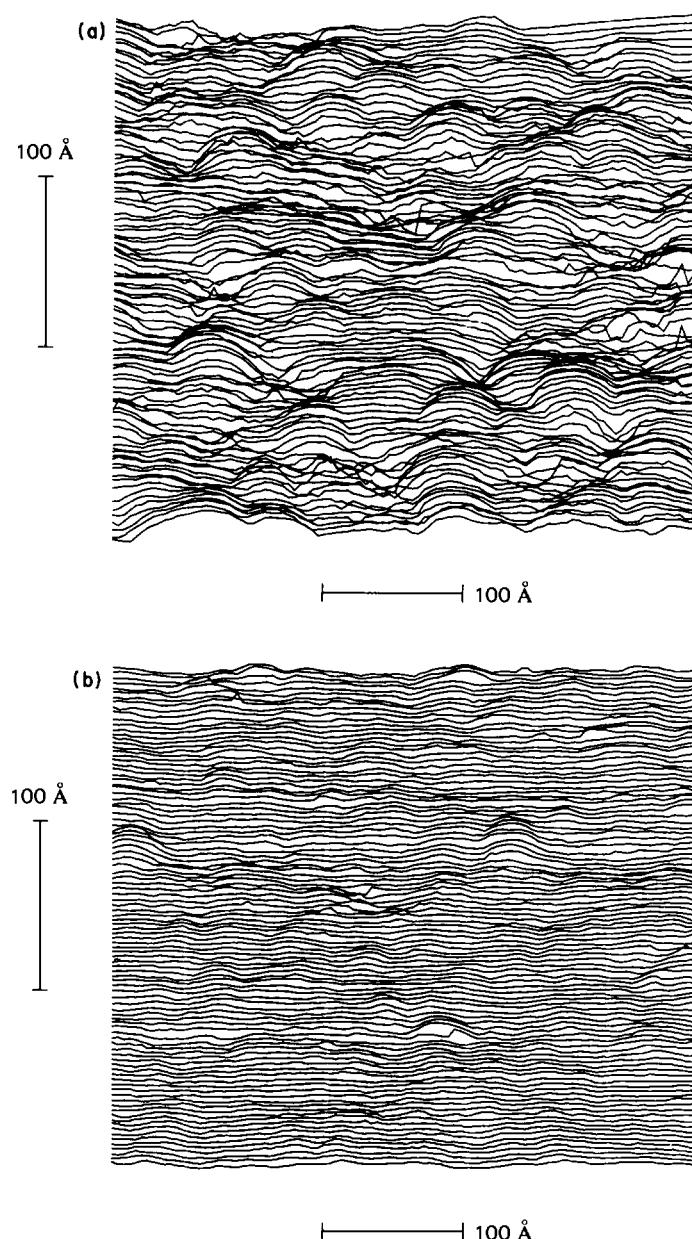


FIG. 11. (a) Scanning tunneling micrograph of a Si (100) surface after exposure to argon ion bombardment at 700 V. The roughened surface topography is clearly seen. (b) An unbombarded control is also shown for comparison. [From Feenstra and Oehrlein (1985).]

because of its higher mobility, and when the incident energy of the ions is reduced. The use of higher temperatures during sputtering has been shown to increase the level of argon retention and slow down removal of residual damage (Bean *et al.*, 1977).

2.5.2 Thermal Methods

Ever since the demonstration that atomically clean surfaces could be generated by thermal treatment of silicon surfaces at high temperature ($\sim 1250^{\circ}\text{C}$) by Allen *et al.* (1959), there has been tremendous interest in refining the technique. The thermal cleaning process consists of briefly (several seconds) elevating the sample temperature to about 1250°C . At this temperature the surface oxides are reduced by the underlying silicon to give a volatile silicon monoxide. It was originally thought that silicon from the substrate diffused through the thin oxide, reacted at the surface and formed the volatile product. Work by Tromp *et al.* (1985) indicates that, for thermally grown oxides, defects mediate its removal. Pinholes may form at these sites. Surface diffusion of silicon along the sides of the pinholes causes further erosion of the oxide. It is possible therefore to get rid of all the surface oxide. However surface roughening can also occur, as silicon is depleted from the pinholes.

The adsorbed carbon compounds are another matter, however. During the ramp up of the substrate, the hydrocarbons decompose and carbon reacts with the silicon to form silicon carbide, which may form in its crystalline form $\beta\text{-SiC}$. This form of carbon is quite stable and difficult to get rid of. There is some indication that it diffuses into the bulk of the silicon and is not present on the surface after prolonged heating. Thermal cleaning of the surface suffers from several disadvantages. It does not adequately account for carbon removal from the surface. The high-temperature treatment may lead to thermal faceting of the silicon surface as well as segregation to the surface of certain impurities. From an MBE point of view the high temperature used negates the objective of low-temperature processing. Another practical issue is the inability to uniformly heat the larger circular silicon wafers in common use today to such high temperatures. It is difficult to clean the surface uniformly and prevent the thermal slip that results from the temperature gradients present across the silicon substrate when these high temperatures are employed.

There have been, over the years, efforts to reduce the temperature at which cleaning may be achieved by a combination of chemical pretreatment prior to sample loading and an appropriate lower-temperature *in-situ* heat cycle to yield a clean surface. The basic philosophy in most of these techniques is to obtain a surface that is passivated by a low-temperature

sublimable oxide. Ishizaka *et al.* (1980) showed that repeated oxidation in hot nitric acid and oxide stripping followed by a final oxide growth in an HCl:H₂O₂ solution results in the elimination of the absorbed hydrocarbons and passivation of the surface by a thin oxide that resists further chemisorption of carbonaceous impurities. Furthermore, this oxide sublimes at less than 850°C. This technique is now quite popular and is used extensively. Others use standard RCA (Kern and Puotinen, 1970) cleaning procedures or variations of that followed by *in-situ* thermal desorption at temperatures of about 850°C to achieve similar results.

Another variation is the use of ozone in the precleaning stage to oxidize the surface (Tatsumi *et al.*, 1985). The extreme oxidizing capability of ozone ensures the oxidation of surface carbon into volatile products and the simultaneous growth of a final passivating oxide. It is, of course, more attractive to perform the ozone treatment *in situ*. This may be done by exposure to oxygen and UV light of wavelength 184.9 nm, which is absorbed by oxygen and converts it to ozone. Tabe (1984) has shown that such dry treatment, even if not done in the same growth chamber so that the sample is exposed to air during transfer, results in superior film quality.

2.5.3 Reactive Beams

The use of reactive beams to clean the silicon surface has also been proposed. Wright and Kroemer (1980) proposed the use of a gallium beam to clean the silicon surface by reduction of the surface oxide to form a volatile gallium oxide, Ga₂O.

In this technique a total of a few hundred monolayers of gallium needs to be evaporated over a period between 15 and 30 min at temperatures above 800°C. At these temperatures the gallium residence time is quite short, and at typical fluxes, steady-state coverages of a fraction of a monolayer are expected. We have observed a beneficial side effect of this treatment. The silicon surface tends to assume greater atomic-level smoothness. This was deduced by the disappearance of transmission spots using RHEED on a purposely roughened surface. This is believed to be due to liquid-phase transport of silicon and redeposition to yield planar surfaces. One disadvantage of using gallium, however, is the possibility of substrate doping by solid-state diffusion especially when long times are involved. This doping is estimated to extend a few tens of angstroms into the surface. These long times are essential for the method to work because of the clustering phenomenon exhibited by gallium.

An alternative technique is to use a silicon beam to remove the surface oxide. The etch rate is exponentially dependent on temperature. As is to be expected, the method is effective only above 800°C. The technique has

been applied by Hirofumi *et al.* (1985). The problem in this technique as implied by Kugimiya *et al.* (1985) is the narrow window of permitted silicon flux where cleaning occurs as opposed to deposition of silicon. If the flux is too low no significant cleaning action occurs. If it is too high deposition may overtake reaction with SiO₂, thus resulting in a defective film. It also, therefore, depends on the thickness of the substrate oxide.

2.5.4 Optical Cleaning

Pulsed-laser irradiation has also been used to generate atomically clean silicon surfaces in extremely short periods of time. A ruby laser (Zehner *et al.*, 1980) was employed. Gorodetsky *et al.* (1985) have shown that the radiation is converted to heat at all fluxes and the resulting cleaning is a thermal process. In fact, surface melting has been observed. This would imply that the reduction of carbon on the surface that is observed may be due to indiffusion.

2.5.5 Verification of Clean Surfaces

One of the concerns is verification that, in fact, an atomically clean surface has been generated. This includes both the surface structure as well as the nature and extent of impurities on the surface. Surface structure is conveniently studied using LEED (Clarke, 1985) and RHEED (Ichikawa and Ino, 1980). These give information about the long-range order at the surface. RHEED to some extent is also sensitive to surface morphology and traces of SiC crystallites on the surface. A sophisticated analysis of the spatial fine structure of the diffracted beams (Gronwald and Henzler, 1982) can also yield information about the step densities on the surface. Surface-sensitive chemical identification techniques such as X-ray photoelectron spectroscopy (XPS) (Carlson, 1975) and Auger electron spectroscopy can identify the impurities on the surface and their chemical state. Unfortunately, these detection techniques while important to test gross cleanliness of the surface are woefully inadequate to ascertain sufficiency of cleaning methods for growth of MBE films of higher quality. For example, most of these techniques are sensitive to about 10⁻⁴ of a monolayer.

Assertions that clean surfaces are obtained on the basis of Auger detectability imply that there could be up to 10¹² impurity atoms/cm² on the surface. If only a small fraction of these contribute to crystal defects such as dislocations and stacking faults in the growth film, the resulting defect density would be incredibly high. In fact, Sugiura and Yamaguchi (1980)

demonstrated a correlation of stacking fault density with preheat temperature and time indicating that desorption of SiO dominates the stacking fault generation process. McFee *et al.* (1983) show a more direct correlation of dislocation density with carbon impurities at the interface, perhaps due to formation of silicon carbide particles. While cleaning recipes are elaborate, evidence indicates that cleaning methods such as the RCA clean followed by *in-situ* native oxide desorption are effective in producing surfaces that are clean enough to allow for the growth of defect-free, device-quality Si MBE films, as long as we use high-grade chemicals and a clean environment and minimize the time interval between cleaning and loading.

2.6 GROWTH

Once an atomically clean silicon surface is generated, growth should be commenced as soon as possible. Even at very low base pressures ($<10^{-7}$ Pa) some adsorption of impurities can occur, as shown in Fig. 12. Practical problems exist in maintaining the low pressure during growth. Typically, turning on the electron-beam evaporators for silicon causes a surge of pressure to the 10^{-6} Pa regime (mostly hydrogen and CO) due to source and filament outgassing. It is important that the wafer not be exposed to this contamination. This is conveniently done by closing off the main substrate shutter.

Care should also be taken to prevent contamination of the source silicon pellet. This is done by ensuring a good mechanical fit of the silicon slug in

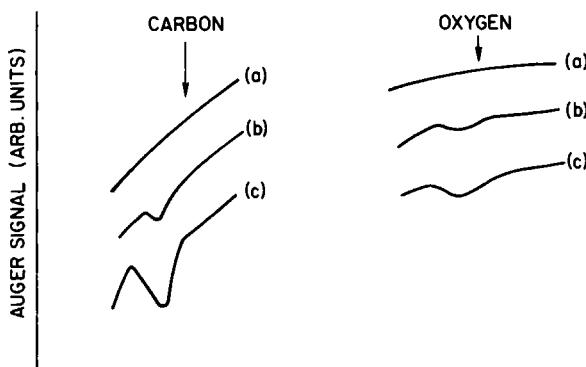


FIG. 12. Recontamination of a clean silicon surface due to exposure after cleaning. The Auger signals of oxygen and carbon are seen to increase. (a) Cleaned at 900°C for 2 min, (b) exposed for 10 min at $\sim 10^{-7}$ Pa, and (c) exposed for 26 min at $\sim 10^{-7}$ Pa. [From Allen (1985).]

the *e*-gun evaporator hearth, and maintaining electron-beam power levels and sweep conditions such that the molten pool is in no danger of reaching the edge of the hearth. Growth rates are controllable from 0.2 Å/sec ($\sim 0.1 \mu\text{m}/\text{h}$) to 30 Å/sec ($\sim 10 \mu\text{m}/\text{h}$). At the higher growth rates there is danger of silicon "spitting"—a sudden burst of silicon from the source due to thermal instabilities and gas pockets. This may also occur if silicon flakes cross the electron-beam path or fall into the hearth. This phenomenon may result in deposition of silicon particles and should be avoided by reducing the growth rate, improving the heat sinking of the silicon source via the hearth, and, of course, using silicon slugs devoid of gas pockets.

2.6.1 Models for Silicon Growth

Silicon MBE is conducted under high supersaturation. Supersaturation is defined by

$$\sigma = (P - P_0)/P_0 \quad (2.6.1)$$

where P is the equivalent pressure of the arriving beam and P_0 is the equilibrium pressure at substrate temperature. A slight degree of supersaturation ($\sigma \geq 1$) is required if crystal growth (as opposed to evaporation) is to take place.

However, in conventional growth techniques high supersaturation is avoided. Too high an arrival rate may not permit the epitaxial rearrangement of the impinging surface atoms. At high supersaturation, therefore, it is possible to have random nucleation of silicon atoms and, consequently, a three-dimensional growth mode. This growth mode is not preferred as it leads to twinning, dislocations, and other defects.

It is very preferable, therefore, for growth to occur in what is called the layered growth mode. As explained by Burton *et al.* (1951), growth in this two-dimensional growth mode occurs by the propagation of steps along the surface. As depicted in Fig. 13 the atomically clean silicon surface consists of several steps. The source of steps may be already existing ledges on more open high-indexed surfaces, dislocations, or the edges of the wafer. Typically, silicon substrates are cut slightly off axis, and thus high-index planes are often exposed. It is easy to see that if the wafer is

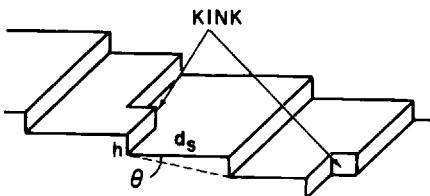


FIG. 13. Steps on a silicon surface. The misorientation of the substrate from the principal plane is shown. Steps arise predominantly by misorientation. A representative kink site is also shown. The density of kinks along a step depends on orientation and temperature.

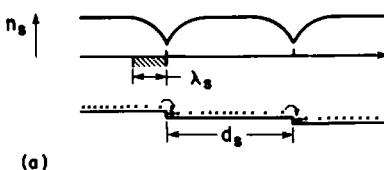
misoriented by a small angle θ from an idealized flat surface, a series of steps would be generated with spacing d_s between them given by

$$d_s = h/\theta \quad (2.6.2)$$

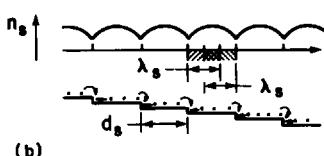
where h is the step height, usually one monolayer ($\sim 3 \text{ \AA}$) if the misorientation is small. Thus, for a misorientation of 0.2° ($\theta = 0.0036 \text{ rad}$) we have a step density of about $10^5/\text{cm}$ or a step every few hundred angstroms. In practice, misorientation or declination of production-quality wafers is anywhere between 5° and 1° decreasing for larger-diameter wafers. The step itself is not smooth but may have kinks in it as depicted in Fig. 13.

Incident silicon atoms are first adsorbed on the surface. Once captured in the surface potential well of the silicon surface they perform oscillations both perpendicular and parallel to the silicon surface. The perpendicular vibrations which lead to desorption are small at MBE growth temperatures. For example, the desorption energy for silicon from silicon, E_{dsi} is about 2.4 eV/atom assuming it to be half the heat of formation (Kubashevski and Alcock, 1979). Assuming a vibration frequency v_{Si} of about 10^{13} Hz the residence time of silicon on the surface even at 950°C is greater than a millisecond. As we shall show presently the silicon atom is incorporated in times much shorter than this.

The kink sites on the steps are perfect sinks for silicon atoms and the silicon adatoms diffuse toward these ledges, and in steady state a concentration profile is set up on the terrace area for the adatoms. If the kink site density along the step is high enough, the entire step may be considered a line sink, and a one-dimensional analysis is possible. The kink site density itself is dictated by free energy considerations and orientation of step and increases with temperature (Leamy *et al.*, 1975). Two cases may arise (Chernov, 1984): (1) the diffusion regions are well separated, as shown in Fig. 14a or (2) they overlap, as shown in Fig. 14b. If λ_s is the surface



(a)



(b)

FIG. 14. Silicon adatom density as a function of distance from a step. (a) The steps are well separated and (b) the steps are close. This is valid only if the steps may be considered slow moving, i.e., at low supersaturation.

diffusion length of silicon atoms, a diffusion profile is set up for approximately a distance λ_s on either side of the step. At the step itself the concentration of the adatoms must be equal to the surface equilibrium concentration at the growth temperature which is given by the equilibrium vapor pressure at growth temperature as

$$n_{\text{seq}} = \frac{P_0}{\sqrt{2\pi kT_0}} \tau_0 \quad (2.6.3)$$

where P_0 is the equilibrium vapor pressure, T_0 the substrate temperature, and τ_0 is the residence time of silicon at the substrate temperature T_0 and is given by

$$\tau_0 = v_{\text{Si}} \exp(-E_{\text{dsi}}/kT) \quad (2.6.4)$$

If the adatom concentration between steps is given by $n_s(x)$ then the flux of adatoms is given by

$$J_s = -D_s \left[\frac{dn_s(x)}{dx} \right] \quad (2.6.5)$$

where D_s is the adatom diffusivity and x the direction of step propagation. Since reevaporation can be neglected the rate of consumption of adatoms at the step must be equal to the impinging flux in steady state

$$dJ_s/dx = F_{\text{Si}} \quad (2.6.6)$$

If the steps are considered stationary the concentration profile is symmetric, and the lateral flux is zero midway between the steps. Choosing the reference point midway between steps,

$$\left. \frac{dn_s}{dx} \right|_{x=0} = 0 \quad (2.6.7)$$

under those conditions (Abbink *et al.*, 1968)

$$n_s(x) = n_{\text{seq}} + \frac{F_{\text{Si}}}{D_s} \left[\left(\frac{d_s}{2} \right)^2 - x^2 \right] \quad (2.6.8)$$

where d_s is the step separation. The flux at the step contributes to step motion and is given by

$$\begin{aligned} J_{\text{step}} &= D_s \left(\frac{dn_s(x)}{dx} \right)_{x=d_s/2} \\ &= F_{\text{Si}} \lambda_s \end{aligned} \quad (2.6.9)$$

The velocity of the step, therefore, is given by

$$V_{\text{step}} = F_{\text{Si}} \lambda_s / N_{0s} \quad (2.6.10)$$

where N_{0s} is the atom density of silicon on the growth plane.

The preceding arguments are correct only for the case of close step spacing where the entire terrace area contributes to flux to the step ($d_s \sim \lambda_s$, where λ_s is the mean diffusion distance). In the more general case the limiting velocity of the step for parallel steps is given by (Burton *et al.*, 1951)

$$v_{\text{step}} = 2\sigma \lambda_s v \exp[-W_{\text{sk}}/kT] \tanh(d_s/2\lambda_s) \quad (2.6.11)$$

Once again this assumes that the step motion can be neglected while solving the diffusion problem. This approximation is generally true when the average distance travelled by the atom is large compared to the distance travelled by the step,

$$\lambda_s \gg v_{\text{step}} t_s$$

where t_s is the representative time scale. This can be written in terms of the supersaturation σ as

$$2\sigma \exp\left[-\frac{W_{\text{sk}}}{kT}\right] \tanh\left(\frac{d_s}{2\lambda_s}\right) \ll 1 \quad (2.6.12)$$

where W_{sk} is the kink energy (the activation energy for a kink atom to move out).

If the steps are reasonably spaced $d_s \sim \lambda_s$ and the supersaturation is large, the assumption of stationary steps is invalid. In such cases the diffusion equation must be solved with moving boundary conditions (Mullins and Hirth, 1963). Voigtlaender *et al* (1985) have attempted such a solution for a regularly spaced step array and they show that the steady-state adatom concentration profile is skewed against the direction of the step motion. this is shown in Fig. 15. The skew is more pronounced at higher supersaturations. This implies that much of the atom supply for the step motion comes mainly from atoms on the terrace at the "bottom" of the step which have to migrate shorter distances along a steeper concentration gradient, which shortens the "capture" time of the adatom. This treatment assumes that the step captures atoms from both the top and the bottom with unity probability. This, however, is not strictly true (Ghez, 1985). In fact, those atoms that approach the step from the top are very likely reflected, and in that case the adatom density profile would not vary much as it approached the step from the top. Thus nonunity capture at the step accentuates the effects of step motion.

The step propagation mechanism was experimentally verified by Ab-

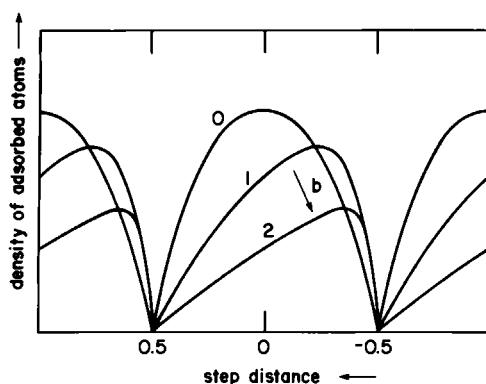


FIG. 15. Silicon adatom densities plotted as a function of distance from step for different normalized supersaturations b . The skew in the distribution arises because of significant step movement at higher supersaturations. See text. [From Voigtlaender *et al.* (1985).]

bink *et al.* (1968) who performed electron replication microscopy *in situ* and were able to resolve monolayer steps. Their surfaces were subject to high hydrocarbon contamination. As a result, there was frequent pinning of steps at silicon carbide particles formed as a result of carbon contamination.

Their observations were that this pinning of steps could lead to the arrest of the step propagation. Initially, if cleaning is imperfect there may be many such pinning sites, although as cleaner surfaces are generated the steps do not have to bow around the impurities and straighten, leading to the idealized step growth mechanisms. In fact, Kasper (1985), who performed similar experiments in a UHV environment, concluded that the surface steps are of low height and there is little bunching or pinning of steps. These conditions no doubt aid the growth of crystalline films with a low density of stacking faults and other dislocations. Furthermore, it is shown that the majority of steps arise due to unintentional misorientation of the substrate, and that in good quality substrates as used in microelectronics the dislocations are not a source of steps. More recently, Sakamoto *et al.* (1985) have observed RHEED intensity oscillations during growth. Using this technique, diffraction patterns using a fixed azimuth are monitored. If periodic oscillations are observed while maintaining a constant growth rate a layered growth mode is deduced.

While in CVD growth of silicon films it has been demonstrated (Tung, 1968) that the growth rate on (110) orientations is higher than on (100) orientations which is higher than on (111) directions, there is no such

growth-rate dependence in the case of silicon grown by MBE. This happens because rejection of adatoms by desorption or chemical inactivity is minimal, and the growth rate is dictated solely by the silicon arrival rate, provided there is adequate surface mobility of the adatoms to sustain crystalline growth. If this latter condition is not fulfilled, defective or even amorphous growth may take place. However, steps may tend to propagate in preferred directions. This is because those steps which have the highest kink density will tend to have higher propagation velocities. In fact, Abbink *et al.* (1968) imply that on (111) planes steps seem to propagate $\langle \bar{1}\bar{1}2 \rangle$ directions, but Cullis and Booker (1971) found no preferred direction, at least, on (110) surfaces.

2.6.2 Growth Temperature Considerations

Jona (1966b) has discussed the temperature considerations for homoepitaxial growth of silicon by vacuum deposition. Epitaxial growth can occur only if the adsorbed atoms have sufficient surface mobility. Since in molecular-beam epitaxy, the adatoms come with only thermal energy and quickly equilibrate with the substrate, the available migration energy is related to the substrate temperature.

Epitaxial growth has been claimed at temperatures as low as 200°C (de Jong, 1983) and even room temperature. However, epitaxial growth *per se* is not the issue. Epitaxial growth of high-quality material with extremely low levels of defects and structural damage is the important criterion. We shall address the question of defects later but mention here that the lowest temperature at which epitaxy may occur on a particular orientation, is an indicator of the ease at which the crystal growth process occurs. However the mechanism of growth at low temperatures may not be identical to those at higher temperatures. For example Jona (1966b) postulates that growth at low temperatures occurs via the crystallization of an intermediate "amorphous" (or polymicrocrystalline) phase. This phase may be a monolayer thick. Jona further argues that the lower epitaxial temperature observed on (100) surfaces as compared to (111) surfaces is plausible because of the nature of the surface structure. A silicon atom on a (111) surface is singly bound and has rotational freedom, while it is doubly bound on the (100) surface. The corrugated nature of the (111) surface compared to the (100) surface makes it more difficult to satisfy all bond requirements simultaneously. This would perhaps explain why growth may proceed at lower temperatures on (100) surfaces.

So far the role of surface reconstruction on epitaxy has been neglected. The silicon surfaces (as do other semiconductors) are reconstructed in that surface atoms do not occupy the same positions as they do in the

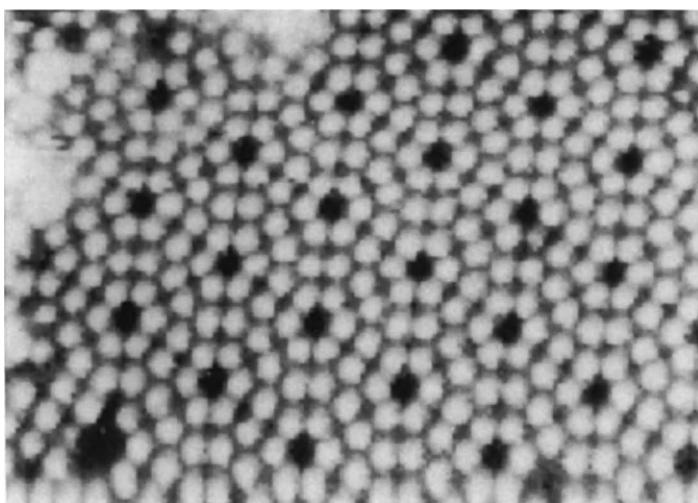


FIG. 16. Scanning tunneling micrograph of the 7×7 reconstruction showing the periodic surface topography on an atomic scale. [From Demuth *et al.* (1986).]

bulk. For example, a silicon (111) surface on cleaning assumes a 7×7 structure, as shown in Fig. 16, which shows a scanning tunneling micrograph of the surface. This implies that the surface unit mesh is 7 times larger than the bulk mesh. During MBE growth this 7×7 structure is retained.

The 7×7 structure is fairly complex, and a consensus on its interpretation is hard to come by (Chadi *et al.*, 1980; Himpsel, 1983; Bennet *et al.*, 1983). Nevertheless based on ion scattering (Tromp *et al.*, 1985) and other experiments (Binnig *et al.*, 1983) the reconstruction is believed to involve 49 surface atoms, and the perturbations are estimated to penetrate at least a few monolayers into the subsurface. In fact, certain defects such as a two-dimensional “stacking” fault as shown in Fig. 17 are also postulated. While the surface may grow by the step growth mechanism, it does so

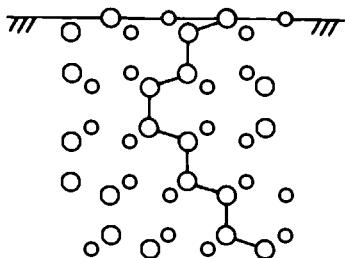


FIG. 17. One possible schematic representation of the 7×7 reconstructed silicon surface, indicating a “partial stacking fault.” The view here is a side view with larger circles and smaller circles representing atoms in different layers. The solid line highlights the partial stacking fault. [Adapted from Tromp *et al.* (1985) and Bennet *et al.* (1983).]

onto a reconstructed surface. This reconstructed surface then transforms into the bulk crystal in the subsurface, and this is a solid-phase transformation. While not much is known about this transformation, clearly it influences the crystal quality and the ease of epitaxy. Grossmann and Feldman (1985) have studied the overgrowth of silicon on (100) and (111) surfaces. They employ ion scattering techniques and find that reordering of a deposited layer of silicon takes place at least to some extent on a (100) 2×1 reconstructed surface even at room temperature in contrast to a (111) 7×7 reconstructed surface, where a higher temperature is required.

2.7 DOPING

One of the main advantages of silicon MBE lies in the fact that simultaneous incorporation of dopants during growth is possible. Since growth temperatures are below that at which solid-state diffusion occurs, the doping profiles that may be generated in MBE are frozen in. Thus, in principle, atomically sharp doping profiles are possible; conventional techniques of doping are limited in the sharpness of doping profiles attainable. Figure 18 shows one of the best doping profiles obtained by ion implantation and subsequent thermal activation. Typically, the smearing is of the order of several hundred to a thousand angstroms, caused by channelling and diffusion.

2.7.1 Doping by Spontaneous Incorporation

Practical considerations dictate the choice of dopant species employed when using thermally generated beams. On the one hand, species with very low equilibrium pressures need to be heated to extremely high temperatures in order to generate useful fluxes. The high temperatures are deleterious to vacuum integrity. On the other hand, materials with very high vapor pressures at low temperatures also need to be avoided as their fluxes would be difficult to control, especially from virtual sources. Such arguments limit the choice of useful dopant sources to antimony for *n*-type doping and gallium and aluminum for *p*-type doping, although recently, Kubiak *et al.* (1984) have reported the use of boron by thermal techniques. It is also possible to use the so-called "capture" sources such as GaP for phosphorus (Wright and Kroemer, 1982) and B₂O₃ for boron (Aizaki and Tatsumi, 1985; Allen, 1985). There is some evidence, however, that the incorporation of the unintended impurities does occur to some extent. This could lead to deep-level defects or other structural defects.

We have seen in the previous section that the actual mechanism of

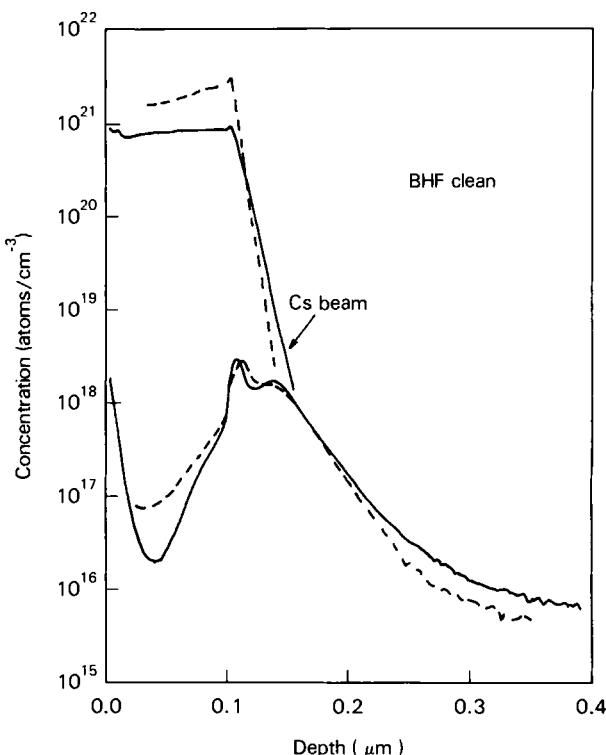


FIG. 18. SIMS depth profiles of a state-of-the-art doping transition obtained by ion implantation and diffusion. The higher concentration curve represents arsenic profiled with a cesium beam in polysilicon, while the lower one represents boron. The effect of channelling is clearly seen. [From Stork *et al.* (1985). Copyright © 1985 IEEE.]

silicon growth can be quite complicated. However, we may still describe the dopant incorporation mechanism by a model whose parameters do not depend to first order on the microscopic details of silicon growth. Further refinements which account for the interaction with the growth mechanism are then possible.

Becker and Bean (1977) and Bean (1978) attempted one of the earliest systematic generation of sharp doping profiles. They observed that, while they could obtain sharp profiles using gallium at 700°C, they were unable to do so in the case of aluminum and antimony at the same temperature, as shown in Fig. 19. Iyer *et al.* (1981) investigated the kinetics of doping in detail and proposed an incorporation model for dopants in silicon MBE.

Some characteristics of the commonly used dopants are:

- (1) a sticking coefficient S that is very small, typically less than 0.01 at useful growth temperatures,

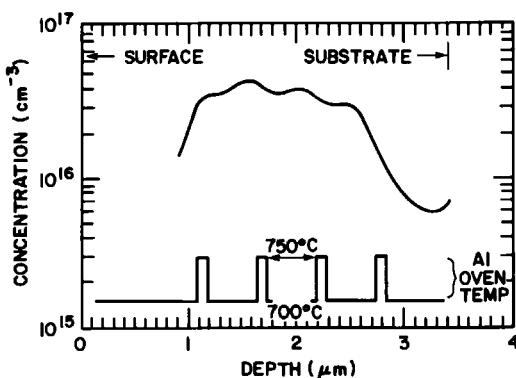


FIG. 19. Smeared aluminum doping profile measured by *C-V* techniques. In this early attempt, abrupt flux changes were effected as indicated. [From Becker and Bean (1977).]

- (2) a very high sensitivity of the sticking coefficient to substrate temperatures that decreases with increasing temperatures,
- (3) a high degree of electrical activation of the dopant approaching unity,
- (4) first-order incorporation processes at higher substrate temperatures and lower dopant fluxes,
- (5) long delay times at typical temperatures, translating into long distances in growth films for doping levels to reach steady state in response to sudden flux changes,
- (6) a saturation phenomenon with respect to incorporation at higher dopant fluxes, and
- (7) a degradation of film quality at very high doping levels.

The model recognizes that kinetic limitations play an important role. Crucial is the recognition that dopants do not incorporate directly into the growing lattice but first adsorb on the surface. This adsorbed phase acts as a reservoir from which dopants incorporate. We consider a silicon host surface, as shown in Fig. 20, held at a temperature T_s . Here T_s is greater than the epitaxial temperature, the temperature above which epitaxial growth occurs.

Incident on this surface is a silicon beam of flux F_{Si} . Coincident on this surface is a dopant beam of flux F_D . Since every silicon atom is incorporated into the growing lattice and contributes to film growth, it is not necessary to consider the kinetics of silicon incorporation.

The dopant flux is initially entrapped on the surface. (See Fig. 21). This initial entrapment is a result of the potential well created by the host surface. The dopant atoms are completely accommodated thermally; the reason for this is the low difference in energies between the incident atoms

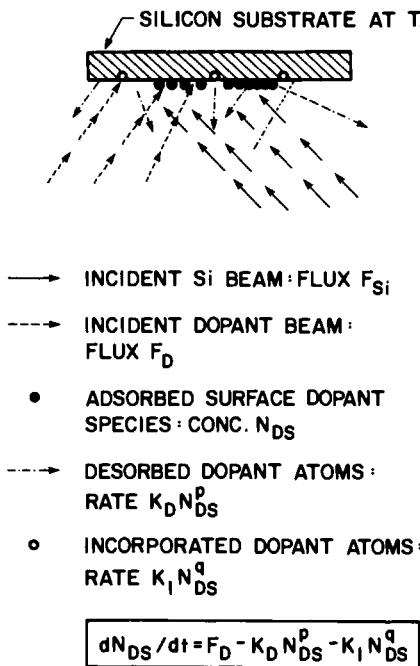


FIG. 20. Schematic representation of the silicon surface during growth with doping. The incident and desorbed beams are shown along with the incorporated atoms. [From Iyer (1981).]

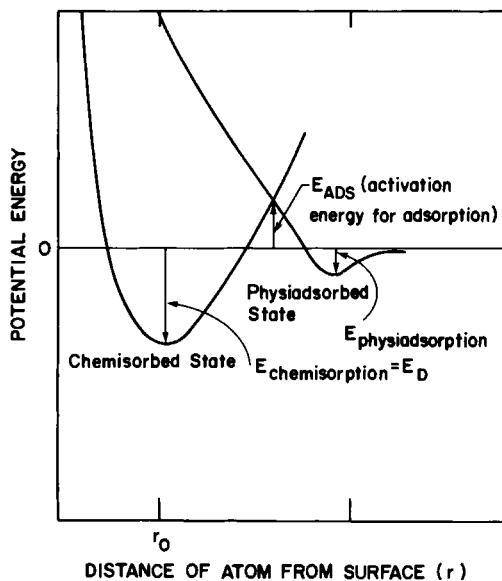


FIG. 21. Surface potential diagram for an incoming dopant atom. A local minimum for physiadsorption and the more stable chemisorbed state are shown.

and those on the surface. Experimental evidence for indium on silicon (Nguyen, 1974) suggests that this assumption is correct. It is probably true for most of the cases being considered here. The assumption of initial entrapment is also substantiated since the desorbed beam is known to be lambertian. This means that the atoms reached equilibrium with the surface and were remitted therefrom rather than being specularly reflected.

The adsorbed atoms continue to oscillate while in the potential wells at the host surface. This is the chemisorbed state in Fig. 21. The physiadsorbed state is usually not important for our analysis although it may be precursor state. Also, in most cases E_{ADS} , the activation energy for adsorption, is negligible. They are incident with thermal energy (typically a tenth of an electron volt or less) and dissipate this energy by launching optical phonons on the surface. It is also possible for the atoms to obtain energy by this process and jump out of the well or desorb. This is a statistical process and may be described by a desorption coefficient K_D and the desorption order p . The desorption order is the order of the rate-limiting reaction involved in the various steps in the desorption process. The total desorption rate depends on the substrate temperature and the concentration of adatoms. The adatoms may also incorporate into the growing lattice at an incorporation rate to be described later. Thus, atoms enter the surface phase by the incident flux, and they leave either by desorption or by incorporation. Each of these is described in detail later. At any time t , the number of adatoms is given by $N_{DS}(t)$ adatoms/cm².

The desorption rate may be described by

$$\frac{dN_{DS}(t)}{dt} = -K_D[N_{DS}(t)]^p \quad (2.7.1)$$

Here K_D is the desorption coefficient, and p is the order of desorption. The absolute desorption rate will always increase with N_{DS} .

In order to describe the desorption process we must first specify K_D and p ; K_D itself may be a function of N_{DS} . It is also a sensitive function of temperature. Frenkel (1924) has shown that K_D may be expressed as

$$K_D = K_{DO} \exp(-E_D/kT) \quad (2.7.2)$$

This activated process has a preexponent K_{DO} which is related to the vibrational frequency of the atom. The activation energy itself is related to the depth of the potential well in which the atom oscillates. The details of determining E_D have been dealt with elsewhere (Iyer, 1981; Metzger, 1983).

It is possible that the desorption of several orders proceeds simultaneously in which case Eq. (2.7.1) may be rewritten as

$$\frac{dN_{DS}}{dt} = -\sum_p K_{Dp}[N_{DS}(t)]^p \quad (2.7.3)$$

where

$$K_{Dp} = K_{DO_p} \exp(-E_{Dp}/kT) \quad (2.7.4)$$

However one process with a single value of p will invariably dominate.

The fact that an adsorbed atom does not promptly incorporate shows that there is a finite rate of incorporation. The actual process of incorporation probably involves a few steps, each being an activated process. Our model presumes that one of these steps is rate determining, and thus the process of incorporation is describable as a process with a single activation energy. We may describe the process by an incorporation coefficient K_I given by

$$K_I = K_{IO} \exp(-E_I/kT) \quad (2.7.5)$$

where K_{IO} is the preexponent and E_I is the activation energy. Summing up the rates for different orders the total rate of incorporation may be written as

$$\frac{dN_{inc}}{dt} = \sum_q K_{IOq} \exp(-E_{Iq}/kT)(N_{DS})^q \quad (2.7.6)$$

The assumption here is that incorporation may take place by single atoms or in twos, threes and so on, corresponding to different values of q .

In practice we need consider only the $q = 1$ term. This is so because the incorporation of foreign atoms introduces strain into the crystal. The incorporation of larger aggregates would need a higher activation energy. This means that larger aggregates would incorporate more slowly. Thus, the incorporation of $q > 1$ may be neglected if single atoms can incorporate. For the same reasons, incorporation into interstitial sites is unlikely. Experimentally, this is observed in the complete activation of all the dopant. (Note that complete activation does not imply complete ionization.) Furthermore, since we are considering electrically active dopants and can only measure shallow ionization level dopants, it turns out that only the singly incorporated atoms are of importance. For these reasons we will in future analysis retain only the $q = 1$ term in Eq. (2.7.6).

We now consider all the processes simultaneously and write down an expression for the increase in the concentration in the surface species of the dopant. In its most general form this is

$$\frac{dN_{DS}}{dt} = F_D - \sum_p K_{Dp}(D_{DS})^p - K_I N_{DS} \quad (2.7.7)$$

Equation (2.7.7) can be solved once a value for p is chosen.

The case $p = 1$ is the easiest to solve. It is also very important practically. Equation (2.7.7) reduces to

$$\frac{dN_{DS}}{dt} = F_D - K_D N_{DS} - K_I N_{DS} \quad (2.7.8)$$

We analyze Eq. (2.7.8) in the steady state, i.e., with $dN_{DS}/dt = 0$. Then

$$N_{DS} = F_D / (K_D + K_I) \quad (2.7.9)$$

Once steady state has been reached, the number of incident atoms per second is equal to the sum of those that desorb and incorporate per second. Equation (2.7.9) also shows that there is on the host surface a concentration of the surface species of the dopant atoms. From these a portion incorporate into the growing lattice. This rate is therefore

$$\frac{dN_{inc}}{dt} = K_I \frac{F_D}{K_D + K_I} \quad (2.7.10)$$

The rate of the number of atoms that incorporate to those that are incident, on a per unit time basis in steady state, is called the sticking coefficient s . Thus

$$s = \frac{dN_{inc}/dt}{F_D} = \frac{K_I}{K_I + K_D} \quad (2.7.11)$$

The resultant steady-state bulk doping concentration N_{DB} is given by inspection as

$$N_{DB} = \frac{dN_{inc}/dt}{F_{Si}} N_O \quad (2.7.12)$$

where N_O is the number of silicon atoms per cubic centimeter. Simplifying Eq. (2.7.12) we get

$$N_{DB} = s(F_D/F_{Si})N_O \quad (2.7.13)$$

The sticking coefficient is an important parameter. It is also referred to as the incorporation probability by some authors. When the sticking coefficient is small, i.e., $s \ll 1$, we have $K_D \gg K_I$ or the desorption rate is higher than the incorporation rate. Then,

$$s \approx K_I/K_D \quad (2.7.14)$$

i.e., the ratio of the incorporation coefficient to the desorption coefficient.

Since both incorporation and desorption have been assumed to be activated processes we get

$$s = \frac{K_{IO}}{K_{DO}} \exp\left(\frac{E_D - E_I}{kT}\right) \quad (2.7.15)$$

Therefore, s behaves like a simple exponential with respect to inverse temperature. The energy coefficient is the difference between the desorption and incorporation energies and the preexponent is the ratio of the two preexponents.

Let us now consider a clean host surface and apply a step flux F_D , i.e.,

$$F_D = \begin{cases} 0, & t < 0 \\ F_D, & t \geq 0 \end{cases}$$

We then have

$$dN_{DS}/dt = F_D - (K_I + K_D)N_{DS} \quad (2.7.16)$$

$$N_{DS}(t) = \frac{F_D}{K_I + K_D} [1 - \exp -(K_I + K_D)t]$$

The time constant of interest here is

$$\tau = (K_I + K_D)^{-1} \quad (2.7.17)$$

The significance of τ , which we shall henceforth refer to as the characteristic dopant incorporation time, is the following. When the silicon/dopant system is subjected to a sudden change of flux, the system approaches its new steady state in an exponential manner in time. The initial rate of approach is given by $1/\tau$. For practical purposes we may assume that steady state has, in fact, been achieved after about four or five time constants.

Large desorption and incorporation coefficients mean smaller characteristic dopant incorporation times, while smaller values mean that steady state will take longer to achieve. A further point to note is that when the sticking coefficient is small, τ is equal to the mean time of residence of the dopant atoms on the surface (τ_D).

The incorporation rate follows the surface concentration behavior. Thus, the bulk doping concentration as a function of time is

$$N_{DB}(t) = s \frac{F_D}{F_{Si}} N_0 \{1 - \exp[-(K_I + K_D)t]\} \quad (2.7.18)$$

If the growth rate is constant, as we have assumed here, the temporal variation is easily transformed to a spatial variation by

$$x = vt \quad (2.7.19)$$

where x is the coordinate of film thickness and v the velocity of growth. This velocity is given by

$$v = F_{Si}/N_0 \quad (2.7.20)$$

Thus,

$$N_{DB}(x) = s \frac{F_D}{F_{Si}} N_0 \left\{ 1 - \exp \left[- \left(\frac{K_I + K_D}{v} \right) x \right] \right\} \quad (2.7.21)$$

Note that in the above transient analysis we have assumed that K_I and K_D are constants, which means that the temperature is constant and there are no saturation effects. The quantity $[(K_I + K_D)/v]^{-1} = \lambda$ is the spatial counterpart of τ . It represents the thickness of film over which variations in doping density occur in response to sudden changes in doping flux.

It must be mentioned here that both τ and λ become smaller as the temperature of growth is increased. However, the sticking coefficient falls with increasing temperature, and this may impose doping limitations on the abruptness of doping profile changes and on the upper level which may be achieved with constant temperature growth.

Figure 22 shows the residence times for gallium and antimony on silicon surfaces as a function of temperature. The values for gallium were obtained by isothermal description studies while those for antimony were obtained by ramped desorption. It is seen for gallium that at 600°C the residence time may be up to tens of thousands of seconds, translating to profile smearing of up to several micrometers at practical growth rates. The

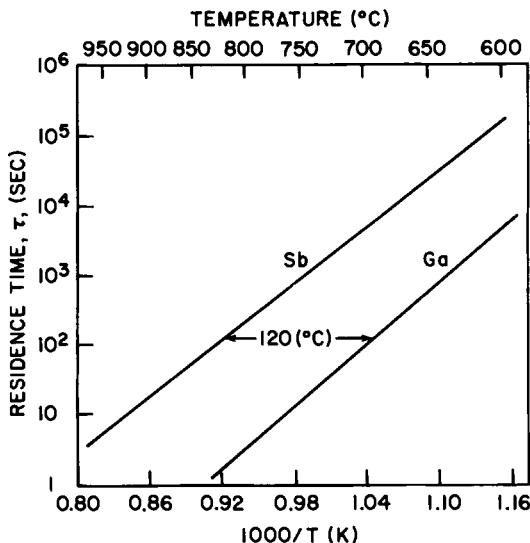


FIG. 22. Residence times for gallium and antimony on silicon. [Adapted from Iyer (1981) and Metzger (1983).]

situation for antimony is even worse and profile smearing may exist even at 800°C. It is clear though that at 700°C, the smearing for gallium would only be of the order of a hundred angstroms at most.

The sticking coefficients have also been measured and these are shown in Fig. 23 for gallium and Fig. 24 for antimony. The agreement with the model is evident in the case of gallium with an energy dependence of the sticking coefficient $E_s = 1.6$ eV. The desorption energy was measured to be about 2.9 eV so that activation energy for incorporation is about 1.3 eV. Interestingly the values for these energies seem independent of crystal orientation. In the case of antimony, the agreement is good at temperatures above 700°C where the value of E_s is 2.05 eV. It is important to note that the steady-state coverage of antimony is less than one monolayer in this case. The incorporation energy E_{ISb} was obtained to be quite low (~ 0.4 – 0.7 eV) with a large uncertainty of the incorporation energy.

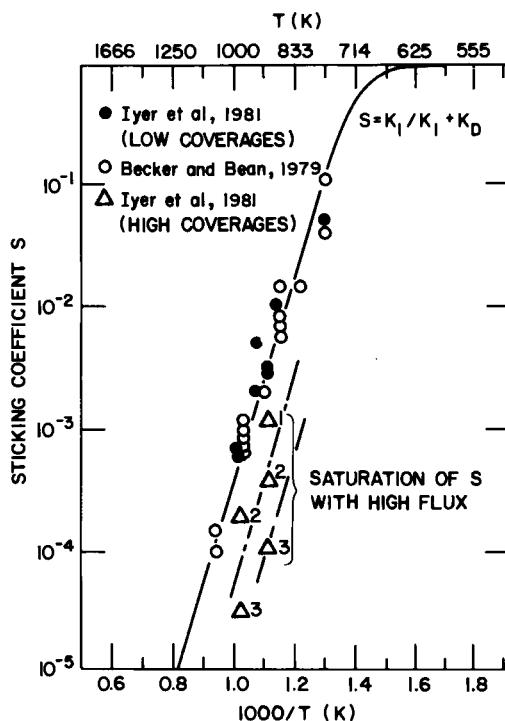


FIG. 23. Sticking coefficient for gallium measured as a function temperature. Also shown are the sticking coefficients obtained at very high fluxes. The solid line is obtained from Eq. (2.7.11).

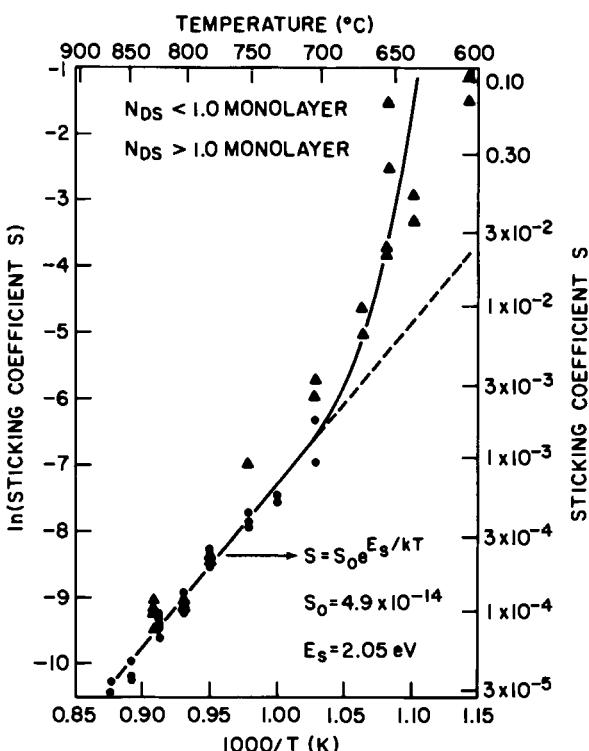


FIG. 24. Antimony sticking coefficient as a function of temperature. At high equivalent surface coverages of antimony, there is an apparent enhancement of sticking coefficient. [From Metzger and Allen (1984).]

2.7.1.1 Details of Incorporation and Its Influence on Growth

It is clear that the surface phase of the dopant plays a very significant role in the incorporation process. It is therefore necessary to investigate the nature of the dopant on the silicon surface. The surface mobility of the dopant as well as the bonding of the dopant both to the silicon surface and other dopant atoms plays an important role. Both gallium and antimony when deposited on silicon exhibit two phases. The first phase represents the dopant bonding to the silicon surface, and the second phase represents the dopant bonding to itself. In the case of antimony, the antimony vapor pressure is large enough at substrate growth temperatures (600–900°C) such that the second phase (Sb–Sb) does not condense, resulting in a maximum two-dimensional coverage of approximately one monolayer of antimony on the silicon surface (Metzger, 1983). The gallium vapor pressure is low enough so that at growth temperatures (600–900°C)

both phases may exist under large gallium flux conditions resulting in three-dimensional nucleation of gallium on the silicon surface.

As we have seen, under conditions where surface impurities are minimal, silicon growth is by lateral migration of steps along the silicon surface. It may, therefore, be questioned as to whether this growth mode is preserved in the presence of a fairly significant surface phase of the dopant. In the case of gallium doping, layered growth by lateral step migration is inferred from RHEED observations where streaking occurs after a few thousand angstroms of film growth. Similar observations are made for antimony at low coverages. Furthermore, good defect densities (not more than in the substrate) have been reported in several MBE laboratories at low to moderate doping levels. Both these observations indicate that at low coverages the layered growth model is valid. The question that then arises is what are the microscopic steps in the incorporation process. We consider three possible cases (Iyer *et al.*, 1984):

(1) Dopant incorporation may proceed by migration from the dopant cluster and diffusion to a kink site at the migrating silicon step.

(2) Alternatively, the migrating step may encounter a cluster and move past it. During the process of the step migration through the cluster, dopant may be incorporated into it. In both cases (1) and (2), it is implied that the dopant does not modify the silicon growth mechanism.

(3) The presence of significant amounts of dopant modifies the growth mechanism. Additional nucleation of silicon, leading to deviations from the layered growth mode, may occur. This results in an increased number of incorporation sites and, consequently, increased incorporation. This has been observed in the case of antimony doping at high antimony coverage (Metzger and Allen, 1984). In addition, the electrical quality of the films is degraded in this case, and there may be incomplete activation. This is evident from the mobility data reproduced in Fig. 25, where at high doping levels corresponding to high surface coverages, significant mobility deterioration is observed (Konig *et al.*, 1981; Metzger and Allen, 1984).

Cases (1) and (2) merit more consideration as they yield better film structure and film properties. The average step velocity is given by

$$v_s = F_{Si}/N_0 \quad (2.7.22)$$

where F_{Si} (atom/cm² sec) is the silicon flux and N_0 (atoms/cm³) is the silicon atom density.

It is easily seen that in case (1) where the dopant atoms migrate to kink sites at steps, the bulk doping level N_{DB} is inversely proportional to F_{Si} . This is because the supply of dopant atoms that can reach incorporation

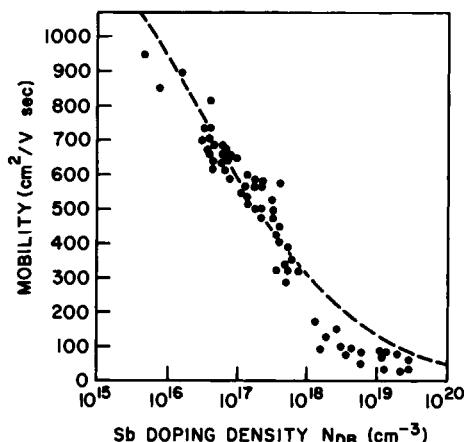


FIG. 25. Majority carrier mobility plotted as a function of carrier concentration for antimony-doped silicon. The dashed line represents bulk. [From Metzger and Allen (1984).]

sites is fixed by the quantity of dopant on the surface. Increasing the silicon flux, or in other words the average step velocity, means that the step has less time to catch a dopant atom. On the other hand, if case (2) prevails, where the dopant incorporates while the step moves past the dopant, we would expect the bulk doping level N_{DB} not to vary with the step velocity or equivalently with the silicon flux. This is because although the number of atoms being incorporated in a given time is greater, the volume it incorporates into is also proportionately greater. Experimental limitations often preclude significant variations of the silicon growth rate. However, in the case of antimony, the work of Tabe and Kajiyama (1983) suggests that the doping level is independent of F_{Si} at least over a factor of two, indicating that in some regimes the second case of incorporation prevails. In the case of gallium, indications are that there is decreased doping level obtained at given flux and substrate temperature for increased silicon flux.

Let us consider further the effect on sticking coefficient. In the case of the migrating adatom incorporating into a moving step, we recognize that several microscopic steps are involved:

- (1) In the case of clustered adatoms in the surface phase, the atom must first leave the cluster. There is an activation energy associated with this process which will be much less than the desorption activation energy, but more than the surface diffusion energy.
- (2) Once the atom breaks away from the island, it migrates on the silicon surface until a suitable kink site is encountered. This migration is

governed by the surface diffusivity of the dopant atom on the silicon surface.

(3) Finally, the dopant atom will incorporate at the kink site.

The supply of dopant atoms in this case, from the considerations mentioned in step (1) is limited by the perimeter of the cluster. We shall therefore refer to this mode as perimetric incorporation.

In the case of incorporation as the step moves through the cluster, the microscopic step involved is the transfer of the atom from the cluster-silicon interface into a kink site on the moving step. This is merely a single jump across the interface. The activation energy for this process is therefore expected to be fairly low. The supply of dopant atoms in this case is dictated by the area of the dopant cluster-silicon interface. We shall therefore refer to this mode as areal incorporation.

We propose that the incorporation rate,

$$R_i = K_i(N_{DS})N_{DS} \quad (2.7.23)$$

can be linearized and expressed as

$$R_i = K_i N_{DS,eff} \quad (2.7.24)$$

where $N_{DS,eff}$ is the effective surface concentration of the dopant, i.e., the dopant that is available and K_i depends only on the temperature. We may now relate $N_{DS,eff}$ to the dopant flux F_d . The clusters may be assumed to be hemispherical for the purpose of this discussion. The addition of dopant atoms on the surface could result in increasing the number of the islands or increasing the volume of the island.

For perimetric incorporation if growth by volume increase is dominant we have

$$N_{DS,eff,p,v} \propto F_d^{2/3} \quad (2.7.25)$$

and if growth by the increase in the number of clusters is dominant we have

$$N_{DS,eff,p,n} \propto F_d \quad (2.7.26)$$

Obviously, when the number of clusters is small, i.e., at very low coverages, increased flux would contribute to increasing the number of clusters, and when coverage is high additional dopant flux contributes to an increase in cluster volume.

The sticking coefficient is given by

$$s = K_i N_{DS,eff}/F_d \quad (2.7.27)$$

Substituting the expression for N_{DS} from Eq. (2.7.25) for perimetric incorporation with volume growth results in

$$s_{p,v} \propto K_i F_d^{-1/3} \quad (2.7.28)$$

Substituting the expression for N_{DS} from Eq. (2.7.26) for perimetric incorporation with an increase in the number of clusters results in

$$s_{p,n} \propto K_i \quad (2.7.29)$$

Thus, at very low fluxes, corresponding to very low coverages, the sticking coefficient would be independent of flux but with increasing coverage and flux would show a $F_d^{-1/3}$ dependence.

In the case of areal incorporation, $N_{\text{DS,eff}}$ is proportional to the area of the interface between the cluster and the silicon surface, and this will increase linearly with dopant flux if the flux contributes to an increased number of clusters, but would increase as $F_d^{2/3}$ if the increased flux causes increased hemispherical cluster volume.

The sticking coefficient for areal incorporation under conditions of increasing volume of a cluster, $s_{a,n}$ is described by

$$s_{a,n} \propto K_i \quad (2.7.30)$$

The sticking coefficient for areal incorporation under conditions of increasing volume of a cluster, $s_{a,v}$ is described by

$$s_{a,v} \propto K_i F_d^{-1/3} \quad (2.7.31)$$

Thus, it is possible, by examining the sticking coefficient behavior with flux, to infer which mechanism is operative. This data is shown in Fig. 26 for gallium doping. The sticking coefficient is normalized to its highest value (i.e., low flux value) at the temperature of growth. The flux is normalized to that flux which produces a unit monolayer on the surface. This was done so that observations at different temperatures may be plotted together. It is seen that there is a reasonably good fit to the perimetric incorporation model.

In the case of gallium, the adlayer shows clustering or island effects even at room temperature (Fig. 27) as seen from the presence of a strong silicon Auger signal even after several monolayers of gallium have been deposited. Kawazu *et al.* (1981) have also reported on desorption of gallium from Si (111) which is higher than that reported by Iyer *et al.* (1981), indicating perhaps a weak coverage dependent lifetime. They also report an ordered overlayer of gallium resulting in a $\sqrt{3} \times \sqrt{3} \text{R}30$ structure which persists with increasing exposure. Their flash desorption studies

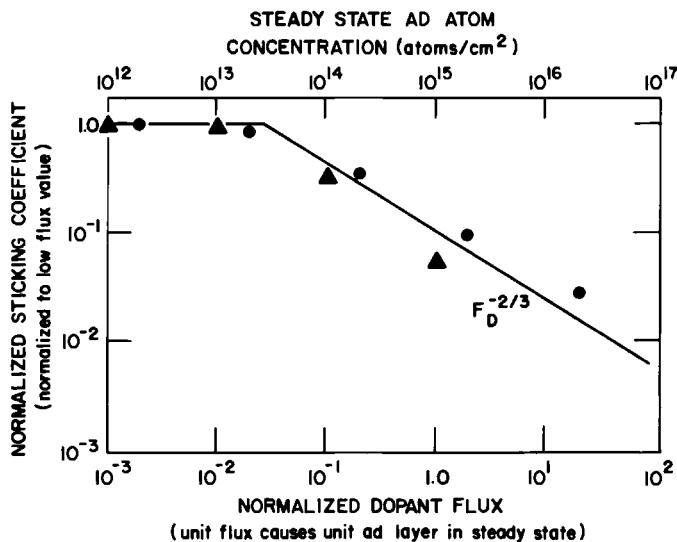


FIG. 26. Normalized sticking coefficient plotted as a function of normalized flux, showing the fall off in the sticking coefficient at higher fluxes. The sticking coefficient is normalized to the low flux value, and the flux is normalized to the flux needed to obtain a monolayer of adsorbed gallium on the surface at the growth temperature: ●, $T_s = 625^\circ\text{C}$; ▲, $T_s = 700^\circ\text{C}$. [From Iyer *et al.* (1981).]

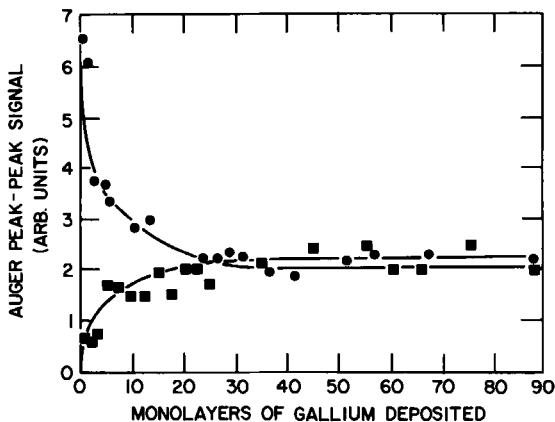


FIG. 27. Auger signal intensities for gallium (■) and silicon (●) as a function of equivalent coverage of gallium indicating a clustering phenomenon. [From Iyer *et al.* (1981).]

also indicate that there are two phases of gallium on the surface, but their AES data is in agreement with that of Iyer, indicating that clustering is occurring though the precise coverage at which it begins is not clear. Perhaps as suggested by Wright (1982) fluxes should be normalized to $\frac{1}{3}$ monolayer at which the $\sqrt{3}$ pattern appears.

The activation energy for incorporation in the case of gallium on silicon was measured to be 1.3 eV. This is a reasonable value for a gallium atom to break off from the perimeter of a gallium island along the silicon surface. This is justified as follows. The bonding energy of gallium to gallium at the surface is 2.7 eV. The desorption energy of gallium to the silicon surface has been measured to be 2.8 eV. Breaking off from the perimeter involves only half the bonds, and the activation energy may be expected to be roughly half the energy, i.e., 1.3–1.4 eV. Also, the transition at which the increased flux contributes to more clusters than to where it contributes to cluster volume growth seems to occur around 1×10^{-2} monolayers.

We may therefore conclude that from the sticking coefficient behavior with respect to silicon growth rate and the value of the incorporation activation energy, the case of gallium incorporation proceeds by gallium atoms breaking off from clusters and migrating to available kink sites. The rate limiting step appears to be the breaking off of the gallium from the cluster.

In the case of antimony, as discussed by Metzger and Allen (1984), there are several regimes. The most useful one is the low-coverage, high-substrate temperature (750–900°C) regime in which the activation energy for incorporation is 0.4 eV. This would agree quite well for antimony atoms jumping across the Sb–Si interface. This is similar to areal incorporation and would agree with the observations of Tabe and Kajiyama (1983) that doping levels are almost independent of silicon flux. At higher coverages and lower substrate temperatures the situation for antimony becomes quite complex and there is evidence that the growth mode itself changes. In this regime, the crystal quality has been observed to be poor.

Barnett and Greene (1985) and Knall *et al.* (1984) have also reported similar results for the case of indium doping of silicon. They have proposed that under some conditions thermodynamically driven surface segregation may account for the surface dopant layer. Segregation however requires a transport process such as diffusion and would not be expected to occur unless greatly enhanced subsurface diffusivities are postulated. In the absence of such enhanced diffusivities and the fact that the process of doping in silicon MBE occurs far from equilibrium, the surface concentration of the dopant is more accurately described as an accumulation layer rather than a segregated layer.

TABLE 1. Maximum Doping Levels Attained

Dopant	Technique	Growth temperature (°C)	Concentration (cm ⁻³)	Reference
Ga	Spontaneous	725	2×10^{18}	(Iyer <i>et al.</i> , 1981)
Ga	Spontaneous	650	6×10^{18}	(Kasper, 1985)
Ga	Ionized (500 V)	900	$>5 \times 10^{19}$	(Sakamoto and Komoro, 1983)
B	Spontaneous	800	5×10^{18}	(Kubiak <i>et al.</i> , 1985)
B	Ionized (BF ₂)	700	$>1 \times 10^{20}$	(Swartz, 1985)
Sb	Spontaneous	725	$>>1 \times 10^{19}$	(Iyer <i>et al.</i> , 1981; Metzger, 1983)
Sb	Secondary	800	1×10^{19}	(Kubiak <i>et al.</i> , 1985)
Sb	Secondary	650	1×10^{19}	(Jorke <i>et al.</i> , 1985)
Sb	Electron enhanced	725	3×10^{19}	(Delage, 1985)
As	Ionized	750	$>1 \times 10^{20}$	(Swartz, 1985)

Another consequence of the slow incorporation of the thermally generated dopants is the inability to achieve high doping levels without increasing the adlayer concentration beyond reasonable values. The highest doping levels reported so far for different dopants are reported in Table 1.

2.7.1.2 Growth of Profiles

One of the most important applications of silicon MBE is the growth of ultrasharp doping profiles in good-quality films. We shall, in this section, outline the principles of designing the required profiles and remaining at the same time in growth regimes that ensure adequate film quality.

The key to the growth of the desired profile is recognizing that the concentration of the dopant on the surface plays a very important role. The doping level at a certain depth in the film depends on the surface concentration at the time that part of the film was grown, the temperature, and the silicon growth rate. The latter two variables are uniquely defined and can be easily changed quite rapidly and, in general, are easily determined. The surface concentration, however, depends on the previous history of the dopant flux. Thus, we need to anticipate the required concentration of the dopant and program the flux accordingly. It can be shown that to achieve an arbitrary doping profile $N_{DB}(z)$ at a growth rate v_{Si} corresponding to a flux F_{Si} of silicon at a temperature T the dopant flux

$$F_d(t) = \frac{F_{Si}}{K_1 N_0 \tau(T)} N_{DB}(z) \cdot N_{DB}(z) + v_{Si} \tau \frac{dN_{DB}(z)}{dz} \quad (2.7.32)$$

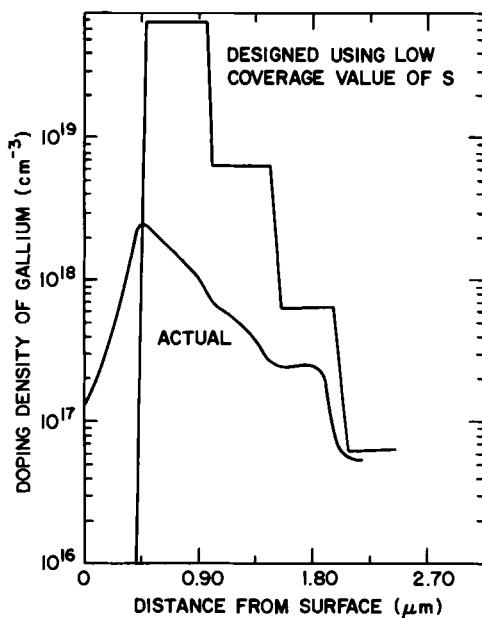


FIG. 28. Gallium doping profile obtained by flux control alone showing the delay effects. [From Iyer *et al.* (1981).]

Figure 28 shows a doping profile obtained by changing just the dopant flux (in this case gallium) with the substrate temperature maintained at 635°C. The dopant flux was increased by factors of ten from 10^{10} to 10^{14} Ga atoms/cm² sec for periods over which 0.5 μm of film were grown. The idealized curve when delay effects are neglected is shown along with the measured profile using anodic sectioning and four-point probe resistivity profiling (Iyer and Allen, 1985). First of all, the actual profile is significantly below the designed profile, more so at higher fluxes. Second, the delay effects are clearly seen, and at 625°C, as to be expected, there is considerable smearing, which corresponds to the independently measured residence times.

In spite of these long delays, it is possible to obtain extremely sharp doping transitions. These are shown in Figs. 29 and 30. In Fig. 29 a transition is made from a high level to a low level. During growth of highly doped portions of the film, there is a large concentration of gallium accumulated at the surface. If the flux is merely turned off the adlayer would take several thousands of seconds to disperse and would continue to dope the film. The technique of "flash-off" consists of briefly elevating the

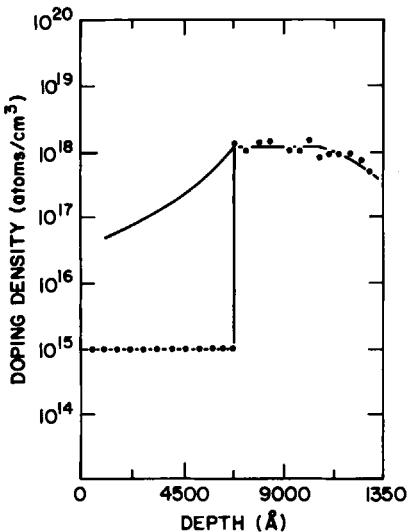


FIG. 29. High-low transition using gallium obtained using flash-off techniques. The solid line shows the profile that would result if flux control were used alone. $T_s = 625^\circ\text{C}$. [From Iyer *et al.* (1981).]

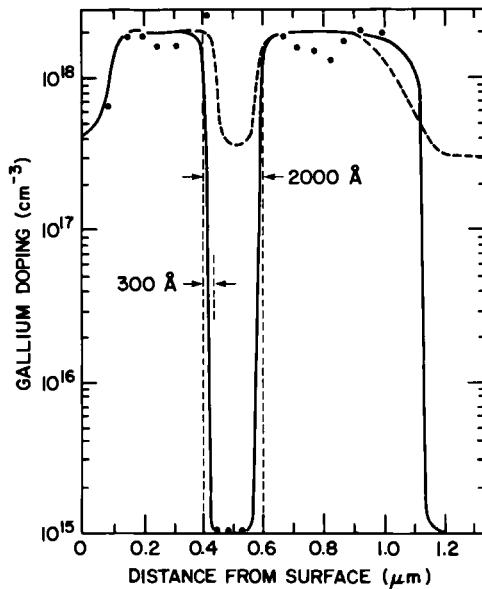


FIG. 30. High-low-high transition using gallium obtained using both prebuildup and flash-off techniques. The heavy dashed line is a SIMS profile. The solid line is obtained differential resistivity techniques. [From Iyer *et al.* (1981).]

sample temperature so that the residence time is minimal (~few seconds), thus causing almost instant depletion of the adlayer, and then reverting to the growth temperature. Growth resumes in the absence of an adlayer, and films with no intentional doping are grown.

In order to go from a low level to a high one the complementary technique of "buildup" is employed. Here the steady-state layer concentration required to attain the intended doping level is computed, and silicon growth is arrested (by shuttering of the silicon beam) until this concentration of the adlayer is reached; growth is then resumed. Figure 30 shows a high-low-high profile obtained using both flash-off and buildup techniques.

These techniques are extendable to obtain sharp transitions between any two doping levels, including different species. Such an arbitrarily designed profile is shown in Fig. 31 and also in Fig. 32. The presence of boron in the MBE film is quite interesting. Apparently, gallium used in these experiments was well purified with respect to aluminum impurities. Thus, there is a significant amount of oxygen dissolved in the gallium after exposure of the charge to air. (Gallium melts at 29°C but can be supercooled below 0°C if it has dissolved impurities.) This dissolved oxygen may react at higher temperatures with boron in the PBN crucible that holds the charge to form volatile B_2O_3 and other suboxides, which incorporate into

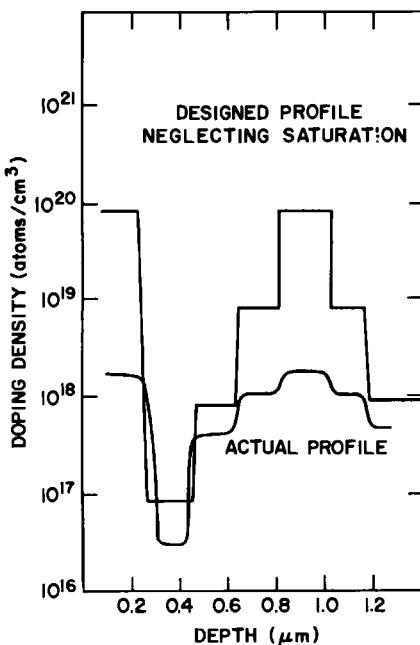


FIG. 31. MBE generated doping profile with sharp doping transitions demonstrating the capability of the $T_s = 700^\circ\text{C}$. [From Iyer (1981).]

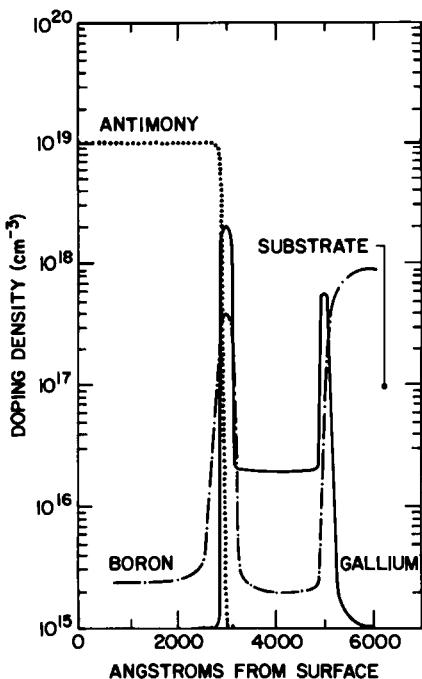


FIG. 32. Doping profile for a TUN-NETT structure. The presence of boron is discussed in the text. [From Iyer *et al.* (1981).]

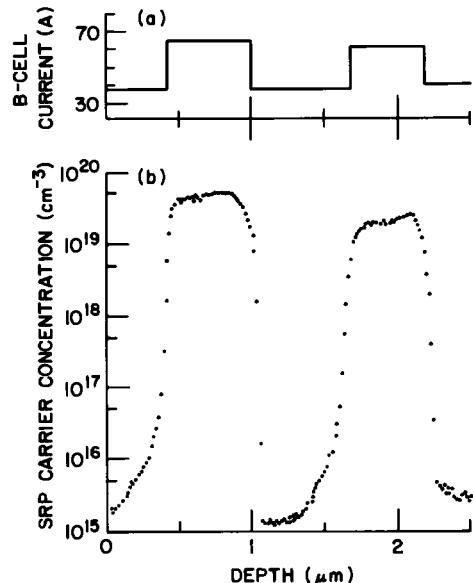


FIG. 33. Sharp doping transitions obtained using evaporated boron is shown in (b). The corresponding boron cell current is shown in (a). No significant delay effects are observed. [From Kubiak *et al.* (1985).]

the growing film. The problem is not serious since both boron and gallium are *p*-type dopants, but it can be eliminated by introducing a small quantity of aluminum which getters the oxygen into nonvolatile Al_2O_3 .

Kubiak *et al.* (1985a) have used evaporated boron as a *p*-type dopant source with very encouraging results. As shown in Fig. 33, there are no delay effects and a sticking coefficient of unity is found. They also show no deterioration of carrier mobility even at high doping levels. Indications are that there are no appreciable kinetic limitations and consequently little doping smear.

2.7.2 Doping by Low-Energy Ion Implantation

As we have seen, doping films by thermally generated dopant beams and relying on spontaneous incorporation mechanisms, while technically simple to do, follows very complex incorporation mechanisms and kinetics. It is limited by delay times, a narrow choice of dopants, and an inability to obtain extremely high doping concentrations in some cases. An attractive alternative to circumvent these difficulties is to force the incorporation through the use of low-energy dopant ion beams directed at the substrate during growth. There are certain constraints that apply when employing this technique. First of all, the implantation is done simultaneously with growth. Since dopant penetration beyond the subsurface is to be avoided and damage due to ion penetration needs to be minimized, a low-energy (typically subkiloelectron volt) dopant ion beam needs to be used. Since high-current low-energy implanters with mass selection are not readily available, the technique is still in its infancy. This method differs from conventional implantation in many ways. For example:

- (1) The energy of the implantation species is much lower (<1 keV compared to several tens or even hundreds of kiloelectron volts).
- (2) The substrate temperature during implantation is elevated above epitaxial temperature.
- (3) There is sustained growth during the implantation.

Furthermore, the incident flux and the incident species are not maintained constant during the process. While low-energy ions are expected to create lattice damage it is possible that the damage is annealed out during growth because of the elevated sample temperature (Nelson and Mazey, 1968) and the proximity of the surface to the damage region. While implantation at elevated temperature has been observed to cause enhanced diffusion (Pfister and Baruch, 1962), such diffusion may turn out to be minimal in the MBE case because the flux of ions used here, when integrated over

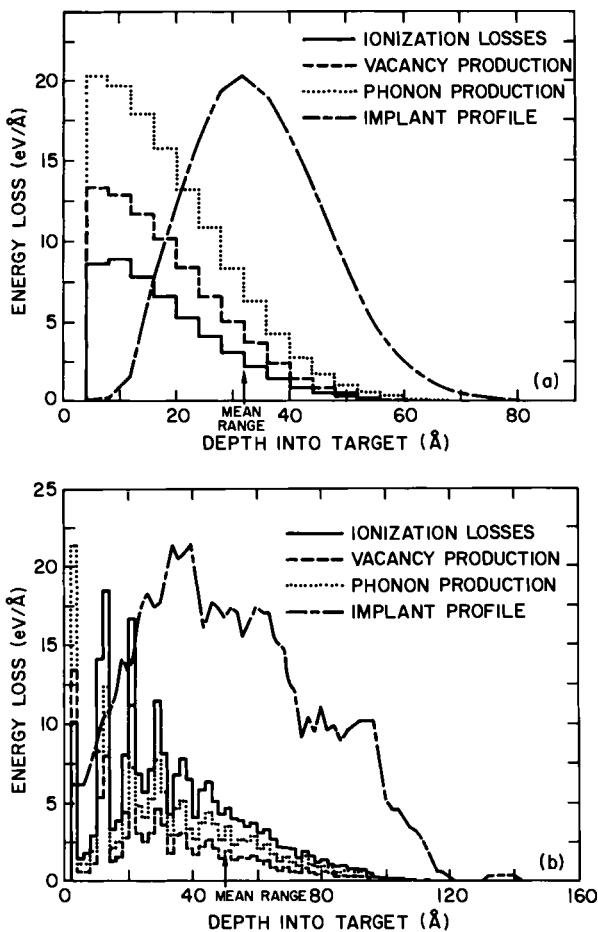


FIG. 34. Monte Carlo simulations of 1-keV ion implantation into silicon for (a) As^+ and (b) B^+ . The damage profile is shown.

the depth they penetrate, is typically lower than in conventional implantation. For example, in Fig. 34 we compare the As^+ and B^+ implantation profiles and vacancy production for two cases using Monte Carlo simulation techniques when the implantation is carried out in an MBE environment, i.e. at 1 keV. No annealing has been assumed. Since damage profiles peak closer to the surface than the implanted profiles, enhanced diffusion (if any) will occur towards the surface. Seidell *et al.* (1985) have reported that in the case where implantation is done into preamorphized silicon followed by solid-phase epitaxial regrowth around 700°C, there is complete

dopant activation but no significant thermal diffusion. The question remains though as to whether damage remains in the form of microdislocation loops, for example, and whether complete dopant activation is possible. These profiles were obtained assuming implantation into an amorphous silicon target at room temperature; so the profiles generated can only be assumed to be qualitatively akin to the MBE case.

Ota (1980) has shown that use of ion doping greatly enhances the sticking coefficient. This is seen in Fig. 35 for different energies for antimony. As is to be expected higher energies are more effective. However film quality, as estimated from carrier electrical mobility, degenerates if temperatures below 800°C or so are employed as shown in Fig. 36. Swartz (1985), however, found that in the case of boron doping using B^+ or BF_2^+ , no degradation of film quality is observed even at temperatures as low as 670°C for energies up to 800 eV. This may be expected from the observation that damage due to lighter species such as boron tends to be much lower although this does not necessarily imply that the residual damage in this case is lower (Michel, 1985).

Ion doping systems are fairly complex. A typical system consists of an

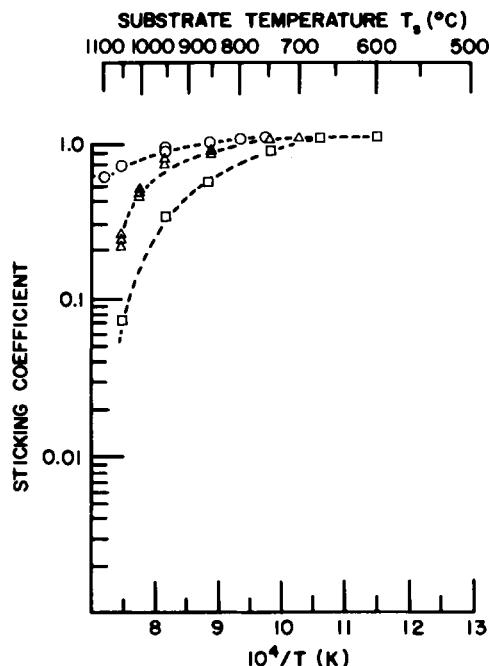


FIG. 35. Enhancement of dopant sticking coefficient for antimony in silicon using ionized dopants incident at low energies. The primary energies are ○, 800 eV; △, 600 eV; □, 400 eV. [From Ota (1980).]

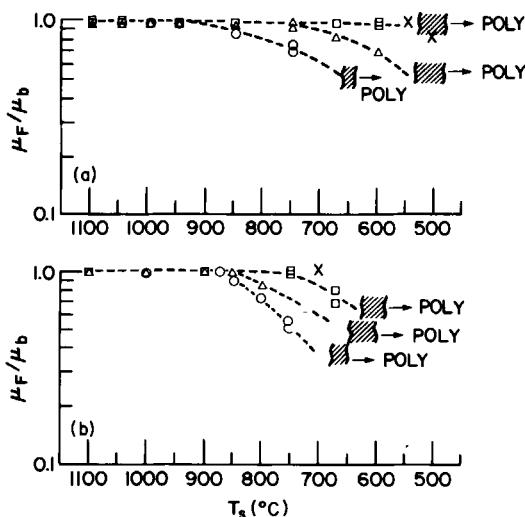


FIG. 36. Majority carrier mobility for ion implanted dopants as a function of substrate temperature showing degradation at high energies and low substrate temperature. (a) Arsenic and (b) antimony. [From Ota (1983).]

ion source—usually a Freeman ion source (Ziegler, 1984)—where the ions are generated by electron discharge. The ions are then extracted from the plasma and accelerated to about 10 kV and focused. The energetic ions are then mass filtered using a magnetic field. The selected beam is thus steered through a curved section of the beamline and decelerated to the desired voltage with reference to ground. Electrostatic scanning of the beam is also employed. In modern ion-doping systems associated with MBE the scanning system usually consists of a radial variable speed scanner so that uniform profiles are achieved over the entire wafer, which is rotating as well. The substrate is usually maintained at ground potential. This is done so that extraneously generated ions, such as from the *e*-gun parts, are not unintentionally accelerated to the substrate. The beam current to the substrate is monitored by Faraday cages. Generally, it is advisable to have more than one monitoring point, one near the substrate into which the beam is deflected during the scanning operation and another before beam deflection. With proper beam monitoring, extremely good control of the ion flux and, hence, the doping level in the film may be achieved. Doping level changes are accomplished by either changing the emission characteristics of the source—a slow process—or, preferably, by overscanning the beam off the substrate or, equivalently, blanking it off for a portion of the time.

Several workers (Clampitt and Jefferies, 1978; Sakamoto and Komoro,

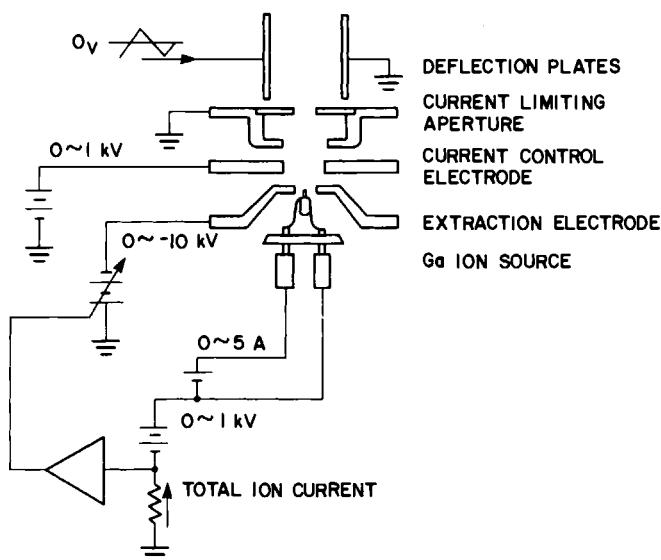


FIG. 37. Schematic of liquid ion source for doping in MBE. [From Sakamoto and Komoro (1983).]

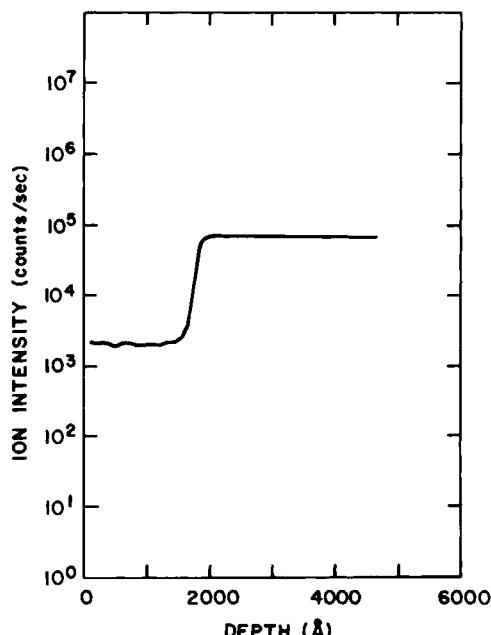


FIG. 38. Gallium SIMS profile obtained with liquid ion source. The vertical scale is in arbitrary units. [From Chrenko *et al.* (1985).]

1983) have reported the use of liquid metal ion sources. As depicted in Fig. 37, the ions are extracted by field emission from a liquid metal tip. Acceleration voltages between 500 and 3000 V have been reported. While the technique works best with metals that are liquid at low temperatures, such as gallium and indium, it can also be extended to other metals by suitable alloying techniques so that the alloy is liquid at reasonable temperatures. If the alloy constituents are chosen carefully, a preferred species is emitted (Ishitani *et al.*, 1982). Figure 38 shows a SIMS profile for an abrupt transition in gallium doping observed by Chrenko *et al.* (1985) using this technique.

2.7.3 Doping by Secondary Implantation

While doping by ion implantation affords an attractive and controlled environment, it suffers from the disadvantage that the equipment is complex and expensive. Kubiak *et al.* (1985b) and Jorke *et al.* (1985) have reported the enhancement of sticking coefficients through the application of negative potential on the substrate during growth and doping under certain circumstances. Since Kubiak *et al.* obtained correlation of doping level with positive and, to a smaller extent, negative applied potential, as shown in Fig. 39, they called it potential enhanced doping (PED). Their observations were that while the effects on antimony were quite spectacular in that a two order of magnitude enhancement was observed at about -400 V substrate bias, no appreciable effects were observed for the gallium case. Their explanation implied that modification of the electrostatic field at the surface and radiation-induced surface damage somehow modified the absorbed species and that ions (perhaps Si^+) were also involved. Jorke *et al.* showed a definite correlation between the silicon ion density impinging on the surface and the number of incorporated antimony atoms. In their work they varied the ionic component of the silicon beam from the *e*-gun evaporator, by allowing the beam to traverse a ring cathode ionizing section. Once again no effects were seen for gallium doping. The picture that emerges from their work is that incorporation is enhanced by "knock-on" implantation of individual atoms in the adlayer into the subsurface, by the impinging silicon ions. Their results are shown in Fig. 40. Their work also showed that the incorporated atom density was proportional to the adatom density and that by increasing the preadjusted concentration of the antimony adlayer, they could increase the doping density for a given antimony ion density and applied negative bias. The lack of incorporation enhancement in the case of gallium may be expected from our earlier observations that gallium tends to cluster on the silicon surface. The cross section for knock-on is thus reduced. Furthermore, since these

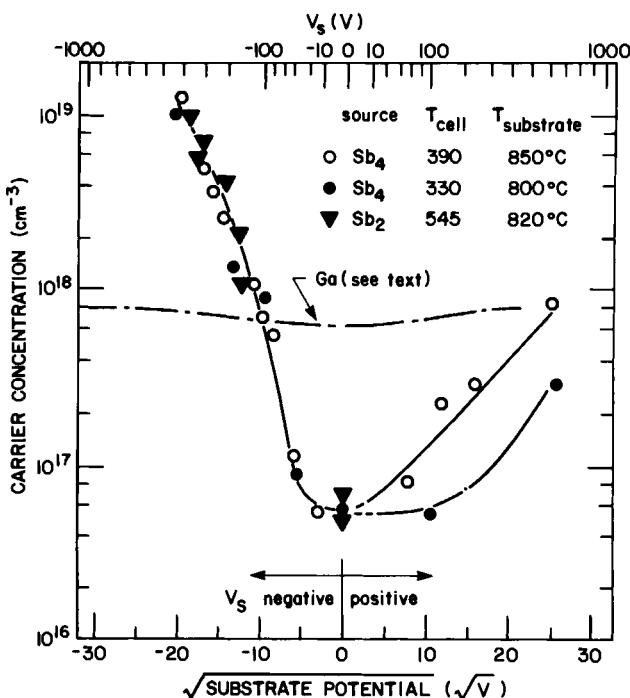


FIG. 39. Enhanced doping levels for antimony obtained for different applied potentials at the substrate. [From Kubiak *et al.* (1985a).]

clusters may be a few monolayers high, the incident silicon ion would be expected to lose its energy in the cluster without causing any knock-on.

Jorke *et al.* have also measured the cross section for incorporation for antimony using Si^+ ions accelerated at 500 V to be about $5 \times 10^{-16} \text{ cm}^{-2}$ at 650°C. We do not expect it to vary much with temperature. The incorporation coefficient concept discussed in connection with spontaneous incorporation is still valid and is given by $K_{ii} = \sigma_i J_{\text{ion}}$. Here σ_i is the cross section of incorporation, and J_{ion} is the Si^+ ion flux at the substrate. During the incorporation process the adlayer gets depleted much faster in this case than in spontaneous incorporation and must be replenished by the incident flux given by $K_{ii}N_{\text{DS}} + K_D N_{\text{DS}}$, where N_{DS} is the adlayer concentration required to give the doping level of interest. In the case of antimony at reasonable temperatures, K_D is very small. Sharp doping transitions are also possible by changing the bias on the sample between high and low values without changing the adlayer concentration. This is shown in Fig. 41. However, it may not be possible to effect arbitrary tailored transitions very easily because bias dependence is not clear and ion current density is not controllable under normal growth conditions. For example, Ostrom

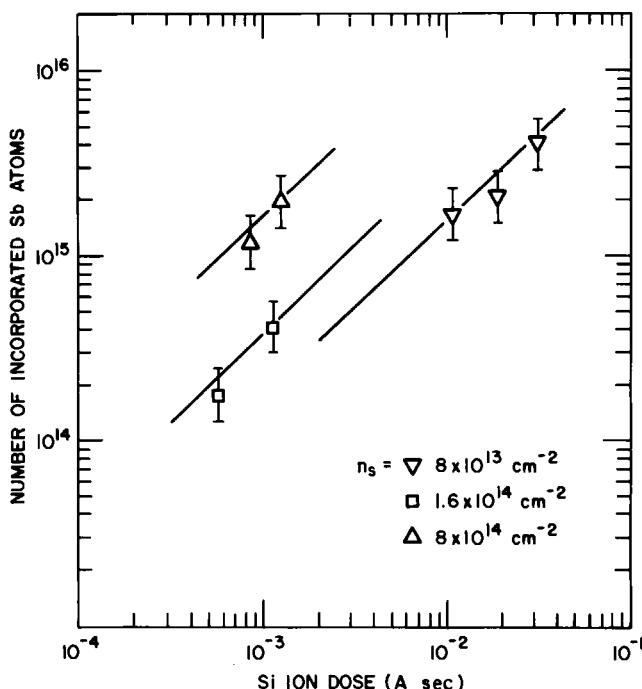


FIG. 40. Enhancement of incorporation as a function of Si⁺ ion density in silicon beam during growth. V_s = -500 V. [From Jorke *et al.* (1985).]

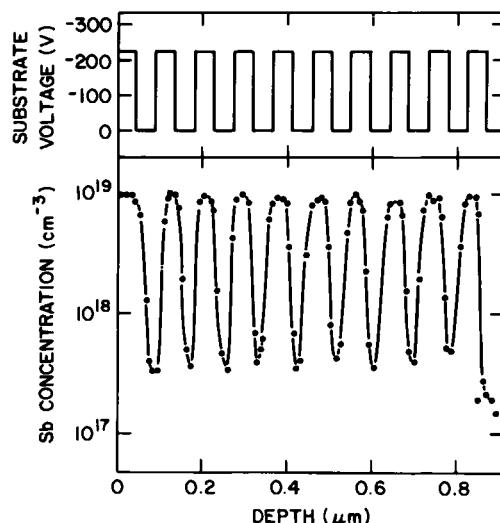


FIG. 41. Sharp doping level transitions using antimony obtained by the technique of secondary implantation. [From Jorke and Kibbel (1985).]

and Allen (1985) report only a slight enhancement at 500 V, indicating a large dependence on system variables. The advantages of doping by secondary implantation lie in the simplicity of the system. The only modification that needs to be done is the ability to bias the substrate appropriately. Since the technique produces significant enhancement even at a bias of a few hundred volts, damage is not a major concern. In fact, as reported by Itoh *et al.* (1977) there may be some enhancement of lateral mobility of the incoming silicon neutrals by energy exchange on the silicon surface leading to superior crystal quality. The disadvantages stem from the possible lack of control that this technique exhibits. Since the ions emanate as a secondary product from the *e*-beam evaporator and are not intentionally generated, there is variation in the Si⁺ ion flux. This depends on the emission current, the total silicon flux, the geometric constraints on the system, and, most of all, the condition of the silicon in the hearth, which varies during evaporation. In addition, the technique does not dispense with need for the dopant adlayer, which is a concern at high coverages. The kinetics of building up this adlayer need to be addressed when using this technique. Finally, the technique is not applicable to the commonly used *p*-type dopants.

Itoh *et al.* (1977) and Takai and Itoh (1983) used partially ionized dopant beams. It is very possible that the doping processes they observe are partially due to secondary implantation.

Delage (1985) has reported the enhancement of the antimony sticking coefficient, produced by irradiating the substrate with low energy (1.4 keV) electrons, at a current density of a fraction of a milliampere per square centimeter, by about two orders of magnitude. This process, which does not work for gallium, may involve modification of the adsorbed precursor state.

2.7.4 Comparison of Doping Techniques

We have described three different doping techniques that can be used in conjunction with silicon MBE. Doping the films is surely the leverage of silicon MBE homoepitaxy, and great attention must be paid to the technique chosen. The advantages and disadvantages of the different techniques are summarized in Table 2.

2.8 DEFECTS AND QUALITY OF SILICON FILMS GROWN BY MBE

Beyond doubt, the success of any epitaxial technique hinges on the quality of the grown films. The defects that are of concern in epitaxial films depend on the applications involved. As long as no defects that

TABLE 2. Comparison of Different Doping Techniques

Consideration	Spontaneous incorporation	Low-energy implantation	Secondary implantation	Electron enhanced
Complexity and cost	Simple, inexpensive	Very complex, expensive	Intermediate, inexpensive	Moderate
Control and reproducibility	Moderate to good	Excellent	Difficult, depends on system variables and growth conditions	Difficult, depends on system variables and growth conditions
Substrate temperature dependence	Highly dependent	Relatively less dependent	Less dependent	Highly dependent
Sharp profile control by	Adlayer concentration	Ion current and temperature	Adlayer concentration, silicon ion current, and substrate potential	Adlayer concentration, electron current, and substrate potential
High levels	Difficult	Possible	Possible	Possible
Crystal quality	Good at low to moderate doping; may degrade at high levels	Good at high growth temperatures; depends on species	Similar to spontaneous	Similar to spontaneous
Remarks	Demonstrated for Sb, Ga, B, Al	Demonstrated for Sb, As, B, Ga	Only Sb	Only Sb

degrade the performance and reliability of the device exist in the active layers of the film, the processes that cause these defects can be tolerated. Silicon technology uses several processes that cause defects to be generated. Ion implantation, for example, produces several defects that persist even after annealing at high temperature (Mader, 1984). The processes are, tailored however, so that these residual defects are far from the *p-n* junctions or from other interfaces of interest. Some defects are purposely introduced, such as ion-implantation-induced gettering sites, to cause defect precipitation at sites where they will be ineffective in damaging device performance.

Thermodynamic considerations require that there be a certain concentration of point defects in a crystal (Rack and Newman, 1977). Generally when dispersed, these point defects, which may include vacancies and interstitials, are required for material processes such as diffusion (Car *et al.*, 1985) and electronic processes such as recombination (Sah and Shockley, 1958) to occur. It is possible to create such defects well above their

equilibrium concentration during growth or ion implantation, for example. At fairly moderate temperatures, these point defects are considerably mobile and may coalesce (Watkins, 1965) to form less mobile extended defects, which can be a serious concern. In conventional processing however, we have the freedom to elevate the sample temperature to at least 900°C after the damage introduction has been done. Very often the temperature is in excess of this. At these temperatures, even extended defects may be annihilated, or at least denuded, from the active device areas.

In silicon MBE, however, we cannot afford the luxury of such high-temperature treatment after the film layers are grown. This is because the advantages of low-temperature MBE processing would be lost in the event of subsequent high-temperature treatment. This means that defects introduced during the growth process may not be annealed out in subsequent processing. Hence, it is doubly imperative that minimal defects are introduced during the MBE growth process as well as in subsequent processing.

Where are defects introduced in the MBE growth process? There are two sources: one, is the substrate. We know that it is very likely that extended defects present in the substrate penetrate into the growing film. The other, of course, is the process of cleaning and growth. High-quality substrates are now routinely available. In fact so-called denuded zone samples (Borland *et al.*, 1984) are also available, which have several micrometers of material near the surface free of defects. So, with proper choice of substrate material, this source of defects can be minimized. As far as MBE process-induced defects are concerned we can only emphasize that diligence in substrate preparation, growth monitoring, and system maintenance are essential. Substrate preparation has already been discussed. To emphasize, correlations have been found between surface contaminants and defect densities.

Regarding process control, there are many factors to consider. Temperature uniformity during both the cleaning and growth processes to within a few degrees centigrade are required. It is also important to keep the sample edges free for expansion and contraction. Tight clamping of the sample should be avoided (Sugiura and Yamaguchi, 1981). Another matter of importance is stability of the silicon beam. Effects such as spitting can be avoided by the use of high-quality single-crystal machined slugs and not focusing the power at one point all the time. Spitting causes the ejection of particles from the melt which condense on the surface and create gross defects. Care should also be taken to avoid flaking which can also result in gross effects. The incorporation of such particulates results in associated strain and consequent dislocations. Vacuum quality is also a significant factor. Ota (1983a) has reported that if the vacuum was degenerated during growth we could observe a significant increase in

dislocation density. It is now accepted that base pressures in the low 10^{-9} Pa regime are not the only prerequisite for the growth of high-quality films. It is important to have a low operating pressure as well (Kasper, 1985). Growth should not be started until the pressure surge, caused by the *e*-beam evaporator turning on, falls from the low 10^{-6} Pa regime well into the 10^{-8} Pa range. Obviously excellent noncontaminating pumping is required in these cases. Interruption of growth is also to be avoided. Allen (1985) shows that such interruption causes the surface contamination of carbon and oxygen to increase slowly. Ota (1983) reports that "S" dislocations are formed when growth is interrupted.

When proper precautions have been taken, several workers have reported the growth of virtually defect-free films. Since different authors have different definitions of what constitutes defect-free materials we shall give some examples. Ota reports that, when the growth occurs layer by layer, no dislocations or stacking faults were observed by TEM. This implies dislocation counts that are below $500/\text{cm}^2$. Defect etching studies are described by Ota (1983a), Archer (1982), and the Annual Book of ASTM Standards (1985). These confirm the above results. Furthermore, Ota implies that these dislocations are propagated from the substrate and are not due to the growth process. Stacking fault nucleation is often related to impurity or particle incorporation. Experiments by Ota and arguments by Tan (1985) indicate that oxygen incorporation or oxygen contamination does not necessarily lead to stacking fault generation. Oxygen however is believed to cause the so called S-pits.

Dopant incorporation processes are also liable to increase the defect count in the grown MBE films. In the case of both spontaneous and secondary implantation induced dopant incorporation, the silicon growth occurs in the presence of an adlayer of dopant. This adlayer certainly influences the growth mechanism. It is safe to assume that when the adlayer concentration exceeds a significant fraction of a monolayer, growth will be disturbed. Metzger (1983), as well as others show that there is a significant deterioration of crystal quality when antimony coverage is about one-tenth of a monolayer.

Aizaki *et al.* (1985) report stacking fault and dislocation densities of a few hundred per cm^2 on (111) oriented films. Generally, (111) orientations tend to have a higher defect density compared to (100) or (110) orientations. They attribute the improvement to the use partially ionized antimony as the dopant. Kasper and Worner (1984) indicate that impurities such as methane in the system cause defect densities up to $4 \times 10^7 \text{ cm}^{-2}$. Nevertheless, a low enough defect density in order get high yield (>50%) is indicated even for medium-scale IC fabrication using MBE films. This implies virtually defect-free films. The use of low-energy ion-implanted

dopants adds a new dimension to defects caused by the doping process. However, not much has been published in this area.

Electrical characterization of films is also done routinely. Almost every group has reported majority carrier mobilities close to bulk values in grown films at least at low to moderate doping levels. Figure 42 shows the relationship of resistivity and doping level for both gallium and antimony doped films. This indicates almost bulk mobility at even higher doping levels. Metzger's (1983) data indicates that at high doping levels there is a deterioration of mobility below bulk values. This is believed to result from excessive antimony coverage required at these levels, which may cause departure from the two-dimensional growth mode to one of three-dimensional nucleation.

Minority carrier lifetimes have been measured by different groups. These results generally correlate well with the structural perfection of the films and the mobility. Minority carrier lifetimes of up to 70 μ sec have been reported (Bean, 1981b). Ota (1983a) reports that his carrier lifetimes are comparable to those in CVD grown films.

Deep-level traps have also been analyzed. Generally the kind of traps observed are highly system dependent. For example, Ota reports no significant deep-level traps. Xie *et al.* (1985), however, show that there is a correlation of traps observed with the cleaning technique employed. Their observation using trap profiling techniques is that a level at 0.58 eV below the conduction band is consistently observed and is related to carbon buildup during growth interruption as well as carbon residues at the inter-

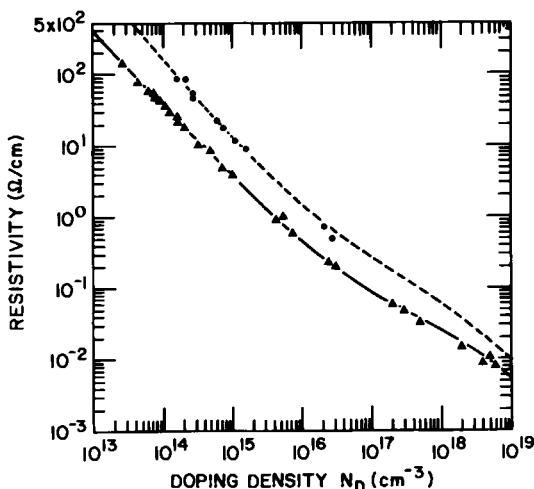


FIG. 42. Resistivity for gallium (●) and antimony (▲) doped films. The curves represent the so-called bulk mobility. [From Swartz *et al.* (1981). Copyright © 1981 IEEE.]

face. The cross section for this trap level is $6.6 \times 10^{-2} \text{ cm}^2$. Sandhu *et al.* (1985) have attempted to identify trap levels associated with metallic impurities such as contamination from stainless steel parts. Their observation is that all such metallic contamination of the films was below $1 \times 10^{11} \text{ cm}^{-3}$.

Robbins *et al.* (1985) have reported on the use of photoluminescence (PL) spectroscopy to study defects in MBE grown films. They show that for films grown between 625 and 750°C luminescence bands D1(0.805 eV), D2(0.870 eV), D3(0.930 eV), and D4(0.990 eV) were observed. These are attributable to radiative recombination at dislocations and correlate well with TEM micrographs which show dislocations. No dislocations were observed in films grown at 850°C either by TEM or indirectly through PL.

Defect characterization is an important aspect of silicon MBE studies and significant effort has been directed towards identifying defects, generation mechanisms, role in device performance as well as devising preventive measures. A wide body of literature exists in these areas. Generally, it is observed from these publications that initially films with high defect levels are grown. However a gradual refinement of cleaning and growth techniques, system design, wafer handling, and system maintenance have in most cases led to lowering of these levels considerably. The use of clean room techniques as practiced by the silicon industry and a greater attention to detail will no doubt further improve film quality.

2.9 APPLICATIONS

Shallow junctions and sharper doping profiles will play a pivotal role in the development of future electronic device technology. The trend to miniaturization both in MOS (Dennard *et al.*, 1979) and bipolar circuits (Ning *et al.*, 1980) requires scaling of both the horizontal and vertical dimensions of the device. While the former is possible using advanced lithographic techniques the latter is possible only by a combination of innovative process steps that minimize the thermal budget of the wafers. For the most part this means lower-temperature processing. It is in this area that MBE will play a very important role and where it can influence mainstream silicon VLSI. The other area of demonstrated leverage is in the area of high-frequency discrete devices. These include microwave oscillators, such as IMPATTs (IMPact ionization Transit Time) and TUNNETTs (TUNNEling Transit Time) as well as high frequency switching devices such *p-i-n* diodes, and analog devices such as varactors. In addition, there are specialized applications, such as the doping superlattices, which are possible only by MBE. We will discuss some of these

applications and show that MBE is capable of producing device-quality materials for these specialized applications and also outline the problems associated with integration of MBE in other applications. Applications conveniently fall into two categories: discrete devices and integrated circuits. Since MBE is physical deposition, blanket deposition of films is easy to accomplish. Patterning presents greater difficulties. Thus, most of the successes of MBE have been in the area of discrete devices, though the advantages of reduced thermal cycle have also been demonstrated using MBE material.

2.9.1 Discrete Devices

A variety of two-terminal devices have been fabricated by MBE. Most of these are diode structures with very demanding profile requirements for high-frequency applications. Straightforward $p-n$ junctions of varying doping levels on either side of the junction are fabricated regularly for routine material characterization. Even unpassivated mesa etched junctions (which tend to exhibit high surface leakage) have leakage currents below 10^{-9} A/cm² (Becker and Bean, 1977). The actual leakage is determined by the growth procedure and doping level near the junction. At higher doping levels, reverse leakage is dominated by tunneling as verified by the temperature characteristics (Iyer, 1981) and soft breakdown characteristics. At low doping levels breakdown voltages in excess of 80 V are obtained.

At AT&T Bell Laboratories, there have been several reports on the fabrication and operation of such devices. Ota *et al.* (1977) have reported a $p-i-n$ switching diode for use in the 40–110-GHz range. The critical requirement in this application is the abrupt transition from the highly doped substrate to the i layer. This transition was achieved by MBE. The reverse leakage was less than 2×10^{-9} A/cm². The fall time was 0.3 nsec, and the return loss was 0.95 dB at 55 GHz. The breakdown voltage was greater than 30 V. It is important to mention that this MBE-fabricated diode was superior to the conventionally fabricated devices. A similar concept was also used to fabricate a microwave diode for use in modulation applications (Ota, 1983a). The profile generated has an abrupt transition from the n^+ substrate and a tailored profile with a peak at the desired junction depth. This was followed by a boron implant to increase the surface concentration beyond that achievable by MBE alone. The active epi thickness was about 1 μm . This design showed the desired frequency characteristics and also a lower value of rf series resistance. In a similar vein, Bean (1981b), has reported a Schottky varactor with an $x^{-1.5}$ doping dependence. This was shown to yield a linear frequency–voltage charac-

teristic when incorporated as the capacitor element of a tank circuit. Ballamy and Ota (1981) have reported a low-barrier Schottky mixer diode for microwave applications. The doping profile consists of a 15-nm wide arsenic spike at the surface with a level of $8 \times 10^{18} \text{ cm}^{-3}$, followed by a 100-nm flat region doped at $8 \times 10^{16} \text{ cm}^{-3}$, followed by a highly doped substrate contact layer. Titanium-based metallurgy was used. The ability to place a dopant spike at the surface allowed for a low barrier to the metal. Moreover, reduction of the epi layer thickness also contributed to a lowering of the series resistance.

Luy *et al.* (1985) have reported on the operation of a W band IMPATT diode made from MBE material. The important consideration in IMPATT design is once again, precise control of the drift region. This means that the highly doped region, where the avalanching process occurs, must be well delineated from the lower-doped drift region. Furthermore, the avalanche region must be localized to minimize the differences in the drift distance for carriers generated at different points. At higher frequencies, the drift regions are quite short (several thousand angstroms) so that conventional diffusion processes to form the avalanching *p*-*n* junction are difficult to implement. For a 90-GHz device, the heavily doped avalanche region is 0.06 μm and the flat drift region is 0.3 μm long. The doping profile measured by spreading resistance and C-V techniques is shown in Fig. 43. The precise transitions are obtained using the buildup technique described earlier. The *p*⁺ layer of the junction was done by shallow boron diffusion or by MBE, although the former was preferred because of higher doping level achieved and the resulting lower series and contact resistance. The power and efficiency characteristics are shown in Fig. 44. Up to 250-mW average output power at 5.8% efficiency was obtained. In fact, AEG-Telefunken uses the silicon MBE process to fabricate such devices on a small manufacturing scale (part number Sn2Q1). This is the first commercial exploitation of the process and demonstrates that silicon MBE is no longer merely a research technique but offers high yields in a specialized manufacturing application.

At even higher frequencies, TUNNET devices have been proposed for microwave oscillator applications. Here, carrier injection into the drift region is accomplished by tunneling rather than avalanching. Tunneling is a quieter process and is also instantaneous. However, implementation of a tunneling junction in silicon requires a highly doped junction, one side of which must be extremely narrow (<200 Å) to ensure a reasonable tunneling current. Such profiles have been demonstrated (Iyer *et al.*, 1981) as shown in Fig. 32.

Katayama *et al.* (1979) demonstrated that silicon MBE films could be used to fabricate MOS transistors. The device structure is shown in Fig.

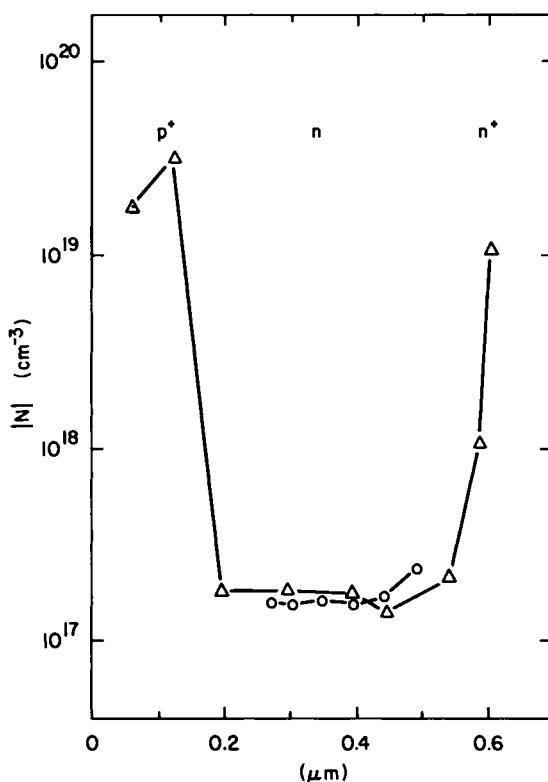


FIG. 43. Measured doping profile for 90-GHz IMPATT diode: Δ , spreading resistance method; \circ , C-V method). [From Luy *et al.* (1985).]

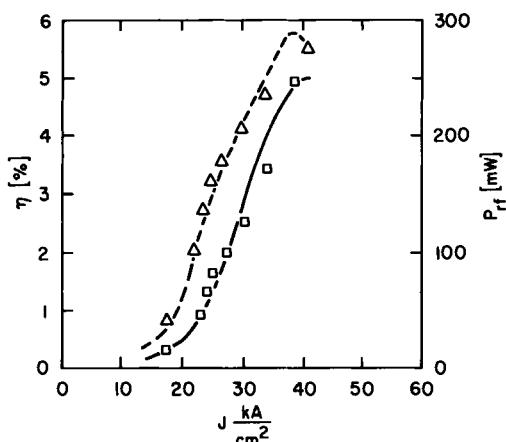


FIG. 44. Efficiency (Δ) and rf power output (\square) obtained from an MBE fabricated IMPATT diode. [From Luy *et al.* (1985).]

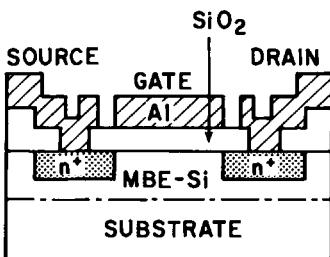


FIG. 45. Device structure of a MOSFET fabricated in MBE-grown film. [From Katayama *et al.* (1979).]

45 and consists of an *n*-epi layer doped unintentionally to $10^{15}/\text{cm}^3$ grown on a boron-doped ($1 \times 10^{15} \text{ cm}^{-3}$) (100) substrate. The structure was then oxidized thermally without any surface treatment such as a preoxidation etch to 150 nm and this was followed by source and drain formation by ion diffusion. An aluminum film was then deposited and patterned to form the gate and contacts. The resulting structure operated in the depletion mode and the characteristics are shown in Fig. 46. An effective mobility in the channel of $1050 \text{ cm}^2/\text{V sec}$ was deduced which was significantly higher than the $800-\text{cm}^2/\text{V sec}$ value obtained for conventionally processed MOSFETs, measured at a gate voltage of 1 V. The channel length was $20 \mu\text{m}$. It is claimed that the enhancement results from the absence of ion implantation damage in the MBE FET, but the reduced surface scattering in the channel because of the atomically smoother oxide silicon interface when

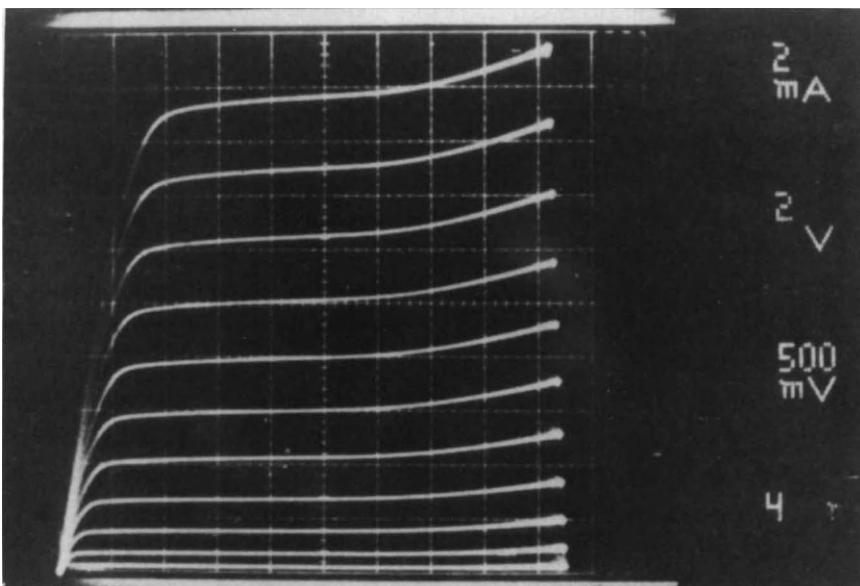


FIG. 46. Device characteristics of an MBE MOSFET. [From Katayama *et al.* (1979).]

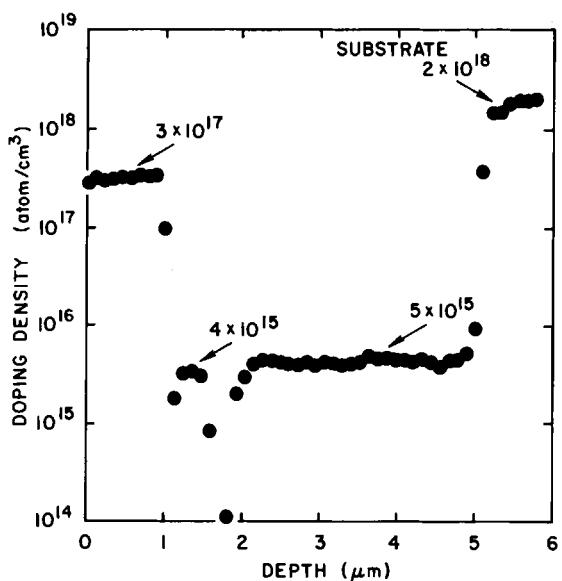


FIG. 47. Measured doping profile for MBE uncompensated bipolar transistor structure. [From Swartz *et al.* (1981). Copyright © 1981 IEEE.]

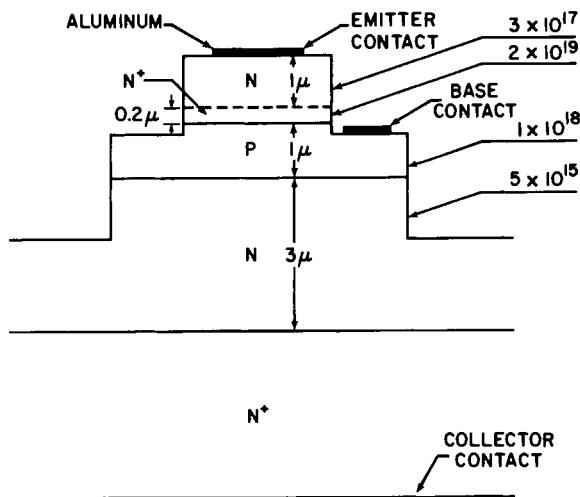


FIG. 48. Schematic of mesa-etched bipolar structure grown by MBE. [From Swartz *et al.* (1981). Copyright © 1981 IEEE.]

the oxide is grown on the intrinsically smoother and cleaner MBE surface could also contribute.

Swartz *et al.* (1981) have reported a bipolar transistor fabricated entirely in MBE material using the doping capabilities to define the junctions. Doping was done by simultaneous ion implantation of BF_2^+ and As^+ for *n* and *p* layers, respectively. The doping profile measured is shown in Fig. 47, and a schematic of the mesa-defined structure is shown in Fig. 48. The base width of 1 μm is rather large but limited by the contacting scheme they employed and not by the MBE process. The characteristics of this device are shown in Fig. 49. A maximum forward current gain of 60 was measured at a collector current of 10 mA and a collector-emitter voltage of 5 V. The collector-emitter breakdown voltage with the base open was 6 V. There was significant leakage current probably caused by defects and the exposed junction due to the mesa etching employed. One more feature of this process is the ability to have all the layers grown uncompensated.

Streit and Allen (1984) have reported a triangular-barrier silicon diode. The device structure, profile, and energy band at zero bias are shown in Fig. 50a. It consists of a *p*-type spike (about 50 Å wide) doped at $3-5 \times 10^{18} \text{ cm}^{-3}$ in an essentially intrinsic matrix, with *n*⁺ terminating contacts. The device characteristics are shown in Fig. 50b. Such a majority carrier device can be designed, by appropriate placement of the spike, to have

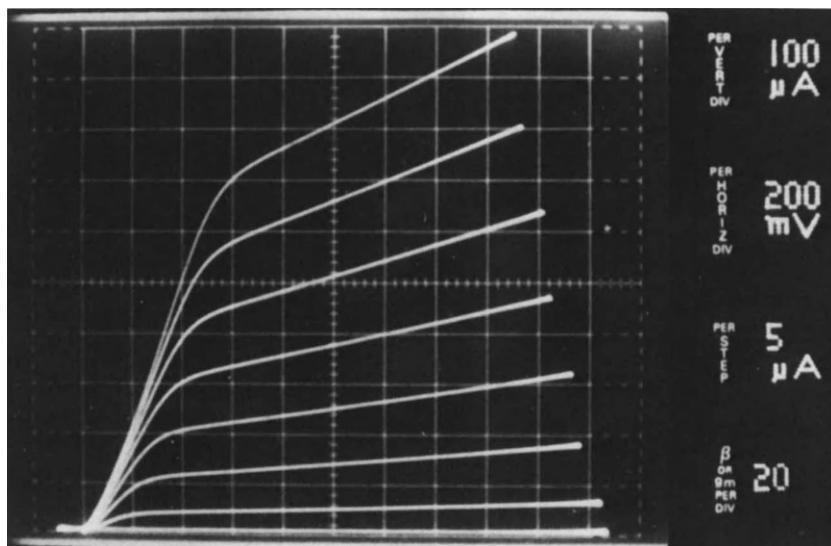


FIG. 49. Device characteristics of MBE bipolar transistor. [From Swartz *et al.* (1981). Copyright © 1981 IEEE.]

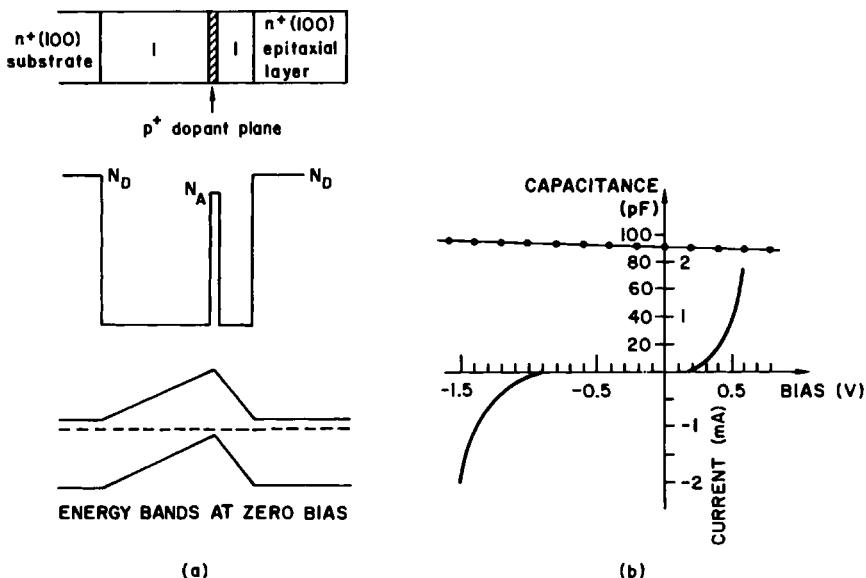


FIG. 50. (a) Device structure, doping profile, and zero bias energy diagram for a triangular barrier diode. (b) $C-V$ and $I-V$ characteristics of the device. [From Streit and Allen (1984). Copyright © 1981 IEEE.]

tailored asymmetric $I-V$ characteristics. These structures have applications in subharmonic mixers, barrier transit time (BARRITT) devices, high-speed photo detectors, and many other similar devices (Allen, 1985).

MBE films have also been used as the starting layer for IC technology much the same way as conventional CVD films are employed. In these applications, leverage is obtained by reducing the epitaxial layer thickness. As before, thinning is possible because of reduced smearing from a highly doped substrate. In fact, Kasper and Worner (1985) have demonstrated such an application in a frequency divider circuit for European television applications. A commercial process line is used to manufacture these chips in small production quantities. This chip used 2- μm design rules. They report being able to reduce the epitaxial layer thickness from 2.5 to 0.9 μm . The thinner epitaxial layer permitted the use of oxide isolation instead of diffused $p-n$ junction isolation, and as a result they were able to get an upper frequency limit (f_t) of 7 GHz as compared to 5 GHz in the conventionally processed devices. Frequency divider ICs with clock frequencies up to 2.8 GHz were fabricated. Swartz *et al.* (1984) have fabricated an NMOS ring oscillator on epitaxial layers grown by MBE. In devices with channel lengths of 96 μm , widths of 96 μm , and gate oxide 100 nm thick, low-field mobility of over 1200 $\text{cm}^2/\text{V sec}$ was measured. The control

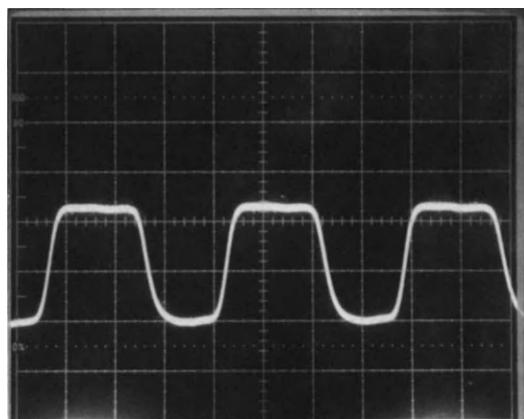


FIG. 51. Output of 17-stage ring oscillator; 0- and 5-V supply voltages were used. Vertical scale is 2 V/div. Horizontal scale is 20 nsec/div. [From Swartz *et al.* (1984). Copyright © 1984 IEEE.]

devices fabricated in bulk silicon had mobilities of about $850 \text{ cm}^2/\text{V sec}$. Inverter structures, simple logic gates and a 17-stage ring oscillator, whose characteristics are shown in Fig. 51, were also fabricated. The delay per stage was 2 nsec as compared with 1.2 nsec for the control. This was attributed to the more positive threshold on the MBE device.

2.9.2 Patterning and Integrated Devices

For successful implementation of silicon MBE into mainstream silicon technology a patterning scheme is required. One of the simplest is via the use of overlaid physical masks, which block out unwanted portions of the beam and allow for deposition in preselected patterns. The technique is often used (Tsang and Illegems, 1977) in III-V MBE to fabricate relatively large structures. The method can be extended to smaller dimensions if the mask is made conformable with the substrate similar to the liftoff structures in widespread use in silicon technology. In such an implementation, a relatively thick oxide layer is grown on the silicon substrate and prepatterned to expose silicon areas. The wafer is then processed by MBE after proper cleaning steps. The temperature of deposition is fixed so that no significant reduction of the oxide occurs. Single-crystal silicon grows on the exposed silicon areas but only polycrystalline silicon grows on the oxide covered areas. Typically this may be expected to happen at temperatures below about 800°C . The polysilicon may then be lifted off by etching the oxide. Cleaning of the exposed silicon areas on the patterned wafer needs special attention. Contamination of these areas from the

surrounding oxide is easily possible especially if sputtering and other beam cleaning techniques are employed. Bean and Rozgonyi (1982) have reported that good-quality patterned films may be grown by this technique if a post-RIE sacrificial oxide layer is grown and the sample is rotated during sputter cleaning. They have demonstrated 500-nm thick lifted-off films with lateral dimensions of less than 1 μm which are essentially defect free. Their results, a sample of which is shown in Fig. 52, indicate that complete and clean liftoff with no faceting is possible under certain conditions.

One of the concerns is the stress at the edge of the patterns which may lead to stacking faults or twins as reported by Kasper and Worner (1985). They also report polysilicon penetration into the single-crystal area resulting in pattern reduction that is much smaller than the film height. Herzog and Kasper (1984) report that the polysilicon on the oxide is under compressive stress, but this has no deleterious effect on the substrate. They have also reported molybdenum Schottky diodes using this material. Needless to say, this method has to be investigated further with respect to leakage currents across junctions made in these patterned layers.

A totally different approach is to tailor the process to MBE. Such an approach recognizes that the best MBE material is that grown on high-quality substrates in a blanket manner. This means that any device isolation will have to be done later. However, any subsequent isolation must be done at lower temperatures typically below 850°C if doping smears are to be restricted to at most a few tens of angstroms. This strategy calls for several complementary technologies such as low-temperature oxidation by plasma techniques (Ray and Riesman, 1981) or high-pressure methods (Katz *et al.*, 1981). In addition, low-temperature passivation schemes will also have to be employed. Such trends are already in place as far as conventional processing is concerned but will have to be pursued more aggressively if silicon MBE is to make an impact on VLSI.

Other isolation schemes have also been proposed. Konaka *et al.* (1982) have suggested a novel scheme. This has been extended by Lin *et al.* (1985) and is outlined in Fig. 53. Here silicon is anodized in an HF-based electrolyte. The simultaneous oxidation and etching action of the bath renders the surface layers porous. The porosity depends on the HF concentration and the current density employed. It is possible to obtain a network of interconnected pores up to a few micrometers beneath the surface. Although porous, the layer retains its crystallinity and can be used to seed an epitaxial silicon layer. Since the porous structure tends to coalesce at high temperatures resulting in voids and ultimately in the collapse of the structure, a low-temperature epitaxial growth technique such as MBE is called for. Generating a clean starting surface is rendered more difficult due to the enhanced impurity trapping in the pores. Beale *et al.* (1985)

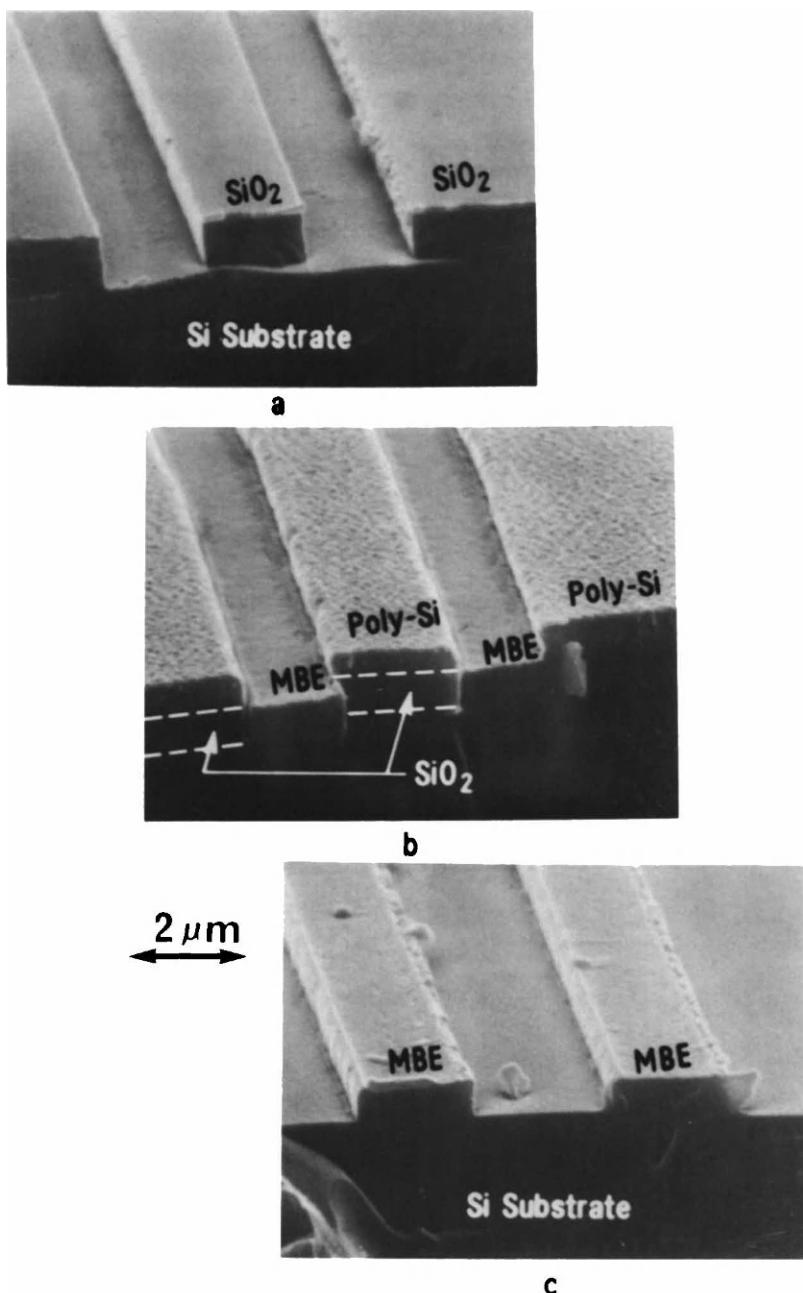


FIG. 52. A lift off generated epitaxial silicon pattern. (a) The pattern showing exposed silicon areas in an oxide covered wafer, (b) after MBE deposition and (c) after lift off. [From Bean and Rozgonyi (1982).]

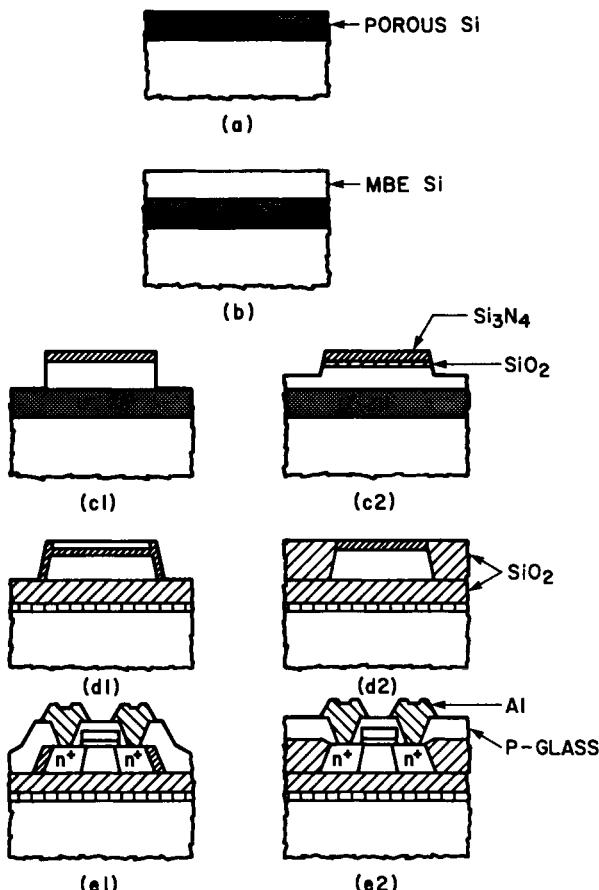


FIG. 53. Schematic of process steps for SOI structure utilizing MBE films on porous silicon. [From Lin *et al.* (1985).]

have used thermal cleaning at 770°C, while Konaka *et al.* report that growth at 770°C requires no special cleaning, presumably because of the cleaning effects of the silicon beam. Lin *et al.* used a silicon beam of flux $7.8 \times 10^{13}/\text{cm}^{-2}$ sec at a substrate temperature of 750°C. Growth commenced at a low rate but after 50 nm was increased to 4 Å/sec. Figure 54 shows a cross-sectional transmission electron micrograph of the porous Si-MBE Si interface. Most of the epi film is defect free but there may be a thin layer (several tens of angstroms thick) that has micro defects at that interface. After MBE growth, a pad oxide is grown and LPCVD nitride is deposited as shown in Fig. 53. Then silicon islands were patterned as shown. The porous silicon is exposed selectively. The structure is then oxidized in steam at 900°C for 4 h. Due to the porosity, the porous layer

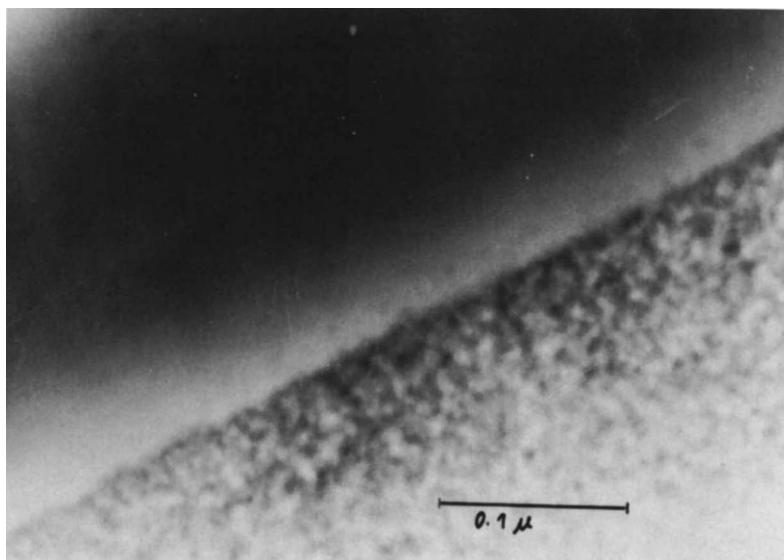


FIG. 54. Cross-sectional transmission electron micrograph showing the interface between the porous silicon and the substrate as well as the overgrown MBE film. The film is essentially defect free except for some possible microdefects at the interface. This region, however, is oxidized. [From Lin *et al.* (1985).]

may oxidize up to 100 times faster than the single-crystal silicon resulting in complete isolation of the patterned epitaxial islands. The structure after this oxidation is shown in Fig. 55. Note that the interface is completely oxidized by this method. A 100- μm wide island was successfully isolated by this technique. *N*-Channel MOSFETs were fabricated in the isolated islands. These results are quite encouraging, but the process needs further optimization and is being investigated by several groups.

2.9.3 Other Devices

In addition, there are several other novel applications of silicon MBE which exploit the sharp doping transition capability of the method. Notable among these is the doping superlattice (Dohler, 1972). This is a periodic structure consisting of alternating *n* and *p* layers with intrinsic layers optionally inserted in between, as shown in Fig. 56. Such structures have been fabricated in other semiconductors and have been shown to have special properties (Ploog *et al.* 1981). A unique property of such structures is the physical separation of the conduction band minima and valence band maxima in real space. This indirect gap in real space results in reduced

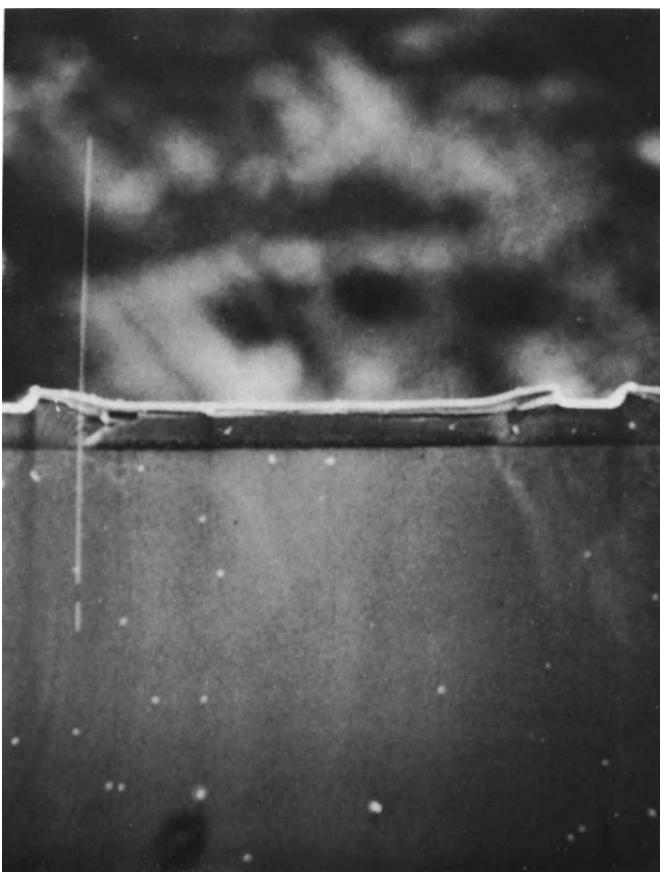


FIG. 55. Cross-sectional scanning electron micrograph showing isolated silicon island after oxidation of porous silicon. The width of the island is 100 μm . [From Lin *et al.* (1985).]

recombination of carriers and consequently greatly enhanced lifetimes for excited carriers. Moreover, these lifetimes may be tailored by design of the doping superlattice from a few milliseconds up to a few hours. The electronic properties, such as the available free carriers and the effective band gap (measured from the conduction band minimum to the valence band maximum), are all electronically tunable over a wide range. The advantage of these $n-i-p-i$ crystals is that they are homoepitaxial structures and thus are not subject to interfacial mismatch problems that may occur in heterostructure superlattices, which may also be designed for similar properties. In addition, we will expect subband structures if the layers are thin enough. Enhanced mobility effects similar to those seen in modulation-doped FETs (also called HEMTs) (Solomon and Markoc,

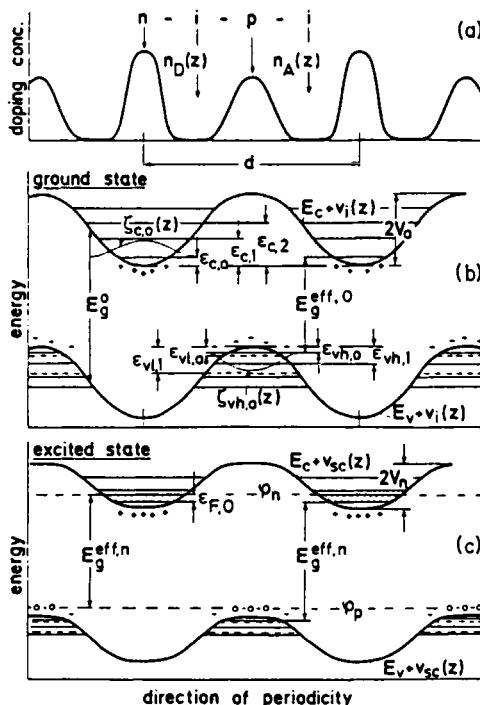


FIG. 56. (a) Doping profile of a $n-i-p-i$ structure. (b) Energy diagram in equilibrium. (c) Energy diagram when excited. [From Dohler and Ploog (1985).]

1983) are also to be expected and have been reported in silicon by Nakagawa and Shiraki (1985). In order to realize these properties, however, the super lattice period must be quite small, typically a few tens of nanometers with doping levels of the order of 10^{18} cm^{-3} . Moreover, many periods are required for real impact of these properties. Silicon MBE offers a fabrication technique for such structures in silicon.

In addition to these there are several other devices that make use of epitaxial silicides, alloy semiconductors containing silicon, etc., which exhibit interesting characteristics. These devices, however, are beyond the scope of this book. The reader is referred to the book on silicon MBE edited by Kasper and Bean (1986) for such applications.

2.10 FUTURE OF SILICON MBE

Silicon MBE promises to be a very exciting field in the coming years. The field is now quite wide as can be seen from attendance at silicon MBE conferences. The trend to higher performance and novel devices that use both silicon homoepitaxy and heteroepitaxy of metals, insulators, and

other semiconductors will only heighten this interest. The controlled environment of MBE provides for studying special material properties and also intricate process science; but this is not all. This understanding has already led to several important and commercially exploited applications as well.

Several more breakthroughs are necessary, however, before the MBE machine is just another tool in the silicon processing facility. Notable among these are, the development of process integration schemes, as well as efficient low-temperature methods to clean the surface and the ability to resume MBE steps after other intermediary processing is done.

Some system design issues also have to be clarified. For example, do we go to high capacity, i.e multiwafer, batch process systems, or do we concentrate on fast-turn-around single-wafer systems? Batch processing requires large platens for multiwafer handling, with the associated problems of platen transport and handling, wafer heating and uniformity of temperature and deposition. The large amount of heat developed requires large chamber sizes to keep the vacuum from degrading due to heating of walls. Single-wafer processing, is attractive for the absence of these problems and the fact that many semiconductor tools are run one wafer at a time, especially for large-diameter wafers. Nevertheless, wafer handling and heat dissipation are important issues. Another issue is the generation of particulates within the system. These issues are gaining more prominence as MBE workers move their equipment into clean room environments.

In summary, silicon MBE offers part of the solution that faces the semiconductor community today. It has certainly extended the capabilities of silicon technology and promises several new device structures in the near future.

ACKNOWLEDGEMENTS

Useful discussions with fellow workers in the field, especially Prof. F. G. Allen and Dr. R. A. Metzger are acknowledged with pleasure.

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3

SILICON LIQUID-PHASE EPITAXY

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3.1 INTRODUCTION

The chemical vapor deposition (CVD) of epitaxial layers of silicon has been extensively studied. In contrast, less work has been reported on the epitaxial growth of silicon films from the liquid phase. The growth of layers from the liquid phase has the advantage of requiring lower temperatures as compared to vapor-phase epitaxial growth. This is important in the fabrication of silicon devices because it minimizes the changes in prediffused regions during epitaxial growth and allows the growth of an abrupt interface between the epitaxial layer and the substrate. In addition, most metallic impurities are expected to have segregation coefficients of less than unity. Consequently, the growth of layers from the liquid phase can be expected to result in a low concentration of such impurities in the epitaxial films. This is desirable for the fabrication of devices requiring high minority carrier lifetime for achieving good device characteristics. This chapter reviews the development of a silicon liquid-phase epitaxial (LPE) growth process and its application to devices.

3.2 HISTORICAL PERSPECTIVE

The growth of epitaxial layers of silicon from the liquid phase can be traced back to the early 1950s (Wartenberg, 1951; Keck and Broder, 1953; Goss, 1953). In these early experiments, the silicon was dissolved in a

variety of solvents, such as aluminum, indium, gallium, silver, and zinc. It was reported that single-crystal silicon could be grown when a seed was introduced into the solution and its temperature lowered to produce supersaturation. This early work was aimed at the growth of bulk silicon ingots rather than epitaxial layers, but the underlying principle of achieving low-temperature nucleation of silicon by using a solvent provided the basis for later work on the growth of epitaxial layers on silicon substrates.

The first successful growth of silicon epitaxial layers from the liquid phase was reported in 1969 (D'Asaro *et al.*, 1969). In this work, the sliding boat technique was used with either tin or tin-lead as a solvent. By using high-resistivity ($>200 \text{ ohm cm}$, *n*-type) silicon to saturate the melt, *n*-type epitaxial layers were obtained with resistivities ranging from 0.2 to 20 ohm cm. The Hall mobility was found to be approximately 70% of the average bulk value. The primary aim of this work was the reduction of interfacial defects. Although the defects in the epitaxial layer were found to be an order of magnitude lower than in the substrate, this approach was not pursued any further.

The sliding boat approach contains several disadvantages, such as problems of melt removal, limited wafer size handling capability, and variability in epitaxial layer quality due to the necessity for changing the melt after each epitaxial growth sequence. The vertical dipping method with the so-called infinite melt eliminates these problems. This method for epitaxial growth was, therefore, adopted by later workers. It was used in 1972 (Kim, 1972) to obtain selective epitaxial growth of highly doped islands of silicon to form ohmic contacts to planar diodes. For this work, a tin-lead solution containing 0.1% gallium was used to form p^+ epitaxial layers. The formation of silicon pedestals was achieved at growth temperatures ranging from 750 to 700°C. Subsequently, this approach was used with a gallium-aluminum melt for the growth of silicon layers for solar cell applications (Girault *et al.*, 1977). The poor quality of these layers dissuaded further pursuit of this technique.

In this chapter, the epitaxial growth of silicon layers from a tin melt, using the vertical dipping method, will be reviewed. This work was undertaken at the General Electric Research and Development Center from 1975 to 1980 with the primary goal of eliminating autodoping during epitaxial growth. During the course of this study, experiments were undertaken to understand the kinetics of the growth and the resulting morphology. In addition, the electrical characteristics of the epitaxial layers were evaluated with the objective of examining the role of tin in the silicon. This technology was also successfully applied to the fabrication of power field controlled devices.

3.3 APPARATUS AND EXPERIMENTAL PROCEDURE

3.3.1 Solvent

All the epitaxial growth discussed in the rest of this chapter was performed using tin as the solvent. As mentioned earlier, other workers have used gallium and aluminum melts for silicon liquid-phase epitaxy. This process is of limited value because the layers are heavily doped *p* type due to a high gallium or aluminum content. For development of the LPE technology discussed here, tin was chosen as a solvent because its incorporation into the silicon during epitaxial growth was not expected to introduce either shallow doping levels or deep lying recombination centers. This was verified experimentally, as discussed later in this chapter. The solubility of silicon in tin at growth temperatures of around 950°C is sufficient to allow the growth of thick layers (up to 100 μm) without serious depletion of the melt. To prepare the melt, high-purity tin (5N purity) was cleaned in the laboratory by repeated heating in a quartz tube under vacuum until the impurities formed a slag on its surface. This was followed by removal of the slag by etching in concentrated hydrochloric acid.

3.3.2 Growth Apparatus

The tin melt was heated to the growth temperature in a quartz crucible with a hydrogen ambient. The epitaxial reactor, as illustrated in Fig. 1, consisted of a quartz tube with a gate valve on top connecting the tube to a stainless steel baffle chamber. The melt was always maintained in a

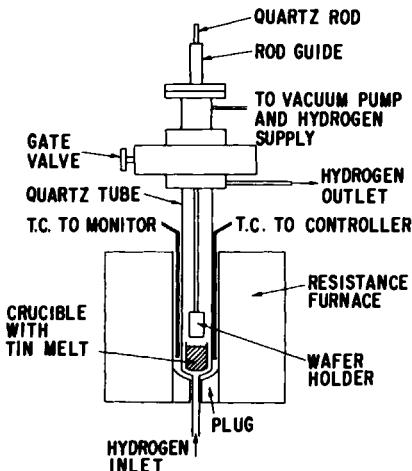


FIG. 1. Liquid-phase epitaxial growth system using the infinite melt approach. [From Baliga (1977a). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

stream of hydrogen flowing from the bottom of the tube towards the top. This hydrogen was purified using a palladium diffuser to minimize oxygen contamination. The temperature of the melt was maintained to within $\pm 1^\circ\text{C}$ using a controller with a Pt/Pt-Rd thermocouple to control the power fed to the furnace elements. The temperature of the melt was monitored by using another Pt/Pt-Rd thermocouple placed outside the quartz tube and positioned at the center of the crucible as shown in Fig. 1. The emf of this external monitor thermocouple was calibrated to the melt temperature by inserting a Pt/Pt-Rd thermocouple held within a quartz tube into the melt prior to performing the epitaxial growth experiments and maintaining the melt at various temperatures.

3.3.3 Growth Procedure

The substrates and saturation wafers were inserted into the melt using quartz holders with a graphite bolt and nut assembly, which held the wafer between quartz surfaces. The quartz holder was first inserted into the rod guide and the flange bolted to the baffle chamber to form a vacuum tight fit with an O-ring. The baffle chamber was then evacuated and backfilled with hydrogen several times to eliminate oxygen contamination. The gate valve was then opened to allow lowering of the holder into the melt.

Prior to each growth, the melt was saturated using a thick silicon wafer. For the growth of lightly doped epitaxial layers, 100-ohm cm, phosphorous-doped silicon wafers were used for saturation. For the growth of heavily doped *p*-type layers, 0.01-ohm cm, boron-doped silicon wafers were used for saturation. During saturation the melt was stirred by oscillation of the quartz holder about a vertical axis. The saturation was conducted until no further loss in the weight of the saturation wafer could be detected. It was observed that 0.47 g of silicon were required to saturate a fresh 99-g tin melt at 950°C . This is in good agreement with the 2 at.% solubility of silicon in tin at this temperature (Thurmond and Kowalchik, 1960). After each epitaxial growth, the silicon in the melt was replenished using the same procedure. The tin melt itself could be used repeatedly for at least 50 growth sequences.

The epitaxial layers were grown on a variety of (111)-oriented silicon substrates. The growth was conducted on the polished face of the wafers as received from the vendor. The wafers were degreased and given a dip in hydrofluoric acid just before loading into the reactor. The substrate temperature was brought up to the melt temperature by holding the wafer above the melt for 10 min. The wafer was then inserted into the melt, and the temperature of the melt lowered at known cooling rates ranging from 0.2 to $7^\circ\text{C}/\text{min}$. The fastest cooling rate of $7^\circ\text{C}/\text{min}$ was achieved by turning

off the power to the furnace for the duration of the growth. The growths reported in this study were conducted with and without supersaturation of the melt, i.e., the melt was either saturated at the temperature at which the substrate wafer was introduced into the melt or at a higher temperature to obtain supersaturation. Growth times ranging from a few minutes up to several hours were used, depending upon the supersaturation and the cooling rate. In all cases, the epitaxial growth was initiated at 950°C. After the growth period, the substrate was first removed from the melt, and then the furnace cooling was terminated to avoid any possible meltback effects. Some tin was usually found to be present on the bottom edge of the wafer after growth. This tin was removed by etching in aqua regia.

To allow determination of layer thickness for measurement of growth rate, *n*-type layers were grown on *p*-type substrates. The epitaxial layers were then defined by angle lapping and delineating the junction with a copper sulfate solution. The epitaxial layer thickness was measured using an interferometer to within $\pm 0.2 \mu\text{m}$. In the absence of stirring during epitaxial growth, the thickness was found to vary by less than $\pm 10\%$ over the entire wafer. With stirring, the layer thickness was found to vary radially from the axis of rotation, as discussed later.

3.4 GROWTH KINETICS AND LAYER MORPHOLOGY

The growth of epitaxial layers from the liquid phase is based on the principle of precipitation of silicon dissolved in a melt onto a single-crystal substrate. To achieve the precipitation of the silicon, the melt must be supersaturated during epitaxial growth. The supersaturation of the melt is created by utilizing the change in the solubility of silicon in the solvent with temperature. In the case of tin as the solvent, the solubility decreases with decreasing temperature. Consequently, epitaxial growth can be achieved either by lowering the temperature during epitaxial growth (called growth with undercooling) or by lowering the temperature of the melt after saturation to create the desired supersaturation and then maintaining a constant melt temperature (called isothermal growth).

3.4.1 Growth Kinetics with Undercooling

The variation of the epitaxial layer thickness as a function of both the cooling rate and the time duration of the growth has been studied (Baliga, 1977a). The five cooling rates that were used in this study were 0.2, 0.5, 0.75, 2.5, and 7°C/min. Under the slowest cooling condition (0.2°C/min), the cooling rate was found to vary from run to run, ranging from 0.165 to 0.25°C/min. In all cases, the layer thickness was found to increase linearly

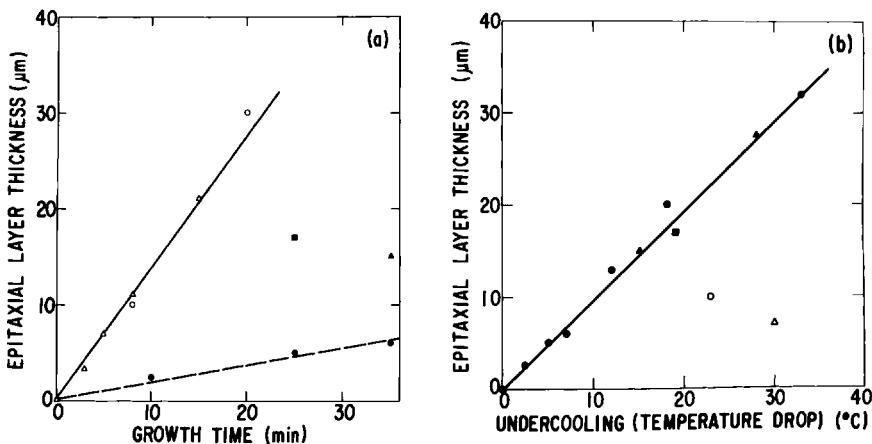


FIG. 2. (a) Linear increase in epitaxial layer thickness with growth time for all cooling rates. Note that, at the higher cooling rates, all the data points fall on the same line. (b) Linear relationship between the epitaxial layer thickness and the total undercooling during growth at slow cooling rates. Cooling rates: ●, 0.2°C/min; ▲, 0.5°C/min; ■, 0.75°C/min; ○, 2.5°C/min; △, 7.0°C/min. [From Baliga (1977a). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

with growth time at each cooling rate, as illustrated in Fig. 2, allowing the definition of a fixed growth rate corresponding to each cooling rate. It was also observed that this growth rate increases with increasing cooling rate until a cooling rate of 2.5°C/min is reached, beyond which no further increase in growth rate occurs. Furthermore, it was observed that the epitaxial layer thickness grown for any specific temperature drop during growth remains independent of the cooling rate, as long as the cooling rate is less than 1°C/min. This can be seen from Fig. 2b. Thus, at the low cooling rates the same layer thickness is obtained per degree Centigrade of temperature drop. At cooling rates above 1°C/min, this phenomenon is no longer observed indicating a change in growth kinetics.

The mechanisms that control the growth rate during flux growth have been reviewed by Elwell (1975) and discussed in more detail by Scheel and Elwell (1973) and by Gilmer *et al.* (1971). The process of crystal growth from solution may be treated as a combination of the following steps: (1) transport of silicon atoms from the bulk solution by diffusion, convection, or forced flow; (2) volume diffusion through a boundary layer; (3) absorption on the crystal surface; (4) surface diffusion to a step; (5) attachment at a step; (6) diffusion along the step; and (7) integration into the crystal at a kink in the step. The first two steps in the process are regarded as mass-transport processes, while the remaining steps are governed by surface kinetic mechanisms. If the surface kinetic mechanisms are rapid compared with

the mass-transport flow, the growth rate will become mass-transport limited. Liquid-phase epitaxial growth generally occurs under these conditions. In this case, if a linear gradient of solute is considered to exist over a boundary layer thickness δ normal to the surface, the growth rate is given by (Elwell, 1975)

$$v = D\sigma\eta_e/\phi\delta \quad (3.1)$$

where D is the solute effective diffusion coefficient, ϕ the density of the crystal, η_e the equilibrium solute concentration, and σ the supersaturation. For the case of a linear dependence of solute solubility on temperature [this is indeed true for the case of silicon dissolved in tin over a temperature range of 800 to 950°C, under which the growths in this study were conducted (Thurmond and Kowalchik, 1960)] and a constant cooling rate C , the growth rate is given by

$$v = DkC/\phi\delta \quad (3.2)$$

where k is a proportionality constant. From this equation, it can be concluded that the growth velocity or thickness grown per unit time v will be proportional to the temperature drop per unit time or the cooling rate C . In other words, the epitaxial layer thickness will be proportional to the temperature drop. Thus, at low cooling rates, when the surface kinetics are rapid compared with mass transport, the epitaxial layer thickness will vary in proportion to the temperature drop, irrespective of the cooling rate. This is consistent with the experimental results obtained for cooling rates for 0.2, 0.5, and 0.75°C/min, as shown in Fig. 2. Similar results have been observed in the case of the growth of GaAs by Mitsuhashi (1970).

With increasing cooling rates, the mass transport rate will increase and can be expected eventually to exceed the surface-kinetic-limited growth rate. Once the growth rate becomes kinetically controlled, the epitaxial layer thickness should become proportional to the time duration of the growth, irrespective of the cooling rate. This phenomenon, however, has not been observed during the growth of III-V or II-VI compounds from the liquid phase. It has been observed in the case of silicon LPE growth in this study at cooling rates of 2.5 and 7°C/min. Thus, it can be expected that, as the cooling rates increase, the growth rate will increase in proportion to the cooling rate, as long as the growth rate is mass-transport limited, and then becomes independent of cooling rate once the growth rate becomes limited by surface kinetics. This behavior is observed in the silicon liquid-phase epitaxial process used in this study, as shown in Fig. 3. In Fig. 3 it can be seen that up to cooling rates of 1°C/min, the growth of the silicon epitaxial layers in this study occurred under mass-transport-limited conditions, while growth at cooling rates above 2°C/min occurred under

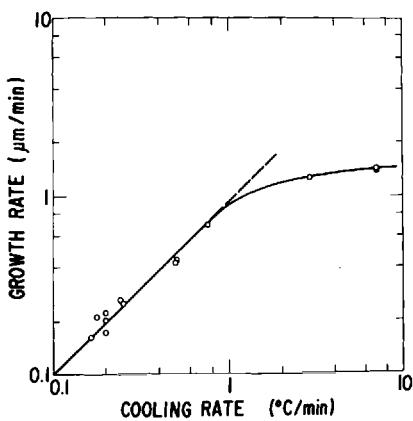


FIG. 3. Variation of the growth rate with cooling rate. Note the saturation in the growth rate observed at high cooling rates. [From Baliga (1977a). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

kinetically controlled conditions. The cooling rate at which this transition occurs is a function of the size and geometry of the crucible, as well as the substrate holder.

The unusual transition from mass-transport-limited growth to kinetically controlled growth in the case of silicon LPE was confirmed by examining the effects of stirring the melt during growth. To achieve the stirring, the substrate holder was rotated about a vertical axis. The rotation cycle consisted of 3 revolutions/min for 10 sec, followed by reversal of the direction of rotation. Since the substrate was rotated about a vertical axis near its center, the boundary layer thickness was considerably reduced at the edges of the wafer, as compared with the middle. Thus, under mass-transport-controlled growth conditions, the epitaxial layer thickness at the edges of the wafer should be greater than at the axis. This was indeed observed at low cooling rates. A typical example of the variation in the layer thickness with and without stirring as a function of distance from the axis of rotation for a cooling rate of 0.5°C/min is shown in Fig. 4c and d. It can be seen that for the case without stirring (Fig. 4c) the layer thickness at the edges is within $\pm 10\%$ of the thickness at the axis, and there is no systematic variation in thickness from one edge to the other. In contrast, in the case with stirring (Fig. 4d), it can be seen that the layer thickness at the edges is about three times greater than at the axis. This phenomenon is observed only at slow cooling rates when the growth is mass-transport limited. Under kinetically controlled growth conditions at high cooling rates, the reduction in boundary layer thickness should not change the growth rate at the edges of the wafer. Indeed this can be seen from Fig. 4a and b, where no systematic change in epitaxial layer thickness from the edge of the wafer to the center (axis of rotation) can be observed both with or without stirring at a cooling rate of 7°C/min.

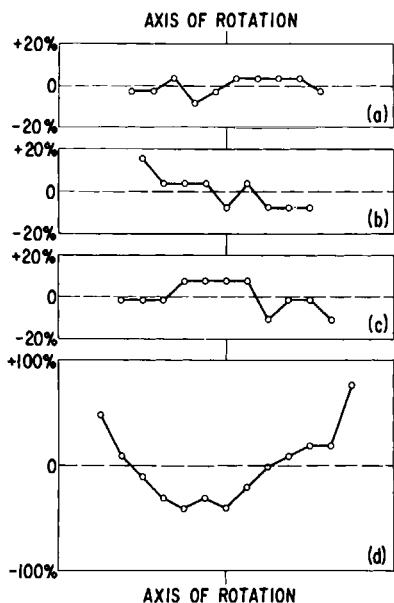


FIG. 4. Measured variation of the epitaxial layer thickness across the wafer from the axis of rotation for cooling rates of 0.5 and 7°C/min, with and without stirring: (a) 7°C/min without stirring, (b) 7°C/min with stirring, (c) 5°C/min without stirring, and (d) 5°C/min with stirring. [From Baliga (1977a). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

3.4.2 Morphology with Undercooling

The morphology of epitaxial layers is an important parameter because it is an indicator of the quality of the crystal. Observation of the morphology can provide important information on the physical processes that control the growth of the epitaxial layer. Furthermore, it is essential to achieve relatively planar epitaxial growth, free of spikes, depressions, and inclusions, if the layers are to be utilized for device fabrication. Consequently, considerable attention has been focused on the surface quality of liquid-phase epitaxial layers of III-V compounds, as well as other materials, such as PbSnTe. These studies have shown that constitutional supercooling (Sekerka, 1973) is an important parameter which influences the surface quality of LPE-grown crystals.

The surface quality of the silicon LPE layers was examined as a function of both the cooling rate and the epitaxial layer thickness (Baliga, 1977b). The change in surface quality of the epitaxial layers with increasing cooling rates under mass-transport-controlled growth conditions is shown in Fig. 5. In all three cases, the epitaxial layers were grown to approximately 15 μm in thickness. It can be seen that at a cooling rate of 0.2°C/min the surface is almost planar, with the exception of a few surface ripples of less than 1 μm in height. These ripples have been found to diminish with increasing layer thickness. When the cooling rate is increased to 0.5°C/min, it has been found that inclusions of tin begin to appear within the

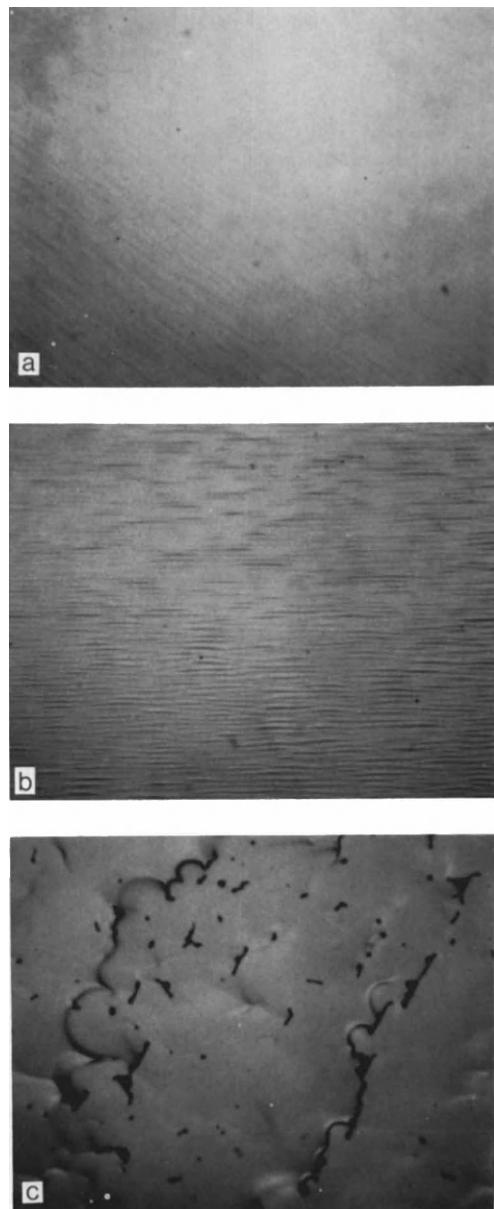


FIG. 5. Photomicrographs of the surfaces of epitaxial layers grown using cooling rates of (a) 0.2, (b) 0.5, and (c) 0.75°C/min. The shorter edge on each photograph represents a distance of 1 mm on the wafer surface. [Reprinted by permission of the publisher from Baliga (1977b). Copyright (1977) by Elsevier Science Publishing Co. Inc.]

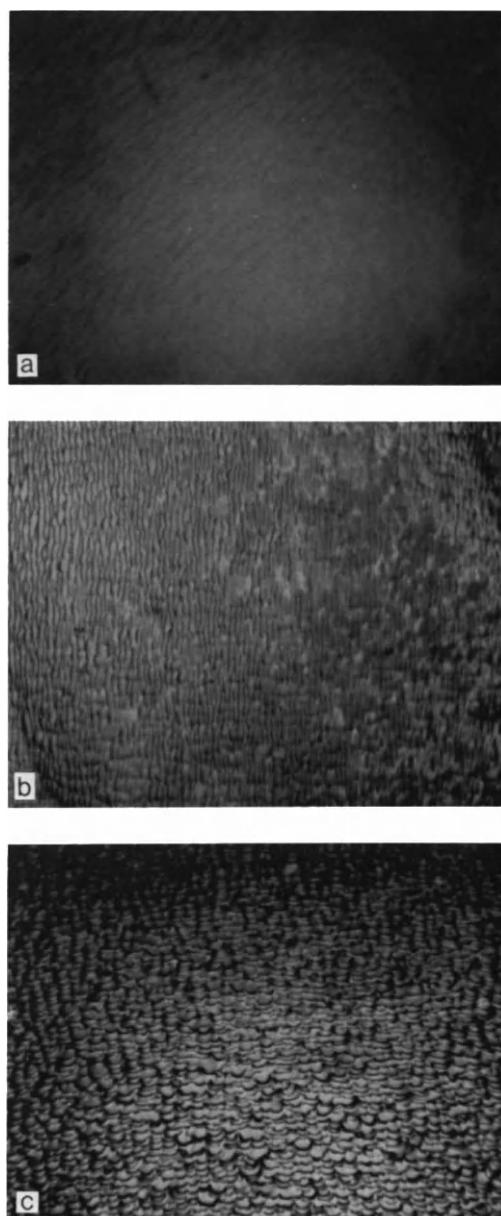


FIG. 6. Photomicrographs of the surfaces of epitaxial layers grown using a cooling rate of $7^{\circ}\text{C}/\text{min}$ to a thickness of (a) 3, (b) 11, and (c) 20 μm . The shorter edge on each photograph represents a distance of 1 mm on the wafer surface. [Reprinted by permission of the publisher from Baliga (1977b). Copyright (1977) by Elsevier Science Publishing Co. Inc.]

epitaxial layer. Angle-lapped cross sections of these epitaxial layers have shown that these inclusions are distributed throughout the epitaxial layer and are not just confined to the interface between the epitaxial layer and the substrate. These observations are indicative of constitutional supercooling during growth (Sekerka, 1973). As the cooling rate increases, the growth rate also increases, thus enhancing the effect of constitutional supercooling as observed here.

At very high cooling rates, the growth of the epitaxial layers becomes kinetically controlled. As a result, constitutional supercooling no longer has an influence on the surface quality. Now the surface morphology becomes strongly dependent on the surface orientation. The change in the surface quality of epitaxial layers as a function of thickness for a cooling rate of $7^{\circ}\text{C}/\text{min}$ is shown in Fig. 6. It can be seen that the surface is now vicinal, with the terraced surface arising from misorientation of the substrate wafer from the (111) plane. These terraces are observed to enlarge with increasing layer thickness. In spite of the very high cooling rate and the higher growth rate, as compared to that at a cooling rate of $0.75^{\circ}\text{C}/\text{min}$, no inclusions were observed in these epitaxial layers. This confirms the earlier conclusion that constitutional supercooling has no influence on the surface quality for layers grown under kinetically controlled growth conditions.

3.4.3 Growth Kinetics under Isothermal Conditions

The preceding results indicate that growth under isothermal conditions should produce the smoothest surface morphologies. This growth, of course, can only be achieved with initial melt supersaturation. In this study (Baliga, 1978), to achieve supersaturation the melt saturation was conducted with stirring until no further loss in weight of the saturation wafer could be detected. Typical saturation times were 45 minutes. After saturation, the melt temperature was lowered to the growth temperature of 949°C .

The epitaxial layer thickness was measured as a function of both supersaturation and growth time. The variation in the layer thickness with supersaturation is shown in Fig. 7 for a growth time of 100 min. In this figure, the supersaturation has been given as the temperature difference between the melt saturation temperature and the growth temperature because the solubility of silicon in tin increases linearly in this small temperature range (Thurmond and Kowalchik, 1960) and, consequently, the temperature difference directly represents the supersaturation. It was found that the epitaxial layer thickness increases linearly with increasing supersaturation.

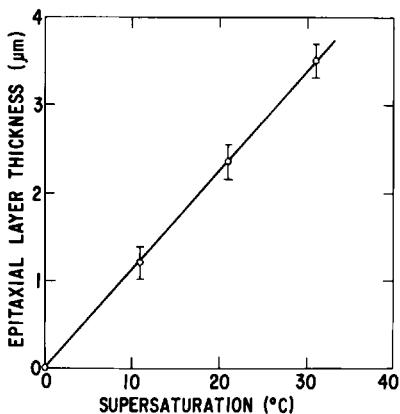


FIG. 7. Linear dependence of epitaxial layer thickness on melt supersaturation for isothermal growth. Growth temperature = 949°C, growth time = 100 min. [From Baliga (1978). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

The observed change in epitaxial layer thickness as a function of growth time is shown in Fig. 8 for a supersaturation of 21°C. From Fig. 8, it can be inferred that the growth rate is decreasing with increasing growth time. This type of behavior has also been observed during the epitaxial growth of GaAs under isothermal conditions (Astles *et al.* 1976).

The kinetics of the epitaxial growth of thin films under isothermal growth conditions has been analyzed by Ghez and Giess (1973). Although their paper discusses the growth of magnetic garnet films, the theoretical analysis can be applied to the data obtained for the growth of silicon layers in this study. The theory is based on the assumption of a stagnant boundary layer through which growth units (silicon atoms here) can diffuse and the incorporation of these units into the epitaxial layer by a first-order reaction at the interface between layer and the melt. A fixed concentration C_L is

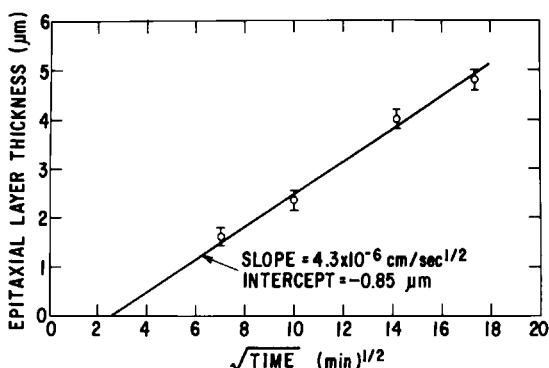


FIG. 8. Dependence of epitaxial layer thickness on growth time for isothermal conditions with a supersaturation of 21°C. Growth temperature = 949°C. [From Baliga (1978). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

assumed beyond the boundary layer. Under these assumptions, the analysis predicts that the epitaxial layer thickness will increase proportional to the square root of the growth time and linearly with supersaturation, as long as the layer density is much larger than the solute concentration in the melt and as long as the growth rate is low because the moving phase boundary was neglected during the analysis. According to this theory, a plot of epitaxial layer thickness versus square root of time will have a slope given by

$$\text{slope} = \frac{2(C_L - C_e)}{P} \frac{\sqrt{D}}{\pi} \quad (3.3)$$

and a negative y-axis intercept given by

$$\text{intercept} = \frac{D(C_L - C_e)}{Pk} \quad (3.4)$$

where C_e is the equilibrium concentration, P the epitaxial layer density, D the diffusion coefficient for the growth units in the melt, and k the surface reaction constant.

It has been shown in Section 3.4.1 that the epitaxial growth of silicon in the present system is mass-transport controlled at lower cooling rates. Thus, under a zero cooling rate (isothermal growth), mass-transport-controlled growth by diffusion through a boundary layer can also be expected to occur. The other assumptions of this theory are also satisfied here because the density of silicon (2.4 g/cm^3) is much larger than the silicon concentration in the melt (a maximum value of 0.045 g/cm^3 for a saturation temperature of 980°C) and the growth rates are extremely small (less than $0.05 \mu\text{m/min}$). This theory, therefore, can be used to analyze the data given in Figs. 7 and 8.

It can be seen from Fig. 8 that the layer thickness indeed increases linearly with the square root of time and has a negative intercept on the y axis. By using this data and Eq. (3.3) and (3.4) for the slope and intercept, the diffusion coefficient D for silicon in tin at 949°C is calculated to be $2 \times 10^{-6} \text{ cm}^2/\text{sec}$, and the reaction constant k is calculated to be $6.4 \times 10^{-5} \text{ cm/sec}$. These values indicated that both the reaction rate at the interface and the diffusion rate through the boundary layer play a role in controlling the growth rate.

The isothermal growth technique is primarily suitable for the growth of thin epitaxial layers. Its application to the growth of thick epitaxial layers is limited by the need for extremely large growth durations and by advent of bulk precipitation in the melt at high supersaturations.

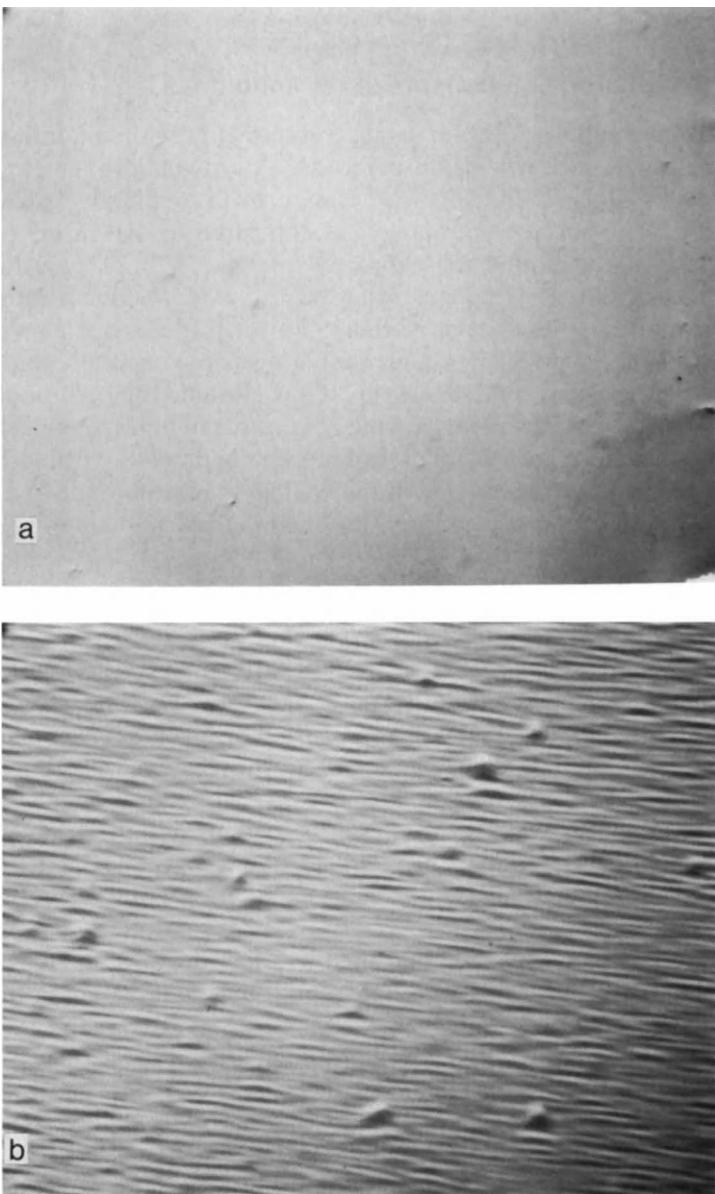


FIG. 9. Comparison of the surfaces of epitaxial layers growth under (a) isothermal conditions and (b) using slow cooling. For isothermal growth, a supersaturation of 21°C was used with a growth duration of 200 min to obtain a layer thickness of 4 μm . In the slow cooling case, a cooling rate of 0.2°C/min was used for 25 min to obtain a layer of thickness of 5 μm . The shorter edge of each photograph represents 1 mm on the wafer surface. [From Baliga (1978). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

3.4.4 Morphology under Isothermal Conditions

The primary motivation for using isothermal growth conditions is to eliminate the surface ripples observed during growth with undercooling. In the case of silicon LPE under isothermal growth conditions, a significant improvement in surface morphology, as compared to that achieved with slow cooling, was immediately apparent (Baliga, 1978). The surfaces of layers grown with slow cooling have been previously demonstrated to exhibit surface ripples. Under isothermal growth, these ripples were absent for all the layers grown under the range of supersaturation (up to 30°C) and epitaxial layer thickness (up to $10\mu\text{m}$) studied here. For purposes of comparison, Nomarski interference contrast photomicrographs of the surfaces of wafers grown under isothermal conditions and under slow cooling conditions are provided in Fig. 9. The significant improvement in surface morphology can be clearly observed in these photographs.

3.5 ELECTRICAL PROPERTIES

In 1977, Girault *et al.* (1977) reported the growth of silicon liquid-phase epitaxial layers by using gallium and aluminum as solvents. Since both gallium and aluminum exhibit shallow acceptor levels in silicon and are readily incorporated into the epitaxial layer, these layers were found to be *p*-type with carrier concentrations above $10^{18}/\text{cm}^3$ and to have short minority carrier lifetimes. In the studies described in this paper, tin was used as the solvent because the incorporation of tin in the epitaxial layer does not introduce either shallow dopant levels or deep lying recombination levels in the silicon energy gap. The carrier concentration and minority carrier lifetime can, thus, be controlled by other dopants, such as boron and phosphorus, and can be adjusted by introducing these impurities into the melt in carefully controlled quantities. However, during the growth of *n*-type epitaxial layers on heavily boron-doped substrates, it was found that the impurity distribution in the layer was strongly influenced by meltback prior to epitaxial growth. In this portion of the chapter, the observed impurity distribution in silicon LPE layers is described and growth conditions that are essential for achieving an abrupt interface between the epitaxial layer and the substrate are defined (Baliga, 1979a). This is followed by results of lifetime measurements, which are of importance to bipolar devices such as solar cells and power thyristors.

3.5.1 Dopant Distribution

As described earlier, in order to grow the epitaxial layers, the melt was first saturated with silicon at the growth temperature by dissolving silicon wafers in the melt. For all the results reported in this section, the saturation

was conducted using phosphorus-doped, float zone wafers with resistivities in excess of 100 ohm cm. For these saturation conditions, the epitaxial layers were found to be *n*-type with doping levels ranging from 1×10^{15} to 1×10^{16} cm³. This doping level was not dependent on the phosphorus concentration in the high-resistivity (>100-ohm cm) saturation wafers and is believed to be controlled by the presence of arsenic contamination in the high-purity tin (five nines purity) used as the melt. The growth was conducted on (111)-oriented *n*-type substrates doped with phosphorus and *p*-type substrates doped with boron. After epitaxial growth, the wafers were etched in aqua regia to remove any tin that may have adhered to the wafer surface. The wafers were then angle lapped, and spreading resistance measurements were made by using an ASR100 spreading resistance probe to obtain the doping profile within the epitaxial layer. The doping profile observed in an epitaxial layer grown on a heavily boron-doped substrate, with a fairly sharp doping transition between the epitaxial layer and the substrate, is shown in Fig. 10. However, under certain experimental conditions, a *p*-type layer with graded doping concentration was observed at the interface between the epitaxial layer and the substrate, as shown in Fig. 11 (Baliga, 1979a).

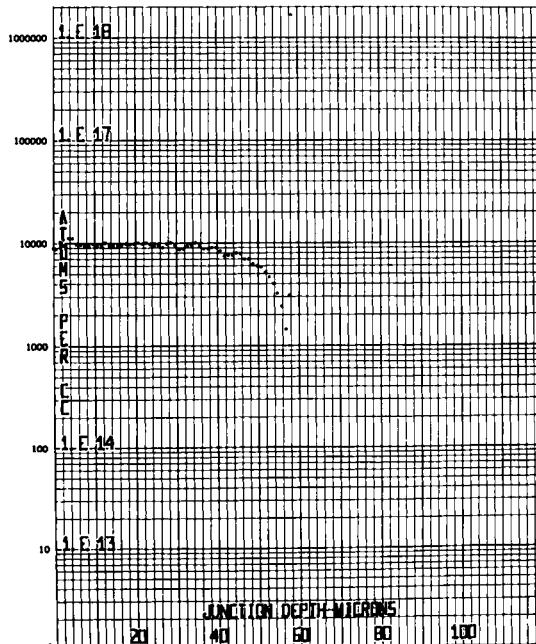


FIG. 10. Dopant distribution profile for an *n*-type epitaxial layer growth on a heavily boron-doped substrate. Note the abrupt transition at the interface between the epitaxial layer and the substrate when no meltback occurs. [From Baliga (1979a). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

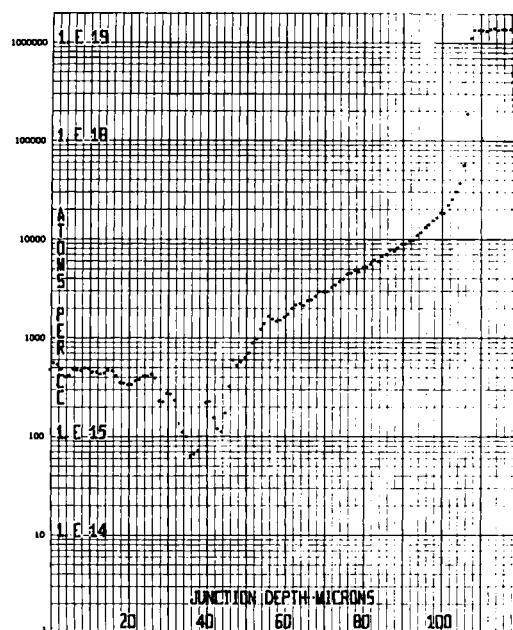


FIG. 11. Dopant distribution profile for an *n*-type epitaxial layer grown on a heavily boron-doped substrate with meltback prior to growth. The meltback produces the exponentially graded *p*-type epitaxial growth near the substrate. [From Baliga (1979a). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

To understand the origin and nature of this layer, growth on heavily boron-doped substrates was conducted under a wide range of experimental conditions. It was found that these experimental conditions could be classified into two types, namely growth with meltback and growth without meltback. The case of growth with meltback is defined as those conditions in which the substrate is introduced into the melt at a higher temperature than the saturation temperature. Since the solubility of silicon in tin increases with temperature, this results in the dissolution of some of the substrate into the melt prior to epitaxial growth. Meltback can also occur if the saturation time is too short. During this dissolution of the substrate (meltback), the boron in the substrate is injected into the melt, and during subsequent epitaxial growth this boron will be incorporated into the epitaxial layer to form the *p*-type graded region. The rapid decrease in the concentration in the *p*-type graded layer with increasing layer thickness indicates that the boron in the melt is rapidly depleted during epitaxial growth and that boron has a large segregation coefficient from liquid tin into solid silicon at the growth temperature (900–1000°C). As epitaxial growth proceeds, the boron concentration in the melt eventually becomes

so low that the layer converts to *n*-type, as seen in Fig. 11. In contrast to this, if the substrate is introduced into the melt at below the saturation temperature, epitaxial growth occurs without meltback, and an abrupt interface between the epitaxial layer and the substrate is observed, as shown in Fig. 10.

3.5.2 Analysis of Dopant Distribution

Based on the preceding description of the origin of the *p*-type graded region in the epitaxial layers, a simple analysis can be performed to obtain an expression for the dopant distribution in the epitaxial layer (Baliga, 1979a). In order to do this, consider growth of an epitaxial layer in the presence of meltback. If the substrate is melted back by a distance d_m , the initial boron content in the melt is given by

$$Q(0) = N_B A d_m \quad (3.5)$$

where N_B is the boron concentration in the substrate and A the area of the substrate. If it is assumed that the boron remains uniformly distributed in the melt during epitaxial growth, then the boron concentration in the epitaxial layer is given by

$$C(t) = k [Q(t)/V] \quad (3.6)$$

where V is the volume of the melt and k the segregation coefficient for boron from liquid tin into solid silicon. From the conservation of boron atoms

$$dQ(t) = -RA dt C(t) \quad (3.7)$$

where R is the growth rate of the epitaxial layer, which can be assumed to be constant during epitaxial growth. It has been experimentally demonstrated that, during the growth of these films by slow cooling of the melt, the growth rate remains independent of growth time and is controlled only by the cooling rate, which was kept constant during the growth of each layer. Equation (3.7) can be integrated with the help of Eq. (3.6) to obtain

$$C(t) = (k/V) Q(0) \exp[-(Ak/V)Rt] \quad (3.8)$$

Since the position in the epitaxial layer from the substrate interface is given by $x = Rt$,

$$C(x) = (k/V) Q(0) \exp[-(Ak/V)x] \quad (3.9)$$

Thus, this analysis predicts an exponential decrease in the boron concentration in the epitaxial layer with distance from the substrate interface. This type of variation is clearly observed in the data shown in Fig. 11.

This analysis demonstrates that the concentration of boron in the epitaxial layer should vary exponentially with distance from the substrate interface. This behavior is based on the assumption that the boron is uniformly distributed in the melt during epitaxial growth. Such an assumption needs to be justified because both accumulation and depletion of dopant concentration has been observed in melts at the interface between the melt and the solid crystal. In addition, the accumulation or depletion of dopants has been found to be a function of the growth rate (Burton *et al.*, 1953). To evaluate this effect, growths were conducted using a wide range of cooling rates to vary the growth rate. The slope of the *p*-type graded region was then measured for equal-area substrates. This slope is plotted as a function of the growth rate in Fig. 12. It can be seen that the slope is essentially independent of the growth rate and has an average value of 460 cm^{-1} . The small scatter in the data points arises from variations in the area of the substrate being dipped into the melt, variations in the angle used for the spreading resistance measurements, and variations in the alignment of the spreading resistance probes with respect to the epi-substrate interface. The absence of a dependence of the slope on the growth rate is not surprising because the growth rates are several orders of magnitude lower than those at which dopant accumulation and depletion are observed during silicon ingot growth (Burton *et al.*, 1953).

Additional evidence for the uniform distribution of boron in the melt was obtained by simultaneous epitaxial growth on a *p*-type and an *n*-type substrate with meltback prior to growth. This was done by mounting a 100-ohm cm, *n*-type, phosphorus-doped substrate and the heavily boron-doped substrate on opposite sides of the same quartz wafer holder. It was observed that the *p*-type graded layer is also formed on the *n*-type substrate and that the concentration as well as the thickness of this *p*-type region

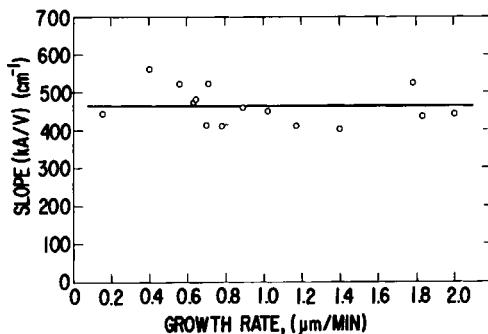


FIG. 12. Slope of the graded *p*-type layer as a function of the growth rate. [From Baliga (1979a). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

matches that observed on the *p*-type substrate. Another piece of evidence for the uniform distribution of boron in the melt was obtained by observing the effect of melt stirring upon the doping profile. It was found that the *p*-type graded layer again exhibited an exponential variation, and the slope of this region was measured as 480 cm^{-1} , which lies very close to the average value of the slope found without stirring. Thus, stirring does not influence the boron incorporation into the epitaxial layer, indicating an absence of any accumulation or depletion of the boron concentration at the growth interface.

3.5.3 Minority Carrier Lifetime

It is well recognized that the minority carrier lifetime is an important parameter which strongly influences the electrical characteristics of bipolar semiconductor devices. Some examples in which the minority carrier lifetime has an influence include the current gain of bipolar transistors, the efficiency of solar cells, and the forward conduction characteristics of power rectifiers and thyristors. In these cases, a large minority carrier lifetime is desirable in order to enhance device performance. Even in the case of other bipolar devices, such as high-speed switching rectifiers, it is desirable to develop adequate processing technology which results in a high minority carrier lifetime, because this allows the subsequent controlled reduction in lifetime by using either the diffusion of deep-level impurities or high energy particle bombardment to obtain the desired device characteristics. A substantial effort in achieving high lifetime during device processing has been expended in the semiconductor industry by careful control of the cleanliness during high-temperature processing. In addition, many gettering techniques have been developed to increase the minority carrier lifetime. In the case of silicon vapor-phase epitaxial growth, it has been found that the minority carrier lifetime is generally much lower than observed in bulk silicon. Furthermore, the minority carrier lifetime in the substrate is degraded during this high-temperature processing step. In this section, the growth of silicon epitaxial layers with high minority carrier lifetimes by using liquid-phase epitaxy is discussed, and the impact of this processing step upon the substrate is described (Baliga, 1982a).

The influence of the liquid-phase epitaxial growth process on the minority carrier lifetime in both the substrate and the epitaxial layer was evaluated. The minority carrier lifetime in the substrates and the as-grown epitaxial layers was measured by using the photo conductivity decay technique (Ryvkin, 1964). To evaluate the influence of typical device processing on the minority carrier lifetime, *p*–*n* junction diodes were also

fabricated in both the substrate and the epitaxial layer, using boron and phosphorus diffusions, and the minority carrier lifetime was subsequently measured by using the reverse recovery technique (Lewis, 1975). As shown in Table 1, the bulk silicon substrates were found to exhibit a very high minority carrier lifetime, as specified by the silicon suppliers. However, even a single high-temperature processing operation, such as wet oxidation at 1000°C for 30 min, was found to reduce the minority carrier lifetime to the range of 20 μ sec. This is typical of most semiconductor processing lines and is associated with the introduction of trace levels of deep-level contaminants either from the wafer cleanup or the furnace ambient. In contrast to this observation, the liquid-phase epitaxial growth process was found to result in not only the growth of epitaxial layers with high minority carrier lifetimes in the range of 100 μ sec, but also in retaining a much higher lifetime in the substrates (also about 100 μ sec). The observation of these high minority carrier lifetimes is believed to arise from the performance of the epitaxial growth in the liquid metal ambient. The melt acts as a gettering agent for deep-level impurities and retards their introduction into the epitaxial layer, as well as into the substrate, during the growth cycle. Table 1 also gives the minority carrier lifetime measured after device processing. Even in this case, it was found that comparable lifetimes were obtained in the bulk silicon substrates and in the epitaxial layers at values close to those observed in substrates on which no epitaxial growth was performed.

These observations substantiate the conclusion that, although a high tin concentration is present in the epitaxial layers as indicated by secondary ion mass spectrometry (SIMS) or Auger measurements, it does not introduce any deep recombination levels which could degrade the minority carrier lifetime. This has been verified by deep-level transient spectroscopy (DLTS) measurements made using the processed wafers. In these measurements, no deep levels could be identified from the background noise, indicating that the deep-level concentration is below the detection threshold of 10^{-3} of the background doping level (10^{15} to $10^{16}/\text{cm}^3$). It can therefore be concluded that earlier reports of deep levels observed by

TABLE 1. Effects of Processing on Lifetime

	Minority carrier lifetime	
	Substrate	Epitaxial layer
Before processing	$800 \pm 200 \mu\text{sec}$	—
After oxidation	$20 \pm 5 \mu\text{sec}$	—
After LPE growth	$100 \pm 10 \mu\text{sec}$	$100 \pm 10 \mu\text{sec}$
After device processing	$20 \pm 5 \mu\text{sec}$	$20 \pm 5 \mu\text{sec}$

DLTS measurements on silicon ion-implanted with tin (Schultz, 1974) were probably associated with unannealed complexes formed by the generation of vacancies arising from the implantation damage.

3.5.4 Autodoping Experiments

Many silicon devices, such as bipolar integrated circuits, microwave IMPATT and PIN diodes, high-speed varactors, and high frequency discrete transistors, require the growth of epitaxial layers on heavily doped substrates with an abrupt transition in the doping between the substrate and the epitaxial layer. These silicon layers have conventionally been grown by vapor-phase epitaxial growth techniques. In this process, two phenomena that prevent the achievement of an abrupt interface are the outdiffusion of the dopant from the substrate into the epitaxial layer during the high-temperature epitaxial growth step and autodoping effects. In general, autodoping can be defined as the transport of dopants from the substrate into the epitaxial layer via the gas phase. Since autodoping degrades the abruptness in the transition between the doping of the substrate and the epitaxial layer and also increases the background doping concentration in the epitaxial layers, many studies have been conducted in order to minimize autodoping effects during silicon vapor-phase epitaxial growth (Bozler, 1973; Gupta and Yee, 1969; Ishii *et al.*, 1975; Skelly and Adams, 1973). These studies have shown that autodoping during vapor-phase epitaxial growth arises primarily from: (1) dopant outgassing into the vapor phase prior to the commencement of epitaxial growth, (2) dopant evaporation from the back surface of the wafer during epitaxial growth, and (3) dopant introduction into the gas phase due to substrate etching by halides during epitaxial growth. Based on these mechanisms, reduction in the autodoping during vapor-phase epitaxy has been achieved by: (1) lowering the epitaxial growth temperature, (2) sealing the back surface of the substrates with silicon dioxide, silicon nitride, or polycrystalline silicon, (3) performing the epitaxial growth in the absence of halides by using silane as the source, and (4) lowering the pressure in the reactor during epitaxial growth so as to reduce the partial pressure of the dopant impurities during deposition. In addition, two-step epitaxial growth procedures have been developed to reduce autodoping effects (Gupta and Yee, 1969; Ishii *et al.*, 1975). Although all of the techniques have been successful in reducing the autodoping, they have not been able to eliminate the problem altogether. This is particularly noticeable when epitaxial growth is conducted over localized diffusions of dopants into the substrates, as is necessary, for example, during the fabrication of integrated circuits. In this case, autodoping causes the lateral transport of the dopant

from the diffused area, which results in severe distortion of the geometry of the diffused buried layer (Srinivason, 1977). Furthermore, in the case of devices requiring closely spaced diffused buried layers such as field controlled devices (Nishizawa *et al.*, 1975; Baradon and Laurenceau, 1976), lateral autodoping can result in the formation of a connecting layer, which prevents the desired isolation between these buried regions. The fabrication of these devices by vapor-phase epitaxy, consequently, requires compensation of the autodoping by the addition of dopants into the gas phase. This approach is difficult to pursue in practice, because of the need to achieve low epitaxial doping concentrations in the presence of strong autodoping effects.

This section discusses autodoping phenomena observed during the growth of silicon layers by using liquid-phase epitaxy (Baliga, 1981). It is demonstrated here that autodoping effects can be completely eliminated by performing the epitaxial growth from the liquid phase. It should be noted that autodoping can occur, even during silicon liquid-phase epitaxial growth, if care is not taken to prevent substrate meltback prior to epitaxial growth. In addition, the results of lateral autodoping studies are discussed for the case of boron-diffused regions in *n*-type silicon substrates. On the basis of these studies, growth conditions have been established which allow the fabrication of closely spaced boron-diffused fingers buried under a *n*-type epitaxial layer. This epitaxial growth technology has allowed the fabrication of high-voltage field-controlled thyristors, as discussed later in this chapter.

3.5.4.1 Heavily Doped Substrates

The first set of autodoping experiments was conducted using 0.01-ohm cm, boron-doped, (111)-oriented silicon wafers. Epitaxial layers were grown on these substrates with the melt undersaturated and supersaturated by 5°C prior to the introduction of the substrates into the melt. The doping profile in the epitaxial layer was then measured by using the ASR100 spreading resistance measurement system. As shown earlier in Fig. 11, when the melt is undersaturated, a *p*-type layer with a graded doping concentration profile is observed at the interface between the epitaxial layer and the substrate. In Section 3.5.2, the nature of this doping profile was analyzed and the *p*-type layer shown to arise from meltback of the substrate prior to epitaxial growth. If the melt is undersaturated when the substrate is introduced into it, part of the substrate is dissolved and the boron in that portion of the substrate is injected into the melt. This boron is subsequently incorporated into the epitaxial layer, forming an exponentially graded *p*-type interface. This phenomenon is similar to the autodop-

ing observed in the case of vapor-phase epitaxy and leads to a nonabrupt doping profile at the interface between the epitaxial layer and the substrate. In contrast, when the melt is supersaturated prior to the introduction of the substrate into the melt, no meltback can occur and an abrupt doping transition is observed at the interface between the epitaxial layer and the substrate, as shown in Fig. 10. Consequently, these experiments show that, although autodoping can occur during silicon liquid-phase epitaxy, it can be completely suppressed by supersaturation of the melt prior to the introduction of the substrates into the melt.

3.5.4.2 Boron-Diffused Substrates

As stated in the introduction, one of the problems encountered during vapor-phase epitaxy is the occurrence of lateral autodoping effects. This has been found to be particularly severe in the case of boron diffusions in *n*-type silicon substrates. Experiments were, therefore, conducted to study lateral autodoping effects during liquid-phase epitaxy. For these experiments, boron diffusions were performed over a portion of 40-ohm cm, phosphorus-doped silicon wafers using thermally grown silicon dioxide as a mask. After stripping the oxide on the wafer surface, *n*-type epitaxial layers were grown with an undersaturation of 5°C to determine the extent of the lateral autodoping. As illustrated in Fig. 13, if the boron injected into the melt due to meltback is localized to the diffused region, the lateral autodoping should be limited to a portion close to the diffused region. In

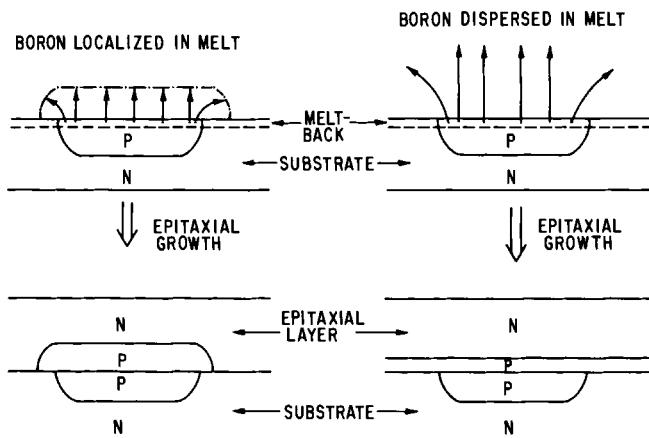


FIG. 13. Illustration of the impact of boron dispersion in the melt on lateral autodoping. [From Baliga (1981). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

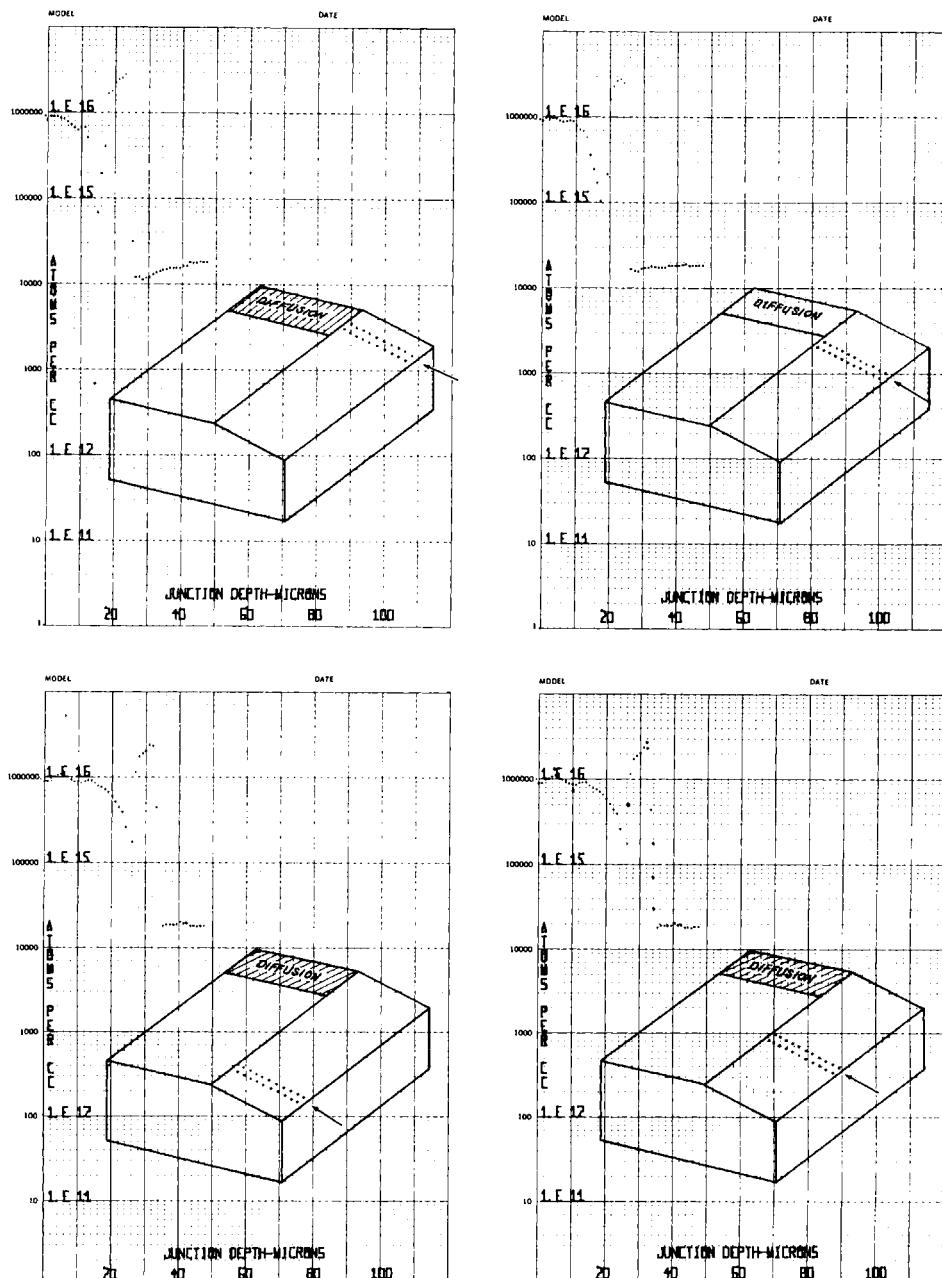


FIG. 14. Measured impurity distribution at four locations on a wafer with boron diffusion into the substrate at one end. The epitaxial layer was grown with partial meltback of the diffused region prior to epitaxial growth. Note that all the profiles are nearly identical indicating rapid dispersal of the boron injected into the melt by meltback. [From Baliga (1981). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

contrast, if the boron injected into the melt is rapidly dispersed, the lateral autodoping should extend across the entire surface of the wafer.

To measure the lateral autodoping, spreading resistance measurements were performed at the diffused portion of the wafer and at various distances from the edge of the diffused region, as illustrated in Fig. 14. In the case shown in Fig. 14 only a part of the diffused layer was etched away by meltback, as can be seen in the profile taken at the diffused region. The profiles taken at various distances from the edge of the diffused region are also shown in Fig. 14. The maximum distance from the edge of the diffused region that was profiled was 1 in. It can be seen that a *p*-type layer is observed at all distances from the edge of the diffused layer. This *p*-type layer has the same peak doping concentration and width at all the profiled locations within the limits of experimental error. From this observation it can be concluded that the boron injected into the melt must be dispersed rapidly throughout the melt during epitaxial growth. The results of these lateral autodoping studies, thus, indicated that to prevent lateral autodoping it is imperative to prevent meltback of the substrate prior to epitaxial growth by careful supersaturation of the melt.

3.6 TECHNOLOGICAL APPLICATIONS

Vapor-phase epitaxial growth of silicon for the fabrication of discrete devices and integrated circuits has been refined since the very inception of silicon technology. This technology is firmly established for routine device and integrated circuit (IC) fabrication due to the availability of equipment for large-scale wafer processing and the excellent control over the growth rate and doping profile provided by modern gas handling systems. Due to these reasons, a new technology such as liquid-phase epitaxy can be expected to be utilized only in those instances where problems are experienced with the use of vapor-phase epitaxial growth. Two examples of this case are discussed in this section of the chapter.

3.6.1 Buried Junction Fabrication

Silicon devices requiring buried regions have been conventionally fabricated by first doing a selective diffusion of a dopant impurity into a substrate of opposite conductivity type and subsequently growing a layer which is of the same conductivity type as the substrate over the surface of the wafer. In the past, this layer has been grown exclusively by using vapor-phase epitaxial growth techniques. One serious problem that has been commonly encountered during vapor-phase epitaxial growth is autodoping. During the fabrication of buried regions for device applications, the autodoping process results in an undesirable increase in the size of the buried regions. Furthermore, autodoping prevents the fabrication of

closely spaced buried grid fingers due to the formation of an initial epitaxial layer which is of the same conductivity type as the diffused regions in the substrate. Since autodoping can be eliminated using liquid-phase epitaxy, it is attractive for buried grid fabrication.

In this study (Baliga, 1979b), test structures were made by the diffusion of boron through oxide windows ($5\text{-}\mu\text{m}$ wide window openings at $20\text{-}\mu\text{m}$ spacings) into a 100-ohm cm phosphorus-doped substrate. This boron diffusion had a surface concentration of $5 \times 10^{19}/\text{cm}^3$ and a junction depth of $3\text{ }\mu\text{m}$. Boron was chosen as the dopant for these experiments because the most severe autodoping effects have been reported for this dopant during vapor-phase epitaxy. After the boron diffusion, the oxide was removed and an epitaxial layer was grown over the surface of the wafer by liquid-phase epitaxy. For the fabrication of the buried grids in this study, the tin melt was initially saturated with silicon at 950°C by dissolving 100-ohm cm phosphorus-doped silicon wafers in the melt. The melt temperature was then lowered to 940°C to ensure supersaturation of the melt. The boron-diffused substrate wafers were introduced into the melt at this temperature, and the furnace temperature was then reduced at a controlled cooling rate of between 0.2 and $0.5^\circ\text{C}/\text{min}$ to induce epitaxial growth. After a suitable growth interval, the substrates were withdrawn from the melt to terminate the epitaxial growth. After epitaxial growth, the wafers were angle lapped and the junctions were delineated by staining techniques to reveal the *p*-type regions. A photomicrograph of the cross section of a wafer after staining is shown in Fig. 15a. It can be seen that isolated *p*-type grid regions have been fabricated by this epitaxial growth process.

These epitaxial growth experiments have been conducted under a wide range of growth conditions by varying the initial growth temperature, the cooling rate, and the degree of supersaturation prior to insertion of the substrates into the melt. These experiments have demonstrated that buried grid regions can be fabricated by silicon liquid-phase epitaxy as long as sufficient supersaturation is achieved in the melt. If the melt is not sufficiently supersaturated, substrate meltback can occur prior to the initiation of epitaxial growth. It has been experimentally found that, even when a small amount of meltback occurs, boron from the diffused areas is injected into the melt and is subsequently incorporated into the epitaxial layer. This results in the formation of an undesirable connecting layer between adjacent grid regions, as shown in Fig. 15b. For the example shown in Fig. 15b, the temperature of the melt was raised by 1°C after saturation. The boron injected into the melt due to meltback can be seen to have created a *p*-type layer across the entire surface of the wafer during the initial epitaxial growth period. Furthermore, other experiments have

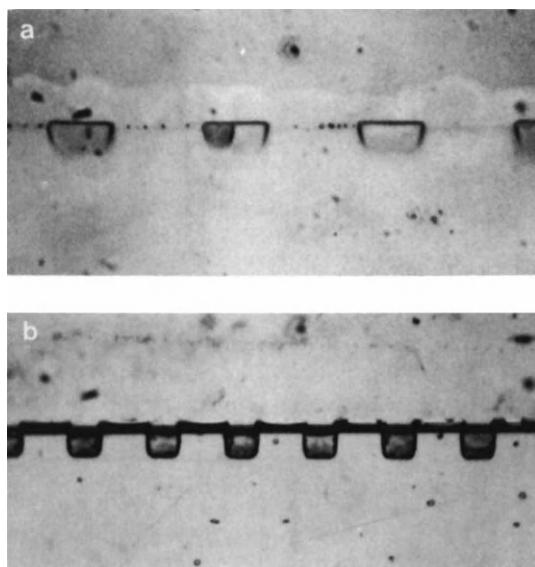


FIG. 15. (a) Isolated, boron-doped, buried-grid regions fabricated in a 100-ohm cm, *n*-type substrate. (b) Meltback-induced *p*-type connecting layer formed between boron-diffused grid regions by slight meltback prior to epitaxial growth. [From Baliga (1979b). Reprinted by permission of the American Institute of Physics.]

shown that, when the meltback is severe, complete dissolution of the boron-diffused regions can occur; thus leaving no grid structure after epitaxial growth. Therefore, supersaturation of the melt prior to the insertion of the substrate into the melt is found to be crucial in achieving buried grid fabrication. The supersaturation can be routinely achieved by using a long saturation time and by lowering the melt temperature by 5–10°C prior to insertion of the substrate into the melt.

3.6.2 Epitaxial Refill

The refilling of deep grooves etched in silicon wafers by preferential etching techniques has been reported for two applications. In the first instance, this process has been used for the fabrication of a vertical multi-junction (VMJ) solar cell structure (Smeltzer, 1975). The fabrication sequence of these devices is illustrated in Fig. 16. Here (110)-oriented, *n*-type silicon substrates are initially oxidized. Deep, vertically walled grooves are then formed by using preferential etching with a mixture of potassium hydroxide and isopropanol. The oxide is then stripped and a *p*-type vapor-phase epitaxial growth step is performed in order to refill the grooves and planarize the surface. In the second instance, the epitaxial

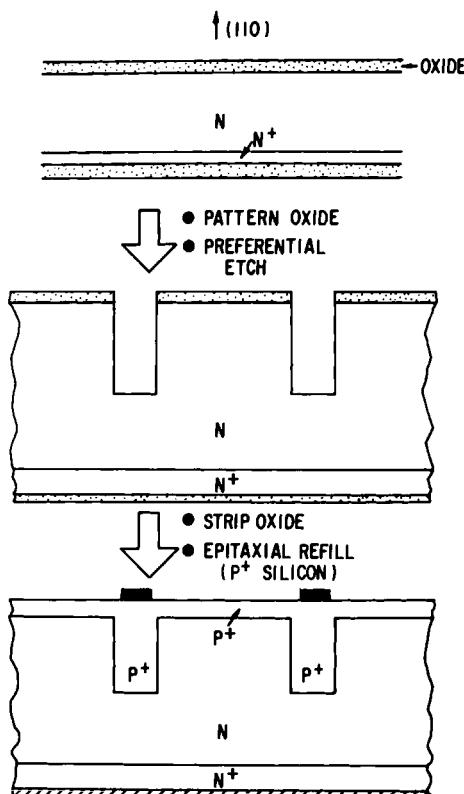


FIG. 16. Epitaxial refill process sequence for the fabrication of the vertical multi junction solar cell structure.

refill process has been used for the fabrication of vertically walled gate regions for high-voltage field-controlled thyristor and junction field-effect transistor structures (Wessels and Baliga, 1978; Baliga, 1980a). The fabrication sequence for this gate structure is illustrated in Fig. 17. In this case, the oxide on the upper surface of the wafer is retained during the vapor-phase epitaxial refill in order to selectively refill the grooves, while preventing epitaxial growth between the grooves, so as to allow subsequent diffusion of the *n⁺* source regions. Although silicon vapor-phase epitaxy has been used successfully for the development of these structures, the significant technical problems that have been encountered include the occurrence of voids in the grooves after refill (Smeltzer, 1975) and the deposition of polycrystalline silicon on the oxide-coated areas of the wafer. An example of the large amount of polycrystalline silicon deposits observed on the oxide is shown in the photomicrograph of Fig. 18. For this

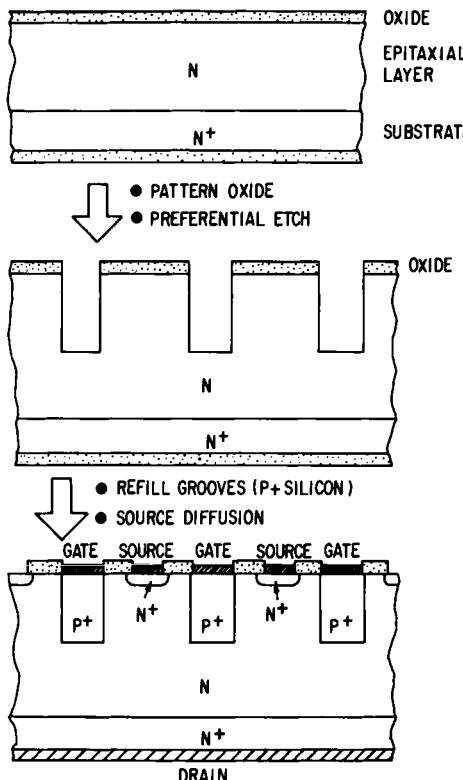
VERTICAL CHANNEL FIELD EFFECT TRANSISTOR

FIG. 17. Epitaxial refill process sequence for the fabrication of gate regions of field-controlled devices.

refill, the vapor-phase epitaxial growth was performed using dichlorosilane with the addition of a carefully controlled amount of HCl gas to reduce as much as possible the deposition of polycrystalline silicon in between the grooves. Although this was successful in minimizing the polycrystalline silicon deposits between the grooves, a significant amount of polycrystalline silicon deposition was observed around the grooves, as shown in Fig. 18. This was found to interfere with subsequent device processing and to result in a reduction in the device yield.

In this section, the use of silicon liquid-phase epitaxial growth for refilling grooves etched in (110) silicon is described (Baliga, 1982a). It is demonstrated here that, under proper growth conditions, epitaxial refilling of the grooves can be achieved without encountering the problems observed with vapor-phase epitaxial refill. The silicon liquid-phase epitaxial

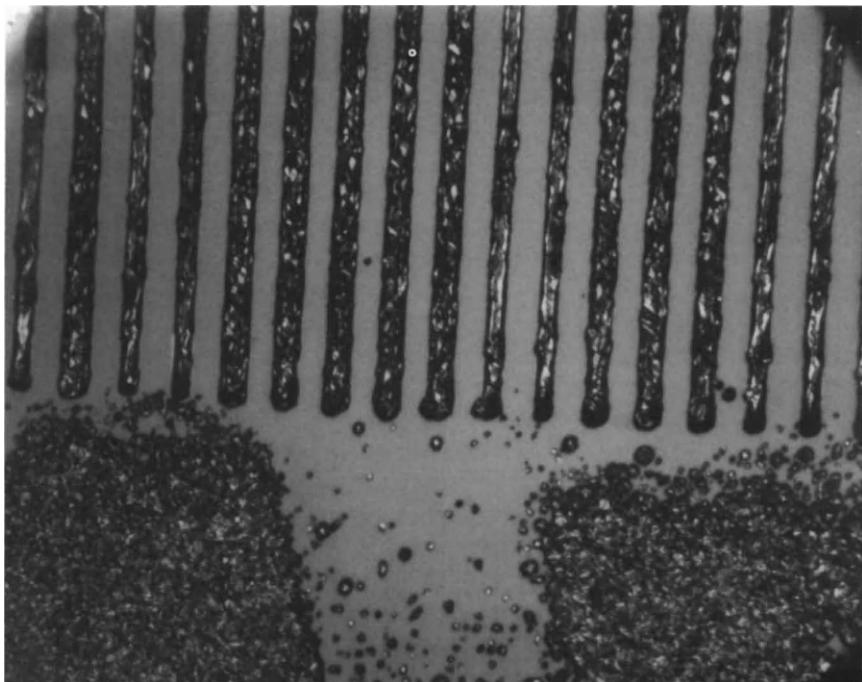


FIG. 18. Photomicrograph of the surface of a silicon wafer after epitaxial refill of grooves using vapor-phase epitaxial growth. Note the large amount of polycrystalline silicon deposited on oxide-covered surfaces around the grooves despite optimization of growth conditions to eliminate deposits between the grooves.

growth process described here has been successful in producing planar refill of the grooves without the formation of voids in the refilled regions. More importantly, no deposition of polycrystalline silicon is observed on the oxide-coated silicon surfaces during the liquid-phase epitaxial refill process. This leaves the surface clean and planarized, which then allows subsequent device processing with high yields. Furthermore, since the silicon liquid-phase epitaxial growth process described here is performed at low temperatures with almost complete conservation of the silicon and since it has been demonstrated to be a high-lifetime process, it is suitable for the fabrication of VMJ solar cell structures.

3.6.2.1 Substrate Preparation

The substrates used for the investigation of the liquid-phase epitaxial refill process were (110)-oriented, phosphorus-doped silicon wafers with resistivities ranging from 80 to 110 ohm cm. These wafers were initially

oxidized to produce an 8000-Å thick oxide layer, which served as the barrier during the preferential etching. The oxide was then patterned by conventional photolithography to open 10-μm wide windows at a repeat distance of 30 μm. The silicon was then etched in a preferential etch consisting of a mixture of potassium hydroxide and isopropanol (Kendall, 1975). The composition and temperature of the etch were chosen such that deep, vertically walled grooves were formed in the wafers with negligible undercutting below the oxide. The groove depth used for the epitaxial refill experiments was typically 8–10 μm.

3.6.2.2 Epitaxial Growth

The silicon liquid-phase epitaxial refill was conducted using tin as a solvent for the silicon. For the purposes of investigating the epitaxial refill process, it was necessary to dope the melt with boron so as to allow delineation of the refilled regions after epitaxial growth. This was performed by using 0.01-ohm cm, boron-doped silicon wafers to saturate the tin melt prior to the epitaxial growth. The temperature of the furnace was then reduced by 5°C to ensure supersaturation of the melt before introduction of silicon substrates into the melt. It was found that, unless supersaturation of the melt was ensured, meltback occurred in the grooves leading to a severe distortion of their shape. An example of the result of meltback is shown in the cross section of a groove shown in Fig. 19. Note that the oxide is not attacked by the melt. Consequently, the meltback not only causes a change in the shape of the groove but results in a large oxide overhang that interferes with subsequent epitaxial growth. With proper supersaturation of the melt, the shape of the groove is retained during the epitaxial growth.

The epitaxial growth was carried out using cooling rates ranging from 0.1 to 7°C/min. It was found that the refilling of the grooves was strongly dependent on this growth parameter. The quality of the refilling of the grooves was also dependent on whether the upper unetched silicon surface was protected by the oxide layer. In the presence of the oxide layer, high-quality epitaxial refilling of the grooves was achieved at the slower cooling rates. In order to examine the progressive filling of the grooves, a series of epitaxial growths was performed using various growth durations. It was found that the epitaxial refill begins at the corners of the bottom of the groove and then extends progressively upwards until a planar refill is achieved after 8 min of growth, as shown in Fig. 20. If the growth is continued beyond this time, the epitaxial growth continues to occur, eventually resulting in the formation of silicon platelets, as illustrated in Fig. 21. Despite the large vertical upward extension of the epitaxial growth,

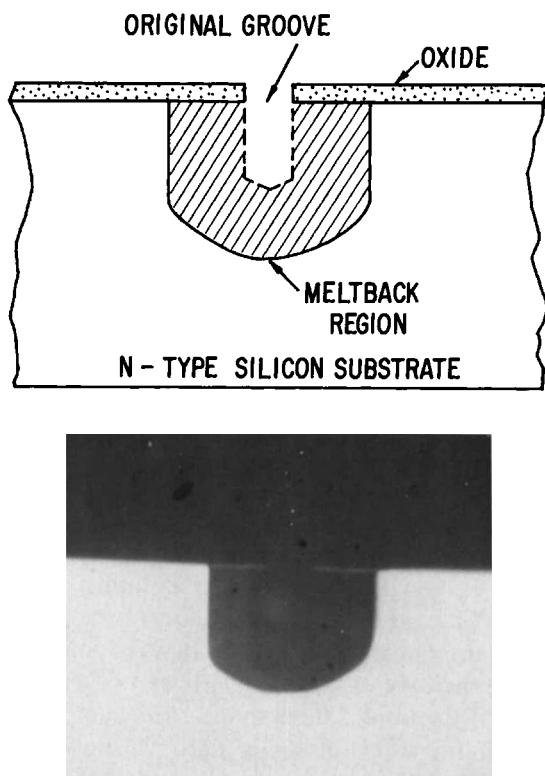


FIG. 19. Distortion of grooves etched in silicon substrates by meltback. The oxide overhang created by the meltback can be seen at the upper edge of the wafer. [From Baliga (1982b). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

very little lateral extension is observed. Since the vertical walls of the grooves are (111) surfaces, this indicates that the growth rate along the (110) direction is much larger than along the (111) direction during silicon liquid-phase epitaxy. In this process, it was found that the grooves could be refilled with no nucleation of silicon on the oxide coated surfaces, thus leaving a clean oxide surface free of polycrystalline silicon deposits. This is an important advantage of the silicon-phase epitaxial refill process when compared with the vapor-phase epitaxial refill process.

Although it was found that planar epitaxial refill can be performed by using silicon liquid-phase epitaxial growth, it should be noted that this is achieved only under slow cooling conditions. At the higher cooling rates,

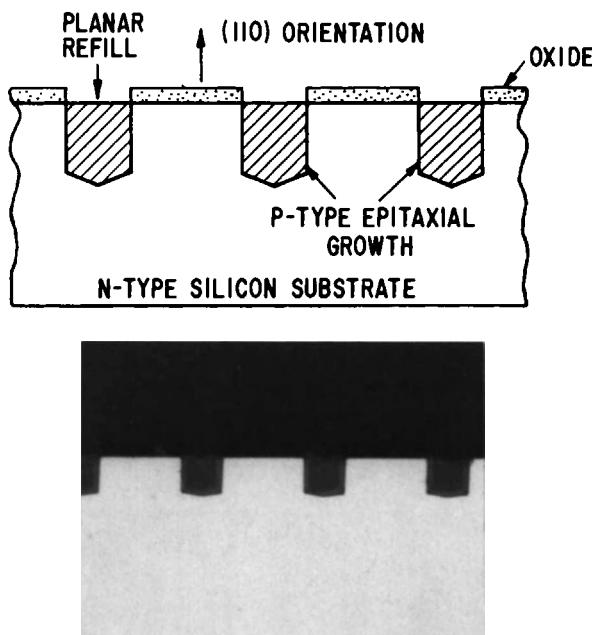


FIG. 20. Planar epitaxial refill achieved by using a cooling rate of $0.2^{\circ}\text{C}/\text{min}$ for 8 min. [From Baliga (1982b). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

preferential growth was observed at the edges of the grooves. This results in the formation of a dual platelet at each groove, as shown in Fig. 22. In this case, the refill was attempted at a cooling rate of $1^{\circ}\text{C}/\text{min}$. Under the higher cooling rates, the refilling of the grooves cannot be accomplished. The formation of the dual platelet, instead of the refilling of the groove, is believed to arise from the higher supersaturation in the melt at the higher cooling rates with diffusion-limited transport of the silicon into the grooves. This causes preferential nucleation of the silicon at the upper end of the groove, with only limited amount of growth occurring at the bottom. As a result of this, the grooves do not fill and the silicon available in the melt is used up by the dual platelet growth at the surface of the wafers, instead of being transported to the bottom of the grooves.

All these experiments were focused on the liquid-phase epitaxial refilling of the grooves in the presence of an oxide layer at the upper surface between the grooves. These results are of interest for the fabrication of the vertically walled gate regions for junction field-effect transistors and

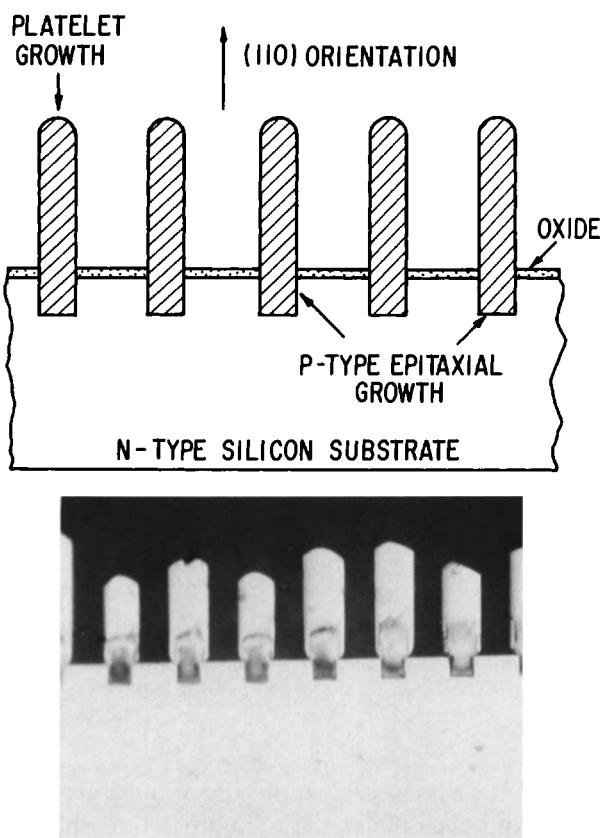


FIG. 21. Silicon platelet formation when growth time was extended to 25 min at a cooling rate of $0.2^{\circ}\text{C}/\text{min}$. [From Baliga (1982b). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

field-controlled thyristors (Wessels and Baliga, 1978; Baliga, 1980a), as illustrated in Fig. 17. The epitaxial refill of the grooves in the absence of the oxide on the upper surface between the grooves was also studied, because this is of interest for the fabrication of vertical multijunction solar cells (Smeltzer, 1975) as illustrated in Fig. 16. A typical cross section of the grooves after epitaxial growth at a slow cooling rate of $0.2^{\circ}\text{C}/\text{min}$ is shown in Fig. 23 in the absence of the oxide on the upper surface. It can be seen that, although the refilling of the grooves has occurred, a planar surface is not achieved because of a large amount of epitaxial growth on

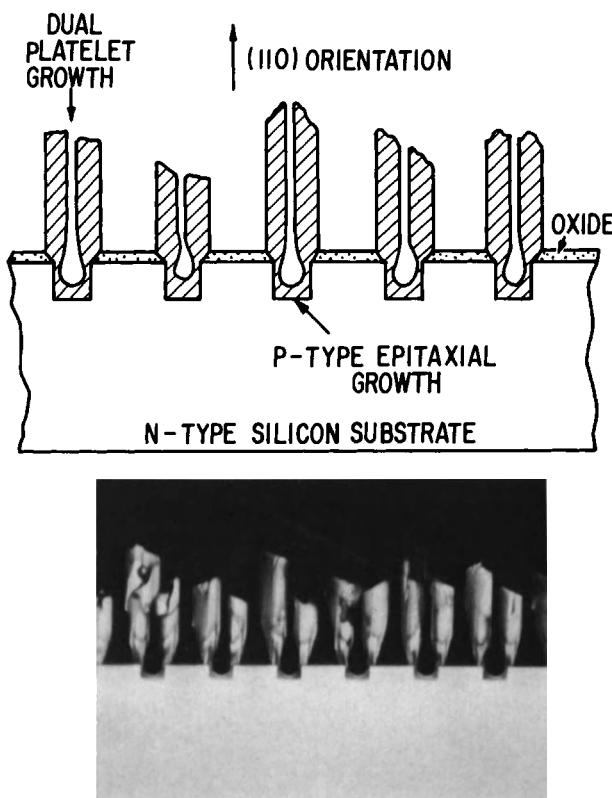


FIG. 22. Dual platelet formation without refilling of the grooves observed when the cooling rate was increased to 1°C/min. [From Baliga (1982b). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

the upper surface. This nonplanar surface may interfere with the subsequent device processing steps. However, it is worth pointing out that this nonplanar surface could also be used to achieve a desirable textured upper surface to reduce the reflection losses in solar cells.

Experiments were also performed at higher cooling rates to investigate the impact on the surface planarity. As in the case of the growths performed at high cooling rates in the presence of the oxide film between the grooves, it was found that the grooves remained unfilled and preferential platelet growth was instead observed at the top surface. Based on these results, it can be concluded that planar epitaxial refill cannot be achieved in the absence of the oxide on the upper surface between the grooves. However,

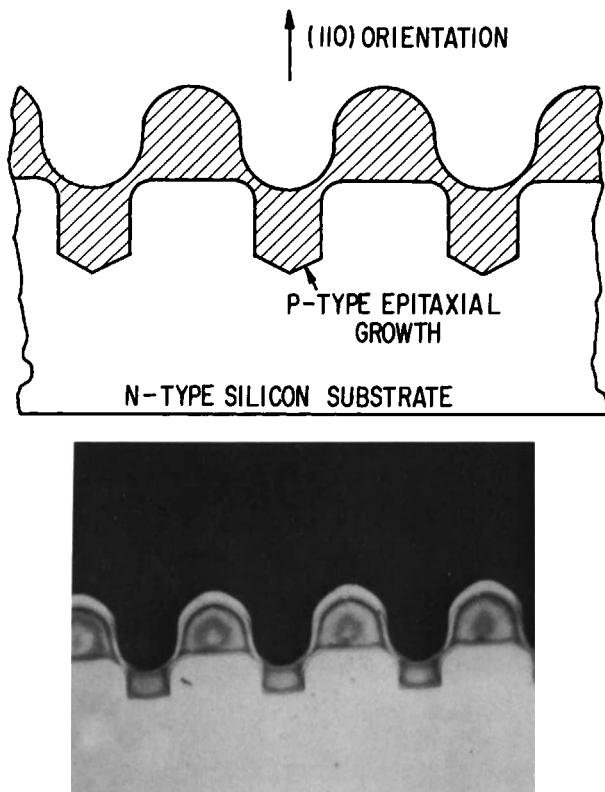


FIG. 23. Cross section of silicon grooves after epitaxial growth at a cooling rate of $0.2^{\circ}\text{C}/\text{min}$ in the absence of the oxide on the upper surface between the grooves. [From Baliga (1982b). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

this does not preclude the application of this epitaxial refill technology to the VMJ solar cells with planar surfaces because the refills could be performed in the presence of the oxide to form a planar surface and a diffusion performed across the upper surface to interconnect them. The advantages of achieving high minority carrier lifetime in the refilled areas (as well as in the substrate), the highly efficient utilization of the silicon during epitaxial growth, and the low epitaxial growth temperatures during the liquid-phase epitaxial growth process could be utilized for the development of a low-cost, high-efficiency solar cell fabrication technology. It is also conceivable that continuous growth of the epitaxial layers can be

achieved by using a temperature gradient in the melt with a source crystal at the higher temperature zone and the substrates at the lower temperature zone in order to achieve an increased throughput.

3.7 APPLICATION TO DEVICES

Although a relatively small effort has been undertaken in silicon liquid-phase epitaxial growth, it has been successfully used for the fabrication of devices where its unique features provide advantages when compared with silicon vapor-phase epitaxial growth. In the cases discussed in this section, the silicon liquid-phase epitaxial growth technology has been used (1) to enhance the breakdown voltage of epitaxially grown junctions by utilizing meltback to create an exponentially graded junction, (2) to fabricate field-controlled thyristors with high blocking gain by using the ability to fabricate closely spaced, boron-diffused buried-grid regions, and (3) to investigate the improvement in solar cell performance by utilizing the high lifetime observed in the layers and in the substrates.

3.7.1 Junction Diodes

The quality of junctions fabricated using silicon liquid-phase epitaxy with tin as the solvent is of importance in evaluating its potential for device applications. The incorporation of a high concentration of tin in these layers has been found by electron microprobe analysis. The presence of this high tin concentration may be expected to have an influence on the junction characteristics, particularly since some studies have implied that the tin introduces deep recombination levels in silicon (Schultz, 1974). In addition, meltback prior to epitaxial growth is expected to improve the crystalline quality of the epitaxial growth, because it provides an *in-situ* substrate surface cleaning prior to growth. However, it has been found that meltback cannot be used for the growth of *n*-type layers on heavily boron-doped substrates if an abrupt interface is required. This section discusses the quality of both abrupt and graded junctions fabricated by silicon liquid-phase epitaxy on heavily boron-doped substrates both with and without meltback (Baliga, 1980b). It is shown here that, in spite of the high tin concentration in the epitaxial layers, the junction characteristics are in agreement with theoretical calculations based on bulk silicon parameters.

For this study, the diodes were fabricated from epitaxial layers grown

at various cooling rates ranging from 0.2 to 7°C/min on heavily boron-doped substrates. In addition, some of these layers were grown with meltback prior to epitaxial growth to allow examination of the influence of the graded *p*-type region on the diode characteristics. The avalanche breakdown voltage of many diodes was measured both at room temperature and at 77 K for each of the wafers. Table 2 lists some of the diode breakdown data, together with the growth conditions and the diode doping profile in the order of increasing exponent factor. This exponent factor α is a measure of the gradient of the junction and is described analytically in the next section. It should be noted that the diode breakdown voltage at 77 K is lower than the value at room temperature. This is an indication that bulk avalanche breakdown is being observed during these measurements. In addition, it can be seen that the breakdown voltage decreases with increasing exponent factor α .

In addition to the breakdown characteristics, the capacitance of these diodes was measured as a function of the applied reverse voltage. The C-V characteristics of four typical diodes are shown in Fig. 24. The broken lines in this figure have been drawn to indicate the shape of the curves for an abrupt junction diode ($C \propto V^{-1/2}$) and a linearly graded junction diode ($C \propto V^{-1/3}$). It can be seen that the curves for diodes with large exponent factors α approach the abrupt junction case, while those for diodes with smaller exponent factors approach the linearly graded case.

Electron microprobe measurements of the epitaxial layers grown in this study indicate that the layers contain tin concentrations in excess of $10^{19}/\text{cm}^3$. This incorporation of tin in the layers may be expected to degrade the quality of the junctions being discussed here. To assess the influence of tin on the junction characteristics, it is necessary to obtain a comparison

TABLE 2. Experimental Data on Graded Junction Breakdown

Sample number	Cooling rate (°C/min)	Exponent factor α (cm^{-1})	N_D (cm^{-3})	Breakdown voltage	
				77 K (V)	Room temperature (V)
GBG-21	0.2	1.0×10^3	6×10^{15}	120	150
GBG-26	2	1.5×10^3	3×10^{15}	100	120
GBG-14	0.5	2.3×10^3	7×10^{15}	130	160
GBG-11	7	2.4×10^3	6×10^{15}	70	80
GBG-5	7	1.5×10^4	8×10^{15}	60	70
GBG-7	0.75	1.0×10^5	5×10^{15}	40	50
GBG-23	0.2	1.0×10^5	1×10^{16}	30	50

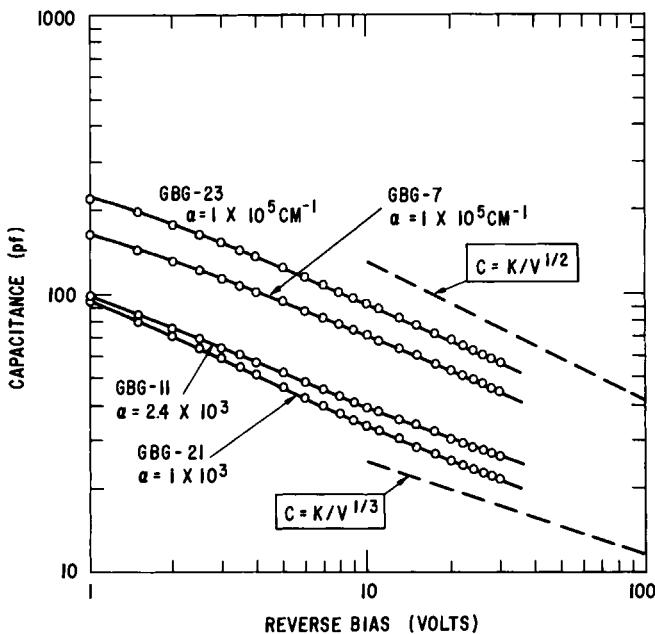


FIG. 24. Variation of the capacitance with reverse bias voltage for abrupt and exponentially graded junction diodes. [From Baliga (1980b). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

of the experimental data with theoretically calculated values of the breakdown voltage based on bulk silicon properties. As shown in a previous section, the doping profile in the epitaxial layers can be described by

$$N_A = N_D \exp(-\alpha x) \quad (3.10)$$

where N_A is the acceptor concentration (boron) and N_D the background donor concentration in the epitaxial layer in the absence of meltback. This doping profile and the electric field distribution are indicated in the inset of Fig. 25. The electric field distribution for this dopant distribution is described by the following Poisson's equation

$$d^2V/dx^2 = -dE/dx = -\rho(x)/\epsilon = -qN_D/\epsilon[1 - \exp(-\alpha x)] \quad (3.11)$$

where $\rho(x)$ is the charge distribution in the junction depletion layer. Integration of this equation provides the electric field distribution

$$E(x) = \frac{qN_D}{\epsilon} \frac{\exp(-\alpha x)}{\alpha} - W_n - \frac{\exp(-\alpha W_n)}{\alpha} + x \quad (3.12)$$

where W_n is the depletion layer width on the n -type side of the junction. This depletion width is related to the applied junction voltage by

$$V_A = \frac{qN_D}{\epsilon} (W_p + W_n) \left[\frac{W_p + W_n}{2} - \frac{1}{\alpha} + \frac{\exp(-\alpha W_n)}{\alpha} \right] \quad (3.13)$$

with

$$W_n + \frac{\exp(-\alpha W_n)}{\alpha} = \frac{\exp(\alpha W_p)}{\alpha} - W_p \quad (3.14)$$

where W_p is the depletion layer width on the p -type side of the junction. In addition, if avalanche breakdown is assumed to occur when the peak electric field in the junction reaches a critical value E_c , then at breakdown

$$W_n + \frac{\exp(-\alpha W_n)}{\alpha} = \frac{1}{\alpha} + \frac{\epsilon E_c}{qN_D} \quad (3.15)$$

From Eq. (3.15), the depletion layer widths at breakdown as well as the breakdown voltage can be calculated as a function of the background doping N_D and the exponent factor α . Using the critical electric field values given by Sze and Gibbons (1966), the depletion layer widths on both sides of the junction and the breakdown voltage have been calculated over a selected range of background doping and exponent factor values and are plotted in Figs. 25 and 26. It can be seen that when the exponent factor exceeds $10^5/\text{cm}$, the breakdown voltage and the depletion layer width on the n -type side of the junction become independent of α , and the depletion layer width on the p -type side of the junction becomes far smaller than that on the n -type side. Consequently, at these large exponent factor values, the diodes will essentially have an abrupt junction characteristic. Similarly, at small values of the exponent factor ($\alpha < 10^2/\text{cm}$), the depletion layer widths on both sides of the junction become nearly equal, indicating that the junction is now approaching the linearly graded case.

A comparison of these theoretically calculated values can now be made with the measured values listed in Table 2. For the wafers with large values for the exponent factor (GBG-7 and GBG-23), the breakdown voltage is within 10% of the calculated values. This indicates that in spite of the high tin concentration in the layers good diode breakdown characteristics can be achieved with this liquid-phase epitaxial growth process for making abrupt junctions. This is of particular significance to the fabrication of devices which require an abrupt transition in doping between the epitaxial layer and the substrate. The achievement of good diode breakdown characteristics in the absence of meltback prior to epitaxial growth is also of significance to the fabrication of buried grid regions. The quality of the

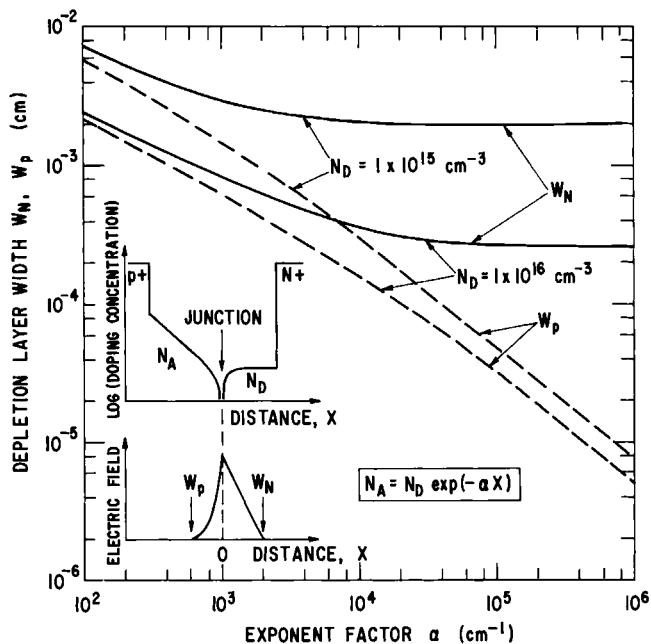


FIG. 25. Calculated depletion layer thicknesses on the *p*-side (w_p) and *n*-side (w_n) of the exponentially graded junciton diode. [From Baliga (1980b). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

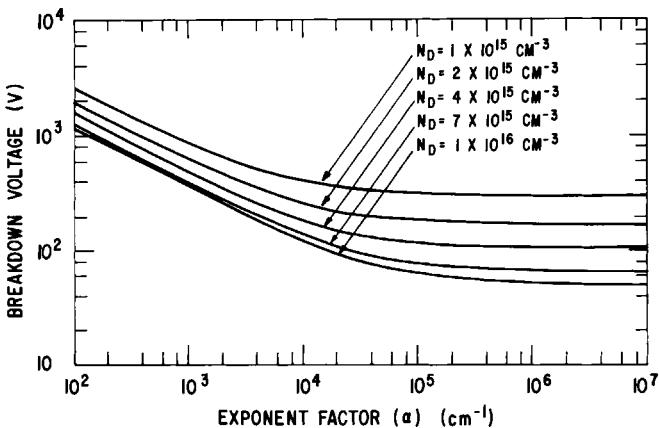


FIG. 26. Calculated breakdown voltage of the exponentially graded junction diodes as a function of the exponent factor α and the background doping level N_D . [From Baliga (1980b). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

diodes grown in the presence of meltback is also of interest because the junction is now located within the epitaxial layer and away from the epi-substrate interface. In addition, Fig. 26 shows that the grading of the doping concentration on the *p*-type side of the junction enhances the breakdown voltage. The measured breakdown voltage of the diodes with exponent factors of about $2 \times 10^3/\text{cm}$ (GBG-14) are indeed about three times larger than those with exponent factors of $10^3/\text{cm}$ (GBG-7), which is in reasonable agreement with the calculated values. It is also worth pointing out that the breakdown voltages of the diodes listed in Table 2 are essentially controlled by the magnitude of the exponent factor and are insensitive to the cooling rate (and, hence, the growth rate) at which the epitaxial layers were grown. Thus, although a high cooling rate has been found to cause a deterioration in the surface quality of the films, it does not seem to cause any significant degradation in the diode breakdown characteristics.

3.7.2 Field-Controlled Devices

Among power devices, the field-controlled thyristor is a relatively recent innovation. This device has characteristics similar to those of conventional thyristors in that the device can block current flow for large applied biases of both positive and negative polarity and can also be operated in such a manner that it conducts large forward currents with a low forward voltage drop. However, the device structure and physics of operation are quite different from those of the conventional thyristor. One striking difference between these devices is that a gate bias is used in conventional thyristors to trigger them from the blocking state to the conducting state, while in the field-controlled thyristor the gate bias is used to maintain the device in its blocking mode of operation. Due to this feature, one of the important parameters used to characterize field-controlled thyristors is the blocking gain. The blocking gain is defined as the ratio of the maximum anode voltage that can be applied before a specified anode leakage current flow commences to the applied gate bias. A large blocking gain is essential for achieving proper device operation with low-voltage gate control circuitry.

The basic structure of the field-controlled thyristor consists of a *p-i-n* rectifier with an integrated gate region which controls the current flow in the forward direction. Two types of gate structures have been fabricated for these devices; namely, the surface-gate structure and the buried-gate structure. The surface gate devices have been fabricated by planar diffusion technology (Houston *et al.*, 1980) and by an epitaxial refill technology (Wessels and Baliga, 1978; Baliga, 1980a; Baliga, 1979c). The surface-gate

structures have the advantage of allowing the gate metallization to run directly over the gate fingers. This provides the device with a low gate resistance, which is essential for achieving high-speed gate turn-off capability. Although the devices that were made by planar diffusion exhibited low blocking gain and poor gate turn-off speed, the vertical channel devices made using the epitaxial refill technology have been shown to exhibit differential blocking gains of over 200 and have gate turn-off times of less than 500 nsec. However, these surface gate structures require interdigitation of the cathode and the gate regions. This results in poor device yield due to photolithographic problems when large-area device fabrication is attempted. This has limited the current handling capability of these devices to below a few amperes. As a result of this, when large-area devices with high current handling capability are desired, the buried-gate device structure is favored.

In the buried-gate field-controlled device structure, shown in Fig. 27, the cathode and the gate regions are located at different levels. This avoids the problem of interdigitation of the gate with the cathode and, consequently, allows the fabrication of devices with large areas. It has been demonstrated by modeling studies (Adler and Baliga, 1980; Yamaguchi and Kodera, 1977) that a high blocking gain results when the channel between the gate regions has a small width (separation between gate regions) and a large depth (depth of the gate regions in the vertical direction). This type of aspect ratio (ratio of length to width) for the channel can be conveniently achieved by planar diffusion of the buried grid regions into an n -type substrate, followed by epitaxial growth of an n -type layer over these diffused regions. The vapor-phase epitaxial growth technique has been used to fabricate buried-grid field-controlled thyristors (Houston

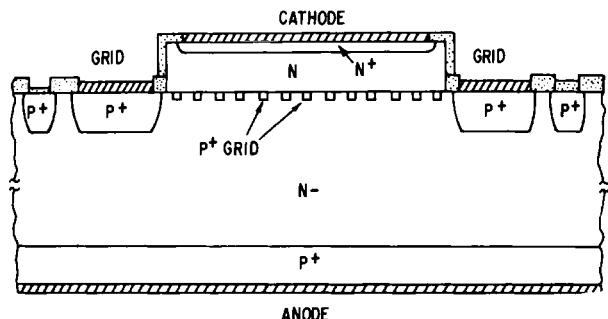


FIG. 27. Cross section of the buried-grid field-controlled thyristor structure with selectively grown cathode region. [From Baliga (1980d). Reprinted by permission of the IEEE, © 1980 IEEE.]

et al., 1980; Nishizawa *et al.*, 1975; Baradon and Laurenceau, 1976). Devices with current handling capability of over 20 A and blocking gains ranging from 20 to 40 have been achieved. However, as discussed in an earlier section, a serious problem encountered during the fabrication of buried grids by using vapor-phase epitaxy arises from autodoping effects. In this section, the application of silicon liquid-phase epitaxy is described for the fabrication of power field-controlled thyristors with the buried-grid structure (Baliga, 1980c). The liquid-phase epitaxial growth technique has allowed the fabrication of field-controlled thyristors with blocking voltages exceeding 500 V and forward current handling capability of up to 10 A.

3.7.2.1 Device Fabrication

The device fabrication procedure will be described with the aid of Fig. 28. The devices were fabricated by starting with 100-ohm cm, phosphorus-doped, (111)-oriented, float-zone silicon wafers with a thickness of 250 μm . After thermal oxidation of the wafers to grow a masking layer of 12,000 Å in thickness, the oxide on the upper surface of the wafers was

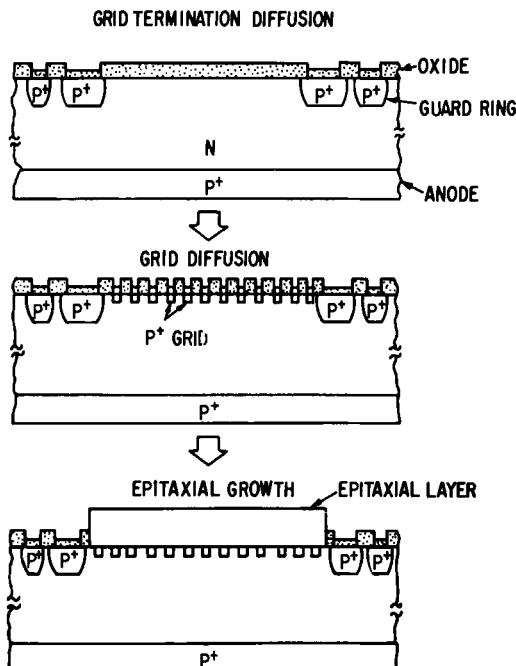


FIG. 28. Process sequence for the fabrication of buried-grid field-controlled thyristors. [From Baliga (1980d). Reprinted by permission of the IEEE, © 1980 IEEE.]

photolithographically patterned to define windows at the periphery of the device for the termination diffusion. A single field limiting guard ring structure, with optimal guard ring spacing, was chosen in order to achieve high breakdown voltages. The guard ring structure was fabricated by planar diffusion of boron to a depth of 20 μm . The p^+ anode region on the back of the wafers was simultaneously fabricated using the same boron diffusion cycle. Following the grid termination diffusion, the oxide in the active area of the device was photolithographically patterned to open 5- μm wide windows in the oxide with a spacing of 15 μm (20- μm repeat distance). Boron diffusion was then performed through these windows to a depth of 2.3, 3.5, and 4.8 μm in order to obtain three different channel aspect ratios. After grid fabrication, a window was opened over the active area of the device for epitaxial growth. A photomicrograph of a device at this stage of fabrication is shown in Fig. 29. The boron-diffused grid fingers

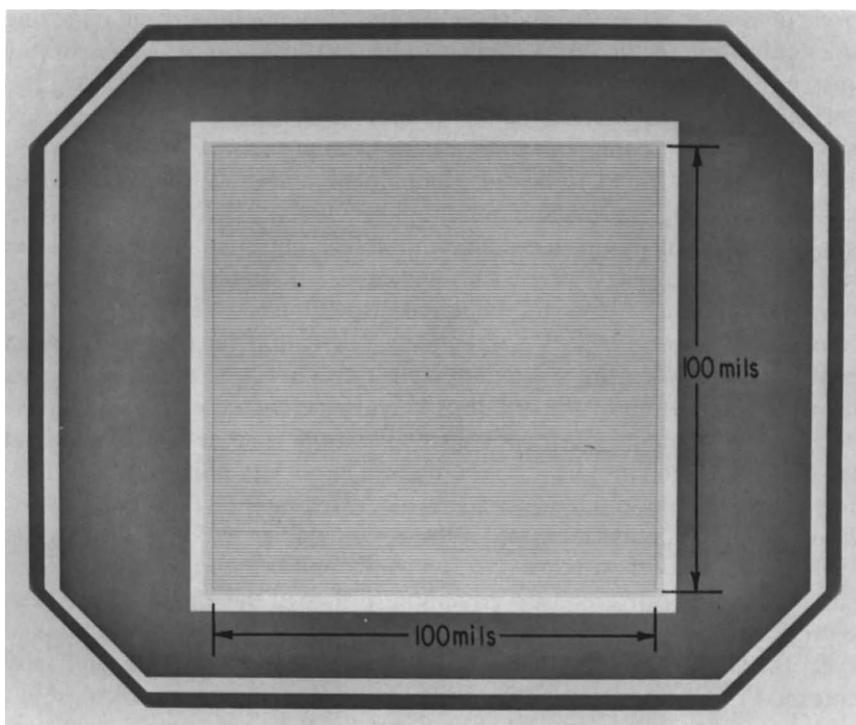


FIG. 29. Photomicrograph of the surface of the field-controlled thyristor after grid diffusion but prior to epitaxial growth. [From Baliga (1980d). Reprinted by permission of the IEEE, © 1980 IEEE.]

are visible within an active area of the device of $2500 \mu\text{m} \times 2500 \mu\text{m}$. Each grid finger has a width of $5 \mu\text{m}$ and a length of $2500 \mu\text{m}$.

The *n*-type epitaxial layer over the grid regions was grown by using silicon liquid-phase epitaxy. In order to obtain the desired *n*-type epitaxial layers with low doping concentrations, the tin melt was saturated at 955°C with 100-ohm cm, phosphorus-doped flat-zone silicon. The saturation was conducted until no further loss in the weight of the saturation wafer was observed. The temperature of the tin melt was then lowered to 950°C in order to ensure supersaturation, so as to prevent meltback. The device wafers were then introduced into the melt, and the temperature was reduced at a cooling rate of 0.2°C per minute to induce epitaxial growth. The growth time was selected to achieve an epitaxial layer thickness of $10 \mu\text{m}$. The substrates were then withdrawn from the melt and any excess tin on the wafers was removed in aqua regia prior to further processing. This growth procedure has been found to result in an abrupt interface between the epitaxial layer and the substrate, with typical epitaxial layer doping levels of between 5×10^{15} and $1 \times 10^{16} \text{ cm}^{-3}$. The importance of achieving supersaturation of the tin melt prior to the introduction of the substrates must be stressed here because, as discussed in an earlier section, the fabrication of buried-grid regions cannot be achieved if any meltback occurs before the commencement of epitaxial growth. A supersaturation of 5°C has been found to be sufficient for obtaining well-defined buried grids without any undesirable autodoping effects. The low growth temperatures used in this process also minimizes outdiffusion of the boron from the diffused grid regions. Another important feature of this epitaxial growth technology is that the epitaxial growth occurs selectively on the exposed substrate surfaces without any nucleation on the oxide. As a result, the epitaxial growth is confined to the active area of the device, as shown at the bottom of Fig. 28, thus leaving the device periphery uncovered for subsequent gate contact metallization. The selective epitaxial growth can be seen in the photomicrograph in Fig. 30. Note the extremely clean, deposit-free, oxide-covered surface. It should be pointed out that, although some lateral extension of the epitaxial growth is observed at the edges of the growth windows, it is insufficient to interfere with device fabrication. The ripples observed on the surface of the epitaxial layer can be reduced by decreasing the growth rate. After the growth of the epitaxial layer, the wafers were oxidized, and the oxide was photolithographically patterned to perform a selective diffusion of phosphorus to form the n^+ cathode region. Windows were then opened in the oxide over the cathode and gate contact areas, after which aluminum contact metallization was evaporated and defined to complete the device structure. The photomicrograph of the device surface shown in Fig. 30 was taken after this step.

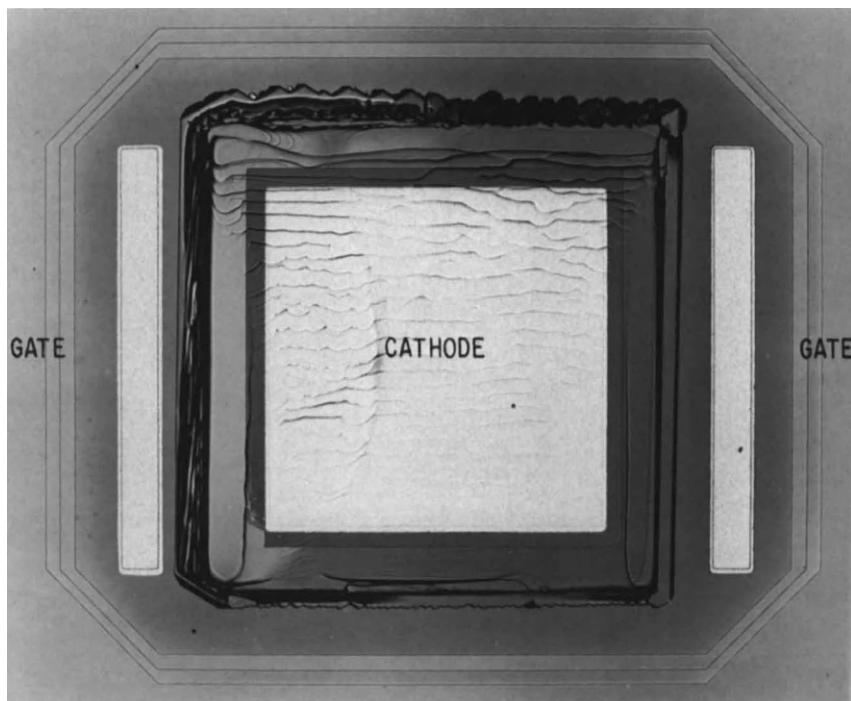


FIG. 30. Photomicrograph of a buried-grid field-controlled thyristor after complete device fabrication. Note the allowance made during the device design for lateral epitaxial growth. [From Baliga (1980d). Reprinted by permission of the IEEE, © 1980 IEEE.]

3.7.2.2 Device Characteristics

3.7.2.2.1 Forward Conduction

The forward conduction characteristics of the buried-grid field-controlled thyristors fabricated by using the above procedure were measured with floating gate potential. A typical forward conduction characteristic for a device with a grid diffusion depth of $2.3 \mu\text{m}$ is shown in Fig. 31. As expected, the characteristics are quite similar to those of a $p-i-n$ rectifier. At low current densities, the anode current is controlled by the diffusion of minority carriers injected from the anode into the n -base region. As the anode current increases, the injection level in the n -base exceeds the background doping level, leading to conductivity modulation effects. These effects control the characteristics of the device up to an anode current of about 0.5 A. At higher currents, recombination in the cathode and anode end regions and a reduction in the ambipolar diffusion length in the n -base, due to carrier-carrier scattering and Auger recombination,

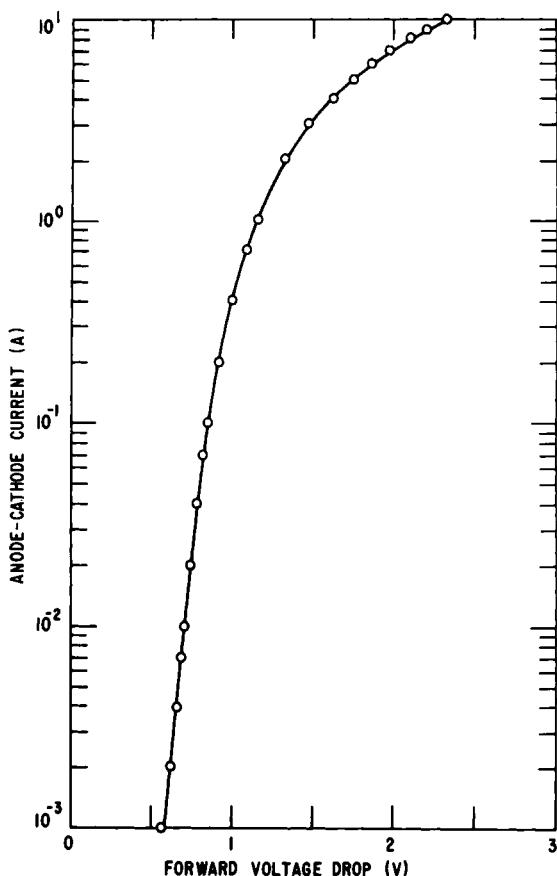


FIG. 31. Forward conduction characteristics of a buried-grid field-controlled thyristor fabricated with grid diffusion depth of 2.3 μm . [From Baliga (1980d). Reprinted by permission of the IEEE, © 1980 IEEE.]

cause a sharp increase in the forward voltage drop. It is worth pointing out that the forward voltage drops observed in these devices are comparable to those observed in typical $p-i-n$ rectifiers with similar base widths. This is a further indication that the epitaxial layers fabricated by silicon liquid-phase epitaxy with tin as a solvent must exhibit good minority carrier lifetime values. Furthermore, it can also be concluded that the liquid-phase epitaxial growth process does not significantly degrade the lifetime in the substrate.

3.7.2.2.2 Forward and Reverse Blocking

Typical forward blocking characteristics of the buried-grid field-controlled thyristors fabricated using silicon LPE devices are shown in Fig. 32 for the three grid diffusion depths utilized for device fabrication. For

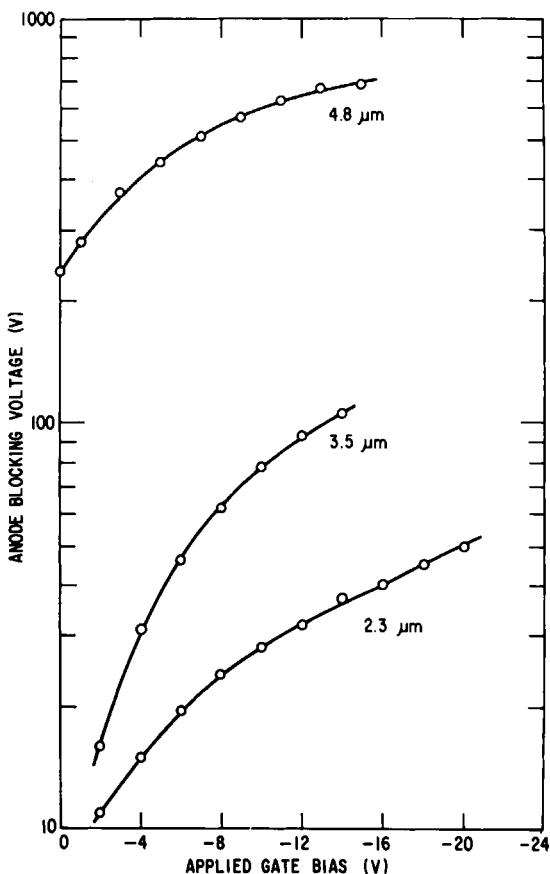


FIG. 32. Forward blocking characteristics of field-controlled thyristors fabricated using grid regions with junction depths of 2.3, 3.5, and 4.8 μm . Note that the latter devices have normally-off characteristics. [From Baliga (1980d). Reprinted by permission of the IEEE, © 1980 IEEE.]

the cases of grid diffusion depths of 2.3 and 3.5 μm , the devices exhibited the expected normally-on forward conduction characteristics at zero gate bias. However, in the case of the devices fabricated with a grid diffusion depth of 4.8 μm , the devices showed forward blocking capability, even at zero gate bias. For 100-ohm cm , n -type silicon, the depletion width due to the built-in diffusion potential of a $p-n$ junction is 3.5 μm . Using this depletion width and a spacing between the grid diffusion windows of 15 μm , an undepleted channel between the grids of 3.4 μm is predicted for a 2.3- μm grid diffusion depth and 1 μm for a 3.5- μm grid diffusion depth. Devices fabricated with these grid diffusion depths, consequently, exhibit the expected forward conduction characteristics at zero gate bias. However, in the case of the 4.8- μm grid diffusion depth, the built-in diffusion

potential of the grid junction is sufficient to completely deplete the channel between the grids and to establish a potential barrier between the anode and cathode, even at zero gate bias. This results in the observed anode blocking characteristics, even at zero gate bias.

The grid diffusion also determines the channel aspect ratio. Two-dimensional modeling studies of current flow in devices of this type have demonstrated that the blocking gain is a strong function of the channel aspect ratio (Adler and Baliga, 1980; Yamaguchi and Kodera, 1977). Increasing the grid diffusion depth in the buried-grid devices increases the channel length and simultaneously decreases its width. The resulting increase in the channel aspect ratio should result in a rapid increase in the blocking gain. This has been observed in the devices fabricated in this study, as shown by the plot of differential blocking gain versus grid diffusion depth provided in Fig. 33. The differential blocking gain increases exponentially with increasing grid diffusion depth. Differential blocking gains of over 40 have been observed for devices fabricated with a grid diffusion depth of 4.8 μm .

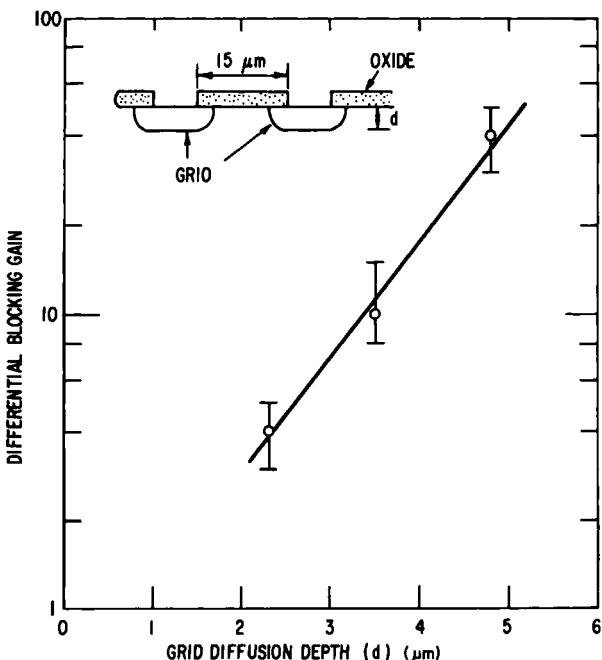


FIG. 33. Exponential increase in the forward blocking gain of buried-grid field-controlled thyristors with increasing grid diffusion depth. [From Baliga (1980d). Reprinted by permission of the IEEE, © 1980 IEEE.]

3.7.2.2.3 Switching Characteristics

As stated in the introduction, the buried-grid structure allows the fabrication of large-area devices with high current handling capability but with limited switching speed due to the inherently high series resistance of the buried grids. Gate turn-off tests performed on the devices fabricated in this study, however, have shown that forced gate turn-off can be achieved at low anode currents. The gate turn-off capability was tested by using a gate pulse to turn-off various steady-state anode currents, while monitoring the time T taken for the anode current to decrease to 10% of its steady-state value. As in the case of earlier devices fabricated using the surface grid structure, the turn-off occurred in two stages. In the first stage, the anode current remains constant after the application of the gate pulse. During this period, a pulse of gate current is observed which removes the charge in the channel region and sets up the gate depletion layer. Following this pulse of gate current, the anode current rapidly decreases to less than 10% of its steady-state value, after which an exponential decay to zero is observed with a time constant of about 8 μ sec. As in the case of the surface grid devices, the turn-off time decreases with increasing gate bias due to the increase in the peak gate current during turn-off which allows more rapid removal of the charge in the channel between the grids. This forced-gate turn-off time was observed to increase with increasing anode current and blocking voltage due to the correspondingly larger charge which must be removed from the channel at each grid bias.

When compared with the surface grid devices, the measured turn-off time is an order of magnitude longer for these buried-grid devices in spite of the significantly lower current densities used during the above measurements. This is a direct consequence of the high grid resistance of the buried-grid structure. In fact, this series grid resistance has been found to prevent forced-gate turn-off in these buried-grid devices when the anode current exceeds 5 A. The buried-grid structure, therefore, is only suitable for the development of high-current devices operating at low frequencies.

3.7.3 Solar Cells

In usual solar cell designs, the front junction consists of a very thin, heavily doped layer. The heavy doping of the layer is required to reduce its resistance. Studies on the effect of heavy doping on the electrical properties of silicon have revealed the existence of a band gap narrowing phenomenon which increases the minority carrier injection into the emitter layer. In addition, as the doping level increases, Auger recombination causes a reduction in the minority carrier lifetime. These effects produce

a loss of 10% in the open circuit voltage and cell efficiency. An alternative emitter design (Wolf, 1980) proposed for solar cells is to maintain the doping level below $10^{17}/\text{cm}^3$ to avoid bandgap narrowing and increase the emitter thickness to maintain the same sheet resistance. Due to the increase in the mobility with decreasing doping level, the emitter thickness for these cells is typically in the range of 10 μm . The optimization of such thick emitter solar cells (Possin, 1984) indicates that the minority carrier lifetime in the emitter must be about 10 μsec to achieve the desired improvements in open circuit voltage and cell efficiency. Such a thick emitter cell is predicted to exhibit an open circuit voltage of 0.75 V and an AM1 efficiency of up to 25% if reflection losses, grid shadowing, and surface recombination are neglected.

During the growth of epitaxial layers using vapor-phase epitaxy, it has been found that the lifetime in the epitaxial layers is generally below 1 μsec . This high-temperature process also degrades the minority carrier lifetime in the bulk. In contrast, the studies on silicon layers grown using liquid-phase epitaxy with tin as the solvent have demonstrated that high minority carrier lifetimes can be obtained in both the epitaxial layer and the substrate. These studies were performed on *n*-type epitaxial layers using substrates which were either high-resistivity *n*-type or highly doped with boron (*p*⁺ substrates). The former substrates (*n*-type) were used to evaluate the impact of the liquid-phase epitaxial growth sequence upon the minority carrier lifetime in the substrate while the latter (*p*⁺) substrates were used to evaluate the lifetime in the epitaxial layers.

For the evaluation of the application of the silicon liquid-phase epitaxial technology for thick emitter solar cell fabrication, *p*-type layers were grown on *n*-type substrates (Possin, 1984). Although no solar cells were made, measurement of the minority carrier diffusion length in the epitaxial layers was performed by using the electron beam induced current (EBIC) technique. It was found that the minority carrier lifetimes were generally in the range of 0.3 to 1 μsec . These low lifetimes are inadequate for obtaining the optimum performance of the thick emitter solar cell. The lower lifetime values obtained in this work when compared to earlier studies can be ascribed to several possible causes. First, the layers grown for the solar cell application were *p*-type, resulting in measurement of electron lifetimes compared to the earlier studies on *n*-type epitaxial layers where hole lifetime was measured. Second, the quality of the epitaxial layers grown for the solar cell development was significantly worse than obtained in the previous work. With improvements in epitaxial growth, it may yet be possible to use the silicon liquid-phase epitaxial growth technology for thick emitter solar cell fabrication.

3.8 SYNOPISTIS

In this chapter, the development of a silicon liquid-phase epitaxial growth technology has been reviewed. By using tin as a solvent for the silicon, *n*- and *p*-type epitaxial layers can be grown whose doping level is independently controlled by the addition of dopants into the melt using appropriately doped saturation wafers. The lowest doping level achieved in this work was limited to $10^{15}/\text{cm}^3$ (*n*-type) due to residual donor impurities in the melt. This value is sufficiently low for a large variety of applications. The important features of this method for silicon epitaxial growth have been found to be (1) a relatively low growth temperature ($\approx 900^\circ\text{C}$), (2) a high minority carrier lifetime ($\approx 10 \mu\text{sec}$), (3) the elimination of auto doping problems, and (4) the ability to perform selective epitaxial growth with no silicon nucleation on oxide-coated surfaces. These features of silicon liquid-phase epitaxy make it attractive for some applications where vapor-phase epitaxial does not provide adequate performance. Some of these cases are (1) buried grid fabrication for vertical-channel field-controlled devices and (2) development of high-efficiency solar cells.

Although the level of the research effort in silicon liquid-phase epitaxy continues to be minuscule compared with other silicon epitaxial growth techniques, this epitaxial growth technique is still under investigation as indicated by some recent publications (Kass *et al.*, 1985; Barnett *et al.*, 1985). The unique features of silicon liquid-phase epitaxy discussed in this chapter can be expected to make it of continued interest for special applications in the future when conventional vapor-phase epitaxy fails to provide adequate results.

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4 SILICON-ON-SAPPHIRE HETEROEPITAXY

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4.1 INTRODUCTION

The use of silicon-on-insulator (SOI) technology has recently gained significant prominence as an alternative to bulk silicon for fabricating specialized, high-performance VLSICs and related devices for both commercial and military applications. With the current trend in VLSI technology toward an ever-increasing packing density and a concomitant reduction in device features to submicrometer dimensions, the need for replacing bulk silicon as a substrate becomes increasingly acute. This trend is mainly dictated by several fundamental device physics considerations such as excessive parasitic capacitance, latchup, and high crosstalk capacitance which severely limit the packing density of scaled-down MOS and bipolar devices in bulk silicon substrates. Most of these limitations are completely eliminated by the use of SOI substrates.

The silicon-on-insulator technology for integrated circuit (IC) applications can be broadly classified into two main groups: heteroepitaxial and recrystallized silicon films on an insulating substrate. Heteroepitaxial silicon technology was initiated in the early 1960s. Research on recrystallized silicon films on insulators is being performed at several laboratories. The primary motivation is to provide high-quality single-crystal silicon films on low-cost substrates. An additional benefit is that three-dimensional structures are feasible. Although substantial progress has been made in achieving high-quality crystalline regions on small areas, additional work is on-going to eliminate grain boundaries and subboundaries to provide a

good-quality film over the entire substrate. Single-crystal silicon films on large-area substrates have been successfully deposited heteroepitaxially on several insulating substrates which include sapphire, spinel, crysoberyl, and gallium phosphide. The availability of sapphire coupled with early successes in depositing single-crystal silicon by conventional CVD techniques, has resulted in silicon-on-sapphire being the dominant heteroepitaxial silicon technology and also the most advanced silicon-on-insulator technology. This chapter reviews advances in the growth, characterization, and processing of SOS material for commercial and military VLSI applications. In general, they are equally applicable to any recrystallized silicon-on-insulator technology. A major deficiency preventing the realization of the full potential of SOS technology has been the quality of the as-grown epitaxial silicon film. Crystallinity, chemical impurities, and electrical properties of SOS films are evaluated by both destructive and non-destructive measurement techniques. Their advantages and limitations are analyzed. Material improvement processes, such as solid-phase epitaxial regrowth, and optimization of epitaxial growth conditions, are reviewed. Their impact on device performance and future potential is also discussed.

The inferior crystallinity of the silicon film in typical as-grown SOS substrates generally results in low minority carrier recombination lifetime and high reverse-bias junction leakage. This precludes the application of SOS to dynamic RAM and bipolar circuits. However, for applications employing majority carrier devices such as monolithic microwave ICs, custom logic circuits, gate arrays, CMOS static RAMs and ROMs, SOS offers several unique advantages. These include high speed (reduced junction capacitance and elimination of interconnect-to-substrate capacitance), high packing density (isolation/guard-ring diffusions and well contacts are not required), a reduced number of masking steps (no isolation diffusion), flexibility and ease in circuit design and layout, smaller short channel length and narrow width effects on threshold voltages, less hot-electron injection into SiO_2 , latchup-free operation under electrical stress and radiation environment, and high tolerances to transient ionizing radiation and cosmic rays. These advantages, except for higher speeds, become very significant as the feature dimensions are decreased. With a decrease in feature sizes, the interelectrode capacitance increases, and the speed differential depends more on the details of the circuit layout and the device scaling methods employed.

Silicon-on-sapphire also has some drawbacks such as low channel mobility, high source-to-drain leakage current, and floating substrate effects on both static and dynamic characteristics. However, for many IC applications, these parameters can be designed into the circuit provided they are reasonably constant and are adequately incorporated in circuit models.

In the past, these factors, coupled with high substrate costs, have resulted in a smaller technical community working on specialized low-volume applications. A major deficiency preventing the realization of the full potential of SOS technology has been the quality of the as-grown epitaxial silicon film. Substantial progress has been made in developing material characterization techniques and better-quality SOS films. These developments, as well as novel material improvement processes, are emphasized in this chapter; a comprehensive review of recent publications has been given by Gupta and Vasudev (1983).

4.2 SAPPHIRE SUBSTRATES

The commercial availability of high-purity sapphire substrates in the early 1960s coupled with early successes in depositing single-crystal silicon films on sapphire led to its eventual domination as the most successful insulating substrate for silicon growth. This was surprisingly achieved in spite of a rather large mismatch between the crystalline and thermal properties of silicon and sapphire. A comparison of the key thermomechanical and crystallographic parameters of silicon and sapphire are shown in Table 1 pointing out some of the advantages and disadvantages of the SOS system. First of all, the crystal structures are completely different. It is, therefore, not obvious which crystal plane of sapphire is best suited for the growth of (100) silicon films. Early experimental observations by Cadoff and Bicknell (1966) indicated that (111) silicon could be deposited on (0001) sapphire planes. Manasevit *et al.* (1974) completed the picture by

TABLE 1. Key Physical and Thermal Properties of Silicon and Sapphire

Parameter	Sapphire	Silicon
Crystal structure	Rhombohedral	Cubic
Lattice parameter (\AA)	$a = 4.75$ $c = 12.97$	$a = 5.43$
Relative dielectric constant	9.4	11.7
Thermal conductivity (cal/cm sec deg)	0.06	0.30
Linear coefficient expansion, ($^{\circ}\text{C}^{-1}$)	7.7×10^{-6}	3.1×10^{-6}
Specific heat (cal/g)	0.10	0.18
Thermal diffusivity (cm^2/sec)	0.15	0.85
Young's modulus (dyne/cm)	29.4×10^{11}	10.7×10^{11}
Tensile stress (dyne/cm)	7×10^9	6.9×10^8
Thermal stress resistance ^a ($^{\circ}\text{C cm}^2/\text{sec}$)	48	142
Melting point ($^{\circ}\text{C}$)	2040	1430

$$\text{TSR} = \frac{(\text{thermal diffusivity})(\text{tensile strength})(1 - \text{Poisson's ratio})}{(\text{Young's modulus})(\text{linear coefficient of expansion})}$$

depositing silicon on a sphere of sapphire and mapping all the various orientation relationships. An examination of the lattice parameter and thermal expansion coefficients in Table 1 for silicon and sapphire clearly predicts a large compressive stress that is likely to be induced in the epitaxial film, when the SOS film is heated or cooled. This is indeed found to be a dominant factor in controlling the SOS electrical properties as will be discussed later. On the positive side, the high melting point of sapphire minimizes any adverse chemical reaction between silicon and Al_2O_3 during growth or device processing. The high dielectric constant of sapphire is of considerable advantage in fabricating microwave strip lines for monolithic microwave integrated circuits at frequencies around 1 to 10 GHz. Although the relatively low value of thermal conductivity of sapphire compared to silicon appears to be a disadvantage for power dissipation, it should be noted that the large reduction in parasitic capacitances of SOS leads to a much lower power dissipation for the same circuit when compared to bulk silicon. Another interesting aspect that is not very well known is that the thermal conductivity of sapphire increases very rapidly on cooling and becomes higher than silicon at temperatures around 20 K. Thus, SOS may offer significant advantages over bulk silicon for dissipating power in high-density CMOS integrated circuits at cryogenic temperatures.

There are at present three major techniques for growing single-crystal sapphire material, and they have been discussed in detail by Cullen and Wang (1978). The three methods include flame fusion or Verneuil growth (Borel, 1978), Czochralski growth (Falkenburg, 1976), and edge-defined film-fed growth (EFG) (Labelle, 1971). Although the flame fusion method has produced the highest-quality crystals with extremely high purity, the lack of sophisticated engineering controls during crystal growth has prevented the achievement of high yields for electronic-grade substrates. The two major commercial techniques for growing sapphire are the Czochralski and edge-defined film-fed, or ribbon, methods. The apparatus for the two methods are shown in Fig. 1. As can be seen from the figure the Czochralski method uses rf heating to melt alumina powder into a melt, while a boule with a diameter ranging from 2 to 4 in. is pulled from the melt with the aid of a seed crystal. The maturity of the Czochralski technology has resulted in the fabrication of substrates with high yield and excellent diameter control. By contrast, the EFG method uses a specially shaped coracle or die to pull "sheets" of sapphire ribbons from an appropriately shaped seed. The width and thickness of the sheet are determined by the die size while the length is determined by the height of the growth apparatus. For both methods the proper control of the solid-liquid interface is critical for achieving good-quality crystals with the proper orientation. The EFG

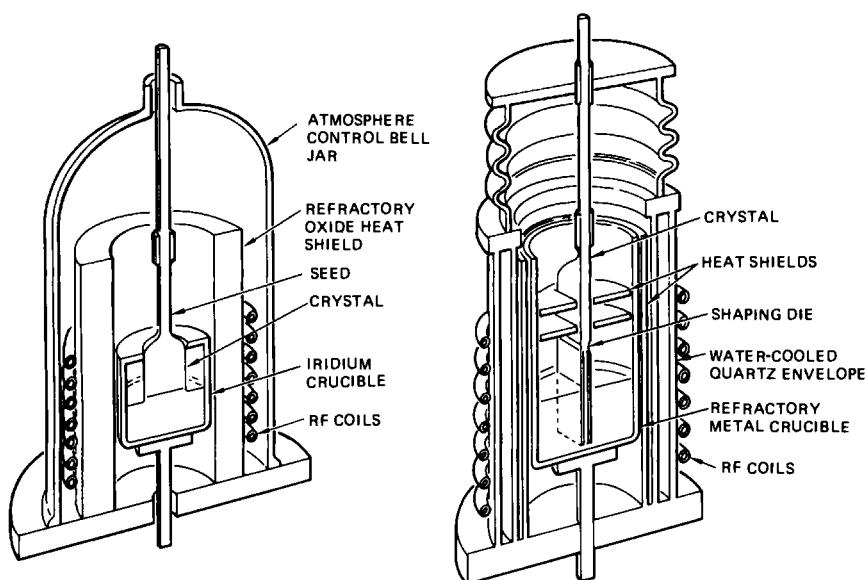


FIG. 1. Czochralski and EFG crystal pulling systems for sapphire growth.

technique has an advantage over the Czochralski technique in that multiple ribbons can be pulled at the same time thereby increasing the yield of substrates. In addition, it appears that the EFG method is more suited economically for producing the large-diameter sapphire substrates (4 in. or larger) than Czochralski. This is primarily due to the size and cost of larger-diameter iridium crucibles for Czochralski which make it economically very difficult to compete with EFG.

Independent of which growth technique is used, the boules or ribbons are further processed before growth of epitaxial silicon. The boules are typically ground and sliced to produce circular substrates with thickness ranging from 16 to about 20 mils. The ribbons are first cut into squares and then ground together as a stack to produce the required circular substrates. Once the substrates are cut and shaped, they are typically polished in a two-step process involving mechanical removal followed by a chemical-mechanical polishing. The final proprietary surface finishing treatment or polish described by Walsh and Herzog (1965) is believed to be very critical in determining the quality of the epitaxial deposition and the characterization of the silicon-sapphire interface. A substrate surface with a relatively low density of crystalline and topographical faults is a prerequisite for the growth of high-quality epitaxial layers by any deposition technique since disturbances of the periodic field at the substrate give rise to defects in the silicon layer during early stages of growth.

4.3 EPITAXIAL DEPOSITION OF SILICON FILMS

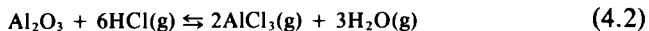
Single-crystal silicon films can be deposited on sapphire substrates by a variety of methods including vacuum evaporation, sputtering, molecular-beam epitaxy (MBE), or chemical vapor deposition (CVD). Of these methods, CVD has proved to be the most successful and is used exclusively in the commercial preparation of SOS films.

The early work on SOS used vacuum evaporation or MBE and is reviewed by Filby and Nielsen (1967). The problems with this approach are related to achieving a low enough vacuum as well as a high enough growth rate for high throughput. In addition the substrate cleaning methods in vacuum were not sufficiently developed for achievement of adsorbate-free surfaces prior to epitaxy. In the MBE technique, the silicon charge in a crucible is heated by an electron beam while the sapphire substrate is held at a temperature of 700–750°C. The evaporation pressure is typically 10^{-8} – 10^{-10} torr and the deposition rate is typically 0.5–1 Å/sec. In principle, the MBE technique is capable of producing the highest quality SOS films due to the ultrahigh vacuum environment and low growth temperatures employed. Work by Eche and Duda (1977) and Bean (1980) has resulted in higher deposition rates and films with excellent crystalline quality.

As mentioned previously, the CVD technique is currently the dominant technology because of its high throughput, low cost, good-quality films, and relative ease in controlling the film properties. The early attempts to deposit silicon films by CVD at temperature of about 1000°C used the hydrogen reduction of silicon tetrachloride (SiCl_4) and dischlorosilane (SiH_2Cl_2). However, these methods generally produced heavily doped *p*-type films as well as substantial chemical attack of the sapphire substrate. The chemical attack is believed to be caused by the formation of HCl during the reaction:

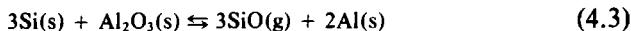


which can then attack the sapphire substrate at temperature of 1050°C or so by the following reaction:



The incorporation of aluminum into the growing silicon film is then achieved via a gaseous doping source leading to *p*-type films. When silane (SiH_4) is used as a deposition source it is found that the chemical attack is greatly reduced, and there are no deleterious reaction by-products. In addition, it was found that silicon films could not be deposited at much lower growth temperatures thereby improving the film quality. Hence, by reducing the deposition temperature and going to a higher deposition rate, it is possible to reduce the chemical attack to below detectable levels and thereby obtain very high-resistivity films attesting to their high purity.

Under nonideal growth conditions and at high temperatures, the silane method can also produce autodoping of the silicon films via the reaction:



This reaction has been proposed to explain the *p*-type autodoping which is present at high (1000°C or higher) growth temperatures.

Ultrahigh-purity hydrogen, nitrogen, and silane are the three main components typically used in a CVD reactor, thereby assuring minimal contamination of the system. The silane as well as dopant gases such as arsine (AsH_3) and diborane (B_2H_6) are generally prediluted with hydrogen in the proper ratio to obtain the desired growth rate and resistivity.

A typical growth process consists of a high-temperature (~1150°C) hydrogen prefire of the sapphire substrate for surface passivation and heat cleaning followed by decomposition of silane in hydrogen at a reduced temperature of 900–1000°C. The deposition rate typically varies from about 0.1 $\mu\text{m}/\text{min}$ to over 3 $\mu\text{m}/\text{min}$. After growth, the wafers are typically cooled slowly to room temperature in a hydrogen atmosphere and then screened nondestructively for quality control.

Several different reactor chamber designs have been used for SOS epitaxy, and the major ones are shown in Fig. 2. The simple pedestal

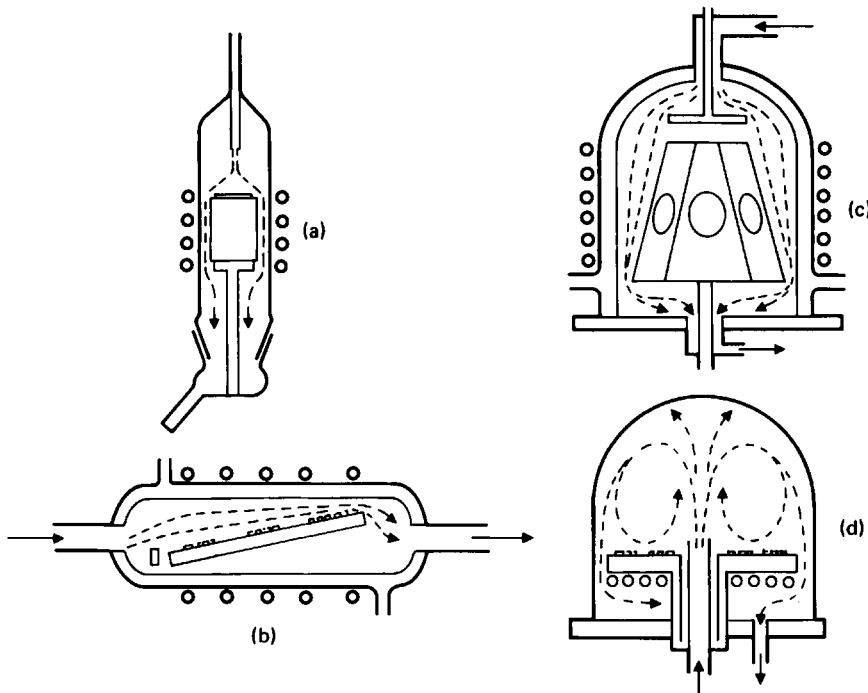


FIG. 2. Reactor chamber designs for chemical vapor deposition (CVD) of SOS films.

system shown in Fig. 2a is the standard system for research and development laboratories and minimizes many of the contamination problems of the larger systems. The horizontal reactor shown in Fig. 2b has been used extensively for silicon and SOS epitaxy, and the gas flow kinetics have been extensively investigated. The vertical reactor design shown in Fig. 2c has also been employed for some commercial applications but has generally produced films with an undesired thickness gradient due to improper gas flow hydrodynamics over the substrate. To achieve good thickness uniformity for films with thicknesses of 0.5 μm or below, it becomes vital to control the gas flows and deposition kinetics over the sapphire substrate. Consequently, the system best suited for these requirements uses the pancake configuration shown in Fig. 2d. These reactors are presently the most common commercial deposition systems for SOS due to their excellent thickness uniformity and dopant uniformity. This feature is further aided in the pancake reactor because the sapphire substrates can be rotated in the gas stream, and there is a relatively high degree of gas-phase turbulence in the chamber. As mentioned previously, it is generally desirable to deposit silicon at a high growth rate and at a relatively low temperature to minimize the sapphire-silane interaction.

The growth of silicon epitaxial films on sapphire substrates is typically dominated by the events occurring during the initial stages of deposition. The final crystal quality also generally tends to be strongly coupled to the nucleation and layered growth that occurs during the early stages of deposition. Consequently, a number of workers have used a variety of techniques such as transmission electron microscopy (TEM) to study the kinetics of silicon epitaxy during the early stages of growth. The most detailed work has been reported by Abrahams, *et al.* (1976) and the modeling work by Blanc and Abrahams (1976). The key results on the nucleation and growth of silicon islands at two different deposition temperatures are illustrated by plan view TEM photographs in Fig. 3. Here, it is clearly seen that at the lower growth temperature (1000°C), the sapphire surface is covered by a dense population of silicon islands during the first 0.5 sec of growth. At the higher temperature (1100°C), the nuclei are less dense in number but larger in size. This is primarily due to surface diffusion which tends to induce coalescence of the silicon thereby increasing the size of nuclei. As growth proceeds, the nuclei which are present at several sites, appear to grow in size and coalesce with time until they eventually cover the substrate. The striking difference between the surface morphology of the films after 4 sec of growth between the two different deposition temperatures is clearly evident in Fig. 3. Due to the larger-sized nuclei and a lower density at the higher growth temperature, the films appear more grainy and show the appearance of growing silicon islands which

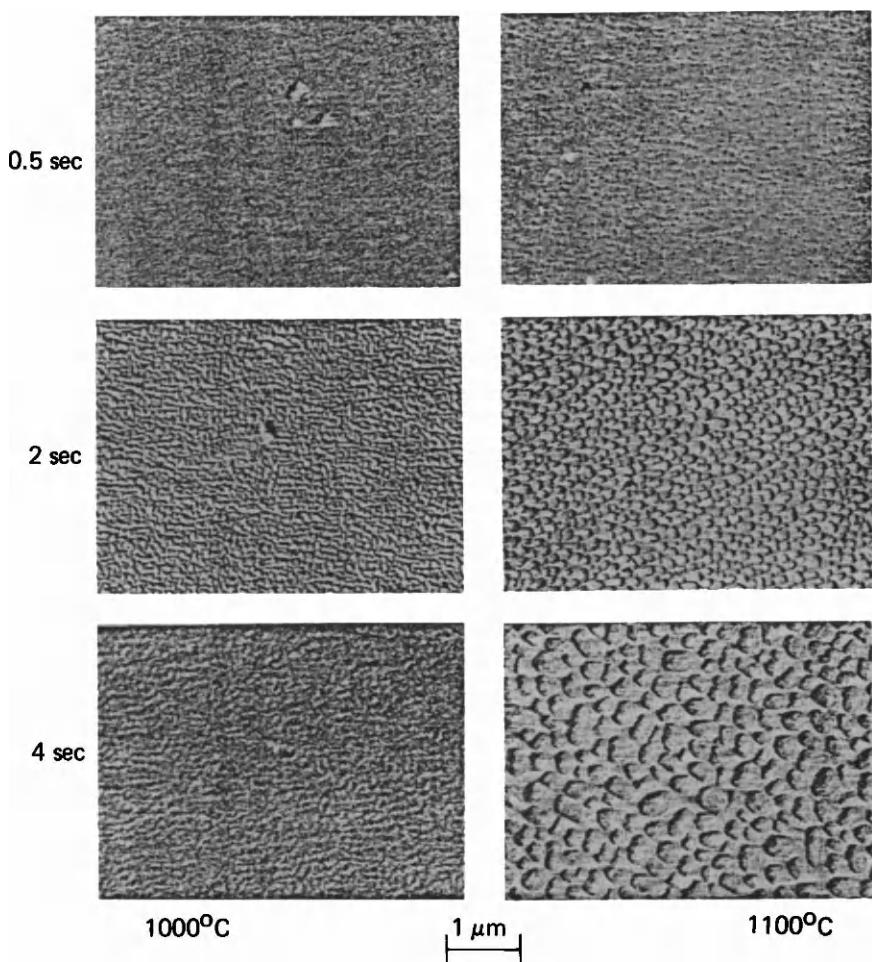


FIG. 3. Plan-view transmission electron micrographs of silicon nuclei of sapphire substrates during the initial stages of growth.

eventually coalesce into a film with a rough surface texture. By contrast, the lower deposition temperature produces a smoother topography due to the smaller sized nuclei which are also in a higher density across the surface.

Based on these observations, we can model the epitaxial growth of silicon on sapphire as the nucleation of silicon islands and their eventual coalescence with time. This is illustrated in a time sequence in Fig. 4. The nuclei are generally a mixture of both (100) and (110) oriented crystallites. As growth proceeds along the (100) direction, the (110) domains become

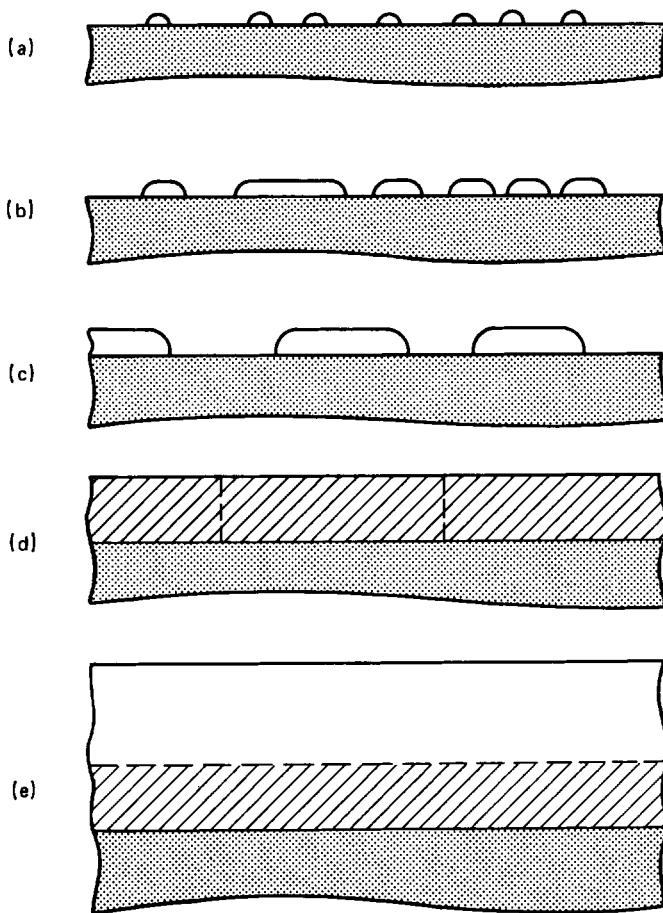


FIG. 4. Schematic of heteroepitaxial growth of silicon films of an insulating substrate.

trapped and eventually get covered by (100)-oriented material. The interface region of an SOS film is thus unique and contains both (110)- and (100)-oriented silicon. As the silicon islands coalesce, stacking faults occur at the island boundaries, and as the fault process is repeated in the (111) direction, microtwins result. Consequently, the interface region of the SOS film is dominated by a high density of unique crystallographic defects such as stacking faults, microtwins, and dislocation arrays. Due to the dominance of the (100) growth matrix with increasing film thickness, it is expected that the defects would decrease with distance away from the silicon sapphire interface. This, in fact, is what occurs and has been clearly observed by high-resolution techniques such as cross-sectional transmis-

sion electron microscopy (XTEM). The technique was originally described by Abrahams and Buiocchi (1975). A typical XTEM micrograph of the silicon sapphire interface region taken at Hughes showing the defect structure is shown in Fig. 5. Here, the dark areas are the primary defects present in the silicon matrix which is shown by the white background. As can be seen, the stacking faults traverse at an angle through the entire film thickness along a (111) growth direction as expected. Very close to the sapphire interface triangular defect regions with a very high density are present in the film. These are the microtwins.

The spatial variation of these crystallographic defects within the silicon film can be determined quantitatively from the XTEM data, and the results are shown in Fig. 6. The results of both Abrahams and Buiocchi (1975) and Linnington (1976) clearly show that the fault density is as high as

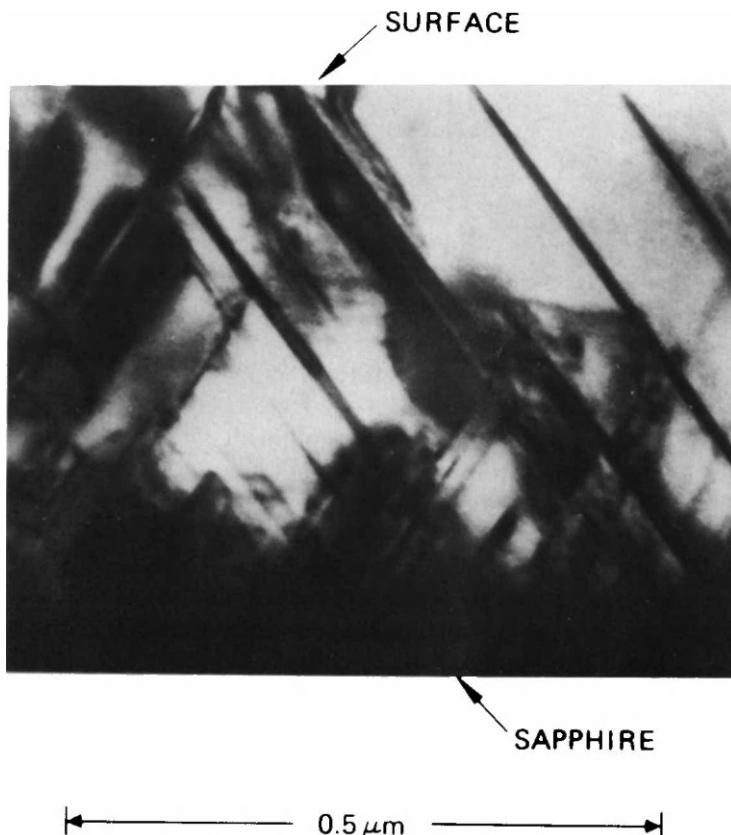


FIG. 5. Cross-sectional transmission electron micrograph of an As-grown silicon-on-sapphire (SOS) film.

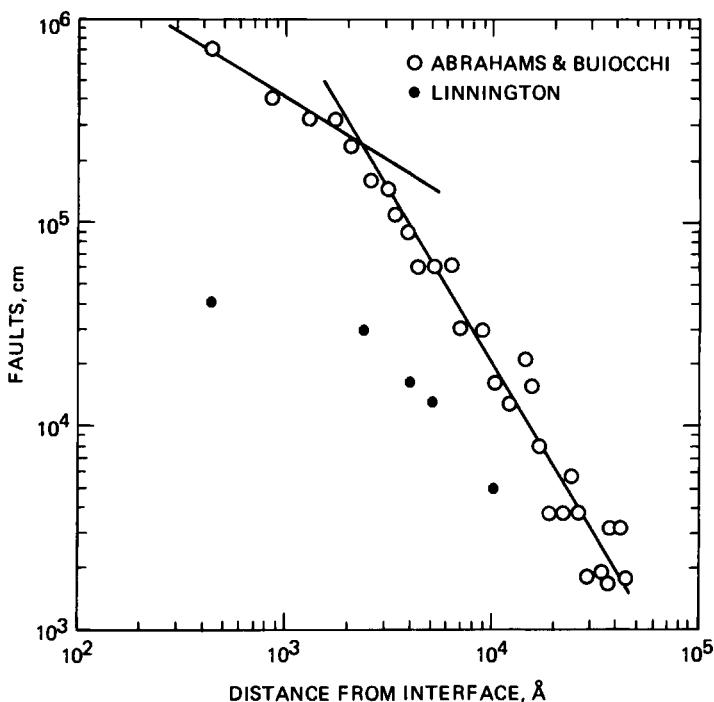


FIG. 6. Spatial defect density profile of microtwins across the thickness of a 0.5 μm silicon-on-sapphire (SOS) epitaxial layer.

$10^6/\text{cm}^3$ near the interface and falls off to $10^3/\text{cm}^3$ at the silicon surface in an exponential dependence with depth. We have been able to correlate this spatial variation in defect density with depth with corresponding electrical measurements of carrier lifetime made in our laboratory using gated MOS devices. The typical variation of minority carrier lifetime with depth for an as-grown SOS film is shown in Fig. 7. Here, we notice that, in excellent agreement with the XTEM data, the lifetime degrades exponentially from about 40 nsec near the surface of the silicon film to less than 0.1 nsec near the sapphire interface. This not only attests to the electrical activity of the crystalline defects in the SOS film but also shows that they behave as recombination centers due to their strong effect on carrier lifetime. Thus, it is expected that the defects produce electrical states very near the midgap region of the silicon and can cause generation-recombination of carriers rather than affecting the type of resistivity of the film.

Several studies on the variation of key film properties of SOS films deposited by CVD have been conducted and have led to significant improvements in the material quality and uniformity. The radial variation of

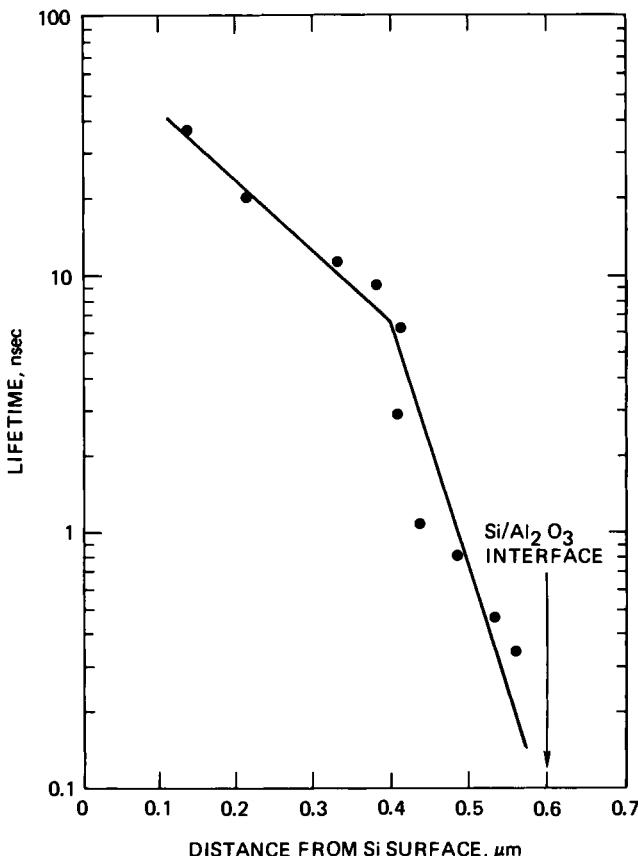


FIG. 7. Spatial variation of minority carrier lifetime with depth in a SOS film determined from gated diode analysis.

thickness in 0.5- μm SOS films at three different growth rates is shown in Fig. 8. Here, we notice that for all three growth rates, the thickness uniformity improves as the growth temperature is lowered, and, in fact, the most uniform films are produced at growth temperature of between 875 and 900°C. Another important characteristic of the SOS film is the surface roughness or haze as measured by the specular reflectance of the silicon surface in the ultraviolet region of the spectrum. The variation of this ultraviolet reflectivity at a wavelength of 280 nm is shown in Fig. 9 for a large number of SOS films as a function of various growth rates at different temperatures. Consistent with the previous data, we see that the films show the lowest reflectivity, corresponding to the lowest surface roughness, at a temperature of around 910°C. This temperature appears

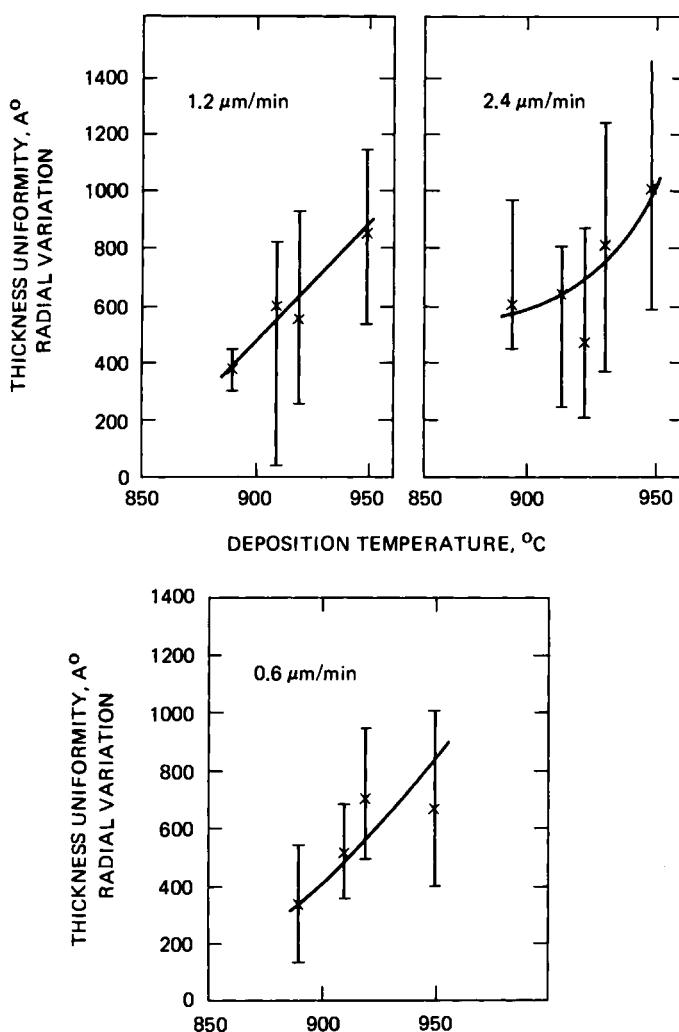


FIG. 8. Variation of silicon epitaxial thickness uniformity with growth temperature for various growth rates.

to be optimum for producing the best SOS films at all three growth rates. For both higher and lower deposition temperatures, it appears that the films become rougher, and, in general, this is indicative of poorer crystalline quality. The corresponding variation of the film electrical quality with growth temperature is shown in Fig. 10. Here, we show the radial variation of the resistivity of undoped SOS films deposited at various temperatures from 850 to over 1000°C. As was pointed out earlier, the lower growth

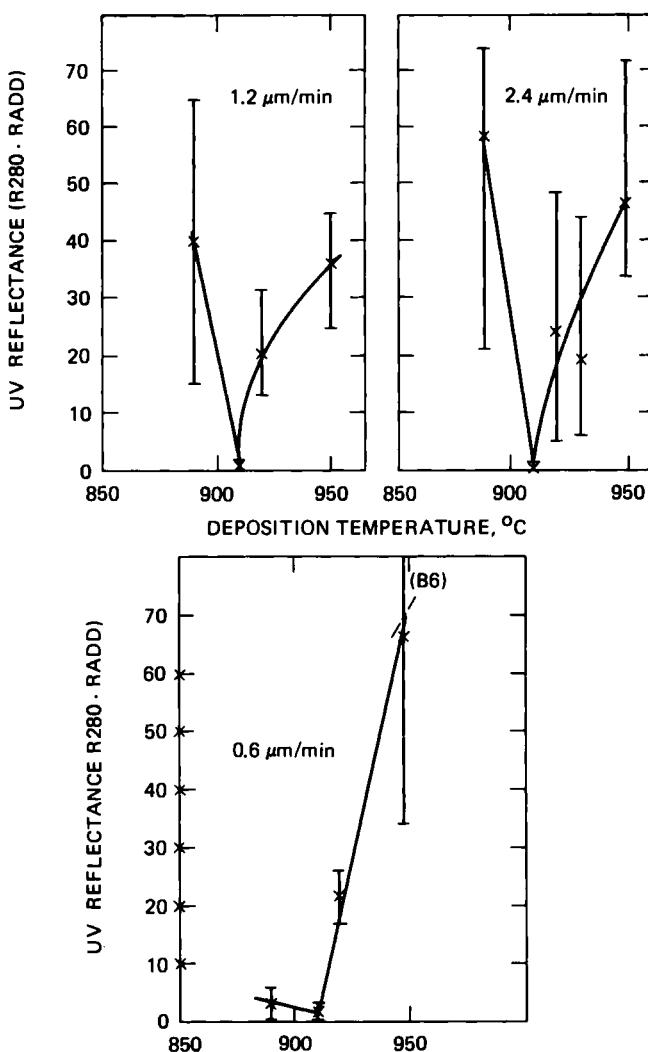


FIG. 9. Variation of ultraviolet reflectance with growth temperature of SOS films at various growth rates.

temperatures tend to suppress the reaction with the sapphire substrate, and the undoped films are thus of high resistivity uniformly across the entire 4-in. wafer. As the temperature of deposition is increased, however, we notice a falloff in the resistivity near the edges of the SOS film, and this tends to proceed inward with increasing deposition temperature. Finally, at the very high deposition temperatures near about 1000°C, we observe a drastic reduction in film resistivity due to autodoping from

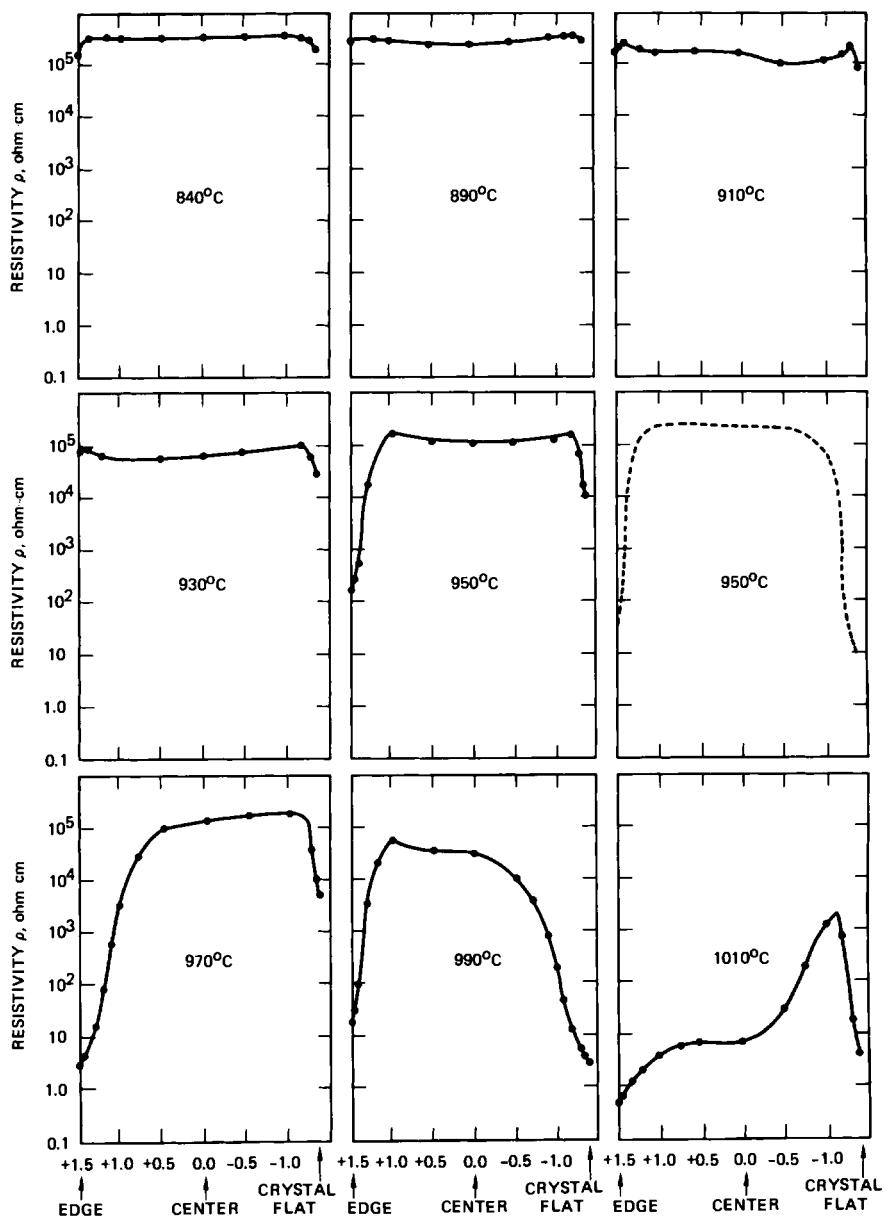


FIG. 10. Variation of spatial resistivity profiles of SOS films deposited at various growth temperatures.

aluminum that is being produced by the silane/sapphire reaction. The edges tend to show this effect in a more pronounced way than the center because of the temperature and film thickness variations, which tend to cause the sapphire edges to be exposed to the reactants for a longer time than other regions of the wafer.

The fact that the lowered resistivity is due to aluminum autodoping and not gas purity is shown by results from a chemical analysis of the SOS films shown in Fig. 11. Here, we show our results of analyzing the aluminum content of SOS films by secondary ion mass spectrometry (SIMS) compared to high-purity bulk silicon for SOS films grown at two different growth temperatures. At the lower temperature, we notice that the silicon sapphire interface is sharp with no evidence of excess aluminum present. Although the background level in the silicon film is about $10^{15}/\text{cm}^3$ compared to about $10^{14}/\text{cm}^3$ for the bulk silicon, this variation is within the limits determined by the instrument sensitivity. For the SOS films grown at temperature close to 1000°C , we notice that the silicon matrix signal at mass 30 falls off deeper than the aluminum signal at mass 27. This clearly indicates the presence of a thin aluminum skin near the silicon sapphire interface due to autodoping from the substrate. Thus, the main contribution to the resistivity decrease is the outdiffusion of aluminum from the sapphire substrate.

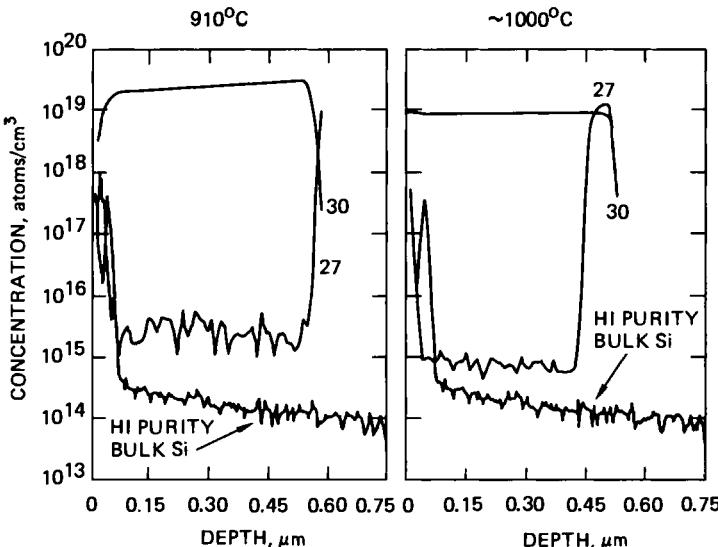


FIG. 11. Depth distribution profiles of ^{27}Al and ^{30}Si in SOS films by secondary ion mass spectrometry (SIMS).

4.4 SOS MATERIAL DIAGNOSTICS

The reliable and reproducible characterization of SOS films for device applications requires specialized techniques and nonstandard measurement procedures due to the complex interrelationship between the crystal structure of the film and its electrical properties. By the very nature of the film structure and growth techniques used, the electrical properties of SOS are dominated by material properties such as crystalline defect density, stress gradients in the film, and autodoping effects of impurities from the sapphire substrate during growth. These arise primarily due to the effects of lattice and thermal expansion coefficient mismatch between the silicon and sapphire leading to large compressive stresses and defects being induced into the film when the silicon crystal is cooled down from its deposition temperature to room temperature. In addition to the complex structural quality of the films, there are two abrupt changes in the chemical composition at the top and bottom interfaces. This compositional gradient creates a large perturbation in the band structure and, for material within a Debye length of both interfaces, there is a gross disruption of ideal electronic transport properties in the film such as resistivity, mobility, and lifetime. Unless special precautions are taken, the measured properties of SOS films are thus bound to be dominated by the effects of the surfaces and can lead to misleading information. The effect of surfaces is much stronger than the simple addition of surface scattering terms to the mobility, since the surface fields extend well into the material and can often entirely deplete the total film thickness. In addition to the strong surface effects, it is usually found that the film structure and electrical properties vary strongly with distance from the substrate. Consequently, it is vital to characterize the film properties as a function of depth into the material in order to accurately assess its device properties. This often requires the development of gated device structures which can vary the conducting portion of the film in a controlled manner.

It is usually desirable to characterize the film electrical properties using simple, reliable and nondestructive measurements. However, due to the unique set of problems encountered in virgin SOS films, such as unstable surfaces, high resistance contacts, and band bending due to interface charges, there is no single set of measurements that can be used for reliably evaluating the electrical characteristics of the film. Consequently, the only reliable approach is to characterize the physical structure of the material nondestructively by suitable optical, analytical, or X-ray measurements and correlate them with electrical measurements on device structures processed on the same substrates. The fabrication of the device structures

with properly passivated surfaces and doped regions overcomes the problems of electrical measurements and their interpretation. Although this approach involves extra effort to fabricate special device structures, they are very useful in determining the properties of the SOS film after some processing has occurred. It is these which are most relevant for the ultimate device application of the SOS film.

The crystallographic characterization of the SOS film on a routine basis also requires the use of techniques that can sensitively and nondestructively detect the crystalline structure. Since the SOS films typically show a large gradient in both defect density and crystallinity across the film, the techniques should be capable of either averaging over the entire film, or profiling the film structure selectively. There are a variety of possible approaches for the crystallographic characterization of the SOS films, such as UV reflectance, transmission electron microscopy, X-ray structure analysis, Raman spectroscopy, and Rutherford backscattering spectroscopy. Each technique has its limits of applicability and unique characteristics in providing crystallographic information. In the characterization of silicon films grown on off-axis substrates, we need to employ techniques that can detect small changes in crystallinity, especially near the silicon sapphire interface, as a result of small but controlled changes in the misorientation of the sapphire substrate. Although the TEM (cross-sectional and vertical) is the most comprehensive and detailed approach for the crystallographic characterization, it is not convenient to apply on a routine basis for the screening of a large number of films. Nevertheless, its use is invaluable when used selectively in detecting small crystalline changes of the silicon sapphire interface.

Of the various nondestructive characterization methods attempted, several key techniques have been selected by our experience as being promising for the evaluation of the structural and electronic quality of the various SOS films prior to device processing. These techniques consist of pole figure analysis, electron channeling, and Rutherford backscattering. They are best suited for providing a quantitative measure of crystalline perfection for correlation with parametric test data and device performance. Another important—although limited—characterization technique is UV reflectance. Each of these is discussed here.

4.4.1 UV Reflectance

Several studies performed at Hughes and RCA have shown that UV reflectance is indispensable as a rapid quality assurance tool for the assessment of SOS film quality and reproducibility as indicated by the

"haze" or surface roughness. However, when films show zero UV reflectance or very small surface scattering compared to bulk silicon, the technique loses sensitivity to crystalline perfection. This behavior is seen in Fig. 12, which compares the UV reflectance spectra for a variety of SOS films and bulk silicon. It is seen that the reflectivity of films containing "no haze" is identical to bulk silicon even though they differ substantially in crystallinity, whereas with heavy-haze the reflectivity of the film drops. Consequently, other techniques have been developed and refined at Hughes which, although more time consuming, are better indicators of the film crystalline quality, especially when the UV index is zero or negative.

Figure 13 shows the excellent correlation between the microtwin density and UV reflectance index on films grown with different growth rates. The samples were specially prepared at different epi deposition conditions, to evaluate the sensitivity of the UV reflectance index. The excellent correlation provides the basis for using UV reflectance. The UV technique is based on the attenuation of the reflected energy in the range of 2 to 5.5 eV due to structural disorder in silicon. The reflectance of silicon at a photon energy of about 4.4 eV (2800 Å) is influenced by both surface topographical imperfections and the lattice disorder due to X_4-X_1 transition; whereas, the reflectance at a photon energy of 3.1 eV (4000 Å) is primarily due to surface scattering. The UV reflectance technique consists

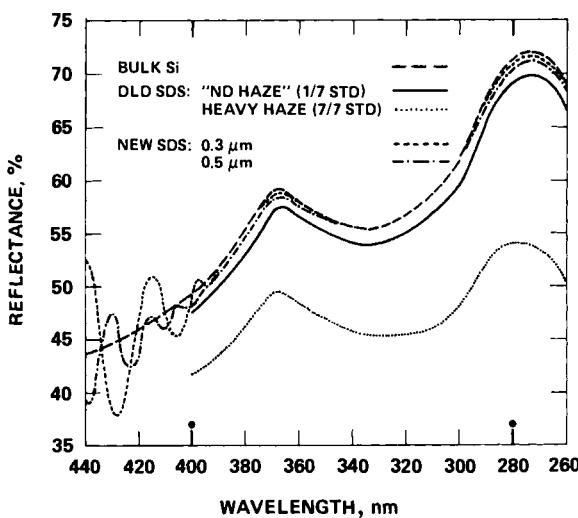


FIG. 12. Variation of surface reflectance (in the UV region) versus wavelength for various SOS films compared to bulk Si.

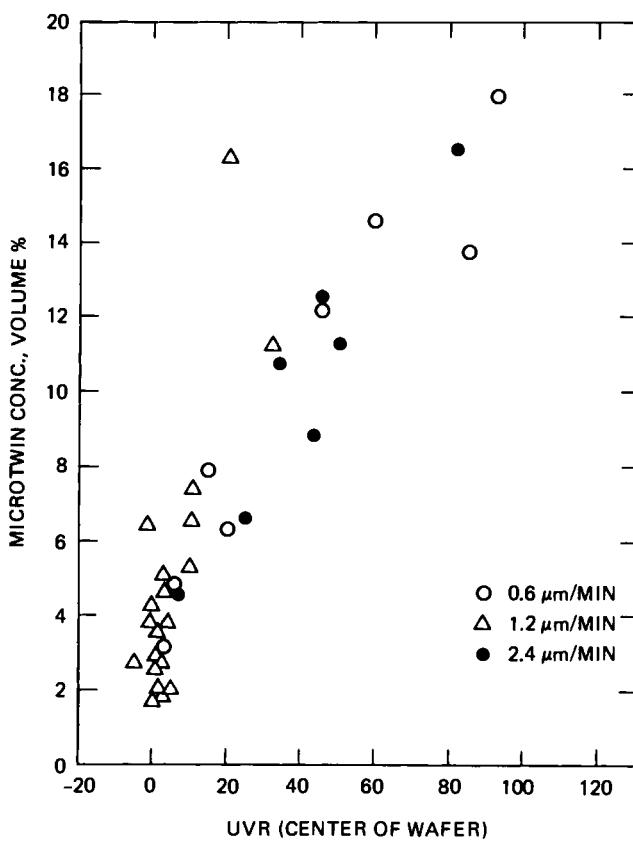


FIG. 13. Correlation of microtwin density of various SOS films with their corresponding ultraviolet reflectance.

of measuring the reflected intensities at two discrete wavelengths of 2800 Å and 4000 Å, rationing them to corresponding values for an ideal bulk silicon reference, and taking the difference. The resulting UV reflectance index is an indication of the surface crystallinity and roughness. A large value represents a poor-quality material whereas a zero value represents a good-quality material. The reference wavelength of 4000 Å avoids optical interference effects from the sapphire substrate for epitaxial silicon thicknesses greater than 5000 Å. The penetration depth in silicon at 4.4 eV is <100 Å, and this technique primarily evaluates a very thin surface region. Its major applications are in providing a rapid material evaluation prior to device fabrication and in quality control screening for 100% wafer inspection.

4.4.2 Electron-Channeling Spectroscopy

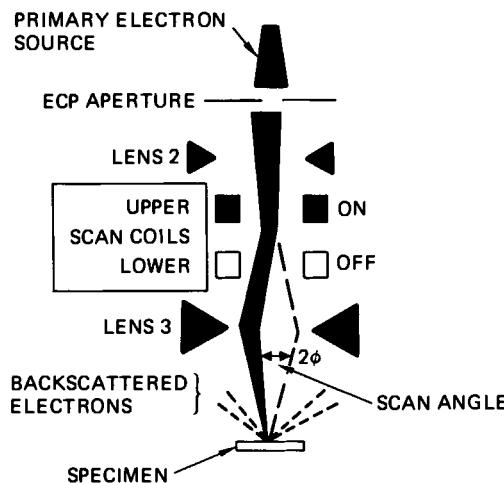
This is another useful nondestructive technique for evaluating the crystalline quality and has been applied to SOS by Vasudev (1982). The measurement is performed in a standard scanning electron microscope. The scan coils are adjusted such that an incident 20 keV electron beam “rocks” in a vertical plane about its focal point. The electron beam penetrates the specimen at different angles during a scan. This produces secondary and backscattered electrons from a shallow surface region ($\sim 500 \text{ \AA}$ in depth) with specific angular distribution and intensity depending on the crystalline perfection and orientation of the specimen. The spatial distribution results in the Kikuchi diffraction pattern consisting of intensity contributions from both low-index planes and some permitted high-index planes which satisfy the Bragg diffraction condition.

Figure 14 shows the typical measurement schematic in an SEM and the ideal backscattered electron intensity as a function of angle, during a line scan along the $\langle 110 \rangle$ direction for a perfect (100) oriented cubic crystal. There is a sharp change in intensity corresponding to exciting a channeling or dechanneling wave in the crystal at angles satisfying the Bragg condition. The sharpness of these transitions and the peak-to-peak intensity is a sensitive indicator of the crystalline perfection of the crystal. The (440) and $(\bar{4}\bar{4}0)$ reflections show changes in the peak-to-peak intensity (electron channeling index) ranging from 3.5 for bulk silicon to 1.54 for high-quality SOS films and 0.2 for medium-quality SOS films. These differences are significantly larger than the corresponding UV reflective indexes of these films, indicating a high measurement sensitivity.

Typical diffraction patterns for a SOS film with varying thicknesses are shown in Fig. 15. It shows the electron channeling diffraction patterns corresponding to the variations in electron intensity during a line scan. The thickest SOS film has a considerable amount of fine structure in the line scan which is similar to the bulk silicon reference but with lower intensity. With a decrease in SOS film thickness, the intensity is reduced as well as the higher order peaks are either broadened or are absent due to degradation in the film crystalline quality. This technique appears very promising and has an advantage that crystallinity can be determined non-destructively. The measurement can also be used as a quantitative index.

Figure 16 shows the variation in the electron channeling index (ECI) [which refers to the peak-to-peak intensity of a $((440))$ reflection normalized to bulk silicon] with depth into various SOS films. The films were selectively etched in 500 \AA steps down to the sapphire substrate to allow “profiling” of the crystallinity with depth. It is seen from the figure that in all the films there is a large drop-off in the ECI numbers as we approach

- SCANNING ACTION IN A SEM
DURING CHANNELING MODE



- BACKSCATTERED INTENSITY
VERSUS SCAN ANGLE (LINE SCAN)

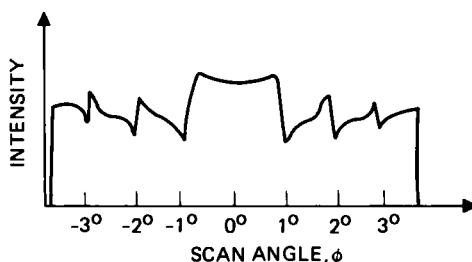


FIG. 14. Schematic of the scanning action in a SEM and the backscattered electron intensity patterns during electron channeling spectroscopy.

the back interface. This is consistent with all other structural characterizations since it indicates that the twin density increases as we approach the sapphire interface. It is seen that film D shows the lowest ECI number near the surface and also at the sapphire interface due to its large defect density. In addition, we see that the double solid-phase epitaxy (DSPE) SOS shows the highest ECI numbers at the surface and interface due to its very low twin content relative to the other films. Among the as-grown SOS films, film B appears to have the lowest twin content consistent with other data.

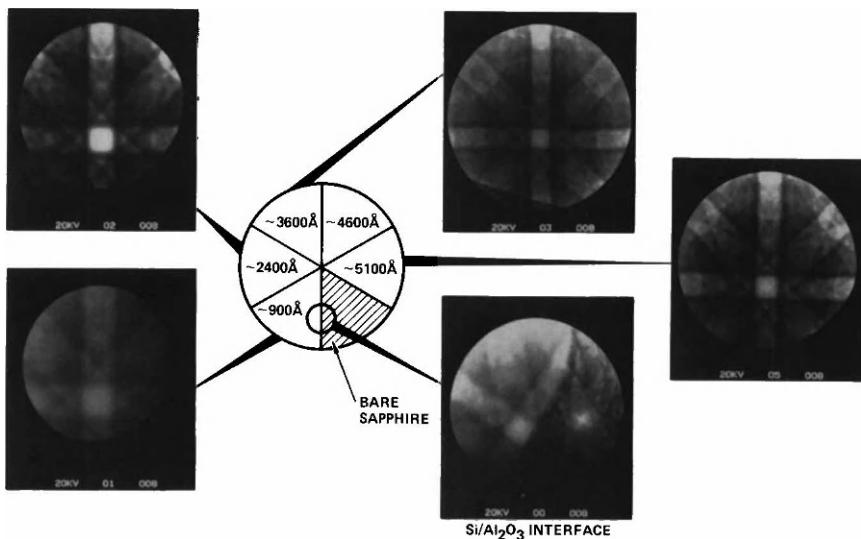


FIG. 15. Variation of electron channeling diffraction patterns with depth into a typical silicon-on-sapphire epitaxial film.

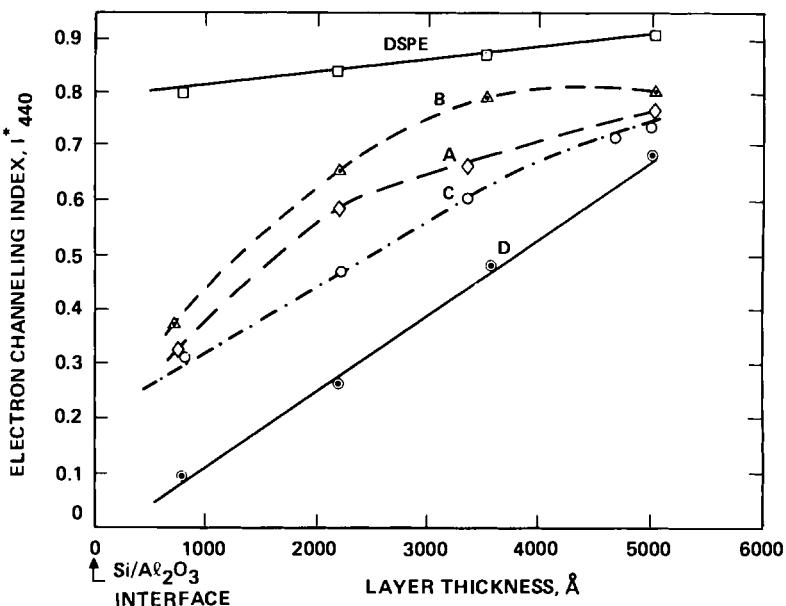


FIG. 16. Spatial variation of electron channeling index with depth for a variety of SOS films with widely varying defect content.

A major attribute of the electron channeling spectra is that it allows us to profile the crystalline quality of the film with depth. This selective etching of the film can be used very effectively during wafer processing to produce a simple electron channeling test pattern consisting of etch steps for subsequent characterization of crystallinity under SEM examination. However, the channeling index at the surface is still a sensitive measure of the crystalline perfection of the SOS film and can be mapped across a wafer for spatial uniformity.

4.4.3 Rutherford Backscattering Spectra

Rutherford backscattering (RBS) is a sensitive technique for characterizing the crystallinity of thin films. It consists of measuring the number of backscattered ions or yield from a crystal that is oriented in a specific direction and bombarded with a beam of light ions such as He^{2+} with energies of 1–3 MeV. By measuring the number of backscattered ions in both the “random” and “aligned” orientations, the defect distributions in the film can be quantitatively assessed. By translating the wafer in an “aligned” orientation RBS scanning can be used to examine spatial uniformity.

Figure 17 shows typical RBS spectra measured on a number of SOS films including a typical spectrum obtained from high-quality bulk silicon

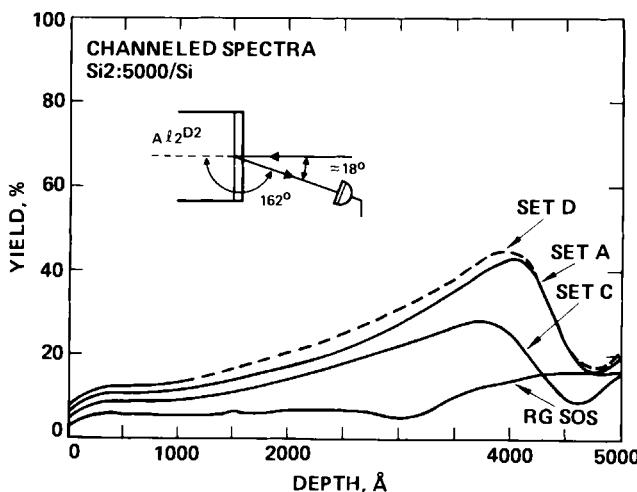


FIG. 17. Rutherford backscattering profiles versus depth for various SOS films with varying twin density.

crystal. It is seen that generally the channelled yield monotonically increases with depth into the film, reaching a maximum at the sapphire interface and then has a sharp dropoff where the silicon film is terminated. The RBS yields of the various SOS films typically range from about 10–12% near the surface to about 45–50% at the sapphire interface. By comparison the bulk silicon and solid-phase recrystallized SOS yields range from 3.2 to 4.2%. The results shown in the figure indicate that excellent correlations can be obtained by comparing the RBS yields at the sapphire interface with either the ECI index or pole figure twin density. Consistent with the previous observations, we see that film D shows the highest RBS yield of 56% at the sapphire interface due to its highest twin density. In addition, the regrown SOS (marked RGSOS) shows the lowest RBS yield near the interface among the SOS films due to its vastly reduced defect content. It is also seen that the yield is much more uniform with depth in the regrown film due to a lower dechanneling.

It is apparent from these comparisons that good cross correlation is obtained between the various structural characterization techniques for the films examined even when the UV index is the same for all and that the latter three techniques are capable of differentiating between films with a poor structural quality (resulting from a high twin density) and those with good crystallinity. This is important for the performance and yield of devices and circuits. Moreover, all three structural diagnostic techniques show promise for providing depth distribution of defects, although only ECP can be done on a routine and nondestructive basis. The spatial variation of defects and twin density across the wafers can complicate interpretation of data and comparisons especially since ECP is a very local "probe" compared with X-ray analysis. However, it can be easily implemented in a scanning mode to study spatial uniformity.

4.4.4 Electronic Characterization

The assessment of the quality of SOS material prior to device fabrication is essential in obtaining high yields and good device performance. The analytical techniques discussed previously measure structural characteristics of the film but do not measure the electronic transport properties of the films.

One potentially powerful method for evaluating the film electronic quality is the Hall-effect measurement as a function of temperature. Its direct application to undoped 0.5- μm SOS films is hindered by difficulties such as surface depletion effects, contact resistance, and inhomogeneities. Hughes has developed both high- and low-temperature Hall measurement techniques which circumvent these difficulties. By examining a large num-

ber of films with vastly different structural characteristics, we find that although the effective high-temperature Hall mobility of carriers at temperatures around 400 K is sensitive to the crystallinity of the film, the method loses sensitivity for films with small variations in twin density. This is because the mobility is affected by both strain and defects, but since strain is the more dominant influence, the high-temperature Hall effect does not vary significantly between SOS samples with relatively small differences in twin content.

However, we have achieved good success using low-temperature Hall measurements made on SOS films when doped by ion implantation of boron or phosphorus. The implant energies are chosen so as to produce a peak in the dopant profile near the silicon sapphire interface, where the mobilities are generally very low due to the high defect density. This allows the dominant conduction region to be at the silicon sapphire interface, a location which is essential for assessing the film quality. The deep implants used are also typical of device implants and, hence, allow for correlation between device mobilities and Hall mobilities. The use of a doped film minimizes surface depletion and contact resistance effects and allows measurements to be made down to 20 K. Figure 18 shows typical data of the measured Hall carrier mobility from phosphorus doped SOS films as a function of temperature. As the temperature is lowered, the carrier density decreases exponentially. The measured activation energy of the various films does not appear to correspond to the phosphorus energy level in bulk silicon but appears deeper suggesting that the energy level may have been shifted in SOS films due to stress effects or that ionization is occurring from a deeper impurity in the film. Corresponding to this variation, we see from Fig. 18 that the Hall mobility of electrons goes through a maximum at 200 K and decreases at a rate of approximately $T^{3/2}$ following a charged impurity scattering model. This low-temperature mobility maximum is found to be a sensitive indicator of the film quality ranging from under 50 cm²/V sec for the type-D films to over 400 cm²/V sec for the type-B films. This correlates well with the structural characterizations which have already shown that D-type films had the highest twin density near the sapphire interface. From Fig. 18, we also see that the carrier density of the type-D film is the lowest and also shows a much more rapid falloff with lowered temperature. Since all the films were doped with identical implants and were annealed under identical conditions, the varying carrier concentration, especially near room temperature, is directly correlated with activation efficiency of the phosphorus ions in the SOS films. By comparing the total integrated sheet carrier concentration with the integrated implanted dose in the silicon, it was found that the electrical activation efficiency varied from under 50% for the type-D film

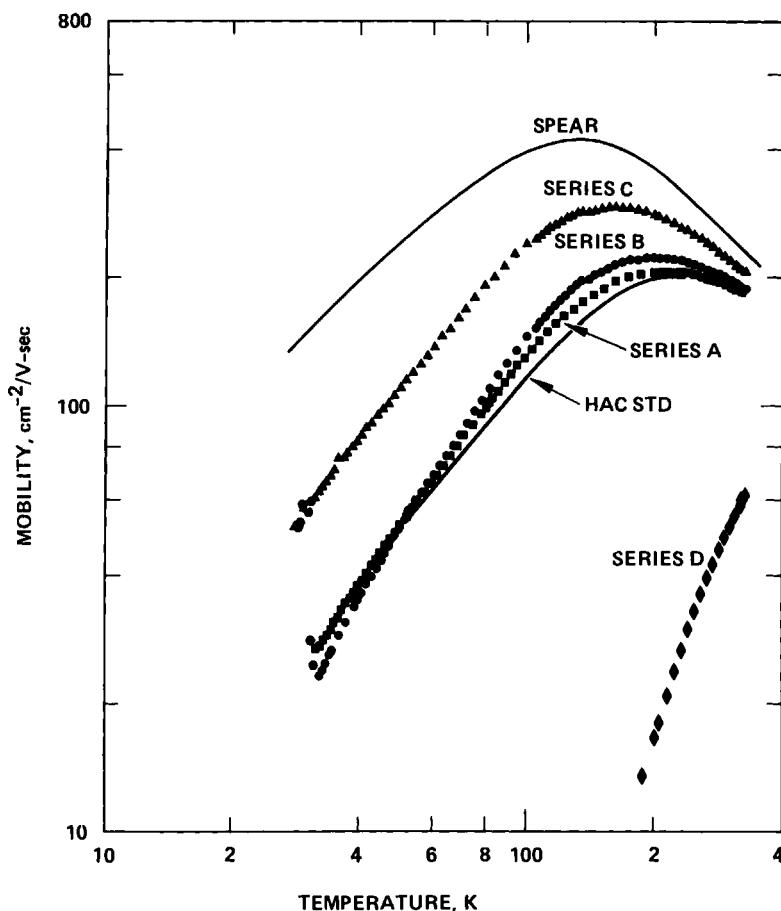


FIG. 18. A comparison of the temperature dependance of Hall mobility for various N-type SOS films with varying twin content.

to over 99% for the type-B and solid-phase epitaxy and regrowth (SPEAR) films (similar to bulk silicon).

It appears that the high twin content in the films leads to a lower activation of phosphorus ions due to redistribution or "gettering" of the phosphorus in the defect regions. This behavior has been confirmed by independent SIMS measurements which have shown a large pileup of phosphorus at the sapphire interface where the twin density is at its maximum value. Hence, it can be seen that the use of low-temperature Hall measurements on doped SOS is a sensitive and meaningful method for distinguishing between films with a high twin content and low twin content. In addition, even for films with similar twin content values, slight

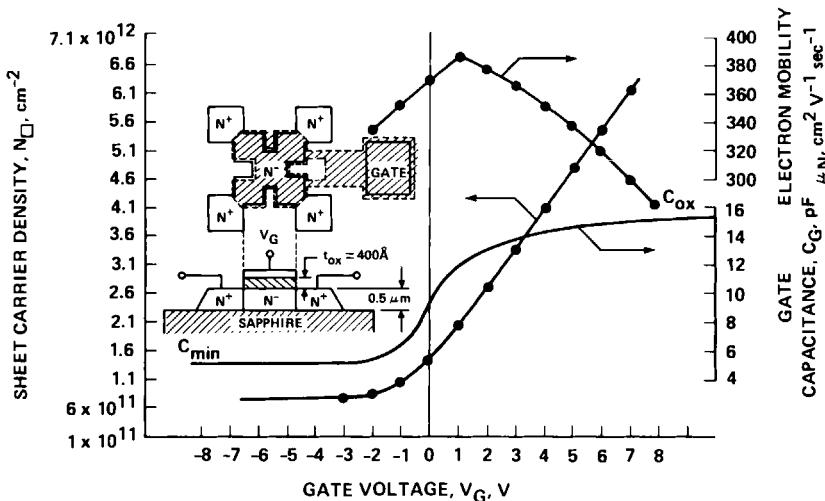


FIG. 19. MOS (grated) Van der Pauw measurements for determining the spatial variation of channel mobility with depth in SOS films.

differences are seen in the peak mobilities and activation efficiencies, which correlate well with the twin density variations in the respective SOS films measured by electron channeling or pole figure analysis. The variation of MOS channel mobility with the gate voltage or depletion into the film is shown in Fig. 19. It shows the decrease in mobility with depth into the film as expected.

4.4.5 Chemical Analysis

The analysis of residual impurities such as aluminum, carbon, oxygen, and heavy metals in SOS films using SIMS and Auger electron spectroscopy (AES) is very important for monitoring the background contamination level in the SOS films. Detecting low levels of aluminum in SOS is difficult due to sapphire dust and charging effects, which often give erroneous results. Special procedures have been developed for sample preparation and instrument conditioning that have allowed detection of aluminum to levels below $10^{15}/\text{cm}^3$ as described by Robertson and Vasudev (1980). We have achieved over two orders of magnitude improvement in detection sensitivity in the SOS, and final levels are close to bulk silicon. This high-sensitivity detection of aluminum in SOS is very important for process control, especially following ion implantation steps, to ensure that undesirable device properties such as high leakage currents are not being induced by excessive aluminum.

4.5 SOS DEVICE TECHNOLOGY

In contrast to bulk silicon technology, where the active channel regions are isolated by field oxide, SOS technology has also employed an alternative simple approach of mesa isolation where the patterned silicon islands are isolated by air on the sapphire substrate. This has resulted in a high radiation tolerance for military applications, due to the absence of a thick field oxide at the edge of the silicon island. However, the fabricated devices have shown low gate oxide breakdown field strength due to a combination of V-groove formation in the gate oxide in the vicinity of the sapphire substrate and the rough surface texture of the silicon island edge. Recent advances have eliminated the problem by modifying the edge profile. In addition to high gate oxide breakdown field strength, field isolation planarizes the surface topography, which is advantageous for photolithographic patterning, etching and metal step coverage. However, the control of the edge doping becomes critical, and it requires high-temperature field oxidation which reduces the packing density. The choice between the two techniques partly depends on whether the application is for commercial or military markets.

Several CMOS/SOS processes have been developed with both mesa-isolation and field-isolation approaches and feature sizes ranging from 0.5 to 2.0 μm . Figure 20 shows typical current-gate voltage characteristics of a 0.5- μm channel length, *p*- and *n*-channel devices. An SOS transistor has three conducting regions in parallel; the top surface and the bulk silicon film (I), the silicon island edge (II), and the silicon surface near the sapphire interface (III). Regions (I), (II), and (III)/(II) primarily contribute to the subthreshold, edge, and back-channel leakages, respectively. Furthermore, the back-channel leakage consists of junction leakage and leakage due to surface states in the sapphire. The leakage components can be separated easily by electrical measurements on edged, edgeless, and gated devices. The back-channel leakage is typically 1.8 and 2.3 $\text{pA}/\mu\text{m}$ of channel width for NMOS and PMOS transistors, respectively, and is optimized by a deep implant. The leakage is primarily caused by the generation centers in the silicon film near the sapphire interface and by the high interface state density. Both of these detrimental effects offer significant advantages for short-channel-length devices. The high interface state density partially decouples the drain field in the channel region and decreases the short-channel-length effect on the threshold voltage. The poor crystallinity results in very low mobility and minority carrier lifetime. This reduces drain-field-dependent leakage currents as well as voltage swings in the substrate bias due to the floating substrate. A significant

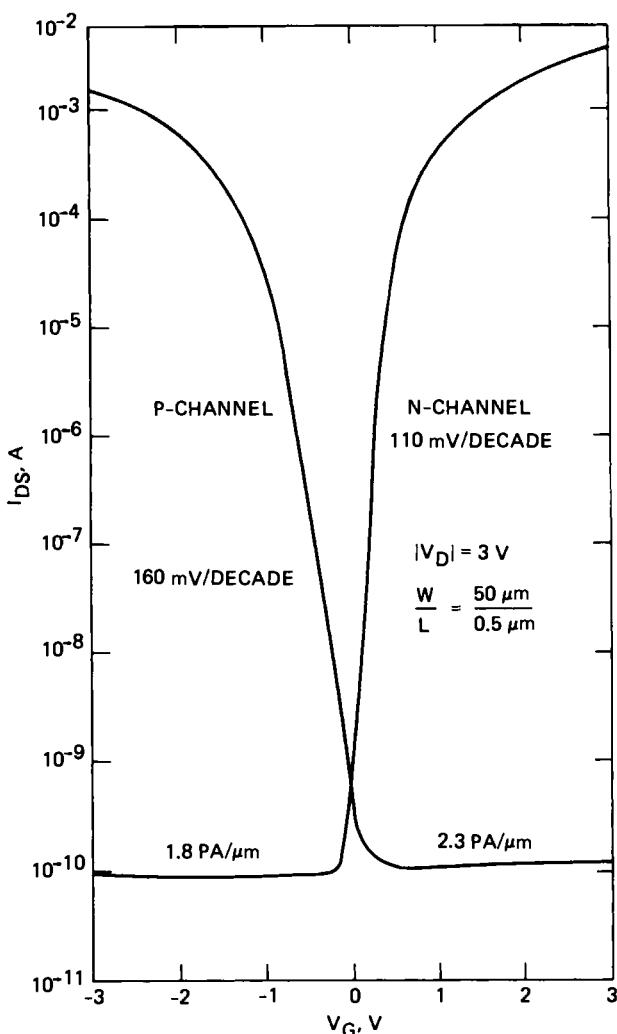


FIG. 20. Subthreshold current-voltage characteristics of submicrometer N-channel and P-channel MOSFETs fabricated in recrystallized SOS films.

improvement in the silicon crystallinity at the sapphire interface would adversely effect these beneficial properties.

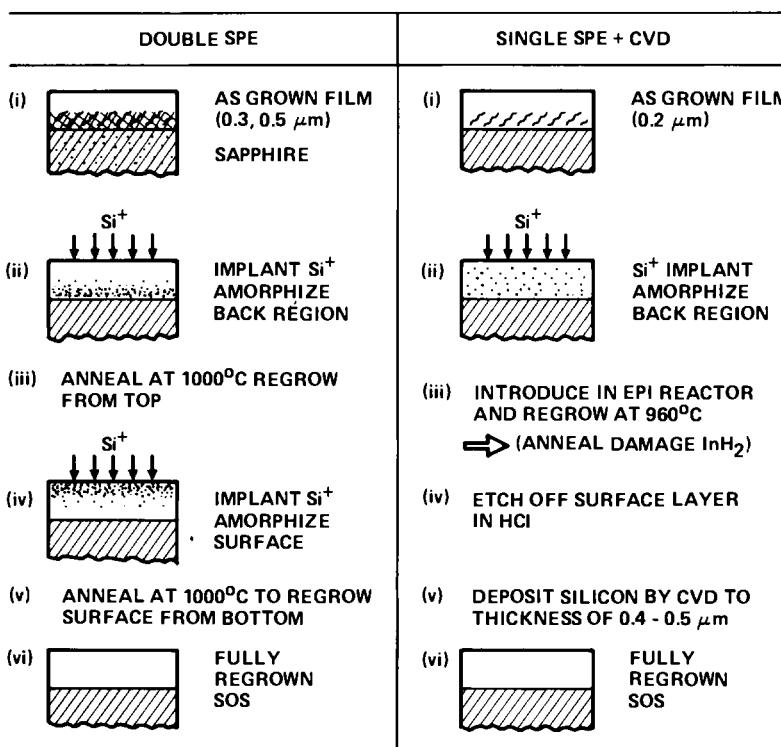
Several recent process advances have resulted in improved device performance. It is shown that the radiation tolerance is significantly improved by increasing the thickness of the gate electrode to minimize the penetration of the boron and phosphorus ions in the gate oxide during

source/drain implantation. In addition, VLSI circuits have been fabricated using silicide gate electrode and dry plasma etching. Other new process techniques applied to SOS include, *e*-beam lithography, high-pressure gate oxide, spacers to form self-registered gradually doped source/drain regions, and source/drain implant activation by laser annealing. These advances indicate the maturity of the process technology.

For proper scaling to micrometer and, submicrometer dimensions, it is desirable to use 0.2–0.3- μm -thick epi silicon films. Standard, as-grown SOS films show a large reduction in mobilities as the epi thickness is reduced. There are several novel techniques that have the potential for providing high mobilities in thinner SOS films. Molecular-beam epitaxy has been applied to SOS with properties superior to those of CVD films. Another promising alternative to MBE is *in-situ* silicon epitaxy by solid-phase crystallization of a deposited amorphous silicon film. At present, these techniques are very research oriented and are not expected to impact production for several years. Methods such as solid-phase epitaxial regrowth and laser annealing are very promising and are beginning to show commercial application.

It has been shown that crystallographic defects in SOS films can be significantly reduced by amorphizing the interface region of an as-grown SOS film by silicon ion implantation and using the relatively undamaged single-crystal silicon region on the surface as a seed for solid-phase epitaxial (SPE) regrowth by furnace annealing. Since the regrowth rate dominates along the $\langle 100 \rangle$ direction, the stacking faults and twins are eliminated, thus leaving dislocations as the major defect in the film. This has been verified by cross-sectional transmission electron microscopy, as well as a variety of other experimental techniques. The most advanced SPE processes have been developed at Hughes Research Laboratories and the basic process steps are shown in Fig. 21. The two processes are called solid-phase epitaxy and regrowth (SPEAR) and double solid-phase epitaxy (DSPE). High-performance submicrometer CMOS devices and circuits have been fabricated on materials made by these techniques. The fabricated devices showed significantly lower $1/f$ noise, lower junction leakage, and significantly higher minority carrier recombination lifetime. The channel mobilities increased by over 50%, as the crystallinity of the top silicon surface was found to be essentially equivalent to bulk silicon.

A comparison of the device characteristics of submicrometer CMOS transistors fabricated in both an as-grown SOS material and a SPEAR recrystallized film are shown in Table 2. As can be seen from the table, the channel mobility is essentially equivalent to bulk silicon and is reflected in the speed of ring oscillators with a propagation delay of 40 ps/stage at 3 V, which is currently a world record and is the fastest CMOS circuit at

EPI EVALUATIONS

- (A) ECP SPECTRA
- (B) X-RAY ROCKING CURVE
- (C) RBS ANALYSIS
- (D) ELECTRICAL CHARACTERIZATIONS

FIG. 21. Schematic of two recrystallization processes for improving SOS material quality developed at Hughes Research Laboratories.

room temperature. More details can be found in the paper by Vasudev (1985). The variation of the ring oscillator speed with bias voltage is shown in Fig. 22. Here we see that the speed can be modelled by the inclusion of a parasitic resistance which fits the measured data very well. The source of the parasitic resistance is the contact resistance and series resistance in the channel. By reducing these further, even lower propagation delay times can be achieved, thereby obtaining the full benefit of a silicon on insulator technology.

TABLE 2. Comparison of Key Device Parameters for NMOS and PMOS Transistors Fabricated in 3000 Å Thick AS Grown and SPEAR Recrystallized Silicon-on-Sapphire (SOS) Films

Parameters	As-Grown	SPEAR
Mobility (cm²/V sec) ($V_G = V_T + 0.5$ V)		
n	300	420–480
p	185	245–280
Subthreshold slope (mV/decade) ($L_{\text{eff}} = 1.4$ μm)		
n	109	92
p	146	120
Leakage current (pA/μm) ($L_{\text{eff}} = 1.4$ μm, $V_D = 3$ V)		
n	1.0	0.4
p	5.0	0.4
Drive current (mA/mm) ($L_{\text{eff}} = 1.4$ μm, $V_D = V_G = 3$ V)		
n	47	63
p	30	39
Inverter delay (psec) ($L_{\text{eff}} = 0.5$ μm, $V_{DD} = 5$ V)	100	40

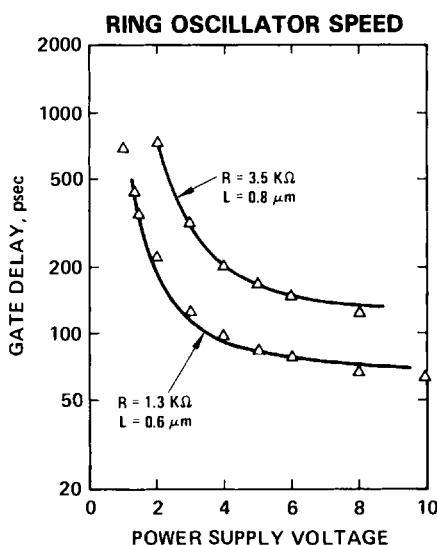


FIG. 22. Variation of the propagation delay per stage versus bias voltage for CMOS ring oscillators fabricated in recrystallized SOS films.

4.6 CONCLUSIONS

Material growth, characterization, and processing of submicrometer heteroepitaxial SOS films for VLSI applications, have been reviewed and advances have been presented. We have shown that the quality and reproducibility of the as-deposited epitaxial film has been significantly improved owing to reduction in concentration of the autodoped aluminum, improvement in surface crystallinity and roughness, reduction in micro-twin density, and incorporation of nondestructive screening techniques for quality control. This is partly due to advances in material characterization techniques and has resulted in improved device performance and circuit yields. Novel material improvement techniques, such as solid-phase epitaxial regrowth and MBE, have been discussed. We have shown that the SOS material quality has been improved and the channel mobilities are significantly increased with lower or similar junction leakages. In addition, several advances have been made in device processing, such as minimization of NMOS edge leakage and edge instability, increase in gate oxide breakdown, and radiation tolerance. A number of advanced processes have resulted in the design and fabrication of very high-performance digital and microwave integrated circuits for both commercial and military applications, thus indicating the maturity of the SOS technology.

ACKNOWLEDGMENTS

The author expresses sincere appreciation to R. C. Henderson, D. C. Mayer, G. D. Robertson, and S. Seymour, all of Hughes Research Laboratories.

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5 SILICON-ON-INSULATOR EPITAXY

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5.1 INTRODUCTION

This chapter addresses the formation of epitaxial layers for silicon-on-insulator (SOI) structures. SOI is a generic term that refers to a structure in which a silicon layer is supported by a dielectric material. This dielectric material can be a thick substrate, such as that shown in Fig. 1a. A typical example of this structure is silicon-on-sapphire (SOS). The thick sapphire substrate serves as a mechanical support as well as a template for epitaxial growth. The thickness of the epitaxial layer is typically 0.6 μm . Alternatively, the dielectric layer is very thin and is supported by a silicon wafer as shown in Fig. 1b. In this case, the dielectric layer serves primarily as an isolation layer, but in some cases it also may serve as a template for epitaxial growth.

SOS has been studied since 1962. Today, it is not widely used except in a niche market where radiation hardness and latchup-free performance are required. The primary reasons for the limited usage of SOS are its high cost (about \$120 for a 100-mm diameter SOS wafer compared to \$45 for an epitaxial wafer or \$15 for a regular bulk wafer in 1985), and its low yield. Low circuit yield is primarily a result of the variability of the quality of the epitaxial layer grown on the sapphire substrates. Recently, the use of an ultraviolet light reflectance technique to monitor the quality of the

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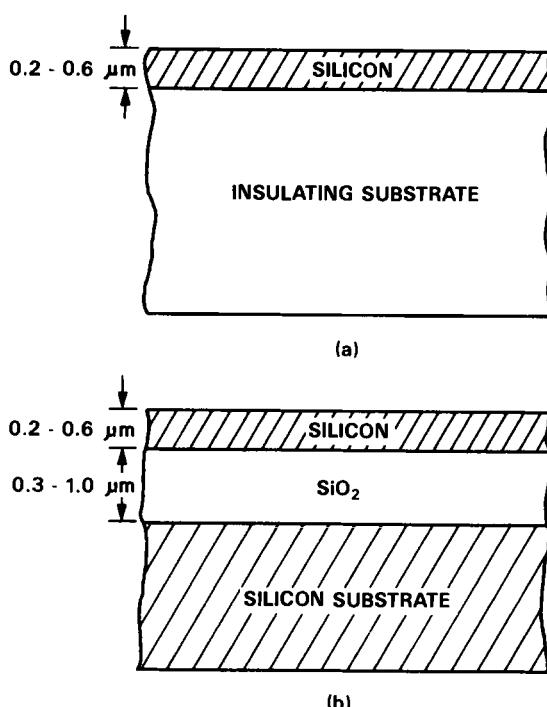


FIG. 1. Two SOI structures: (a) thick insulating substrate; and (b) thin insulating substrate supported by a silicon wafer. [From Lam *et al.* (1982b).]

epitaxial layer has significantly improved the quality of the materials and, hence, the yield (Kjar *et al.*, 1983)

In this chapter, we shall limit the discussion to the SOI case shown in Fig. 1b, which has received much attention lately. Readers who are interested in SOS are referred to Chapter 4 and Lam *et al.* (1982b) for a more detailed discussion of the subject.

The interest in SOI structures comes about because of the growing interest in using complementary metal–oxide–semiconductor (CMOS) circuits for very large scale integration (VLSI). A CMOS structure fabricated on SOI is shown in Fig. 2a.

A CMOS/SOI technology possesses many advantages over a bulk CMOS technology. As device feature size and the separation between devices become smaller, isolation between devices is becoming more difficult. The isolation requirements are such that there should be minimum physical separation between devices while providing maximum electrical isolation. This requirement has pushed conventional oxide isolation technology to a point where it will not be adequate below 1-μm minimum

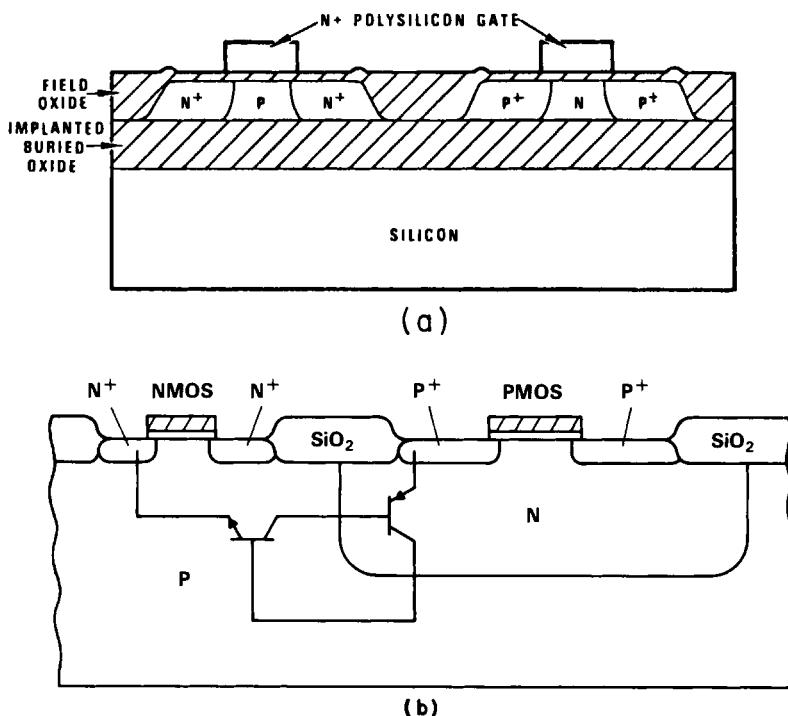


FIG. 2. Comparison of CMOS structures (a) on SOI and (b) on bulk silicon. Also shown are the parasitic bipolar transistors responsible for latchup.

feature size. With SOI, however, the isolation requirements are easily met by etching away the silicon between active device areas (and if desired, refilling the etched areas with silicon dioxide).

Since both *n*- and *p*-channel devices are isolated from each other and from the substrate, no parasitic bipolar devices responsible for latchup, such as the one shown in Fig. 2b, are present. Hence, latchup is eliminated. In order to eliminate latchup in bulk CMOS, especially when the device feature size is scaled below 1 μm , elaborate isolation schemes such as trenches (Rung *et al.*, 1980) have to be used. Junction isolation such as twin wells (Parrilo *et al.*, 1980) are becoming necessary to tailor device properties as well as to control the *n*-well and *p*-well dopant concentration to reduce latchup. The twin-well approach appears to require a minimum of about 3 μm separation between the *n*-channel and *p*-channel devices. This space between the devices is disproportionately large for submicrometer devices and does not scale readily. In the case of CMOS/SOI, the minimum spacing between the two devices can be the minimum feature size and therefore scales with feature size. This translates to an increase

in packing density and is expected to be important in submicrometer CMOS.

In submicrometer CMOS, the well dopant concentration is expected to increase to avoid punchthrough and other short-channel effects (Dennard *et al.*, 1974). With an increase in the well concentration comes an increase in junction capacitance. With the problems of hot-electron effects affecting gate oxide reliability (Nagai *et al.*, 1975), it is unlikely that gate-oxide thickness will be scaled as aggressively as in the past. This results in gate oxide capacitance remaining relatively stable. Hence, scaling to submicrometer will result in the junction capacitance becoming a larger portion of the total capacitance in a circuit. In CMOS/SOI, the junction capacitance is fixed as the dielectric layer thickness remains the same with scaling. Hence, it is expected that the total capacitance in an SOI structure will become increasingly smaller compared to a similar bulk structure. If CMOS/SOI devices have the same driving capability of comparable bulk CMOS devices, the lower total capacitance will result in a faster overall circuit.

Spurious charges are generated in a circuit by cosmic rays or by alpha particles, which are generated when traces of radioactive elements in packaging materials decay. These energetic particles generate electron-hole pairs in the silicon wafer. If these charges are collected at critical nodes of the circuit, then circuit upset, or electronic memory upset, commonly known as soft error (May and Woods, 1978), occurs. As device feature sizes become smaller, the critical charge required to upset them becomes smaller. Hence, it is expected that electronic circuits will be more susceptible with scaling. In SOI structures, the active devices are separated from the bulk wafer by the dielectric layer. Any charges generated in the bulk wafer will not be collected in the active devices. Hence, SOI devices are known to be more resistant to upsets and soft errors. Partly for this reason, SOS circuits have been chosen for use in spaceborne electronics and avionics. The advantages of using SOI for submicrometer CMOS are summarized in Table 1.

Two different kinds of bipolar-on-SOI structures have been demonstrated, and they are shown in Fig. 3. Figure 3a shows a conventional vertical bipolar structure with the addition of a buried oxide layer. Figure 3b shows a horizontal bipolar structure, which is very similar to an MOS device except that contact is now made to the base region of the transistor as well. Interest in SOI also comes from users of bipolar circuits for many of the same reasons stated earlier. In addition, it will be easier to implement complementary bipolar circuits with SOI. SOI also makes possible the horizontal bipolar structure, which can improve significantly the packing density of bipolar circuits to match that of MOS.

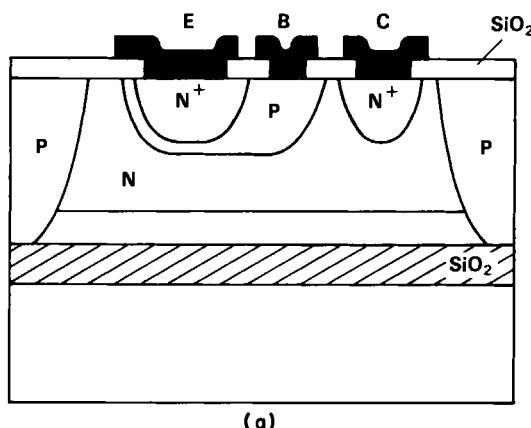
TABLE 1. Advantages of SOI in Submicrometer CMOS

Advantages	Reasons
Ease of lateral isolation	Lateral isolation without linewidth loss can be achieved with complete-island-etch isolation. No parasitic short-channel "field" oxide device.
Higher speed, as much as 2X, is possible	Junction capacitance in MOS is becoming a larger component of the total capacitance as gate oxide thickness will not be scaled as rapidly in submicrometer CMOS for reliability and hot-electron reasons. Higher substrate (well) doping concentration to reduce short channel effects.
Free from latchup	Dielectric isolation
High immunity to soft error	As capacitances in submicrometer devices get smaller, alpha-particles induced soft-error will become more severe. Dielectric isolation and a smaller generation volume in SOI reduce susceptibility.
Higher packing density (typically 20%-30%)	Minimum pitch at moat isolation possible and no need for well isolation in CMOS.
High voltage possible	Dielectric isolation

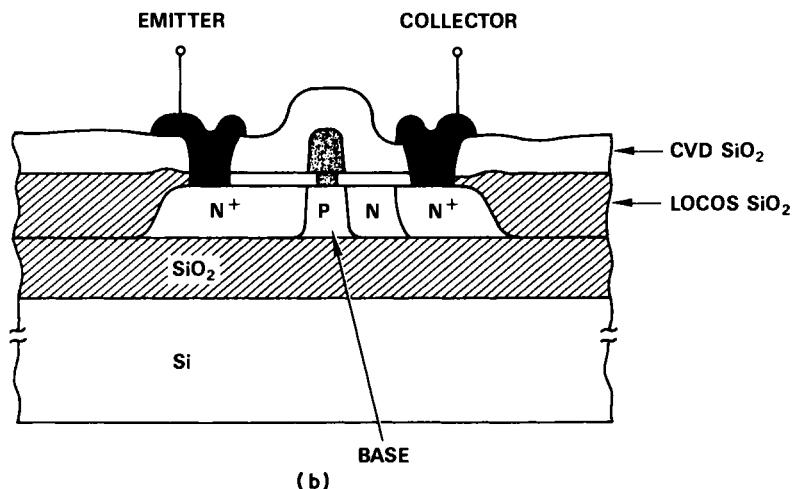
Dielectric isolation (Kamins, 1972) and junction isolation (Jayaraman *et al.*, 1984) techniques have been used extensively for high-voltage device and high-voltage integrated circuit (IC) applications. However, these techniques are, in most cases, not compatible with VLSI techniques. The trend of high-voltage integrated circuits is to include more and more low-voltage control functions on the same chip as the high-voltage power devices. This integration can be implemented easily on SOI technologies, and it is expected that SOI will be used in an increasingly larger number for these applications.

As the density of an IC becomes higher, the number of interconnects within an IC increases, usually at a rate proportional to the $\frac{2}{3}$ power of the number of elements (Keyes, 1979). Hence, the size of the IC becomes correspondingly larger. This trend makes the unexplored third dimension of the wafer very attractive as a means of stacking devices on top of each other in order to reduce the length and number of interconnects and as a means to improve the architecture of ICs. The placing of active elements in multilayered structures to form an IC is generically referred to as a three-dimensional integrated circuit (3D IC). The need for 3D IC necessitates the development of deposited single-crystal silicon materials on dielectric very much similar to SOI.

The first demonstrated 3D IC structure is the stacked CMOS shown in Fig. 4 (Chen *et al.*, 1983). This structure is interesting because it realized a CMOS inverter, which is a basic building block for most logic and



(a)



(b)

FIG. 3. Bipolar structures on SOI: (a) vertical bipolar transistor and (b) horizontal bipolar transistor.

memory circuits. The bottom device is a conventional n -channel MOS field-effect transistor (MOSFET) fabricated in bulk silicon. The top device is an SOI device, which is fabricated in polysilicon material deposited by low-pressure chemical vapor deposition (LPCVD). This structure demonstrated the impact in improved packing density and improved circuit performance of 3D ICs (Sundaresan *et al.*, 1984). The use of LPCVD polysilicon materials limits the potential of this stacked CMOS device

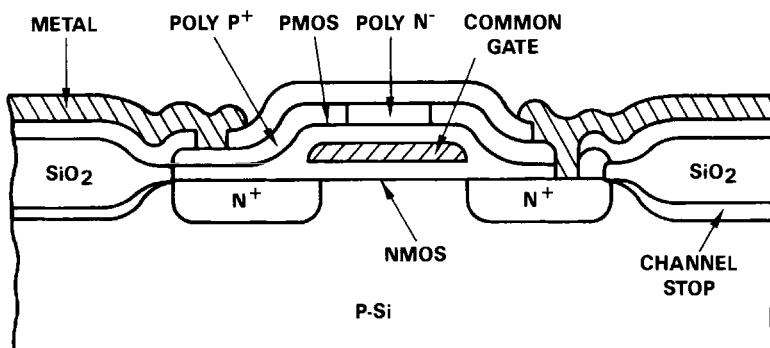


FIG. 4. Stacked CMOS structure. [From Chen *et al.* (1983).]

because of its low drive current. If this device can be fabricated in a single-crystal silicon material, the use of stacked CMOS and 3D ICs can be materialized. Many of the approaches to achieve SOI structures are directly applicable to the fabrication of 3D IC structures. Hence, the development of these two fields has progressed in tandem.

In this section, we have briefly discussed the potential applications of SOI and the attributes of SOI that makes it attractive for these applications. In the following sections, we discuss several epitaxial growth approaches to achieve SOI structures.

5.2 EPITAXIAL GROWTH ON IMPLANTED BURIED DIELECTRIC

5.2.1 Implanted Buried Dielectric SOI Process

Among all the recently studied SOI processes, implanted buried dielectric is probably at the most advanced state of development. It is also known as the Separation by Implanted Oxide (SIMOX) process (Izumi *et al.*, 1979). The implantation process is shown schematically in Fig. 5. Oxygen or nitrogen ions are implanted into a bulk silicon wafer to form a buried dielectric layer beneath the surface. The fluence, typically on the order of $2 \times 10^{18}/\text{cm}^2$, is chosen such that a stoichiometric dielectric material is formed. The energy of the ions, typically 150 keV, is chosen such that the ions can penetrate sufficiently deep into the surface of the wafer so as to leave a high-quality silicon layer at the surface thick enough to support subsequent anneal and epitaxial growth. With these typical parameters for oxygen ions, a buried oxide layer of 0.45 μm and a surface silicon

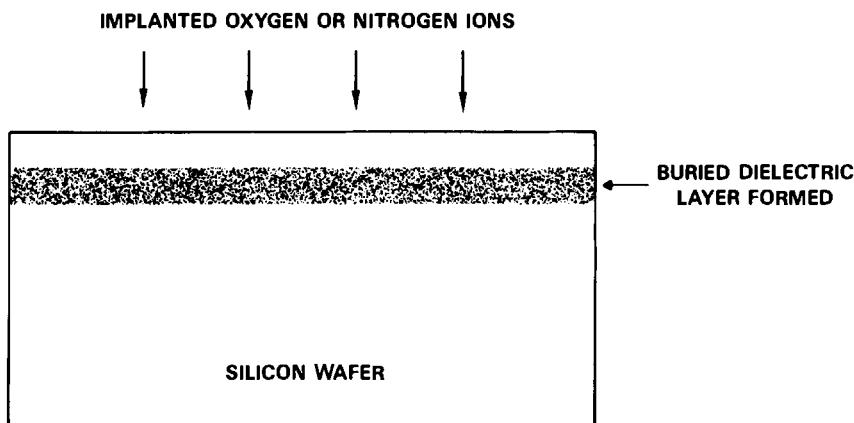


FIG. 5. Implanted buried oxide process.

layer of 0.15 μm result. An epitaxial growth of typically 0.2 μm will result in a total silicon thickness of 0.35 μm , which is the ideal thickness for most VLSI CMOS processes.

The thickness of the buried dielectric layer is directly proportional to the fluence while the throughput of the process is inversely proportional to the fluence. Hence, the choice of the fluence is a compromise between a thicker dielectric and a higher throughput. In addition, a higher fluence results in more damage to the surface silicon material, resulting in a lower-quality seed for subsequent epitaxial growth. The choice of implantation energy is also a compromise among several considerations. A low-energy implantation has the advantage of a lower spread in the distribution of the implanted ions, resulting in a lower total fluence required to reach stoichiometric concentration. On the other hand, a low-energy implantation induces more damage in the surface silicon region, resulting in a more defective seed material for subsequent epitaxial growth. It is generally believed that below 70 keV, the surface silicon layer will become polycrystalline regardless of subsequent heat treatment. A high-energy implant has the potential advantage that, if the buried oxide is embedded sufficiently deep beneath the surface, the surface silicon layer may be thick enough for device fabrication that no subsequent epitaxial growth is needed. However, a higher-energy implantation results in higher dispersion of the implanted ions, necessitating a higher fluence to achieve stoichiometric concentration. In addition, the power generated by an implanter is equal to the product of beam current and ion energy. By going to a higher energy,

we are forced to accept a lower ion current for a given power constraint; hence, throughput is reduced. With the next generation ion implanters being developed, it is unlikely that ion energies in excess of 200 keV will be available due to limitation in the design of high-voltage, high-current power supplies.

When an energetic ion is implanted into a silicon wafer, it loses its energy to the lattice. The initial energy transfer is through electronic interactions with little momentum transfer. Hence, little damage is done to the lattice. As the ion penetrates more deeply and starts to slow down, nuclear interaction becomes increasingly important as the nuclear interaction cross section increases. Eventually, enough momentum is transferred from the ion to the nucleus to cause a displacement. The displaced nucleus may have enough energy that it may cause further displacement. Because of both the cascade effect and forward scattering, the damage increases with depth until the incoming ion and the displaced nucleus have less and less energy that they eventually come to a halt. The range of the implanted ions has a Gaussian profile (Fig. 6a) while the damage profile peaks before the peak of the Gaussian (Fig. 6b). Figure 6 shows that if the energy of the implanted ions is chosen high enough, the surface region can be relatively free of the implanted ions. More importantly, if the energy is high enough, the amount of damage done at the surface can be low. In Fig. 6b, a critical damage level is depicted with the dotted line. It is defined as the level of damage above which single-crystal material cannot be recovered even after high-temperature annealing. For damage below this critical level, a single-crystal silicon surface layer can be retained after

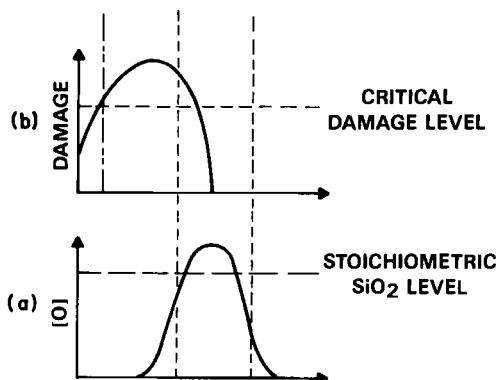


FIG. 6. Implanted buried oxide process: (a) implanted oxygen ion profile; and (b) lattice damage profile.

implantation. This critical level is dependent on the fluence and the temperature during the implantation (Morehead *et al.*, 1972) A higher wafer temperature during implantation allows *in-situ* self-annealing to take place. It was found that there is an optimum temperature for this process (Holland *et al.*, 1984). Below this optimum temperature, damage in the top silicon layer is too high. Above this temperature, oxygen diffuses toward the surface and results in extensive precipitate formation.

5.2.2 Material Characteristics

The as-implanted material has been characterized by cross-sectional transmission electron microscopy (XTEM). Figure 7 is a typical result obtained for an as-implanted sample. The amorphous silicon dioxide region is apparent. Even without high-temperature annealing, the *in-situ* temperature of about 500°C is sufficiently high so that significant diffusion occurs resulting in a stoichiometric silicon dioxide region. The superficial silicon region is highly defective. Careful inspection of the micrograph shows that a very thin single-crystal layer (about 40 nm thick) exists at the top surface.

After annealing the wafer at 1150°C for 3 h in a nitrogen ambient, the superficial silicon layer crystallized through a solid phase regrowth process where the remaining single-crystal layer acts as the seed for regrowth. At the same time, the superficial silicon region becomes denuded of oxygen due to outdiffusion. Figure 8 is an XTEM micrograph of a buried oxide sample after this high-temperature annealing step. At the surface between the superficial silicon and the buried oxide, oxide precipitates can be observed. Prominent defects found in the superficial silicon are dislocations with a density on the order of $1 \times 10^8/\text{cm}^2$.

Typical results from Rutherford backscattering spectroscopy and MeV He²⁺ ion channeling experiments are shown in Fig. 9. The dip in the random spectrum between 800 keV and 1.1 MeV shows the position of the buried oxide layer due to a lower density of silicon in the buried oxide layer. From Fig. 9, the thickness of the superficial silicon layer is estimated to be 150 nm while the buried oxide is about 500 nm thick. The aligned spectrum indicates the crystallinity of the superficial silicon layer and can be calibrated against that of an unprocessed silicon wafer. The peak at the surface is a result of a surface oxide layer. The minimum yield for the superficial silicon layer is about 15%, compared to about 3% for an unprocessed silicon wafer.

The minimum channeling yield of the superficial layer has also been studied as a function of anneal time. It is observed that the channeling yield is very high immediately after ion implantation, but decreases rapidly as the annealing time at 1150°C increases (Fig. 10). This is a result of the

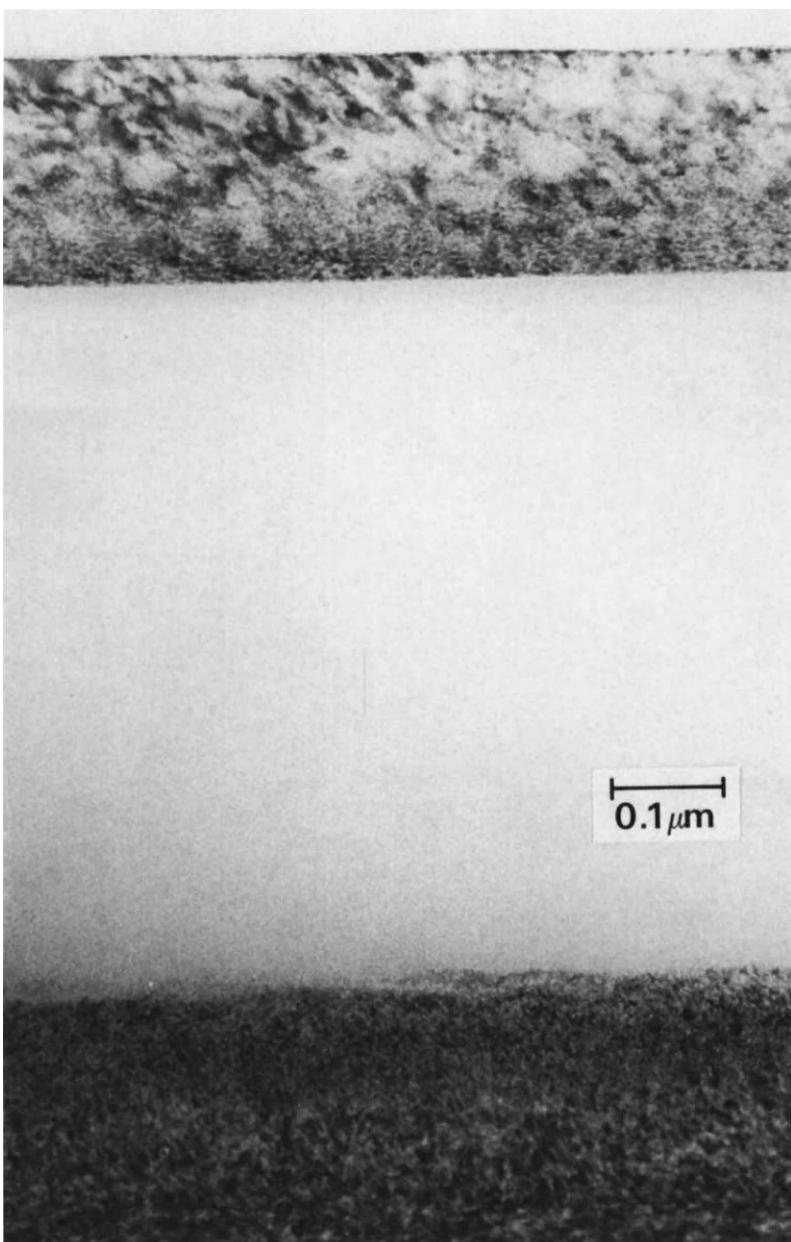


FIG. 7. Cross-sectional TEM micrograph of a silicon wafer after oxygen ion implantation. Ion dose was $2.6 \times 10^{18}/\text{cm}^2$, and the ion energy was 150 keV.

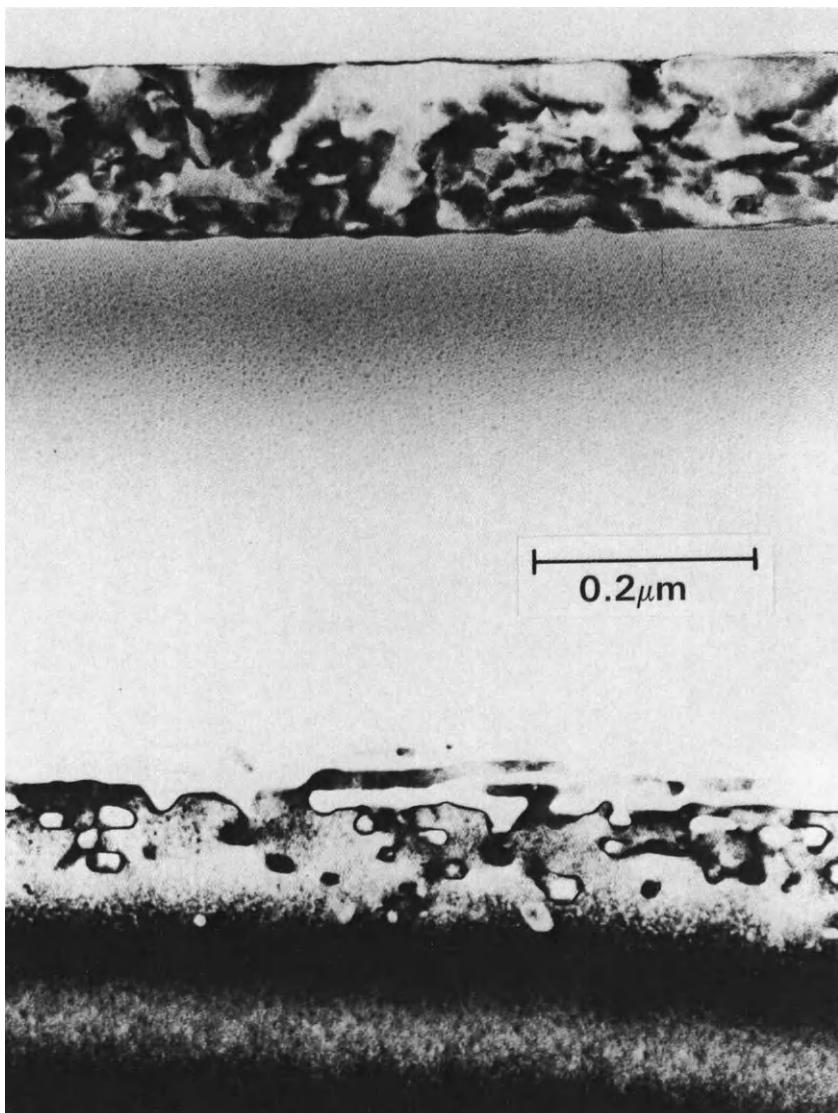


FIG. 8. Cross-sectional TEM micrograph of the sample shown in Fig. 7, but after a 1150°C anneal for 3 h. Note that although the top silicon layer is single crystal, it is defective and full of silicon dioxide precipitates.

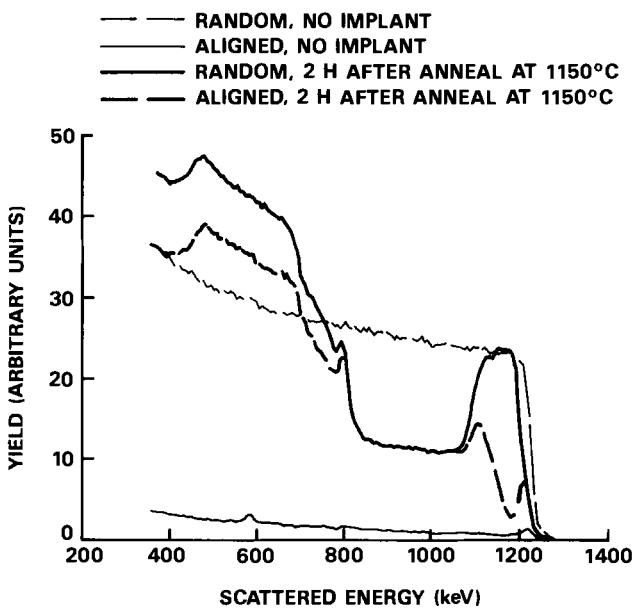


FIG. 9. Rutherford backscattering spectra of implanted buried oxide SOI.

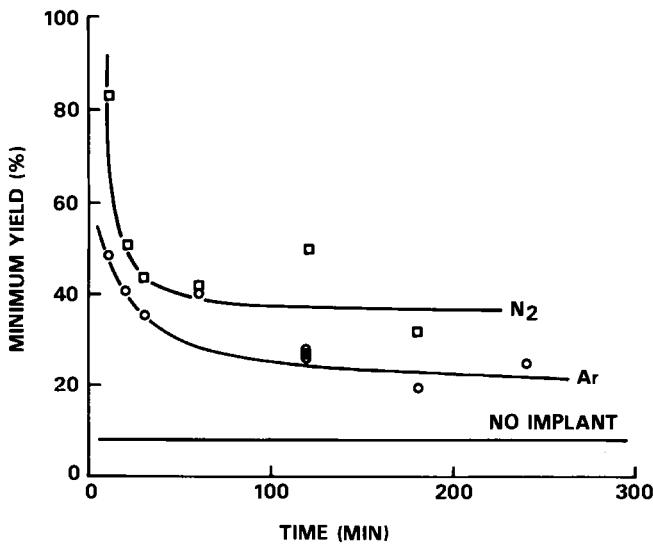


FIG. 10. Minimum yield of Rutherford backscattering spectra of implanted buried oxide SOI as a function of anneal time.

rapid solid-phase regrowth that occurs during the annealing. However, the minimum yield decreases at a much slower rate after several hours of anneal, apparently reaching a state where all remaining defects are stable at the annealing temperature of 1150°C.

5.2.3 Epitaxial Growth

The thickness of the superficial silicon layer is about 150 nm and is not thick enough for most device applications. Hence, an epitaxial layer is added to increase the thickness before device fabrication.

A dichlorosilane epitaxial process at 1100°C has been successfully used to grow epitaxial layers on the buried oxide material. For MOS applications, only a thin (0.2–0.3- μm) epitaxial layer is needed. Hence, the growth rate must be reduced to obtain improved uniformity and reproducible results. In addition, the seed material (superficial silicon layer) is very thin and extreme care must be exercised to protect and preserve this layer before and during the epitaxial process. On the other hand, surface preparation is of utmost importance in the epitaxial process to prevent nucleation of defects.

Because of the very thin seed material, HCL surface treatment cannot be used to avoid removal of the seed material. Surface cleaning prior to epitaxial deposition is accomplished by an *in-situ* anneal in hydrogen at 1130°C for 5 min, which reduces any native oxide from the surface. Even with hydrogen surface cleaning, extreme care must be exercised as excessive anneal with hydrogen at high temperatures will eventually lead to etching or pitting of silicon. We shall return to this issue later.

Because of the requirement of a thin (0.2–0.3- μm) epitaxial layer, a low growth rate is desired. This can be easily achieved by diluting the dichlorosilane gas with hydrogen during deposition. In fact, a 5% dichlorosilane mixture yields a deposition rate at 1100°C of 0.07 $\mu\text{m}/\text{min}$ of deposition. This slow deposition rate gives a total deposition time of about 3–4 min, which is sufficiently long for excellent control of thickness and reproducibility from run to run. Typical thickness control is well within $\pm 5\%$.

The epitaxial silicon layer can also be grown on buried oxide SOI wafers before they are annealed at 1150°C in nitrogen. The wafer will, of course, receive a short (about 5-min) anneal in hydrogen at 1130°C during surface oxide reduction. This approach has also been demonstrated, and results will be discussed in a later section.

5.2.4 Epitaxial Thickness Measurement

Measurement of the thickness of an epitaxial layer, especially when it is less than 1 μm thick, has always been a very difficult task. The most commonly used technique is infrared reflectance from a lightly doped

epitaxial layer grown on a heavily doped substrate. This technique fails for very thin epitaxial layers because outdiffusion of the impurity from the heavily doped substrate smears the definition of the epitaxial boundary. The outdiffusion can occur over a thickness of about 0.1–0.3 μm due to autodoping and diffusion. Hence, the percentage error of this measurement technique increases rapidly as the epitaxial layer thickness is reduced below 1 μm . This problem poses a severe challenge to very thin epitaxial layer growth.

Fortunately for buried oxide SOI, the presence of the buried oxide creates a multilayered structure with well-defined interfaces so that a reflectance technique can be used for the measurement of epitaxial layer thickness. The thickness of the buried oxide layer can also be measured by this method. The superficial silicon layer (which may include the epitaxial layer), the buried oxide layer, and the substrate form a three-layered structure. Since the dielectric constants of these layers are well known, the reflectance characteristics of this structure is well characterized. In fact, standard reflectance measurement equipment can be used directly to measure this structure. A method developed on an IBM film thickness analyser is shown below.

Figure 11a shows the output waveform of one such measurement. The circles were actual reflectance values measured by the equipment. The solid curve is the calculated value of the reflectance based on the maxima and minima of the measured values and the input values of buried oxide thickness and index of refraction of silicon. In this case, the total superficial silicon thickness was measured to be 532.7 nm. Note also that the reflectance maxima and minima are modulated by a slowly varying envelope (Fig. 11b). The node of this envelope gives a measurement of the actual buried oxide thickness. The node of the envelope occurs at about 510 nm. The actual oxide thickness in this case was 520 nm, obtained from XTEM measurement. This yields an agreement to better than 2%. This result shows that the use of epitaxial growth on buried oxide combined with reflectance measurements can conceivably be used as a calibration technique for very thin epitaxial growth.

5.2.5 Physical Characteristics of the Epitaxial Layer

Epitaxial layers grown on buried oxide SOI have been extensively characterized by XTEM and RBS. A typical XTEM micrograph of an epitaxial layer is shown in Fig. 12. The epitaxial layer is of good quality. The only kind of defect that can be observed is dislocation which, in most cases, propagates from the interface between the original superficial silicon layer and the buried oxide. Stacking faults are not commonly generated during the oxygen ion implantation process. Hence, if the epitaxial process

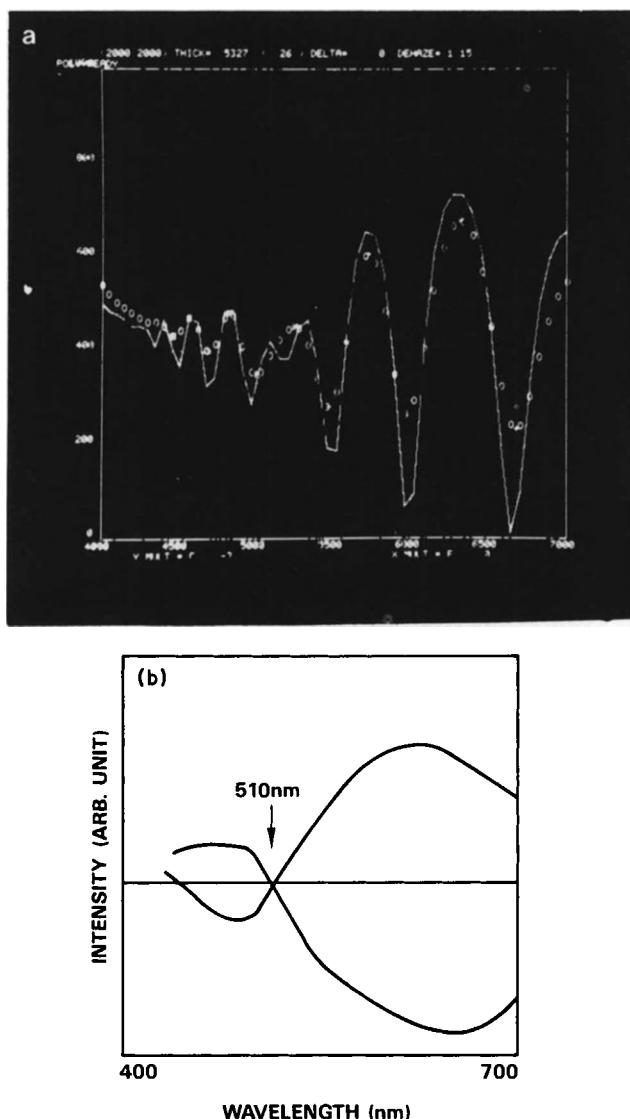


FIG. 11. Optical reflectance of SOI structure: (a) actual reflectance and (b) envelope of the reflectance, showing the node of the envelope, which gives the value of the thickness of the buried oxide layer.

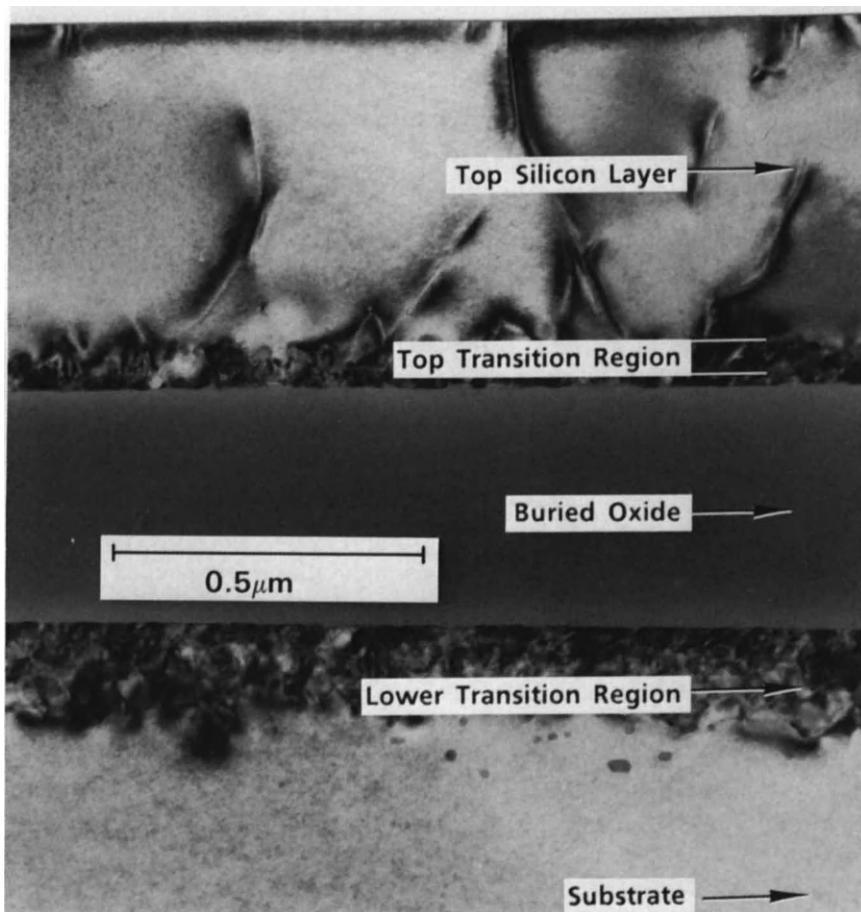


FIG. 12. Cross-sectional TEM micrograph of an epitaxial layer grown on buried oxide SOI. The primary defects are dislocations.

is well controlled, stacking faults will not be generated in the epitaxial layer. Microtwins are rarely observed, but if they do occur, they are usually generated at the interface between the buried oxide layer and the superficial silicon layer.

Silicon dioxide precipitates are observed extensively at the interface of the superficial silicon layer and the buried oxide. They are formed during the high-temperature annealing process immediately after ion implantation. During the annealing, oxygen diffuses out of the superficial layer, forming a denuded layer close to the surface. However, close to the

interface where the oxygen concentration is very high (but below stoichiometric silicon dioxide level) and where damage level is high, oxygen precipitates can easily nucleate and grow.

Figure 13 compares the backscattering yield of channeled He^{2+} ion for three materials: epitaxial layer grown on buried oxide SOI, an epitaxial layer grown on sapphire substrates, and unprocessed silicon material. At the surface, the channeling yield of epitaxial silicon on buried oxide SOI is very low, only slightly higher than that of silicon material. The channeling yield becomes much higher at the interface between the superficial silicon layer and the buried oxide layer. This is expected due to the high density of precipitates observed in XTEM (Fig. 12). The channeling yield of the SOI material is much lower compared to SOS. This is a result of two factors. The defect density in buried oxide SOI is lower than that in SOS. The prominent defects in SOS are microtwins, and being planar defects, they cause more dechanneling than linear defects such as dislocations commonly found in buried oxide SOI.

For epitaxial layers grown without a 1150°C anneal, the defect characteristics are different. This is shown in Fig. 14, which is an XTEM micrograph of such a film. A high-quality epitaxial film is obtained. However, the dislocation density in the epitaxial layer is higher compared to the case of epitaxial growth on annealed SOI material.

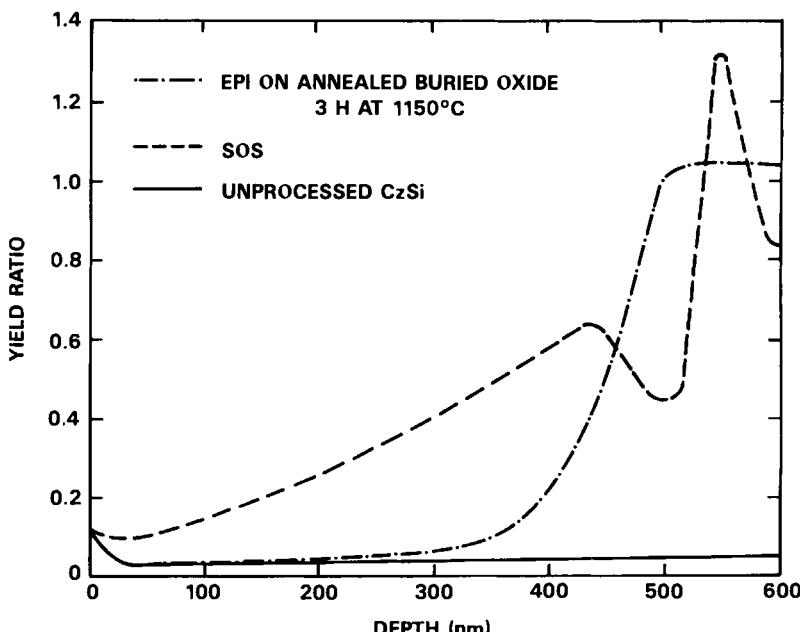


FIG. 13. Comparison of Rutherford backscattering spectra of buried oxide SOI, SOS, and bulk silicon.

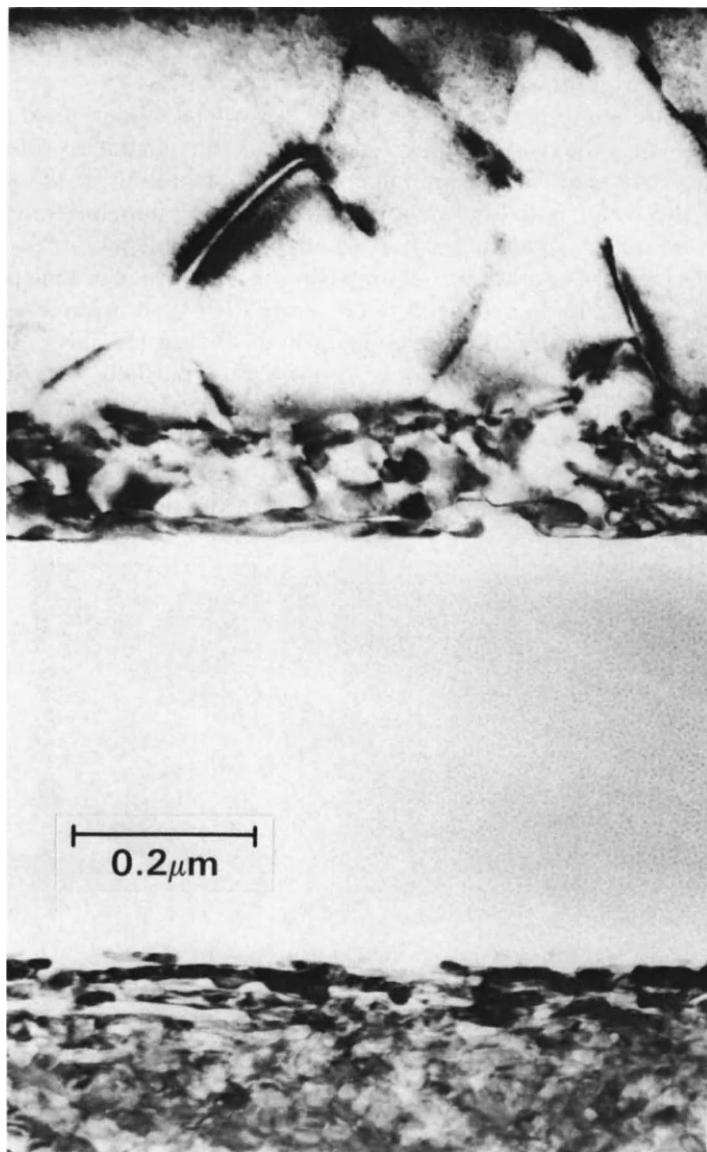


FIG. 14. Cross-sectional TEM micrograph of an epitaxial layer grown on buried oxide SOI before any post-implantation high-temperature anneal.

5.2.6 Macroscopic Defects

Three kinds of macroscopic defects have been observed in epitaxial buried oxide SOI films.

Cracks are sometime observed in the superficial silicon layer. These cracks are caused by stress in the superficial silicon film due to volumetric expansion as a result of the high fluence ion implantation. If the temperature of the wafer is held at or above 400°C during implantation, *in-situ* stress relief occurs, and cracking is usually not a problem.

Another macroscopic defect is shown in Fig. 15a, which is a micrograph obtained from scanning electron microscopy (SEM) showing a top view of a buried oxide wafer after epitaxial growth. Figure 15a shows that the superficial silicon layer is no longer continuous, partially exposing the implanted buried oxide layer. Furthermore, the buried oxide layer appears to have been etched, with deep channels formed. By depositing a doped polycrystalline silicon (polysilicon) layer on the top of this wafer, we can actually measure electrical continuity between the deposited polysilicon

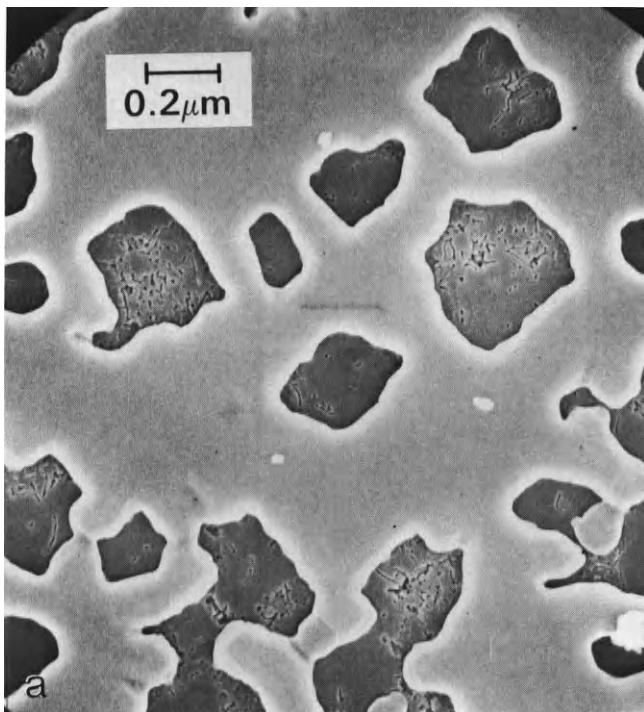


FIG. 15. Defects induced in epitaxial growth. (a) Top view scanning electron micrograph after epitaxial growth. Voids are observed in the silicon layer. The buried oxide layer has also been etched. (b) Cross-sectional TEM of the same sample showing channels that were etched in the buried oxide.

layer and the silicon substrate. This means that the etched channels in the buried oxide reach the substrate. Figure 15b shows an XTEM micrograph of the wafer shown in Fig. 15a. The discontinuity of the epitaxial layer is evident. A dark image is apparent in the buried oxide layer, and it is believed to be the image of one of the etched channels. There is evidence of regrowth at the edge of the opening in the epitaxial layer. The interface

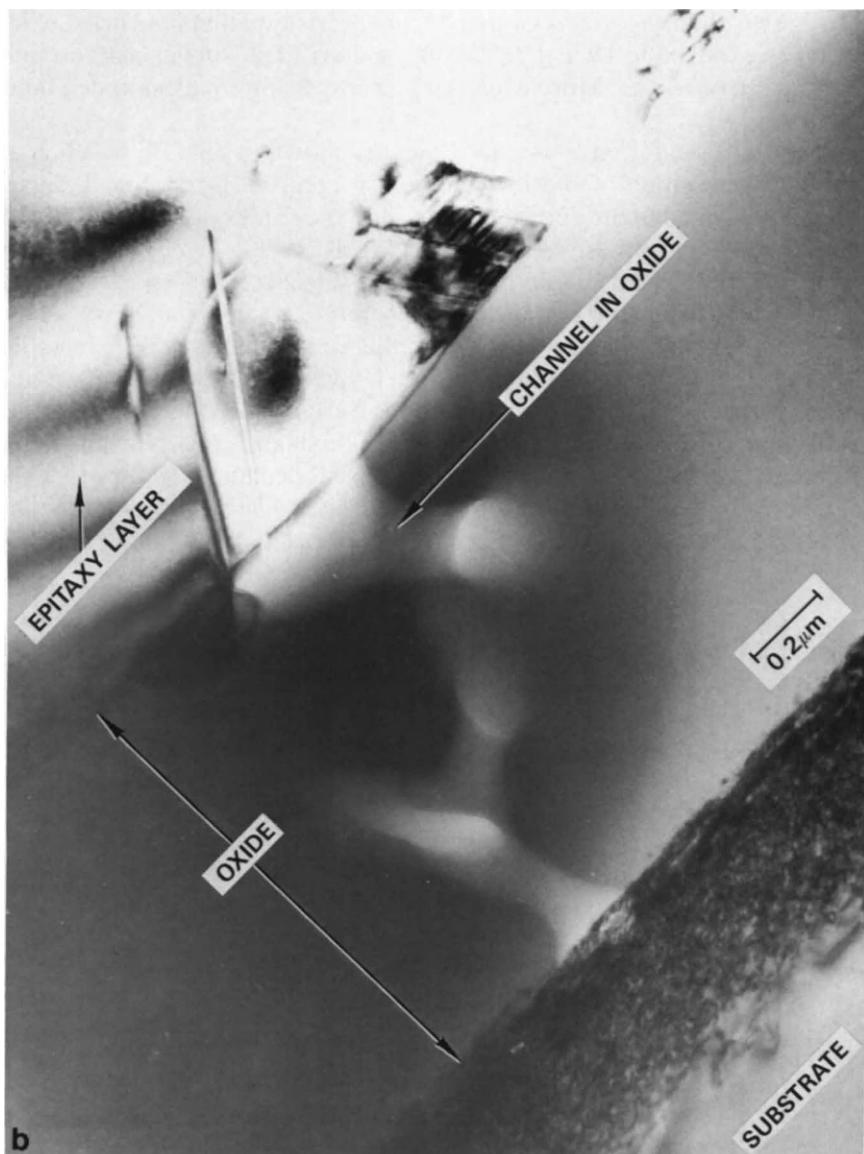


FIG. 15. (continued)

between the superficial silicon layer and the buried oxide layer close to the edge of the opening has a very different characteristic, with microtwins emanating from the interface. This is characteristic of epitaxial overgrowth (see Section 5.5). A tentative explanation of the formation of this defect is as follows: during the epitaxial process, dichlorosilane decomposes to form silicon and HCl. The HCl etches the superficial silicon layer and, when the buried oxide layer is exposed, continues to etch the buried oxide layer. This theory is corroborated by an observation that if a buried oxide wafer is exposed to HCl at 1100°C for a short time, similar macroscopic defects are observed. More work is under way to improve our understanding in this area.

The third kind of macroscopic defect is shown in Fig. 16, which is an optical macrograph of the top view of an epitaxial layer. Small square holes are formed in the epitaxial layer, with their sides parallel to the [110] directions. Within these holes, the superficial silicon layer is completely removed, exposing the underlying buried oxide layer. It is speculated that under a hydrogen ambient at high temperature, the implanted oxygen in the superficial silicon layer escapes in the form of gaseous SiO, resulting in local etching of the superficial silicon layer. Once local etching occurs, the pitted area becomes the preferred diffusion path of oxygen, further enhancing the etching process. Subsequent epitaxial growth results in the faceted surfaces along the [110] directions. Calculations show that the equilibrium partial pressure of SiO in hydrogen is a very strong function of temperature, as shown in Fig. 17. Hence, etching of silicon and SiO

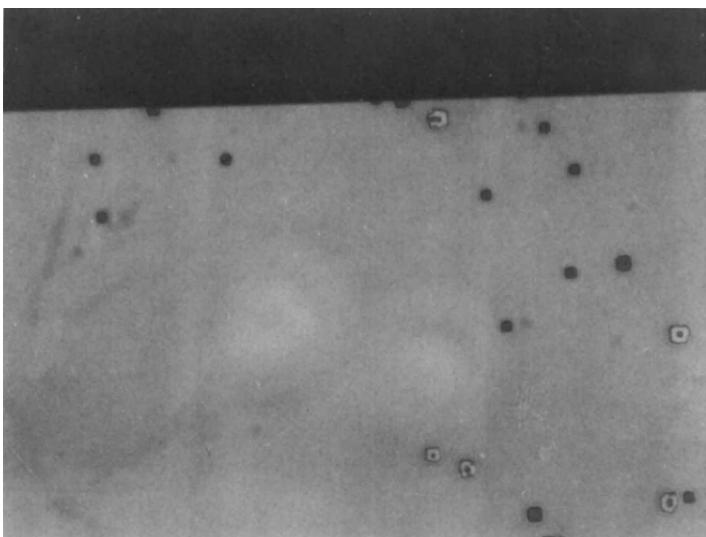


FIG. 16. Optical top-view micrograph of pits in the epitaxial layer. Note the square geometric pattern of the pits.

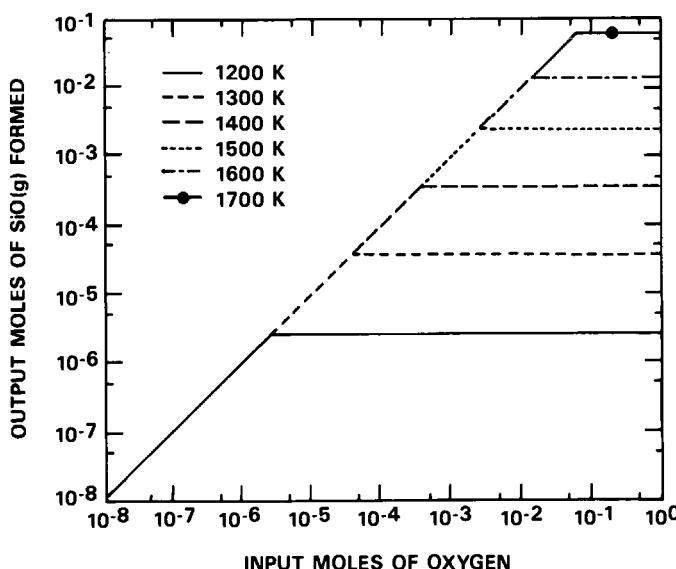


FIG. 17. Partial pressure of SiO as a function of temperature and oxygen concentration. (Courtesy of A. Bowling, Texas Instruments.)

outdiffusion can be reduced by lowering the temperature of the epitaxial process. Experimental observation has confirmed this hypothesis. By reducing the temperature of the epitaxial process, the density of this kind of macroscopic is significantly reduced.

5.2.7 Applications

There are many potential applications of this SOI technology: submicrometer CMOS, high-voltage circuits, dielectrically isolated bipolar devices, and radiation-hardened microcircuits.

One example of circuit demonstration is illustrated in Fig. 18, which shows an experimental 4 K-bit CMOS static random access memory (SRAM) fabricated on the buried oxide material (Chen *et al.*, 1984). Figure 19 shows the output waveform of the memory circuit showing that the access time of the memory, the time delay between the chip-select waveform (top waveform) and the output waveform (bottom waveform), is about 55 nsec. Electrical characteristics of devices fabricated in the buried oxide SOI material are comparable to those of devices fabricated in bulk silicon. This experimental circuit demonstrates that buried oxide SOI material is compatible with VLSI CMOS circuit fabrication.

The breakdown voltage of the 0.5-micrometer thick buried oxide is typically 340 V. Hence, the breakdown field is equivalent to about 6.8 MV/cm, compared to a breakdown field of typically 8–10 MV/cm for thermally growth silicon dioxide. This relatively high breakdown voltage makes this

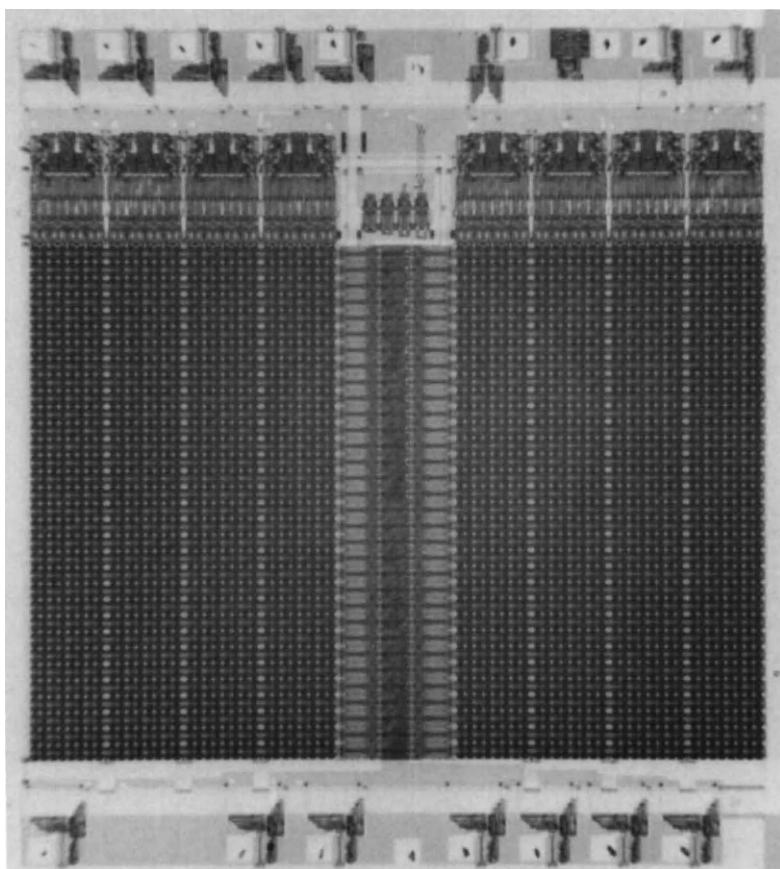


FIG. 18. Optical micrograph of 4 K-bit CMOS/SOI SRAM.

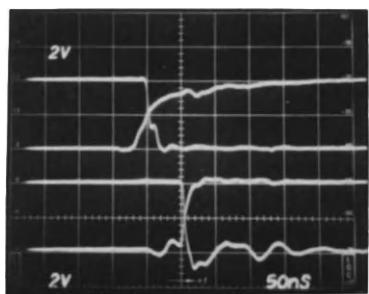


FIG. 19. Output waveform of circuit in Fig. 18 is shown at the bottom of this figure. The waveform on top is the address signal. The delay between the address signal and the output signal is the access time, which is about 55 nsec.

material suitable for applications in high-voltage devices and circuits. In addition, if *p*-type substrates were used to produce the buried oxide SOI material, the fixed oxide charge between the bottom interface of the buried oxide and the substrate will form a depletion layer of silicon immediately beneath the buried oxide layer. This depletion layer will further add to an increased susceptibility to high-voltage breakdown as the electric field is now sustained across the combined dielectric layer composed of the buried oxide layer and the depleted silicon.

5.3 LATERAL EPITAXY FOR SOI: LIQUID-PHASE PROCESS

5.3.1 Zone Melting Crystallization

In 1979, Tasch *et al.* (1979) and Lee *et al.* (1979) showed that by scanning a focused laser beam (with power density in excess of 100 KW/cm^2) across the surface of a polysilicon layer deposited on an oxide substrate, large grains of silicon resulted. This melting and crystallization process is depicted in Fig. 20. When the focused laser beam, which is typically 40–80 μm in diameter, is scanned across the surface of the polysilicon layer, the polysilicon under the illumination of the laser beam is melted. As the beam is scanned across, the molten silicon at the trailing edge of the molten zone cools and freezes. This crystal growth is seeded by the polysilicon immediately adjacent to the molten silicon. In addition, the direction of crystal growth follows the steepest temperature gradient. This is indicated in Fig. 20a by the arrows, which point towards the growth directions. The resulting grain structure is shown in Fig. 20b. The large crystals are aligned in a chevron structure, a combined result of the Gaussian intensity profile of the laser beam and growth along the steepest temperature gradient.

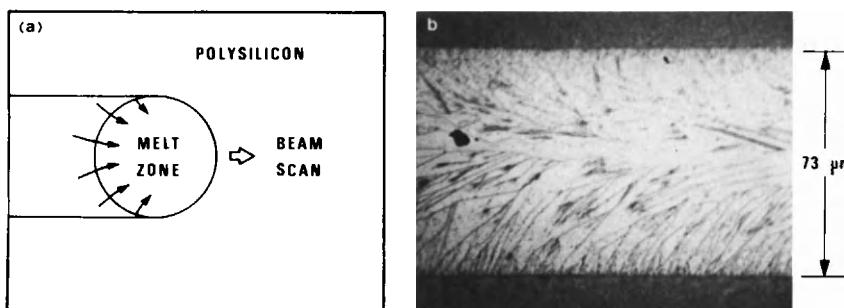


FIG. 20. Laser-induced liquid-phase lateral epitaxy: (a) schematic showing the melt zone and the steepest thermal gradient, which is the direction of crystal growth, and (b) optical micrograph of a resulting grain structure.

Crystal growth across the entire surface of a wafer can, in principle, be accomplished by scanning the laser across the wafer in a raster fashion. The resultant grains, however, are still polycrystalline, albeit with much larger grain size. This is a result of the lack of a single-crystal seed. Single-crystal growth can be achieved by a technique shown in Fig. 21, (Lam *et al.*, 1981). This approach makes use of the silicon wafer, which is usually used as the supporting substrate, as a seed material. An oxide layer is grown on the silicon substrate followed by etching of windows in the substrate. Subsequent deposition of polysilicon results in the polysilicon layer coming in direct contact with the substrate at the windows. As a laser beam illuminates the polysilicon on silicon region (seed region), the polysilicon and a portion of the underlying silicon is melted. As the beam is scanned away, the molten silicon freezes and crystallizes epitaxially. This results in the propagation of the seed from the substrate to the surface silicon layer. As the laser beam scans into the polysilicon on oxide region, the epitaxially grown silicon at the trailing edge of the beam seeds the growth.

Figure 22 is an optical micrograph of an example of this lateral epitaxial growth process. The silicon wafer have been etched in a Secco etch (d'Aragona, 1972) to delineate the defects. In this figure, the laser beam was scanned from left to right and stepped from top to bottom. The silicon film was 0.5 micrometer thick, and the underlying silicon dioxide layer was 1 micrometer thick. As shown in Fig. 22, single-crystal growth extended from the seed laterally by about 20–30 micrometers. Beyond that,

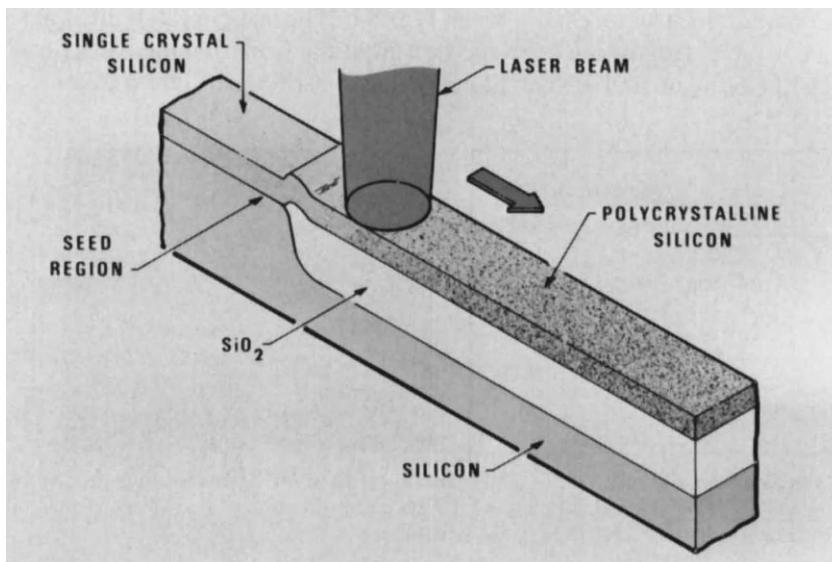


FIG. 21. Lateral epitaxy with seeding.

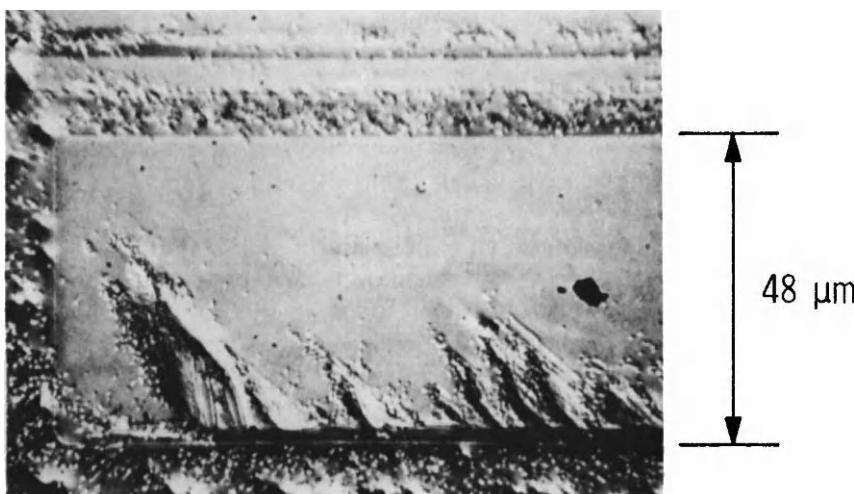


FIG. 22. Top-view optical micrograph of seeded lateral epitaxy. The sample has been etched to delineate defects. Most of the SOI area is single crystal, with a low etch-pit (defect) density. The defect density becomes higher toward the bottom of the SOI area, which eventually becomes polycrystalline.

dislocations (manifested by small etch pits) started to form and coalesced to form subboundaries (etched lines) (Pinizzotto *et al.*, 1982). The formation mechanisms of these defects will be discussed later. Close to the corner where the laser beam entered the silicon-on-oxide area, a defective region was also formed. Defects in this region were formed when the melt fronts from the seed regions on top and to the left collided. These defects are a result of the geometry and are inherent to melt-growth processes in silicon.

Heat sources such as optical radiation or electron beams have been used. Optical radiation has proved to be more effective as the process window, the range of input power density used, is wider. This is a result of the change in reflectivity of silicon as it undergoes a phase transformation. Liquid silicon is metallic in nature and has a high reflectivity for optical radiation. Once silicon is melted, it absorbs less light and, hence, provides a negative feedback effect to stabilize the temperature rise within the melt (Hawkins and Biegelsen, 1983). With electron beams as the heat source, however, molten silicon continues to absorb energetic electrons, resulting in an excessive temperature rise and eventually causing splattering of the melt. Nonetheless, electron beams have been used successfully albeit with a smaller process window. Both line-shaped electron beams (Hayafuji *et al.*, 1983) and scanned beams (Davis *et al.*, 1983) have been demonstrated.

The most popular optical heat source besides a laser beam is a graphite

strip heater (Fan *et al.*, 1981), one of which is shown in Fig. 23. The graphite strip heater is an example of a resistively heated radiation source. The process is shown schematically in Fig. 24. A bottom graphite heater raises the temperature of the wafer to about 1200°C. The top scanning strip heater is heated to about 1750°C and is scanned across the surface of the wafer while maintaining a gap of about 2 mm from the surface of the wafer. The silicon absorbs the radiation from the scanning top heater and melts. Hence, a molten zone is dragged along with the scanning top heater. In cases where a seed is provided by contacts to the substrate, a {100}-oriented silicon SOI layer is obtained (Lam *et al.*, 1982a). Even without a seed, a {100} texture is preferred (Geis *et al.*, 1982a). A typical result without seeding is shown in Fig. 25.

In the graphite strip heater process, the melt zone is very wide (about 5 mm) compared to the thickness of the film (0.5 μm). Hence, the liquid film is in a very unstable condition as it wants to break up and form droplets to minimize its total surface energy. Obviously, this is undesirable for SOI formation. It has been found that a thick cap of 2 μm of deposited oxide stabilizes the surface and prevents delamination of the molten film (Lam *et al.*, 1982a).

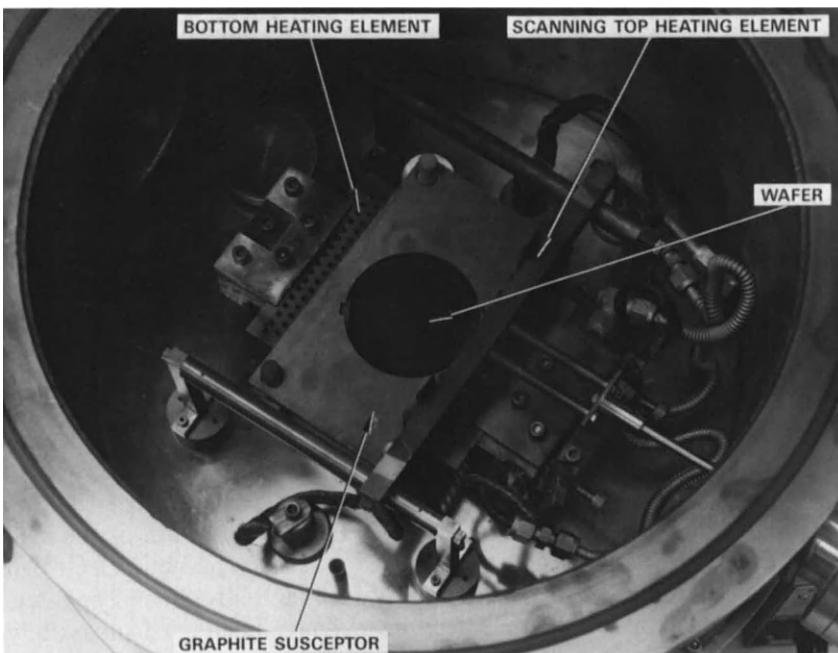


FIG. 23. View inside a typical graphite strip heater reactor.

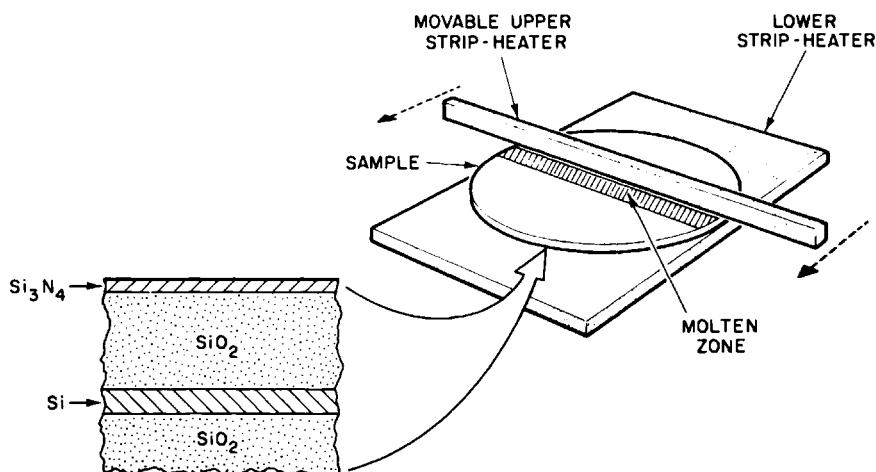


FIG. 24. Schematic of the graphite strip heater process. [From Geis *et al.* (1982a).]

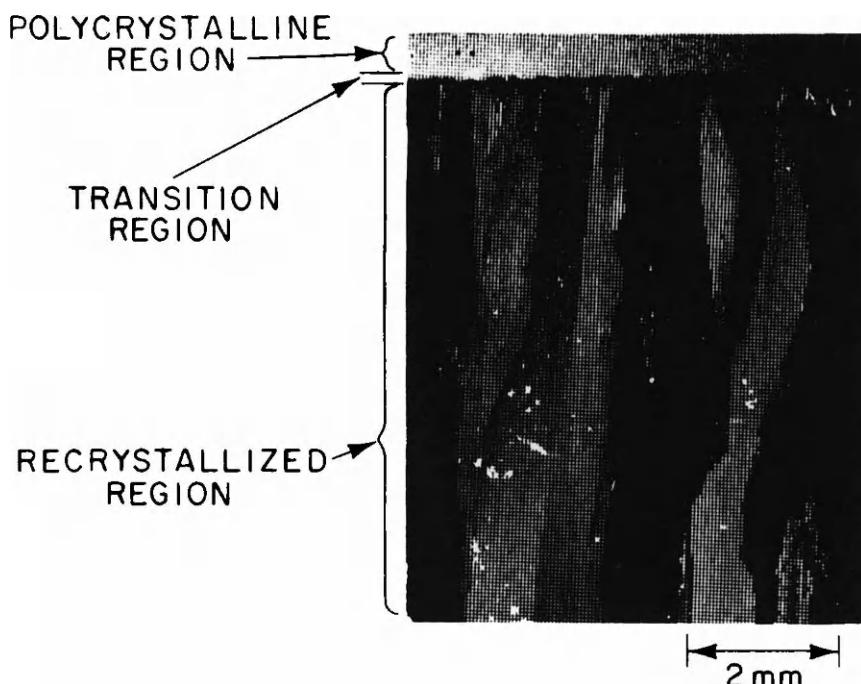


FIG. 25. Optical micrograph of lateral epitaxial film grown with a graphite strip heater process: low magnification showing large-grain polycrystalline structure. [From Geis *et al.* (1982a).]

5.3.2 Defect Characterization

The prominent defects in SOI films formed by this technique are grain boundaries and very low angle grain boundaries (or subboundaries). Grain boundaries are usually formed in unseeded growth (see, for example, Figs. 20b and 25). These grain boundaries are formed due to seeding from a multitude of grains of different orientation. They can be eliminated by using either a single-crystal seed as described earlier or by a variety of grain boundary filtration techniques (Atwater *et al.*, 1982).

Even though grain boundaries can be eliminated, subboundaries have so far eluded efforts to eliminate them. Typical subboundaries are shown in Fig. 26, which also shows an "etch-pit grid" technique to delineate defects in thin-film SOI material (Glis *et al.*, 1982a). In this technique, small openings are etched in an oxide mask on top of the SOI film. The

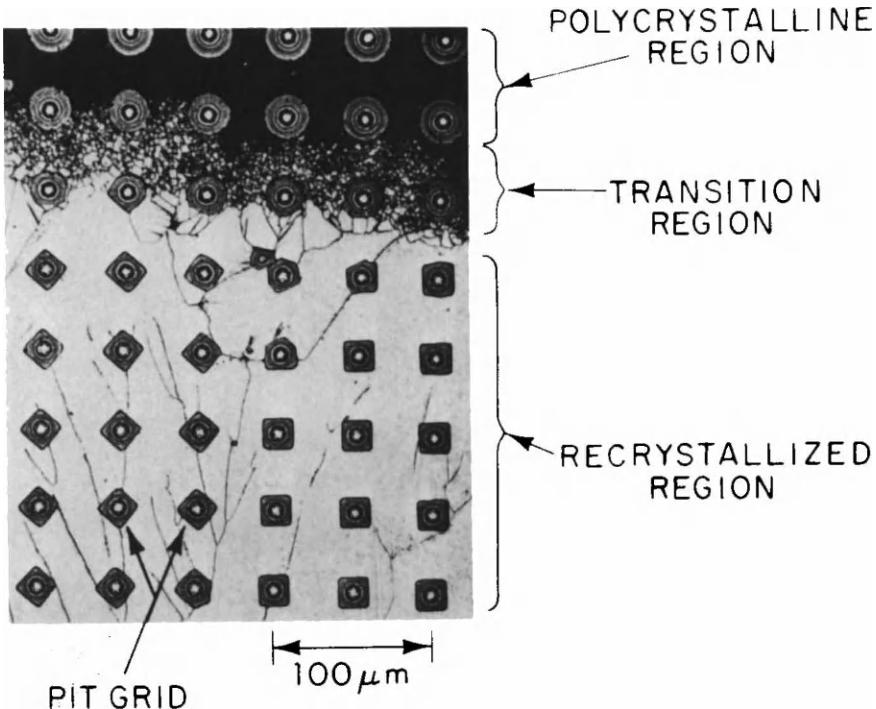


FIG. 26. Optical micrograph of lateral epitaxial film grown with a graphite strip heater process: a grid array of etch pits has been etched to reveal grain boundaries and defects within grains. Note that a subboundary does not alter the shape of the etch pit that it intersects. [From Geis *et al.* (1982a).]

SOI film is then subjected to an orientation-dependent etch such as KOH, which etches silicon very rapidly along {100} surfaces and slowly along the {111} surface. The net result is that etch pits are formed on {100} surfaces with edges along [110] directions. Hence, if a linear defect in the SOI film is a grain boundary, an "etch-pit" that is intercepted by a grain boundary will not be square. In Fig. 26, there are many "etch-pits" that are intercepted by a linear defect but still maintain their square shape. These defects are the subboundaries. Misorientation across one such subboundary has been measured to be less than 0.5 degree (Pinizzotto *et al.*, 1982). These subboundaries are actually formed by the coalescence of dislocations. Individual dislocations within a subboundary can be imaged by TEM (Pinizzotto *et al.*, 1982).

The formation of these subboundaries has been identified with the faceting of the growth front (solid–liquid interface) (Geis *et al.*, 1982b). In this experiment, the molten silicon is temporarily frozen by a burst of helium gas injected at the melt–solid interface. As a result, an approximate demarcation of the instantaneous solid–liquid interface is produced. An example of such an experiment is shown in Fig. 27a. The facets are close to {111} planes. The micrographs illustrate that subboundaries originate at the interior corners of the faceted solid–liquid interface. A similar demarcation was obtained by electrical pulsing and is shown in Fig. 27b.

Presently, there are two schools of thought on the causes for the formation of these subboundaries. Constitutional supercooling is the thesis of one (Fan *et al.*, 1984) while stress relief is the primary focus of the other (Lam *et al.*, 1981). Low-pressure chemical vapor deposition is commonly used for the deposition of polysilicon for SOI. During an LPCVD process, impurities (mostly carbon and oxygen), are incorporated in the film. As the solid freezes from the melt, these impurities are rejected into the liquid immediately in front of the growth front due to segregation effects. This causes the impurity concentration to increase, thereby lowering the freezing point of this region, resulting in the liquid being in a supercooled condition. This supercooled condition can be sustained if the temperature gradient is steep enough (Fig. 28). However, in most experimental conditions encountered, this is not the case. Hence, dendritic growth results, and subboundaries are formed when these dendrites merge. There is evidence that supports this theory since very high concentrations of impurities are found at the subboundaries. An example is shown in Fig. 29 (Fan *et al.*, 1984).

Alternatively, it is believed that due to the change in volume in silicon during the melting or freezing process, stress is built up within the thin

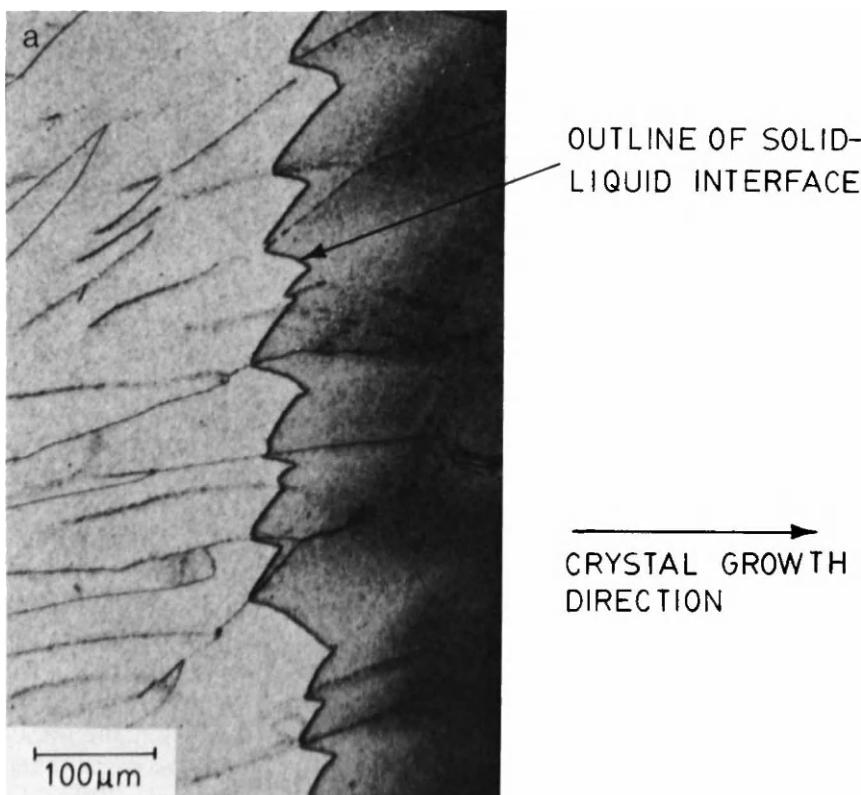


FIG. 27. Optical micrographs of lateral epitaxial films grown using the strip heater process. (a) The molten silicon was suddenly cooled by a helium jet during the course of the melting process. It was believed that the sudden cooling produced an approximate demarcation of the instantaneous solid-liquid interface. The facets are close to (111) planes. The micrograph illustrates that subboundaries originate at the interior corners of the faceted solid-liquid interface. (b) A similar demarcation was obtained by electrical pulsing. [From Geis *et al.* (1982b). Reprinted by permission of the publisher, The Electrochemical Society, Inc.]

film. Point defects will diffuse along stress gradients and coalesce to form a dislocation. Further coalescence of these defects results in the formation of subboundaries (Lam *et al.*, 1981; Pinizzotto *et al.*, 1982).

Presently, it is believed that a combination of these two effects is responsible for the formation of these subboundaries. This is still an area of active research and more detailed results are needed to confirm these theories.

The liquid-phase process is driven by temperature gradients, which in turn cause another problem. When the silicon substrate is subjected to a



FIG. 27. (continued)

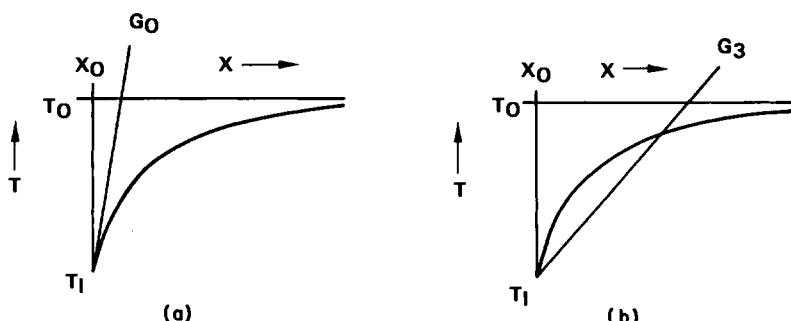


FIG. 28. Thermal conditions at the solid-liquid interface. The curved lines illustrate the melting point of the liquid as a function away from the interface (X_0). The melting point is depressed at the interface due to supersaturation with impurities rejected from the solid. The straight lines illustrate the actual temperature gradients. (a) Planar growth front is obtained because the actual temperature gradient is steep enough to prevent supercooling. (b) Dendritic growth results due to supercooling as temperature gradient is not steep enough.

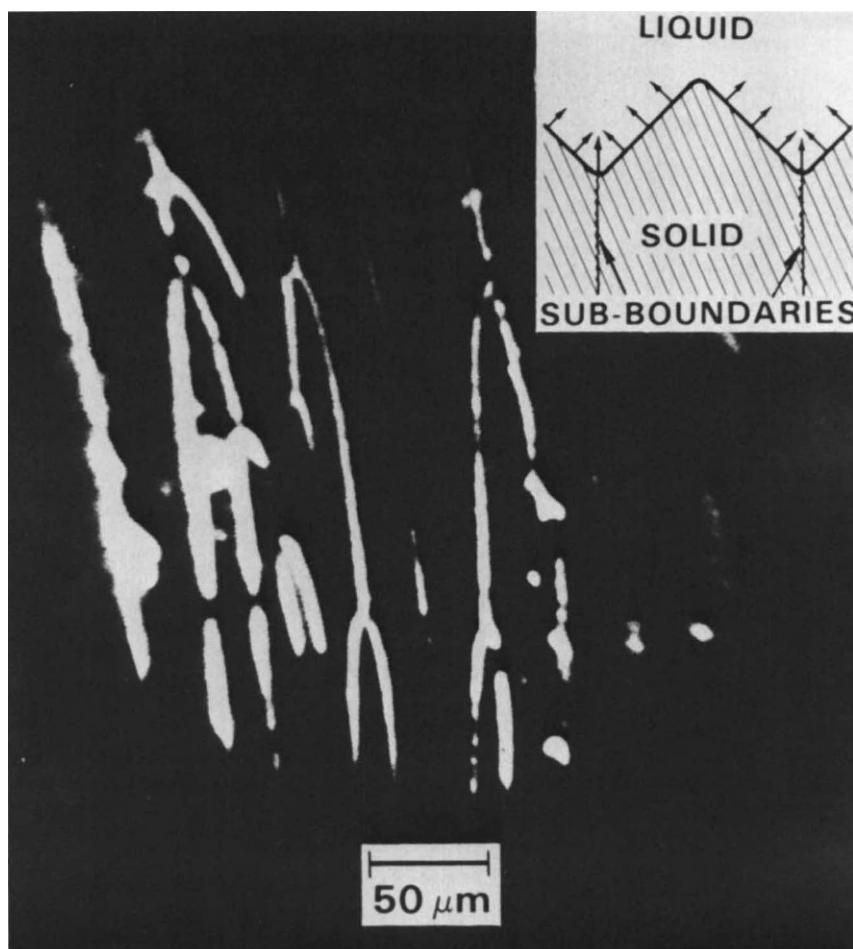


FIG. 29. Oxygen map obtained by SIMS, showing that oxygen concentration is highest at the subboundaries. Inset is a schematic diagram showing faceted interface with increased impurity concentration in liquid at inner corner, where subboundary originates. [From Fan *et al.* (1984).]

large temperature gradient, slip lines will form to relieve the stress built up in the wafer. In more severe cases, the wafer will be warped immediately after the melting and crystallization process. Wafer warpage will prevent the wafer from being used in any subsequent device fabrication. In less severe cases, the wafer is not warped sufficiently to prevent further processing although slip lines are already formed. However, on subsequent thermal cycling, wafers with slip lines are more likely to deform, causing severe difficulties in photolithographic alignments. While the graphite strip heater process is more susceptible, all wafers that are processed with the liquid phase process will have this problem.

5.3.3 Liquid-Phase Growth with a Stationary Heat Source

A modified liquid-phase growth technique has been used to grow very thick silicon films on thick insulators for high-voltage applications. This process has been called lateral epitaxial growth over oxide (LEGO) (Celler *et al.*, 1983). This approach uses a stationary heat source, primarily a bank of high-intensity tungsten-halogen lamps, on top of the wafer. Radiative cooling from the back side establishes a small temperature gradient across the wafer of about 5°C. Since thermal conductivity in silicon is about 100 times higher than that of its oxide, temperature gradients within the wafer are established vertically through the seeding contacts and laterally outward along the top silicon film from the seed areas. A cross section of a typical sample is shown in Fig. 30. This sample was deposited using an epitaxial process based on the decomposition of silane. Hence, the deposited film grows epitaxially on the seed region and is polycrystalline on the oxide.

When heat energy of typically 75 W/cm^2 is supplied to this sample for about 10 sec, the entire deposited layer and a part of the silicon substrate melt. The integrity of the wafer is maintained by a delicate balance between the heat energy supplied and the radiative cooling from the back side. However, once operating conditions are established, they are quite reproducible. Upon removal of the heat source, epitaxial growth proceeds from the molten silicon in the substrate upward through the seeding area. Growth proceeds through the seed area and spreads laterally into the SOI area. The resulting silicon-on-oxide area is single crystal with the same orientation as the substrate. An example is shown in Fig. 31. As is inherent to any liquid-phase growth process, when the solidification fronts from two seed regions collide, defects are formed. Furthermore, because of the volume expansion encountered when molten silicon freezes, there will be excess silicon protruding from the surface at the locations where these fronts collide. Hence, it is necessary to polish off the protruding material

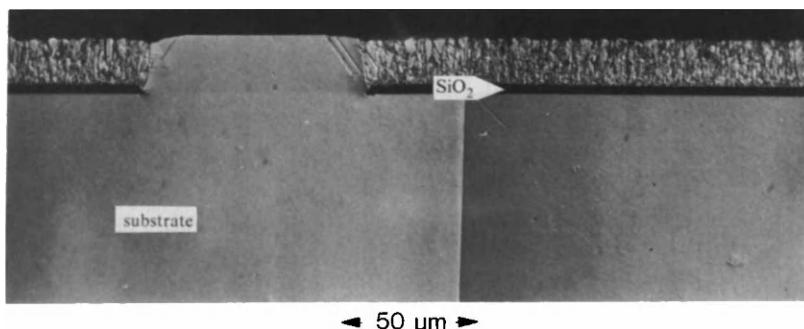


FIG. 30. Cross section of an as-deposited LEGO structure after a 10-sec Schimmel etching. [From Cellar *et al.* (1983).]

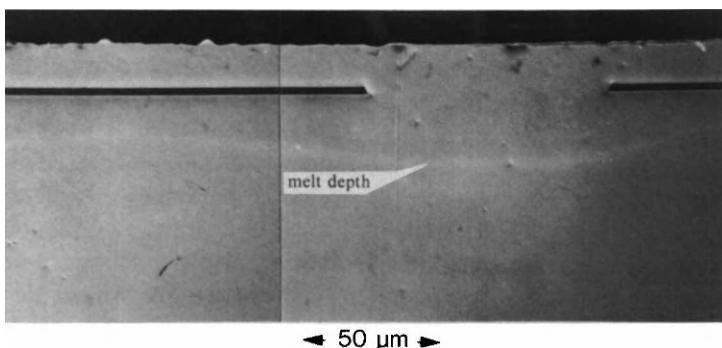


FIG. 31. Etched cross section of epitaxially grown LEGO sample. Defects are scarcely found. [From Cellar *et al.* (1983).]

in order to obtain a flat surface. Compared to a conventional dielectric isolation approach, the amount of silicon material to be removed by polishing is significantly smaller.

5.3.4 Device Characteristics

The SOI material produced with the liquid-phase process has been used to produce both MOS (Tsaur *et al.*, 1982a) and bipolar experimental devices, (Rodder and Antoniadis, 1983). In general, the carrier mobility obtainable in the SOI material is related to the number of grain boundaries in the active channel region and whether the grain boundaries are perpendicular or parallel to the flow of the carriers (Tsaur *et al.*, 1982b). In general, a defect represents a potential barrier for the carriers (holes or electrons). For a defect with a higher degree of disorder (such as a grain boundary), the electrical potential barrier is higher due to a higher interface trap density within the defect. For a defect with a lower degree of disorder (such as a subboundary or an isolated dislocation), the electrical barrier is lower. This is consistent with the electrical measurements obtained. The carrier mobility in laser-processed material without seeding (primary defects are grain boundaries) is about one-half or one-third of that in graphite strip heater processed material or laser processed material with seeds (primary defects are subboundaries and dislocations).

When the SOI materials were first used to produce MOS devices, an anomalous effect in the leakage current was observed (Kamins and von Herzen, 1981). This is shown in Fig. 32. The leakage current in long channel length devices is well behaved and independent of channel length. However, as the channel length is reduced, the leakage current increases rapidly. This phenomenon is related to the enhanced diffusion of dopants from the source and drain regions of the device along defects in the channel regions. This explanation has been confirmed experimentally (Johnson *et al.*, 1981). These experimental results are reproduced in Fig. 33 which

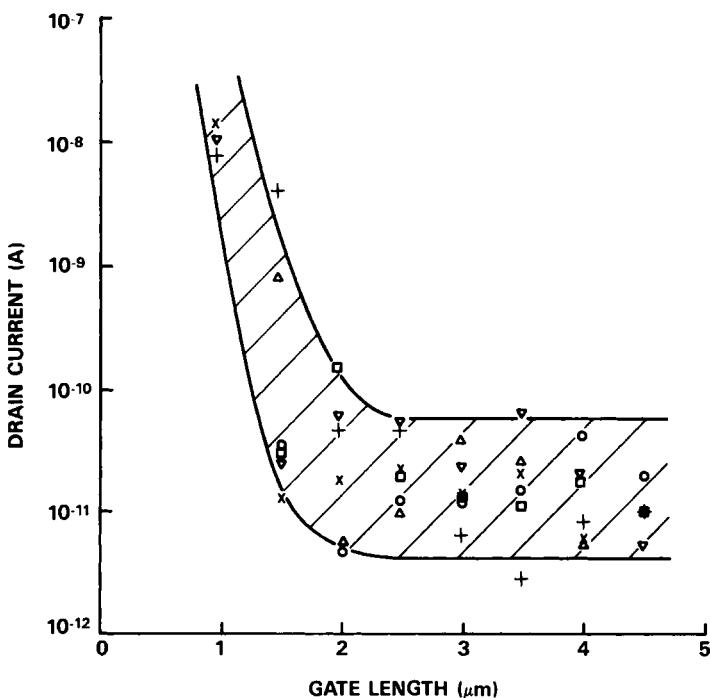


FIG. 32. Leakage current in MOSFETs as a function of channel length. MOSFETs were fabricated in SOI grown with lateral epitaxy using a scanning electron beam. [From Kamens and von Herzen (1981). Copyright © 1981 IEEE.]

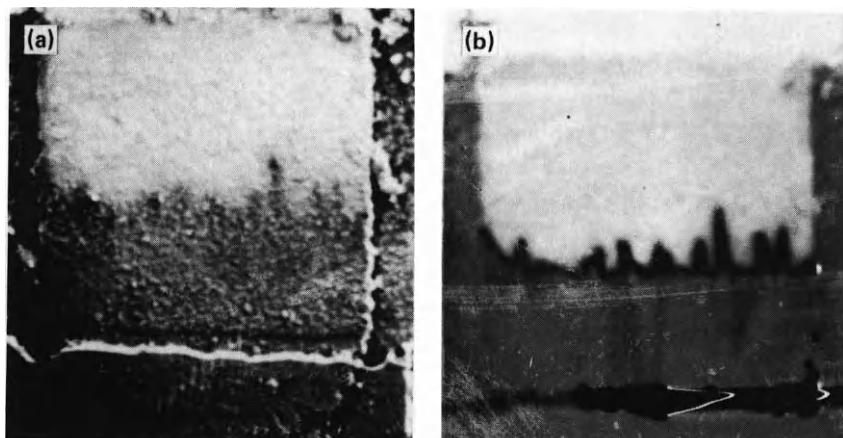


FIG. 33. Comparison of (a) voltage contrast and (b) electron beam induced current images of a lateral $p-n$ junction diode fabricated in laser-induced lateral epitaxial SOI material. Island width is 24 μm . The protrusions are an indication of enhanced dopant diffusion along grain boundaries. [From Johnson *et al.* (1981).]

compares scanning electron micrographs under voltage contrast and under electron beam induced current (EBIC) of a $p-n$ junction in an SOI material processed with a laser. The protrusions of low efficiency (dark regions) in EBIC are due to enhanced arsenic diffusion along grain boundaries and the concomitant doping of grains in the regions immediately adjacent to these arsenic-rich boundaries. It was estimated that the diffusion along grain boundaries is about 3 to 4 orders of magnitude higher than that in ordinary silicon material.

5.4 LATERAL EPITAXY FOR SOI: SOLID-PHASE PROCESS

5.4.1 Solid-Phase Epitaxy

It was observed that by depositing an amorphous silicon layer in high vacuum on a clean silicon surface and annealing the deposited layer *in-situ*, the deposited layer was transformed to a single-crystal layer (Roth and Anderson, 1977). If the experiment was performed carefully to maintain an atomically clean surface and to ensure a high vacuum to avoid contamination, very high-quality single-crystal layers can be obtained. Figure 34 shows an RBS channeling spectrum of such an epitaxial film. The deposited amorphous silicon regrows epitaxially because the crystalline form is the stable equilibrium phase with the lowest energy. The competing process is one of crystalline nucleation within the amorphous silicon film, which will result in polycrystal formation. The crystalline-amorphous interface progresses through the amorphous layer by annealing at temperatures between 500°C to 600°C. The low temperatures are chosen to minimize the crystalline nucleation rate while maintaining enough atomic mobility to permit the amorphous to crystalline phase transformation. The driving force for solid-phase epitaxy (SPE) is the free energy of the phase transformation.

5.4.2 Lateral Solid-Phase Epitaxy

A structure such as one shown in Fig. 35 has been studied to extend SPE laterally into amorphous silicon deposited onto an oxide layer as a means to obtain SOI. This concept is quite similar to the seeded liquid-phase growth discussed in the previous section. However, in this case, a temperature gradient is not required to drive the lateral growth. Since lateral SPE (L-PSE) can proceed at temperatures around 600°C, it is an attractive process for producing SOI, especially for 3D ICs. A low-temperature process will result in less dopant redistribution and also induce

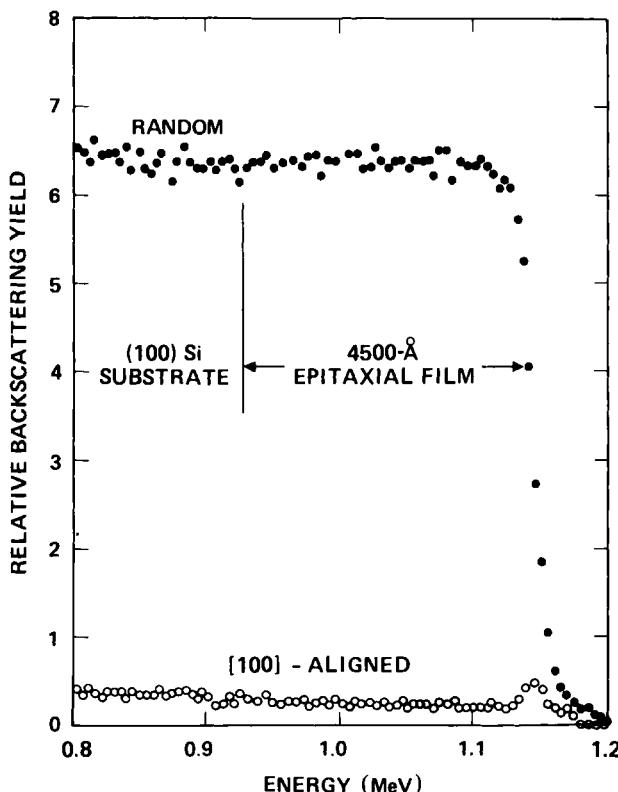


FIG. 34. 2-MeV He⁺ channeling spectra of an epitaxial silicon grown by SPE at 525 \pm 25°C for 2 h. [100]-aligned (channeled) data are shown by open circles, the non-aligned (random) yield by solid dots. [From Roth and Anderson (1977).]

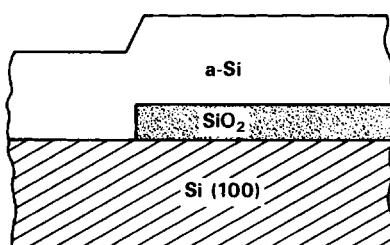


FIG. 35. Lateral SPE for SOI.

less stress in the wafer. This will overcome most of the limitations of the liquid-phase process discussed earlier.

Lateral SPE experiments have been successfully demonstrated by several groups (Ohmura *et al.*, 1982; Yamamoto *et al.*, 1983; Kunii *et al.*, 1983). A typical example is shown in Fig. 36 (Yamamoto *et al.*, 1983). Sample A was prepared by electron-beam evaporation in high vacuum (less than 5×10^{-6} Pa at 500°C). The deposited silicon-on-silicon region was epitaxial while the deposited silicon-on-oxide region was polycrystalline. The polycrystalline layer was subsequently amorphized by implantation with silicon ions. Sample B was prepared in the same vacuum chamber except that the deposition was performed at room temperature. Hence, the entire deposited film was amorphous. Furthermore, it was found that the film was less dense. The samples in Fig. 36 have been etched in a Wright etch to delineate the boundaries between the crystalline and polycrystalline regions. The L-SPE SOI regions can be clearly distinguished adjacent to the silicon-on-silicon seed regions. The amount of lateral growth increases with time of anneal. In addition, L-SPE in sample A is more extensive compared to sample B. Moreover, facetlike surfaces can be discerned at the boundaries between L-SPE growth and the polycrystalline regions.

It is believed that L-SPE is more successful in sample A because the deposited silicon material is more dense as it was deposited at an elevated temperature. Similar results have been observed in silicon material deposited using the CVD method (Kunii *et al.*, 1982).

The length of the L-SPE region has been plotted as a function of annealing time in Fig. 37 for two samples deposited with method A, with seed windows aligned along the $\langle 010 \rangle$ and the $\langle 011 \rangle$ directions. The growth rate in the $\langle 010 \rangle$ samples exhibits two distinct regions, an initial region characterized by a growth rate of 3.1×10^{-8} cm/sec and a second region characterized by a growth rate of 1.2×10^{-8} cm/sec. The $\langle 011 \rangle$ sample is characterized by only one growth rate which is the same as the second rate in the $\langle 010 \rangle$ case.

It has been shown (Kunii *et al.*, 1984) that (111) and (110) facets are formed during L-SPE growth along $\langle 011 \rangle$ and $\langle 010 \rangle$ directions, respectively. The vertical SPE growth rate on (111) surfaces has been observed to be 1.8×10^{-8} cm/sec at 600°C (Yamamoto, *et al.*, 1984) and is very close to the measured rate of 1.2×10^{-8} cm/sec measured here for L-SPE growth. Hence, it is believed that L-SPE along $\langle 011 \rangle$ proceeds by growth along (111) surfaces. The vertical SPE rate on (110) surfaces has been measured to be 4.7×10^{-8} cm/sec at 600°C (Yamamoto *et al.*, 1984). This rate is comparable to the growth rate of 3.1×10^{-8} cm/sec measured for the initial growth rate along the $\langle 010 \rangle$ direction. Hence it is believed that along

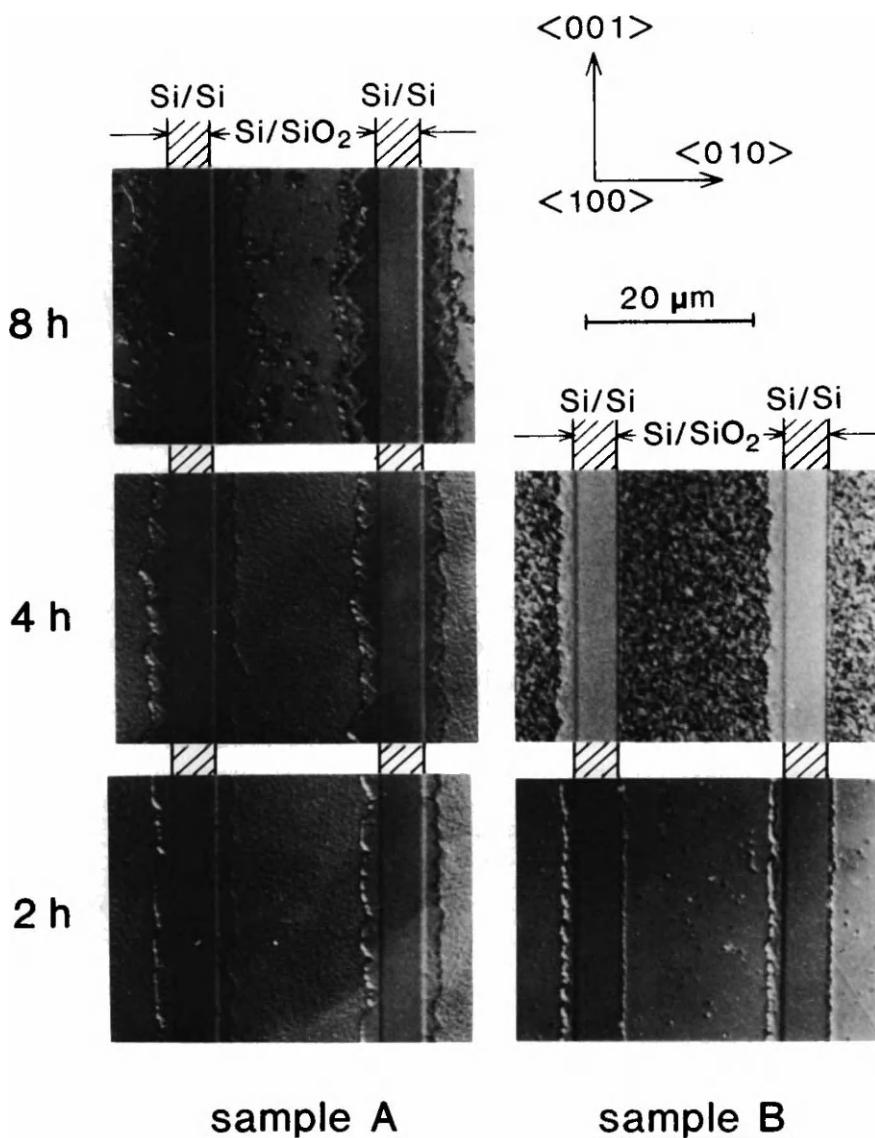


FIG. 36. Nomarski optical micrographs for samples annealed at 600°C. Sample A was deposited at a higher temperature and, hence, is more dense. Sample A films were then amorphized by silicon ion implantation. Sample B was deposited at room temperature as amorphous films. [From Yamamoto *et al.* (1983).]

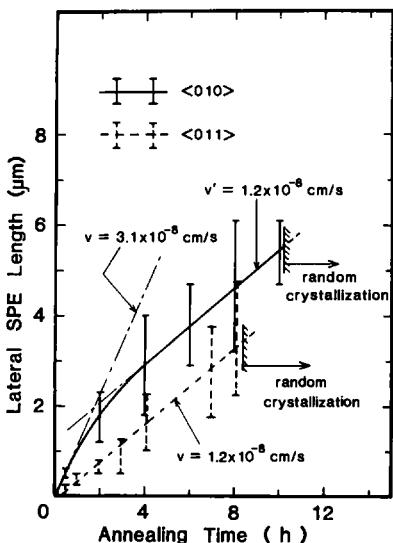


FIG. 37. L-SPE length as a function of anneal time. Annealing temperature = 600°C. [From Yamamoto *et al.* (1983).]

the $\langle 010 \rangle$ direction, initial L-SPE proceeds along (110) facets and eventually rotates to the (111) facets. This faceting is observed in Fig. 36. However, because of the lower L-SPE growth rate experimentally observed, it is believed that the growth front in L-SPE is more complicated than is suggested by a simple (111) faceting model (Yamamoto *et al.*, 1984).

Faceting has also been observed in L-SPE when the surfaces between the seed region and the oxide supporting the amorphous silicon are not level. This is demonstrated in Fig. 38 (Tamura *et al.*, 1984).

The extent of L-SPE depends on the growth rate as well as on the control of random nucleation. The incubation time (time to nucleation) shown in Fig. 37 varies for different samples, and the controlling mechanisms are not well understood. It is possible that the temperature and ambient of anneal, the density and the impurity level of the deposited amorphous silicon layer, flaws in the surfaces of the amorphous silicon film, and foreign objects in the film may be responsible for the variability in the incubation period. This is still an area of active research.

One possible application of L-SPE is shown in Fig. 39, which shows a stacked CMOS structure. In a stacked CMOS inverter, a *p*-channel device is stacked on top of and shares the same gate with an *n*-channel device. A polysilicon *p*-channel device has been used in a static random access memory application where a relatively low performance device can be used. For stacked CMOS to be widely applicable, a single-crystal *p*-channel device is required. Lateral SPE is an ideal candidate for this application as a seed is readily available in a stacked CMOS structure.

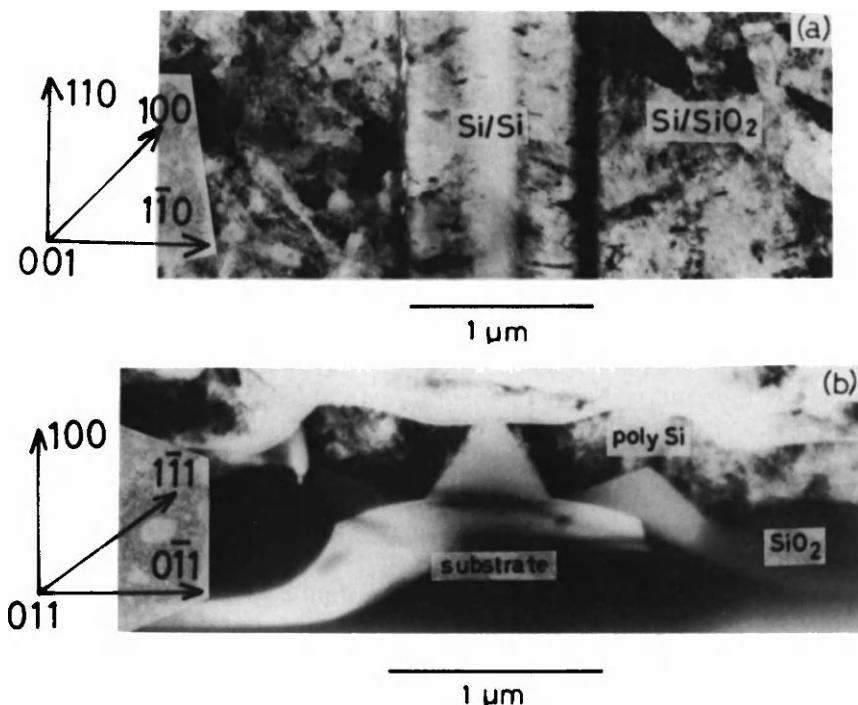


FIG. 38. TEM micrograph showing defects generated at the oxide edge in a $\langle 110 \rangle$ -directed stripe-oxide cut L-SPE sample. [From Tamura, *et al.* (1984).]

Furthermore, in VLSI the scaling in feature size implies that the amount of L-SPE growth required to achieve single crystal in the channel region of the *p*-channel device is on the order of several micrometers. Hence, the results demonstrated by Yamamoto, *et al.* (1984) are already sufficient for device application. However, L-SPE seems to be intolerant to large steps in the growth path (Tamura *et al.*, 1984). Hence, proper planarization is essential for desired L-SPE growth. Furthermore, more reproducible L-SPE results need to be demonstrated.

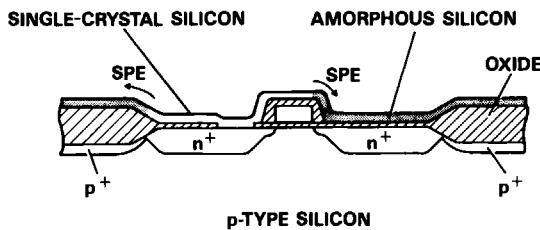


FIG. 39. Application of L-SPE to stacked CMOS.

5.5 LATERAL EPITAXY FOR SOI: VAPOR-PHASE PROCESS

5.5.1 Epitaxial Lateral Overgrowth

The epitaxial lateral overgrowth (ELO) method for obtaining SOI using a vapor-phase process is shown in Fig. 40. In this approach, a dielectric layer, preferably oxide, is grown on a silicon wafer. Windows are then cut in this dielectric layer, exposing the underlying silicon. An epitaxial layer is then grown using a CVD process. If the epitaxial process is chosen properly, the initial growth will nucleate on the silicon in the window regions only and not on the oxide layer (selective epitaxy). After the epitaxial layer has built up above the window region, it would be desirable to adjust the epitaxial growth conditions to extend the epitaxial growth laterally over the oxide regions adjacent to the windows. In this phase of growth, it is desirable to have a high lateral growth velocity to vertical growth velocity ratio. In addition, random nucleation on the exposed oxide regions should be discouraged. If sufficient lateral overgrowth is accomplished to obtain a wide enough SOI region to support device fabrication, successful ELO is accomplished. Hence suppression of nucleation on oxide-covered surfaces and large lateral to vertical growth ratio are the two most important elements in the ELO process.

It has been observed that when a dielectric layer is exposed to a supersaturated silicon gas, nucleation of silicon on the dielectric is not spontaneous, but is delayed by an incubation period, (Fig. 41) (Claasen and Bloem, 1980a). After this incubation period, the density of nuclei increases very rapidly to the saturation density and does not change substantially with time. The incubation period is different for different dielectric surfaces and is longer for an oxide surface than for a silicon nitride surface because of a higher density of free surface adsorption sites for nuclei formation on nitride. The incubation period also increases with increasing concentration of HCl in the growth ambient because HCl etches the adsorbed nuclei, thus reducing their growth rate. HCl also has the effect of

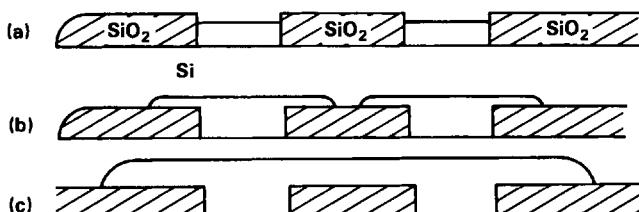


FIG. 40. Schematic representation of the ELO process: (a)-(c) represent different stage of growth. [From Jastrzebski (1983). Copyright 1983 North-Holland Publ. Co., Amsterdam.]

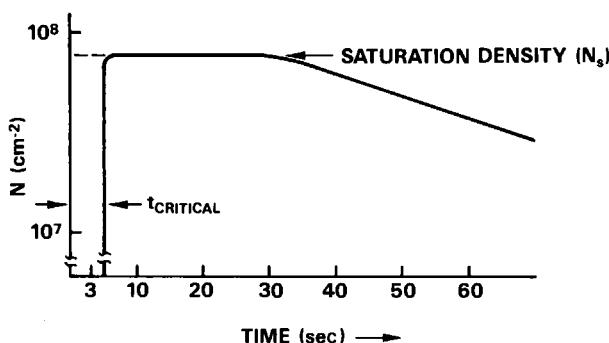


FIG. 41. Density of polysilicon precipitates as a function of time: $\text{SiH}_4 (8.8 \times 10^{-4}$ bar) and $\text{HCl} (4.4 \times 10^{-3}$ bar) at 1000°C on a SiO_2 substrate; H_2 is the carrier gas. [From Claasen and Bloem (1980a). Reprint by permission of the publisher, The Electrochemical Society, Inc.]

increasing the critical size of the nuclei. The incubation time decreases with increasing growth temperature since a higher temperature increases the surface mobility of the adsorbed atoms, requiring less time for polysilicon condensation. The incubation time also decreases with increasing concentration of the feeder gas such as SiH_2Cl_2 again because of a higher condensation rate (Claasen and Bloem, 1980a; Jastrzebski *et al.*, 1982a).

The saturation density of nuclei is dependent on the surface of the dielectric and is typically much smaller on an oxide surface than on a nitride surface (Claasen and Bloem, 1980b). This effect is a result of the fact that in the presence of hydrogen, adsorbed silicon will react with silicon dioxide and reduce it to SiO . This acts as a competing process for nucleation. The saturation density is much lower if hydrogen is used as the carrier gas instead of nitrogen. In addition to the above-stated reaction, atomic hydrogen will also be adsorbed at surface sites, reducing available sites for silicon adsorption. The saturation nuclei density is also dependent on the growth temperature and the gas used. This effect is illustrated in Fig. 42. It is noteworthy that the temperature dependence of the nuclei density is different in silane than in the chlorosilanes (Claasen and Bloem, 1980b). This is a result of the fact that the decomposition of chlorosilane compounds decreases rapidly with decreasing temperature in the presence of hydrogen. However, in the case of the silane/ H_2 system, the decomposition is not very temperature sensitive in that temperature range, and the nuclei density is affected primarily by the surface mobility of the adsorbed silicon atoms.

With these discussions, we can establish a set of experimental conditions to ensure selective epitaxial growth. These conditions are shown in

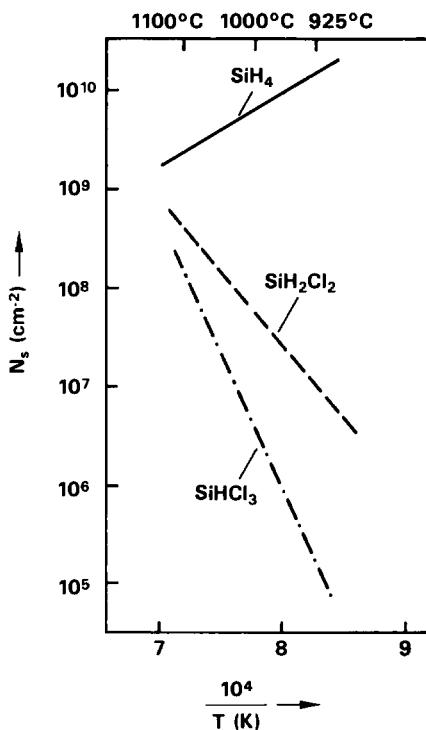


FIG. 42. Density of polysilicon nuclei on an SiO_2 substrate as a function of growth temperature for SiH_4 , SiH_2Cl_2 , SiHCl_3 , and H_2 is the carrier gas. [From Claasen and Bloem (1980b). Reprint by permission of the publisher, The Electrochemical Society, Inc.]

Fig. 43 for the $\text{SiH}_4/\text{HCl}/\text{H}_2$ system (Claasen and Bloem, 1981). In addition, oxide is the preferred dielectric for its low density of nucleation sites.

The preceding discussion has so far ignored the important effects of heterogeneous nucleation of polycrystalline silicon material on the dielectric surface. Heterogeneous nucleation occurs at sites on the dielectric surface with imperfections, and the nucleation rate generally follows the same trend as that of homogeneous nucleation. In order to reduce heterogeneous nucleation, a clean dielectric surface is essential. However, in practice, defects and particulates do occur on the dielectric surface, and in spite of the suppression of homogeneous nucleation, heterogeneous nucleation usually is the limiting process for selective epitaxial growth. Because of this, a sequential grow and etch process was developed. (Jastrzebski *et al.*, 1982b).

In this process, a short HCl etch cycle follows a growth cycle. The growth cycle is chosen empirically for a particular set of growth conditions and dielectric surface so that nucleation just begins to occur. An etch cycle immediately follows and is so chosen (again empirically) so that the pre-

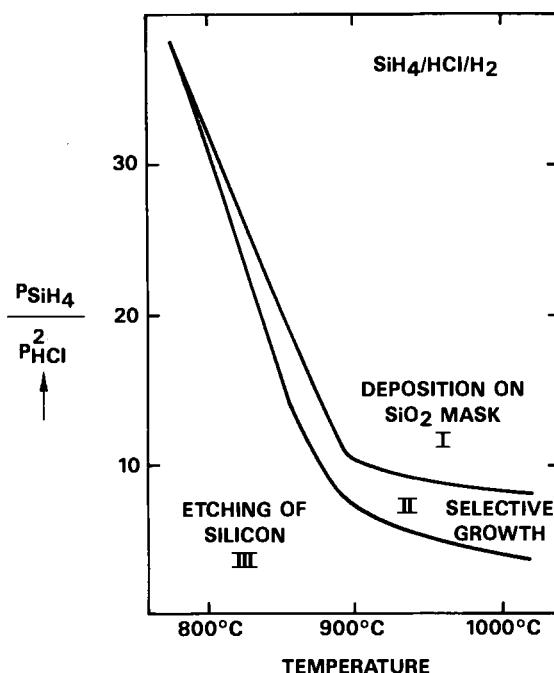


FIG. 43. Dependence of nucleation on temperature and the concentration of SiH_4 and HCl in hydrogen. Region I, deposition on SiO_2 ; region II, selective growth; region III, etching of silicon. [From Claassen and Bloem (1981). Reprint by permission of the publisher, The Electrochemical Society, Inc.]

viously formed nuclei can be completely removed. During the etch cycle, the nucleated polysilicon particles will etch much faster than the epitaxial silicon because of a larger surface to volume ratio. Hence, the successive growth and etch processes will result in a highly selective growth.

In the initial part of the growth period when $t < t_{critical}$, the horizontal growth velocity has been observed to be as high as 40 times that of the vertical growth velocity (Rathman *et al.*, 1982). The velocity of vertical growth is limited by the diffusion of the reactants along the gradient set up due to the depletion of reactants at the surface during growth. In the horizontal growth direction, however, no depletion of reactants occurs along the dielectric surface as nucleation on the dielectric surface has not occurred. Hence, the horizontal epitaxial growth rate is limited by the reaction rate on the surface, resulting in a much higher growth rate.

For $t > t_{critical}$, nucleation occurs on the dielectric surface and, hence, depletes the reactants immediately above the horizontal growth front.

Once this occurs, the growth rate is limited by diffusion. However, the horizontal growth rate can still be higher than the vertical rate due to diffusion of adsorbed silicon atoms towards the growing interface along the dielectric surface. However, as the horizontal growth fronts from two adjacent dielectric windows approach each other, the dielectric surface area for adsorption and subsequent diffusion of silicon atoms is reduced, decreasing the number of silicon atoms reaching the growing surface and, hence, the growth rate. This effect is illustrated in Fig. 44 (Jastrzebski *et al.*, 1983a).

As the growth surfaces, especially those with {100} orientation, from two seed windows approach and eventually collide with each other, voids may be formed. This effect is illustrated in Fig. 45. As the growth surfaces approach each other, the flux of silicon atoms reaching the bottom growing interface decreases as the gap is reduced. However, the top of the growing surface maintains its growth rate as the rate of silicon atom arrival is unchanged. Eventually, the top portion of the growth surfaces meet and pinch off any further growth at the bottom surface, resulting in a void. Void formation may not occur for growth surfaces that are faceted with (101), (111), (311), or (511) surfaces. These facets recess the top of the lateral growing surface, avoiding pinchoff of the bottom surface. In these cases, however, a depression is formed when the two growth surfaces meet.

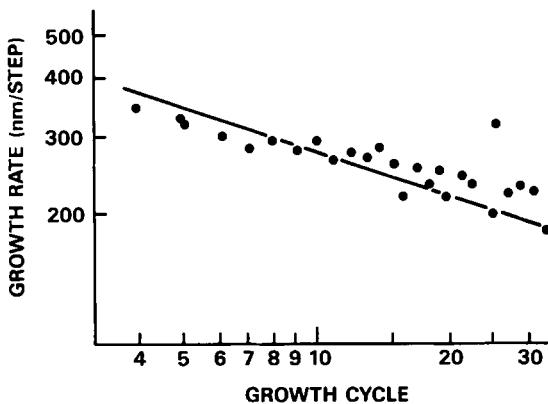


FIG. 44. Lateral growth rate as a function of the number of growth steps (growth time) for ELO growth over 20- μm wide SiO_2 islands oriented along the [010] direction on a (100) substrate. Growth conditions chosen to support nucleation on SiO_2 mask. [From Jastrzebski *et al.* (1983a). Reprint by permission of the publisher, The Electrochemical Society, Inc.]

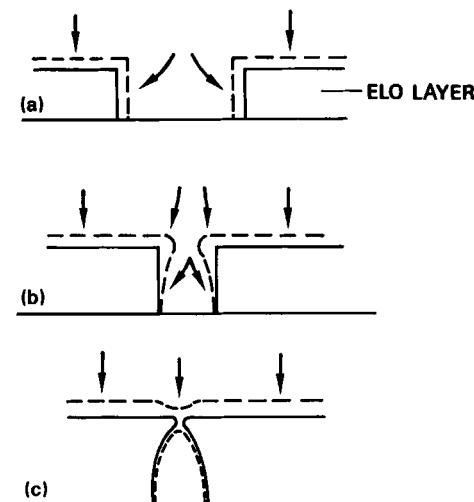


FIG. 45. Schematic representation of void formation at the SiO_2 interface upon completion of the ELO process. Arrows represent flux of silicon atoms to the growing interface. Solid line marks interface prior to the growth cycle, dashed after completion of the cycle. [From Jastrzebski (1983). Copyright 1983 North-Holland Publ. Co., Amsterdam.]

5.5.2 Defects in ELO Films

In growing ELO films, high-quality monocrystalline films can be obtained if the growth and etch cycles are controlled properly. If a growing surface encounters and engulfs a nucleated polysilicon particle during a growth cycle, a polycrystalline inclusion is formed. In the worst case, the film becomes polycrystalline. Even if the growth and etch cycles are chosen properly, the presence of the dielectric layer causes defect formation due to the difference in the coefficients of thermal expansion between the dielectric and silicon. This difference results in a strain in the material that creates a stress field for defects to nucleate and coalesce.

For ELO films grown on (100) substrates with the dielectric windows along the [100] directions, very high-quality lateral epitaxial films can be obtained. An example is shown in Fig. 46. In Fig. 46 only isolated dislocations can be found. The void characteristic of laterally growing {100} surfaces can also be seen (cf. Fig. 45). However, if the oxide windows are along the [110] direction, highly defective epitaxial layers are formed.

It is believed that defects will form along high-stress points in the structure, especially at the interface between the dielectric layer and silicon. In the case of dielectric edges along the [110] directions, once defects

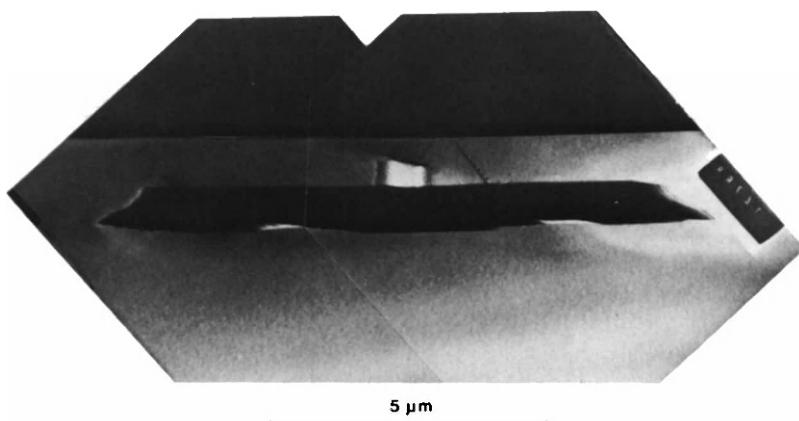


FIG. 46. Typical cross-sectional TEM micrograph of an ELO film grown over 6- μm wide SiO_2 islands oriented along $[010]$ for (100) substrate, under conditions that suppress nucleation on SiO_2 . [From Jastrzebski (1983). Copyright 1983 North-Holland Publ. Co., Amsterdam.]

are nucleated along the high-stress points, they can glide along the $\{111\}$ planes and coalesce into more extensive defects. However, in the case of a dielectric with edges along the $\langle 100 \rangle$ plane, higher energy is required to nucleate and grow defects, and, hence, less defects are formed for the same growth conditions.

5.5.3 Device Applications

Because the ratio of horizontal to vertical growth velocity in a typical ELO process is 1.5, large-area thin-SOI films cannot be obtained. In order for CMOS on SOI application, a 0.3–0.5- μm thick SOI film is required. Hence, in this stage of development, ELO films are unsuitable for CMOS. Hence, only bipolar devices have been fabricated in this material to demonstrate the device properties of this material (Jastrzebski *et al.*, 1983b). Since the ELO process produces a high-quality silicon epitaxial film, the bipolar devices exhibited characteristics comparable to those fabricated in bulk silicon.

5.6 HETEROEPITAXY FOR SOI

The most common heteroepitaxial SOI system is silicon-on-sapphire (SOS) where (100) silicon epitaxial films are grown on thick $(\bar{1}\bar{0}2)$ sapphire

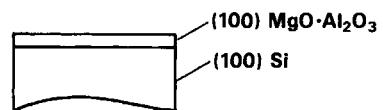
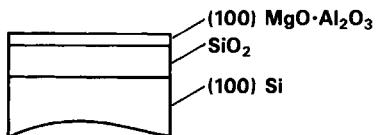
substrates. This subject is dealt with in chapter 4, and it will not be repeated here. Instead, this section will concentrate on the growth on silicon epitaxy on a foreign dielectric material that is in turn grown epitaxially on a silicon wafer.

This approach is more attractive than SOS for several reasons. Few available substrates not even sapphire, can match the thickness uniformity and flatness uniformity achievable in bulk silicon wafer. This flatness uniformity will be reproduced on an epitaxial layer. In VLSI where the patterning of very fine lines is required, a flat surface is absolutely essential for good yield. With a bulk silicon wafer as the substrate, the dielectric epitaxial layer, not the silicon epitaxial layer, is strained during thermal cycling, thus reducing the effects of strain on the electrical properties of the epitaxial silicon material. A wide variety of dielectric materials can be used. This allows a wider choice of dielectric material as the insulating layer to match its physical properties, such as the lattice constant and coefficient of thermal expansion, with those of silicon.

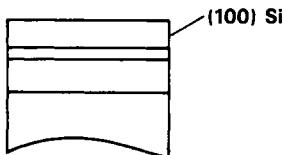
With the continued scaling of device feature sizes in VLSI, the thickness of the silicon layer is becoming thinner and thinner and the crystallinity at the silicon–dielectric interface is becoming more and more important. Unfortunately for heteroepitaxy, if lattice parameters are not matched, defects will be formed, especially at the interface. Another potential disadvantage of this approach is that these dielectric materials may create potential contamination and compatibility problems. These potential problems notwithstanding, there have been several attempts to produce SOI materials using spinel (Ihara *et al.*, 1982) and various fluoride compounds (Asno and Ishiwara, 1984).

An example of using spinel is shown in Fig. 47 (Mikami *et al.*, 1983). In this case, a relatively thin (less than 0.8 μm) spinel film is grown at 980°C on a silicon wafer. A thicker film will result in cracking of the spinel epitaxial layer due to mismatch in thermal expansion coefficients. In order to increase the thickness of the dielectric layer, an oxide layer is grown between the epitaxial spinel film and the underlying silicon substrate. This is possible because oxygen can diffuse through the spinel layer. Eventually, a silicon epitaxial layer is grown on the spinel layer.

Although a thinner spinel layer alleviates the cracking problem, it is also more defective compared with a thicker layer (Mikami *et al.*, 1983). Hence, subsequent silicon epitaxy is grown on a more defective seed. However, a thicker silicon epitaxial layer can be grown, where the defect density decreases with the thickness of the epitaxial layer. It has also been found that by growing the oxide film between the spinel and silicon substrate, the silicon epitaxial layer is strain free. It is possible that the silicon

(a) MgO·Al₂O₃ EPITAXIAL GROWTH

(b) THERMAL OXIDIZATION



(c) Si EPITAXIAL GROWTH

FIG. 47. Formation of a Si/Spinel/SiO₂/Si Structure. [From Mikami *et al.* (1983).]

dioxide layer provides a buffer layer to relieve the stress that otherwise would have been present in the spinel and silicon epitaxial layers.

This heteroepitaxial approach is still at a very early stage of development, and it is too early to judge its relative probability of success.

5.7 SUMMARY

In this chapter, we have reviewed the various epitaxial approaches used to produce SOI material. Different approaches will be used for different applications. For VLSI applications, the epitaxial growth on buried oxide material will be preferred because of its compatibility with conventional VLSI processes. In addition, it provides a uniform and reproducible material that is essential for high-volume manufacturing. Cost of the implantation process will be a non-issue when very high-current implanters (>100 mA) are available and when researchers in the field continue to invent new approaches to reduce the oxygen ion dose requirement.

The liquid-phase process is being pursued for applications in three-dimensional integration, high-voltage devices, and for silicon ICs on foreign substrates (such as glass). The disadvantage of this approach is that it is a high-temperature process. Hence, if it can be done as an initial part

of the process and the temperature gradients can be controlled so as to introduce insignificant amounts of substrate damage, the liquid-phase process can find applications in the above-mentioned fields.

SOI formed by the solid-phase approach is most attractive in three-dimensional applications. It is inherently a low-temperature process, and, hence, is most suitable for application where additional device layers needed to be added to existing structures. However, it must be proven that L-SPE can be performed without ultrahigh vacuum before it can be widely accepted as a viable approach.

The success of the vapor-phase method is limited by nucleation on the dielectric surfaces, which reduces the lateral to vertical growth ratio. Unless researchers can find a way to overcome this difficulty, it is unlikely that this approach will find wide application. It may be used, however, as part of a process flow to produce structures that may not otherwise be possible (such as selective epitaxial growth on silicon using a silicon dioxide window).

Heteroepitaxy will unlikely be a viable approach for VLSI. It may find applications in high-voltage devices or microwave devices. The more interesting applications are the growth of other semiconductors (such as GaAs or HgCdTe) on these dielectrics as a means of integrating different semiconductor systems onto a monolithic structure. However, much work is needed before this can become a reality.

Since 1979, an intense effort has been devoted to the field of SOI. It is fulfilling for the author as a participant to see this effort finally coming to fruition.

ACKNOWLEDGMENT

The author is grateful to B-Y. Mao and P-H. Chang for providing several TEM micrographs.

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