World of Wafers

_ SOI與Bulk Si的瑜亮情結_1

Silicon on Insulator vs Bulk Si
(on Planar and FinFETs)

王不老說半导

World of Wafers

_ SOI與Bulk Si的瑜亮情結_1

Silicon on Insulator vs Bulk Si (on Planar and FinFETs)

王不老說半导

瑜亮情結:牛頓與萊布尼茲的微積分之爭

- 長達二百年的歷史審判，最後的輸家是牛頓
- 被告的是英國皇家學會的外籍德國院士萊布尼茲，控方的背後主角是皇家學會會長牛頓，而委員會在調查的過程中也不請萊布尼茲來做說明，皇家學會的審判定了案，但歷史的審判才剛開始
- 英國的數學家執著於牛頓的微積分符號，難懂的極限觀念及《Principia》中的古典幾何表示法，自外於歐陸的進展而不自覺
- 等到1813年，英國才幡然夢醒，成立分析學社(Analytic Society)，採用萊布尼茲的符號與想法時，但已失去了科學研究的主導地位
- 蓋棺論定，萊布尼茲的微積分勝出， 斯坦福哲学百科全书稱他為絕世天才(universal genius)

http://episte.math.ntu.edu.tw/articles/sm/sm_17_04_1/index.html

萊布尼茲在棺材裡大笑勝出

The binary, or base 2, number system, expresses all numbers as a combination of the digits 0 and 1 (rather than the ten digits 0 - 9 used in the normal base 10 system).
It is a place value system, but rather than using units, tens, hundreds, thousands, etc (powers of 10), it uses powers of 2: 2, 4, 8, 16, 32, 64, etc.

Decimal	Binary
1	1
2	10
3	11
4	100
5	101
6	110
7	111
8	1000
9	1001
10	1010
...	

e.g. the binary number 110100101 is equivalent to:

1 x	256 =	256
1 x	128 =	128
0 x	64 =	0
1 x	32 =	32
0 x	16 =	0
0 x	8 =	0
1 x	4 =	4
0 x	2 =	0
1 x	1 =	1
		411

Binary Number System

Calculus Notation

Differentiation

Newton used a dot over the dependent variable to indicate a derivative, two dots for a second derivative, etc.

$$\dot{y} = \frac{dy}{dt}$$

Leibniz just used dx and dy to indicate infinitesimal increments in the independent and dependent variables.

$$\frac{d(f(x))}{dx} \text{ or } \frac{dy}{dx}$$

The use of the prime mark for derivatives dates from Joseph Louis Lagrange's work on differential calculus in the late 18th / early 19th Century.

$$f' \quad f''$$

Integration

Newton never used one consistent notation for integration, sometimes using a bar above a variable and sometimes putting the variable in a box.

$$\overline{x} \text{ or } \boxed{x}$$

We have come to use Leibniz's notation, which uses an extended 'S' to indicate the sum of infinitely many infinitesimal quantities $f(x)$ for each infinitesimal increment dx, between the two stated limits a and b.

$$\int_a^b f(x)\,dx$$

Leibniz's and Newton's notation for Calculus

https://www.storyofmathematics.com/17th_leibniz.html

萊布尼茲在棺材裡大笑勝出

The binary, or base 2, number system, expresses all numbers as a combination of the digits 0 and 1 (rather than the ten digits 0 - 9 used in the normal base 10 system).
It is a place value system, but rather than using units, tens, hundreds, thousands, etc (powers of 10), it uses powers of 2: 2, 4, 8, 16, 32, 64, etc.

Decimal	Binary
1	1
2	10
3	11
4	100
5	101
6	110
7	111
8	1000
9	1001
10	1010
...	

e.g. the binary number 110100101 is equivalent to:

$$
\begin{array}{rcr}
1 \times 256 & = & 256 \\
1 \times 128 & = & 128 \\
0 \times 64 & = & 0 \\
1 \times 32 & = & 32 \\
0 \times 16 & = & 0 \\
0 \times 8 & = & 0 \\
1 \times 4 & = & 4 \\
0 \times 2 & = & 0 \\
1 \times 1 & = & 1 \\
\hline
 & & 411
\end{array}
$$

Binary Number System

Calculus Notation

Differentiation

Newton used a dot over the dependent variable to indicate a derivative, two dots for a second derivative, etc.

$$\dot{y} = \frac{dy}{dt}$$

Leibniz just used dx and dy to indicate infinitesimal increments in the independent and dependent variables.

$$\frac{d(f(x))}{dx} \text{ or } \frac{dy}{dx}$$

The use of the prime mark for derivatives dates from Joseph Louis Lagrange's work on differential calculus in the late 18th / early 19th Century.

$$f' \quad f''$$

Integration

Newton never used one consistent notation for integration, sometimes using a bar above a variable and sometimes putting the variable in a box.

$$\overline{x} \text{ or } \boxed{x}$$

We have come to use Leibniz's notation, which uses an extended 'S' to indicate the sum of infinitely many infinitesimal quantities $f(x)$ for each infinitesimal increment dx, between the two stated limits a and b.

$$\int_a^b f(x)\,dx$$

Leibniz's and Newton's notation for Calculus

https://www.storyofmathematics.com/17th_leibniz.html

瑜亮情結: SOI vs Bulk FinFET

- SOI 晶圓天生比較貴: (Δ = ~$300/wafer)
  - adding ~10% raw wafer cost of a 28nm node (~$3k/wafer), but advocates claimed **die cost is cheaper**
  - adding ~2% of a 5nm node (~$16k/wafer)
- SOI 制程步驟卻可較少(所以較省錢):
  - GF claimed 22nm planar FD-SOI is about 40% less masks than 14nm/16nm FinFETs
    - FD-SOI ~ bulk Si @Yielded wafer cost (the figure on the right)
  - 12nm FD-SOI (planar) is 40% less masks vs 10nm bulk FinFETs (but no products even at Q1'22)
- 有些像白金與黃金價格之爭

https://semiengineering.com/inside-fd-soi-scaling/

22nm planar FD-SOI

Table 1. Process complexity comparison.

Process factor	Bulk	FDSOI - implant	FDSOI - in-situ
Photo masks	47	34	32
Implants	63	17	15
Steps	328	250	241

Table 2. Fabricated wafer cost

Cost factor	Bulk	FDSOI - implant	FDSOI - in-situ
Depreciation	$1,857.71	$1,666.09	$1,623.03
Equipment maintenance	$443.12	$395.10	$384.48
Direct labor	$34.79	$25.17	$23.69
Indirect labor	$67.91	$49.13	$46.33
Facilities	$199.32	$163.97	$157.90
Material	$130.00	$500.00	$500.00
Consumables	$227.58	$213.39	$209.81
Monitor wafers	$17.83	$20.79	$20.48
Total unyielded wafer cost	$2,978.3	$3,033.60	$2,965.70
Wafer yield	97.70%	98.30%	98.40%
Yielded wafer cost	$3,049.10	$3,085.70	$3,013.60

https://www.icknowledge.com/news/SoitecReport20110709.pdf

https://www.globalfoundries.com/sites/default/files/product-briefs/pb-12lp-11-web.pdf

瑜亮情結: SOI vs Bulk Si FinFET

- SOI 晶圓天生比較貴: (Δ = ~$300/wafer)
  - adding ~10% raw wafer cost of a 28nm node (~$3k/wafer), but advocates claimed **die cost is cheaper**
  - adding ~2% of a 5nm node (~$16k/wafer)
- SOI 制程步驟卻可較少(所以較省錢):
  - GF claimed 22nm planar FD-SOI is about 40% less masks than 14nm/16nm FinFETs
    - FD-SOI ~ bulk Si @Yielded wafer cost (the figure on the right)
  - 12nm FD-SOI (planar) is 40% less masks vs 10nm bulk FinFETs (but no products even at Q1'22)
- 有些像白金與黃金價格之爭

https://semiengineering.com/inside-fd-soi-scaling/

22nm planar FD-SOI

Table 1. Process complexity comparison.

Process factor	Bulk	FDSOI - implant	FDSOI - in-situ
Photo masks	47	34	32
Implants	63	17	15
Steps	328	250	241

Table 2. Fabricated wafer cost

Cost factor	Bulk	FDSOI - implant	FDSOI - in-situ
Depreciation	$1,857.71	$1,666.09	$1,623.03
Equipment maintenance	$443.12	$395.10	$384.48
Direct labor	$34.79	$25.17	$23.69
Indirect labor	$67.91	$49.13	$46.33
Facilities	$199.32	$163.97	$157.90
Material	$130.00	$500.00	$500.00
Consumables	$227.58	$213.39	$209.81
Monitor wafers	$17.83	$20.79	$20.48
Total unyielded wafer cost	$2,978.3	$3,033.60	$2,965.70
Wafer yield	97.70%	98.30%	98.40%
Yielded wafer cost	$3,049.10	$3,085.70	$3,013.60

https://www.icknowledge.com/news/SoitecReport20110709.pdf

https://www.globalfoundries.com/sites/default/files/product-briefs/pb-12lp-11-web.pdf

瑜亮情結: SOI vs Bulk Si FinFET

- SOI 晶圓天生比較貴: (Δ = ~$300/wafer)
  - adding ~10% raw wafer cost of a 28nm node (~$3k/wafer), but advocates claimed **die cost is cheaper**
  - adding ~2% of a 5nm node (~$16k/wafer)
- SOI 制程步驟卻可較少(所以較省錢):
  - GF claimed 22nm planar FD-SOI is about 40% less masks than 14nm/16nm FinFETs
    - FD-SOI ~ bulk Si @Yielded wafer cost (the figure on the right)
  - 12nm FD-SOI (planar) is 40% less masks vs 10nm bulk FinFETs (but no products even at Q1'22)
- 有些像白金與黃金價格之爭

22nm planar FD-SOI

Table 1. Process complexity comparison.

Process factor	Bulk	FDSOI - implant	FDSOI - in-situ
Photo masks	47	34	32
Implants	63	17	15
Steps	328	250	241

Table 2. Fabricated wafer cost

Cost factor	Bulk	FDSOI - implant	FDSOI - in-situ
Depreciation	$1,857.71	$1,666.09	$1,623.03
Equipment maintenance	$443.12	$395.10	$384.48
Direct labor	$34.79	$25.17	$23.69
Indirect labor	$67.91	$49.13	$46.33
Facilities	$199.32	$163.97	$157.90
Material	$130.00	$500.00	$500.00
Consumables	$227.58	$213.39	$209.81
Monitor wafers	$17.83	$20.79	$20.48
Total unyielded wafer cost	$2,978.3	$3,033.60	$2,965.70
Wafer yield	97.70%	98.30%	98.40%
Yielded wafer cost	$3,049.10	$3,085.70	$3,013.60

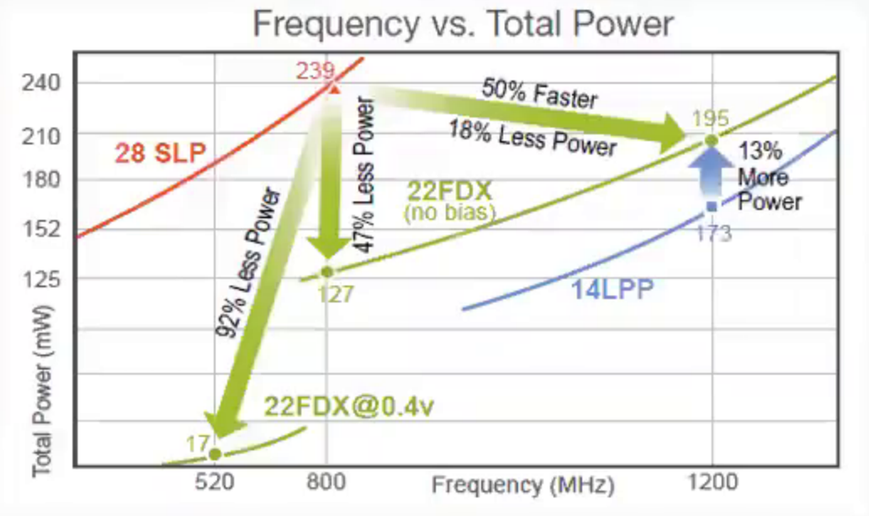
https://www.icknowledge.com/news/SoitecReport20110709.pdf

https://www.globalfoundries.com/sites/default/files/product-briefs/pb-12lp-11-web.pdf

https://semiengineering.com/inside-fd-soi-scaling/

SOI 發展歷史一覽

- IBM 是开发 SOI 流程技术的先驱
  - 45nm SOI available through MOSIS
- NXP/Samsung have SOI for 28nm node
- AMD were designed on SOI, but moved to TSMC bulk Si FinFETs to beat Intel
- GF has been developing FDSOI since 2012
  - Providing 22nm planar FDSOI (22FDX)
  - But failed in multiple fronts (20/14/7nm) before focusing on specialized processes (Samsung supported GF@14nm)
- Intel and TSMC use bulk Si-FETs only

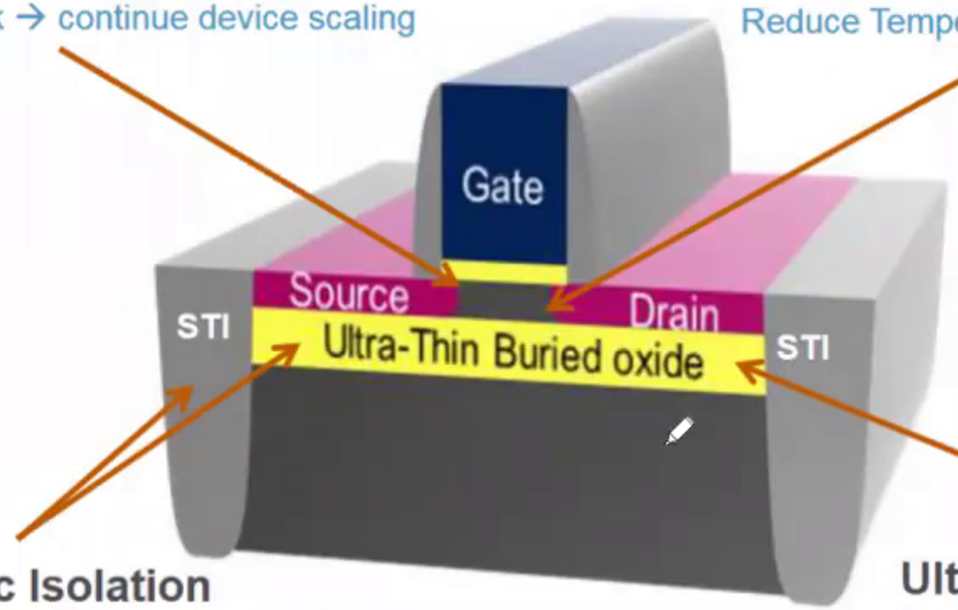


https://gf.com/sites/default/files/fd-soi-offers-alternative-to-finfet.pdf

SOI 對付 Bulk Si Planar-FETs 優勢很夠

Ultra-Thin BODY
Excellent Electrostatic Control of the channel
Low SCE, DIBL → Low V_t @ High V_D
Gate length shrink → continue device scaling

Undoped Channel & no Pocket
Less V_t variability & SRAM V_{min} improved
Lower Power Consumption
Reduce Temperature dependency & no RDF



Total Dielectric Isolation
Lower SD capacitances & Lower SD Leakage
Less Sensitive to Temperature
Higher power efficiency

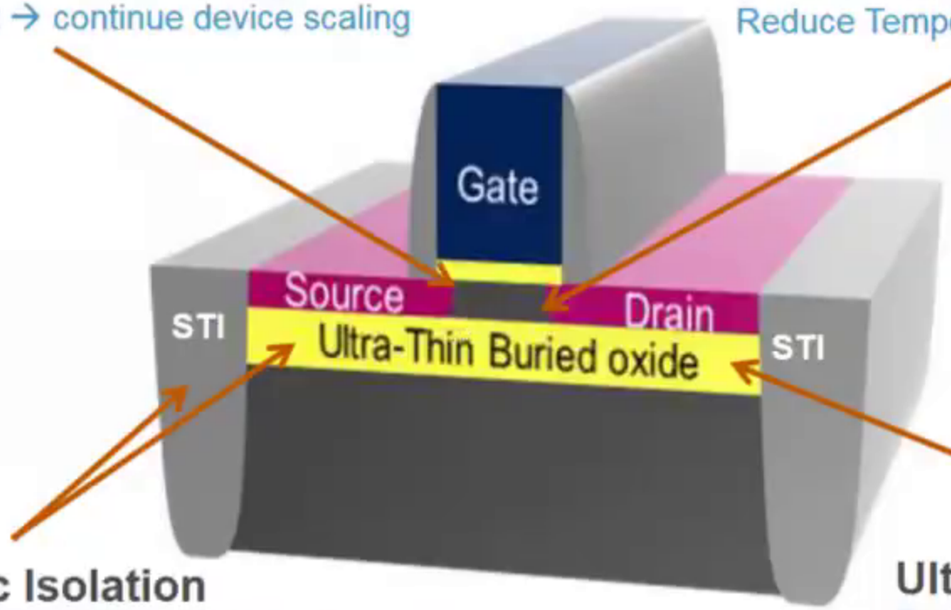
Ultra Thin BOX
Body Biasing (BB) → FBB & RBB
Speed boost due to BB
GP Implantation → V_t adjustment

https://www.coventor.com/blog/everything-you-need-to-know-about-fdsoi-technology-advantages-disadvantages-and-applications-of-fdsoi/

SOI 對付 Bulk Si Planar-FETs 優勢很夠

Ultra-Thin BODY
Excellent Electrostatic Control of the channel
Low SCE, DIBL → Low V_t @ High V_D
Gate length shrink → continue device scaling

Undoped Channel & no Pocket
Less V_t variability & SRAM V_{min} improved
Lower Power Consumption
Reduce Temperature dependency & no RDF



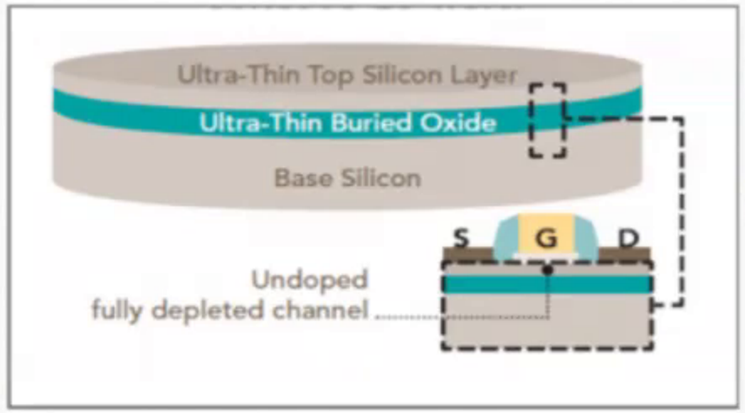
Total Dielectric Isolation
Lower SD capacitances & Lower SD Leakage
Less Sensitive to Temperature
Higher power efficiency

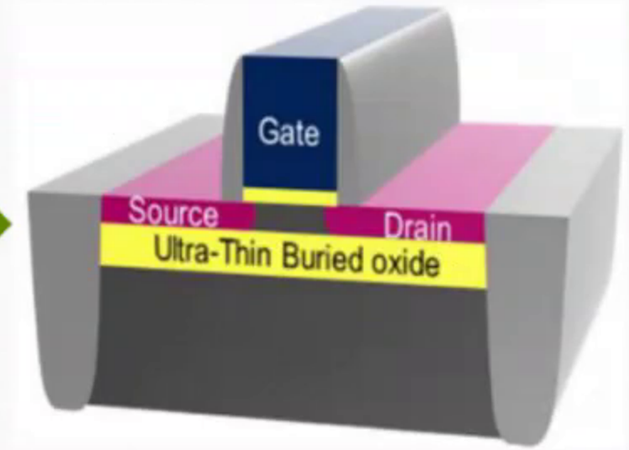
Ultra Thin BOX
Body Biasing (BB) → FBB & RBB
Speed boost due to BB
GP Implantation → V_t adjustment

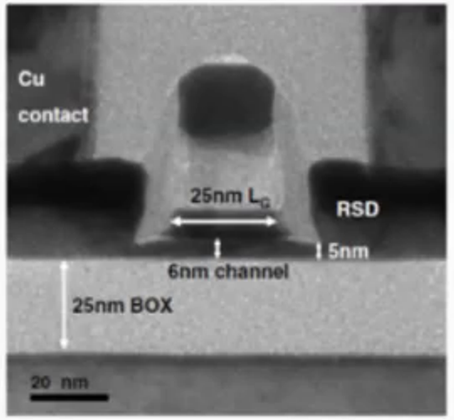
https://www.coventor.com/blog/everything-you-need-to-know-about-fdsoi-technology-advantages-disadvantages-and-applications-of-fdsoi/

Fully Depleted Silicon on Insulator (FDSOI)

- FDSOI advantages over planar-FETs
  - GF provides FD-SOI CMOS (22FDX)
  - Samsung provides eMRAM on FD-SOI (28FDS)







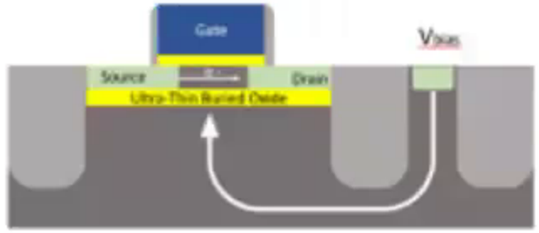
*28nm FDSOI Transistor**

https://www.coventor.com/blog/everything-you-need-to-know-about-fdsoi-technology-advantages-disadvantages-and-applications-of-fdsoi/
https://news.samsung.com/global/samsung-electronics-starts-commercial-shipment-of-emram-product-based-on-28nm-fd-soi-process

Fully Depleted Silicon on Insulator (FDSOI)

28nm FD SOI

- **Power – Performance Benefits**
  - Improved electrostatics enables **shorter gate lengths**
  - Reduced device parasitics
  - Device back bias allows for **lower Vdd** while maintaining performance
  - **Device tuning** with back biasing to compensate process variation
- **Analog Integration and Performance Benefits**
  - Higher gain, better matching and lower 1/f noise
  - Gate first integration removes density rules for precision analog
- **Better SER and Latchup Immunity**
  - **10-100x better** SER performance versus 28nm bulk alternatives
  - Thin buried oxide layer makes device immune to latchup



But back biasing consumes area

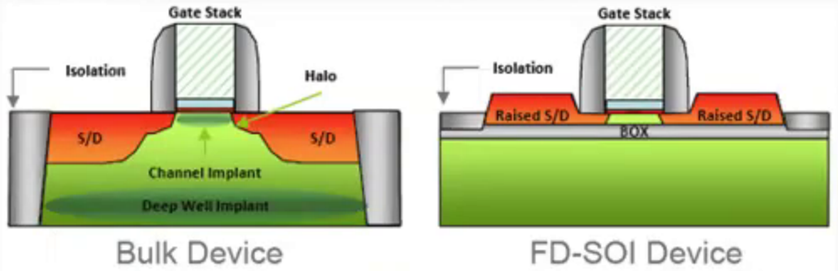
Body Biasing: Faster when required and more energy efficient when performance isn't as critical

14 CONFIDENTIAL AND PROPRIETARY

SOI Advantages and Disadvantages

Advantages

- Diffusion capacitance reduction (since bottom touches insulator)
  - Lower power (smaller diffusion capacitances)
- Reduced short channel effect
- Lower device threshold voltages
- Latch-up elimination (since no lateral PNP device possible)
- Reduced body effect/source follower action (smaller)
- Reduced soft error rate (SER): absence of well/substrate as in bulk)



The fully depleted SOI transistor at 20 nm is significantly simpler than even a simplified version of the bulk CMOS transistor.

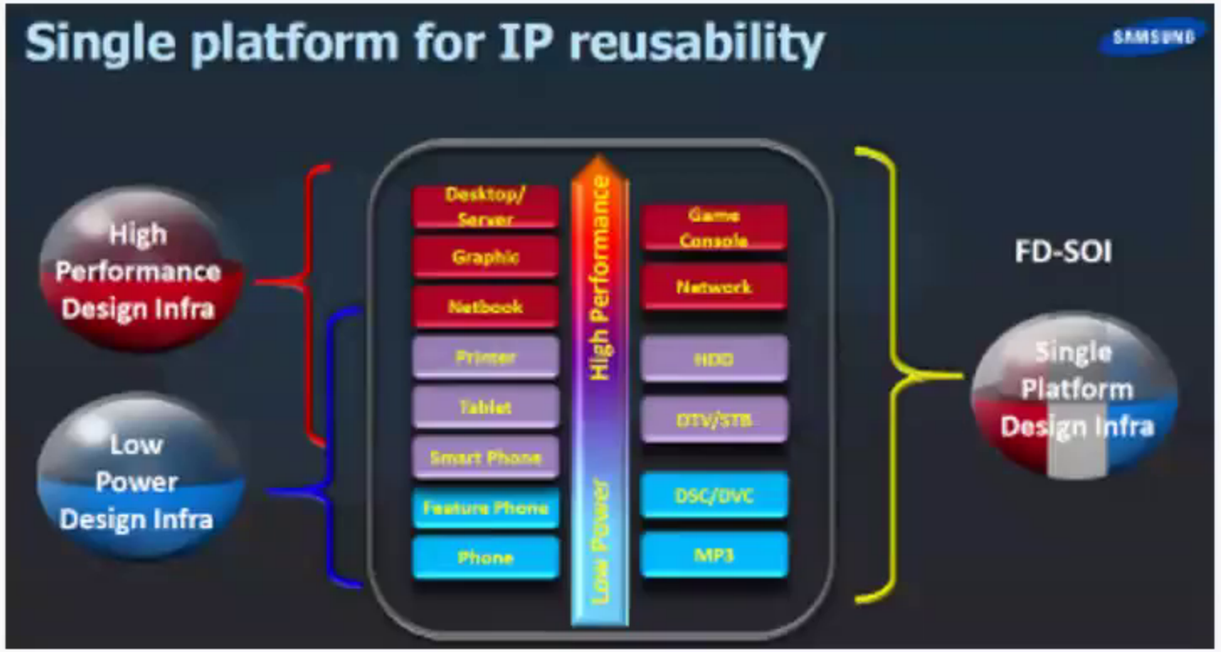
Disadvantages

- History Effect
- Higher Drain Induced Barrier Lowering
- Self Heating

https://www.eetimes.com/its-time-to-look-at-fd-soi-again/

SOI other Significant Advantages

- 理論上，FD-SOI从高性能到低功耗设备，只需开发一次IP。FD-SOI为IP可重用性提供了一个单一平台，節省大量工程资源(1X cost而已)
- 但使用bulk- Si芯片的公司卻往往需要維持两个(低性能與高性能)独立的工程设计资源团队，因为伺务器和电话开发的IP是分開的(2X cost)

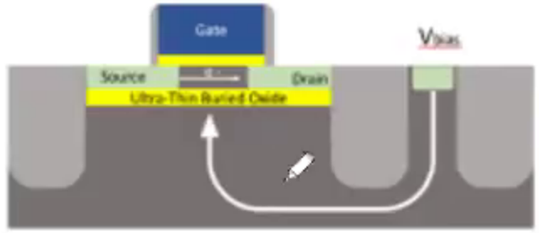


https://www.eetimes.com/8-fd-soi-questions-youre-afraid-to-ask/

Fully Depleted Silicon on Insulator (FDSOI)

28nm FD SOI

- **Power – Performance Benefits**
  - Improved electrostatics enables **shorter gate lengths**
  - Reduced device parasitics
  - Device back bias allows for **lower Vdd** while maintaining performance
  - **Device tuning** with back biasing to compensate process variation
- **Analog Integration and Performance Benefits**
  - Higher gain, better matching and lower 1/f noise
  - Gate first integration removes density rules for precision analog
- **Better SER and Latchup Immunity**
  - **10-100x better** SER performance versus 28nm bulk alternatives
  - Thin buried oxide layer makes device immune to latchup



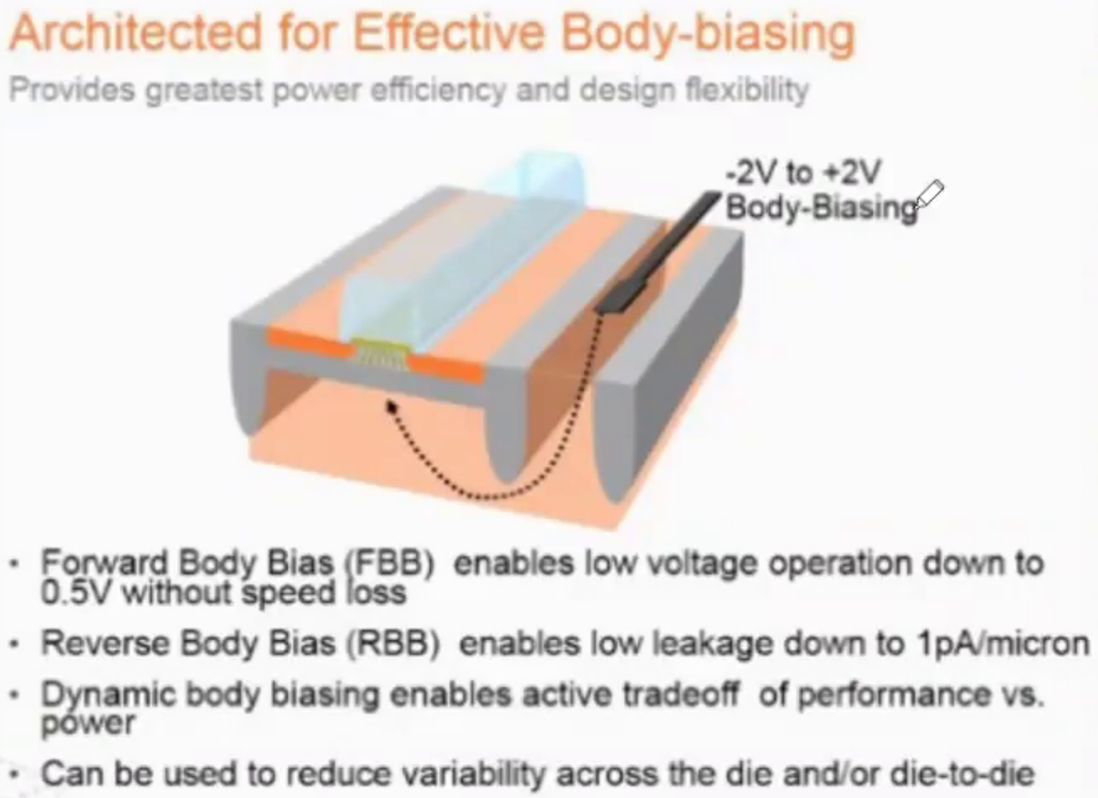
But back biasing consumes area

Body Biasing: Faster when required and more energy efficient when performance isn't as critical

14 CONFIDENTIAL AND PROPRIETARY

SOI other Significant Advantages

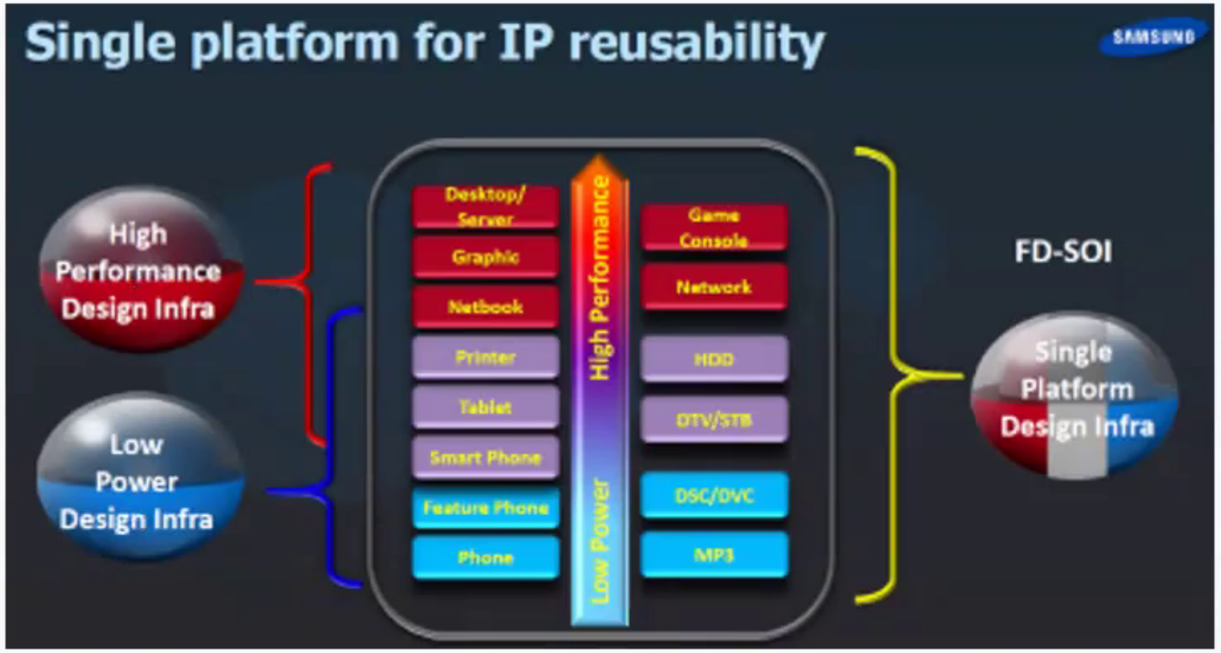
- FD-SOI的(body-biasing)阀体偏置，提供了靈活的IC設計空間，可实现更高的功率效率和设计灵活性
- IC设计人员需要使用多種CPU來构建设计高性能芯片，但他们可以用FD-SOI的 body-biasing來減少所需CPU種類，大幅降低设计與制造成本
- 但是TSMC/Intel 卻仍不理不採(三星/GF卻大推)



https://www.eetimes.com/8-fd-soi-questions-youre-afraid-to-ask/

SOI other Significant Advantages

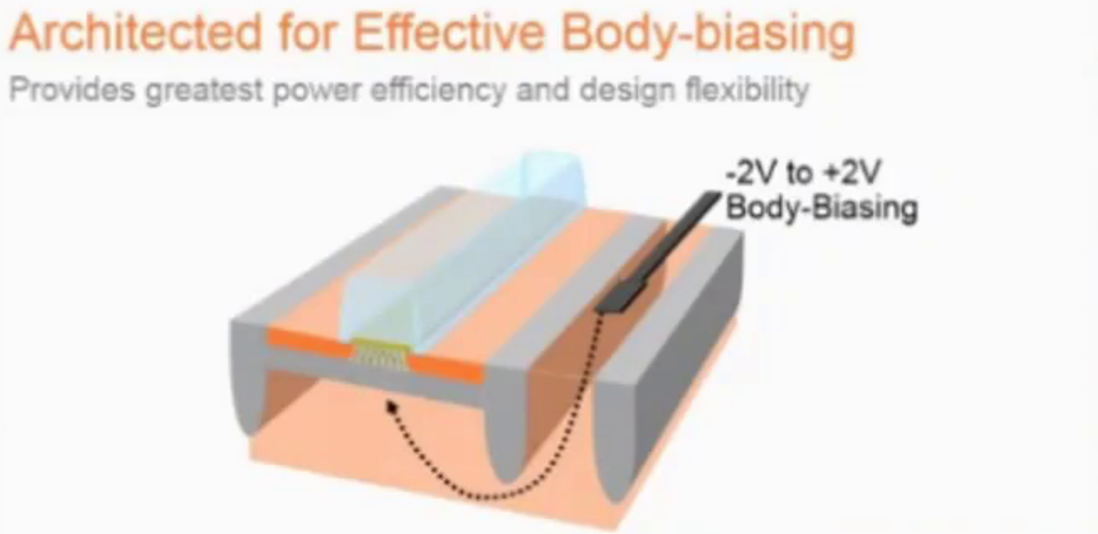
- 理論上，FD-SOI从高性能到低功耗设备，只需开发一次IP。FD-SOI为IP可重用性提供了一个单一平台，節省大量工程资源(1X cost而已)
- 但使用bulk- Si芯片的公司卻往往需要維持两个(低性能與高性能)独立的工程设计资源团队，因为伺务器和电话开发的IP是分開的(2X cost)



https://www.eetimes.com/8-fd-soi-questions-youre-afraid-to-ask/

SOI other Significant Advantages

- FD-SOI的(body-biasing)阀体偏置，提供了靈活的IC設計空間，可实现更高的功率效率和设计灵活性
- IC设计人员需要使用多種CPU來构建设计高性能芯片，但他们可以用FD-SOI的 body-biasing來減少所需CPU種類，大幅降低设计與制造成本
- 但是TSMC/Intel 卻仍不理不採(三星/GF卻大推)



- Forward Body Bias (FBB) enables low voltage operation down to 0.5V without speed loss
- Reverse Body Bias (RBB) enables low leakage down to 1pA/micron
- Dynamic body biasing enables active tradeoff of performance vs. power
- Can be used to reduce variability across the die and/or die-to-die

https://www.eetimes.com/8-fd-soi-questions-youre-afraid-to-ask/

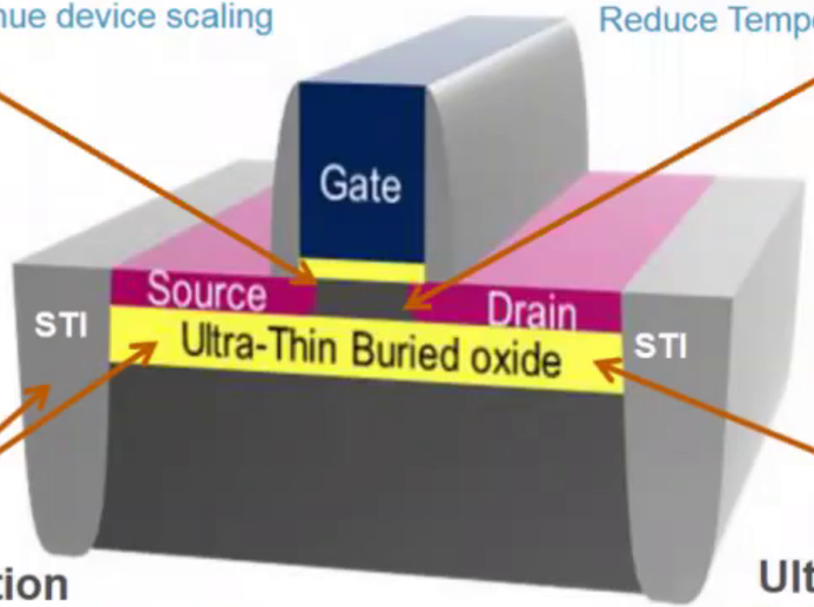
SOI 對付 Bulk Si FinFETs 優勢不夠

Ultra-Thin BODY
Excellent Electrostatic Control of the channel
Low SCE, DIBL → Low V_t @ High V_D
Gate length shrink → continue device scaling

Undoped Channel & no Pocket
Less V_t variability & SRAM V_{min} improved
Lower Power Consumption
Reduce Temperature dependency & no RDF

Si FFT也有 ultra-thin body

Si FFTchannel也是undoped



Si FFT只有屁股漏電，而且屁股越來越小

Si FFT用HKMG也可調Vt

Total Dielectric Isolation
Lower SD capacitances & Lower SD Leakage
Less Sensitive to Temperature
Higher power efficiency

Ultra Thin BOX
Body Biasing (BB) → FBB & RBB
Speed boost due to BB
GP Implantation → V_t adjustment

https://www.coventor.com/blog/everything-you-need-to-know-about-fdsoi-technology-advantages-disadvantages-and-applications-of-fdsoi/

SOI 對付 Bulk Si FinFETs 優勢不夠

- **Bulk FFT 只有屁股漏電，而且屁股越來越小**
- **SOI reduces leakages by design (due to Box), bulk FinFETs also reduces junction leakage 100x due to the nature of FinFETs, i.e., taller and narrower fin for scaled nodes (hence smaller bottom fin area)**

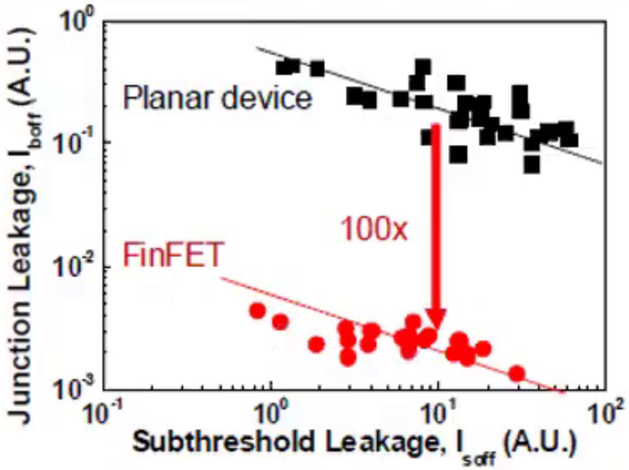


Figure 15. N-FinFETs junction leakage decreases by 100 times at the same I_{soff} leakage compared to the planar NFETs using similar process conditions.

High Performance 22/20nm FinFET CMOS Devices with Advanced High-K/Metal Gate Scheme C.C. Wu et al, IEDM'10, 27.1

SOI 對付 Bulk Si FinFETs 優勢不夠

還有很多其他說不清楚的問題

- 有人就是信不過完全由法國人掌握的科技 (Grenoble是否太美了?)
  - CEA-Leti (屬是法国原子能委员会，CEA)，开发了"Smart-Cut"技术
  - Soitec完善了超薄FD-SOI晶圆
  - STM推出了基于FD-SOI的SoC
- Lack of a clear up-front IP strategy on FD-SOI (some owned by ST, others owned by Leti and Soitec) was problematic

https://www.planetware.com/tourist-attractions-/grenoble-f-rh-gren.htm

https://www.eetimes.com/8-fd-soi-questions-youre-afraid-to-ask/

SOI 對付 Bulk Si FinFETs 優勢不夠

還有很多其他說不清楚的問題

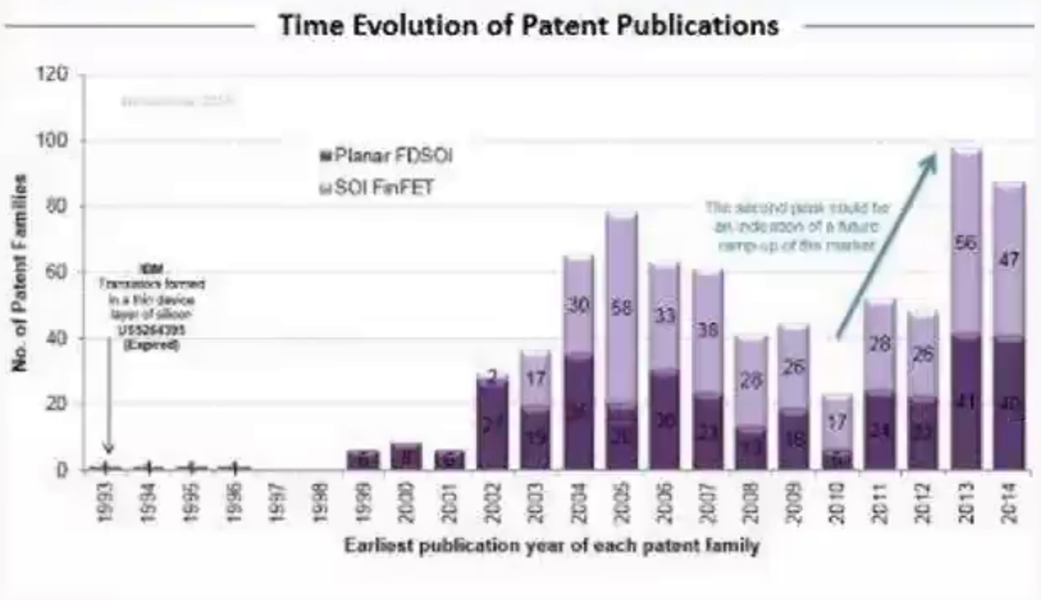
- 有人就是信不過完全由法國人掌握的科技 (Grenoble是否太美了?)
  - CEA-Leti (屬是法国原子能委员会，CEA)，开发了"Smart-Cut"技术
  - Soitec完善了超薄FD-SOI晶圆
  - STM推出了基于FD-SOI的SoC
- Lack of a clear up-front IP strategy on FD-SOI (some owned by ST, others owned by Leti and Soitec) was problematic

https://www.planetware.com/tourist-attractions-/grenoble-f-rh-gren.htm

https://www.eetimes.com/8-fd-soi-questions-youre-afraid-to-ask/

为何英特尔/台积电堅持bulk Si FinFET?

1. TSMC/Intel 本身專利不足，根本不想這條路，以免被卡脖子
2. SOI 的製程甚至成本优势，仍不足以逼二者替换bulk-Si FinFETs (離婚再娶成本太高)
3. 高良率bulk-Si FETs的基线(baseline)已經形成，實在沒力氣再搞一個SOI (此再娶也可能不見得比元配好)
   - 例如台积电(和英特尔)即使在3NM也没有转向NS-FET，因为新的架构影响了基线(baseline)
   - 三星在5/4/3NM节点賭上NS-FET，但良率問題不小

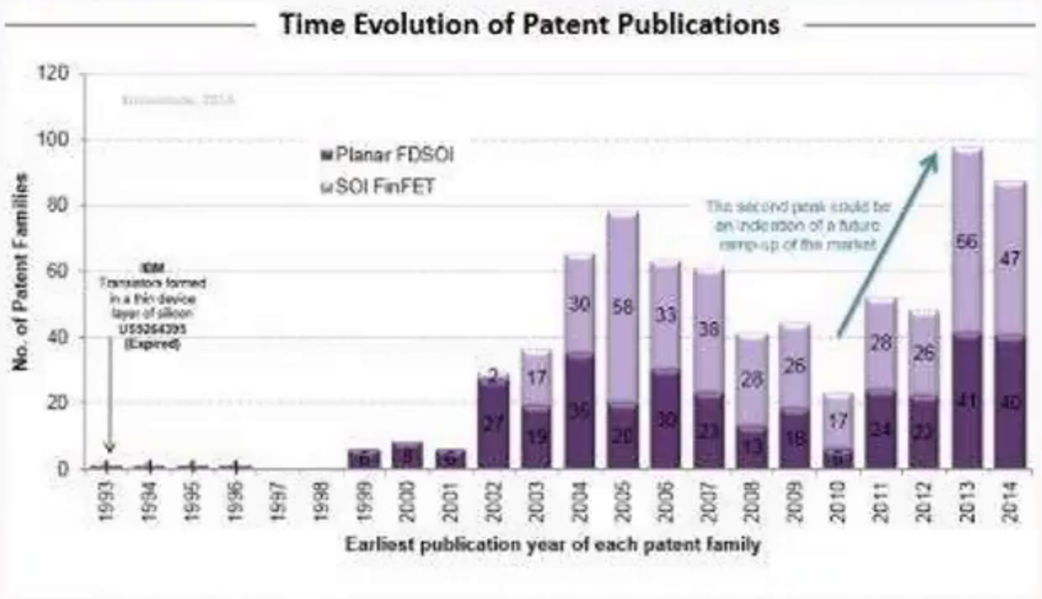


SOI專利大都屬於IBM/ GF/ AMD/Leti/ SOITEC/STM等，TSMC/Intel 只有小貓兩三隻

https://www.eetimes.com/8-fd-soi-questions-youre-afraid-to-ask/

为何英特尔/台积电堅持bulk Si FinFET?

1. TSMC/Intel 本身專利不足，根本不想這條路，以免被卡脖子
2. SOI 的製程甚至成本优势，仍不足以逼二者替换bulk-Si FinFETs (離婚再娶成本太高)
3. 高良率bulk-Si FETs的基线(baseline)已經形成，實在沒力氣再搞一個SOI (此再娶也可能不見得比元配好)
   - 例如台积电(和英特尔)即使在3NM也没有转向NS-FET，因为新的架构影响了基线(baseline)
   - 三星在5/4/3NM节点賭上NS-FET，但良率問題不小



SOI專利大都屬於IBM/ GF/ AMD/Leti/ SOITEC/STM等，TSMC/Intel 只有小貓兩三隻

https://www.eetimes.com/8-fd-soi-questions-youre-afraid-to-ask/

附錄:A parasitic PNPN Latch-up in CMOS

- The N-well is the base for either vertical PNP and the collector for either lateral NPN
- The P-type substrate (P^-) serves as the base for either lateral NPN and the collector for either vertical PNP

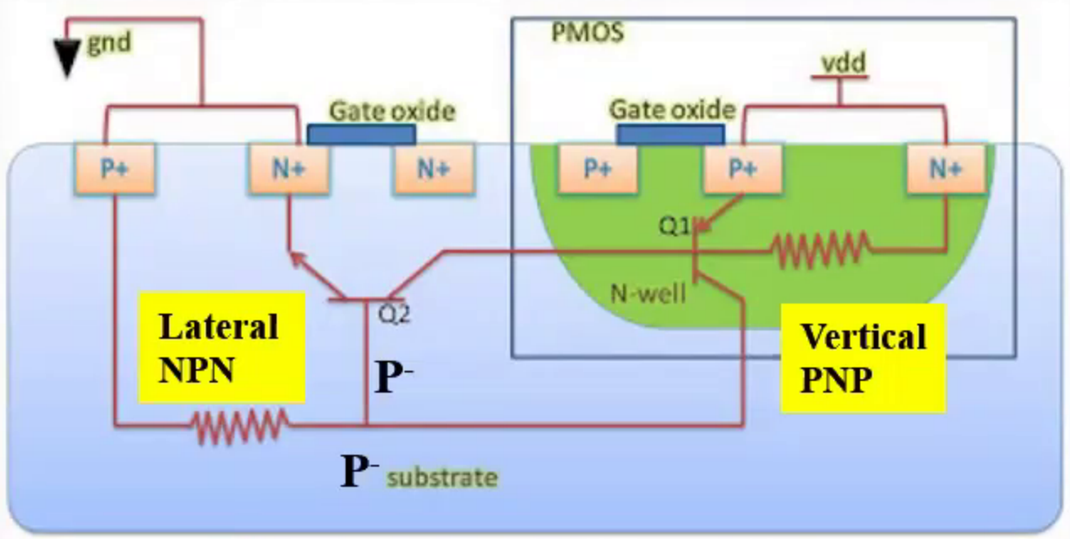
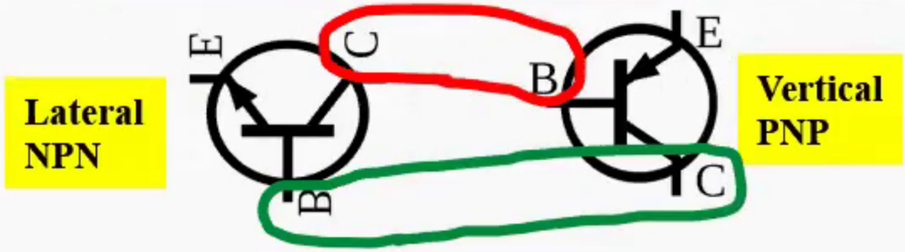


Figure 1 : Latchup formation in a CMOS device



https://vlsiuniverse.blogspot.com/2013/03/latchup-condition-in-cmos-devices.html

By Zedh - Own work, CC BY-SA 4.0, https://commons.wikimedia.org/w/index.php?curid=307326516

附錄:A parasitic PNPN Latch-up in CMOS

- The N-well is the base for either vertical PNP and the collector for either lateral NPN
- The P-type substrate (P^-) serves as the base for either lateral NPN and the collector for either vertical PNP

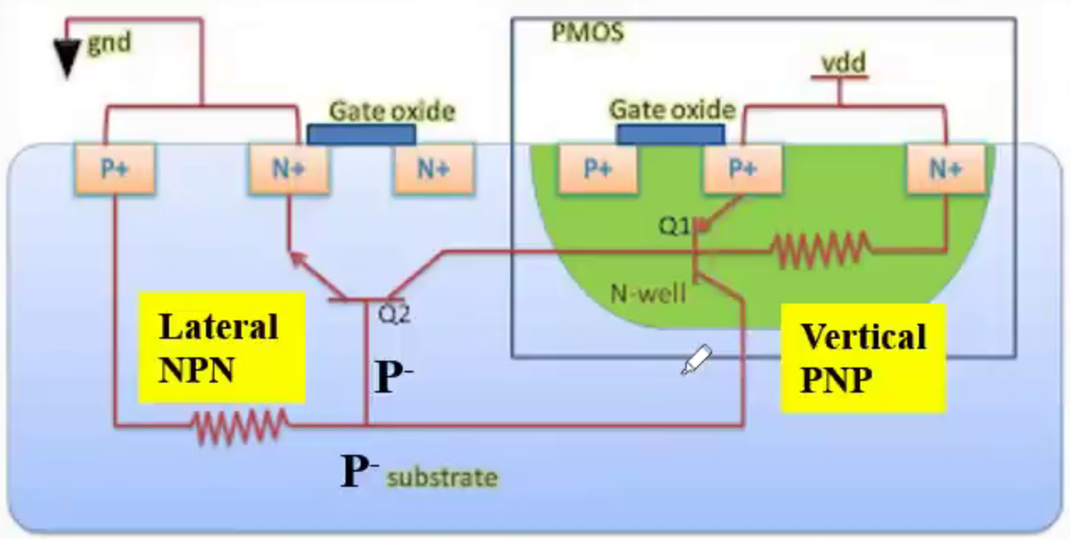
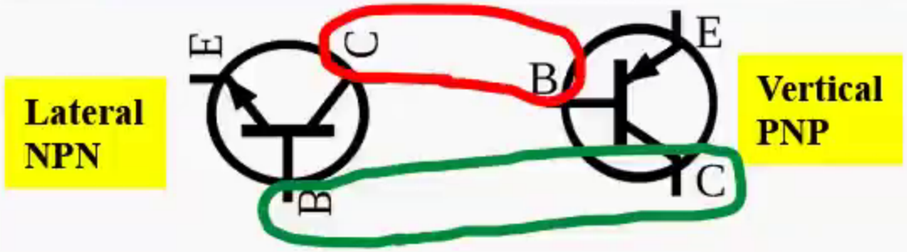


Figure 1 : Latchup formation in a CMOS device

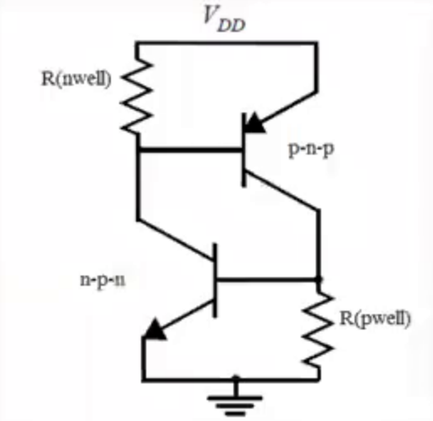


https://vlsiuniverse.blogspot.com/2013/03/latchup-condition-in-cmos-devices.html

By Zedh - Own work, CC BY-SA 4.0, https://commons.wikimedia.org/w/index.php?curid=307326516

附錄: More about PNPN Latch-up Loop

- The proportion of carriers able to cross the base and reach the collector is a measure of the BJT efficiency (α and β), the common emitter gain is β_F, $\beta_F = \frac{I_C}{I_B}$
- For latch-up to occur the current gain of the loop formed by the two bipolar transistors be larger than unity ($\beta_F > 1$)



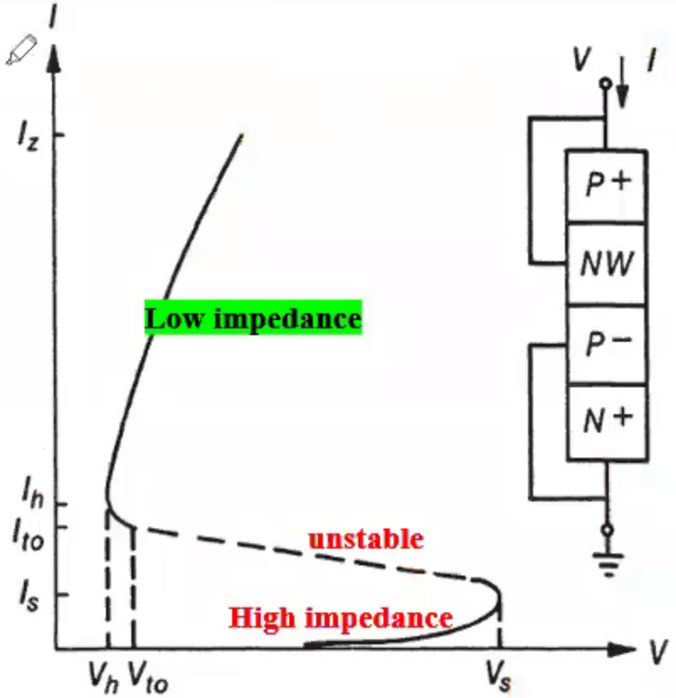


Figure 2-4. Illustrative PNPN current/voltage characteristics. A stable high impedance state is defined by $I < I_s$, and a low impedance state by $I_h < I < I_z$. At the turn-off point reverse bias on the center junction is zero.

Latchup in CMOS Technology, *Ronald R. Troutman*

https://en.wikipedia.org/wiki/Latch-up#/media/File:Latchup_ckt.png

附錄: SOI is naturally latch-up free

- SOI = silicon on insulator
  - Parasitic PNPN paths is blocked by the Box (of SOI)
  - Box reduces soft errors significantly
- A Few Notes:
  - SOI still needs STI (and can be shallower), but not DTI
  - Floating body effect in PD-SOI avoided by using FD-SOI
  - Bulk Si leakage to substrate is less in FinFETs than in Planar FETs since fins are tall and thin
  - SOI key gate level capacitance advantage does not alleviate BEOL loaded FinFETs (airgap, if materialized, helps more in capacitance reduction than SOI)

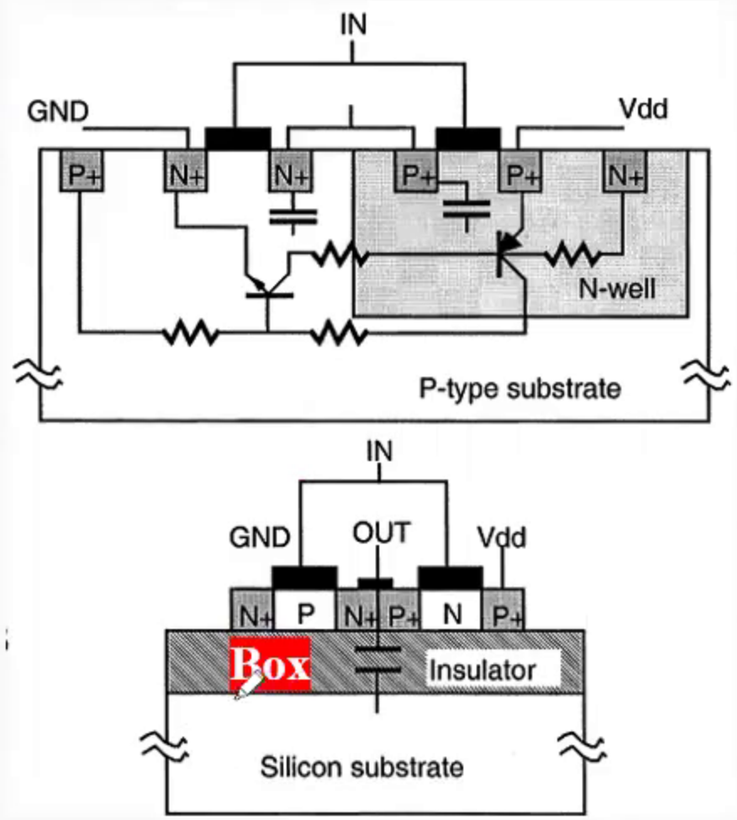


Figure 1-1. A: Cross section showing the latch-up path in a bulk CMOS inverter. B: Cross section of an SOI CMOS inverter.