

芯片制程統計基礎篇

_台积5纳米超变态良率

Chip Yield Model Development

Extending to TSMC 5nm yield

王不老說半导

誰是限制良率的罪魁禍首?

限制良率的罪魁禍首:

- Process-limited yield
 - Contaminants (以前很糟(見右下圖), 但現已緩解)
 - Inadequate process margin (誰解決誰贏)
 - Cobalt (英特爾的軟肋之一)
 - Multi-patterning (三星/英特爾的軟肋之二)
 - Poor mask/PDK design (see below)
- Design-limited yield
 - 顧客與代工工廠共同合作設計產生的PDK/Mask design 出了問題(三星的軟肋之一)

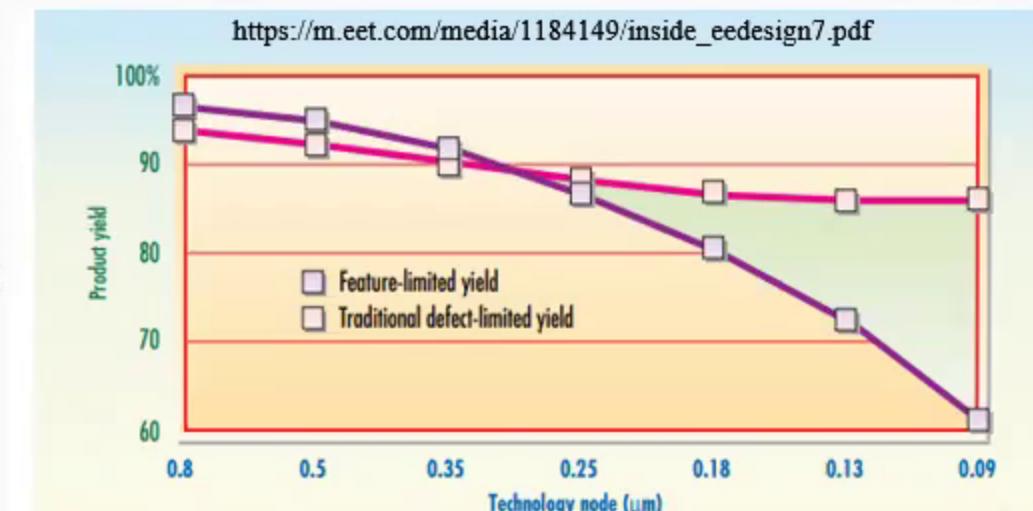
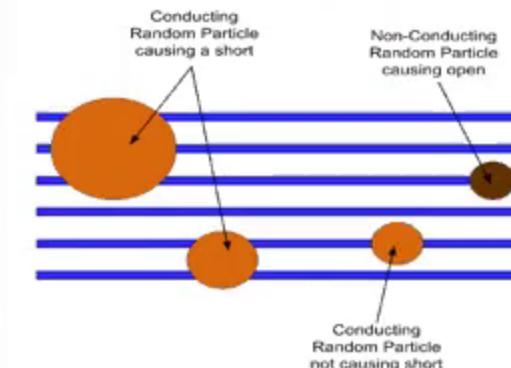


Fig. 1

The modeled trends with defect-limited versus feature-limited yield with successive IC technology nodes. The defect-limited yield trend assumes constant failure rates for each successive technology node. The feature limited yield trend assumes a 50% improvement for each successive technology node, while the number of features grows >50% per node.



<https://scholarworks.umass.edu/cgi/viewcontent.cgi?referer=https://www.google.com/&httpsredir=1&article=1863&context=theses>

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限制良率的罪魁禍首：

- Contaminants (右圖們，以前很糟，但現已解決)
 - 目前教課書上所有的良率公式，皆不適用了（見下圖，台積良率竟在理論估計值之上）

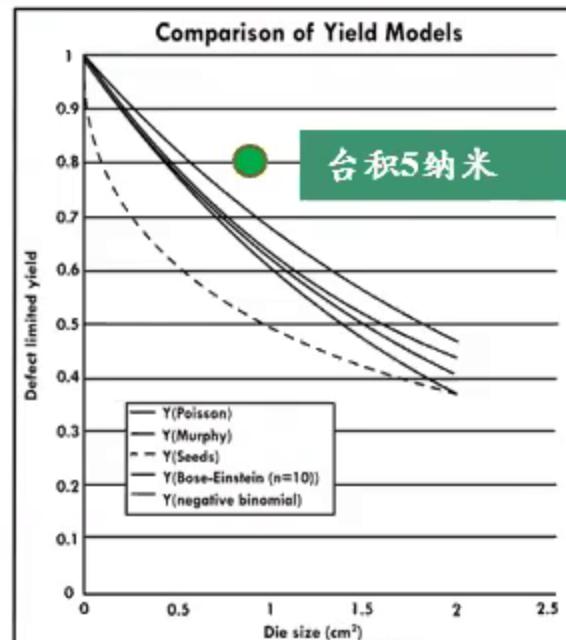
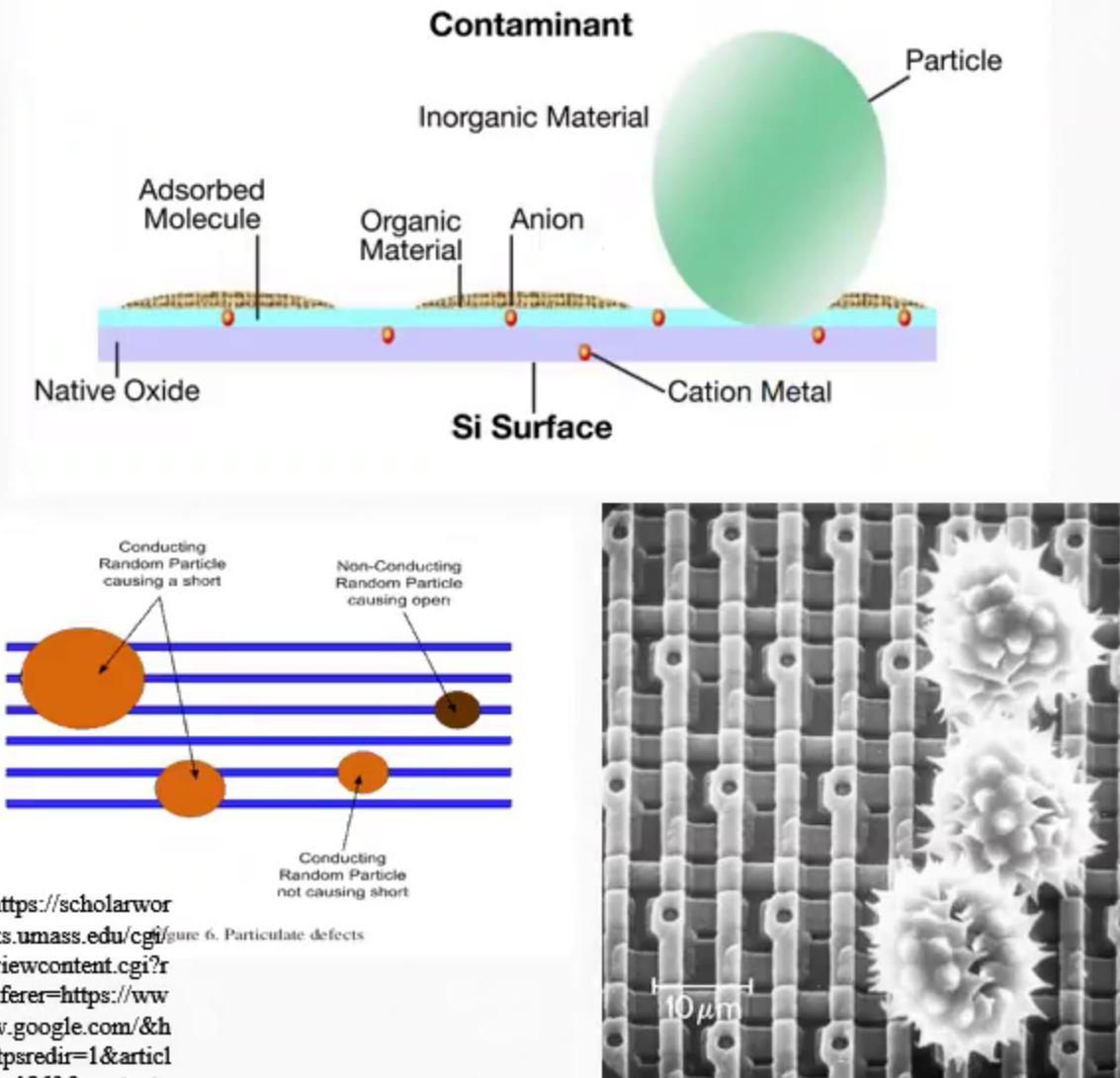


Figure 7: Defect yield density as a function of die size for different models. In all of these the yield reduces with die size. The steepest drop is for the Seeds model, which assumes an exponential dependence for the defect density distribution. Adapted from *Microchip fabrication - Peter van Zant*.

<https://www.mksinst.com/n/wafer-surface-cleaning>



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- Cobalt (英特爾的軟肋之一)
 - Cobalt fill in high aspect ratio **difficult**
 - **Void formation can be a big issue**
 - Intel invented this process but failed to deliver yield performance
 - **Intel lost 10NM markets (CEO was kicked out)**
 - TSMC, as the copycat, did a better job
 - **No issues, TSMC became world No.1**

Cobalt fill/reflow

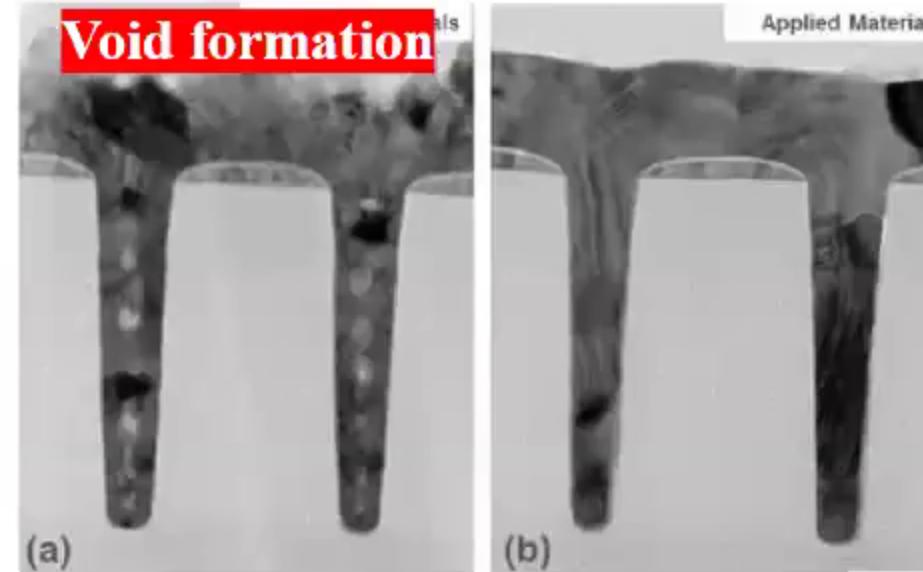


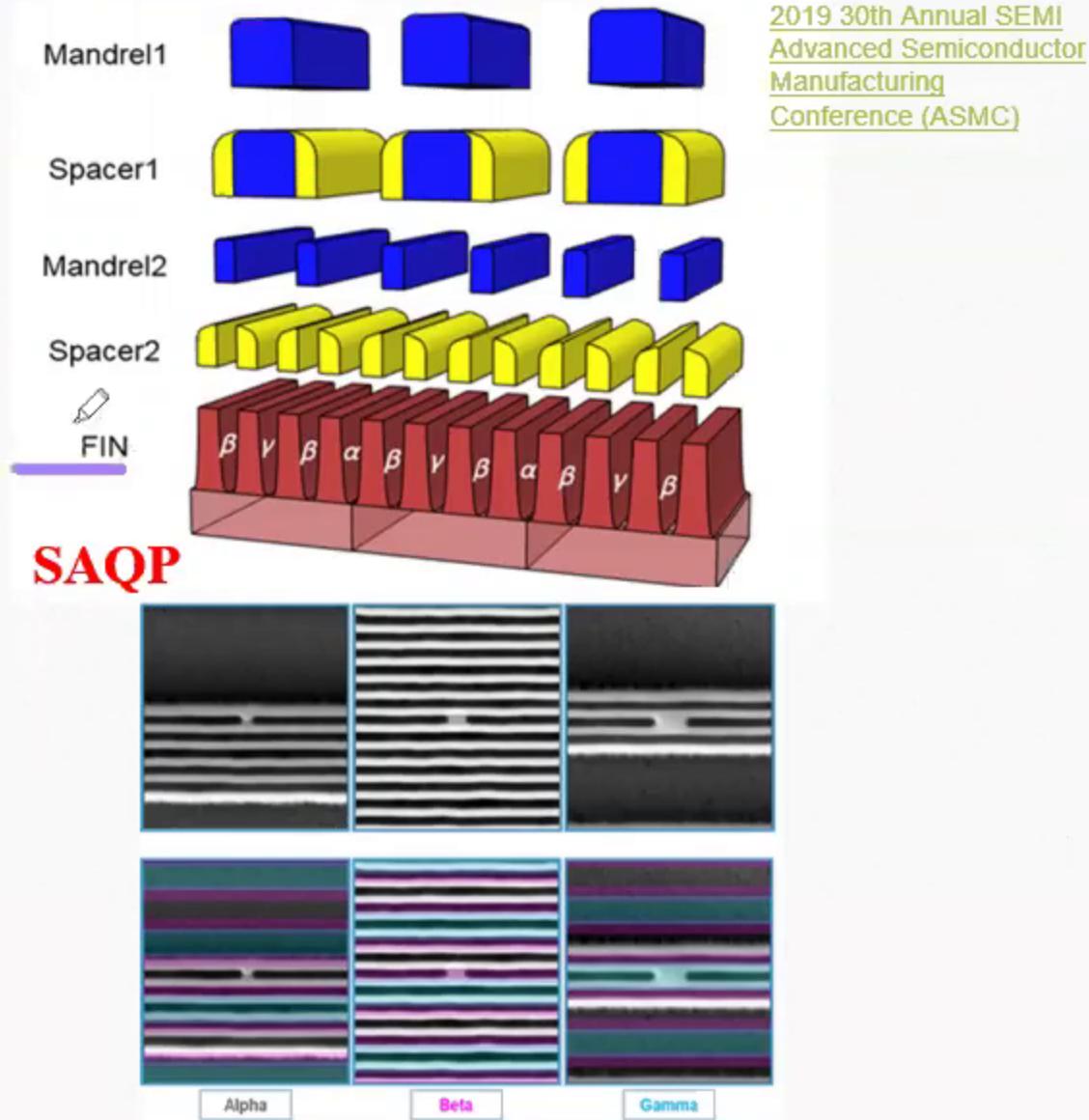
Fig. 1: Cross-section TEM images of trench structures filled with (a) as deposited CVD Co film and (b) annealed Co film.

Electron beam detection of cobalt trench embedded voids enabling improved process control for Middle-Of-Line at the 7nm node and beyond, IEDM'17, Breil et al

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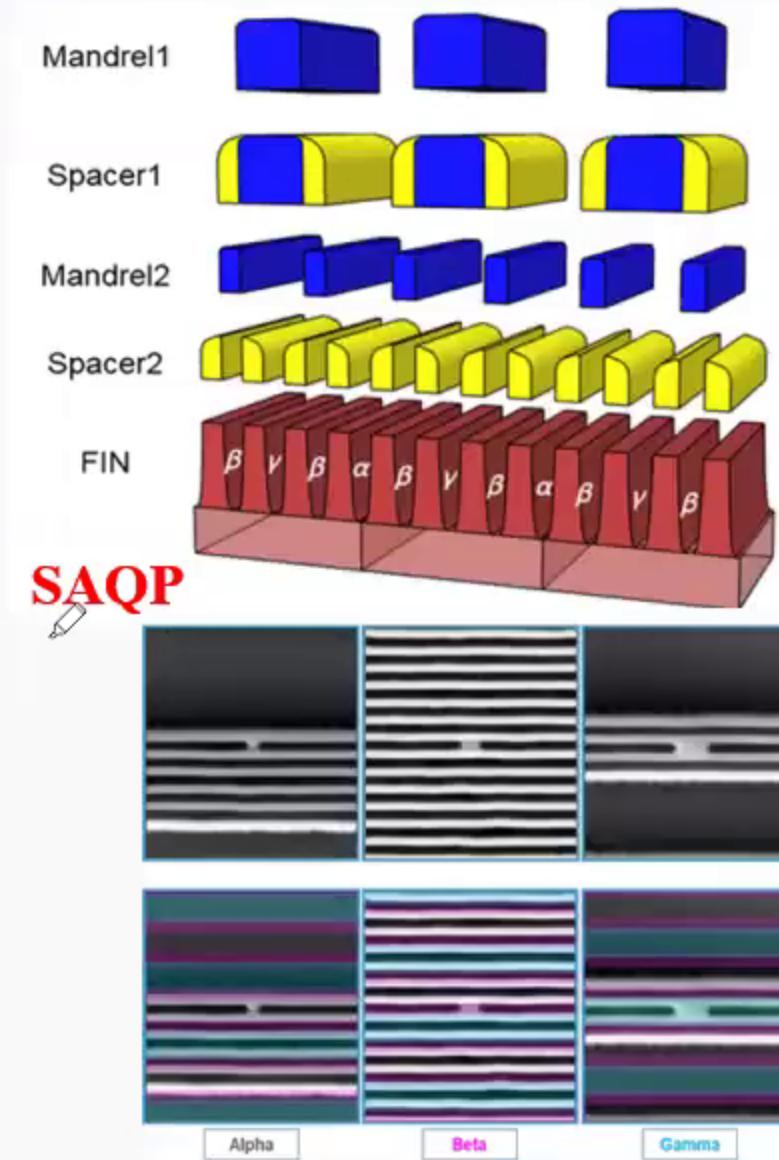
- Multi-patterning (三星/英特爾的軟肋)
- 多重图形 (Multiple patterning) 是指一种在半导体制造过程中的技术。在光刻过程中使用了多重图形曝光增强了制作图形的密度(右圖是四次曝光 SAQP)
 - 四次曝光比一次曝光(EUV)產生缺陷的概率大增，而且很難測到，因此也很難找出原因
 - 大家(三星/英特爾/台積)都有這個問題，但是台積大量應用了EUV，使得他的對 SAQP 的需求，比其他對手要少得多，所以他的良率為第一



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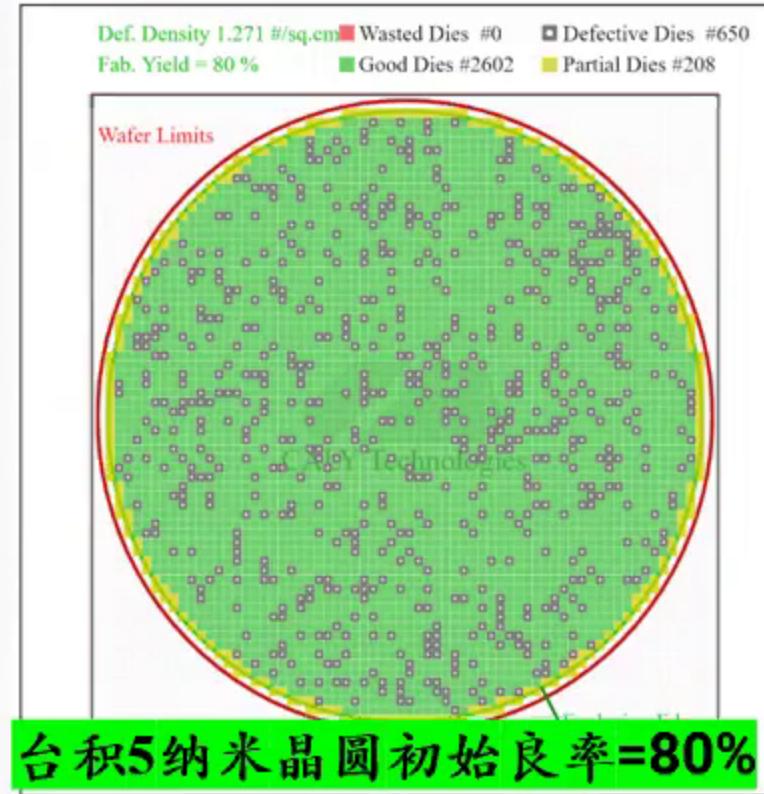
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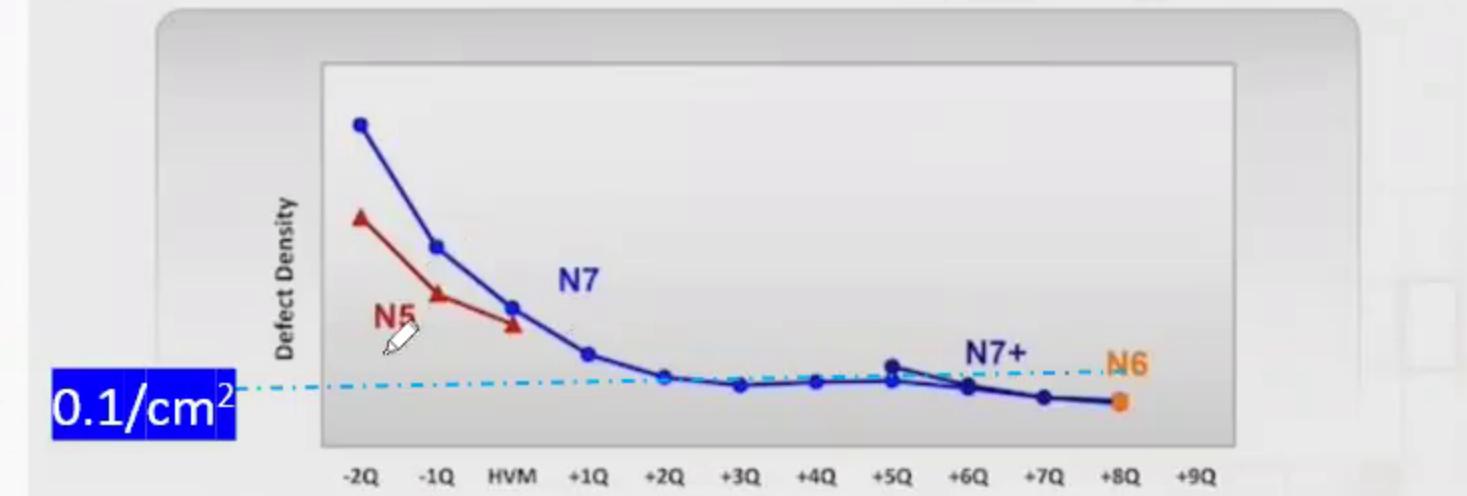
2019 30th Annual SEMI
Advanced Semiconductor
Manufacturing
Conference (ASMC)

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- 台积量產時 DD ~ $0.1/\text{cm}^2$
 - NVidia 10: ~80% Yield
 - Zen2 Chiplet: ~94% Yield



- N5 offers 15% faster speed, 30% less power and 1.8X logic density over N7
- N5 product D0 performance is progressing ahead of N7
- N5P extends additional 5% speed gain and 10% power enhancement over N5



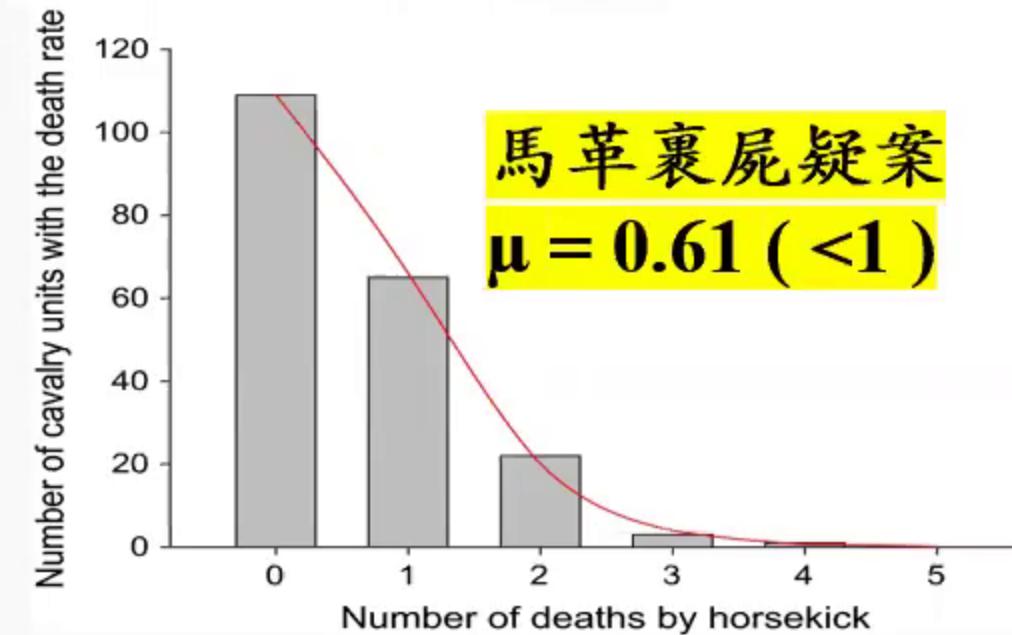
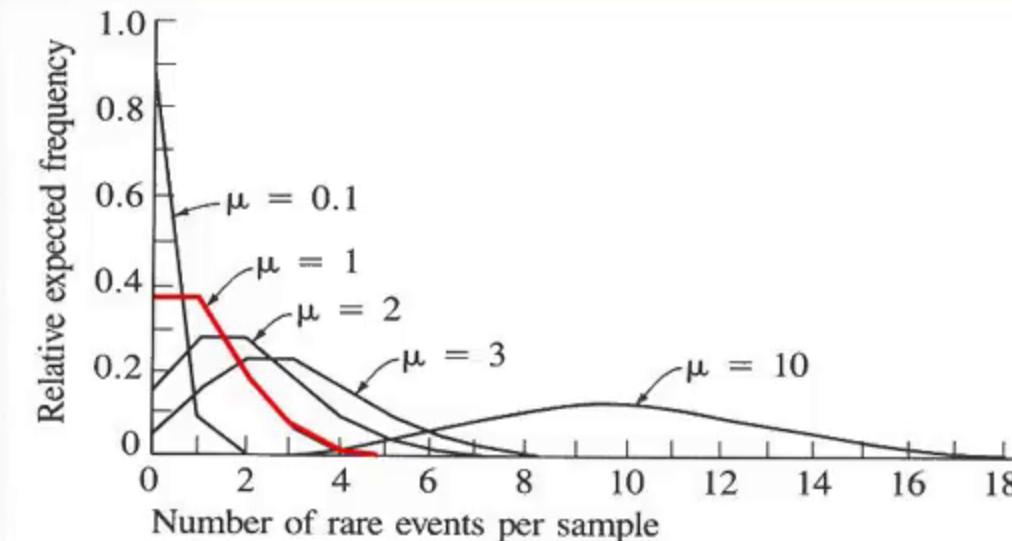
<https://www.anandtech.com/show/16028/better-yield-on-5nm-than-7nm-tsmc-update-on-defect-rates-for-n5>

Anything below $0.5/\text{cm}^2$ is usually a good metric, and we've seen TSMC pull some interesting numbers, such as 0.09 / cm^2 on its N7 process node only three quarters after high volume manufacturing

回味：柏松分布解謎了百年馬革裏屍疑案

Bortkiewicz 發現馬革裏屍疑案數據之分布乃是柏松 (Poisson Distribution)

- PMF(Poisson) : $P(k | \mu) = \frac{e^{-\mu}}{k!} \mu^k$,
 $k = 0, 1, 2, 3..$
 - 其中 μ 是 (隨機) 事件發生的平均值
 - k 是隨機事件發生的次數 (**0 開始的整數**)
 - 柏松是 discrete (一個一個數的), 所以有以上概率質量函數 probability mass function (PMF), 此函數值就是概率

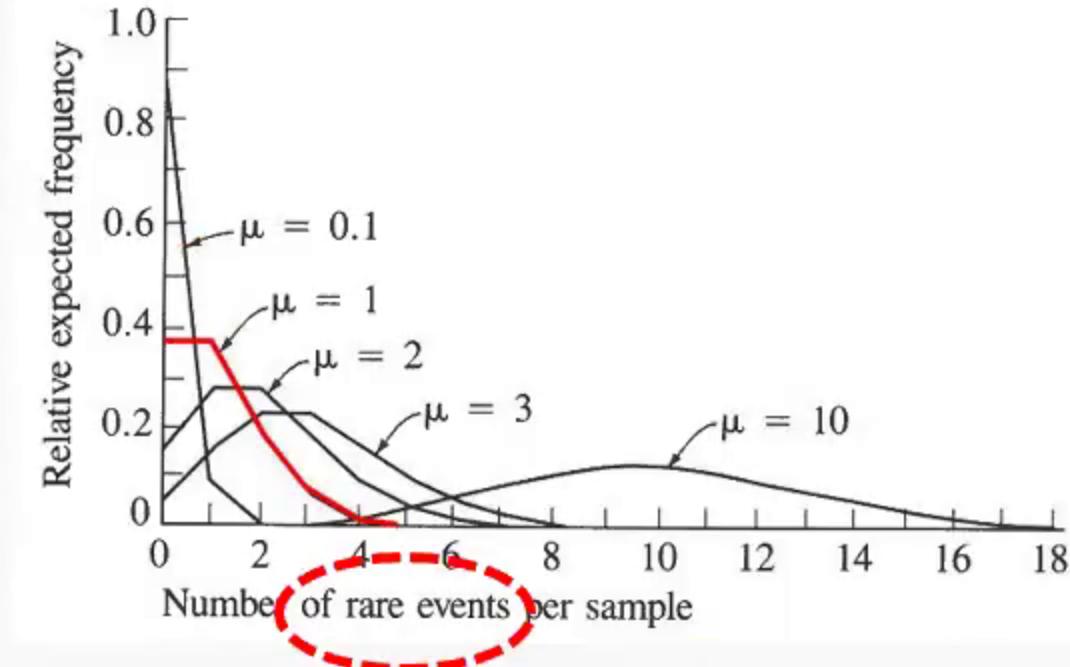


回味: 泊松过程



- 泊松过程 (Poisson Process) is a model for a series of discrete event where the *average time between events is known*, but the exact timing of events is random.

- Events are independent of each other.
The occurrence of one event does not affect the probability another event will occur.
- The average rate (events per time period) is constant.
- Two events cannot occur at the same time.



芯片良率的故事一：柏松分布

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- 如果下一个缺陷出現的要間隔時間 t ，就等同于 t 之內沒有任何缺陷出現($\mu = \lambda t$)，此為最簡單的良率 **Y**
- 以此觀念演繹出第一代的良率如右下所示

$$P(k | \mu) = \frac{e^{-\mu}}{k!} \mu^k$$

$$P(k=0 | \mu) = e^{-\mu}$$

$$Y = P(k=0) = e^{-\mu} = e^{-Da}$$

- $D = \text{defect density}$ = 是缺陷隨機發生的平均值，這是柏松分布的重要假設
- a = 缺陷所影響的芯片上的電路面積

芯片良率的故事二: Murphy

- 然而真正的良率數據分布卻沒有那麼簡單，因為往往會有一些晶圓上的缺陷竟是一簇簇(cluster)，如此一來，一經違反了柏松分布要求數據必須要有一個穩定的平均值
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$$Y = \int_0^{\infty} e^{-DA} f(D) dD$$

$f(D)$ 也並不好找

芯片良率的故事三: Gamma

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$$f(D) = [\Gamma(\alpha)\beta^\alpha]^{-1} D^{\alpha-1} e^{-D/\beta}$$

整体良率为

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Negative binomial

$$Y_r = \frac{1}{\left(1 + \frac{AD_0}{\alpha}\right)^\alpha}$$

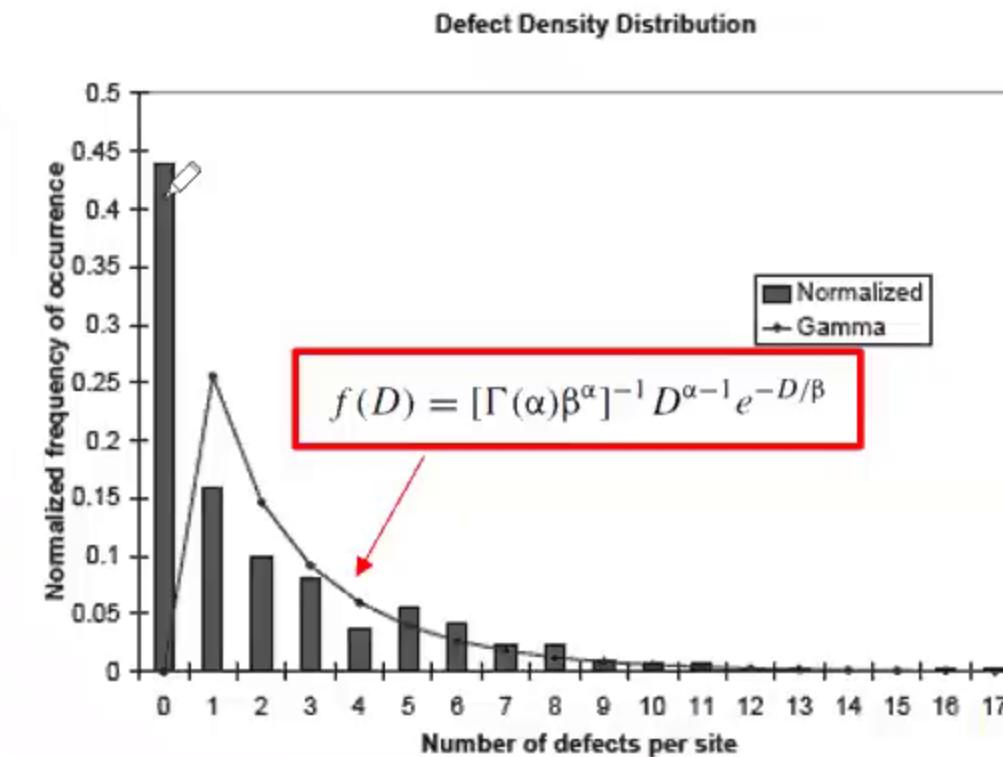


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DEFECT-ORIENTED TESTING FOR NANO-METRIC CMOS VLSI CIRCUITS, 2007, Manoj Sachdev and José Pineda de Gyvez

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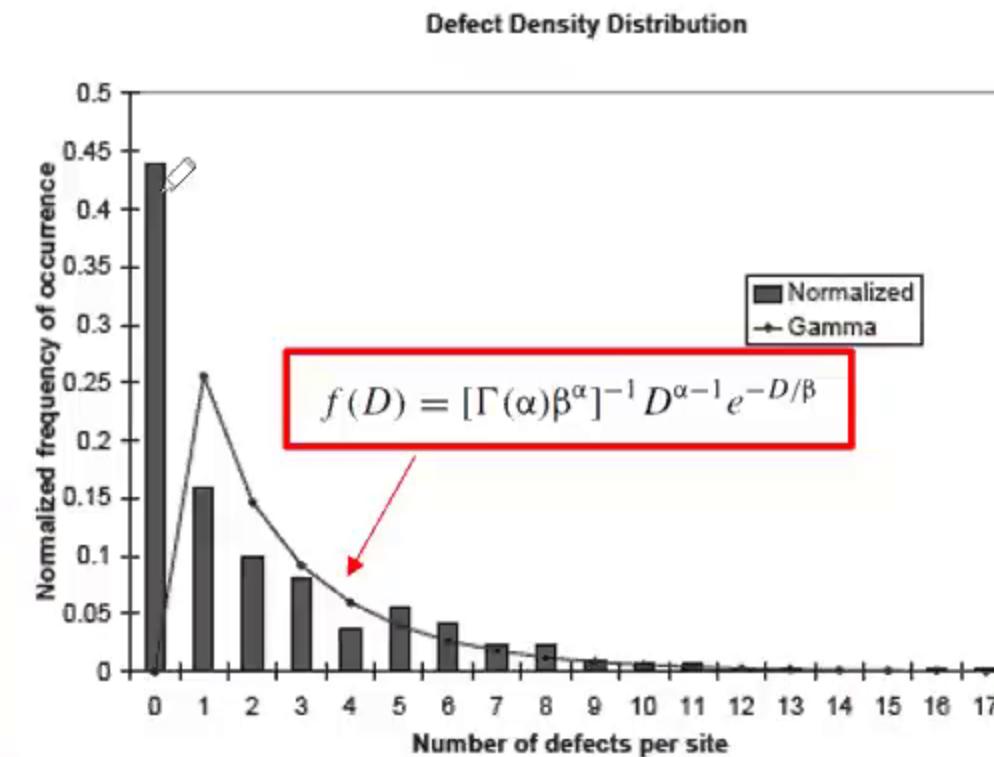


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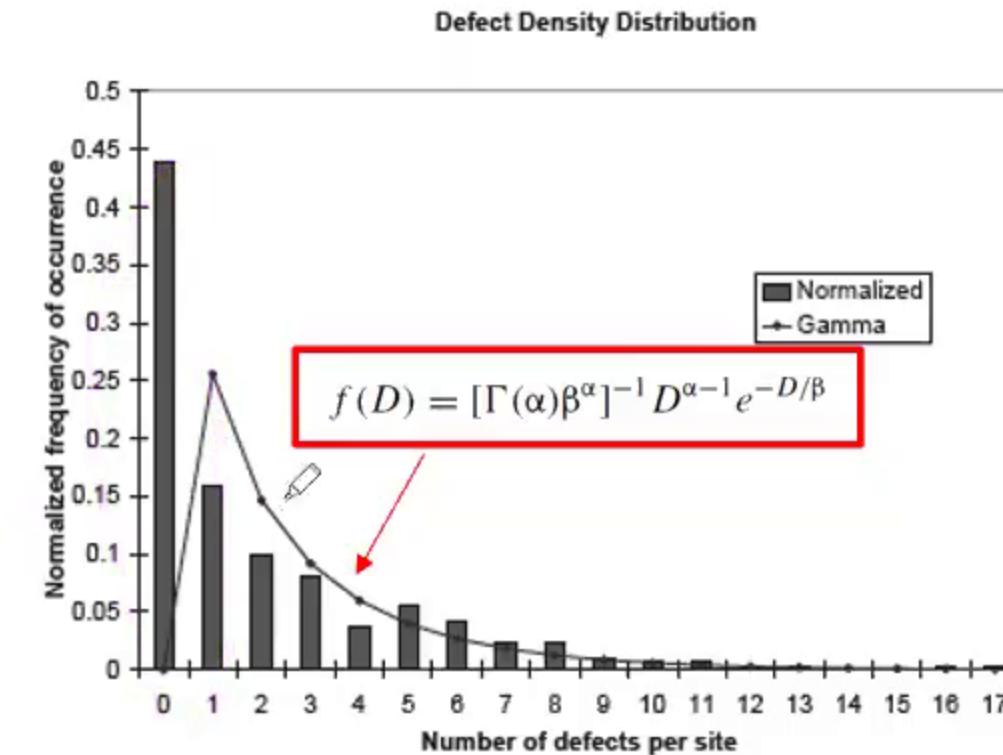


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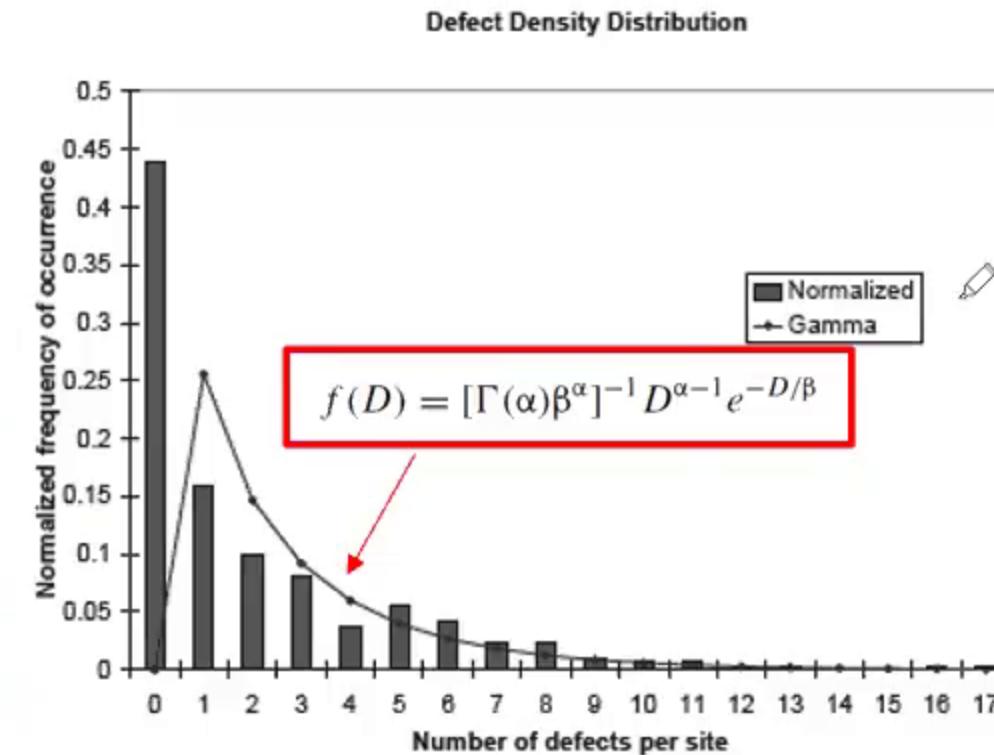


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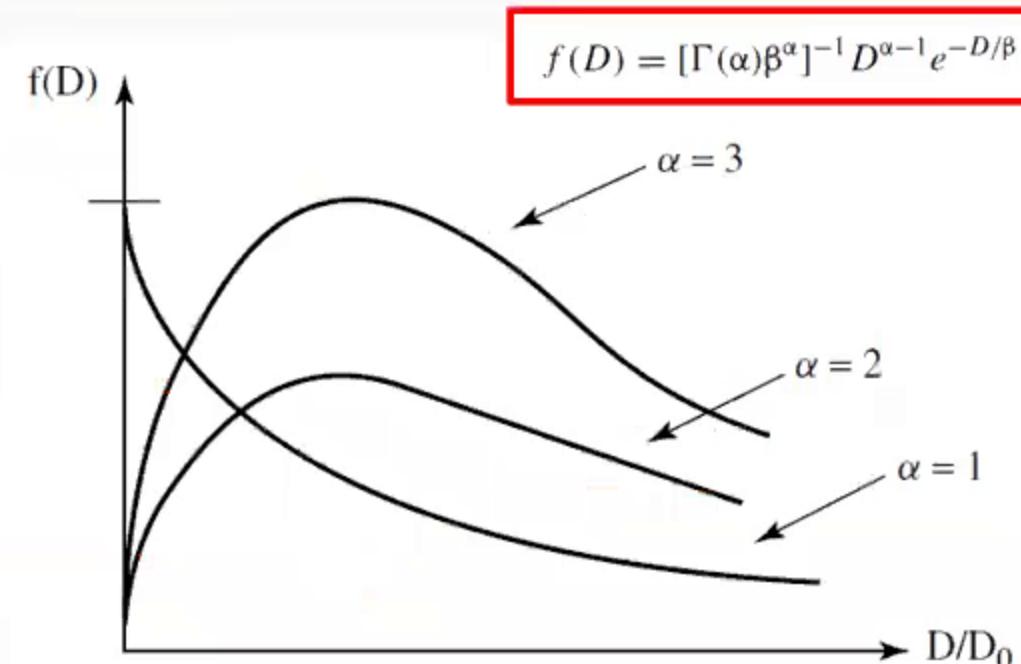
芯片良率的故事四：NB 良率推演

- 良率 $Y = f(A, D)$
 - D = defect density
 - A = critical area (in which a defect occurring has a high probability of resulting in a fault), ”缺陷必殺區”
- Murphy 建議良率 Y 如下：

$$Y = \int_0^\infty e^{-DA} f(D) dD$$

- Okabe 建議 $f(D)$ 如下：

$$f(D) = [\Gamma(\alpha)\beta^\alpha]^{-1} D^{\alpha-1} e^{-D/\beta}$$



Negative binomial

$$Y_r = \frac{1}{\left(1 + \frac{AD_0}{\alpha}\right)^\alpha}$$

芯片良率的故事五：公認的結局

- 這只是基本功，是“必要”但“非充分”的

Negative binomial

$$Y_r = \frac{1}{\left(1 + \frac{AD_0}{\alpha}\right)^\alpha}$$

Murphy

$$Y_r = \left(\frac{1 - e^{-AD_0}}{AD_0}\right)^2$$

Bose-Einstein

$$Y_r = \frac{1}{(1 + AD_0)^n}$$

Seeds

$$Y_r = e^{-\sqrt{AD_0}}$$

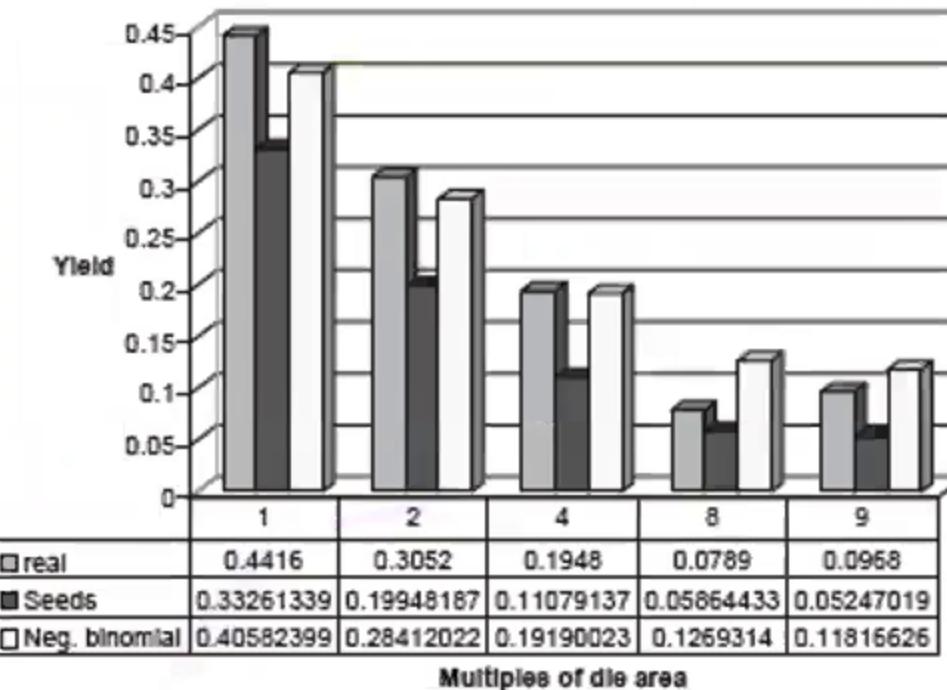
Poisson

$$P(k) = \frac{\lambda^k k e^{-\lambda}}{k!}$$

$$Y_r = P(0) = e^{-\lambda} = e^{-AD_0}$$

$$Y_r = \int_0^\infty F(D) e^{-AD} d$$

Yield Modeling. Seeds and Negative Binomial Models



- ITRS 建議使用以上Negative-Binomial (NB) distribution 產生的良率公式

Figure 7-5. Yield of Seeds and Negative Binomial models.

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芯片良率的故事六：台積實例

- 已知：台積5納米良率為80%， die size = 10mmx10mm (Apple A13)
- 試問：若芯片面積(A)改變， NB 良率變化為何？
- 解答：

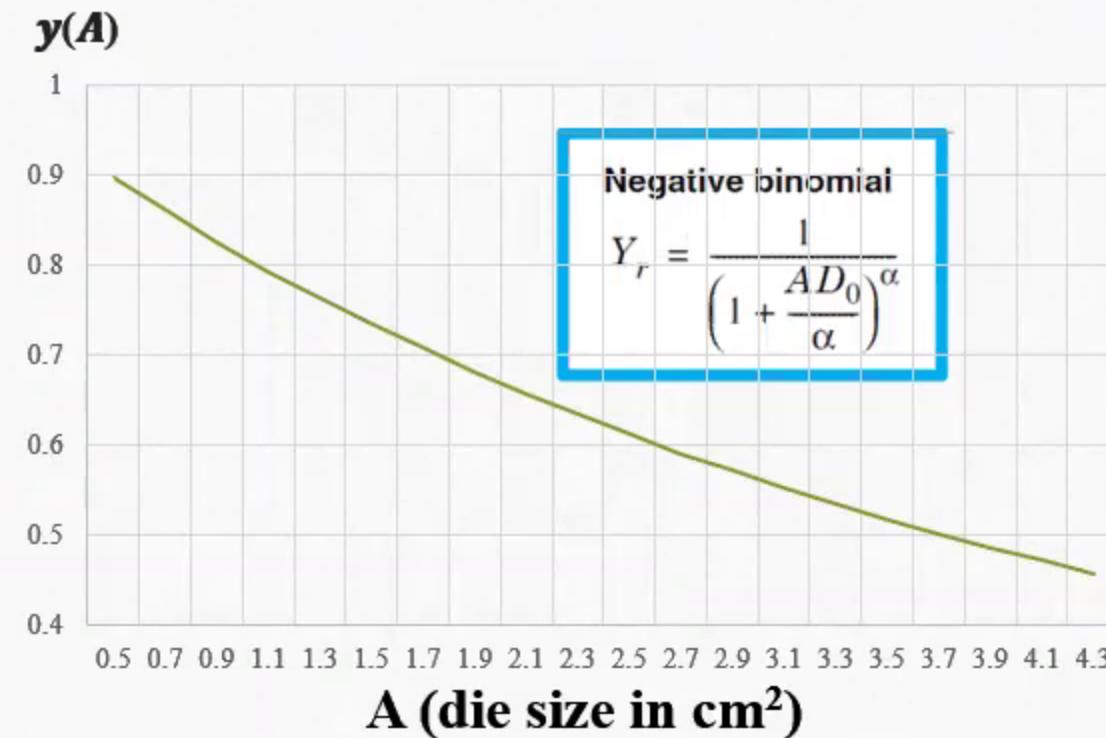
- 我們先用簡單指數良率公式，估計 defect density D_0

$$Y_r = P(0) = e^{-\lambda} = e^{-AD_0}$$

- $0.8 = \exp(-1\text{cm} * 1\text{cm} * D_0)$
- $\therefore D_0 = -\ln(0.8) = 0.223/\text{cm}^2$

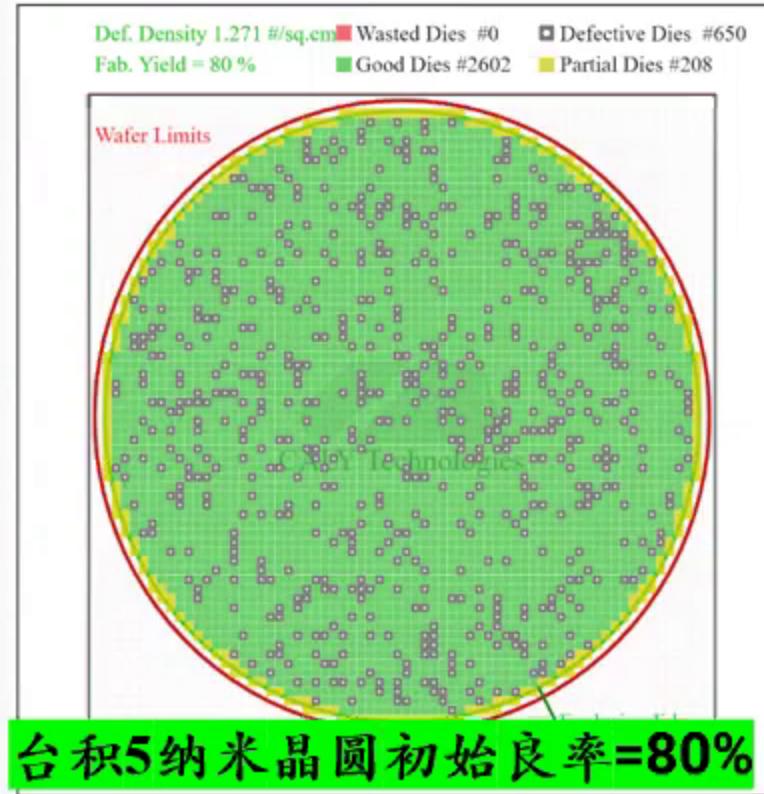
- 解答：
- ITRS 建議 $\alpha = 2$

$$\therefore y(A) = \left(1 + \frac{A * 0.223}{2}\right)^{-2}$$

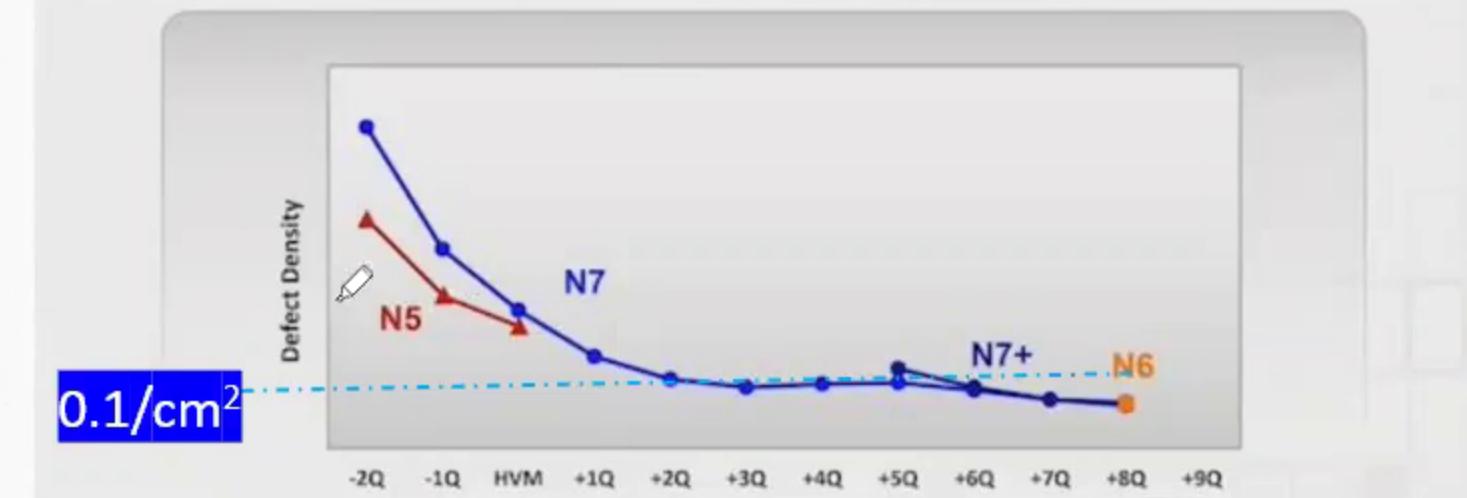


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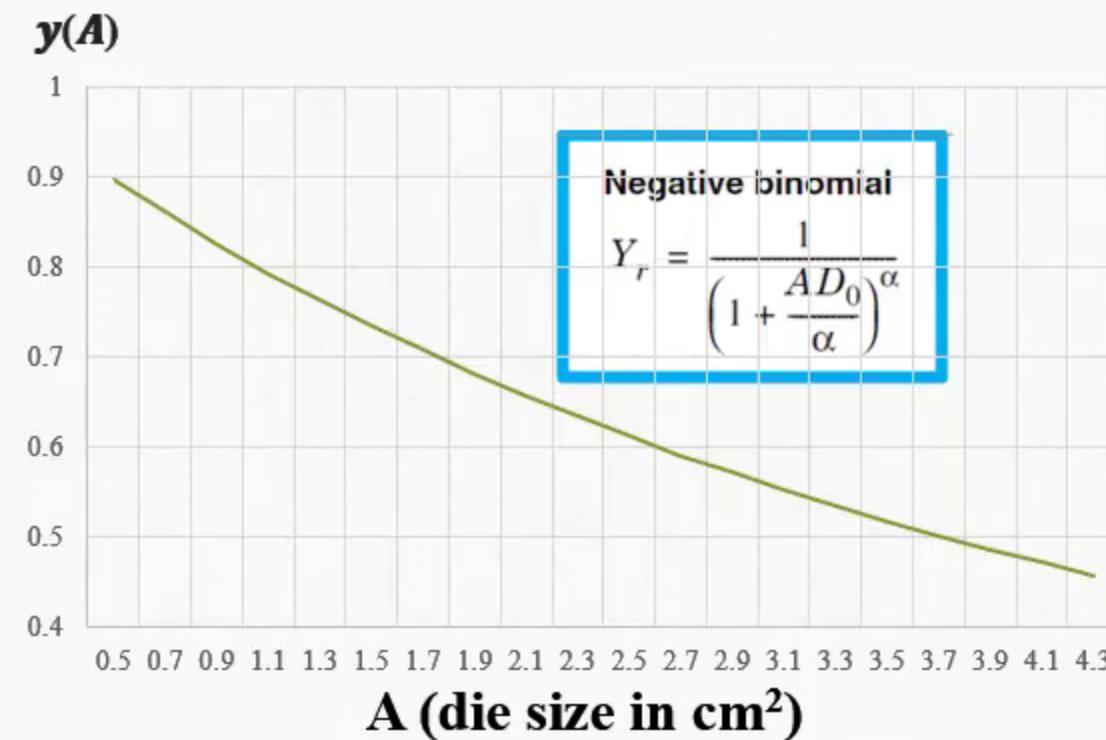
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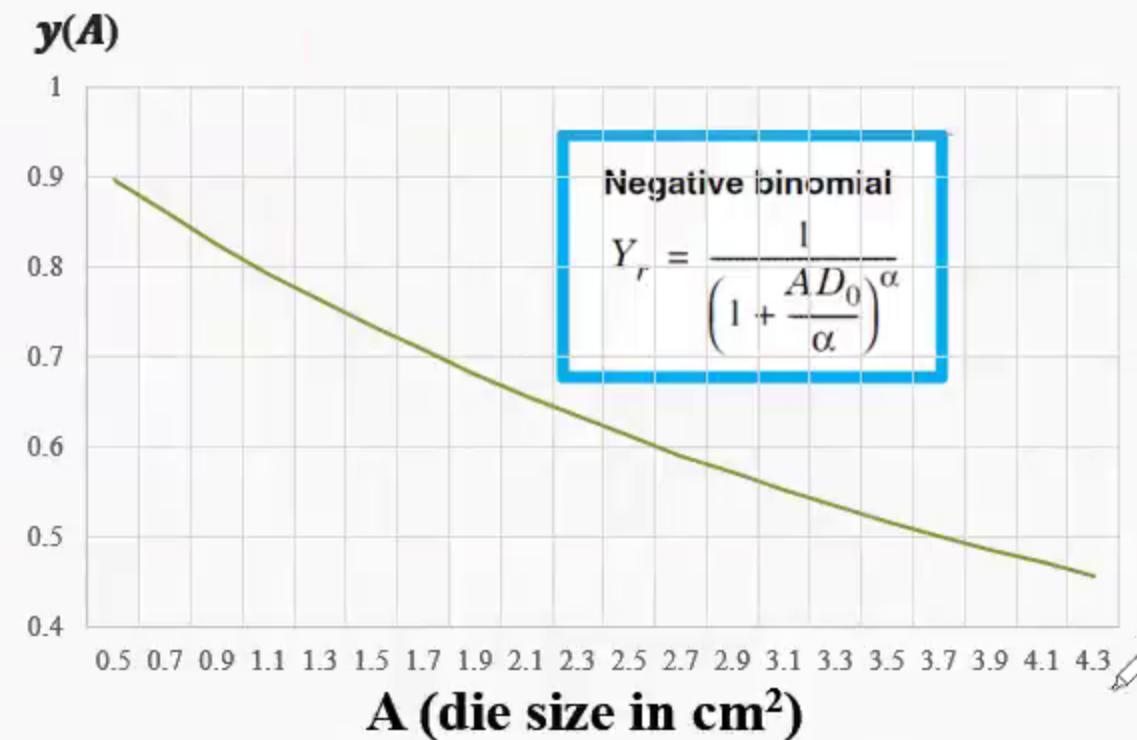
- 已知：台積5納米良率為80%， die size = 10mmx10mm (Apple A13)
- 試問：若芯片面積(A)改變， NB 良率變化為何？
- 解答：

- 我們先用簡單指數良率公式，估計 defect density D_0

$$Y_r = P(0) = e^{-\lambda} = e^{-AD_0}$$

- $0.8 = \exp(-1\text{cm} * 1\text{cm} * D_0)$
- $\therefore D_0 = -\ln(0.8) = 0.223/\text{cm}^2$

- 解答：
 - ITRS 建議 $\alpha = 2$
 - $\therefore y(A) = \left(1 + \frac{A * 0.223}{2}\right)^{-2}$



芯片良率的故事七: 芯片越大, 良率越低

芯片尺寸 vs 良率

- FPGA (Xilinx, VU19P) 芯片超大 = 9cm^2
 - 良率非常低, 一個300mm晶圓只能得到一個或數個芯片, 所以要價極高
- 中芯建議小chiplet 概念, 見右圖, die size越小, 良率越高

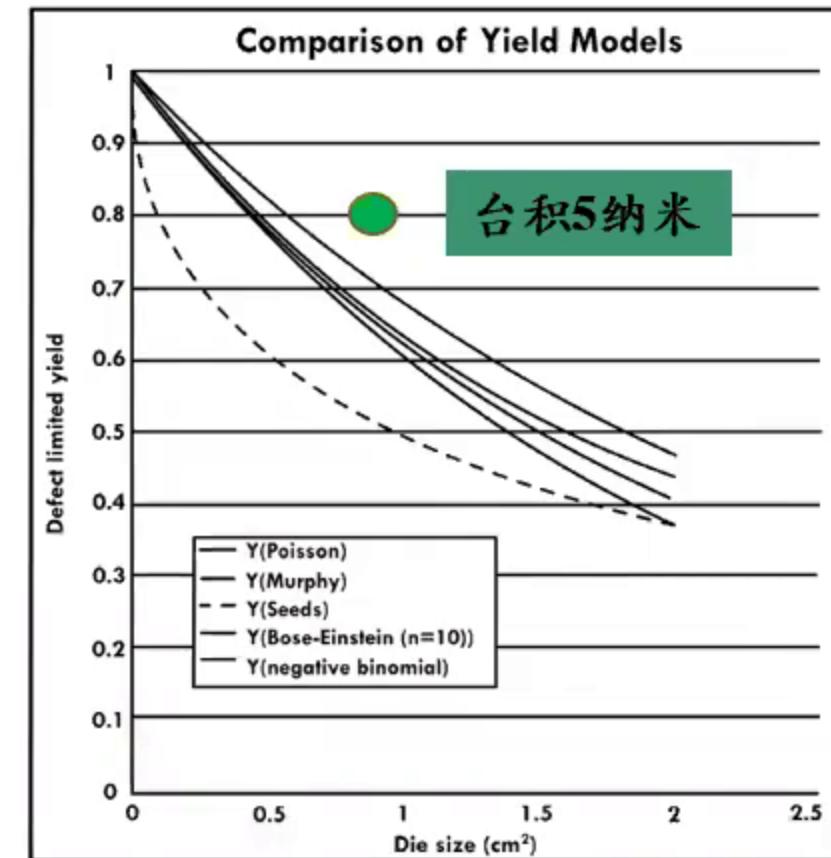


Figure 7: Defect yield density as a function of die size for different models. In all of these the yield reduces with die size. The steepest drop is for the Seeds model, which assumes an exponential dependence for the defect density distribution. Adapted from *Microchip fabrication - Peter van Zant*.

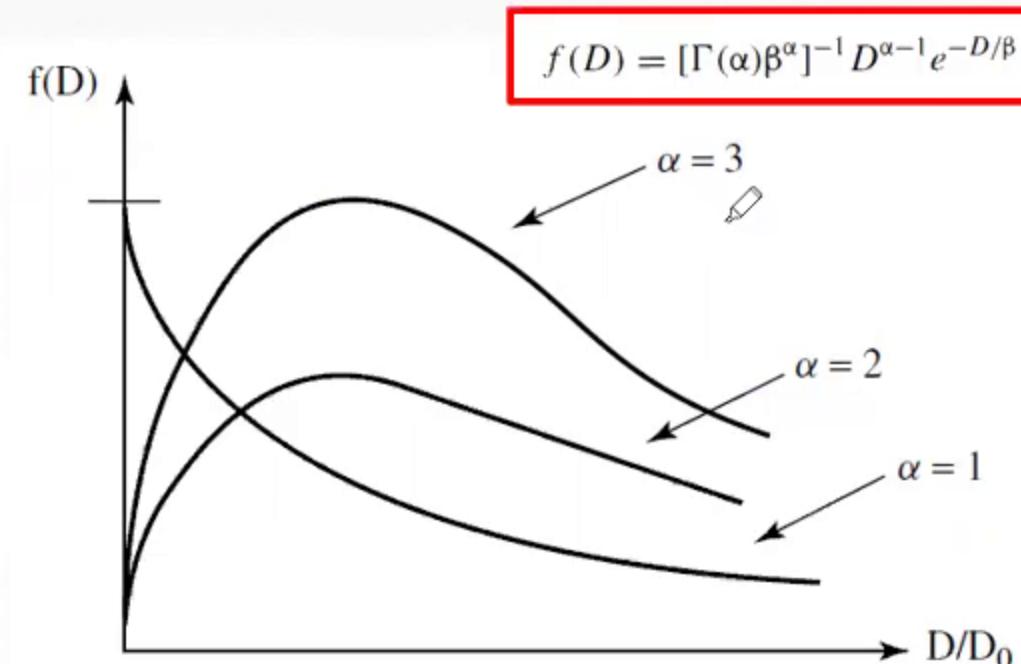
芯片良率的故事四：NB 良率推演

- 良率 $Y = f(A, D)$
 - D = defect density
 - A = critical area (in which a defect occurring has a high probability of resulting in a fault), ”缺陷必殺區”
- Murphy 建議良率 Y 如下：

$$Y = \int_0^\infty e^{-DA} f(D) dD$$

- Okabe 建議 $f(D)$ 如下：

$$f(D) = [\Gamma(\alpha)\beta^\alpha]^{-1} D^{\alpha-1} e^{-D/\beta}$$



Negative binomial

$$Y_r = \frac{1}{\left(1 + \frac{AD_0}{\alpha}\right)^\alpha}$$