

THIN-FILM TRANSISTORS

edited by
Cherie R. Kagan
Paul Andry

*IBM T. J. Watson Research Center
Yorktown Heights, New York, U.S.A.*



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Preface

As thin-film transistors (TFTs) are increasingly incorporated into applications, particularly for mobile computing and communication devices, there is a need for a book dedicated to describing the device physics, operation, various structures, and characteristics of the TFT. This book gives an account of materials for TFTs, providing an evolutionary presentation of materials past, present, and potentially future, and describing the important or desirable materials properties. In particular, the electrical requirements of TFTs in active-matrix liquid crystal displays—the most notable application of TFTs—are outlined, followed by future applications of TFTs in the computation and communications devices that are increasingly pervading our daily lives.

The book is divided into two main parts. [Chapters 1–5](#) focus on the development, materials, device fabrication, and properties of TFTs based on amorphous and polycrystalline silicon. It also includes an in-depth presentation of the “killer application” of amorphous silicon transistors in active-matrix liquid crystal displays. [Chapters 6–10](#) describe new, alternative, and potentially disruptive technologies based on organic and organic-inorganic hybrid semiconducting materials. These materials may be deposited by low-cost, low-temperature processes on a wide range of substrates, including plastic, that may enable flexible electronic applications. The properties, processing, patterning, and device characteristics of TFTs based on organic and organic-inorganic hybrid materials are examined.

Chapter 1 gives a historical perspective, describing the major steps in TFT development, from the first patents issued in the 1930s to the present day. The chapter describes the characteristics of early transistors prepared from compound semiconductors, as well as the pioneering work of Shockley and others, which began in the study of TFTs but ultimately led to the development of both the point contact transistor and the JFET through detailed studies of surface states in elemental semiconductors. Following the analysis of the JFET in the 1950s, which led to a model of device operation still used today (the gradual channel

approximation), the chapter describes the re-emergence of the TFT in the 1960s as a candidate for low-cost logic, once again using polycrystalline compound semiconductors such as CdS and CdSe. With the introduction of CMOS, however, the proliferation of the TFT was effectively put off until the 1970s. The chapter outlines how major breakthroughs in amorphous and polycrystalline silicon materials and device processing, as well as the advent of active-matrix display technology, eventually brought us to a place where applications using TFTs are ubiquitous.

[Chapter 2](#) discusses the preparation and properties of TFTs employing today's workhorse material, amorphous silicon (a-Si). Making use of the gradual channel approximation in the linear and saturation regimes, the important electrical characteristics and extracted device parameters of a number of popular TFT structures are compared and contrasted, and the most important aspects of each structure are described, including device geometry, process flow, and number of mask levels. The chapter discusses the key plasma-enhanced chemical vapor deposition (PECVD) process parameters leading to high-electrical-quality semiconductor and gate insulator materials, including substrate temperature, gas pressure, gas flow and mixing ratios, and input rf power. Electrical quality of the a-Si TFTs is correlated with interface and bulk film properties, including roughness, stress, stoichiometry, etch rate, hydrogen content, impurity concentrations, optical constants, and electrical conductivity. In the final section, the author deals with the subject of fabricating a-Si TFTs on plastic substrates, and in particular the challenges of low-temperature PECVD deposition, the need for special preparation of the substrates, the use of inorganic gas barrier layers, and the effects of stress and their mitigation.

[Chapter 3](#) begins with the numerical simulation of a-Si thin film transistors. While the simulations performed make use of the specific deep gap and tail density of states for a-Si, the approach is intended as a model for the simulation of any TFT. It includes the basic equations used to generate the electrostatic potential and carrier Fermi potentials in the device and hence the current densities and electric fields during operation. Researchers building TFTs from new materials often attempt to quantify only parameters such as the mobility and on/off ratio. However, meaningful extraction of parameters from electrical characteristics must take into account not only the properties of the underlying semiconductor material but also the boundary conditions imposed by the device geometry, especially the contacts. An important, often overlooked, consideration is the effect of contact resistance, which for TFTs with staggered electrodes is typically neither negligible nor necessarily linear. Simulation, in concert with characterization of TFTs in the linear and saturation regimes, allows one to probe the true nature of the semiconductor and thus accurately measure the mobility, subthreshold slope, threshold voltage, contact resistance, and other properties as well as the associated dependencies of each of these on temperature, semiconductor thickness, and ap-

plied bias. Accurate determination of these parameters not only sheds light on the bulk and interfacial electronic states present in the materials comprising the device, but represents a major step toward qualifying these as *de facto* transistor materials for existing and future commercial applications. [Chapter 3](#) continues to describe advanced structures and processes, both for enabling accurate measurements of electronic materials quality and for enabling higher-performance TFTs for advanced display applications. Finally, the authors describe some of the basic mechanisms of bias-induced instability in a-Si/SiNx TFTs, experimental methods by which these mechanisms may be distinguished, and a simple model for extracting threshold shift as a function of bias, temperature, and time.

[Chapter 4](#) covers the preparation and properties of polycrystalline silicon TFTs. The development of polycrystalline TFTs is driven primarily by the push toward higher integrated functionality on the display panel and lower power operation. Starting from the TFT requirements for both integrated drivers and pixel switches, the authors describe the critical areas of poly-Si fabrication, including thin Si film deposition, recrystallization, gate insulator formation, and dopant activation. The advantages and disadvantages of crystallization methods are outlined, including solid-phase crystallization, rapid thermal annealing, and metal-induced crystallization. Advanced low-temperature recrystallization methods, notably excimer laser annealing, are detailed as they are becoming increasingly important in commercial products requiring higher-mobility polycrystalline silicon. The main factors controlling grain size, and hence mobility, are considered in terms of the obvious technological need for good throughput, electrical uniformity, and reproducibility of the poly-Si films produced. Formation of the gate insulator (subject to the constraints on thermal budget), and, in particular, trade-offs between process throughput and TFT performance, due to the dual requirement of high interface quality and good bulk insulator properties, are discussed. The chapter concludes with the presentation of a representative 8 mask level process flow for the fabrication of a low-temperature poly-Si active matrix array for LCD applications.

[Chapter 5](#) describes the use of TFTs as the array switching elements in active-matrix liquid crystal displays. The basics of liquid crystal operation in an LCD panel and the limitations of passive matrix driving, leading to the widespread adoption of active-matrix displays, are discussed. Working from the design side, the author outlines a simple, physically based parameter analysis to identify functional dependencies, performance limits, and minimum requirements for TFTs in displays, independent of active-channel semiconductor. Based on the design requirements, the dynamic TFT requirements in terms of on/off current ratio, pixel charge-up time, and voltage feedthrough switching error based on a particular array design are outlined. The effects of TFT nonlinear contact resistance and parasitic capacitance are discussed, as well as other sources of flicker in active-matrix liquid crystal displays. Solutions to electrical overstress and electrostatic

discharge are presented as a means of improving active-matrix yield and thereby lowering total panel production cost. The author notes the need for active-matrix array testing and compares testing schemes. Recent commercial applications of TFTs for integrated drive circuitry and built-in multiplexing for improved panel testing are also discussed. Active-matrix driving schemes are illustrated, including methods that minimize scan line delay and vertical crosstalk. Finally, the author provides a short review of the specifications of common driver chips used today, followed by a description of system-level electronics, and, in particular, some of the challenges associated with designing and driving state-of-the-art, high-resolution, large-area displays.

In [Chapter 6](#), organic TFTs are introduced. The advances made in synthetic control over material purity and functionality and in physical understanding of charge transport in organic semiconductors have enabled the fabrication of organic transistors with field-effect mobilities and current modulation comparable to that for a-Si transistors. The best organic semiconductors based on small molecules (e.g., pentacene and copper phthalocyanine), short-chain oligomers (dihexylhexathiophene), and polymers (regio-regular polythiophene) are highlighted. This chapter describes the molecular structure and physics of charge transport in the organic solid state that gives rise to semiconducting behavior. The important materials properties and the correlation between the morphology of the thin film and the charge carrier mobility in organic transistors are presented. An account is given of the progress made in these materials systems and their device fabrication and modeling.

Small molecules and short-chain oligomers are typically insoluble but, when deposited by vacuum evaporation, form thin films that are ordered and oriented. They provide model systems for studying intermolecular charge transport in organic semiconductors and yield organic TFTs with the highest field-effect mobilities of $\sim 1 \text{ cm}^2/\text{V}\cdot\text{sec}$. [Chapter 7](#) reviews the vacuum techniques used to grow organic materials, as well as advances in both n- and p-type small-molecule organic semiconductors. Emphasis is placed on the thin-film deposition and device structure and characteristics of pentacene, today's front-running organic semiconductor. Engineering the device structure of pentacene transistors has been shown to improve device performance as high-dielectric-constant gate insulators can be used to achieve low-voltage operation and molecular surface modification can improve pentacene morphology and therefore device mobility.

[Chapter 8](#) begins with a more in-depth presentation of how the flexibility in the chemistry of organic molecules, oligomers, and polymers may be used to tailor the device characteristics of n- and p-channel organic transistors. The exploration of organic transistors is driven by the unique ability to deposit organic semiconductors by low-cost, low-temperature processes that may reduce the cost of electronic circuits and displays and enable the fabrication of flexible electronic applications. Integration of organic semiconductors into circuits requires the de-

velopment of low-cost, low-temperature patterning processes. Novel processes such as screen-printing, micromolding in capillaries, microcontact printing, and near-field photolithographic techniques used to fabricate organic transistors are described. These materials and techniques are combined to form an organic transistor backplane in the demonstration of an electrophoretic display, or “electronic paper.” A perspective is given on the development of low-cost, large-volume processing such as reel-to-reel techniques that may be used to make very low-cost logic devices and displays. Finally, larger-scale integration of organic TFTs in architectures to prepare logic devices such as inverters and ring oscillators is explained.

Solution deposition provides the lowest-cost and therefore most desirable route for the deposition of materials for transistors, particularly for large-area applications. Organic polymers are typically more soluble, since they may be chemically modified with organic side chains, and are better film formers than small molecules and short-chain oligomers. [Chapter 9](#) presents the preparation, ink-jet printing, and device physics and characteristics of polymeric TFTs. Improvements in the field-effect mobility of polymeric transistors have been achieved through the design and synthesis of molecular systems with structural regularity and through the use of surface templating to improve the order in polymeric thin films. While polymeric TFT performance has improved, it is not as good as small-molecule TFTs, but the flexibility to ink-jet-print entire circuits offers an advantage for the fabrication of low-cost electronics for applications presented in this chapter, such as radiofrequency identification tags and displays.

[Chapter 10](#) presents organic-inorganic hybrid materials as the semiconducting channel materials in TFTs. Organic-inorganic hybrid materials are molecular-scale composites that promise the high carrier mobilities of inorganic semiconductors, but may be deposited by the low-cost, low-temperature techniques common to organic materials. A subset of hybrid materials known as organic-inorganic perovskites is described, along with the chemical flexibility, crystal structure, and physical properties of these materials. Hybrid materials can be deposited from solution or from the vapor phase to form polycrystalline thin films. To date, solution-deposited organic-inorganic TFTs have mobilities comparable to those of a-Si and the best vacuum-deposited organic transistors. The chapter provides a simple method to pattern these materials and devices using microcontact printed molecular templates to restrict the semiconductor deposition to the channels of transistors.

*Cherie R. Kagan
Paul Andry*

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Contributors

Zhenan Bao Bell Laboratories, Lucent Technologies, Murray Hill, New Jersey, U.S.A.

Lukas Buergi Cavendish Laboratory, University of Cambridge, Cambridge, United Kingdom

Christos D. Dimitrakopoulos IBM T. J. Watson Research Center, Yorktown Heights, New York, U.S.A.

Ananth Dodabalapur Microelectronics Research Center, University of Texas at Austin, Austin, Texas, U.S.A.

Richard Friend Cavendish Laboratory, University of Cambridge, and Plastic Logic Ltd., Cambridge, United Kingdom

Francis Garnier Laboratoire des Matériaux Moléculaires, Thiais, France

M. K. Hatalis Lehigh University, Bethlehem, Pennsylvania, U.S.A.

Webster E. Howard eMagin Corporation, Hopewell Junction, New York, U.S.A.

Jin Jang Kyung Hee University, Seoul, Korea

Cherie R. Kagan IBM T. J. Watson Research Center, Yorktown Heights, New York, U.S.A.

Jerzy Kanicki* University of Michigan, Ann Arbor, Michigan, U.S.A.

Howard E. Katz Bell Laboratories, Lucent Technologies, Murray Hill, New Jersey, U.S.A.

Takeo Kawase Cavendish Laboratory, University of Cambridge, and Epson Cambridge Laboratory, Cambridge, United Kingdom

Frank R. Libsch IBM T. J. Watson Research Center, Yorktown Heights, New York, U.S.A.

Sandrine Martin University of Michigan, Ann Arbor, Michigan, U.S.A.

David B. Mitzi IBM T. J. Watson Research Center, Yorktown Heights, New York, U.S.A.

John A. Rogers Bell Laboratories, Lucent Technologies, Murray Hill, New Jersey, U.S.A.

Henning Sirringhaus Cavendish Laboratory, University of Cambridge, and Plastic Logic Ltd., Cambridge, United Kingdom

A. T. Voutsas Sharp Laboratories of America, Camas, Washington, U.S.A.

* CPOS, University of California, Santa Barbara, California (sabbatical)

1

Thin Film Transistors—A Historical Perspective

Webster E. Howard

eMagin Corporation, Hopewell Junction, New York, U.S.A.

1.1 INTRODUCTION

Thin-film transistors (TFTs) have in the past 10 years become the “rice” of the electronic flat panel industry, just as silicon chips were earlier called the “rice,” or staple, of the electronic computer revolution. Tens of giant factories today turn out millions of displays each per year, with each display incorporating several million thin-film transistors.

How we got to this point is an interesting tale of technology evolution and development that stretches over nearly 70 years, going back to the earliest days of semiconductor physics. It was at that time that materials were first being classified according to their electronic structure so that semiconductors were understood not just as materials with conductivity intermediate between that of metals and insulators, but as crystalline materials with a small number of mobile charges per unit cell and a distinguishing temperature dependence of conductivity.

Looking back, we can see that the concept of the thin-film transistor and its potential utility significantly predated the device that gave rise to the term *transistor*. Indeed, for many years it was overshadowed by the astounding developments associated with the original bipolar transistor and its technological cousin, the metal oxide semiconductor field-effect transistor (MOSFET).

In this chapter we will review, decade by decade, how the thin-film transistor has evolved in materials and structure to the forms most widely used today.

1.2 THE 1930s

Most authors have credited Lilienfeld [1] with the first invention of a field-effect device, in a 1934 patent. In his favor is the fact that his example embodiment, shown in Figure 1.1, has appropriate example materials, namely, a semiconductor active layer (Cu_2S), an insulator (Al_2O_3), and a metal gate (Al). The problem comes in his description of the invention and in his wording of his claims. He reveals no understanding of semiconductors as a class of solids, and indeed he specifies that the active layer should be of “substantially greater conductivity” than the substrate (gate). Even though the claims are in this matter contradictory to his examples, one might have followed his teachings and made a working device, despite the fact that he presents no evidence of actually having done so. The figure also shows a thinning of the active layer in the middle, which he requires to be of molecular dimensions in its thickness.

As argued by Brody [2], Heil [3], in his 1935 patent, has a more solid claim to inventorship of the TFT. Heil displays a knowledge and understanding of semiconductors, including the existence of *p*-type (called by him “gap”) semiconductors. He also refers to their characteristic temperature dependence of resistivity, inverse to that of metals. His device structure, shown in Figure 1.2, is correct, and his example materials include tellurium, cuprous oxide, vanadium pentoxide, and iodine. Of these, tellurium was used with considerable success many years later. Heil’s patent, like that of Lilienfeld, also seems to be a concept patent, with no indication of any reduction to practice.

Shockley [4] has described in great detail the efforts at Bell Laboratories, immediately preceding and following World War II, to develop electronic switch-

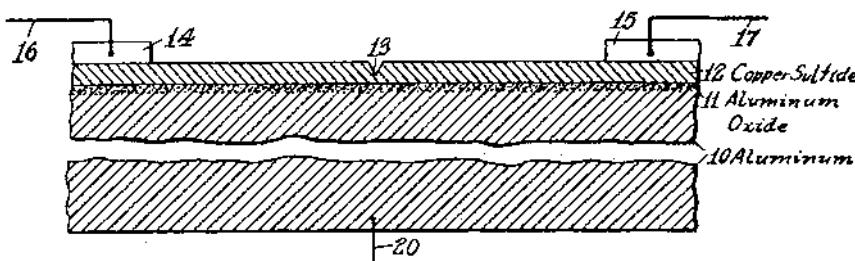


FIGURE 1.1 Diagram of the first field-effect electronic device. (From Ref. 1.)

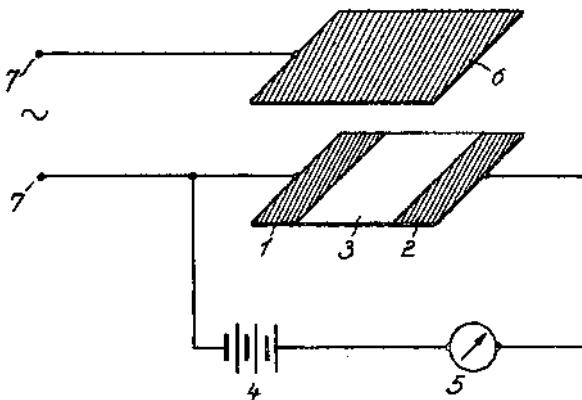


FIGURE 1.2 Diagram of an early field-effect device. (From Ref. 3.)

ing devices to replace the mechanical telephone switching systems then in use. Some scientists were leaning toward the use of vacuum devices, but Shockley and his team were aiming at a solid-state solution.

Shockley's original thinking, in 1939, was based upon his understanding of the Shottky diode, i.e., a metal–semiconductor contact. He realized that adjacent to the metal the semiconductor was depleted of mobile charge and that the extent of the depletion region depended upon the applied voltage. This and his knowledge of vacuum tubes led him to envision a triode where a grid embedded in semiconductor material could be used to deplete a zone between cathode and anode, cutting off the flow of current. This first idea, in a simpler geometry, represented the invention of the metal–semiconductor field-effect transistor, or MESFET. This particular Shockley invention was not to be realized as an effective device until the late 1960s, by C. A. Mead [5].

1.3 THE 1940s

Returning to his Shottky-gate idea after the war, and realizing that his embedded-gate structure might be difficult to make, Shockley adopted his basic strategy of trying the simplest approach first. However, he did not return to the MESFET structure. Instead, the simplest approach was judged to be the application of an electric field to a semiconductor film using an insulator and a gate electrode.

Fortunately, or unfortunately, depending upon your historical perspective, rather than trying a familiar compound semiconductor such as copper oxide or one of the lead salts, Shockley had already decided that semiconductor research

should be focused for simplicity on elemental semiconductors, specifically germanium and silicon. Thus the attempt to make a thin-film field-effect device used a germanium film.

The results were surprising and disappointing. The change in conductivity observed was far smaller than expected theoretically, based upon the capacitance of the gate structure. The explanation for the failure was, according to Shockley, provided by John Bardeen. Bardeen recognized that implicit in the calculation of the expected effect was the assumption that charge added electrostatically would have the same mobility as the native bulk charge and that this assumption would not be valid if there were a significant number of surface states with energies located in the germanium band gap.

It was this observation, according to Shockley, that creatively redirected the program from improving the field-effect device to studying surface states on germanium. Improving the device, for example, by trying a different semiconductor, might have led to a better TFT sooner. But the study of the germanium surface states led relatively quickly to the discovery of the point-contact transistor by Bardeen and Brattain in late 1947 [6], which in turn led to the invention of the junction transistor in early 1948 [7]. At that point, however, bipolar devices became the focus of attention, not only at Bell Laboratories but among almost all electronic device physicists and engineers.

Later in 1948, Shockley's analysis of pn junction structures led him to invent the junction field-effect transistor, now known as the JFET, almost as an afterthought to his all-consuming bipolar junction transistor work.

1.4 THE 1950s

There was little activity on TFTs in the 1950s, but Shockley's publication, in 1952, on the junction field-effect transistor [8] has great importance nevertheless. Looking back at this work, it appears that it greatly influenced subsequent work and analysis on TFT devices as well as the terminology used from that point on. The negative terminal of an electron channel device or the positive terminal of a hole channel device became the “source,” with the opposite terminal becoming the “drain.” The insulated field electrode, called by Heil the “control electrode,” became the “gate.” [Figure 1.3](#) shows a schematic drawing of a JFET, as treated by Shockley, taken from Dacey and Ross [9].

One of the striking characteristics of both JFET and TFT is the saturation of source–drain current versus source–drain voltage. Analysis of the characteristic led to the concept of a “pinch-off” (see Fig. 1.3), a point between the source and drain where the local carrier density goes nearly to zero.

The mathematical analysis of this phenomenon by Shockley introduced a simplifying approach now known as the gradual channel approximation, whereby the device is viewed as a chain of one-dimensional devices, the characteristics

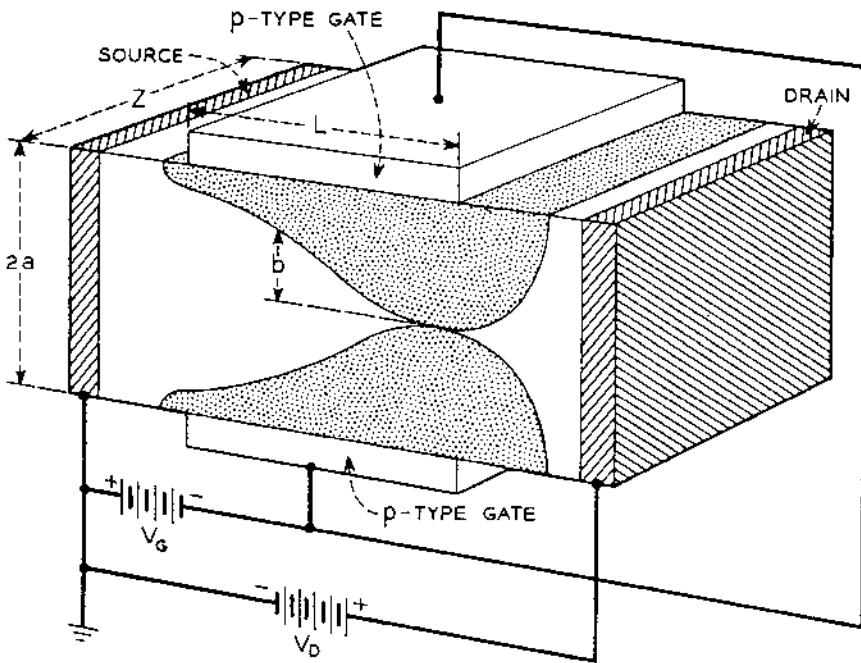


FIGURE 1.3 Schematic of the space charge regions in a junction field-effect transistor. (From Ref. 9.)

of which are determined only by their position in the larger device. That is, nonlocal transport effects are ignored, and quasi-equilibrium is assumed throughout. While any high-performance field-effect transistor, e.g., a modern JFET or MOSFET, requires a much more sophisticated three-dimensional modeling to achieve an accurate description, the fact is that for most of today's TFT applications, the gradual channel type of analysis is sufficient.

The basis for the analysis of frequency dependence, or speed, of TFTs also goes back to the days of Shockley and his coworkers, who analyzed JFETs. What comes out of the analysis of Dacey and Ross, for example, is the importance of the quantity μ/L^2 , familiar to TFT designers as a device figure of merit, where μ is the channel mobility and L is the channel length.

1.5 THE 1960s

The history of the TFT as everyone knows it today really began with the work of P. K. Weimer at RCA Laboratories in 1962 [10]. He used thin films of polycrys-

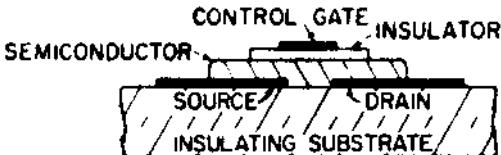


FIGURE 1.4 Schematic diagram of Weimer's top-gate staggered CdS TFT structure. (From Ref. 10.)

talline cadmium sulfide, similar to those developed for use in photodetectors, together with insulating films such as silicon monoxide, in what would now be called a staggered structure, with the source and drain contacts on the opposite side of the film from the gate. His structure is shown in Figure 1.4. On a glass substrate, source and drain electrodes are formed by evaporating gold through a shadow mask. The CdS film is next evaporated, also through a shadow mask, followed by SiO and finally a second gold evaporation for the gate.

Weimer achieved transconductances of 25,000 $\mu\text{A/V}$ for gate capacitance values of about 50 pF. These parameters would yield a nominal maximum oscillation frequency $g_m/2\pi C_G$ of 80 MHz, where g_m is the transconductance, and C_G is the gate capacitance, although his actual results were closer to 20 MHz.

His analysis of the behavior in the linear regime led him to the now familiar result that

$$\frac{g_m}{C_G} = \frac{\mu_d V_D}{L^2} \quad (1.1)$$

where μ_d is the drift mobility of the induced carriers and V_D is the drain voltage. Weimer's highest transconductances corresponded to mobilities of $140 \text{ cm}^2/\text{V-s}$.

The threshold behavior of Weimer's TFTs suggested a fairly large density of interface states that had to be filled before mobile charge could be induced (see Fig. 1.5). This density was estimated at $10^{12}\text{--}10^{13} \text{ cm}^{-3}$, although he reported that some units had much lower thresholds and therefore much lower interface state densities.

Shortly after Weimer's initial report, one of his colleagues, F. V. Shallcross [11], reported very similar results in TFTs made with CdSe. In 1964 Weimer [12] reported *p*-channel TFTs made with tellurium as the active material. These devices, which exhibited mobilities of about $200 \text{ cm}^2/\text{V-s}$, required very thin active layers ($\sim 150 \text{ \AA}$) to ensure enhancement mode operation, i.e., little or no current at $V_G = 0$. The Te work was motivated by a desire to provide the technology for complementary circuitry, important for low power dissipation.

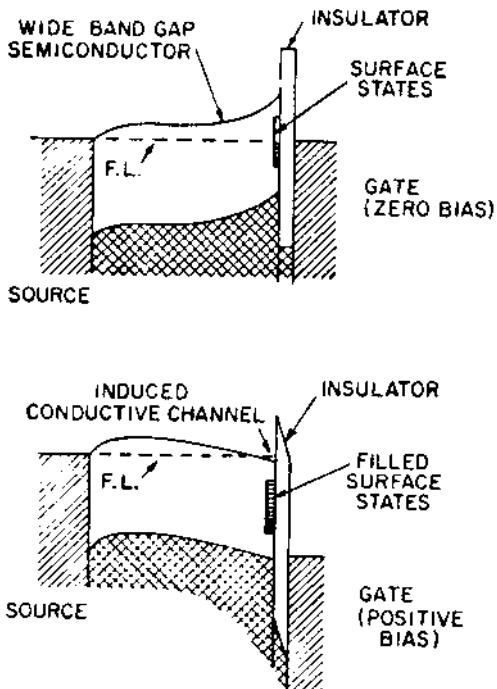


FIGURE 1.5 Band diagram of a TFT with and without bias, emphasizing the role of interface states. (From Ref. 10.)

On the theoretical side, Borkan and Weimer published in 1963 [13] their analysis of TFT characteristics. As mentioned earlier, this was based upon Shockley's analysis of the JFET, which is now known as the gradual channel approximation.

In the case of a TFT, the device is considered to vary in only one dimension, x , along the channel. The induced charge density $qn(x)$ is then given by

$$qn(x) = C_g (V_G - V_T - V(x)) \quad (1.2)$$

where C_g is the gate capacitance per unit area, V_T is the threshold voltage for conduction, and $V(x)$ is the channel voltage at x .

Assuming that the mobility of the induced carriers is a constant, equal to μ_d , the current I is given by

$$I = Wq\mu_d n(x) = \mu_d W C_g (V_G - V_T - V(x)) dV(x)/dx \quad (1.3)$$

Integrating this along the channel,

$$\int_0^L I dx = \mu_d WC_g \int_0^{V_D} [(V_G - V_T) - V] dV \quad (1.4)$$

So

$$IL = \mu_d WC_g \left[(V_G - V_T)V_D - \frac{V_D^2}{2} \right] \quad (1.5)$$

Thus,

$$I = \frac{\mu_d WC_g}{L} \left[(V_G - V_T)V_D - \frac{V_D^2}{2} \right] \quad (1.6)$$

$$I = \frac{\mu_d C_G}{L^2} \left[(V_G - V_T)V_D - \frac{V_D^2}{2} \right],$$

where $C_G (= LWC_g)$ is the total gate capacitance.

This simple result, which is plotted in [Figure 1.6](#), fits very well the experimental results, shown in [Figure 1.7](#). After almost 40 years, one can still design most TFT applications using this simple relation [Eq. (1.6)].

Of course, mobility is not constant, independent of gate voltage; the confinement of the induced carriers by the electric field generally causes the mobility to decline with increasing electric field. Also, Eq. (1.6) describes only the static characteristics.

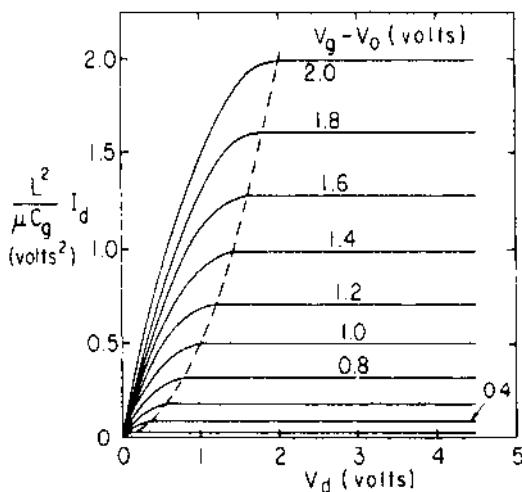


FIGURE 1.6 Theoretical variation of drain current versus drain voltage for various gate voltages. (From Ref. 13.)

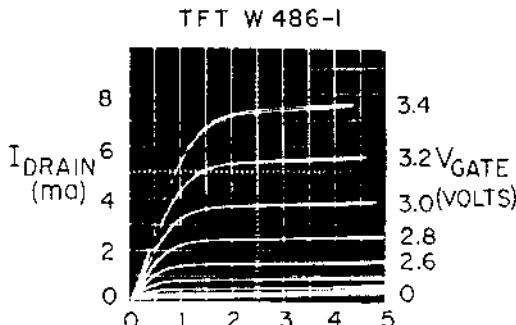


FIGURE 1.7 Experimental results for drain current versus drain voltage for various gate voltages, for a CdS TFT. (From Ref. 13.)

Traps in the semiconductor bulk or at the semiconductor–insulator interface can greatly affect the frequency response of the TFT when used as an amplifier, oscillator, or switch. R. R. Haering [14] has analyzed the frequency dependence of the transconductance in the presence of traps, showing that it depends upon the variation of mobility with gate voltage. The presence of traps also is manifested in the temperature dependence of g_m . Figure 1.8, from Miksic et al. [15], shows clearly several trap levels in a CdS TFT.

In addition to the effects of semiconductor and interface traps, traps in the gate insulator can cause slow instabilities, as charges tunnel into and out of the traps. Koelmans and DeGraaff [16] showed that, given an insulator trap as indicated schematically in Figure 1.9a, with associated population distribution, illustrated in Figure 1.9b, the amount of charge transferred is logarithmic with time. This was in good agreement with their observation on CdSe TFTs, where the change in drain current with time was found to be proportional to $\ln t$.

Through this period the motivation of most laboratories in pursuing TFT technology was that it would provide a basis for lower-performance logic at very low cost, relative to the cost and performance of circuitry based upon crystalline silicon. Glass is cheaper than silicon, and evaporated films use small volumes of material. However, with the emergence, starting in 1962, of the insulated-gate field-effect transistor [17] (IGFET) (see Fig. 1.10), now known as the metal oxide–semiconductor field-effect transistor (MOSFET), and with the emerging vision of ever more dense integrated circuit chips, this expectation of great cost savings was more and more difficult to sustain. Laboratory after laboratory in the late 1960s decided that the paths to both high-performance and low-cost logic went through crystalline silicon technology. This led to a decline in TFT development activity by the end of the 1960s.

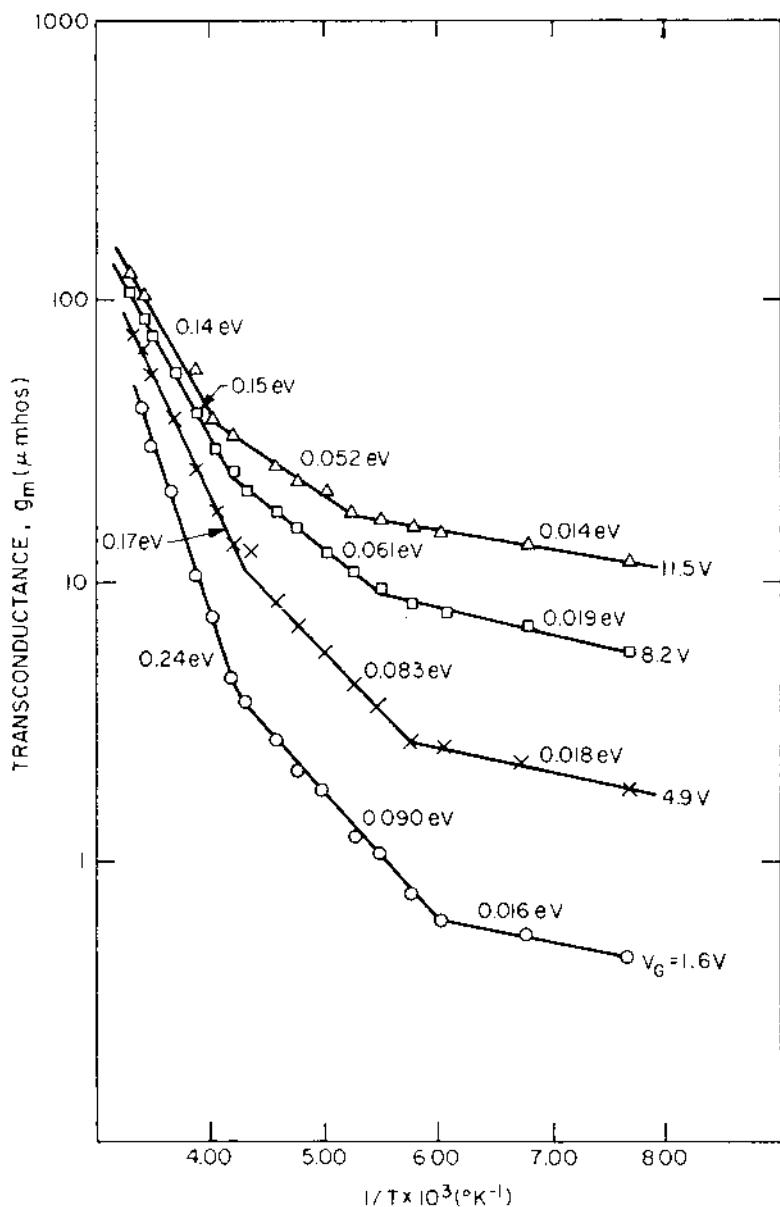
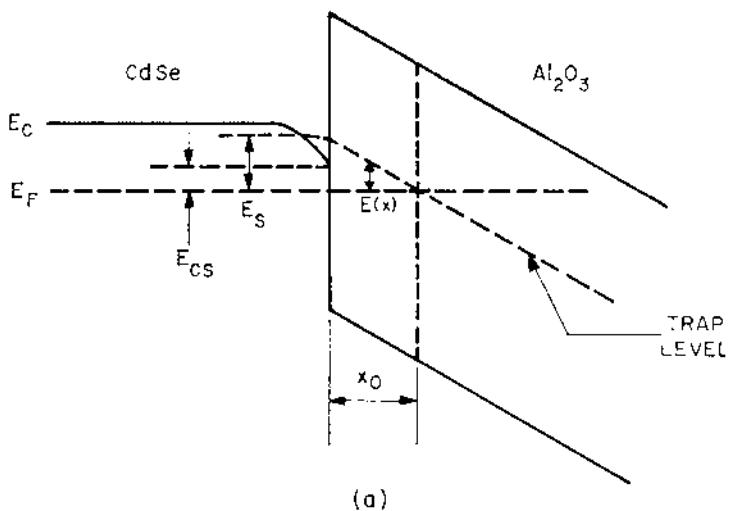
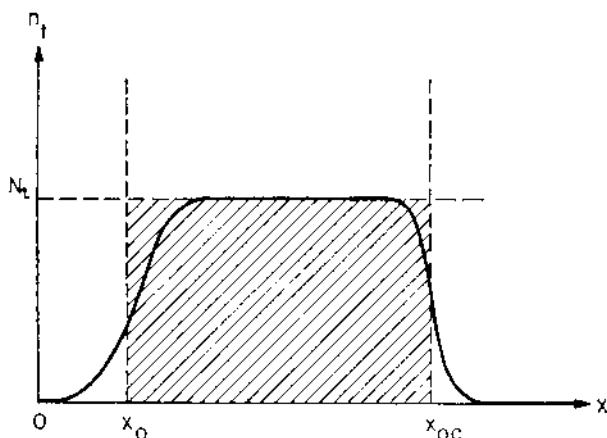


FIGURE 1.8 Temperature dependence of transconductance at various gate voltages, for a CdS TFT, showing multiple activation energies from traps. (From Ref. 15.)



(a)



(b)

FIGURE 1.9 Schematic band diagram (a) and trapped charge distribution (b) for a CdSe TFT with a single midgap trap in the insulator. (From Ref. 16.)

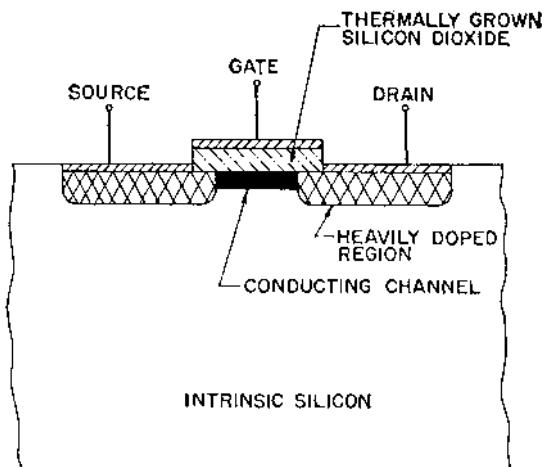


FIGURE 1.10 Schematic cross section of an insulated-gate field-effect transistor (IGFET) in crystalline silicon. (From Ref. 17.)

1.6 THE 1970s

What dramatically changed the prospects for TFTs in the 1970s was the realization that with crystalline silicon, low cost was inseparable from miniaturization, whereas some applications required large arrays of low-cost electronics. The paper that, in hindsight, heralded the golden opportunity (or, in today's terms, "killer application") for TFTs was published in 1971 by Lechner et al. [18]. Liquid crystal displays had been invented in the 1960s, and many people were trying to figure out how to exploit them in complex displays, including television displays. When disposed in matrixes with simple x - y electrodes, liquid crystals exhibited too much crosstalk; i.e., a change in one cell would be reflected by changes in other cells. Lechner and his coworkers realized that providing a nonlinear circuit element at every x - y intersection of the liquid crystal matrix would greatly improve the prospects of making displays with good image characteristics. They were remarkably creative in reviewing many possible technical approaches to improving the addressing of liquid crystal matrix displays. In fact, in subsequent years, nearly every one of their proposals was reduced to practice by someone.

Of most interest to us was the proposal by Lechner et al. to use, at every x - y intersection, a TFT plus a capacitor to store and hold a voltage on the liquid crystal in that cell (see Fig. 1.11).

According to T. P. Brody of Westinghouse Electric, he had already decided in 1968 that the use of TFTs to make high-performance electroluminescent matrix

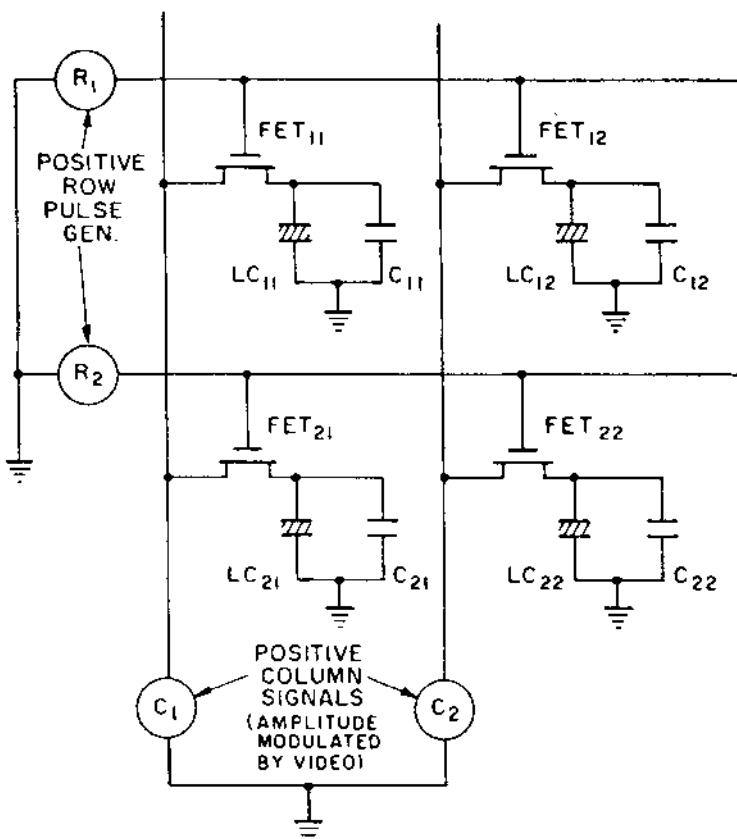


FIGURE 1.11 Electrical schematic of a portion of a thin-film transistor-addressed liquid crystal matrix display. (From Ref. 18.)

displays was an exciting opportunity. Electroluminescent matrix displays, like liquid crystal displays, suffered from crosstalk problems when addressed with simple x - y electrodes. By 1971, he and his group had received contracts to make both electroluminescent and liquid crystal displays using TFT arrays for addressing. By 1973 they had demonstrated a liquid crystal display with 120×120 picture elements in a $6'' \times 6''$ format [19] (see Fig. 1.12). At each intersection of the matrix was a CdSe TFT.

The characteristics of these TFT devices are described in Brody et al. [20]. With channel lengths of $50 \mu\text{m}$ and channel widths of $25 \mu\text{m}$, they exhibited transconductances of only $5\text{--}6 \mu\text{S}$ at 5 V (see Fig. 1.13). They state their mobility

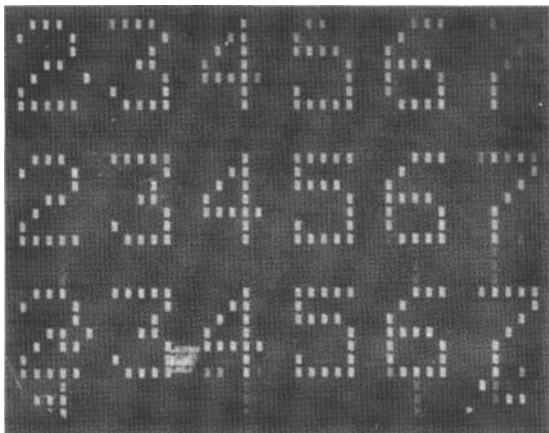


FIGURE 1.12 Photograph of the first TFT-addressed liquid crystal matrix display. (From Ref. 19.)

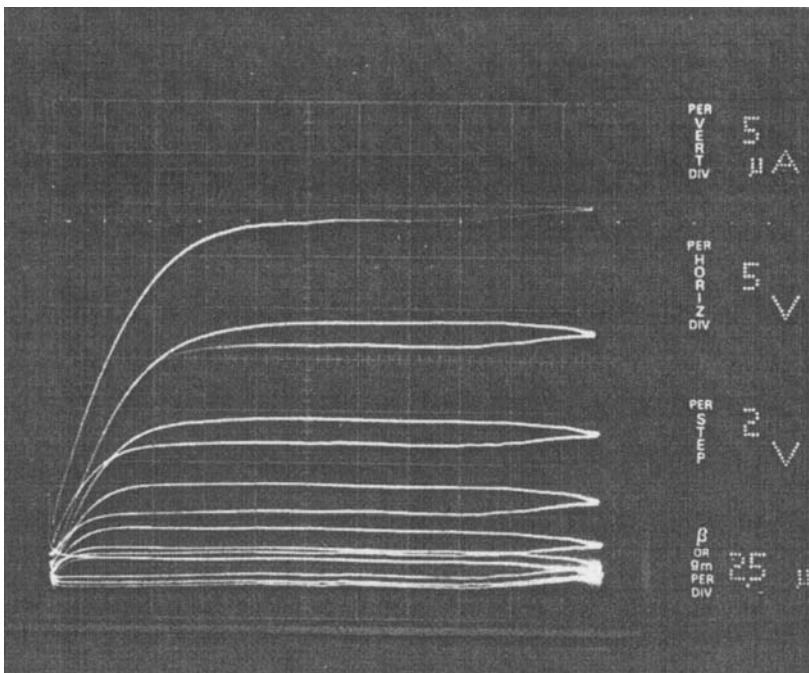


FIGURE 1.13 Source-drain characteristics of CdSe TFTs used in the first TFT/LC displays. (From Ref. 20.)

as $20 \text{ cm}^2/\text{V}\cdot\text{s}$. For the liquid crystal application, these had more than adequate conductance in the ON state, but the OFF currents were too large ($\sim 100 \text{ nA}$), necessitating the use of a storage capacitor at each pixel.

Brody and his group increased the resolution of their displays to 30 lines per inch in 1978 [21], but the smaller pixel capacitance that resulted dictated a reduction of OFF current to below 1 nA. This was achieved by a combination of annealing the TFTs at higher temperature and changing the channel length to $75 \mu\text{m}$. Their ON/OFF ratio, an important parameter for liquid crystal addressing applications, was still less than 10^5 .

By this time, the display applications of TFTs were motivating the work of most groups. As a result, efforts were increasingly focused on the issues of stability and ON/OFF ratio, as well as OFF current, or leakage. Stability was a serious issue. Even as late as 1975, Brody et al. [22] described how the circuits they employed for driving an electroluminescent display panel could tolerate threshold drifts of 6–8 V. As described by Lee et al. [23] in 1980, “TFTs have been notorious for their poor DC stability, which manifests itself as a slow decay of drain current when the device is operated with a steady gate voltage.”

While CdSe remained the principal active layer material for TFTs, there were other efforts. In 1975, Kramer[24] reported a thin-film electroluminescent display driven by PbS TFTs. Unfortunately, few details were provided concerning the TFT characteristics.

In 1979, however, a new material was introduced, with profound implications. LeComber, Spear, and Ghaith [25] described a TFT using amorphous silicon as the active material. It had previously been discovered that hydrogenated amorphous silicon, in contrast to pure amorphous silicon, could be doped with donors or acceptors to induce *n*- or *p*-type conductivity [26]. This suggested that the hydrogenation was passivating a large density of midgap states associated with dangling bonds in the silicon random network. The resulting crystal-like behavior led LeComber et al. to make a TFT, using glow-discharge Si_3N_4 as a dielectric and glow-discharge silicon as the active layer. Their TFT, which exhibited ON currents of several microamperes and OFF currents of about 1 nA (see Fig. 1.14), was recognized by them to fit criteria for driving liquid crystal displays, as published by Brody et al. [20]

In contrast to some great insights, which may initially be ignored, this result was immediately embraced. As was the case with Shockley in the 1940s, device physicists have a preference for elemental materials, and silicon was already known to have reproducible properties and to be amenable to large-area deposition. In particular, it was being explored for use in solar cells [27].

CdSe exhibits much higher mobilities than amorphous silicon, but CdSe is a polycrystalline compound; its properties are influenced by grain size, grain boundary interface states, stoichiometry, etc., and it can be sensitive to ambient

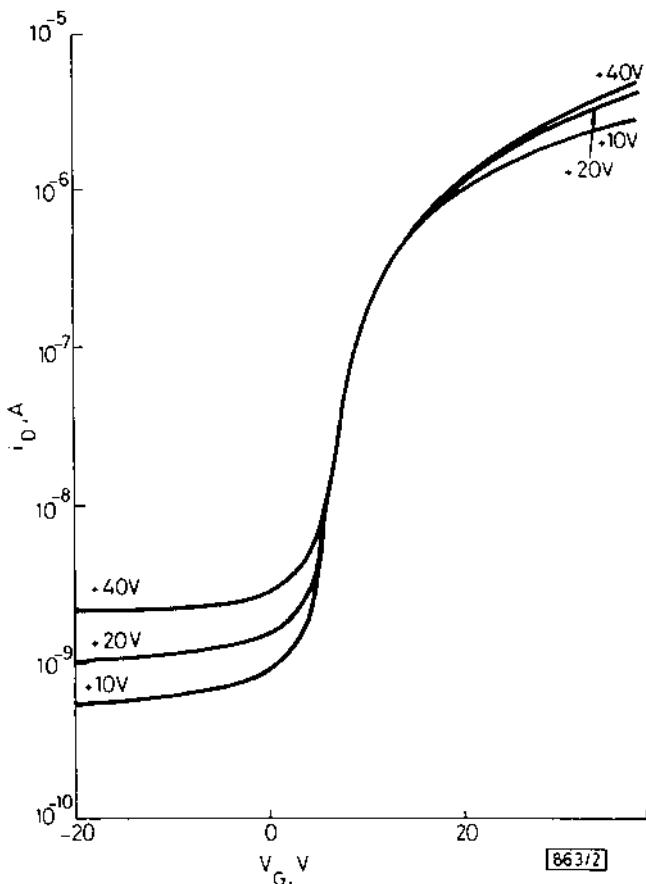


FIGURE 1.14 Log of drain current versus gate voltage (transfer characteristics) of the first a-Si TFTs, for various drain voltages. (From Ref. 25.)

gases such as H_2O and oxygen. Amorphous silicon has no grain boundaries and is self-passivating (against bulk changes).

While the debate as to which material was best suited for use in TFTs would continue for the next 20 years, economically, for the most important application, which was in liquid crystal displays, the issue was effectively decided in 1979 by the persuasiveness of the results of LeComber et al.

1.7 THE 1980s

Despite the excitement generated by the arrival of the a-Si TFT, significant improvements in CdSe TFTs emerged in 1980. M. J. Lee and coworkers at Imperial

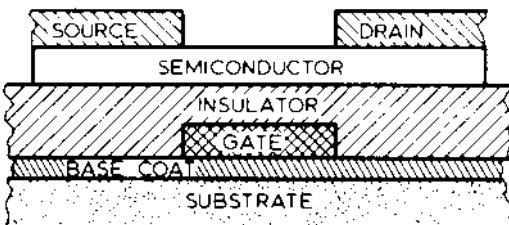


FIGURE 1.15 Schematic cross section of the inverted-staggered CdSe TFT structure used by Lee et al. (From ref. 23)

College reported [23] an impressive set of characteristics: mobility of $140 \text{ cm}^2/\text{V}\cdot\text{s}$, ON/OFF ratio up to 10^6 , OFF currents of less than 3 nA , and gate stability characterized as less than 10% change in drain current in 100 years of DC operation. Their device structure was of the inverted-staggered type, shown in Figure 1.15. The gate insulator was rf-sputtered SiO_2 , and chromium contacts were used. The films were annealed in N_2 at 380°C for 1.5 hr. Their devices had threshold voltages of about 2 V, and effects of fast traps in the CdSe were not noticeable on a scale of microseconds. The I-V curves fit very well to the gradual channel analysis, indicating a constant mobility and excellent saturation up to 12 V.

Also in 1980, F. C. Luo et al. [28] of Xerox reported a low-leakage CdSe TFT with OFF current at 0 V of only 2.5 pA . They used a double-gate structure to achieve this (see Fig. 1.16), with In/Au contacts and a combination of Al_2O_3 and SiO_2 for the gate insulators. The active layer was also less than 100 \AA thick. This TFT was engineered for use with liquid crystals as a pixel TFT. For example, the mobility was only about $18 \text{ cm}^2/\text{V}\cdot\text{s}$, apparently due to a trap density of more than 10^{18} cm^{-3} . Because the OFF state was achieved at $V_G = 0$, the device in

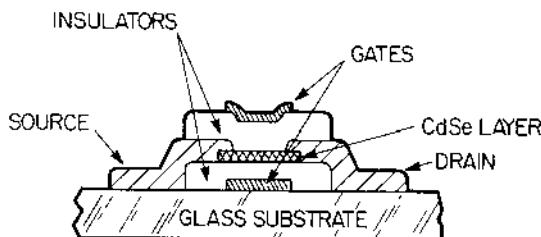


FIGURE 1.16 Schematic cross section of the double-gate structure used by Luo et al. to achieve low-leakage currents in CdSe TFTs. (From Ref. 28.)

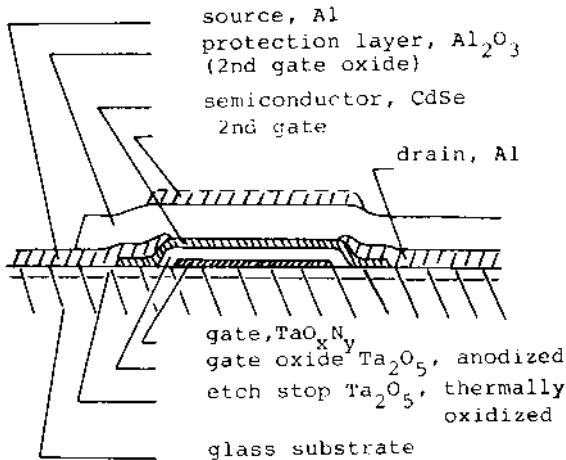


FIGURE 1.17 Schematic cross section of double-gate self-aligned structure for CdSe TFTs used by Lueder and coworkers. (From Ref. 30.)

use in a TFT/liquid crystal (TFT/LC) display is very stable. A display life of 10^4 hr was projected, assuming a duty cycle of 1/850.

Lueder and his coworkers in 1979–81 [29–31] introduced a new approach to TFT fabrication using photolithography instead of shadow masks. They also introduced anodic Ta_2O_5 as a gate insulator material in a double-gate structure, shown in Figure 1.17. The use of the anodic oxide as a self-aligned, pinhole-free insulator became very popular later in the 1980s in a-Si TFTs, where it was usually used in conjunction with a second plasma-deposited layer. Their devices, like Luo's, were optimized for the liquid crystal application and had similar characteristics. Their use of photolithography also included a process for making source–drain contacts that are self-aligned to the gate. This feature can reduce pixel-charging errors due to gate–source parasitic capacitance.

The year 1980 saw the introduction as well of the polysilicon TFT, in a report by Depp et al. [32] of IBM. They used chemical vapor-deposited polysilicon to achieve good mobility and TFT characteristics (see Fig. 1.18). With mobilities around $50 \text{ cm}^2/\text{V}\cdot\text{s}$, they obtained ring oscillators with $2\text{-}\mu\text{s}$ delay per stage. These were high-temperature polySi TFTs, employing as gate insulator SiO_2 grown thermally at 1050°C . This approach requires a high-temperature substrate such as quartz; glass cannot be used.

By 1982, both the IBM group [33] and Nishimura et al. [34] of Mitsubishi were using laser recrystallization of polySi to improve mobilities and lower threshold voltages, achieving values as high as $400 \text{ cm}^2/\text{V}\cdot\text{s}$ for electron mobility.

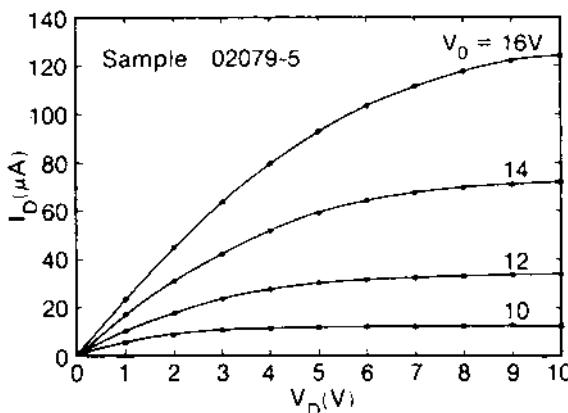


FIGURE 1.18 Source-drain characteristics of the first polysilicon TFTs. (From Ref. 32.)

The motivation for pushing up the mobility was to be able to integrate drive circuitry as well as providing pixel TFTs.

That same year saw reports of TFT/LC displays employing a-Si as well as tellurium. The Te-based displays, by Matsuura et al. [35] of Sharp Corporation, are shown in Figure 1.19. Their characteristics, shown in Figure 1.20, were suitable only for low-content displays, because of their high OFF current. They did, however, exhibit a desirable insensitivity to light, as shown.

The a-Si TFT/LC report from Okubo et al. [36] of Canon showed TFT characteristics with an ON/OFF ratio of more than 10^6 (see Fig. 1.21) and mobility of $0.3 \text{ cm}^2\text{V}\cdot\text{s}$. These were shown to be suitable for driving their 240×240 arrays. Kawai et al. [37] of Fujitsu also reported an a-Si-based TFT/LC display

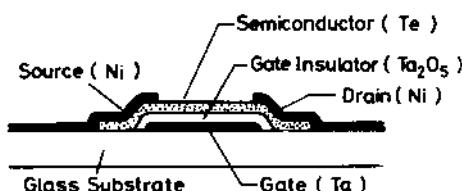


FIGURE 1.19 Schematic cross section of an inverted-staggered Te TFT. (From Ref. 35.)

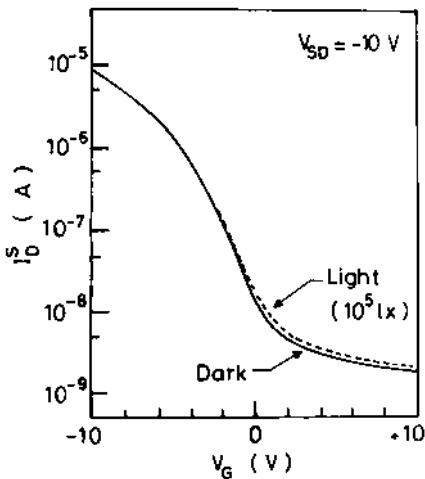


FIGURE 1.20 Transfer characteristics of Te TFTs, showing insensitivity to illumination. (From Ref. 35.)

of low content. Their TFTs were not quite as good in ON/OFF ratio, but they included a light shield (see Fig. 1.22), since a-Si has considerable photoconductivity and the display application involves bright backlighting.

In 1983 the Fujitsu group described a new self-aligned a-Si structure [38], using the approach introduced by Lueder's group for CdSe. Their ON/OFF characteristics were greatly improved ($>10^8$) (see Fig. 1.23), partly due to a 300°C anneal. At the same conference, Suzuki et al. [39] of Toshiba presented results for 220×240 pixel arrays using a-Si with ON/OFF ratios of 5×10^6 , V_T of 3 V, and mobility of $0.3 \text{ cm}^2/\text{V}\cdot\text{s}$. The Suzuki TFTs were of the back-channel cut type. That is, contacts were made by depositing doped n^+ a-Si on top of undoped a-Si in situ. After forming metal source and drain, the n^+ layer is etched off between source and drain (see Fig. 1.24).

On the poly-Si front, Morozumi et al. [40] of Suwa Seiko reported TFTs with excellent switching characteristics (see Fig. 1.25) achieved by the use of a dual-gate approach (see Fig. 1.26). These were formed on quartz wafers using high-temperature processing. This approach yields excellent TFT stability, as in MOSFET technology, but substrate cost is quite high compared to glass. In 1984 Oana [41] of Toshiba described a process for making poly-Si TFTs on glass (see Fig. 1.27), but the OFF currents of 100 pA and ON/OFF ratio of 10^5 (see Fig. 1.28) are not adequate for high-content LC display application.

The company most notably pursuing CdSe TFTs for display application in this period was Panelvision. In a 1985 paper, Luo et al. [42] described a 640×400

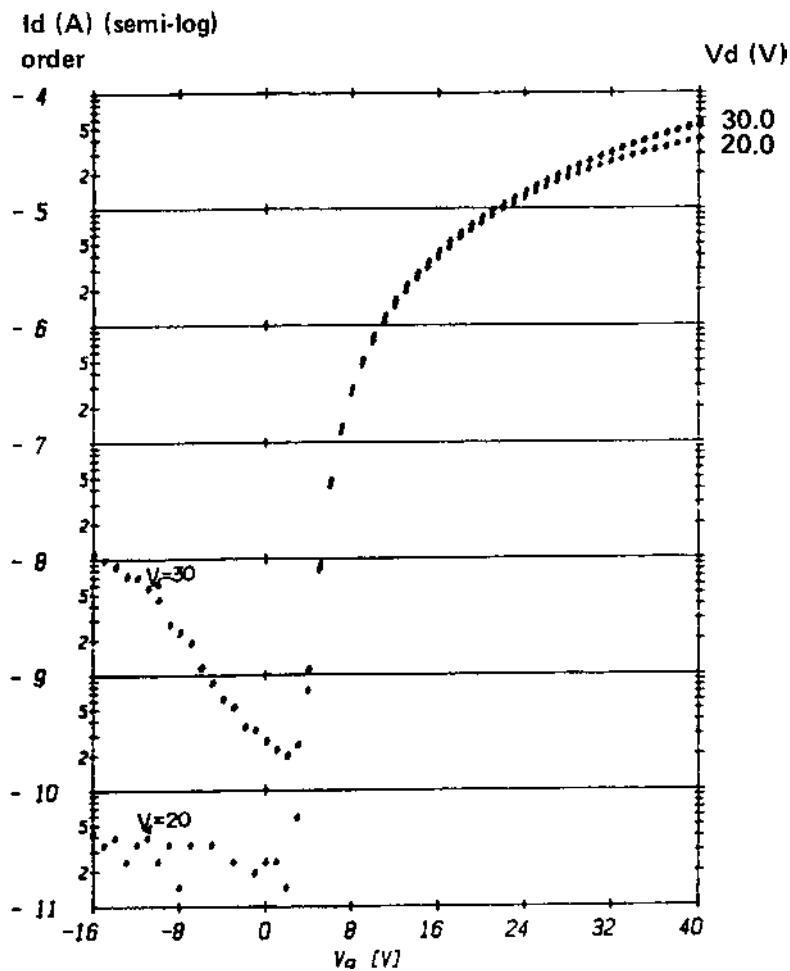


FIGURE 1.21 Transfer characteristics of an early a-Si TFT for liquid crystal display application, for two different drain voltages. (From Ref. 36.)

TFT array of TFTs used to make a display. The TFTs were photolithographically produced, but their characteristics ($I_{ON} \sim 1 \mu\text{A}$; $I_{OFF} \sim 100 \text{ pA}$) were not adequate for good grayscale rendition.

The following year there were two notable reports of a-Si TFT arrays for use in pocket television sets. Funada et al. [43] of Sharp used a trilayer inverted-staggered structure in which a back-channel insulating layer is deposited by the

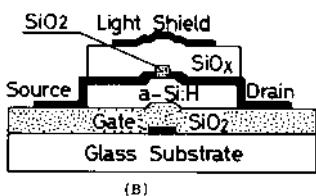
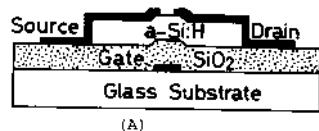


FIGURE 1.22 Schematic cross section of a conventional TFT structure (a) and an improved structure incorporating a back-channel passivation layer and a light shield. (From Ref. 37.)

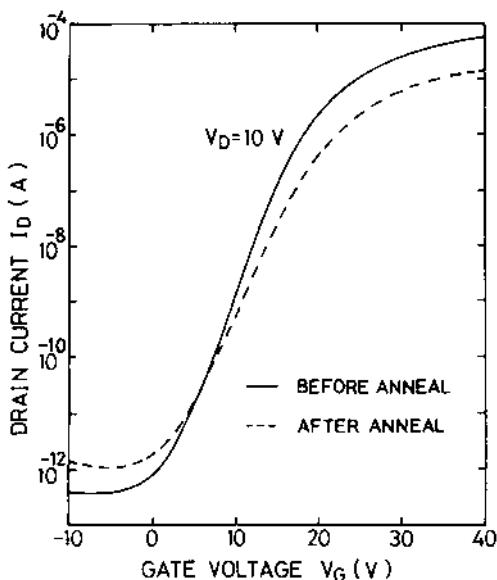


FIGURE 1.23 Transfer characteristics of an a-Si TFT with high ON/OFF ratio, increased by annealing. (From Ref. 38.)

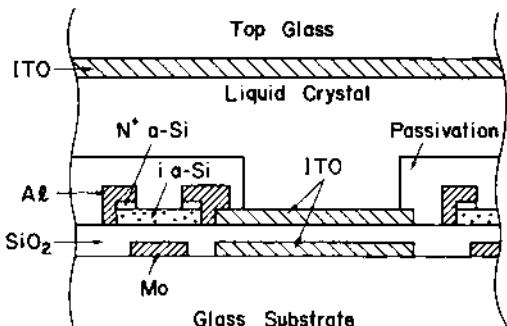


FIGURE 1.24 Schematic cross section of an inverted-staggered back-channel cut a-Si TFT. (From Ref. 39.)

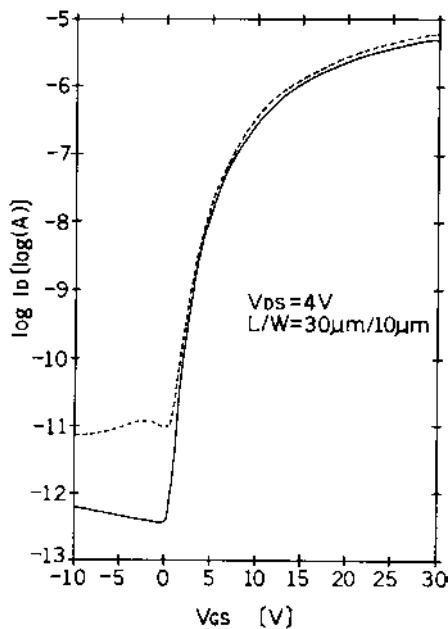


FIGURE 1.25 Transfer characteristics of a double-gate low-leakage poly-Si TFT. (From Ref. 40.)

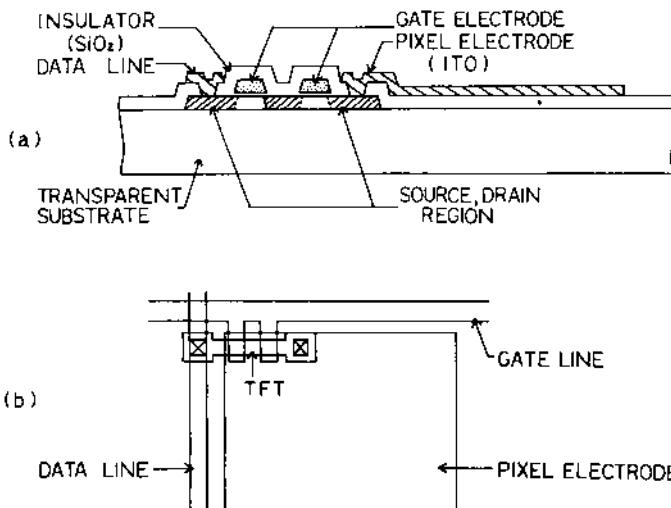


FIGURE 1.26 Schematic cross section (a) and layout (b) of a double-gate low-leakage poly-Si TFT. (From Ref. 40.)

same plasma-enhanced chemical vapor deposition (PECVD) technique used to deposit the active layer (see Fig. 1.29). They reported a mobility of $0.3 \text{ cm}^2/\text{V}\cdot\text{s}$ and ON/OFF ratio greater than 10^6 . Hotta et al. [44] of Matsushita also reported greater than 10^6 ON/OFF ratio and a mobility of $0.9 \text{ cm}^2/\text{V}\cdot\text{s}$ using the back-channel cut described earlier, where the contact layer is deposited in situ. At this stage in a-Si TFT development, it became clear that it was easier to make a good contact with the back-channel cut approach, but it was easier to control OFF current (back-channel leakage) with the trilayer approach. The best way to imple-

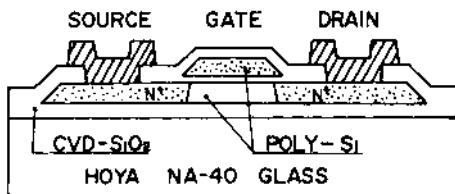


FIGURE 1.27 Schematic cross section of a poly-Si gate, low-temperature poly-Si TFT on glass. (From Ref. 41.)

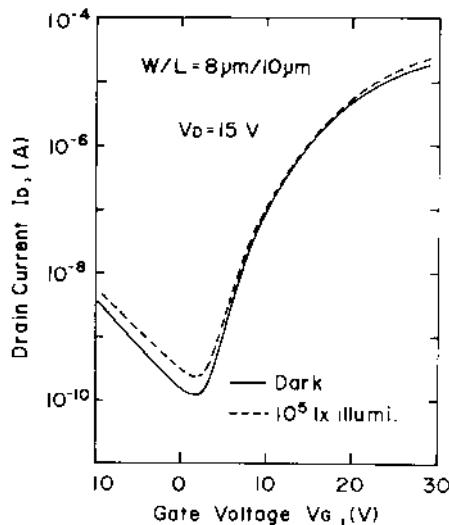


FIGURE 1.28 Transfer characteristics of the low-temperature poly-Si TFT shown in Fig. 1.27. (From Ref. 41.)

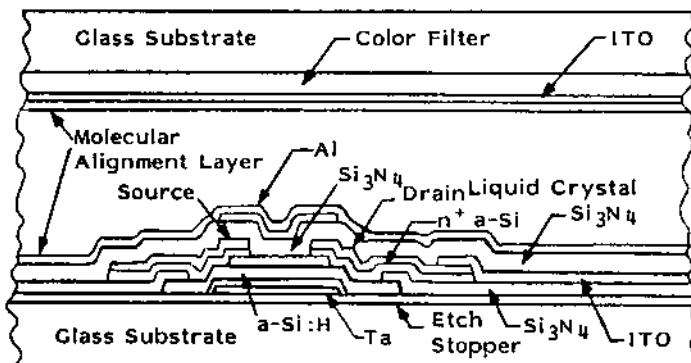


FIGURE 1.29 Schematic cross section of an a-Si TFT employing a plasma nitride/a-Si/plasma nitride trilayer structure. (From Ref. 43.)

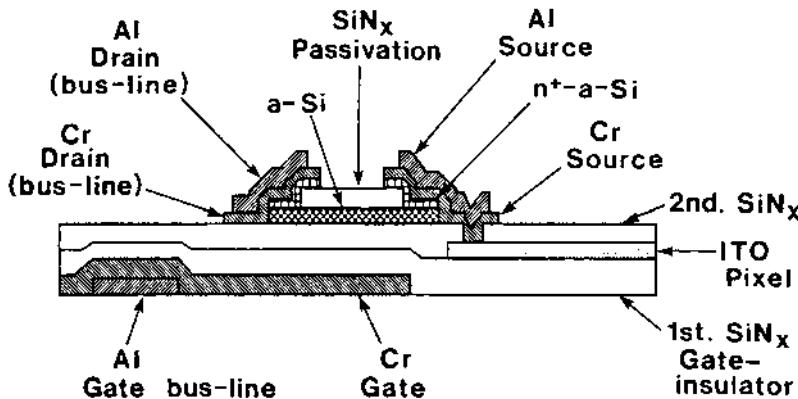


FIGURE 1.30 Schematic cross section of an a-Si TFT of the “etch-stopper,” or in situ trilayer, type. (From Ref. 45.)

ment the trilayer approach is to deposit the two insulator layers and the active layer in situ, for minimum contamination of the interfaces. This was done by Moriyama et al. [45] of NEC, among others (see Fig. 1.30).

On the CdSe front, Vanfleteren and Van Calster[46] in the mid-1980s described a process for making TFTs that they claimed combined the electrical characteristics of single-pump-down structures using shadow masks with the precision of photolithographically patterned structures. According to them, photolithography normally leads to contamination, either from residues or from sputter cleaning. In their structure, shown in Figure 1.31, the CdSe layer, which is doped

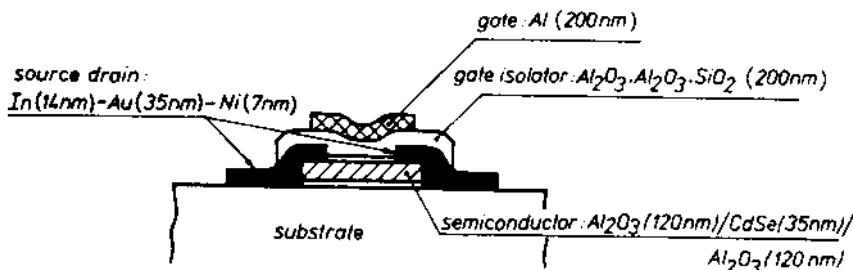


FIGURE 1.31 Schematic cross section of a trilayer CdSe TFT with both interfaces formed in situ. (From Ref. 46.)

with Zn, is sandwiched between two Al_2O_3 layers in a single pump-down liftoff deposition, thereby controlling the critical interfaces as in the trilayer a-Si TFTs. Following that, the top insulator is etched back to allow for In/Au/Ni contacts. Then a gate insulator and gate are applied, resulting in a top-gate, coplanar configuration. The trouble is that for LC applications, the OFF current of 5 nA and ON/OFF ratio of 3×10^3 are not sufficient, even though the mobility of $50 \text{ cm}^2/\text{V}\cdot\text{s}$ ensures fast switching ($<200 \text{ ns}$).

Pursuing low-temperature poly-Si, Morozumi et al. [47] were able to produce both low OFF currents ($<0.1 \text{ pA}$) and high ON/OFF ratios ($>10^7$), but this was accomplished by using their double-gate structure and thin, fine-grained films with low mobility ($\sim 2\text{--}3 \text{ cm}^2/\text{V}\cdot\text{s}$), thus negating the benefits of poly-Si for integrating fast driver circuits.

The first TFTs with low OFF current and high ON/OFF ratio without sacrificing mobility were achieved by Spachmann et al. [48] of the University of Stuttgart group, using CdSe. Their numbers were $<1 \text{ pA}$, $\text{ON}/\text{OFF} > 10^8$, and $\mu = 102 \text{ cm}^2/\text{V}\cdot\text{s}$ (see Fig. 1.32). Their TFTs were photolithographically patterned inverted-staggered type (bottom gate, top contacts), and the characteristics were obtained only after several anneal cycles, sputter-cleaning of the Ta_2O_5 gate insulator surface prior to CdSe deposition, and e-beam deposition of an Al_2O_3 passivation layer. Even so, the threshold is greater than 10 V, suggesting a high density of interface states. Also, the channel length was $30 \mu\text{m}$, so the quantity

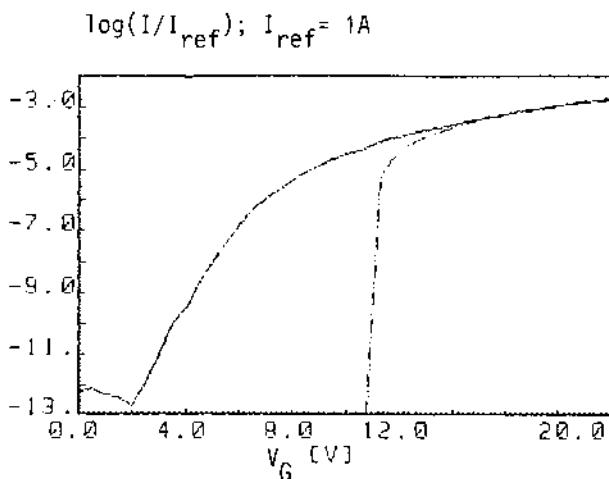


FIGURE 1.32 Transfer characteristics of a high-ON/OFF-ratio CdSe TFT (the dashed curve is theoretical). (From Ref. 48.)

μ/L^2 is not much better than for many of the a-Si TFTs being reported in this period.

By the end of the 1980s, many companies had mastered the art of making good a-Si TFTs, that is, devices with good OFF currents (<1 pA), good ON/OFF ratios ($>10^7$), reasonable mobilities ($0.5\text{--}1.0\text{ cm}^2/\text{V}\cdot\text{s}$), and good stability. Emphasis had shifted to array-performance issues such as gate-line conductivity and manufacturing issues such as the number of mask levels required for a process. In the gate metallurgy area, Ta, which was used for its good anodic oxide but which was rather resistive, gave way to more conductive systems, such as Al/Cr-layered gates [45] and Mo-Ta alloy gates[49], leading eventually to aluminum alloy gates.

1.8 THE 1990s

High-temperature poly-Si TFTs can meet all of the requirements for driving liquid crystals, including the formation of integrated drive circuits. In 1990 Stupp et al. [50] of Philips reported devices that had OFF currents of 0.1 pA, ON/OFF ratio of 10^{10} , and electron mobility μ_n of $35\text{ cm}^2/\text{V}\cdot\text{s}$ (see Fig. 1.33). These impressive

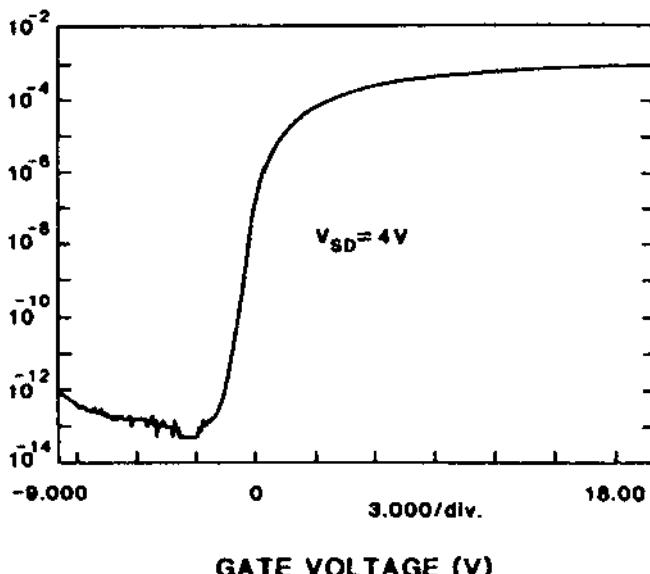


FIGURE 1.33 Transfer characteristics of a high-ON/OFF-ratio high-temperature poly-Si TFT. (From Ref. 50.)

results were achieved by recrystallizing amorphized deposited poly-Si to form the active layer in top-gate devices, which were then hydrogenated. The hydrogenation both lowered the OFF current and increased the ON current. After these results, no one doubted the utility of high-temperature poly-Si TFTs for liquid crystal displays. Indeed, they are still used today for viewfinders and entertainment headsets. Unfortunately, the high cost associated with using quartz substrates and high-temperature processing makes them uneconomical for large direct-view displays.

It did not take long for low-temperature poly-Si TFTs to emerge with characteristics almost as good as those of their high-temperature cousins. In 1991 Little et al. [51] of Seiko-Epson showed results from TFTs with OFF currents of 0.1 pA, ON/OFF ratio of more than 3×10^8 , and mobility of more than $20 \text{ cm}^2/\text{V}\cdot\text{s}$ (see Fig. 1.34). They achieved this by using solid-phase crystallization at 600°C of a-Si deposited at 550°C . They also used both electron cyclotron resonance (ECR) deposition of SiO_2 as well as atmospheric-pressure CVD

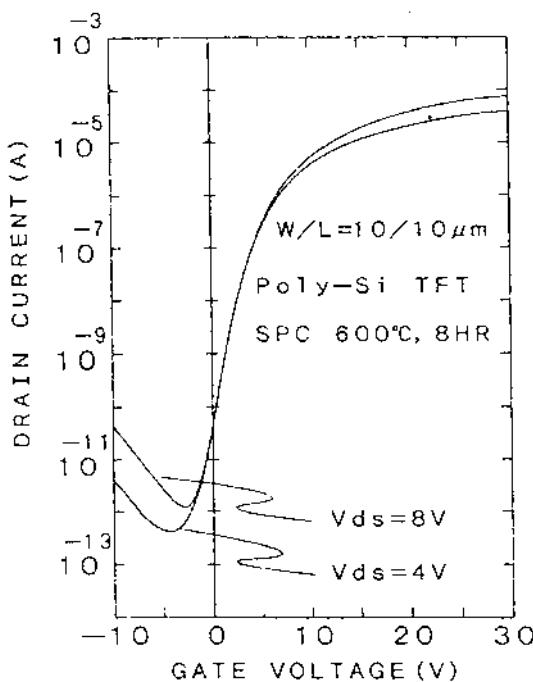


FIGURE 1.34 Transfer characteristics of a high-ON/OFF-ratio low-temperature poly-Si TFT. (From Ref. 51.)

(APCVD) of SiO_2 to form the gate insulators. Since there are numerous glasses that can withstand heating at these temperatures, this technology can be used for large-area direct-view displays, especially if it is judged important to integrate the peripheral drive circuitry. With performance no longer an issue, the decision as to whether to use a-Si TFTs with attached drive circuitry or low-temperature poly-Si (LTPS) TFTs with integrated drive circuitry has become an economic one. In this arena, LTPS has struggled, with little success, against an increasingly powerful a-Si juggernaut that has captured most of the market for liquid crystal displays. Not all displays are liquid crystal, however, and new technologies with different circuit requirements can tip the economic balance. Organic light-emitting diodes, for example, require current sources, and LTPS TFTs can easily deliver at least an order of magnitude more current for the same-size device.

Returning to the prototypical CdSe TFTs, these seem to have passed a high watermark of sorts in 1993, when the last international workshop on the subject was held in Strasbourg, France. At that meeting, M. J. Lee et al. [52] were able to report TFTs with mobilities of more than $250 \text{ cm}^2/\text{V}\cdot\text{s}$ and circuit speeds of 140 MHz in a ring oscillator configuration. Dobler et al. [53] described devices with mobilities close to $400 \text{ cm}^2/\text{V}\cdot\text{s}$ (see Fig. 1.35), which they used to make LC displays with good characteristics. The workshop also included contributions

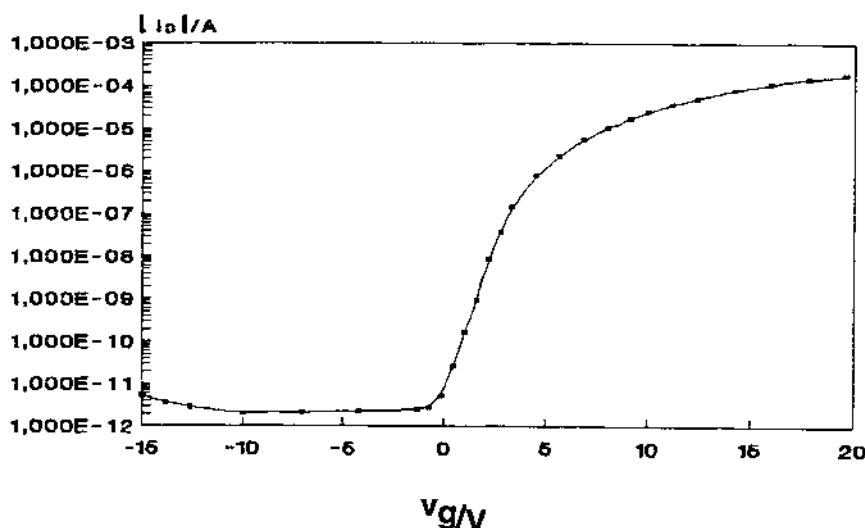


FIGURE 1.35 Transfer characteristics of a high-mobility ($>300 \text{ cm}^2/\text{V}\cdot\text{s}$) CdSe TFT. (From Ref. 53.)

from Litton Systems Canada (which had taken over Panelvision), describing their attempt to introduce a display product using CdSe TFTs.

The year 1990 marked the debut of a new class of TFT, based upon organic semiconductor active layer material. Garnier [54] reported TFTs using evaporated hexathiophene as active material, claiming mobilities comparable to those of a-Si. Since then, many others have taken up this lead, and organic TFTs are being pursued as candidates for integration onto flexible plastic substrates for a future generation of rugged, lightweight displays that can be rolled up like a map. The development and status of these organic TFTs have recently been reviewed by Dimitrakopoulos and Mascaro [55].

1.9 SUMMARY AND COMMENTS

In the more than six decades since their conception, thin-film transistors have undergone extensive evolution, development, and refinement. As their intended uses went from switching systems to low-cost computer logic to flat panel display addressing, new materials, structures, and fabrication techniques were introduced. CdS and CdSe gave way to a-Si as the most widely used active layer material, while poly-Si is increasingly pursued as a “next-generation” TFT technology. Still, of all the TFT materials, none has come close to attracting the investment associated with a-Si. This is more a matter of economics than physics, since only a-Si has reached the point where almost anyone can set up equipment and quickly achieve predictable performance characteristics, using a relatively small number of process steps. a-Si is similar to crystalline silicon in this respect. Poly-Si and CdSe devices are much more sensitive to details of film preparation and processing, so much so that one seldom sees results from two sources that are essentially indistinguishable.

Reproducibility is an issue that perhaps can be overcome, but there is another dilemma that bedevils polycrystalline TFTs. For high performance, one wants both high mobility, which is associated with large grain size, and short channel length. The number of grains in a channel length becomes small but still uncertain. The consequence of going down this path is increasing variation from transistor to transistor, often to unacceptable levels in terms of display uniformity and power dissipation (greater variations require higher-logic voltages). Considering these issues, it seems likely that the dominance of a-Si will only yield to an economical process for producing good single crystal silicon on glass (or plastic).

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2

Preparation and Properties of Hydrogenated Amorphous Silicon Thin-Film Transistors

Jin Jang

Kyung Hee University, Seoul, Korea

2.1 INTRODUCTION TO THE HYDROGENATED AMORPHOUS SILICON THIN-FILM TRANSISTOR

This chapter deals with the preparation and properties of hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs). Here we compare and contrast the electrical characteristics of a number of popular TFT structures and shed light on the most important aspects of the plasma processes used to deposit the critical semiconducting and insulating layers in these devices. Figure 2.1 depicts a number of thin-film transistor structures according to the position of the active layer, gate insulator, and source/drain electrodes. A staggered TFT has the gate and source/drain electrodes on opposite sides of the semiconductor, whereas a coplanar TFT has the gate and source/drain electrodes on the same side of the semiconductor. Fabrication of a typical top-gate staggered TFT starts with the formation of the source/drain electrodes on glass. In order to form a low-resistance contact, a suitable doping scheme must be used, which may include plasma doping or n^+ a-Si:H deposition; in the latter case, the n^+ a-Si:H on the source/drain metal must be patterned before the intrinsic (i-) a-Si:H deposition. During this process

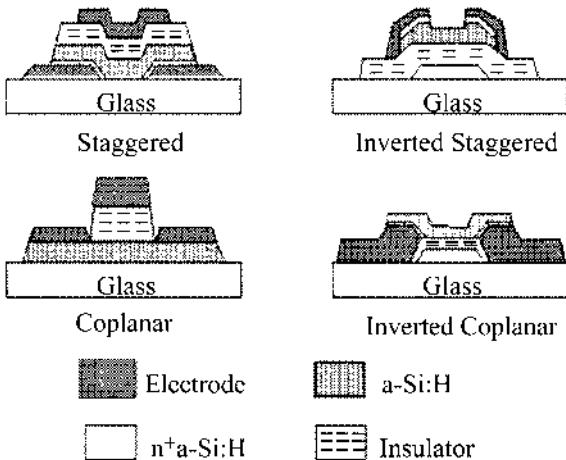


FIGURE 2.1 A few of the most popular a-Si:H TFT structures.

the n^+ a-Si:H layer is exposed to the air, so care must be taken at this step to remove any oxide that might form between the n^+ and i a-Si:H. Following the n^+ a-Si:H is patterned, intrinsic a-Si:H and SiN_x gate insulator are deposited sequentially in a PECVD chamber, and the gate electrode is formed on the SiN_x . Since the nitride layer is deposited after the a-Si:H in this configuration, care must be taken to control the plasma power during the nitride deposition to avoid damaging the a-Si:H close to the interface where the accumulated electron channel will be formed during device operation.

In a coplanar TFT, the intrinsic a-Si:H, SiN_x , and source/drain contact are on the same side of the semiconductor. As with the top-gate staggered TFT, the SiN_x is deposited on the a-Si:H in a standard top-gate process flow; therefore the plasma damage to the a-Si:H during SiN_x deposition should be minimized. In a coplanar a-Si:H TFT, special attention has to be made to minimize any offset between the edge of the gate and the source/drain electrodes; otherwise a high series resistance forms at the contact in the offset region.

In an inverted-staggered a-Si:H TFT the gate is first formed on the substrate, and gate insulator, a-Si:H, and source/drain are deposited sequentially. Therefore, the gate and source/drain are once again on the opposite side of a semiconductor. This structure is also referred to as a bottom-gate TFT. The inverted-staggered TFT, widely used in the manufacturing of active-matrix LCD panels, is commonly fabricated as one of two popular structures: the back-channel-etched (BCE) structure or the etch-stopper (ES) structure. Many LCD companies either are currently

using or are moving toward using the BCE a-Si:H TFT because of its simpler manufacturing process flow compared with the ES a-Si:H TFT.

2.2 SIMPLE CHARACTERIZATION OF A HYDROGENATED AMORPHOUS SILICON THIN-FILM TRANSISTOR

As with the MOSFET (metal oxide–semiconductor field-effect transistor) and the JFET (junction field-effect transistor), there are two operational regimes: the linear region and the saturation region. In the linear region the drain current increases linearly with drain voltage ($V_D \ll V_G$), as in ohmic conduction. On the other hand, the drain current is constant with increasing drain voltage in the saturated region.

2.2.1 Linear Region

A gradual channel approximation is assumed in the channel of the TFT, where x is the direction perpendicular to the channel and y is parallel to the channel, and the carrier density per unit area in the channel depends on y (see Fig. 2.2). The carrier density per unit area in the channel depends on the potential $V(y)$ caused by the drain potential V_D [1].

When the gate potential is higher than the threshold voltage, V_{TH} , the mobile charge Q_I in the channel is related to the gate potential V_G via [2]

$$Q_I = - C_{SiN_x}(V_G - V_{TH}) \quad (2.1)$$

where C_{SiN_x} is the capacitance per unit area of the SiN_x gate insulator. In Eq.

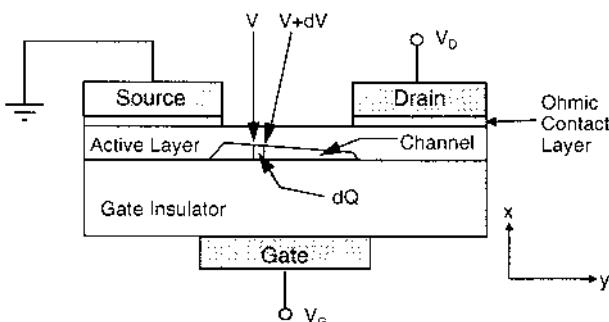


FIGURE 2.2 Cross-sectional view of the channel region of a TFT used to derive the gradual channel approximation.

(2.1) the channel potential V is assumed to be zero; however, the induced charge Q_I is a function of y , so Eq. (2.1) is replaced by the following equation:

$$Q_I = - C_{\text{SiN}_x} (V_G - V_{\text{TH}} - V) \quad (2.2)$$

On the other hand, the current induced by majority carriers can be written as

$$I_D = W \mu_n Q_I E_y \quad (2.3)$$

where W is channel width, μ_n is the electron mobility, and E_y is the electric field at y . The equation is a simplified form of the current density formula where the diffusion term has been taken to be negligible:

$$J_n = \frac{I_n}{A} = q \left(\mu_n n E + D_n \frac{dn}{dx} \right) \quad (2.4)$$

By substituting $E_y = - dV/dy$ and Eq. (2.2) into Eq. (2.3) we obtain

$$I_D dy = W \mu_n C_{\text{SiN}_x} (V_G - V_{\text{TH}} - V) dV \quad (2.5)$$

By integration of the current increment from $y = 0$ to L , that is, from $V = 0$ to V_D , we obtain the gradual channel expression for the drain current:

$$I_D = C_{\text{SiN}_x} \mu_n \frac{W}{L} \left[(V_G - V_{\text{TH}}) V_D - \frac{1}{2} V_D^2 \right] \quad (2.6)$$

In the linear region ($V_D \ll V_G$) the drain current can be written as

$$I_D = C_{\text{SiN}_x} \mu_n \frac{W}{L} (V_G - V_{\text{TH}}) V_D \quad (2.7)$$

The field-effect mobility in the linear region is obtained using Eq. (2.7) [2].

2.2.2 Saturation Region

The gate field-induced carrier density at the drain disappears as the drain potential increases. Eventually, when $V_D = V_G - V_{\text{TH}}$, the electron channel becomes completely pinched off, and the drain current saturates. For $V_D > V_G - V_{\text{TH}}$, Eq. (2.6) is no longer valid. The saturation drain current can be obtained by substitution of $V_D = V_G - V_{\text{TH}}$ into Eq. (2.6) [3], yielding

$$I_D = \frac{C_{\text{SiN}_x} \mu_n W}{2L} (V_G - V_{\text{TH}})^2 \quad (2.8)$$

The field-effect mobility in the saturation region is obtained from Eq. (2.8). Deviations from the simple gradual channel approximation are often related to contact resistance effects and gate-voltage-dependent mobility. In general, extraction of the field-effect mobility from the saturation characteristics of an a-Si TFT

leads to a higher value than extraction in the linear region, particularly as channel lengths become shorter.

Figures 2.3 and 2.4 show, respectively, the transfer and output characteristics of an a-Si:H TFT. The on/off drain-current ratio is important, because these TFTs form the active switches in an active-matrix liquid crystal display (AMLCD), where the on-current determines the rate of pixel charging and the off-current is associated with the leakage of the pixel voltage. As shown in Fig. 2.3, the on/off drain current ratio at $V_D = 10$ V is greater than 10^7 . Figure 2.4 indicates good contact performance at low drain voltages; high-resistance contacts exhibit “current crowding” close to the origin of the output plot due to large potential drops at the contacts, an effect that is absent in Fig. 2.4.

The a-Si:H TFT characteristics shown in this section are derived from TFTs fabricated at Kyung Hee University by means of the following procedure. First, Cr metal was deposited by RF sputtering and patterned to form the gate electrodes. Next, silicon nitride, a-Si:H, and n^+ a-Si:H were deposited sequentially by plasma-enhanced chemical vapor deposition (PECVD). Thicknesses for the SiN_x , a-Si:H, and n^+ a-Si:H layers were 350, 150, and 50 nm, respectively. Next, an active island was formed and source/drain metal was deposited and patterned for source/drain contacts. In the final step, the n^+ layer between the source/drain was etched away, completing the bottom-gate BCE TFT.

There are several methods to get the field-effect mobility and the threshold voltage from the characteristics of an a-Si:H TFT. Figures 2.5 through 2.7 show

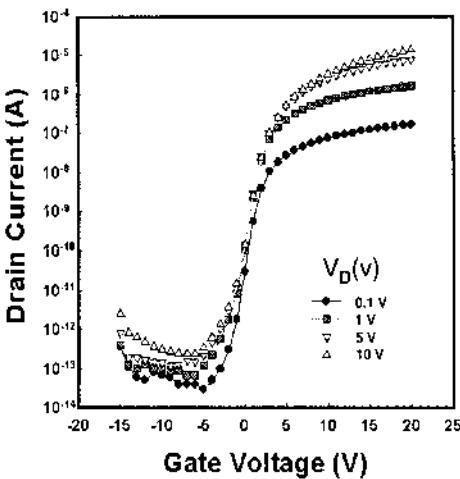


FIGURE 2.3 Transfer characteristics of an a-Si:H TFT ($W = 39 \mu\text{m}$, $L = 5 \mu\text{m}$).

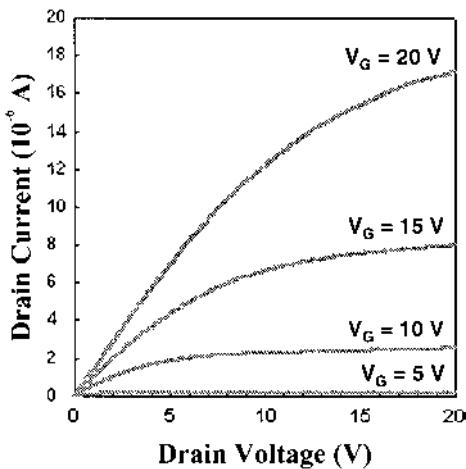


FIGURE 2.4 Output characteristics of an a-Si:H TFT ($W = 39 \mu\text{m}$, $L = 5 \mu\text{m}$).

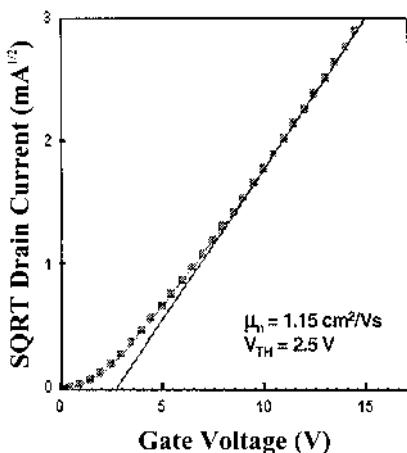


FIGURE 2.5 Plot of square root of drain current as a function of gate voltage for an a-Si:H TFT to obtain the field-effect mobility in the saturated region ($W = 39 \mu\text{m}$, $L = 5 \mu\text{m}$).

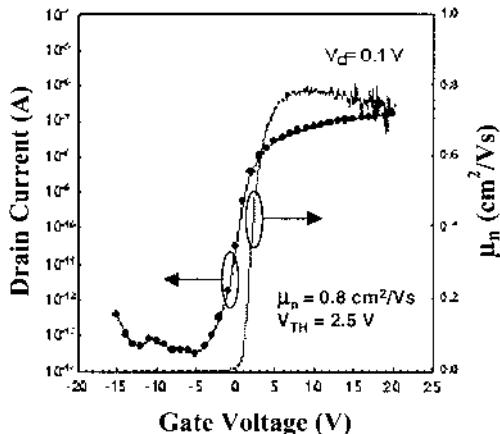


FIGURE 2.6 Transfer curve of an a-Si:H TFT at $V_D = 0.1 \text{ V}$ and field-effect mobility extracted from the transconductance ($W = 39 \mu\text{m}$, $L = 5 \mu\text{m}$).

the field-effect mobility and V_{TH} for the same a-Si:H TFT whose transfer and output characteristics were shown in Figs. 2.3 and 2.4, respectively. Figure 2.5 shows the saturation mobility extracted from plotting the square root of the drain current versus the gate voltage. Figure 2.6 shows the extraction of the linear mobility by means of a linear-region transconductance plot. Figure 2.7 shows the

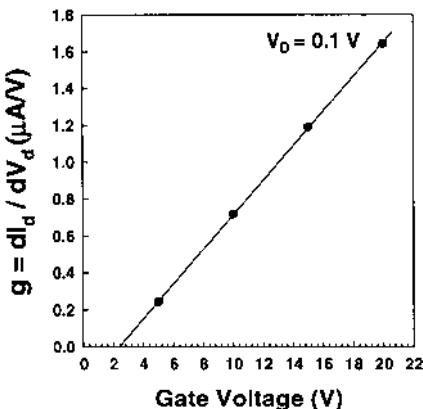


FIGURE 2.7 Field-effect mobility extracted from channel conductance in the linear region ($W = 39 \mu\text{m}$, $L = 5 \mu\text{m}$).

linear-region mobility extracted from the channel conductance at $V_D = 0.1$ V. The field-effect mobility and threshold voltage in the foregoing three cases are: $1.15 \text{ cm}^2/\text{V}\cdot\text{s}$ and 2.5 V, $0.8 \text{ cm}^2/\text{V}\cdot\text{s}$ and 2.5 V, and $0.78 \text{ cm}^2/\text{V}\cdot\text{s}$ and 2.5 V, respectively. The threshold voltage is the same (2.5 V) for the three cases, but the field-effect mobility is $0.8 \text{ cm}^2/\text{V}\cdot\text{s}$ in the linear region and $1.15 \text{ cm}^2/\text{V}\cdot\text{s}$ in the saturated region. Therefore, the mobility in the saturated region is higher by $0.35 \text{ cm}^2/\text{V}\cdot\text{s}$ than the value in the linear region. Note that the field-effect mobility of a-Si:H used in the manufacturing of TFT-LCDs is typically $0.5\text{--}0.6 \text{ cm}^2/\text{V}\cdot\text{s}$ and threshold voltage is about $2\text{--}4$ V. It is worth noting that in an AMLCD, the TFT is always found in the linear region during the pixel-charging operation.

The gate voltage swing, S , defined as the voltage required to increase the drain current by a factor of 10, is given by

$$S = \frac{dV_G}{d(\log I_D)} \quad (2.8)$$

From the straight line in [Figure 2.3](#), the S is 0.86 V/decade. Note that S is given by the maximum slope in the transfer curve.

The field-effect mobility and threshold voltage are derived from the transconductance, g_m (as in the case of MOSFETs and polycrystalline Si TFTs), given by

$$g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D=const.} = \frac{W}{L} C_i \mu_n V_D \quad (V_D < V_{Dsat}) \quad (2.9)$$

The transfer curve at $V_D = 0.1$ V and the field-effect mobility from it are shown in [Figure 2.6](#).

The performance of the TFT depends on the characteristics of the a-Si:H, such as the density of states, the conductivity, the interface state density between gate insulator and a-Si:H, and its device geometry. [Table 2.1](#) summarizes the factors influencing a-Si:H TFT performance. Here, the most important factors are the density of states in the a-Si:H, the interface states between a-Si:H and SiN_x , the interface charge at the back surface, and the quality of the n^+ contacts. To increase the field-effect mobility, the degree of disorder in the a-Si:H should be minimized [4,5]. The width of the band-tail states decreases with the degree of disorder. Detailed simulations of TFT performance as a function of the a-Si:H density of states are presented in [Chapter 3](#).

The drift mobility of electrons in a-Si:H is only about 10% of the conduction-band mobility (μ_0) because of multiple carrier trapping into the band-tail states and is given by

$$\mu = \mu_0 \exp \left(- \frac{E_c - E_A}{KT} \right) \quad (2.10)$$

where $E_c - E_A$ is the width of conduction-band tails; a value of ~ 0.1 eV for

TABLE 2.1 Factors Influencing a-Si:H TFT Performance

TFT performance	Dominant factor
On-current	<ul style="list-style-type: none">• W/L• Drift mobility• Interface states (a-Si:H/SiN_x)• Ohmic contact• Gap state density• Back interface states
Off-current	<ul style="list-style-type: none">• W/L• Fermi level (a-Si:H)• Interface (a-Si:H/SiN_x) states• Back surface charge• n⁺ contact (n⁺a-Si:H)• Band gap
Field-effect mobility	<ul style="list-style-type: none">• Width of band tails• Interface states (SiN_x/a-Si:H)
Gate voltage swing	<ul style="list-style-type: none">• Gap states (defect states)• Interface states

good material is typical, and it depends on the preparation conditions [6]. The extended-state band mobility in the conduction band is $\sim 10 \text{ cm}^2/\text{V}\cdot\text{s}$ from many experiments [7]. Accumulated carriers may also be trapped at interface states between the a-Si:H and SiN_x gate insulator. Therefore, modification of the interface by plasma treatment is important to achieve a high-mobility a-Si:H TFT. High-performance a-Si:H TFTs have field-effect mobilities of 1.5–2.0 $\text{cm}^2/\text{V}\cdot\text{s}$ [8].

Off-state drain current can be reduced by decreasing the dark conductivity of the a-Si:H, which depends on the position of the Fermi level. The Fermi level should be around the midgap of a-Si:H to have a low-level, off-state drain current. The charge density at the back surface between the back channel and passivation should be minimized to have low off-state leakage current. Any electron accumulation layer formed at the back surface increases the leakage current, so the a-Si:H bands should be flat at the back surface with the passivation layer.

2.3 DETAILED COMPARISON OF HYDROGENATED AMORPHOUS SILICON THIN-FILM TRANSIS FOR STRUCTURES

2.3.1 Inverted-Staggered Hydrogenated Amorphous Silicon Thin-Film Transistor

The inverted-staggered (bottom-gate) a-Si:H TFT is widely used in the manufacture of TFT-LCDs. There are two common bottom-gate a-Si:H TFT structures:

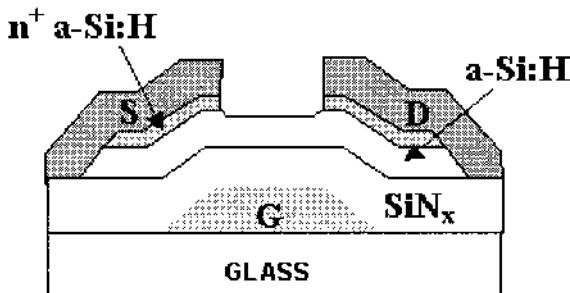


FIGURE 2.8 Cross-sectional view of a back-channel-etched (BCE) a-Si:H TFT.

the back-channel-etched (BCE) TFT shown in Figure 2.8 and the etch-stopper (ES) TFT shown in Figure 2.9. A number of differences in the fabrication process and TFT performance exist between the two.

The BCE a-Si:H TFT saves at least one photo-mask step for array fabrication compared to the ES a-Si:H TFT; however, it needs a rather thick (~200-nm) intrinsic layer to have enough process margin for n^+ etching. The n^+ layer between the source and drain electrodes must be overetched to completely remove the n^+ a-Si:H layer over the channel [9]. In an ES a-Si:H TFT, the back-channel is protected by another SiN_x layer (the ES layer), so the n^+ etch process is rather easy and the intrinsic layer can be very thin [10]. However, the processing is a little more complicated than that of the BCE a-Si:H TFT, since there are twice the number of PECVD loading and unloading steps. After SiN_x/a-Si:H/SiN_x “trilayer” deposition, the etch-stopper island must be patterned, after which the n^+ a-Si:H layer is deposited in a separate PECVD step. In the case of the BCE TFT, the gate

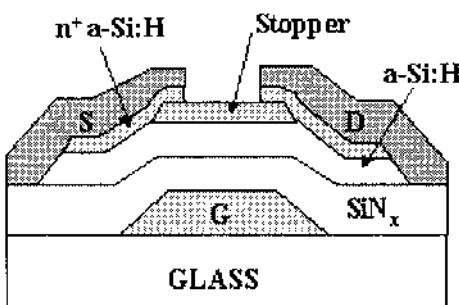


FIGURE 2.9 Cross-sectional view of an etch-stopper (ES) a-Si:H TFT.

insulator SiN_x , undoped a-Si:H, and n^+ a-Si:H layers are deposited sequentially in a single pump-down. Most of the LCD companies in Korea, Japan, and Taiwan are currently adopting a BCE a-Si:H TFT because of its simple fabrication process [11].

While it requires more process steps to produce, the ES a-Si:H TFT has much less photo-leakage current, and its extrinsic mobility can be a little higher because of a very thin i-layer. Note that the extrinsic field-effect mobility degrades when increasing the i-layer thickness because of the series contact resistance between n^+ and channel [12]. The series resistance can be lower in an ES a-Si:H TFT because of its thin i-layer. Similarly, the photo-leakage current of an a-Si:H TFT is reduced by decreasing the i-layer thickness, which admits less optical absorption of light from a backlight [13].

Figures 2.10 through 2.12 depict cross-sectional views of three types of self-aligned a-Si:H TFTs. Note that all self-aligned TFTs are of the ES type. Figure 2.10 shows a semi-self-aligned a-Si:H TFT, where a gate is used as a mask for ES patterning. In this structure the mask for the ES is not needed, but there is 1–2 μm of overlap between the gate and source/drain due to overetching of the photoresist (PR) for the ES pattern. For this process to work, the a-Si thickness should be thin enough (less than ~ 30 nm) to allow high transmittance of UV light via back-exposure.

[Figure. 2.11](#) shows a completely-self-aligned a-Si:H TFT using an ion-doped layer and silicide contacts [13]. The overlap capacitance between the source/drain and gate can be reduced in this structure. However, the silicide should be formed at less than 300°C because the a-Si:H TFT degrades with increasing temperature above 300°C. Because of low-temperature silicide formation, Cr [14], Mc [15], and Ni [16] silicides have been adopted. A layer of n^+

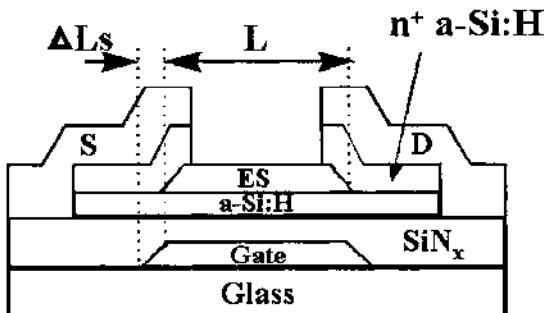


FIGURE 2.10 Cross-sectional view of a semi-self-aligned a-Si:H TFT using backside exposure for etch-stopper patterning.

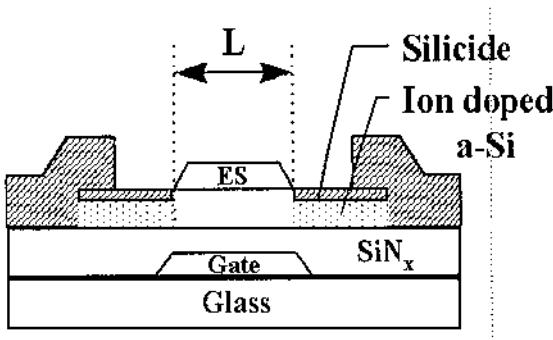


FIGURE 2.11 Cross-sectional view of a completely self-aligned a-Si:H TFT using ion doping and silicide contacts.

$\mu\text{c-Si}$ can be used instead of silicide because of its low sheet resistance [17]. Note that the conductivity of n^+ $\mu\text{c-Si}$ can be above 10 S/cm; however, the growth of $\mu\text{c-Si}$ on a-Si:H is quite different from that on a glass substrate.

Figure 2.12 shows a cross-sectional view of a completely self-aligned TFT using a laser-annealed n^+ poly-Si contact that was formed during the laser heating by the diffusion of P atoms into the Si from SOG (spin-on glass) [18]. This is a self-aligned structure formed by the exposure of laser light using the gate as a mask.

A major advantage of the completely self-aligned structure is that it reduces the pixel feed-through voltage, ΔV_p , due to the reduction in overlap capacitance between gate and source/drain. It is especially useful in a large-area display,

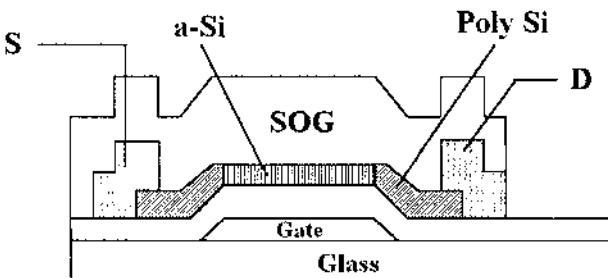


FIGURE 2.12 Completely self-aligned a-Si:H TFT with n^+ poly-Si contacts recrystallized by excimer laser annealing (ELA).

which require repeated stitched exposures by a stepper. Due to the inhomogeneity of ΔV_p , there may be stitch (area defects) in the TFT-LCD because the overlap capacitance changes shot by shot. However, the formation of silicide at low temperatures and the light leaking through from the gate side are the drawbacks of this structure for LCD manufacturing. The gate should screen the light completely to have a low off-state leakage current; however, in a completely self-aligned structure, the light blocking by the gate may not be complete.

Regardless of the structure chosen, the gate insulator SiN_x deposited by PECVD must be of high quality. One problem that may arise during the deposition process is particle generation and/or the electrical breakdown due to the charges in the plasma. In the early stages of TFT-LCD manufacturing, this problem was countered by Toshiba through the use of a double-layered gate insulator such as $\text{SiN}_x/\text{APCVD SiO}_2$ [19]. However, the deposition of two separate layers using different equipment is more complicated; thus the double-layered gate insulator is not widely adopted in the manufacturing of LCDs today [20]. The double-layered approach can reduce the breakdown through the gate insulator and also reduce the pinhole density that might be caused by a plasma-generated particle or by electrical breakdown. In PECVD processing the important point is to reduce the particle generation caused by gas-phase polymerization.

Figure 2.13 shows a cross-sectional view of an a-Si:H TFT with a planarized gate. A layer of BCB (benzocyclobutene) is used for planarization because of its good insulating and planarization properties [21,22]. The gates can be planarized by the deposition of organic insulator by simple spin coating. As panel sizes increase and resolution becomes higher, the problem of RC delay in the metal lines becomes more important. The TFT parasitic capacitance, C_{gs} between gate and source/drain and the overlap capacitance at the gate and data lines crossovers

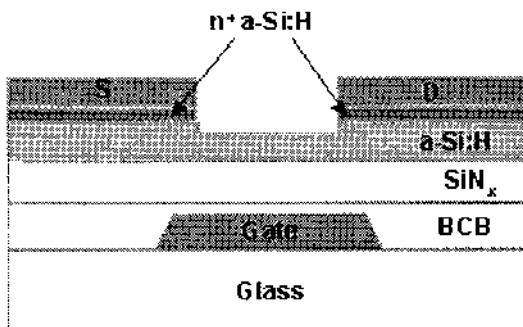


FIGURE 2.13 Cross-sectional view of an a-Si:H TFT having a planarized BCB layer over the gate.

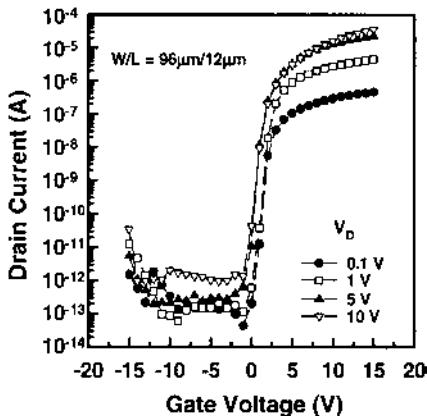


FIGURE 2.14 Transfer characteristics of an a-Si:H TFT with 70-nm-thick SiN_x on a BCB planarized gate.

are major factors that contribute to the capacitance C . The feed-through voltage shift, ΔV_p , depends on the C_{gs} ; its implications for AMLCD performance are discussed in detail in [Chapter 5](#).

The RC delay induces nonuniformity of the display because the gate pulse is distorted. To reduce the resistance R , low-resistivity metals such as Al, Cu, and Ag may be used. In the case of Al, it has a hillock problem that is induced by heating it above 300°C [23]; with Cu and Ag, etching and adhesion to the substrate may be issues [24]. When we increase the metal thickness, good step coverage at the gate-line edge becomes an issue that can decrease the production yield of the TFT arrays. Planarization can solve the step coverage issue and allow for a thicker gate metal, which also decreases the RC delay.

A planarized gate insulator with a low-dielectric-constant material also decreases the crossover capacitance. An a-Si:H TFT having a very thin gate insulator and a planarized gate layer has been fabricated that shows low threshold voltage and thus a high on-current at low driving voltage. This TFT is suitable for low-power-consumption TFT-LCDs with a low driving voltage. Figure 2.14 shows the transfer characteristics for an a-Si:H TFT with a planarized gate using a BCB. Note that the thickness of gate insulator SiN_x is only 70 nm [25]. The V_{TH} and μ_n are 2.48 V and $0.944 \text{ cm}^2/\text{V}\cdot\text{s}$, respectively.

2.3.2 Staggered Thin-Film Transistor Structure

A staggered (top-gate) a-Si:H TFT was adopted by Hosiden Co. in Japan, and it has several advantages: the process allows the utilization of Al gate metal, and the etching of the n^+ a-Si:H in the channel region is easy in comparison to the

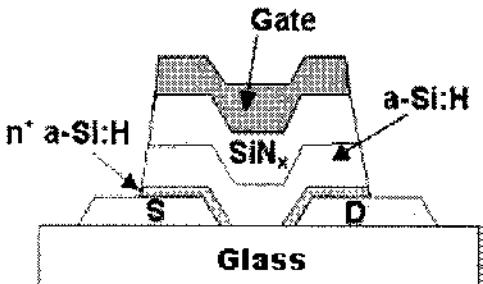


FIGURE 2.15 Cross-sectional view of a staggered (top-gate) a-Si:H TFT.

inverted-staggered TFT [26]. Note that the process temperature after Al deposition can be less than 250°C. As mentioned earlier, any plasma damage to the a-Si:H during the SiN_x deposition should be minimized by reducing the RF power. One disadvantage is that the n^+ a-Si:H is exposed to air before the a-Si:H and SiN_x are deposited by PECVD, which can lead to contact problems. This also means that twice the number of PECVD process steps, including loading and unloading, are needed for the TFT manufacture as compared with the BCE a-Si:H TFT structure. Figure 2.15 shows a cross-sectional view of a top-gate staggered TFT. Only one company in Japan uses this structure for LCD manufacturing.

2.3.3 Short-Channel Hydrogenated Amorphous Silicon Thin-Film Transistor

A short-channel TFT is needed to meet the demand for high-resolution display. Typically, the extrinsic field-effect mobility decreases when reducing the channel length, mainly due to the increase in the ratio of contact resistance to on-state channel resistance [27]. One approach to reducing the contact resistance is to replace the n^+ a-Si:H contact layer with a laser-annealed poly-Si n^+ layer, as shown in Figure 2.16.

Because the resistivity of n^+ a-Si:H is typically $\sim 100 \Omega\text{-cm}$, the contact resistance becomes a more important component of the total on-state resistance when the channel length is very short. Therefore, to investigate the short-channel effect of a-Si:H TFTs without a contact problem, n^+ poly-Si can be adopted, as shown in Figure 2.16. In this structure the poly-Si is made by the laser exposure from the backside, in which case the a-Si:H remains only in the channel region.

The kink effect, which is typically seen in poly-Si TFTs, is not present in the current–voltage characteristics of a short-channel a-Si:H TFT [28]. The kink effect is due to the breakage of covalent bonds by hot carriers generated in the high-electric-field region close to the drain; however, in a-Si:H the carriers cannot

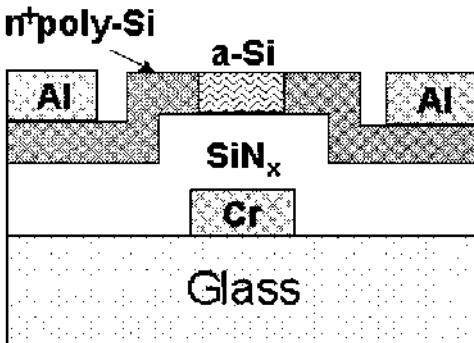


FIGURE 2.16 Cross sectional view of a short-channel a-Si:H TFT, where crystallization of the contact region is done via backside laser exposure.

achieve high velocity because of a short mean free path of ~ 10 nm. Thus the carriers are scattered before absorbing enough energy in the applied electric field. The scattering in a-Si:H is due mainly to the disorder potential. This is an advantage of using an a-Si:H in short-channel devices.

2.3.4 Coplanar Thin-Film Transistor

Most a-Si:H TFTs produced today are of either the normal (top-gate) or inverted (bottom-gate) staggered structure. The staggered configuration addresses the need for sufficient overlap between the gate and source/drain electrodes to achieve good carrier injection at the contacts, which is in turn due to the high resistivity of undoped a-Si:H ($>10^{10} \Omega\text{-cm}$). Any series resistance between the channel and source/drain degrades the TFT performance. It is very difficult to have an overlap between the gate and source/drain in a coplanar TFT by using conventional photolithography. Conventional ion implantation used for MOSFETs and poly-Si TFTs cannot provide a good a-Si:H TFT because the ion damage in the n^+ region cannot be removed by annealing at “low” temperatures ($\sim 350^\circ\text{C}$), and the a-Si:H and SiNx films degrade with heating above 350°C .

Even though the coplanar TFT is not used in the manufacturing of LCDs, it has several advantages, such as low parasitic capacitance between the gate and source/drain and low parasitic resistance between the channel and source/drain provided there is no offset between the source/drain contact and the electron channel. To this end, low-resistivity Ni silicide can be formed at 250°C with a sheet resistance less than 10 ohms/square [29].

A coplanar TFT has been developed using a triple layer of a-Si:H/SiNx/a-Si:H, Ni silicide, and ion doping. This structure is similar to a MOSFET [30].

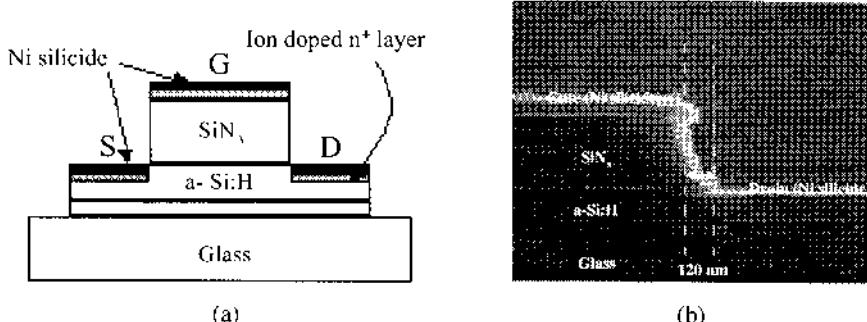


FIGURE 2.17 Schematic (a) and SEM cross-sectional (b) views of a coplanar a-Si:H TFT.

Figure 2.17 is a schematic cross-sectional view of the coplanar TFT (a) and its scanning electron microscopy (SEM) picture at the edge (b). The fabrication process was as follows: starting with the glass substrate, a-Si:H, SiN_x , and thin a-Si:H layers were deposited sequentially by PECVD. Following island formation of the top a-Si:H and SiN_x , ion doping was carried out to dope the source/drain contact. A thin Ni layer was subsequently deposited by sputtering and then heated at 250°C for 30 minutes for silicide formation. The Ni remaining on the silicide was then etched away, yielding a coplanar TFT [31,32]. Note that the offset at the source/drain region is $\sim 0.13 \mu\text{m}$, as shown in the SEM. This is an acceptable value in view of the diffusion length of electrons in a-Si:H.

The carrier transport takes place in a plane for a coplanar TFT, as opposed to an inverse-staggered TFT, where there is a series resistance between the channel and source/drain. Because of the transport in a plane, the series resistance in well-designed coplanar TFTs can be reduced to a level of $\sim 10^4 \Omega$, which is one order of magnitude less than that ($\sim 10^5 \Omega$) of an inverted-staggered a-Si:H TFT [33]. The parasitic capacitance between the gate and source/drain can also be greatly reduced in a coplanar TFT, compared to the staggered TFT. Figure 2.18 shows the transfer (a) and transconductance characteristics (b) for a coplanar TFT. The field-effect mobility in the linear region is $\sim 0.6 \text{ cm}^2/\text{V}\cdot\text{s}$, and the on-off drain current ratio is higher than 10^7 [34]. The mobility fit in the linear region is also shown in the inset of Figure 2.18b.

In an inverted-staggered a-Si:H TFT, the gate insulator is thick ($>300 \text{ nm}$) because of the need for adequate step coverage at the gate edge to reduce the possibility of shorting at the edges. However, in a coplanar TFT there is no step coverage problem, and thus the gate insulator can be very thin. Note that the gate SiO_2 is less than 10 nm in a MOSFET. In one experiment, the gate insulator was

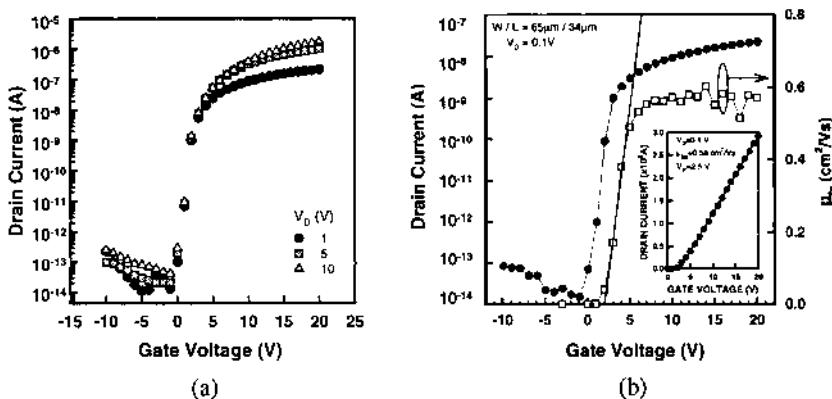


FIGURE 2.18 Transfer (a) and transconductance (b) characteristics of a coplanar a-Si:H TFT.

reduced to 35 nm for a coplanar TFT [32]. It is also noted that the a-Si:H can be made thin enough (< 5 nm) in a coplanar TFT to reduce the light absorption in the i-layer [33]; this decreases the photoleakage current significantly [35].

2.3.5 High-Voltage Hydrogenated Amorphous Silicon Thin-Film Transistor

If an offset region is made intentionally between gate and source/drain in an a-Si:H TFT by photolithography, this creates a high series resistance, meaning that the current is very low. However, if the drain field is increased in this structure, space-charge-limited currents appear as a result of high field in the offset. Since the density of states in the gap at the Fermi level of a-Si:H is quite low, i.e., $10^{16} \text{ cm}^{-3} \text{ eV}^{-1}$, the Fermi level can be shifted by the electrons injected to the a-Si:H at a high drain field. This results in an increase in the drain current up to the level of conventional a-Si:H TFT. In order to fill the states in the gap by the injected electrons, the drain voltage must be higher than 50 V, depending on the geometry of the TFT [36]. In this way, then, one can design a TFT that may be operated at high voltage.

2.4 PECVD MATERIALS DEPOSITION FOR HIGH-PERFORMANCE HYDROGENATED AMORPHOUS SILICON THIN-FILM TRANSISTORS

2.4.1 Deposition of Hydrogenated Amorphous Silicon by PECVD

The a-Si:H and SiN_x utilized in TFT array fabrication are prepared by PECVD. The TFT performance depends on the preparation conditions, such as substrate

temperature, RF power, and gas dilution. Oxygen incorporation during a-Si:H deposition in particular has been found to greatly degrade TFT performance, because it increases the defect density in the undoped a-Si:H.

Hydrogenated amorphous silicon has a short-range order, which means that the coordination number, bond angle, and bond length are close to those for a single crystalline Si within 2 or 3 atomic distances, but there is no periodicity in the long range. Because of this there are a considerable number of localized states in the gap. The hydrogen in the a-Si:H reduces the dangling bonds by passivation. Therefore, the dangling bond density of $\sim 10^{20} \text{ cm}^{-3}$ in vacuum-evaporated a-Si or sputtered a-Si is reduced to $10^{15}\text{--}10^{16} \text{ cm}^{-3}$ in PECVD a-Si:H, where hydrogen content is 10–30 at.%. The hydrogen reduces the tail-state density in addition to the reduction of dangling bonds, because the disorder is decreased by hydrogen incorporation. Typically, undoped a-Si:H for TFT applications is prepared at a substrate temperature of 220–350°C. The hydrogen in a-Si:H may be incorporated as SiH or SiH₂; however, only films with hydrogen bonded as Si-H are suitable for TFT application [37].

Precursor gases for PECVD deposition of a-Si:H may be SiH₄ or Si₂H₆, with H₂, He, and/or Ar being used as carriers/diluents to decrease the density of localized states or modify the material into μc -Si. The μc -Si is deposited by PECVD under similar deposition conditions used for a-Si:H, except with high dilution of silane with hydrogen. The grain size is usually less than 50 nm, and film shows a columnar growth. Because the grain size is quite small and there are a lot of defects inside the grains, the field-effect mobility of μc -Si is comparable to that of high-quality a-Si:H TFTs. Moreover, the off-state drain current is much higher than that of a-Si:H TFT because of its high conductivity ($>10^{-6} \text{ S/cm}$) and high density of defects.

The hydrogen/silane dilution ratio is typically higher than 30 for the growth of μc -Si, and the RF power is also an important parameter. The role of hydrogen during the deposition in the PECVD chamber can be summarized as follows:

1. Hydrogen atoms cover the growing surface and increase the diffusion length of the Si precursors. Therefore, the precursors can migrate to a more stable position [38].
2. Atomic hydrogen diffuses into the silicon network down to a few nanometers and thus enhances the relaxation of Si atoms, leading to the more stable structure [39].
3. Atomic hydrogen etches the weak Si–Si bonds and thus more stable Si–Si bonds are formed [40].

The precursor for a-Si:H deposition is SiH₃ [41]. Films of a-Si:H deposited by PECVD at lower RF power have better step coverage and low defect density, whereas a-Si films deposited at higher RF power generally have more defects. Particles can be formed by plasma polymerization of radicals and/or ions in the PECVD chamber. In addition, the plasma potential during deposition can cause

ion damage of the growing film, which is especially a problem at high RF power [42].

Among the various deposition control variables, such as gas flow rate, gas pressure, RF power, and substrate temperature, the hydrogen content of the final film is greatly affected by the substrate temperature. The hydrogen content decreases with increasing substrate temperature because of the enhanced out-diffusion of hydrogen from the film. Therefore, the optical band gap decreases when increasing the substrate temperature, since the optical band gap increases with hydrogen content in the a-Si:H.

The deposition rate increases with the gas flow rate, but at high flow rates there is more gas-phase, plasma polymerization. At too low a flow rate, more ion damage is expected because of the increased plasma potential. Therefore, an optimum intermediate flow rate is important for the deposition of device-quality a-Si:H.

During a-Si:H deposition, the precursor arriving at the growing surface is mainly SiH₃, and it bonds with the surface atoms, resulting in the deposition of a-Si:H and out-diffusion of hydrogen. The products can be H₂ and/or SiH₄. Deposition occurs by heterogeneous reaction at the growing surface [43], and ion bombardment of the surface can affect the film property. Increasing the RF power decreases the surface diffusion length of precursor radicals and increases the sticking coefficient to the substrate. Table 2.2 shows the physical properties of device-quality a-Si:H used for TFT fabrication

TABLE 2.2 Physical Properties of a Device-Quality a-Si:H

Material constant	Typical value
Dark conductivity	10^{-11} S/cm
Conductivity activation energy	0.82 eV
Photoconductivity ($100\text{ mW}\cdot\text{cm}^{-2}$)	1×10^{-4} S/cm
Optical band gap	1.7–1.8 eV
Temperature coefficient of optical band gap	2.7×10^{-4} eV/K
Electron mobility	$0.5\text{--}1.0\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$
Hole mobility	1×10^{-3} to $5 \times 10^{-3}\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$
Carrier diffusion length	< 1.0 μm
Electron affinity	3.93 eV
Refractive index	4.3
Density	$2.2\text{ g}\cdot\text{cm}^{-3}$
Hydrogen content	18 at.%
Valence-band tail slope	42–50 meV
Conduction-band tail slope	25 meV
ESR spin density	$\sim 10^{15}\text{ cm}^{-3}$

2.4.2 Deposition of SiN_x by PECVD

Plasma-deposited silicon nitride, SiN_x, is used for the passivation of electronic devices and as the gate insulator of choice for a-Si:H TFTs. As a passivation film, silicon nitride protects against the diffusion of water vapor, sodium, and oxygen into the active device. The hydrogen content of plasma-deposited silicon nitride is 10–40 at.%, and most of the hydrogen atoms are bonded as Si-H and/or N-H, depending on the preparation conditions, such as RF power, feeding gas, and substrate temperature. Total hydrogen content decreases with increasing substrate temperature or increasing RF power [44].

Silicon nitride has an amorphous structure, and its properties depend on the relative atomic concentrations of silicon, nitrogen, and hydrogen. For good-electrical-quality a-Si:H TFTs, PECVD-deposited SiN_x is much more suitable than stoichiometric Si₃N₄. Silicon nitride deposited at 300–350°C (abbreviated as SiN_x or SiN:H) is quite a different material from Si₃N₄ produced by CVD at 700–900°C [45].

Hydrogen in SiN_x saturates the traps, so the defect density is much less than that of a CVD Si₃N₄. The interface charge density between a-Si:H and SiN_x is typically in the range of 2×10^{11} to $7 \times 10^{12} \text{ eV}^{-1}\text{cm}^{-2}$, and it strongly depends on the deposition conditions: it increases with decreasing substrate temperature or decreasing RF power. Note that the trap density in SiN_x increases on heating above 400°C, because the hydrogen is out-diffused as a result of breakage of hydrogen bonds in Si-H and/or N-H modes [46].

The ability to form a good insulating film at low temperature (less than 350°C) having a low interface state density with a-Si:H ($\sim 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$) makes SiN_x a good gate insulator. In addition, the ability to employ the same PECVD equipment used to deposit the a-Si:H is an important advantage. SiN_x is typically deposited from a mixture of SiH₄, NH₃, N₂, and He at 300–350°C. The RF power is typically higher than that used for a-Si:H deposition, and the best material for the TFTs is a N-rich SiN_x [47].

The field-effect mobility in the linear region is of prime importance for pixel charging in TFT-LCD applications. The interface between SiN_x and a-Si:H affects the field-effect mobility; in particular, the surface roughness of the SiN_x layer is important because it affects the initial growth of a-Si:H, which forms the active channel layer for the TFT [48]. [Figure 2.19](#) is a plot of the field-effect mobility of an a-Si:H TFT as a function of average surface roughness of the SiN_x insulator. The straight line in the figure indicates that mobility increases with decreasing roughness. This plot was obtained using data from a-Si:H TFTs produced where all other deposition conditions were kept constant except those of the SiN_x process [48]. The surface roughness depends both on the SiN_x deposition conditions and on any surface modification by plasma treatment.

[Figure 2.20](#) shows a cross-sectional view of an a-Si:H TFT with an APCVD SiO₂ gate insulator. By exposing the SiO₂ surface to a N₂ plasma treatment, it

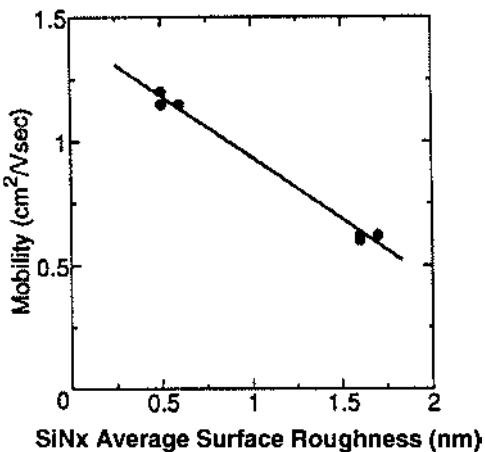


FIGURE 2.19 Field-effect mobility of a-Si:H as a function of the surface roughness of SiN_x . (From Ref. 49.)

was found that the TFT performance was significantly improved [49]. Contrary to the Si/SiO_2 interface, which is highly stable, hydrogen in the a-Si:H film can degrade the interface by forming O–H bonds. Thus, exposure of the surface to the N_2 plasma prevents the formation of O–H bonds by terminating the oxide surface with N atoms.

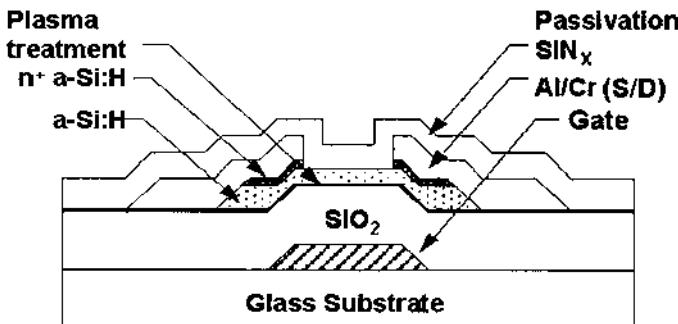


FIGURE 2.20 Cross-sectional view of a BCE TFT where the SiO_2 gate insulator has been treated with N_2 plasma prior to a-Si:H deposition.

2.4.3 Deposition of n^+ Hydrogenated Amorphous Silicon by PECVD

Deposition of an n^+ a-Si:H layer between undoped a-Si:H and a metal allows the formation of an ohmic contact between them. The ohmic contact also acts as a hole-blocking layer because it acts to depress the position of the contacting semiconductor valence band with respect to the Fermi level of the metal. The resistivity of n^+ a-Si:H is about $100 \Omega\text{-cm}$, which is much higher than that of n^+ crystalline silicon. Even though the resistivity is relatively high, the current is not generally limited by the n^+ contact itself, because the drain current is on the order of microamps. For typical AMLCD TFT channel lengths ($\sim 10 \mu\text{m}$) and for thicknesses of a-Si:H below $\sim 100 \text{ nm}$, the use of n^+ poly-Si or n^+ $\mu\text{c-Si}$ contact layers does not appreciably increase the drain current over that of standard n^+ a-Si:H contact. In most cases, n^+ a-Si:H is deposited by PECVD using a silane mixture containing $\sim 1\%$ PH_3 . PECVD deposition using this doping gas mixture diluted at a ratio of $\sim 1:50$ in hydrogen allows the formation of n^+ $\mu\text{c-Si}$. Adding more than $\sim 1\%$ PH_3 to silane does not further decrease the resistivity of n^+ a-Si:H, because the defect density of the material begins to grow in proportion to the added dopant, negating any further enhancement of the free carrier population.

2.4.4 Interface Improvements

One of the greatest advantages of the a-Si:H TFT is its extremely low leakage current of less than 1 pA in the off-state, even though the staggered structure has significant gate to source/drain overlap. This is due to the relatively high band gap of $\sim 1.8 \text{ eV}$ and low density of states in the gap. To further reduce the leakage current in a BCE-type a-Si:H TFT, a hydrogen plasma treatment of the back-channel may be beneficial. This treatment may increase the hydrogen content in the active layer, but this depends on the treatment time. When the treatment time is long, the surface region is partially changed into microcrystalline phase, resulting in an increase in leakage current. The treatment also influences the interface between the back-channel of a-Si:H and the passivation layer. He plasma can also be used for the reduction in the leakage current [51].

Improvement in the field-effect mobility is important for the application of TFTs in high-resolution and large-area displays. [Figure 2.21](#) depicts a cross-sectional view of an a-Si:H TFT where the SiN_x gate insulator surface has been plasma treated with He, H_2 , NH_3 , or N_2 before deposition of the a-Si:H layer. [Figure 2.22](#) shows the field-effect mobility and threshold voltages resulting from the four treatments. In each case, the mobility increases with plasma exposure up to a certain time, after which it begins to fall off. Experiments such as these have shown that the enhanced mobility may be due to a decrease in surface roughness following treatment [52]. The stability of the TFT may also be im-

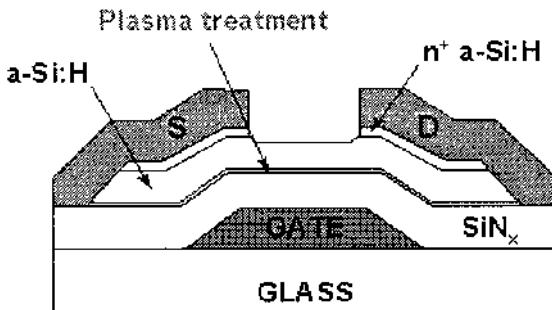


FIGURE 2.21 Cross-sectional view of a BCE TFT where the SiN_x gate insulator has been treated with He, H_2 , NH_3 , or N_2 plasma prior to $a\text{-Si:H}$ deposition.

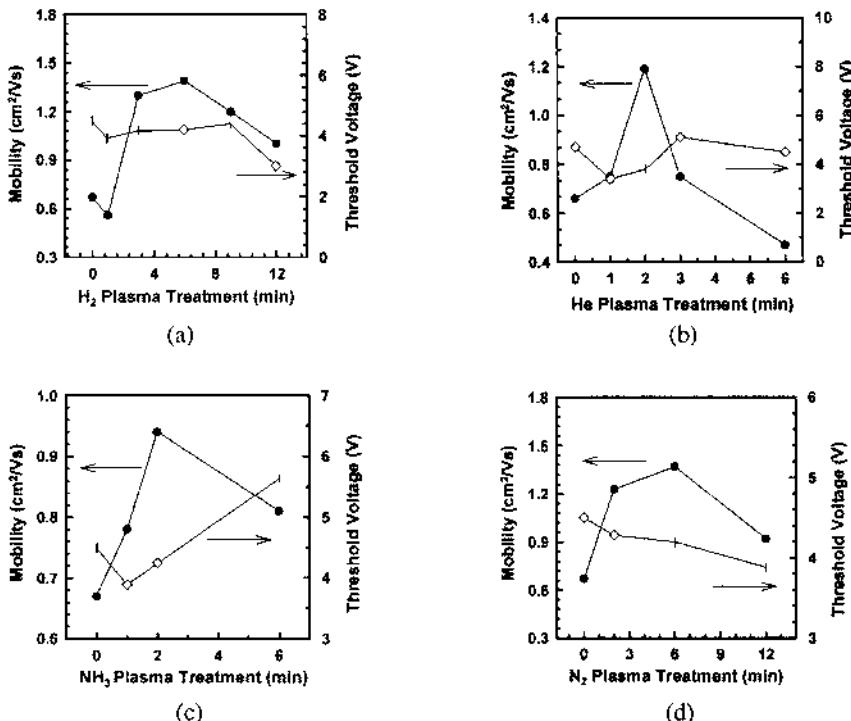


FIGURE 2.22 Field-effect mobility and threshold voltage of $a\text{-Si:H}$ TFTs resulting from gate SiN_x plasma treatments with H_2 (a), He (b), NH_3 (c), or N_2 (d) plasma.

proved by the removal of metastable species such $\text{Si}(\text{NH})_x$ on the SiN_x surface, which act as interfacial trap states. During the plasma exposure these metastable species can be etched away and/or modified, leaving a more stable interface. The degradation resulting from long exposure times is generally attributed to ion-induced damage of the SiN_x .

2.5 HYDROGENATED AMORPHOUS SILICON THIN-FILM TRANSISTORS ON PLASTIC SUBSTRATES

Glass is clearly the substrate of choice in today's TFT-LCD manufacturing lines. While flexible plastic substrates have a number of advantages, in that they are lightweight, rugged, foldable, compact, conformal, and of low cost, they also are more susceptible to chemical attack, less thermally stable, and have rougher surfaces. The greatest difference between conventional a-Si:H TFT processing and TFT fabrication on plastic is the substrate temperature [53,54]. Because of dimensional change of the plastic during heating, the substrate temperature should be kept as low as possible. A second important issue associated with plastic is its high gas permeability, which makes it necessary to deposit some form of gas barrier on both faces of the plastic before TFT fabrication begins.

2.5.1 Low-Temperature Deposition

A typical substrate temperature for a-Si:H TFT on glass substrate is $\sim 300^\circ\text{C}$; however, the substrate temperature of a-Si:H on plastic should be kept less than $\sim 150^\circ\text{C}$, because most plastic cannot withstand prolonged heating above this temperature. The actual upper limit depends on the plastic material itself [55].

When producing a-Si:H TFTs on plastic at low temperatures, leakage current through the SiN_x gate insulator becomes a serious issue, in addition to the degradation in the TFT performance. The hydrogen content in SiN_x increases with decreasing substrate temperature, and this may be one cause of the increased leakage current [56]. Dilution of the silane/ammonia plasma with a halogen or hydrogen in the deposition chamber can result in an improved-quality SiN_x even at low substrate temperatures. He dilution of the silane plasma reduces the deposition rate and thus increases the film density [56,57]. In general, the deposition rate decreases with increasing carrier gas dilution, and hydrogen or argon dilution in the chamber increases the refractive index of SiN_x [57]. These experimental results indicate that some form of dilution in the plasma is necessary to deposit device-quality SiN_x at low temperatures.

As the RF power is increased, the refractive index of SiN_x increases while its etch rate deceases, indicating that the film becomes denser [56]. In order to improve the density of SiN_x deposited at lower substrate temperatures, He, Ar, and/or H_2 are added to the plasma. The radicals or ions from the dilution gas etch

the weak Si–Si and Si–N, resulting in the reduction in the deposition rate. In good-quality films there are more Si–N bonds and less Si–H bonds. He dilution improves the film density, but it also changes the stress in the films. Films deposited using He dilution exhibit compressive stress, compared to those grown without He dilution, which exhibit tensile stress, but the magnitude of the stress is reduced by a factor of 10 by using He dilution [65].

A good deal of experimental work has been performed on the deposition of a-Si:H at low temperatures. One technique for depositing a-Si:H at low temperature is by reactive RF sputtering [58], where hydrogen is added to the Ar ambient in the sputtering chamber in order to deposit device-quality material that has a hydrogen content of 5–10 at %. Films deposited at low temperature generally have high hydrogen content, but most of the hydrogen is bonded as Si–H₂, and the film can be porous, leading to gas absorption from the air. Further, the film may have a columnar structure and a significant density of defects [59]. The addition of He and/or hydrogen causes the growth rate to decrease and the hydrogen to bond as Si–H, improving the electronic properties. Improvement in device-quality a-Si:H at low temperatures by hydrogen dilution has been attributed to the fact that the slower growth rate, and copious amounts of activated hydrogen help to form stable Si–Si bonds, which would normally occur due to thermal relaxation at 300°C [57].

Hydrogen dilution of silane plasma at low temperatures has been studied as a means of improving the material properties of μ c-Si as well as a-Si:H. It is known that μ c-Si can be obtained by diluting silane in a large volume of hydrogen, but the dependence is affected by substrate temperature. The hydrogen content in the film drops when the μ c-Si is formed. Note that even at 100°C, μ c-Si can be grown from a silane–hydrogen mixture.

He dilution can have a similar effect. It is found that the SiH₂ density in a-Si:H, which appears in Fourier transform infrared (FTIR) spectrum at 2090 cm⁻¹ (stretch) and 890 cm⁻¹ (scissors-wagging doublet), decreases with increasing He dilution. This means that the Si–H bond density increases and the Si–H₂ bond density decreases by an addition of He to the silane plasma. By optimizing the He dilution ratio, the quality of a-Si:H can be improved and its properties made similar to device-quality a-Si:H deposited at optimum substrate temperatures [59]. By simultaneous optimization of He dilution and RF power, good-quality a-Si:H TFTs have been fabricated at substrate temperatures as low as 110°C [59]. The following properties have been measured: on–off drain current ratio of \sim 10⁷, a field-effect mobility of \sim 0.5 cm²/V-s, and a good linear output characteristic, with no current crowding at low drain voltage.

2.5.2 Gas-Barrier Films for Plastic Substrates

One of the difficulties associated with processing plastic substrates is gas out-diffusion from the plastic during heating and subsequent gas absorption during

TABLE 2.3 Transmission Rate (TR) for the Plastic Films

Material	Density (g·cm ⁻³)	Melting point (°C)	O ₂ TR (cm ³ m ⁻² d ⁻¹)	H ₂ O TR (gm ⁻² d ⁻¹)
PE (30 µm)	0.91–0.94	104–120	4800	15
PP (19 µm)	0.84–0.91	130–170	1700	5
PET (12 µm)	1.38–1.42	256–260	140	46

d = day

cooling to room temperature. Associated with this out-diffusion and subsequent absorption of gas is an undesirable change in substrate dimension once it has been heated and cooled [61]. High gas permeability of the substrate can lead to instability of the TFTs over time. To prevent gas absorption in the plastic substrate, an inorganic gas-barrier film, such as PECVD SiO₂ or SiN_x, can be used. By depositing a suitable thickness of SiO₂ or SiN_x, the transmittance of oxygen and H₂O vapor can be reduced by a factor of 100 [62]. Prior to the deposition of the gas-barrier layer, the plastic substrate must be heated at an appropriate temperature for a prolonged time, on the order of 48 hours, to remove the gas absorbates and the vapor trapped within the substrate. This preannealing process reduces the volume of the plastic. Following the preannealing, the gas barrier is deposited to protect it from any further gas absorption.

Table 2.3 shows the gas transmittance characteristics of the plastic substrates PE (polyethylene), PP (polypropylene), and PET (polyethylene terephthalate) for water vapor and oxygen [63]. PET, which has the highest melting point of the three materials, can transmit 140 cm³ of oxygen and 46 g of water vapor per day across an area equal to 1 m².

Figure 2.23 shows the shrinkage for PES (polyethersulfone) at 180 and 200°C. The change is very drastic during the early stage and then gradually saturates. The ultimate change in substrate dimension strongly depends on the sample temperature; even after prolonged heating, the shrinkage is smaller at lower temperature. The shrinkage characteristics can be explained by an activated process of gas desorption from the plastic substrate [64].

Degassing of the plastic substrate is usually done at a temperature slightly higher than the maximum TFT processing temperature, to prevent further shrinkage during TFT fabrication. Films of SiO₂, SiN_x, AlO_x, AlN_x, and Ta₂O₅ have been used as gas barriers. These not only protect the plastic from gas adsorption, but can also improve the adhesion of metal to the substrate [61].

2.5.3 Stress Effects

Stress arises from differences in the thermal expansion coefficients between plastic and the a-Si:H/SiN_x films, and it increases with increasing deposition tempera-

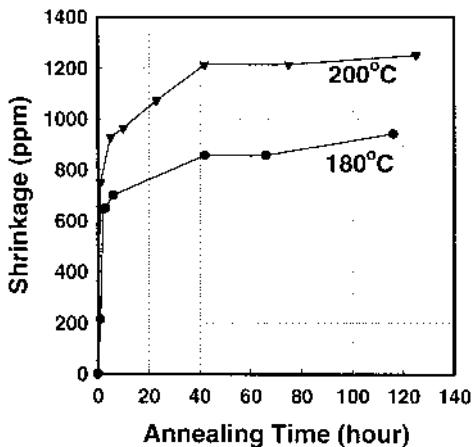


FIGURE 2.23 Shrinkage of a PES (polyethersulfone) substrate at 180°C (●) and 200°C (▼)

ture. Stressed films on plastic are susceptible to peeling or cracking, a problem that only becomes more serious at higher deposition temperatures. If there is no loss of adhesion, plastic films tend to bend because of the stress induced by the relative thermal expansion between a-Si:H/SiN_x and plastic [61]. Table 2.4 shows the thermal expansion coefficients for typical materials used in the fabrication of a-Si:H TFT arrays. In general, the thermal expansion coefficients of most plastics are almost 10 times that of SiN_x. Because of this large difference, cracking, peeling, and bending are major issues to be overcome in plastic display fabrication, and the deposition temperature should therefore be as low as possible.

Figure 2.24 shows the substrate elongation at each major process step during the fabrication of an a-Si:H TFT array on a PES substrate, where an organic material is used as the first layer of the gate insulator stack. In the figure, size deformation does not appear except during the PECVD process. Reversible size

TABLE 2.4 Thermal Expansion Coefficients for TFT Electronic Materials and Typical Plastic Substrates

Dielectrics	Metals	Glass	PES	PET	PAR	PC
5.5–7.5	8.5–30	5	50	70	57	20–50

Unit: ppm/°K; PAR: polyarylate; PC: polycarbonate.

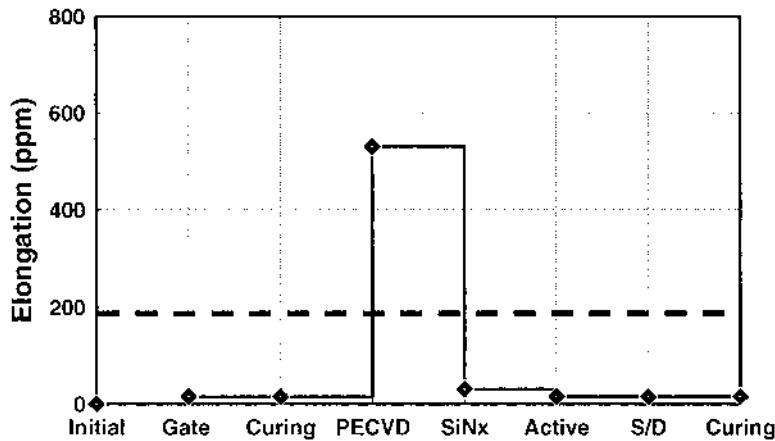


FIGURE 2.24 Elongation as a function of processing steps for an a-Si:H TFT fabricated.

deformation took place when the fabrication process was not carried out continuously. In the case where the sample was stored in vacuum until processing resumed, there was no size deformation, indicating that the origin of deformation is gas absorption during the process intermission.

Thin-film transistor performance may degrade as the stress-induced bending of the substrate increases. To prevent the substrate from bending, both sides of the plastic are coated with the same thickness of gas-barrier material. Regardless, internal stress exists between the plastic and SiN_x , which can increase the leakage

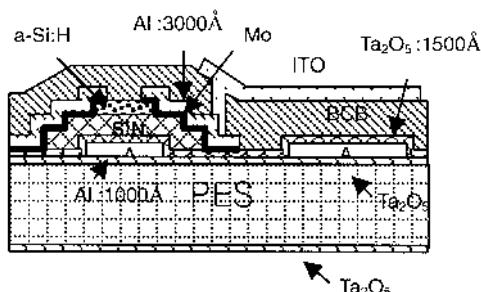
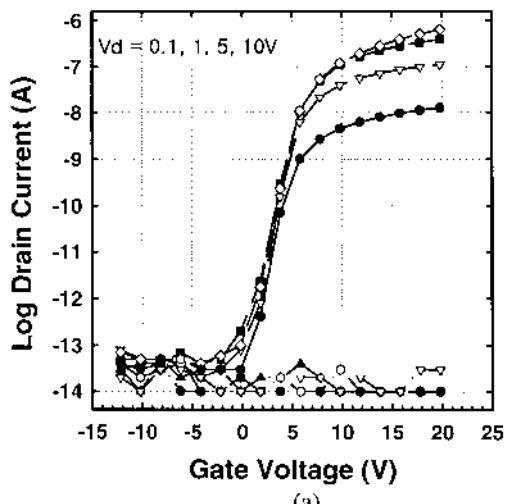
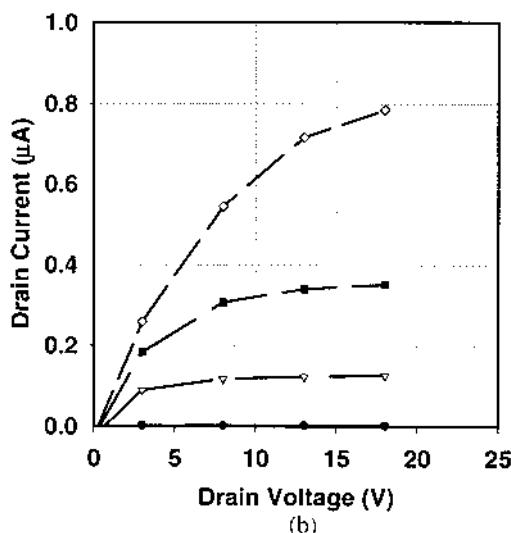


FIGURE 2.25 Cross-sectional view of a-Si:H TFT fabricated on plastic using a TaO_x .



(a)



(b)

FIGURE 2.26 Transfer (a) and output characteristics (b) of an a-Si:H TFT fabricated on PES at 150°C.

current of the TFT [56]. [Figure 2.25](#) shows cross-sectional views of a-Si:H TFTs on plastic using a TaO_x . The patterning of the SiN_x and the adoption of a double-layered gate insulator greatly decreases the gate leakage current. Besides being useful for gate planarization as well as protecting gate lines against chemical attack, organic dielectrics are more amenable to plastic substrate processing due to the closer match of their mechanical properties with those of the substrate.

[Figure 2.26a](#) shows the transfer characteristic of an a-Si:H TFT built on plastic. The width (W) and length (L) of the TFT were 4 and 16 μm , respectively. The a-Si:H TFT has a field-effect mobility of $0.4 \text{ cm}^2/\text{V}\cdot\text{s}$, a threshold voltage of 1.8 V, and a gate leakage current of less than 10^{-13} A . The low leakage current results from the double-gate insulator. In this structure, the SiN_x layer is kept relatively thin, enough to reduce the interface state density between the a-Si:H and the gate insulator and to keep gate leakage low, but not thick enough to cause significant bending of the substrate.

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3

Hydrogenated Amorphous Silicon Thin-Film Transistors

Jerzy Kanicki* and Sandrine Martin

University of Michigan, Ann Arbor, Michigan, U.S.A.

3.1 MOTIVATION

This chapter focuses on issues related to the engineering of high-performance hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) suitable for large-area high-resolution active-matrix liquid crystal displays (AMLCDs). In particular, the underlying physics, numerical simulation, and characterization of a-Si:H TFTs and a-Si:H advanced TFT structures are described.

Ever since the solid-state revolution, silicon-based devices and integrated circuits have replaced most of the conventional circuitry in electronics. The change is so significant that the lives of almost everyone in the world have been affected. Vacuum tubes, once dominant composing elements of electronic appliances such as computers and radios are now historic exhibits and can hardly be seen without going to a museum. However, vacuum tubes have not completely disappeared from our lives. The giant vacuum cathode ray tubes (CRTs) still remain the major information display terminal for television and computers. Yet

* CPOS, University of California, Santa Barbara, California (sabbatical)

the CRT is gradually being replaced by the emerging technology of flat-panel displays (FPDs). The advantages of FPDs are obvious, especially for portable applications such as laptop computers, medical imaging X-ray sensors, and avionic displays. Today, it is also clear that the heavy and bulky CRTs will soon become history just like their other vacuum counterparts. In fact, the commercial battle between CRTs and FPDs is very intense. The main reason for FPDs' not having completely taken over the CRT market is that they cost more than CRTs, but the gap is closing every year. In fact, 2003 is expected to be the first year when FPD revenue will exceed that of CRTs.

Among various FPDs, the dominant product on the market is liquid crystal displays (LCDs). There are two types of LCDs: passive and active addressing modes; the advantages of the former lay in its low cost, while the latter enables high-resolution displays. For active-matrix LCDs, silicon (amorphous or polycrystalline) thin-film transistors serve as the key pixel electrode–switching element. Hydrogenated amorphous silicon is well suited for AMLCDs because it can easily be deposited over large areas at low temperatures that are fully compatible with glass or plastic substrates. In addition, it has a high dark resistivity, leading to TFTs with low leakage currents. Films of a-Si:H can be *n*- or *p*-doped to allow for the fabrication of low-resistance contacts. The processing of a-Si:H TFTs is similar to the crystalline silicon metal oxide–semiconductor (MOS) integrated circuit technology, which makes AMLCDs more mature than other technologies, such as organic displays based on light-emitting devices. Finally, a-Si:H technology benefits from the tremendous investment in a-Si:H solar cells made several years ago, and so has become the dominant player in the active-matrix display world.

3.2 NUMERICAL SIMULATION OF AMORPHOUS SILICON THIN-FILM TRANSISTORS

Since hydrogenated amorphous silicon thin-film transistors were described by LeComber et al. in 1979 [1], they have been widely used as switching devices in active-matrix liquid crystal displays [2]. To improve the electrical performance of a-Si:H TFT for high-resolution AMLCDs, for instance, it was important to evaluate how the a-Si:H density-of-states (DOS) and the TFT source/drain series resistances affect the device electrical performance [3–5]. It was expected that a good understanding of a-Si:H physics combined with the a-Si:H DOS model would substantially reduce the time and cost of a-Si:H TFT process optimization.

Device modeling can be preliminarily divided into two fields: analytical modeling and numerical modeling. In the early days only analytical modeling could be achieved because of limited computer resources for numerical modeling. The advantage of analytical modeling of a-Si:H TFTs [6–9] is that the device performance and design parameters are related by a closed-form equation, helping

the understanding and improvement of the device electrical performance. Furthermore, analytical modeling can be integrated easily into existing CAD tools such as SPICE for circuit simulation. However, for a device with more complicated materials or structures, it is difficult to derive a closed-form equation that can represent the device physics. For instance, it is more difficult to model a-Si:H TFTs analytically than metal oxide–silicon field-effect transistors (MOSFETs) because the a-Si:H large density-of-states makes it difficult to solve Poisson's equation and other differential equations. Furthermore, analytical modeling has difficulty dealing with two- or higher-dimensional structures. Therefore, analytical modeling often has to simplify the device structure into one dimension. However, some structures, such as the a-Si:H TFT with thin semiconductor layer, cannot be simplified into a one-dimensional structure, and any simplifying assumptions made during the derivation will limit the accuracy of obtained results.

Although it is time consuming and difficult to incorporate into circuit simulators, numerical modeling usually provides a more flexible method in the modeling of devices, so different model assumptions may be analyzed and compared. The numerical method resolves basic semiconductor equations such as Poisson's and continuity equations without any simplifications. Based on these equations, the influence of different distributions of density of states and source/drain contact resistances can be analyzed from the point of view of two-dimensional current flow.

3.2.1 Simulation Model

Today the most popular structure for a-Si:H TFTs is the inverted-staggered structure shown in Figure 3.1. The semiconductor layer consists of intrinsic a-Si:H and heavily *P*-doped (n^+) a-Si:H. The gate insulator is usually hydrogenated

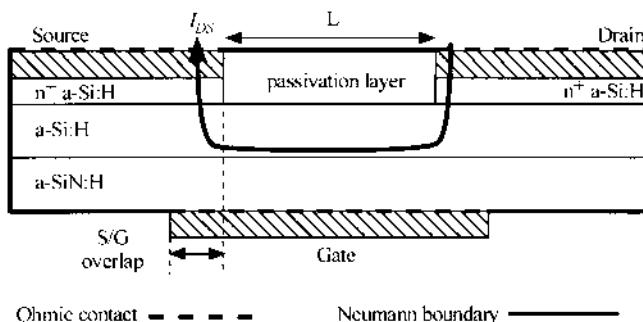


FIGURE 3.1 Cross section of the a-Si:H TFT structure used for numerical simulations. (Adapted from Ref. 19 with permission from Elsevier Science.)

amorphous silicon nitride ($\text{a-SiN}_x\text{:H}$). The inverted-staggered a-Si:H TFT operates in the accumulation mode. When a positive voltage is applied to the gate electrode, the band bending at or near the gate insulator/amorphous semiconductor interface is increased and electrons accumulate near the interface to form the conduction channel. If a positive drain voltage is applied to the drain electrode, the drain–source current flows from the drain to the source electrodes through n^+ a-Si:H , intrinsic a-Si:H , and conduction channel (see Fig. 3.1).

If the electrostatic potential and quasi-Fermi levels are known as a function of position, all the physical phenomena can be determined. To calculate these three variables, the two-dimensional Poisson's equation and continuity equations are solved simultaneously [10]. Poisson's equation is given by

$$\nabla \cdot (\epsilon \nabla \psi) = q[p - n - (N_A^- - N_D^+)] \quad (3.1)$$

where ϵ is the permittivity of a-Si:H , ψ is the electrostatic potential, q is the electronic charge, p and n are electron and hole concentrations, respectively, and N_A^- and N_D^+ are the concentrations of ionized acceptor-like and donor-like states, respectively.

The continuity equations for electrons and holes, respectively, are as follows:

$$-\frac{1}{q} \nabla \cdot J_n = G_n - R_n \quad (3.2)$$

$$\frac{1}{q} \nabla \cdot J_p = G_p - R_p \quad (3.3)$$

where J_n and J_p are the current density for electrons and holes, respectively, G_n and G_p are the generation rates ($\text{cm}^{-3}\text{s}^{-1}$) for electrons and holes, respectively, and R_n and R_p are the recombination rates ($\text{cm}^{-3}\text{s}^{-1}$) for electrons and holes, respectively. The net recombination rate through every defect state is given by the Shockley–Read–Hall formulation [11].

The two-dimensional a-Si:H TFT structure is decomposed into a discrete mesh structure by the finite-element method. Grid points are placed nonuniformly and depend on the estimated distribution of carrier concentrations. The area near the $\text{a-Si:H}/\text{a-SiN}_x\text{:H}$ interface and the source/drain-gate overlap have denser grid points. A larger number of grid points can improve the accuracy of simulation but will also increase computation time. To ensure an acceptable compromise, the number of grid points is increased until the simulation results are within 2% of variations: for a 10 μm -channel-length a-Si:H TFT, the total number of grid points in our device structure is about 800. Once the grid points are determined and drain and gate voltages are set, the simulation program resolves the nonlinear partial differential equations (Poisson's equation, electron and hole continuity equations) using Newton's method [10] and ψ , n , and p as unknowns. All the physical parameters, such as current, electrostatic potential, electron concentra-

tion, hole concentration, electrical field, and energy band bending, can be calculated.

3.2.1.1 Boundary Conditions

Two types of boundary conditions are used in this simulation: ohmic contact and Neumann (reflective) boundary. These boundaries are illustrated in [Figure 3.1](#). The contacts between source/drain metal and n^+ a-Si:H, and gate metal and gate insulator interfaces are assumed to be ohmic. On the other hand, the outer edges of a-Si:H TFT are assigned to be Neumann boundaries. Ohmic contacts are considered as simple Dirichlet boundaries, where the boundary fixes the electrostatic potential and the electron and hole concentrations along the boundary. For a given specific contact resistance (R_c in $\Omega\text{-cm}^2$), the electrostatic potential ψ is determined by

$$\psi = \psi_{\text{ref}} + V_a - \frac{R_c}{A} I_a \quad (3.4)$$

where A is the area of the boundary, $\psi_{\text{ref}} = E_c - E_F/q$ at the terminal, E_F is the Fermi-level position, V_a is the terminal voltage, and I_a is the terminal current.

On the other hand, the outer edges of the a-Si:H TFT are assumed to be limited by the Neumann boundary conditions, so the current flows out of the device only through the drain and source contacts. Assuming no surface charges on such edge, the normal components of the electrostatic potential and carrier concentration gradients are set to zero:

$$\frac{\partial \psi}{\partial \hat{r}} = \frac{\partial n}{\partial \hat{r}} = \frac{\partial p}{\partial \hat{r}} = 0 \quad (3.5)$$

where \hat{r} is the direction perpendicular to the external boundary.

Traditionally, the MOSFET boundary conditions are based on the semi-infinite semiconductor assumption; i.e., the width of the space-charge regions (or the effective Debye length) is much smaller than the thickness of the semiconductor, and the band bending decreases to zero in the bulk of the semiconductor layer ($d\psi/dy = 0$ and $\psi = 0$ at $y = t_{\text{a-Si:H}}/2$). However, these boundary conditions are not always applicable to a-Si:H thin-film transistors [12–14]. Thin a-Si:H layers (500–2500 Å) and low free-carrier density will allow the depletion region to extend over the entire semiconductor layer. Thus the traditional boundary conditions at the interface between the a-Si:H and the passivation layer cannot be applied to a-Si:H TFTs.

The set of the three-coupled nonlinear partial differential Eqs. (3.1), (3.2), and (3.3) are numerically solved for every grid point at given drain, source, and gate biases. Examples of the simulated static transfer characteristic in linear and

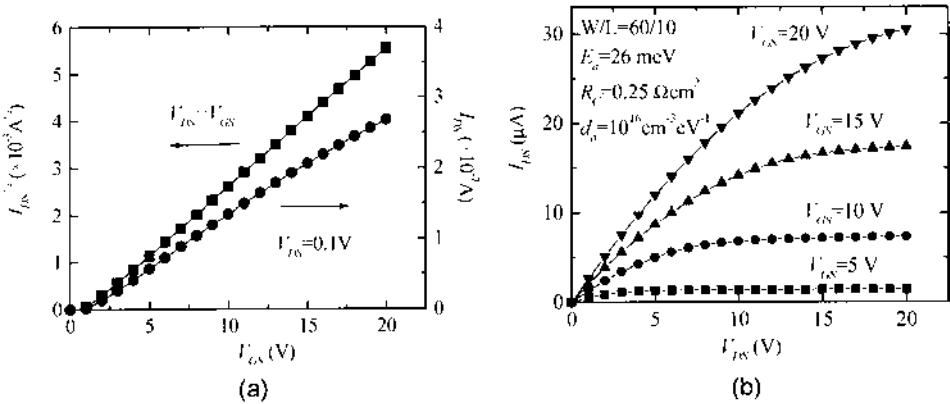


FIGURE 3.2 (a) Simulated transfer characteristics in linear and saturation regimes. (b) Simulated output characteristics. (From Ref. 15.)

saturation regimes are shown in Figure 3.2a [15]. The field-effect mobility (μ_{FE}) and threshold voltage (V_T) were extracted in linear and saturation regions [16] using the gradual channel approximation equations:

$$I_{DS} = \frac{\mu_{FE} C_i W}{L} (V_{GS} - V_T) V_{DS} \quad (3.6)$$

for $V_{DS} = 0.1$ V (linear region), and

$$I_{DS} = \frac{\mu_{FE} C_i W}{2L} (V_{GS} - V_T)^2 \quad (3.7)$$

for $V_{DS} = V_{GS}$ (saturation region), where C_i is the gate insulator capacitance per unit area, L is the channel length, W is the channel width, V_{GS} is the gate-source voltage, and V_{DS} is the drain-source voltage. An example of output characteristics is shown in Figure 3.2b.

3.2.1.2 Amorphous Silicon Density-of-States Model

The model of the density-of-states for a-Si:H proposed by Davis and Mott [17] is adopted in this simulation. The states present in the a-Si:H electronic gap consist of two types: band-tail states and deep-gap states. For numerical simulation, the continuous distributions of both acceptor- and donor-like states within the mobility gap was approximated by several discrete energy states. A total number of

90 discrete energy states with an 0.02 eV interval constitutes a trade-off between accuracy and computation time.

The distributions of band-tail states are given by Eqs. (3.8) and (3.9):

$$g_{CBA} = g_{ta} \exp\left(\frac{E - E_c}{E_a}\right) \quad (3.8)$$

$$g_{VBD} = g_{td} \exp\left(-\frac{E - E_v}{E_d}\right) \quad (3.9)$$

where g_{ta} and g_{td} are the densities of acceptor- and donor-like tail states at $E = E_c$ and $E = E_v$, respectively, and E_a and E_d are the characteristic slopes of the conduction- and valence-band tails, respectively. The valence-band-tail states are below the Fermi level and have negligible influence on a-Si:H TFT electrical characteristics in the ON-state. This is not the case for the conduction-band-tail states, which can significantly affect the a-Si:H TFT electrical performance. Transfer characteristics in the saturation region calculated for different E_a values are shown in Figure 3.3a: the corresponding μ_{FE} decreases and V_T increases when E_a increases. We should note that the lower E_a values are associated with a-Si:H film having an enhanced short-range order.

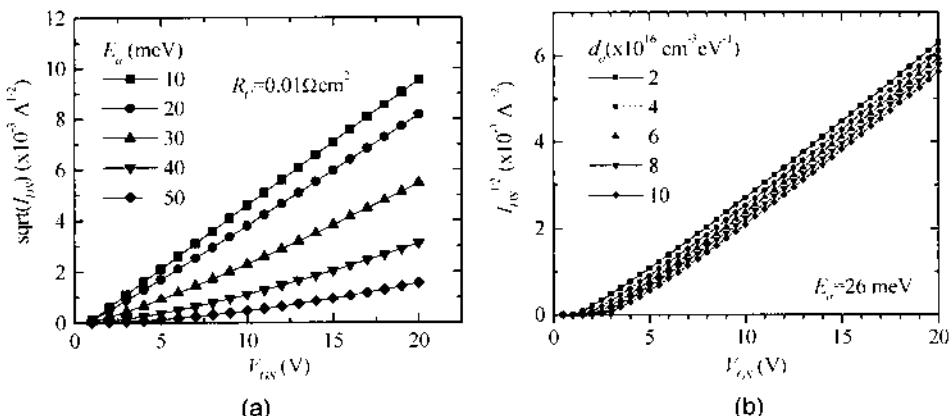


FIGURE 3.3 Simulated transfer characteristics in the saturation regime for (a) different conduction-band-tail slopes and (b) different peak values of deep-gap states. (From Ref. 15.)

The deep-gap states are modeled by two Gaussian-like distributions representing the donor- and acceptor-like traps:

$$g_{DGa} = d_a \exp\left(-\frac{(E - \lambda_a)^2}{\sigma_a^2}\right) \quad (3.10)$$

$$g_{DGD} = d_d \exp\left(-\frac{(E - \lambda_d)^2}{\sigma_d^2}\right) \quad (3.11)$$

where d_a and d_d are the peak values of the Gaussian distribution of acceptor- and donor-like deep-gap states, respectively, λ_a and λ_d are the mean energies of the Gaussian distributions of acceptor- and donor-like states, respectively, and σ_a and σ_d are the standard deviations of the Gaussian distributions of acceptor- and donor-like states, respectively. The description and default values for these equations and typical geometry parameters used in this simulation are listed in [Table 3.1](#).

Simulated transfer characteristics are plotted in Figure 3.3b for peak values of deep-gap states, d_a ranging from 2×10^{16} to $10^{17} \text{ cm}^{-3}\text{eV}^{-1}$. The TFT field-effect mobility is not affected, but the threshold voltage increases with increasing d_a .

3.2.1.3 Source and Drain Contact Resistances

Based on the current flow shown in Figure 3.1, the a-Si:H TFT source/drain series resistances consist of three parts: (1) the specific contact resistances between the source/drain metal electrodes and the n^+ a-Si:H layers; (2) the resistances of n^+ a-Si:H film; and (3) the resistances due to the intrinsic a-Si:H layers between the source/drain n^+ a-Si:H layers and the conducting channel (a-Si:H/a-SiN_x:H interface). Parts (2) and (3) will be discussed in section 3.3.4.

In general, the contact resistance depends on the specific contact resistance (R_C) and the contact area. Today R_C is limited by the poor doping efficiency of n^+ a-Si:H, and it is about $0.1\text{--}1 \Omega\text{-cm}^2$ with current a-Si:H TFT technology. For a given source/drain metallurgy, one way to reduce the contact resistance is to increase the doping efficiency of n^+ a-Si:H. Kanicki [18] showed that when the n^+ a-Si:H film resistivity (R_f) is reduced from 100 to 10 $\Omega\text{-cm}$, the R_C decreases from 30 to 0.1 $\Omega\text{-cm}^2$. The experimental relation between R_f (in $\Omega\text{-cm}$) and R_C (in $\Omega\text{-cm}^2$) for Mo/ n^+ a-Si:H contacts can be described by [18]

$$\log(R_c) = -1 + 1.25 \log(R_f) \quad (3.12)$$

For large R_C , a nonnegligible portion of the applied drain voltage drops on the high source/drain contact resistances, leading to a reduced field-effect mobility [19].

TABLE 3.1 Parameters Used for the Numerical Simulations, Unless Specified Otherwise

Parameter	Value	Description
λ_a (eV)	0.98	Mean value of Gaussian-distributed acceptor-like deep-gap states
σ_a (eV)	0.2	Variance of the Gaussian-distributed acceptor-like deep-gap states
λ_d (eV)	0.56	Mean value of the Gaussian-distributed donor-like deep-gap states
σ_d (eV)	0.17	Variance of the Gaussian-distributed donor-like deep-gap states
σ_n (cm^2)	10^{14}	Electron capture cross section of the conduction-band-tail states
μ_{n0} (cm^2/Vs)	8	Electron mobility in conduction-band extended states
σ_p (cm^2)	10^{14}	Hole capture cross section of the valence-band-tail states
μ_{p0} (cm^2/Vs)	6	Hole mobility in valence-band extended states
ϵ_{SiN}	6.9	Dielectric constant of the gate insulator
d_a ($\text{cm}^{-3}\text{eV}^{-1}$)	10^{16}	Peak value of Gaussian-distributed acceptor-like deep-gap states
d_d ($\text{cm}^{-3}\text{eV}^{-1}$)	10^{16}	Peak value of Gaussian-distributed donor-like deep-gap states
E_a (meV)	26	Conduction-band-tail characteristic energy
E_d (meV)	55	Valence-band-tail characteristic energy
E_G (eV)	1.8	Band gap of a-Si:H
g_a ($\text{cm}^{-3}\text{eV}^{-1}$)	10^{21}	Density of states at E_c
g_d ($\text{cm}^{-3}\text{eV}^{-1}$)	10^{21}	Density of states at E_v
L (μm)	10	Channel length
d (μm)	3	Source/drain gate overlap
R_c (Ωcm^2)	0.25	Source/drain specific contact resistances
R_t (Ωcm)	1.25	n^+ a-Si:H film resistivity
$t_{\text{a-Si:H}}$ (μm)	0.25	a-Si:H film thickness
t_{nSi} (μm)	0.07	n^+ a-Si:H film thickness
$t_{\text{a-Si:N}}$ (μm)	0.35	a-SiN _x :H (gate insulator) film thickness
W (μm)	60	Channel width

3.2.2 Temperature Effect on Amorphous Silicon Thin-Film Transistors

Transfer characteristics simulated at different temperatures ranging from 300 to 420 K at $V_{DS} = 0.1$ V show temperature-activated behavior, and the field-effect activation energy E_{act} can be calculated from the Arrhenius plot, i.e., the slope of $\log(I_{DS})$ versus I/T plot at a given V_{GS} .

An increase in the density of the deep-gap states causes only a threshold voltage shift and consequently no change of the $E_{act} - V_{GS}$ curve above threshold [20]. On the other hand, the conduction-band-tail has a significant effect on the activation energy curve. Figure 3.4 shows the $E_{act} - V_{GS}$ curves calculated for various conduction-band-tail slopes. The field-effect activation energy clearly increases with increasing density of conduction-band-tail states. An increase of the energy difference between the conduction-band edge and the Fermi level (at 0 K) can also be observed [21].

An experimental result is also given in Figure 3.4: Simulation cannot explain the experimental curve. This can be achieved by considering the temperature dependence of the source/drain series resistance. By adding temperature activated behavior of the S/D contact resistances and resistances of the n^+ a-Si:H layers, good fit can be obtained between the experimental and simulated field-effect activation energy curves [21].

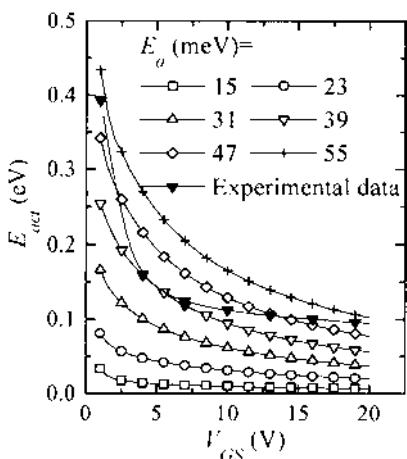


FIGURE 3.4 Simulated evolution of the a-Si:H TFT field-effect activation energy for various conduction-band-tail slopes. (From Ref. 15.)

3.2.3 Amorphous Silicon Thin-Film Transistors Under Illumination

The numerical simulation program developed for the analysis of the a-Si:H TFT under illumination [22,23] is similar to the one described earlier, used in the dark. It solves simultaneously the three equations describing the steady-state conduction in semiconductors: the Poisson equation, electron and hole continuity equations, out of thermal equilibrium, using the Shockley–Read model for the carrier recombination rate. The amorphous silicon density-of-states is modeled by two exponential band tails and two Gaussian distributions of monovalent states, where the recombination process takes place. The program takes into account the a-Si:H density-of-states at the interfaces (a-Si:H/a-SiN_x:H and back-channel interfaces) and in the bulk of the semiconductor. The gate insulator is assumed to be ideal; i.e., there is no charge trapping or fixed charge present in the insulator layer. The TFT is illuminated from the source–drain side, and we assume that the whole a-Si:H layer is exposed to the light. The spatial resolution of the three-equation set is achieved over the whole a-Si:H TFT structure by defining an irregular 2D mesh, thinner at the interfaces between two different layers. For each set of input conditions (voltages and illumination conditions), we obtain, at every node of the 2D mesh, the values of the three unknowns: electrostatic potential and electron and hole Fermi potentials. These values allow us to deduce 2D maps of the physical parameters, such as the current densities, carrier densities, and electric field.

Figure 3.5 shows the TFT transfer characteristics simulated in the dark and under a uniform monochromatic illumination. We can distinguish both the a-Si:H TFT electron and hole threshold voltages, which delimit three main TFT operating regimes [24]:

- (I) electron accumulation layer created at the a-Si:H/a-SiN_x:H interface;
- (II) no accumulation layer;
- (III) hole accumulation layer created at the a-Si:H/a-SiN_x:H interface.

In regime (I), the TFT drain current is associated with the drift diffusion of electrons in the accumulation layer (conduction channel). In regime (II), the TFT drain current results from the same mechanism as in regime (I), but the conduction occurs uniformly in the whole amorphous silicon layer (channel and bulk), since there is no carrier accumulation at the a-Si:H/a-SiN_x:H interface. Because the carrier densities in the whole amorphous silicon layer depend mostly on the light-induced generation and carriers recombination rates, in this regime the TFT drain current is sensitive to the amorphous silicon thickness and to the bulk density of states of amorphous silicon. In regime (III), the existence of the hole accumulation layer at the a-Si:H/a-SiN_x:H interface, in combination with

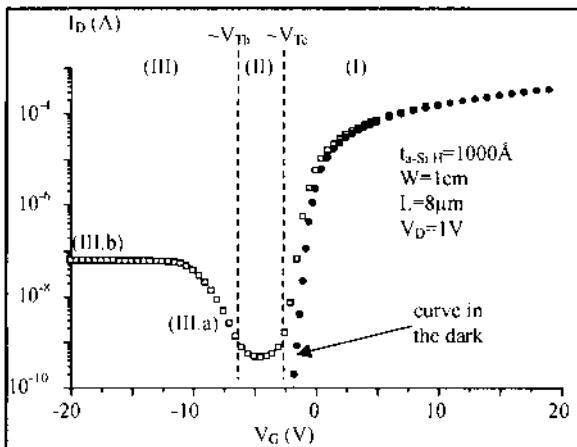


FIGURE 3.5 Simulated a-Si:H TFT transfer characteristics under illumination and in the dark. (From Ref. 23, with permission from Society for Information Display.)

the $n+$ a-Si:H source/drain contact layers, results in a situation similar to two a-Si:H pn junctions located at the source and drain access areas. For a positive drain voltage, the source and drain junctions are, respectively, in the ON- and OFF-state.

We can actually distinguish two different conduction regimes within regime (III): In regime (III.a), the TFT current increases with the magnitude of the gate voltage, while it reaches a plateau in (III.b). The distinction between these two regimes depends on the relative importance of two different physical mechanisms: In regime (III.a), the drift diffusion of holes in the accumulation layer (conduction channel) is predominant, whereas in regime (III.b) the recombination of electrons and holes in the drain (OFF-state) pn junction depletion region is the most important. We should note that the importance of the source junction has been mentioned in [25], but we do not think that it is critical in regimes (III.a) and (III.b). Figure 3.6 shows the simulated variations of the electron and hole Fermi potentials along the usual TFT current path between the source and drain contacts. We can see that, in regime (III.a) (here for $V_G = -7.5$ V), the main variation of the Fermi potentials happens in the accumulation layer, where the drift diffusion of holes occurs. The conduction in this regime is similar to the conduction when the TFT is in the accumulation regime (gate voltage larger than the electron threshold voltage); however, in this regime the majority carriers are the holes

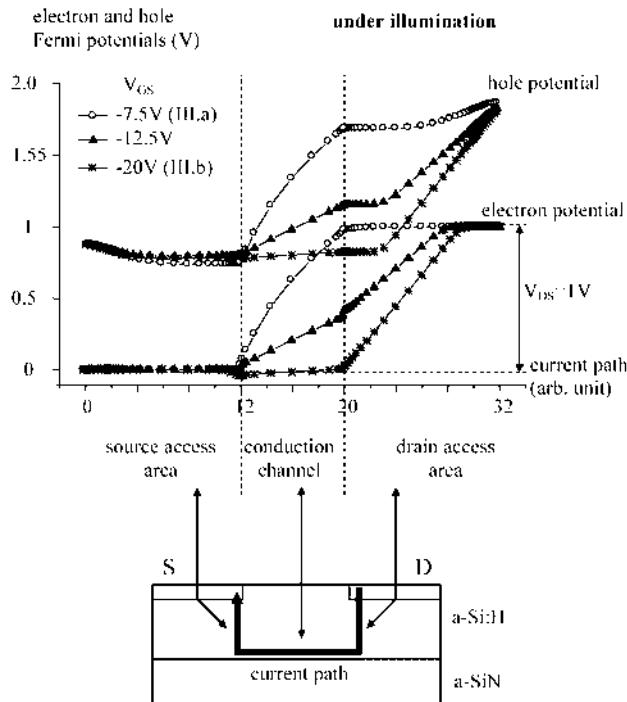


FIGURE 3.6 Simulated variations of the electron and hole Fermi potentials along the main TFT current path under illumination. (From Ref. 24.)

instead of the electrons. In contrast, in regime (III.b) (here for $V_G = -20$ V), the main variation of the Fermi potentials occurs in the drain pn junction depletion region, where the recombination of electrons and holes is taking place. Photogenerated current at the drain junction is the lowest [25] and is therefore the bottleneck in the process. Consequently, the a-Si:H TFT current depends only on the light-induced generation and recombination of electrons and holes in the drain pn junction depletion region. Actually, for high negative voltages, the recombination rate can be neglected, and the TFT current is therefore set only by the light-induced generation of electrons and holes (as in a photodiode case). This can explain why, in this regime, there is no longer any influence of the gate voltage (saturation phenomenon) or channel length on the TFT drain current as observed experimentally [23]. However, we should note that this saturation regime is not always reached for typical values of the gate voltage.

The parameters that influence the a-Si:H TFT drain current depend on the TFT operation regime to be considered. The electron and hole threshold voltages depend mostly on the amorphous silicon density-of-states associated with both the a-Si:H/a-SiN_x:H interface and the bulk a-Si:H; the difference between the two threshold voltages is higher for a larger density-of-states. In regime (II), the TFT drain current depends strongly on the amorphous silicon thickness but also on the a-Si:H bulk density-of-states; it increases with a-Si:H thickness and decreases with a-Si:H density-of-states. The drain current in regime (III.b) depends only on the light-induced generation of electron–hole pairs in the drain *pn* junction depletion region (between the drain contact and the a-Si:H/a-SiN_x:H interface); it increases with the illumination intensity and with the *pn* junction area.

3.3 AMORPHOUS SILICON THIN-FILM TRANSISTOR CHARACTERIZATION

3.3.1 Normalization of Thin-Film Transistor Characteristics

a-Si:H TFT transfer characteristics need to be normalized to accurately compare samples with different geometric parameters and/or different gate insulators [26]. First, in order to take into account the geometrical dependence of the TFT characteristics in the linear regime, we should use the normalized TFT conductance (in Ω^{-1}) instead of the TFT drain current:

$$G = \frac{I_{DS}}{V_{DS}W/L} \quad (3.13)$$

where V_{DS} is the source–drain voltage and W and L are the TFT channel width and length, respectively.

Then instead of the gate voltage, we should use the electrical charge induced by the gate voltage at the amorphous semiconductor/gate insulator interface (in C/cm²):

$$Q_{\text{ind}} = V_{GS} \times C_i \quad (3.14)$$

where C_i is the insulator capacitance per unit area. Alternatively, we can use G/C_i versus V_{GS} characteristics for the analysis of the TFT linear regime.

In the TFT saturation regime, we should use the normalized TFT current expressed by

$$I_{DS\text{norm}} = \frac{I_{DS}}{C_i W / 2L} \quad (3.15)$$

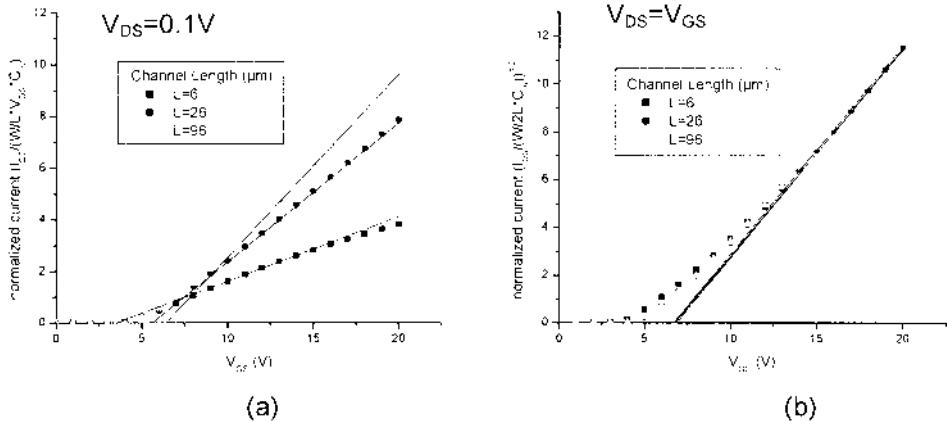


FIGURE 3.7 Normalized a-Si:H TFT transfer characteristics and fitting used for extraction of the field-effect mobility and threshold voltage in the (a) linear and (b) saturation regimes.

Examples of normalized TFT characteristics in linear and saturation regimes are shown in Figure 3.7a and b, respectively.

3.3.2 Extraction of Thin-Film Transistor Electrical Parameters

The most basic TFT characterization involves the extraction of field-effect mobility, threshold voltage, and subthreshold swing. To obtain meaningful extracted TFT electrical parameters, the fitting range must be chosen carefully to ensure that devices with different geometry, gate insulator characteristics, or measurement conditions are compared in the same operating states, which do not necessarily occur at comparable gate voltage ranges.

In the linear regime, i.e., for low drain voltage, the TFT apparent field-effect mobility μ_{FE} and threshold voltage V_T are deduced from the following equation, using the MOSFET gradual channel approximation:

$$\frac{I_{DS}}{V_{DS}C_i W/L} = \mu_{FE} (V_{GS} - V_T) \quad (3.16)$$

The fit of the experimental data to Eq. (3.16), as shown in Figure 3.7a, is performed around a fixed value of the normalized drain current $I_{DS}/(V_{DS}C_i W/L)$.

In the saturation regime (typically for $V_{DS} = V_{GS}$), the TFT field-effect mobility and threshold voltage are calculated from the following equation:

$$\frac{I_{DS}}{C_i W/2L} = \mu_{FE}(V_{GS} - V_T)^2 \quad (3.17)$$

The fit of the experimental data to Eq. (3.17), as shown in Figure 3.7b, is performed around a fixed value of the normalized drain current $I_{DS}/(C_i W/2L)$.

In addition, the normalized threshold voltage $V_T \times C_i$ should be used instead of the threshold voltage, to allow for comparison of devices with different gate insulator characteristics.

The subthreshold swing (S) is usually extracted from the TFT transfer characteristic in the subthreshold regime, using the following equation:

$$S = \left(\frac{d \log (I_D)}{d V_{GS}} \right)^{-1} \quad (3.18)$$

The fit of the experimental data to Eq. (3.18), as shown in Figure 3.8, is performed around a fixed value of $I_{DS}/(V_{DS}W/L)$. $I_{DS}/(V_{DS}W/L)$ can also be used in Eq. (3.18). From the value of the subthreshold slope, we can also calculate the equiva-

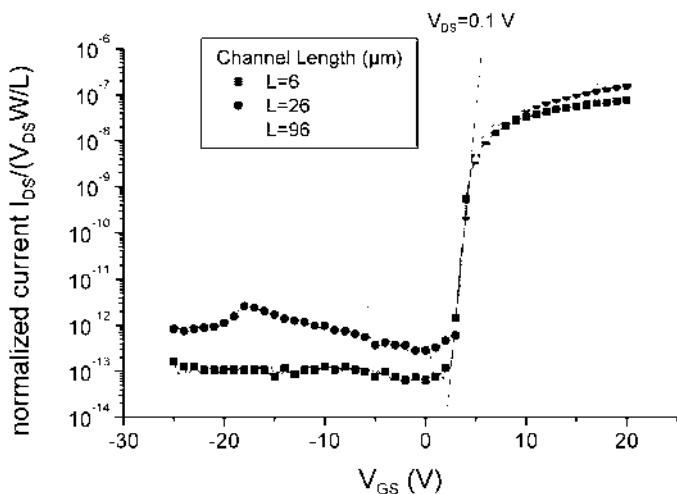


FIGURE 3.8 a-Si:H TFT transfer characteristics and fitting used for extraction of the subthreshold swing.

lent maximum density-of-states that can be present at the amorphous semiconductor/gate insulator interface [27]:

$$N_{ss}^{\max} = \left(\frac{S \log(e)}{kT/q} - 1 \right) \frac{C_i}{q} \quad (3.19)$$

where q is the electron charge, k is the Boltzmann constant, and T is the temperature. N_{ss}^{\max} can be used to compare devices with different gate insulator characteristics.

In the linear regime, the MOSFET equation predicts that, for low V_{DS} , a linear $I_{DS} - V_{GS}$ characteristic should be observed. However, $I_{DS} - V_{GS}$ characteristics of TFTs often exhibit a nonlinear behavior inconsistent with the predictions of the MOSFET gradual channel equation, as seen, for example, in Figure 3.9. This deviation from the ideal MOSFET behavior [9,16,28,29] has been associated with dispersive transport in a-Si:H [30]. More precisely, the device model was modified to include an additional parameter, γ , representative of the $I_{DS} - V_{GS}$ nonlinearity at low V_{DS} , as follows:

$$I_{DS} = M(V_{GS} - V_T)^\gamma V_{DS} \quad (3.20)$$

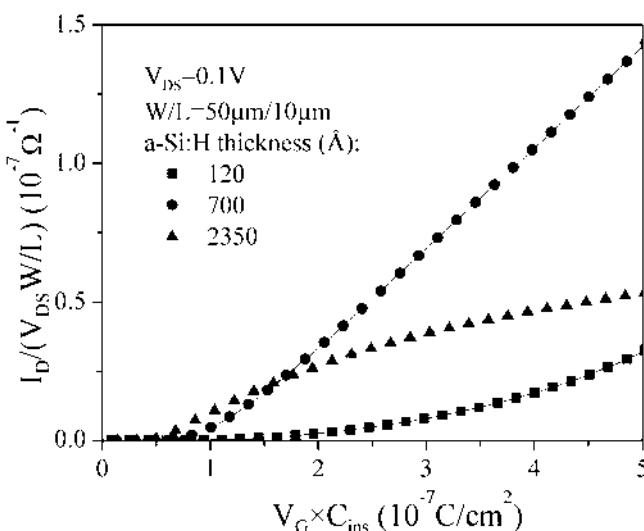


FIGURE 3.9 a-Si:H TFT transfer characteristics in the linear regime exhibiting significant nonlinearity.

where $M = \mu_{FE} C_i (W/L)$. The physical signification of γ is often given by

$$\gamma = 2 \frac{T_0}{T} - 1 \quad (3.21)$$

where T_0 is the characteristic temperature of the amorphous semiconductor density-of-states distribution around the position of the Fermi level [16], i.e., typically the characteristic temperature of the conduction-band-tail states. The equation is valid for $T < T_0$. The nonideal situation of $\gamma > 1$ is associated with a high density of conduction-band-tail states, which can usually be attributed to variations of the Si–Si bond angles and distances in the amorphous semiconductor. However, γ can be significantly underestimated in the case of nonnegligible source and drain series resistances [31].

We should note that, when the TFT parameter extraction is performed using Eq. (3.20), the unit of the term $\mu_{FE} C_i (W/L)$ is $A/V^{\gamma+1}$ (instead of A/V^2 as in the case of the MOSFET-based equation) and consequently depends on the value of γ . Therefore, to ensure proper comparison between samples with different γ -values, the TFT field-effect mobility and threshold voltage are extracted using Eq. (3.16), i.e., based on the MOSFET gradual channel approximation. Eq. (3.20) was used separately for the extraction of the γ -parameter only.

3.3.3 Thin-Film Transistor Source/Drain Series Resistances

The complete analysis of a-Si:H TFT electrical performance also involves the extraction of the TFT source and drain series resistances, the intrinsic field-effect mobility, and intrinsic threshold voltage. The intrinsic a-Si:H TFT parameters are representative of the electrical characteristics of the conduction channel itself without the influence of the parasitic series resistances. They can be extracted by the well-known transmission line method (TLM) [32,33] using a series of TFTs with different channel lengths measured at a low source–drain voltage, so we can neglect the space-charge-limited currents (SCLC) effect.

The total TFT ON-resistance is:

$$R_T = \frac{V_{DS}}{I_{DS}} = r_{ch} L + 2R_{S/D} \quad (3.22)$$

where r_{ch} is the channel resistance per channel-length unit and $2R_{S/D}$ is the total (source + drain) series resistances, respectively. Using Eqs. (3.16) and (3.22), we can express the total TFT ON-resistance R_T as a function of the TFT apparent field-effect mobility and threshold voltage:

$$R_T = \frac{L}{\mu_{FE} C_i W(V_{GS} - V_T)} \quad (3.23)$$

The same equation applied to the ideal TFT (conduction channel only) lets us express the channel resistance as a function of the intrinsic mobility and threshold voltage, μ_{FEi} and V_{Ti} , which are representative of the conduction channel material, without the influence of the TFT series resistances:

$$r_{ch} = \frac{1}{\mu_{FEi} C_i W(V_{GS} - V_{Ti})} \quad (3.24)$$

The extraction of the TFT source and drain series resistances and intrinsic field-effect mobility and threshold voltages is rather straightforward using a series of TFTs with different channel lengths, as shown in Figure 3.10. We first plot the total TFT ON-resistance as a function of the TFT channel length for different gate voltages, ensuring that the TFT is in accumulation regime, and then we fit the experimental data to linear curves. This lets us obtain the TFT total series resistances ($R_S + R_D$) from the y-intercepts and the channel resistance per channel-length unit (r_{ch}) from the slopes. By plotting the reciprocal of r_{ch} as a function of the gate voltage and, once again, determining its linear fit, the x-intercept gives the intrinsic threshold voltage V_{Ti} and the slope yields the intrinsic field-effect mobility μ_{FEi} as indicated by Eq. (3.24).

The TFT series resistances are closely related to the overlap between source (or drain) contact and gate contact. The TFT drain current does not usually flow

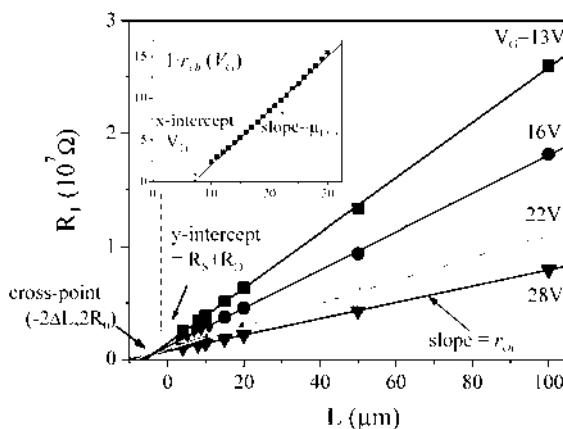


FIGURE 3.10 Illustration of the transmission line method used to extract the S/D series resistances and the a-Si:H TFT intrinsic parameters. The total ON-resistance R_T has been plotted as a function of the TFT channel length for different gate voltages. The inset shows the evolution of $1/r_{ch}$ with the TFT gate voltage. Symbols: experimental results; solid lines: linear fits. (Adapted from Ref. 26)

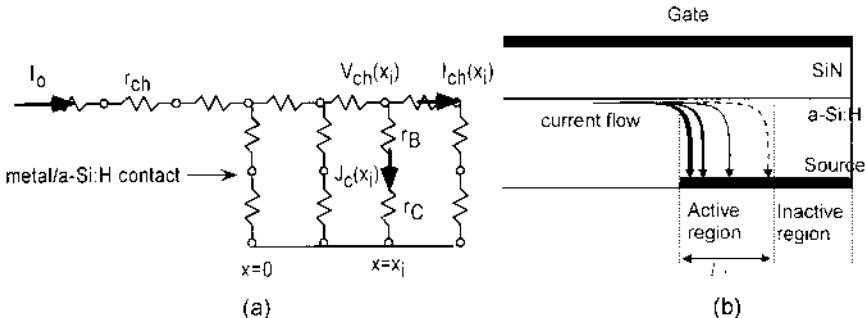


FIGURE 3.11 (a) Equivalent circuit near and above the a-Si:H TFT source electrode. (Adapted from Ref. 39.) (b) Representation of the characteristic length L_T . (From Ref. 23.)

through the whole source or drain contact but is more likely limited to a specific area of the contact [34–36]. More precisely, we can define the TFT characteristic length (L_T) representing the dimension (along the source–drain axis) of the effective contact area. Figure 3.11 illustrates the top-gate a-Si:H TFT cross section and simplified schematic circuit diagram at the source contact. At the source-electrode side, the change of the channel current above the source electrode can be expressed as

$$\frac{dI_{ch}(x)}{dx} = -WJ_c(x) \quad (3.25)$$

with

$$J_c(x) = V_{ch}(x)/r_{Ceff} \quad (3.26)$$

and

$$r_{Ceff} = r_B + r_C \quad (3.27)$$

where $I_{ch}(x)$ is the horizontal current in the channel (a-Si:H/a-SiN_x:H interface) at position x , $J_c(x)$ is the vertical current density at position x , $V_{ch}(x)$ is the electrical potential in the channel at position x , and r_B and r_C are the vertical bulk and contact resistivity (in $\Omega\text{-cm}^2$), respectively.

The variation of $V_{ch}(x)$ along x can be expressed as

$$\frac{dV_{ch}(x)}{dx} = -I_{ch}(x)r_{ch} \quad (3.28)$$

Combining Eqs. (25), (26), and (27), we have

$$\frac{d^2V_{\text{ch}}(x)}{dx^2} = \frac{1}{L_T^2} V_{\text{ch}}(x) \quad (3.29)$$

with

$$L_T^2 = \frac{r_{\text{Ceff}}}{W r_{\text{ch}}} \quad (3.30)$$

where L_T is the characteristic length of the source (drain) series resistance at a fixed V_{GS} .

The boundary conditions for Eq. (2.28) are

$$\left. \frac{dV_{\text{ch}}(x)}{dx} \right|_{x=0} = -I_0 r_{\text{ch}} \quad (3.31)$$

and

$$\left. \frac{dV_{\text{ch}}(x)}{dx} \right|_{x=d} = 0 \quad (3.32)$$

where I_0 is the total TFT drain-to-source current.

We can solve Eq. (3.29) for $V_{\text{ch}}(x)$ analytically:

$$V_{\text{ch}}(x) = I_0 r_{\text{ch}} L_T \frac{\cosh[(x-d)/L_T]}{\sinh(d/L_T)} \quad (3.33)$$

The series resistance $R_{S/D}$ (in ohms) at the source or drain contact can then be expressed as

$$R_{S/D} = \frac{V_{\text{ch}}(x=0)}{I_0} = r_{\text{ch}} L_T \coth\left(\frac{d}{L_T}\right) \quad (3.34)$$

and

$$L_T = \frac{R_{S/D}}{r_{\text{ch}} \coth(d/L_T)} \quad (3.35)$$

The values of $R_{S/D}$ and r_{ch} are determined experimentally from Eqs. (3.22) and (3.24), respectively. Therefore, L_T can be calculated by solving Eq. (3.35) numerically. Furthermore, if $d/L_T \gg 1$, Eq. (3.35) can be reduced to

$$L_T = \frac{R_{S/D}}{r_{\text{ch}}} \quad (3.36)$$

and from Eq. (3.30) we can obtain the effective contact resistance:

$$r_{\text{Ceff}} = W L_T^2 r_{\text{ch}} = \frac{W R_{S/D}^2}{r_{\text{ch}}} \quad (3.37)$$

It can be shown that, as expected for a-Si:H TFTs, r_{Ceff} and L_T vary with V_{GS} in

Eq. (3.35) through Eq. (3.37). Assuming that r_C is V_{GS} independent, this variation can be associated with a variation of series bulk resistivity (r_B) with V_{GS} . Thus, we can approximate the source/drain contact resistivity (in $\Omega\text{-cm}^2$) by

$$r_C = R_{C\text{eff}}|V_{GS} >> 0 \quad (3.38)$$

if the bulk resistivity r_B is assumed to be negligible, as compared to r_C , at high V_{GS} for TFTs with thin a-Si:H layers. Taking this assumption into consideration, the r_C -value that we obtain ($0.18 \Omega\text{-cm}^2$ for top-gate a-Si:H TFTs) is smaller than the one calculated by assuming a uniform conduction through the contact area ($1 \Omega\text{-cm}^2$ for top-gate a-Si:H TFTs) [36]. This difference is associated with the difference between the characteristic length L_T and the source/drain contact width used in respective calculations of r_C . Therefore, the vertical current flow at the source (or drain) contact is effectively confined within a distance of about L_T from the edge of the contact.

The characteristic length L_T increases with the amorphous silicon thickness, the a-Si:H bulk density-of-states, and the source and drain contact resistances [23]. It is a critical parameter for designing TFTs. It is clear that, above the L_T -value, the contact dimension (i.e., the overlap between the source or drain contact and the gate contact) has no influence on the parasitic series resistances, since the current does not flow through the further part of the source or drain contact (inactive region). On the contrary, below L_T the whole contact area is active with respect to the current flow: The resistance is roughly proportional to the reciprocal of the contact dimension. Therefore, an increase in the contact dimension results in a reduction of the TFT series resistances and an improvement in the TFT electrical performance. However, we have to keep in mind that an increase of the overlap between the source or drain contact and the gate contact also yields to an increase in the TFT parasitic capacitances that can degrade the TFT performance, especially when used in active-matrix displays and detectors.

It has also been shown that the resistivity of the a-Si:H access region is closely associated with the band profile in the a-Si:H layer between the source (or drain) contact and the conduction channel [37] and therefore depends strongly on both the a-Si:H thickness and the a-Si:H density-of-states. If the a-Si:H density-of-states were constant throughout the electronic gap, the characteristic length of the band bending (potentials variations) would be the Debye length L_D , which can be simply approximated by the following equation:

$$L_D = \sqrt{\frac{\epsilon_{\text{a-Si:H}}}{q^2 \times \text{density-of-states}}} \quad (3.39)$$

where q is the electron electric charge and $\epsilon_{\text{a-Si:H}}$ is the amorphous silicon relative permittivity. Although the actual a-Si:H density-of-states is not constant throughout the electronic gap, the characteristic length L_D defined by Eq. (3.39) can still

be used to describe quantitatively the influence of a-Si:H thickness and density-of-states on the band profile.

The effect of the series resistances can also be partially represented as an increase in the apparent channel length: The total TFT ON-resistance is

$$R_T = \frac{V_{DS}}{I_{DS}} = 2R_{S/D} + \frac{L}{\mu_{FEi}C_iW(V_{GS} - V_{Ti})} \\ = 2R_0 + \frac{L + 2\Delta L}{\mu_{FEi}C_iW(V_{GS} - V_{Ti})} \quad (3.40)$$

where ΔL is independent of the gate voltage and R_0 represents the limit of the source and drain series resistance for a very high gate voltage [32]. ΔL and R_0 are usually extracted from the R_T versus L curves, as shown in [Figure 3.10](#): All the $R_T - L$ curves have a common cross point located slightly away from the y-axis [19,26,32], whose coordinates are ($x = -2\Delta L$, $y = 2R_0$). ΔL is associated with an effective channel length longer than the mask-specified channel length, i.e., the current path extending beyond the source/drain contact edges. It depends significantly on the source and drain contact resistances, as shown by the simulated results plotted in [Figure 3.12](#).

The $I_{DS} - V_{DS}$ characteristics and their derivatives can also be used to evaluate qualitatively the effect of the source and drain series resistances. By plotting the derivative of the $I_{DS} - V_{DS}$ characteristics, we can better visualize the current crowding phenomenon that is associated with high source and drain series resistances. The presence of a significant current crowding results in an

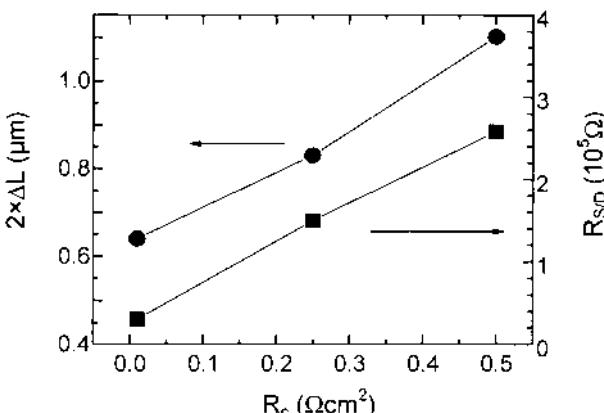


FIGURE 3.12 Simulated evolution of ΔL and $R_{S/D}$ as a function of the source-drain specific contact resistance. (Reprinted from Ref. 19 with permission from Elsevier Science.)

increase in the dI_{DS}/dV_{DS} curve for low V_{DS} values, while the absence of crowding yields a monotonic (decreasing) curve [32].

3.3.4 Gated Four-Probe Amorphous Silicon Thin-Film Transistors

3.3.4.1 Device Structure

Because of their staggered structure, TFTs often suffer from high source and drain series resistances that can affect their intrinsic channel performance, as described earlier. To accurately evaluate the a-Si:H TFT intrinsic properties without the influence of the parasitic series resistances, the gated four-probe TFT (GFP TFT) structure [19,38,39] has been developed by Chen et al. for the first time. This structure can also be called a five-terminal (FT) TFT, an intrinsic point probe MOSFET, or a Kelvin probe TFT.

The GFP TFT is a TFT with two additional narrow electrodes placed between the source and drain contacts (see Fig. 3.13). Such a structure is expected to allow for the evaluation of the potential difference along the conduction channel, assuming that the potential difference is the same at the conduction channel

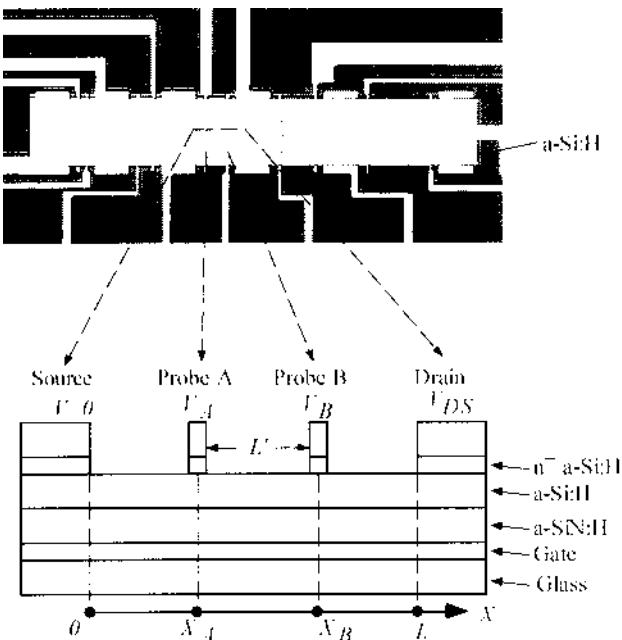


FIGURE 3.13 Top and cross-sectional views of the GFP a-Si:H TFT structure. (From Ref. 38.)

interface (amorphous semiconductor/gate insulator) and at the back interface (passivation layer/amorphous semiconductor). We have shown that, indeed, GFP-TFTs can be used to accurately study TFT conduction channel intrinsic properties [38].

The gradual channel approximation in the linear region is used to describe the a-Si:H TFT electrical characteristics:

$$G = \frac{I_{DS}}{V_{DS}W/L} = \mu_{FE}C_i(V_{GS} - V_T) \quad (3.41)$$

where G is the normalized channel conductance. For the GFP a-Si:H TFT structure, the $G' - V_{GS}$ characteristics are derived from

$$G' = \frac{I_{DS}}{(V_B - V_A)W/L'} = \mu_{FEi}C_i(V'_{GS} - V_{Ti}) \quad (3.42)$$

where G' is the effective normalized channel conductance, V_A and V_B are the potential for the two inner probes; $V_{GS}' = V_{GS} - (V_B + V_A)/2$ is the effective gate bias, and $L' = (X_B - X_A)$ is the GFP effective channel length. Since probes A and B sense only the potential, V_A and V_B are the true potentials at the back channel and we can assume that the difference $V_A - V_B$ is the same as the corresponding potential difference in the conduction channel. Hence, by using the GFP a-Si:H TFT structure, intrinsic field-effect mobility (μ_{FEi}), intrinsic threshold voltage (V_{Ti}) and channel conductance activation energy (E_{act}) can be extracted from Eq. (3.42), without the influence of the TFT source/drain series resistances.

3.3.4.2 Bidimensional Numerical Simulation of Amorphous Silicon Gated Four-Probe Thin-Film Transistors

The 2D Semicad Device simulation program previously described was used to numerically study the effect of the series resistances on a-Si:H TFT and GFP a-Si:H TFT characteristics [38,40]. The $G - V_{GS}$ and $G' - V'_{GS}$ characteristics for a-Si:H TFT and GFP a-Si:H TFT structures have been simulated for different R_C . [Figure 3.14](#) shows the evolution of the extracted field-effect mobility as a function of the channel lengths for three different R_C values for a-Si:H TFT and GFP a-Si:H TFT structures. As expected, the field-effect mobility of the conventional TFT decreases with decreasing channel length and increasing R_C values. On the other hand, since R_C has no influence on $G' - V'_{GS}$ characteristics of the GFP a-Si:H TFT structure, the field-effect mobility does not change with the GFP TFT effective channel length.

The electrical characteristics of real GFP TFTs have been studied by adding two additional probes (A and B) to the standard TFT design. It is assumed that

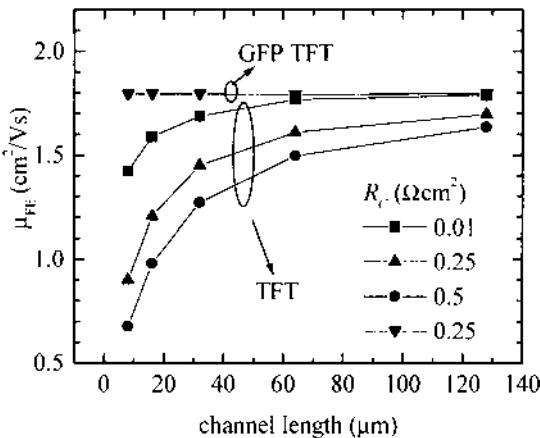


FIGURE 3.14 Simulated evolution of the field-effect mobility and the threshold voltage as a function of the channel length for a-Si:H TFT and GFP a-Si:H TFT structures having different R_c values. (From Ref. 15.)

these contacts are ohmic and that no current flows through these probes. The GFP and conventional TFT conductances (G' and G) were calculated using the same equations that have been used for experimental data. It has been verified that, for the typical a-Si:H thicknesses used in TFTs, the potential difference between the probes was similar to the potential difference in the conduction channel, although some differences were observed for very thick films (semiconductor thickness larger than 2000 Å).

In addition, the simulations have shown that the probe widths have to be less than 4 μm, typically, and the distance between probes and source/drain contacts larger than 1 μm, typically, to prevent any modification of the TFT characteristics. For larger probe widths, a significant electric field fringing effect is observed, resulting in a higher conductance for the TFT itself [40]. A similar effect was observed for distances between probes and S/D contacts shorter than 1 μm, typically. However, it should be noted that, for the typical GFP TFT design (probe width ~ 2 μm, distance probes—S/D about 10 μm), the electrical field fringing effect can be neglected and we can assume that the two inner probes do not affect the TFT electrical behavior.

The GFP TFT structure can be used to investigate the effect of the a-Si:H density-of-states on the TFT intrinsic electrical performance. An increase in the density of conduction-band-tail (CBT) states result in a reduction of the field-

effect mobility and an increase in the threshold voltage, as shown in Figure 3.15. It also results in an increase in the γ -coefficient associated with the transfer characteristics non-linearity. However, γ -values extracted for conventional TFTs can apparently be reduced by the TFT parasitic resistances and can therefore lead to incorrect TFT analysis. Figure 3.16 shows that $\gamma = 1$ can be observed for a TFT with a high density of CBT states and high source/drain series resistances. In contrast, the GFP TFT structure allows for the accurate estimation of γ , converging toward 1 for low values of the CBT density-of-states. In contrast, an increase of the density-of-deep-gap states results only in an increase of the threshold voltage, as is clearly seen in Figure 3.17. It has no effect on the TFT intrinsic field-effect mobility or γ . Therefore, μ_{FE} and γ are associated mainly with the conduction band-tail characteristic energy. The GFP TFT structure can be used to distinguish between the changes due to a variation in the amorphous semiconductor density of conduction-band-tail states from the ones associated with the density of deep-gap states.

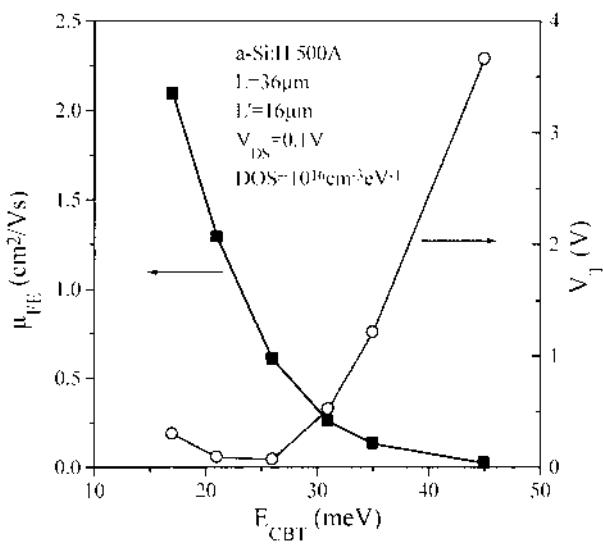


FIGURE 3.15 GFP a-Si:H TFT field-effect mobility and threshold voltage in linear regime as a function of the characteristic energy of the a-Si:H conduction band tail. (From Ref. 40, with permission from Society for Information Display.)

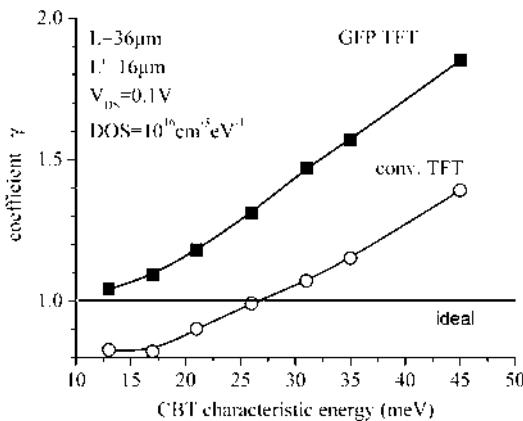


FIGURE 3.16 Coefficient γ as a function of the a-Si:H conduction-band-tail characteristic energy. (From Ref. 40, with permission from Society for Information Display.)

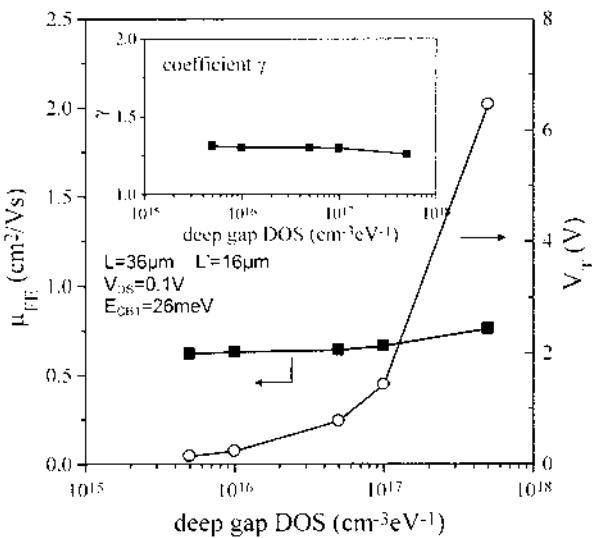


FIGURE 3.17 GFP TFT field-effect mobility and threshold voltage in the linear regime as a function of the density of deep-gap states. The inset shows the variation of γ with the density of deep-gap states. (From Ref. 40, with permission from Society for Information Display.)

3.3.4.3 Gated Four-Probe Thin-Film Transistor Experimental Results

To test the GFP a-Si:H TFT structure experimentally, a-Si:H TFT and GFP a-Si:H TFT structures were fabricated on the same Corning 7059F glass substrate in the same processing run [38]. The $G' - V_{GS}$ characteristics for a-Si:H TFT and GFP a-Si:H TFT having different channel lengths (L or L') are shown in Figure 3.18. For a-Si:H TFTs, in the linear region, a lower conductance is observed for a shorter-channel-length device because of the effect of the TFT source/drain series resistance. For the GFP a-Si:H TFT, as expected, no channel length dependence is observed in the $G' - V_{GS}$ characteristics. Similarly, high source and drain contact resistances result in significant degradation of the conventional TFT conductivity, while the GFP TFT conductivity is not affected [40]. Finally, a thicker a-Si:H layer (3000 Å) also causes a strong reduction in the source–drain conductance of the a-Si:H TFT due to a higher S/D series resistances while GFP TFT characteristics are nominally independent of the a-Si:H film thickness [39].

3.3.5 Amorphous Silicon Thickness Effects

The a-Si:H film thickness has a significant effect on the a-Si:H TFT characteristics, mostly in the ON-state and subthreshold regime. One does not observe any notable a-Si:H film thickness effect on the TFT OFF-current, as shown in Figure

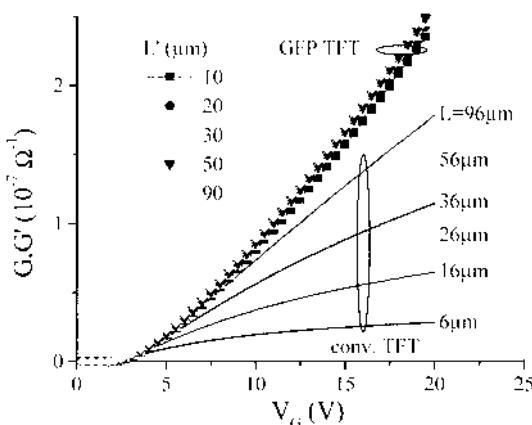


FIGURE 3.18 Normalized conductance versus gate voltage curves measured for conventional and GFP TFTs, for different TFT channel lengths. (Adapted from Ref. 39.)

3.19, but one clearly notices the thickness dependence of the TFT ON-state parameters in the linear regime. When the thickness of the amorphous silicon layer increases, the following changes occur:

1. Improvement of the subthreshold slope (inset Fig. 3.19)
2. Increase of the apparent field-effect mobility for thin a-Si:H layers (Fig. 3.20)
3. Reduction of the apparent field-effect mobility for thick a-Si:H layers (Fig. 3.20)
4. Increase of the intrinsic field-effect mobility (for all the a-Si:H thicknesses, Fig. 3.20)
5. Reduction of the threshold voltage (Fig. 3.20)
6. Reduction of the γ -coefficient (Fig. 3.21)

The evolution of the subthreshold slope and the intrinsic field-effect mobility in the linear regime suggests that the electronic quality of the amorphous silicon (in terms of density-of-states) is improved, while the reduction of the TFT apparent field-effect mobility observed in the case of a very thick a-Si:H film results most likely from a stronger influence of the parasitic access resistances.

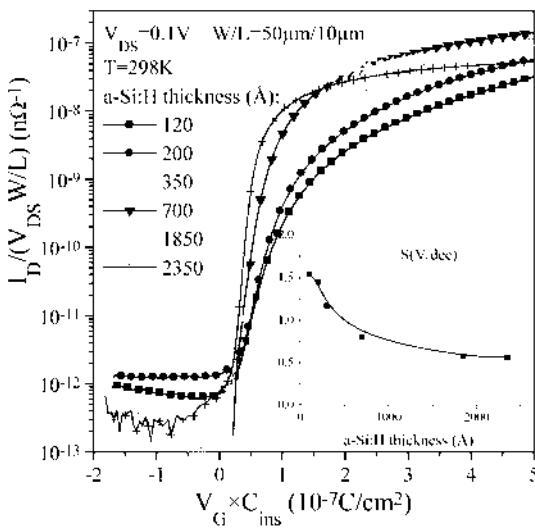


FIGURE 3.19 TFT transfer characteristics measured in the linear regime ($V_{DS} = 0.1$ V) for 10- μ m-long top-gate a-Si:H TFTs with different a-Si:H thicknesses. The inset shows the evolution of the subthreshold swing as a function of the a-Si:H thickness. (From Ref. 26.)

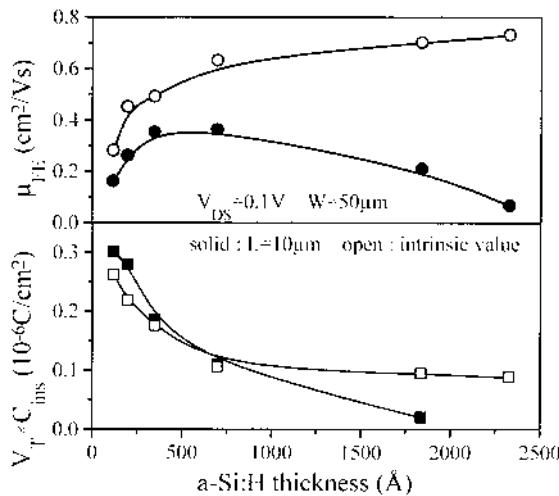


FIGURE 3.20 Variations of the a-Si:H TFT ON-state parameters in the linear regime as a function of the a-Si:H thickness. Solid symbols show apparent field-effect mobility and normalized threshold voltage for 10- μm -long TFTs and open symbols show intrinsic field-effect mobility and normalized threshold voltage. (From Ref. 26.)

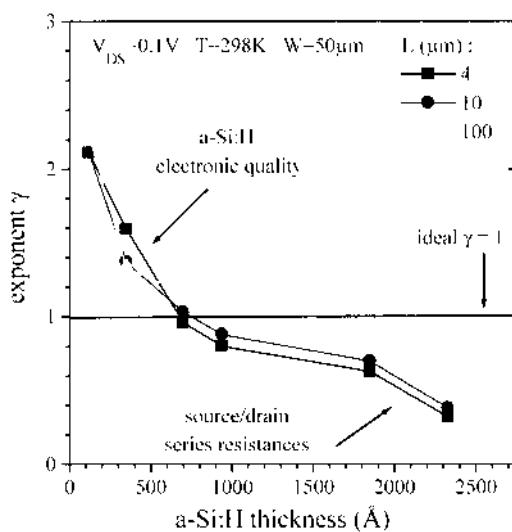


FIGURE 3.21 Exponent γ variations as a function of the a-Si:H thickness for different TFT channel lengths. (From Ref. 26.)

The reduction of the threshold voltage is probably due to a weaker influence of the back interface when the amorphous silicon thickness increases. The decrease of the γ -exponent with increasing a-Si:H thickness suggests a lower density of conduction-band-tail states present in thicker a-Si:H films. The results obtained in the saturation regime exhibited the same trend as the ones obtained in the linear regime: The TFTs made from thicker a-Si:H films have better electrical performance (higher field-effect mobility and lower threshold voltage) than the thinner ones. This is consistent with the idea that the amorphous silicon quality is improved when the film thickness increases. As shown in [Figure 21](#), for a very thick a-Si:H film and short TFT channel length, higher source/drain series resistances result in a low γ -value, i.e., less than 1. The increased effect of the source/drain series resistances has been confirmed by the analysis of TFT output characteristics and their derivatives [26]: Current crowding was much more significant for thicker a-Si:H films. In addition, the series resistivity r_{ceff} increased with the a-Si:H film thickness, which confirms the significant effect of the access region between the source (or drain) contact and the conduction channel on the TFT S/D series resistances [37].

As explained earlier, the increase of the amorphous silicon thickness first results in an improvement of the a-Si:H TFT electrical performance, due to a better material electronic quality; then, for thicker a-Si:H layers, the access resistances become more and more significant and degrade the TFT electrical performance. Thus, it is necessary to find a compromise between amorphous semiconductor quality and source and drain access resistances. We can define an optimum amorphous silicon thickness as the one that results in the highest apparent field-effect mobility ([Fig. 3.22](#)), which depends on the electronic quality of the material and on the TFT source and drain series resistances. Similarly, an optimum value of the a-Si:H thickness can be defined, from the evolution of the TFT field-effect activation energy (E_{act}), as a function of the film thickness. It is well established that E_{act} depends on both the a-Si:H electronic quality and the source and drain series resistances ([Fig. 3.23](#)). We can see from Figures 3.22 and 3.23 that the TFT field-effect mobility and field-effect activation energy are optimized for similar values of the a-Si:H thicknesses. Also, we can notice in Figures 3.22 and 3.23 the clear dependence of the optimum a-Si:H thickness on the TFT channel length, connected to the stronger influence of the source and drain series resistances on shorter-channel TFTs. In comparison with long-channel TFTs, the degradation of short-channel TFT electrical performance with increasing a-Si:H thickness clearly appears for thinner a-Si:H layers. Typically, for these devices the optimum thickness for a 100 μm -long TFT is above 1000 Å, while the apparent field-effect mobility of a 10- μm -long TFT starts degrading for a-Si:H films thicker than 500 Å. The optimized a-Si:H thickness for short-channel TFTs, such as the ones used in AMLCDs, is below 500 Å, which is comparable to the a-Si:H thickness used for bottom-gate trilayer a-Si:H TFTs. This value is signifi-

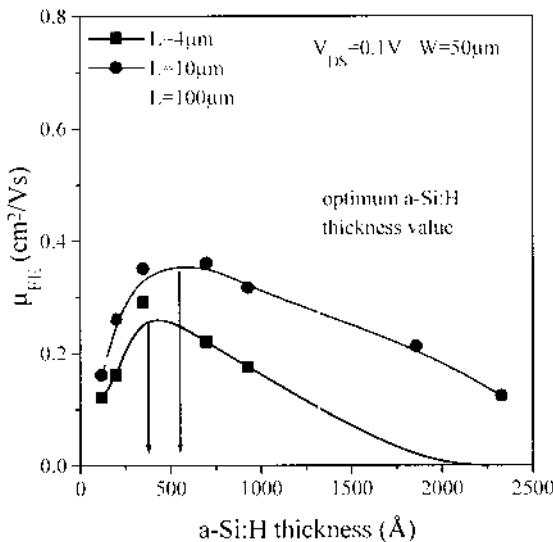


FIGURE 3.22 Variations of the a-Si:H TFT apparent field-effect mobility with a-Si:H thickness for different TFT channel lengths. (From Ref. 26.)

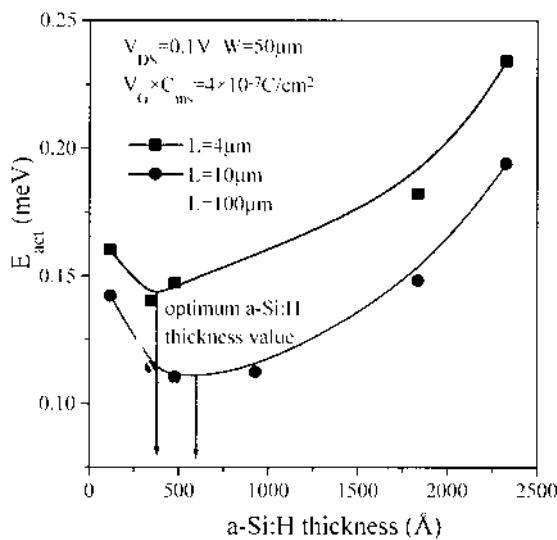


FIGURE 3.23 Variations of the a-Si:H TFT field-effect activation energy with a-Si:H thickness for different TFT channel lengths. (From Ref. 26.)

cantly smaller than the typical amorphous silicon thickness used for back-channel-etched TFTs, which is about 1500 Å.

3.3.6 Amorphous Silicon Thin-Film Transistor Under Illumination

To analyze the photosensitivity of a-Si:H TFTs in detail, we define the ratio between TFT drain current under illumination and in the dark [41]:

$$R_{L/D} = \frac{I_{DS\text{illum}}}{I_{DS\text{dark}}} \quad (3.43)$$

Figure 3.24 shows the TFT transfer characteristics measured in the dark and under illumination (white light, halogen bulb). The typical variations of $R_{L/D}$ with the TFT gate voltage are also shown in this figure. We can clearly see a peak corresponding to the TFT weak-accumulation regime, typically observed for small, positive gate voltages. In the strong-accumulation regime, the TFT current ratio decreases, as expected, because of the dominant effect of the gate voltage on the concentration of accumulated carriers. In the OFF-state, $R_{L/D}$ is significantly higher than in the ON-state, but still several decades lower than the peak value. The existence of the peak in the weak-accumulation regime can be understood by looking at the TFT transfer characteristics (Fig. 3.24). Because of the subthreshold slope change under illumination, we can identify a small gate

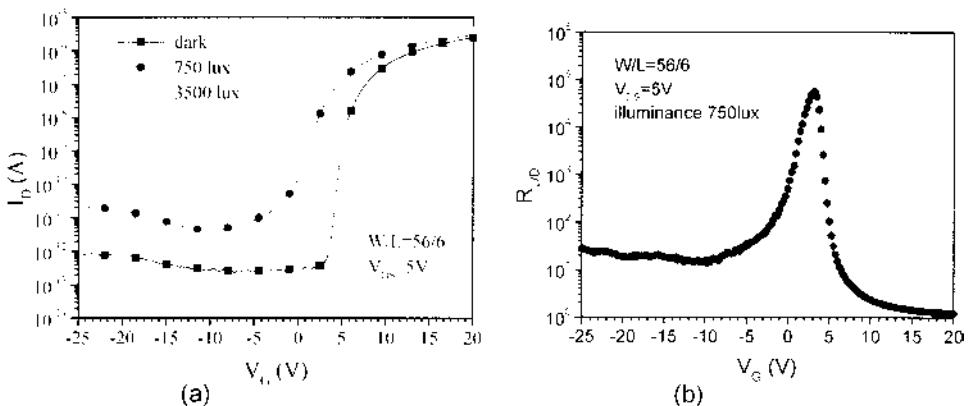


FIGURE 3.24 (a) Measured a-Si:H TFT transfer characteristics in the dark and under white-light illumination. (b) Typical behavior of the $R_{L/D}$ ratio between the TFT drain current under illumination and in the dark as a function of the TFT gate voltage, under white-light illumination. (From Ref. 41.)

voltage range for which the TFT is in the OFF-state in the dark and almost in the ON-state under illumination. This gate voltage range will therefore provide the highest R_{LD} ratio.

R_{LD} does not significantly depend on the drain voltage, ranging from 0.1 to 15 V. In the ON-state, the TFT current is proportional to the channel width and roughly inversely proportional to the channel length, neglecting the S/D series resistances. In the OFF-state in the dark, the TFT OFF-current is usually independent of channel width and channel length. We believe that this is due to a very low value of the TFT OFF-current in the dark: What we measure might be either measurement noise or transient current, in which other mechanisms are involved. When the TFT is under illumination, the carrier concentration is increased and the OFF-state conduction mechanisms are similar to the ON-state situation; the current is therefore again proportional to the channel width and inversely proportional to the channel length. Consequently, the peak value of R_{LD} increases with increasing channel width and with decreasing channel length.

The R_{LD} peak value can be as much as two to three orders of magnitude above the current ratio in the TFT OFF-state and could therefore be used very easily to detect the presence of light, even at low light intensities. We can clearly see in Figure 3.25a that the R_{LD} peak is significant even for very low illuminance values. The variations of R_{LD} (at $V_G = 1$ V) with the illuminance (IL) are shown in Figure 3.25b and clearly exhibit a power-law dependence; e.g., $R_{LD} \propto IL^\gamma$, with $\gamma = 0.7$. Similar behavior was reported in the literature for the dependence of a-Si:H photoconductivity on illuminance. However, we should note that the R_{LD} peak is quite narrow, with a typical width at half height of a few volts or less. Consequently, the R_{LD} peak value strongly depends on the considered gate voltage, and a slight shift of the TFT transfer characteristic could result in erroneous values. The peak ratio in the low-accumulation regime can therefore be used to detect the presence of light but not to accurately quantify the light intensity. The OFF-regime, in which R_{LD} is much less sensitive to the gate voltage, would be more appropriate for this purpose.

The effect of the illumination wavelength on the TFT photosensitivity has also been studied. Two types of measurements were performed using monochromatic light at different wavelengths: constant optical power density (1.5×10^{-4} W/cm²) and constant optical flux (6×10^{14} photons/cm²s). The results in both cases are quite similar: A significant increase of the TFT photosensitivity with increasing photon energy was observed. This behavior is clearly associated with the absorption curve of amorphous silicon [41].

Finally, the effect of the TFT operation temperature was investigated, using monochromatic light ($\lambda = 620$ nm, $P = 77$ μ W) to avoid any parasitic heating of the sample that can occur under white-light illumination [41]. From the analysis of the TFT operation, we have concluded that, for the same gate voltage, the TFT current increases with temperature much faster in the dark (OFF-state) than

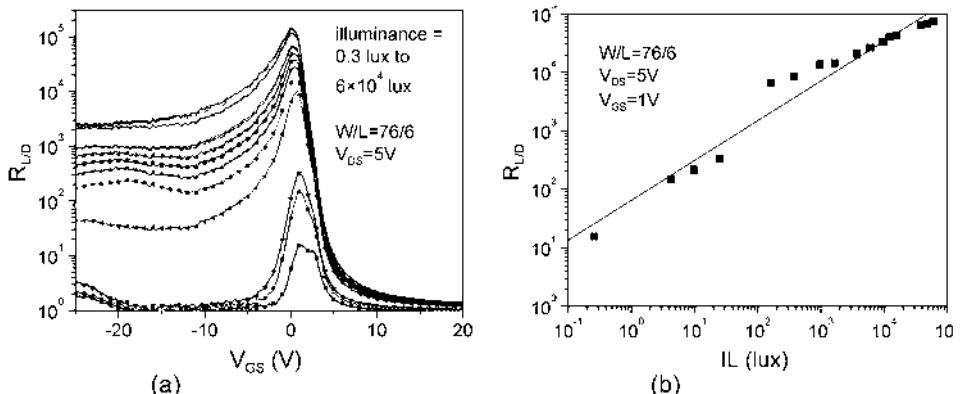


FIGURE 3.25 (a) R_{LD} as a function of the a-Si:H TFT gate voltage, for different white-light intensity values. (b) R_{LD} (for $V_G = 1$ V) as a function of the illuminance (IL). Symbols show experimental data; the solid line shows the fit to a power-law behavior, with an exponent $\gamma \sim 0.7$. (From Ref. 41, with permission from Society for Information Display.)

under illumination (weak-accumulation regime). We can therefore expect R_{LD} to decrease with increasing temperature, which was experimentally confirmed [41].

3.4 ADVANCED HYDROGENATED AMORPHOUS SILICON THIN-FILM TRANSISTOR STRUCTURES

3.4.1 High-Performance Back-Channel-Etched Hydrogenated Amorphous Silicon Thin-Film Transistors

To improve productivity and to lower the fabrication costs of AMLCDs, there was a need to enhance the throughput and operation up-time of plasma-enhanced chemical vapor deposition (PECVD) tools used in the fabrication of a-Si:H TFTs. This should be achieved without sacrificing a-Si:H TFT electrical performance. One method consists of increasing the rate of deposition of the PECVD materials. Different methods, such as very high-frequency plasma [42], high pulsed-RF power density [43], helium dilution [44], and the unique design of electrodes for efficient ionization in the multichamber system for cost-effective manufacturing [45,46], have been developed to produce a-Si:H film with a high deposition rate. Among these different technologies, only a very high-frequency (60 MHz) PECVD [47] and a multichamber PECVD [45,46] systems approach have been

used in the production of a-Si:H TFTs. For very high-frequency (60 MHz) PECVD, it has been reported [47] that a-Si:H TFT having a high field-effect mobility (μ_{FE}) ($1.1 \text{ cm}^2/\text{V}\cdot\text{s}$) can be fabricated from high-deposition-rate materials. However, in another high-frequency (40 MHz) PECVD system of a similar design, a slightly lower mobility ($0.7 \text{ cm}^2/\text{V}\cdot\text{s}$) has been obtained [48]. At the same time, a-Si:H TFTs exhibiting $\mu_{FE} \approx 0.8 \text{ cm}^2/\text{V}\cdot\text{s}$ were fabricated from high-growth-rate materials [49] produced in a multichamber PECVD system.

3.4.1.1 Back-Channel-Etched Device Structure and Fabrication Process

The most commonly used TFTs have a bottom-gate (BG) back-channel-etched (BCE) structure, shown in Figure 3.26. The thicknesses of N-rich hydrogenated amorphous silicon nitride (a-SiN_{1.5}:H), intrinsic a-Si:H, and *P*-doped (n^+) a-Si:H are 2480, 2000, and 500 Å, respectively. The channel length is defined by using the source/drain metal (3000-Å-thick Mo) as a mask. The channel width and length of typical TFTs are 116 and 32 μm, respectively. Using this structure, high-field-effect-mobility TFTs have been fabricated [50] from high-deposition-rate materials deposited at 320°C in a 13.6-MHz AKT 1600 multichamber PECVD system. The a-Si:H was deposited under the following conditions: silane flow = 250–500 sccm, hydrogen flow = 2800 sccm, pressure = 2–4 torr, and RF power = 150 W. The microstructure of the high-deposition-rate materials was similar to the one obtained for low-rate PECVD films [51]. The materials used in these TFTs have the following properties: (1) a-Si:H deposition rate is 50 nm/min, dark conductivity is about $2.6 \times 10^{-11} \Omega^{-1} \text{ cm}^{-1}$, activation energy is 0.94 eV, Tauc optical bandgap is 1.78 eV, and hydrogen content is about $3 \times 10^{21} \text{ cm}^{-3}$; (2) a-SiN_{1.5}:H growth rate is 190 nm/min, etching rate in oxide etch solution is 61 nm/min, Tauc optical bandgap is 5.0 eV, dielectric constant is 7.0 (measured at 1-MHz frequency), and hydrogen content is about $1.9 \times 10^{22} \text{ cm}^{-3}$; (3) n^+ a-Si:H growth rate is 60 nm/min, film resistivity is 41 Ω·cm, activation energy is 0.2 eV, Tauc optical bandgap is 1.74 eV, and Mo/ n^+ a-Si:H contact resistance (R_c) is 0.25 Ω·cm².

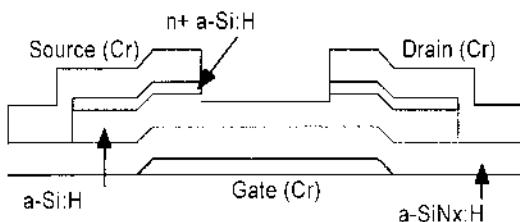


FIGURE 3.26 Cross section of BCE a-Si:H TFT.

3.4.1.2 Back-Channel-Etched Device Electrical Performance

Figure 3.27a shows the TFT output characteristics for various gate voltages. No current-crowding effect is observed at small drain voltages, suggesting good electrical/ohmic quality of the source/drain contacts. Figure 3.27b shows the TFT transfer characteristics for various V_{DS} . At $V_{DS} = 10$ V, the ON- to OFF-current ratio exceeds 10^7 and the OFF-current is less than 10^{-12} A. In the linear regime ($V_{DS} = 0.1$ V) the subthreshold swing (S) is about 0.3 V/dec, corresponding to a maximum density of deep-gap states, localized at or near the a-SiN_x:H/a-Si:H interface, $N_{ss}^{\max} = 8 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ [27]. The TFT field-effect mobility is 1.45 and 1.15 cm²/V-s in the saturation and linear regimes, respectively. The TFT field-effect mobility is channel length dependent, as expected, and the intrinsic TFT field-effect mobility is about 1.60 cm²/V-s. This high field-effect mobility value is in agreement with a low density of the interface states, mentioned earlier. The TFT threshold voltage is 2.0 and 1.9 V in the saturation and linear regimes, respectively. This low V_T is also consistent with a low density of interface states. From the temperature dependence of the $I_{DS} - V_{GS}$ characteristics, the field-effect activation energy was calculated as a function of V_{GS} [50]: The activation energy is on the order of 50 meV at $V_{GS} = 20$ V. This activation energy value corresponds to a slope of conduction-band-tail states of about 27 meV.

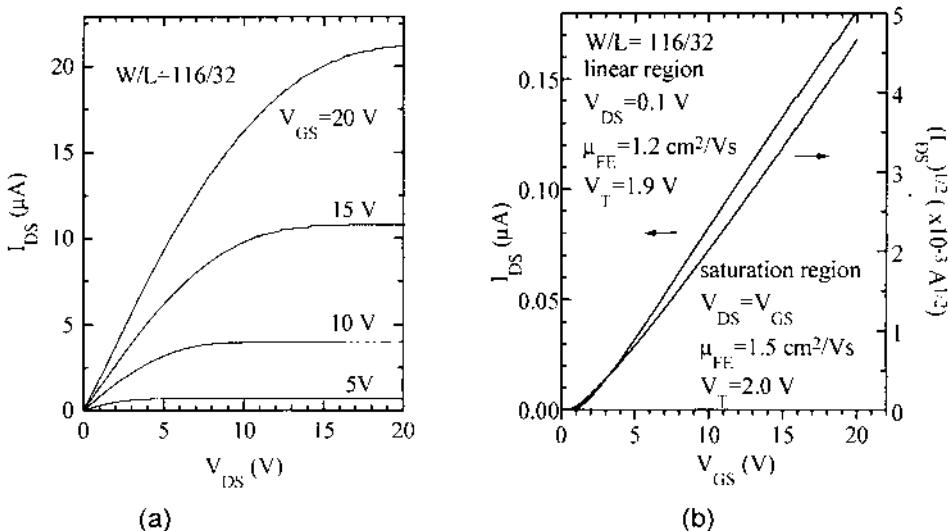


FIGURE 3.27 (a) Output and (b) transfer characteristic of a high-performance BCE a-Si:H TFT. (From Ref. 50.)

3.4.2 Gate-Planarized Hydrogenated Amorphous Silicon Thin-Film Transistor

The reduction of gate busline RC propagation delay and the enhancement of the pixel-electrode aperture ratio are very important for large-area, high-resolution, and low-power AMLCDs. Gate planarization technology [52,53] allows for the use of thick and, consequently, low-resistivity gate electrodes (Al or Cu) without having problems associated with electrode step coverage, taper edge definition [54,55], hillock formation when pure Al is used, or Cu-etching difficulties [56].

3.4.2.1 Gate-Planarized Device Structure and Fabrication Process

The fabrication process of the back-channel-etched (BCE) gate planarized (GP) a-Si:H TFTs is very similar to that of the conventional BCE a-Si:H TFTs; no additional photolithography step is needed. These GP-TFTs were fabricated on Corning 7059 glass substrate. First, a 5500-Å-thick Cr layer was prepared via DC sputtering. After the gate electrode/busline definition, a benzocyclobutene (BCB, $\epsilon_r = 2.4$) layer about 6000 Å thick was spin-coated directly over the Cr gate lines without any adhesion/barrier metal layer. After spin-coating, the BCB was cured in an N_2 convection oven at 250°C for 1 hr. Following the BCB curing, hydrogenated amorphous silicon nitride (a-SiN_x:H), intrinsic (i) and P-doped (n^+) a-Si:H films, having thicknesses of 500, 2000, and 600 Å, respectively, were deposited by PECVD at 250°C. After the active island definition, the gate vias composed of a-SiN_x:H and BCB layers were defined by reactive ion etch (RIE) using a CF₄/O₂ gas chemistry. A 3500-Å-thick Cr film was used to fabricate the source/drain (S/D) contact electrodes. After wet patterning of the S/D electrodes, the back-channel-etch of the n^+ - and i-a-Si:H layers was done by RIE using a CCl₂F₂/O₂ gas chemistry. The gate insulator capacitance per unit area was 10^{-8} F/cm².

The electrical properties of BCB, such as its dielectric strength and current leakage induced by electric-field bias and the interface properties with c-Si, have been evaluated from metal–insulator–metal (MIM) and metal–insulator–semiconductor (MIS) structures, respectively. The leakage current density is about 3×10^{-7} A/cm² at an electric field of 2 MV/cm. This leakage current density is about an order of magnitude higher than typical values found for a high-quality nitrogen-rich a-SiN_x:H film [57]. A higher leakage current found in the BCB material can be associated with its smaller-energy band gap (~3.9 eV), in comparison with the PECVD a-SiN_x:H films (~5.3 eV) [51]. Carrier injection through the BCB layer by Schottky and/or Frenkel–Poole emission can be responsible for this leakage current [58]. It has also been observed that when BCB is in direct contact with the c-Si, serious trapping and detrapping can occur under a high electric field. This may not be acceptable for electronic device applications. From

an analysis of MIS structure characteristics, it appears that a carrier injection barrier is needed when the BCB is in direct contact either with the amorphous semiconductor active layers or metal contacts.

Figures 3.28a and b show SEM photographs of the conventional and the GP TFT-array structures, respectively. In Figure 3.28a, clear steps of the source/drain electrodes over the gate-electrode edges and the busline crossover edges

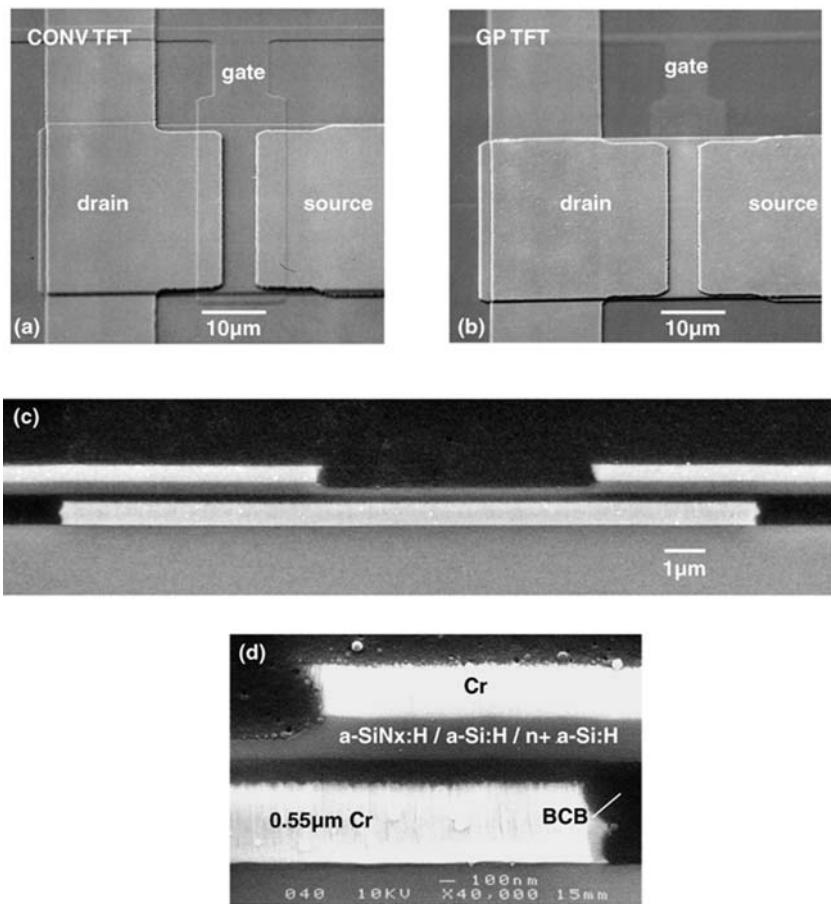


FIGURE 3.28 SEM photographs of (a) the conventional (CONV) and (b) the gate-planarized (GP) a-Si:H TFT structures. (c) Cross-sectional view of the GP-TFT. (d) Enlargement of the GP-TFT cross section in the source–gate overlap region. (Adapted from Ref. 52.)

can be seen for a thin ($\sim 800\text{-}\text{\AA}$ -thick) gate electrode. In contrast, in Figure 28b, almost no steps are detected over an even thicker gate electrode ($\sim 5500\text{ \AA}$ thick). Figures 3.28c and d show the cross section of the GP-TFT and the enlargement of the GP-TFT ($L = 6\text{ }\mu\text{m}$) in the source–gate overlap region, respectively. From this figure, it is clear that very good planarization of the thick-Cr-gate electrode has been achieved by the BCB layer. Even though the Cr electrode sidewalls are very rough (this most often occurs in the wet etching process), as shown in Figure 3.28d, the BCB layer can still completely fill the region adjacent to the sidewall areas without any void formation, and thus make it possible to produce a smooth PECVD a-SiN_x:H layer over the gate electrode corners. This excellent filling property of the BCB layer can thus ensure that no porous a-SiN_x:H layer is developed at the gate electrode corners and the dielectric defects caused by the subsequent wet etchant attack can be reduced. Therefore, there is no step coverage problem of the gate insulator over such a thick gate electrode structure. In addition to Cr gate metal, this technology can be applied to different gate metallurgies, such as Cu [59].

3.4.2.2 Gate-Planarized Thin-Film Transistor Electrical Performance

Figure 3.29 shows the GP-TFT ($W/L = 56/6$) output and transfer characteristics for different source–drain voltages ($V_{DS} = 0.1, 1, \text{ and } 10\text{ V}$). For $V_{DS} = 10\text{ V}$, an ON- to OFF-current ratio of about 10^7 can be obtained. For $V_{DS} = 0.1\text{ V}$, the subthreshold swing (S) is about 0.43 V/dec . From this S -value, the calculated

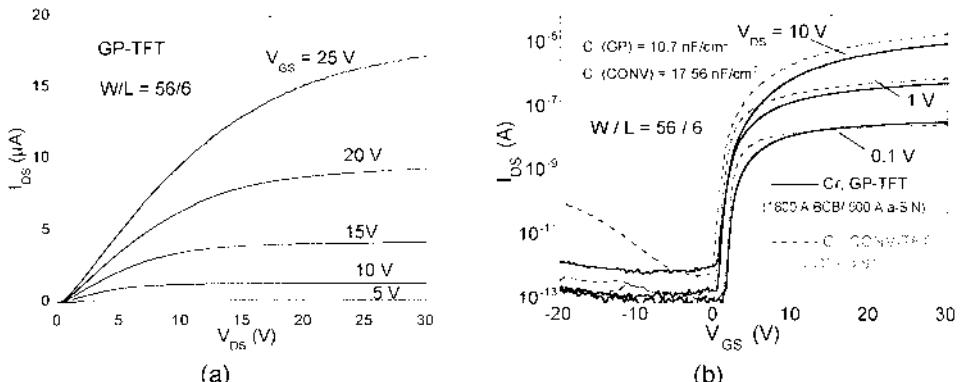


FIGURE 3.29 (a) Output characteristics of the GP-a-Si:H TFT. (b) Transfer characteristics of the GP-TFT (solid lines) and the conventional TFT (dashed lines) at different V_{DS} voltages. (Adapted from Ref. 52.)

maximum density of interface states (N_{ss}^{\max}) is about $4 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ [27]. To compare the GP-TFT electrical performance with that of conventional devices, Cr-gate TFTs having the same PECVD materials, except a 3300-Å-thick a-SiN_x:H layer ($C_i = 1.8 \times 10^{-8} \text{ F/cm}^2$), were fabricated. The S -value obtained for the conventional TFT at $V_{DS} = 0.1 \text{ V}$ is about 0.26 V/dec, which corresponds to $N_{ss}^{\max} \sim 3.8 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$. The GP- and conventional TFTs have very similar N_{ss}^{\max} values, indicating that the quality of the a-SiN_x:H/a-Si:H interface is similar in both devices. The field-effect mobility (μ_{FE}) and threshold voltage (V_T) of the GP-TFT in the linear regime are about $0.30 \text{ cm}^2/\text{V-s}$ and 3.48 V , respectively, while in the saturation region they are about $0.90 \text{ cm}^2/\text{V-s}$ and 5.96 V , respectively. The μ_{FE} and the V_T values for the conventional TFT are about $0.25 \text{ cm}^2/\text{V-s}$ and 1.93 V in the linear region and $0.95 \text{ cm}^2/\text{V-s}$ and 2.56 V in the saturation region, respectively. The higher V_T found for the GP-TFT is associated with its smaller gate insulator capacitance: Normalized threshold voltage values $V_T \times C_i$ of GP- and conventional TFTs are comparable. The BCB thickness had no effect on the TFT field-effect mobility and normalized threshold voltage, which can further confirm that the density-of-states of the a-Si:H layer and a-Si:H/a-SiN_x:H interface are not modified by the BCB film. However, a thicker BCB film resulted in a lower TFT drain current and a higher threshold voltage because of a reduction of the gate insulator capacitance. We should also note that a significant electrical instability of this type of device was observed [60], which can present a potential challenge for long-term operation. Electrical instability issues are discussed in Section 3.5.

3.4.3 Buried-Busline Hydrogenated Amorphous Silicon Thin-Film Transistor

To avoid the reduction of the TFT drain current and the increase in threshold voltage associated with gate planarization technology as mentioned earlier, a new device, named the buried-busline (BBL) structure, has been developed for large-area and high-resolution AMLCDs [60].

3.4.3.1 Buried-Busline Device Structure and Fabrication Process

A schematic cross section of the BBL structure is shown in [Figure 3.30](#). In comparison with the conventional a-Si:H TFT busline structure, one additional photolithography step is needed in the BBL structure, to define the buried gate buslines.

First, a 4500-Å-thick Cr film ($\rho_g = 3 \times 10^{-5} \Omega\text{-cm}$) was deposited on a Corning 7059 glass substrate via rf sputtering. After patterning the Cr BBLs, a low-dielectric-constant planarization layer, benzocyclobutene (BCB; $\epsilon_r \approx 2.4$), was spin-coated directly over the BBLs. Then the Cr/BCB layers were cured in

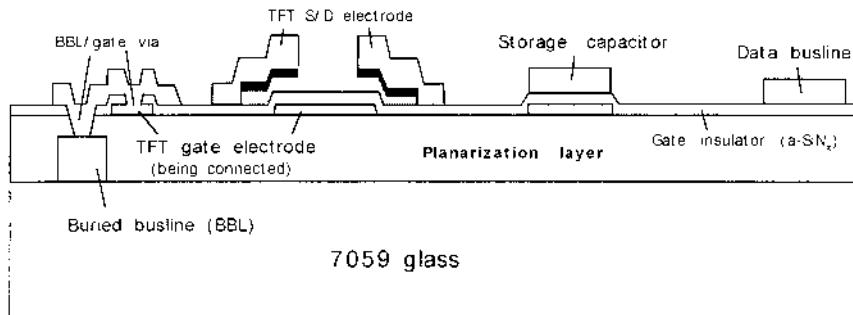


FIGURE 3.30 Schematic drawing of the BBL a-Si:H TFT structure. From [60].

a N₂ convection oven at 250°C for 1 hr. Following the BCB curing, a thin (700 Å) Cr layer was sputtered and patterned (TFT gate electrodes) over the BCB layer. Then amorphous silicon nitride, intrinsic and P-doped (n^+) a-Si:H films, having a thickness of about 2000, 2000, and 600 Å, respectively, were deposited via PECVD. After the active island definition, the BBL/gate via holes were opened through a-SiN_x:H and BCB layers by reactive-ionetch (RIE) using CF₄/O₂ gas mixture. Mo was used for the TFT source/drain metal contacts and BBL/gate via hole interconnects. Finally, the TFT back-channel etch was carried out by RIE using CF₄ gas.

Figure 3.31a shows the SEM picture of a TFT-pixel array incorporating the BBL structure. In this structure, to reduce the busline crossover capacitance,

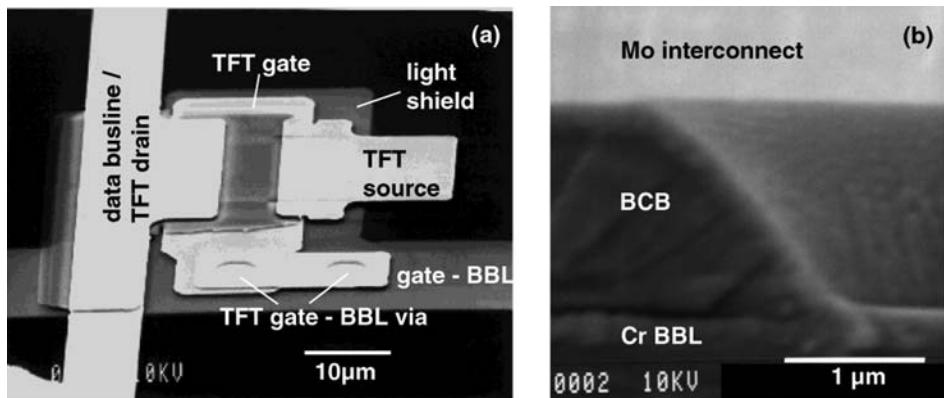


FIGURE 3.31 (a) SEM picture of the BBL-TFT structure; (b) cross-sectional SEM picture of the via hole over the gate BBL. (From Ref. 60.)

the gate busline (gate BBL) of the pixel arrays, which is connected to the TFT gate electrode, is buried by the BCB planarization layer. Figure 3.31b shows a cross section of the via hole over the BBL. It is clear from this figure that a very good conformal step coverage of the Mo interconnect over the BBL via hole has been achieved. This property ensures the absence of open circuits between the TFT gate electrodes and the BBLs. Also, in this structure the crossover defects (e.g., shorts and open circuits) between gate BBLs and data buslines can be prevented, since the gate BBL has been isolated from the source/drain metal layer.

3.4.3.2 Buried-Busline Device Electrical Performance

Figure 3.32a shows the transfer characteristics of the BBL (in solid lines) and the conventional- (CONV-; in dashed lines) a-Si:H TFTs for different source–drain voltages (0.1, 1, and 10 V). For the conventional TFT, a-Si:H and n⁺ a-Si:H layers of comparable thickness have been used; but the Cr gate electrode and a-SiN_x:H gate insulator are 1500 and 3000 Å thick, respectively. This figure indicates that the BBL-TFT has a higher ON-current than the conventional TFT, due to its

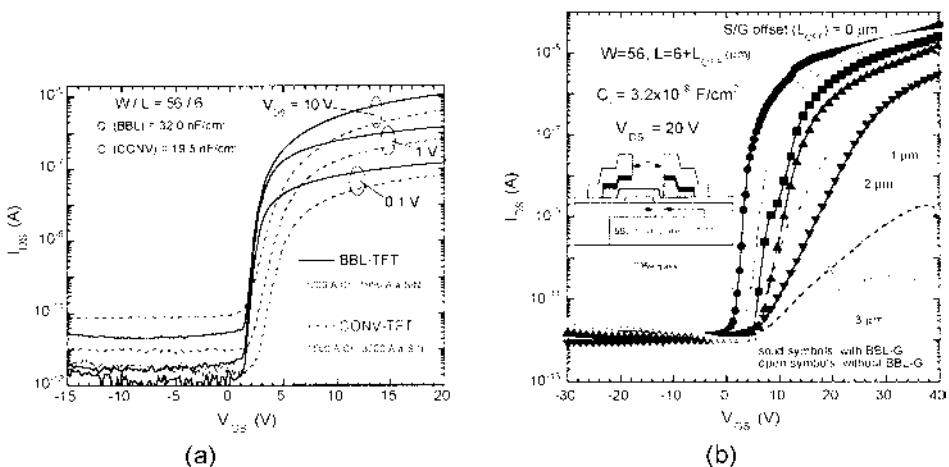


FIGURE 3.32 (a) Transfer characteristics of the BBL (solid) and the conventional (CONV-) (dashed) a-Si:H TFTs for different V_{DS} voltages. (b) Transfer characteristics of the BBL a-Si:H TFTs with source/drain gate offset ranging from 0 to 3 μm. The inset shows the cross section of the BBL TFT with source/drain gate offset. (From Ref. 60.)

larger gate insulator capacitance per unit area (C_i). In addition, the BBL-TFT has a smaller OFF-leakage current, which can be attributed to a better step coverage of the a-SiN_x:H layer over a thin (700 Å) Cr gate electrode used in the BBL structure. The subthreshold swing (S) of the BBL-TFT is about 0.31 V/dec, which corresponds to a maximum density of interface states of about 8×10^{11} cm⁻²eV⁻¹. The BBL-TFT field-effect mobility in the linear regime ($L = 6 \mu\text{m}$) is about 0.33 cm²/V-s, similar to the value obtained for the conventional TFT (0.34 cm²/V-s). Normalized threshold voltages are also similar, but, as expected because of its thinner gate insulator, the BBL-TFT has a lower threshold voltage (2.57 V) than the conventional a-Si:H TFT (4.07 V).

The BBL structure can also be used as a light-shield or field-plate electrode underneath the TFT gate electrode. This light-shield electrode can reduce the photoinduced leakage current in the TFT channel region associated with multiple reflection due to the backlight illumination. The other applications of the BBL structure are a low-feed-through-voltage TFT and a high-voltage TFT when the BBL is used as a field-plate placed underneath the normal TFT gate electrode (both electrodes are connected) [61,62]. In the conventional a-Si:H TFT structure, because of the nonnegligible series resistance, certain source/drain-to-gate overlap ($\Delta L_{S/D-G}$) is needed to increase the TFT ON-current level [19,36]. In contrast, with the BBL field plate, the current levels are very similar for the TFTs having different $\Delta L_{S/D-G}$ ranging from 0 to 3 μm [52]. This can be attributed to the formation of the extended electron channel (in the a-Si:H layer adjacent to the a-SiN_x:H layer) over the BBL field plate (outside the TFT gate electrode); i.e., the effective $\Delta L_{S/D-G}$ has been increased when the BBL field plate is added to the conventional a-Si:H TFT. The formation of such a conductive channel due to the electron accumulation by the BBL field plate (BBL-G) can thus maintain a high TFT ON-current. This is a very important foundation for AMLCDs. The direct consequence of this discovery is that the TFT ON-current level is not reduced when the gate-to-source/drain overlap capacitance ($C_{gs} \propto \Delta L_{S/D-G}$) is reduced. Hence, smaller feed-through voltages are produced in display operation due to smaller C_{gs} values.

Finally, the BBL can be applied to a high-voltage a-Si:H TFTs [62]. In conventional high-voltage a-Si:H TFTs, an offset between the TFT gate and drain/source electrodes is needed [63]. This gate offset can increase the TFT operating voltage range, but at the same time it reduces the TFT ON-current because of a large increase in the channel resistance along the nonoverlap gate–source/drain regions. As shown in [Figure 32b](#), BBL-TFTs have much higher I_{DS} currents than conventional high-voltage TFTs without the BBL field plate. This is clearly visible for a large gate offset (L_{OFF}). This type of high-voltage TFT structure is very attractive for LCDs requiring high-voltage switching devices, such as active-matrix reflective cholesteric LCDs [64].

3.4.4 Fully Self-Aligned Hydrogenated Amorphous Silicon Thin-Film Transistor

In the past, several researchers have introduced inverted-staggered self-aligned a-Si:H TFT structures to reduce the capacitive component of the TFT gate delay [35,65–68]. In all structures, the source/drain electrodes were aligned with the gate electrode by a back-substrate exposure technique [66], which simplifies the TFT fabrication. However, the intrinsic a-Si:H layer needs to be very thin to allow the UV light to pass through the a-Si:H layer for patterning the source/drain electrodes. The gate electrode should also be very thin in order to reduce the step coverage, resulting in an increased resistive component of the gate delay. A fully self-aligned (FSA) BCE Al-gate a-Si:H TFT has been developed [69] to reduce the gate line resistivity by using Al metallurgy.

3.4.4.1 Fully Self-Aligned Back-Channel-Etched Thin-Film Transistor Structure

This FSA BCE Al-gate a-Si:H TFT [69] requires only two masks, incorporating anodic aluminum oxidation and back-substrate exposure techniques. First, an Al-gate electrode was defined on a Corning 1713 glass substrate, followed by anodic oxidation (mask #1) [70]. Then the n^+ a-Si:H/a-Si:H/a-SiN_x:H layers were deposited via PECVD in one pump-down at a substrate temperature of 300°C. A successive deposition of different layers in one pump-down is essential for high-performance, stable TFTs. Next, a positive photoresist (Microposit 1827) was coated on the top and illuminated by UV light from the glass substrate side (back-substrate exposure). The a-Si:H and n^+ a-Si:H layers should be very thin to allow exposure of the photoresist, since a-Si:H-layer light absorption is film-thickness dependent. The UV wavelength that can be used for back-exposure ranges from 365 to 405 nm. In this experiment, the transmittance of the UV light was about 90 and 100% for Corning 1713 glass substrate and a-SiN_x:H film, respectively. However, the UV light transmittance decreased drastically for thick a-Si:H layers. Consequently, this FSA a-Si:H TFT process can work only for a-Si:H layers thinner than 1000 Å. To achieve good step coverage over the gate electrode, the Al sidewall profile was tapered during the patterning in a wet etchant solution of a mixture of phosphoric acid, nitric acid, acetic acid, and DI water. Next, a chromium (Cr) metal layer was deposited at room temperature via DC magnetron sputtering. After the liftoff process, the TFT channel area over the gate was opened, with the n^+ a-Si:H layer uncovered. The liftoff was done in hot liquid under ultrasonic agitation. The channel etch-back of n^+ a-Si:H was carried out via RIE using O₂ and CCl₂F₂ chemistry. Then the source and drain electrodes were patterned with photomask (mask #2). The Cr etching was done with a mixture of acetic acid and ceric ammonium nitrate. RIE etching of the

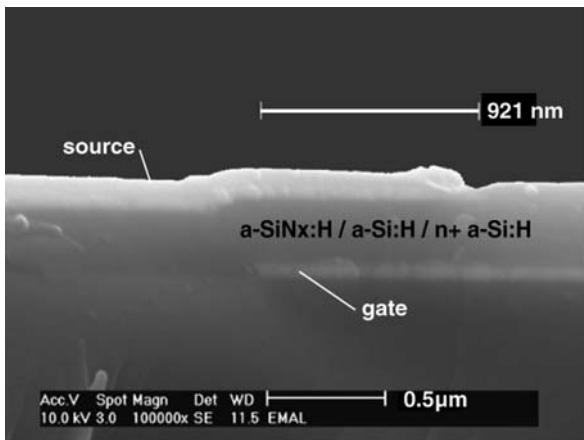


FIGURE 3.33 SEM picture of FSA BCE Al-gate a-Si:H TFT. The overlap between gate and source/drain electrodes is 921 nm. (From Ref. 69, with permission from Society for Information Display.)

n^+ a-Si:H and a-Si:H layers followed the wet etching of the source/drain area to avoid additional photomask for active-island definition. The typical thicknesses of each layer were 700 Å for Al, 3000 Å for a-Si_x:H, 220 Å for a-Si:H, 100 Å for n⁺ a-Si:H, and 1500 Å for Cr.

A SEM photograph of a self-aligned BCE a-Si:H TFT with a gate length of 7 μ m is shown in Figure 3.33. The overlap between the gate and the source–drain electrodes is about 1 μ m and was found to be uniform. This source/drain–gate overlap is attributed to the UV-light diffraction effect during the back-exposure. Changing the exposure and development times controls the overlap length, which ranges from 0.4 to 1 μ m. This value is much smaller than the typical overlap of conventional a-Si:H TFT (\sim 3 μ m), which decreases parasitic capacitance and RC delay associated with the scan buslines.

3.4.4.2 Fully Self-Aligned Back-Channel-Etched Thin-Film Transistor Electrical Performance

Figure 3.34 shows the output and transfer characteristics of a FSA TFT with $W/L = 56/7$. The TFT field-effect mobility and threshold voltage in the saturation regime are 0.58 cm²/Vs and 14.56 V, respectively. The corresponding normalized threshold voltage is about 3×10^{-7} C/cm⁻². The TFT OFF-current is 2.4×10^{-13} and the ON-OFF-current ratio is about 2×10^7 . The subthreshold swing is

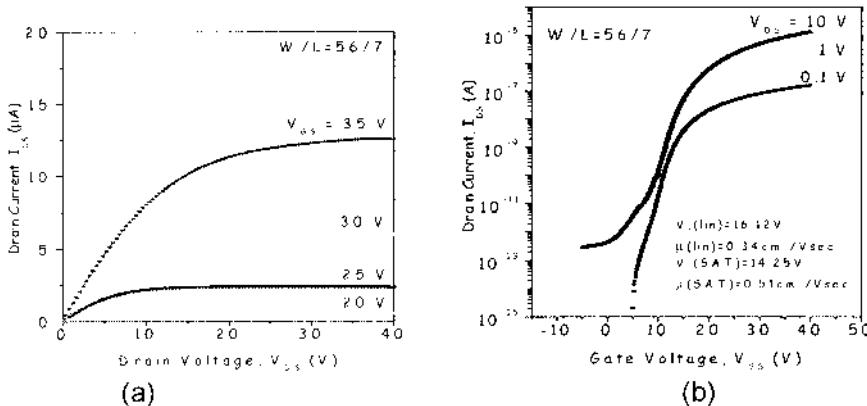


FIGURE 3.34 (a) Output and (b) transfer characteristics of an FSA BCE Al-gate a-Si:H TFT. (From Ref. 69, with permission from Society for Information Display.)

about 1.5 V/dec, corresponding to a maximum density-of-states at the amorphous semiconductor/gate insulator interface of about $3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. The rather high normalized threshold voltage and subthreshold swing of this FSA a-Si:H TFT may result from a high density-of-states present in the thin a-Si:H layer [26]. On the other hand, a thin a-Si:H layer yields low source/drain access resistances. Indeed, the TFT field-effect mobility and threshold voltage showed little channel length dependence for channel lengths above 7 μm , which can be attributed to reduced source and drain access resistances [26]. The lack of current crowding in our FSA Al-gate a-Si:H TFT output characteristics [69] also supports the idea of small source/drain access resistances.

3.4.5 Top-Gate Hydrogenated Amorphous Silicon Thin-Film Transistors

3.4.5.1 Device Structure and Fabrication Process

So far, most display manufacturers have adopted bottom-gate a-Si:H TFTs in AM-LCDs [2]. However, the top-gate TFT structure can be very attractive, because of, among other things:

1. The possible use of a very thin a-Si:H layer, which can reduce the light-induced TFT leakage current [2].
2. The gate lines, being deposited at the top of gate insulator, can be very thick (no step coverage concern over the gate lines as it is the case for

bottom-gate TFTs) to reduce the gate-line *RC* delay in a large-area high-resolution AMLCDs [71].

3. A smaller number of photomask steps, in comparison with some bottom-gate a-Si:H TFTs, can lower the AMLCD production cost [72].
4. The possible modification of the conduction channel region could improve the a-Si:H TFT performance.
5. The compatibility with poly-Si TFTs that are used to fully integrate the AMLCDs.

The top-gate TFT structure was used as early as 1984 [73] when CNET (Centre National d'Études des Télécommunications, France) fabricated the "NS2S" structure (normal staggered, two photomask steps). The biggest advantage of this structure was its very simple process, resulting in a very low fabrication cost. However, the NS2S structure was not adopted by display manufacturers because of its poorer electrical performance in comparison with the standard bottom-gate TFT structures [2].

Today, the electrical performance of all TFTs are comparable, mostly because of the improved quality of the interface between a-Si:H and a-SiNx:H. Also, the quality of the source and drain contacts has been improved by using either the selective deposition of *P*-doped (*n*+) a-Si:H layers [74] or the phosphine treatment (*P*-treatment) of the ITO contacts [75]. Both methods will ensure a high-quality ohmic source and drain contacts and a reduced number of photomask steps.

Top-gate TFTs have also been used in AMLCDs, initially [76] by the Hosiden Corp. and later by the Hosiden and Philip Display (HAPD) Corp. A top view and a cross section of a top-gate a-Si:H TFT are shown in Figure 3.35. In this

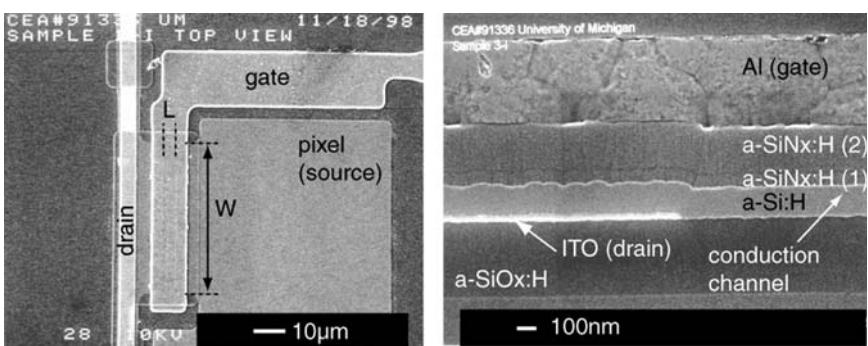


FIGURE 3.35 Top view and cross section of a top-gate a-Si:H TFT. (From Ref. 26.)

structure, a first gate insulator layer is deposited just after the a-Si:H and during the same deposition process. The active island (a-Si:H and a-SiN_x:H(1) layers) is then patterned before the deposition of the second insulator layer (a-SiN_x:H(2)). The number of mask steps required to produce this TFT is 4, which is comparable to or less than the number needed for the fabrication of typical bottom-gate TFT structures (4 and 5, for the back-channel-etched and the tri-layer structures, respectively). More precisely, the fabrication sequence for these top-gate TFTs is the following: first, a metal electrode (light shield) is deposited and patterned on glass substrates, and then it is covered with silicon oxide (a-SiO_x:H). Next, an indium–tin oxide (ITO) layer is deposited and patterned to form source and drain electrodes, and selective phosphorus treatment of the ITO-patterned electrodes is employed to achieve ohmic source/drain contacts [77]. Then an intrinsic a-Si:H/a-SiN_x:H bi-layer and a second a-SiN_x:H gate insulator are deposited by PECVD at 250°C. Finally, aluminum is deposited and patterned as the TFT gate electrode.

The phosphorus treatment of the source and drain electrodes is a critical step in the TFT fabrication, for it ensures the ohmic contacts that are necessary to achieve high-performance devices. Indeed, TFTs fabricated using a similar process but without the phosphorus treatment exhibited poor electrical performance and severe current crowding associated with high source and drain series resistances. Secondary ion mass spectrometry (SIMS) analysis of treated ITO electrodes has shown the high selectivity of the phosphine treatment. After treatment, the concentration of phosphorus atoms on the ITO electrodes is more than a decade higher than the concentration of phosphorus atoms on the substrate outside of the ITO electrodes. In addition, X-ray photoelectron spectroscopy (XPS) was used to show that, following the phosphorus treatment of ITO surface, an InP layer is formed at the ITO-treated surface. These results are consistent with other analyses performed on similar samples [75].

The electrical properties and the quality of the a-SiN_x:H(1) layer are critical for the TFT electrical performance. Indeed, a significant improvement in device performance, especially the apparent field-effect mobility, has been obtained by using the aminosilane regime for the deposition of the a-SiN_x:H(1) layer [78]. The quality of the interface between the a-Si:H and the a-SiN_x:H layers is also important for the device electrical performance. High-performance top-gate TFTs have been fabricated by using a nitridation process for the a-Si:H surface before the deposition of a-SiN_x:H gate insulator [79]. Output and transfer characteristics curves for a top-gate TFT are shown in [Figure 3.36](#).

3.4.5.2 Electrical Performance

Top-gate a-Si:H TFTs with electrical performance similar to bottom-gate TFTs have been fabricated. For an 8-μm-long TFT ($W = 50 \mu\text{m}$) with a-Si:H and a-

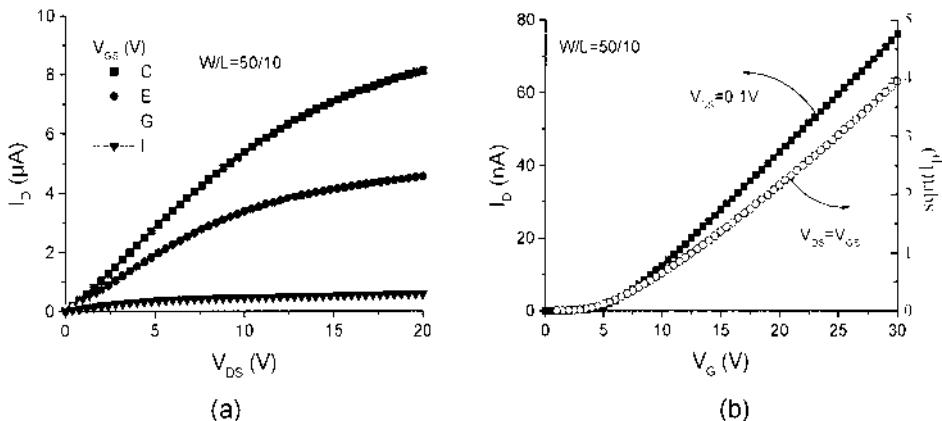


FIGURE 3.36 (a) Output and (b) transfer characteristic of top-gate a-Si:H TFT.

SiN_x:H thicknesses of 1350 and 2600 Å, respectively, the following performance was obtained:

- Field-effect mobility of 0.52 and 0.57 cm²/V-s in the linear and saturation regimes, respectively
- Threshold voltage of 2.4 and 2.2 V in the linear and saturation regimes, respectively, corresponding to a normalized threshold voltage $V_T \times C_{ins} = 5.5 \times 10^{-8}$ and 5.1×10^{-8} C/cm² in the linear and saturation regimes, respectively
- Subthreshold slope of 0.57 V/dec (in the linear regime), corresponding to a maximum density of states at the amorphous semiconductor/gate insulator interface of about 10^{12} eV⁻¹cm⁻² [27]

The electrical performance of these top-gate a-Si:H TFTs are comparable to the typical electrical performance observed for bottom-gate a-Si:H TFTs, which shows that the general belief that top-gate a-Si:H TFTs have a worse electrical performance than bottom-gate a-Si:H TFTs is not always valid [2,80].

3.5 ELECTRICAL INSTABILITIES IN HYDROGENATED AMORPHOUS SILICON THIN-FILM TRANSISTORS

It has now been well established that a-Si:H/a-SiN_x:H TFTs are not as stable as their crystalline MOSFET counterparts, but instead exhibit a shift in threshold voltage as a result of prolonged application of gate bias. Experimentally it has been established that this threshold voltage shift is a function of a number of

factors, including the magnitude, polarity, and duty cycle of the applied gate bias stress, the temperature at which the TFT is stressed, and the total stress time [81]. Underlying these observations is the understanding that these instabilities reflect the electronic quality of the PECVD a-Si:H and a-SiN_x:H films as well as the interface between them, since it is known that threshold instability can be minimized by careful control of process conditions such as deposition rate, gas flow ratio, and substrate temperature, which are known to control hydrogen content and bonding in the films.

The instability in a-Si:H TFTs has generally been attributed to one of two mechanisms: charge injection and subsequent trapping in the a-SiN_x:H gate insulator, or a bias-induced increase in silicon dangling-bond states in the a-Si:H. Often both mechanisms are invoked simultaneously to explain a range of experimental results, and either may dominate, depending on sample preparation conditions. The rationale behind the model for increased density of deep states within the a-Si:H has its origins in experiments showing degradation of TFT characteristics after prolonged illumination [82], and thus a connection to the well-known creation of metastable dangling-bond states observed in the Staebler–Wronski effect [83]. Hepburn et al. studied charge trapping and release from a-Si:H/a-SiN_x:H/n + c-Si samples using alternating combinations of gate stress, photoinduced discharge, and thermal annealing [84]. They fit their photoinduced decay data using a Gaussian trap model with an energy depth of 0.85 eV and an attempt-to-escape frequency of 10¹² Hz, but found a second activation energy of 1.5 eV in their annealing data. The thermal activation energy was attributed to dangling-bond states similar to those responsible for the Staebler–Wronski effect, since these were known to have a 1.5-eV activation energy [85]. As for the photodecay results, since charge release was found to drop to zero for illumination at sub-band-gap energies, internal photoemission was effectively ruled out. These observations were explained as resulting from the neutralization of the residual deep-trapped charge by the generation and redistribution of photoinduced carriers, rather than from direct release from trapping centers. It was postulated that population of the a-Si:H tail states induced by optical illumination could result in a silicon atom having an unstable configuration; a similar mechanism was suggested by Street to occur as a result of phosphorus doping [86]. The unstable situation is resolved by the breaking of weak Si–Si bonds and the formation of dangling-bond defects:



During the late 1980s, investigations were performed to elucidate whether deep-trap creation in the a-Si:H or charge injection into the a-SiN_x:H gate insulator played the primary role in TFT instability [87]. The use of an ambipolar transistor proved to be an excellent investigative tool for this purpose. An ambipolar a-Si:H TFT is one in which both electron and hole currents flow (albeit not equally, due to the large difference in electron and hole mobility), and it is produced

simply by dropping the $n+$ a-Si:H source and drain contact layers from the fabrication process. In order to have sufficiently large drain currents and to avoid undesirable contact resistance effects, these devices are usually physically quite large. Their utility lies in the fact that characteristic curves are produced for both negative and positive gate bias in the same device. If charge injection in the gate insulator is responsible for the TFT electrical instability, we expect a rigid shift of both the electron and hole conduction curves along the gate voltage axis *in the same direction*. On the other hand, if the density of deep-gap states is modified in the a-Si:H and the Fermi level moves through these states in establishing the conduction channel accumulation layer, then we expect the electron and hole current-voltage curves to shift in *opposite directions*. The band-bending diagrams showing deep-gap states filling under accumulation and inversion for this scenario are illustrated in [Figure 3.37](#).

Three sets of transfer characteristics for an ambipolar TFT are shown in [Figure 3.38](#) corresponding to the following sequential experimental conditions: after annealing at 180°C (no stress), after $+25\text{ V}$ stress for 4 hours, and again after -25 V stress. In this case, the transfer characteristics for electron and hole currents corresponding to the positive stress condition move in opposite directions, indicating an increase in deep-gap states in the a-Si:H. The curves shift in the *same* direction, however, for the negative gate stress condition, indicating a net positive charge in the amorphous silicon nitride layer and little further defect creation. Interestingly, when the same experiment was repeated, but with a large positive bias voltage of $+70\text{ V}$ following the initial $+25\text{ V}$ stress, the final set of curves both shifted to the right by nearly equal amounts, indicating that charge

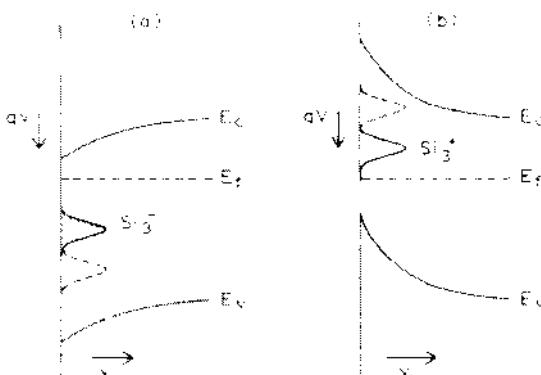


FIGURE 3.37 Band bending in a-Si:H under accumulation (a) and inversion (b). The created dangling bonds are negatively charged under positive bias and positively charged under negative bias. (From Ref. 87.)

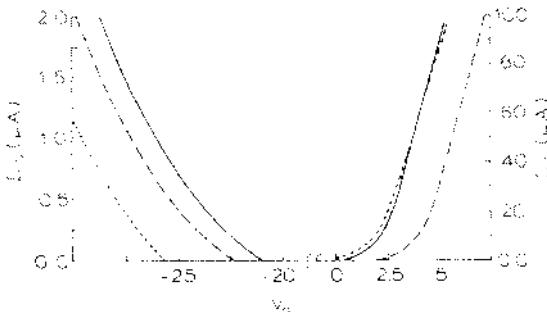


FIGURE 3.38 Ambipolar transfer characteristics corresponding to the following conditions: solid lines—after 180°C anneal; dashed lines—after +25-V bias stress for 4 hours; dotted lines—after -25-V bias stress for an additional 4 hours. (From Ref. 87.)

injection into the a-SiN_x:H gate insulator becomes dominant at high positive gate stress. Clearly both a-Si:H deep-gap-state creation and charge injection were seen to play roles in the materials chosen for this study.

On some other ambipolar devices, the results were slightly different [88]. Figure 3.39 shows transfer characteristics of ambipolar bottom-gate TFTs before and after positive and negative stress. Positive stress results in a shift of the

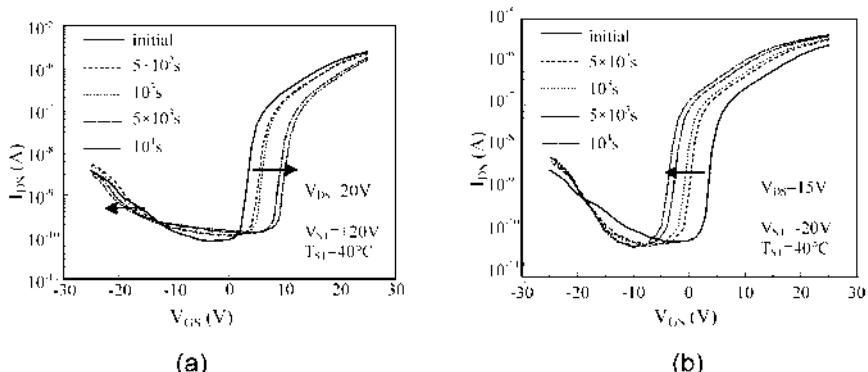


FIGURE 3.39 Evolution of ambipolar a-Si:H TFTs transfer characteristics under (a) positive and (b) negative steady-state gate bias-temperature-stress. Stress and measurements were performed at 40°C. (From Ref. 88)

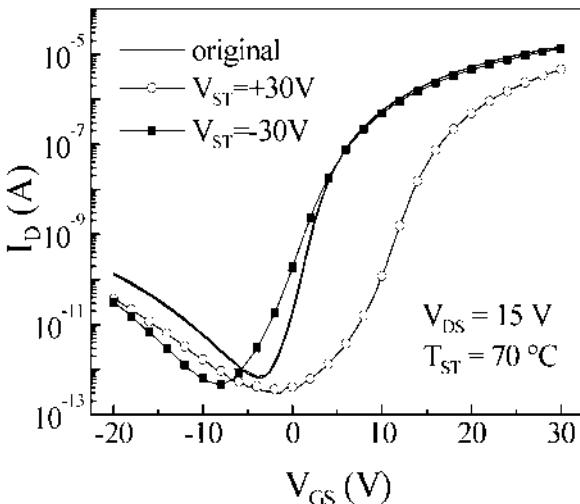


FIGURE 3.40 Evolution of conventional top-gate a-Si:H TFTs transfer characteristics after positive and negative steady-state gate bias-temperature-stress. Stress and measurements were performed at 70°C.

electron branch towards positive gate voltages while the hole conduction branch shifted towards positive voltages for short stress times, then towards negative voltages. This suggests mostly an increase of the density of deep-gap states in a-Si:H near the a-Si:H/a-SiN_x:H interface and a possible charge trapping in the gate insulator. The negative stress resulted in a shift of the electron conduction branch towards negative voltages and no significant shift of the hole branch. This corresponds to a decrease of deep-gap states in the band-gap region in combination with charge trapping in the a-SiN_x:H layer [88].

The simultaneous investigation of the electron and hole conduction branches has also been performed through measurements of conventional top-gate a-Si:H TFTs at high temperatures, as seen in Figure 3.40. Here, a positive stress results in electron and hole branches shifting towards positive and negative voltages, respectively, suggesting a creation of deep-gap states. Negative stress, on the other hand, results in almost no change of the electron branch and a shift of the hole branch towards negative voltages, which suggests that both defect creation and charge injection in the gate insulator occurred.

By the early 1990s, improvements in a-Si:H material quality and experiments with new structures and measurement techniques were suggesting that

although both instability mechanisms played roles, charge injection into the gate insulator was dominant. Gelatos and Kanicki stressed a-Si:H/a-SiN_x:H capacitors both positively and negatively, and used pulsed photocapacitance measurements to separate “fast” interface and/or a-Si:H bulk states from “slow” states within the gate insulator [89]. As in previous studies, they found that negative stress had no effect on a-Si:H bulk states but could lead to positive charge trapping in the gate insulator. It was determined that positive bias stress led to both a-Si:H gap-state creation as well as negative charge accumulation in the gate insulator but that no more than about one-third of the measured shift in the *CV* curves could be accounted for by a-Si:H bulk states measured by photocapacitance. In other words, charge injection into the insulator was the dominant factor.

A number of possible electron injection mechanisms leading to TFT instability were proposed by Powell [90], including Fowler–Nordheim injection, trap-assisted injection, and constant-energy tunneling from the a-Si:H conduction band, among others. These are illustrated in Figure 3.41. Building on results showing charge injection to be primarily responsible for TFT threshold shift,

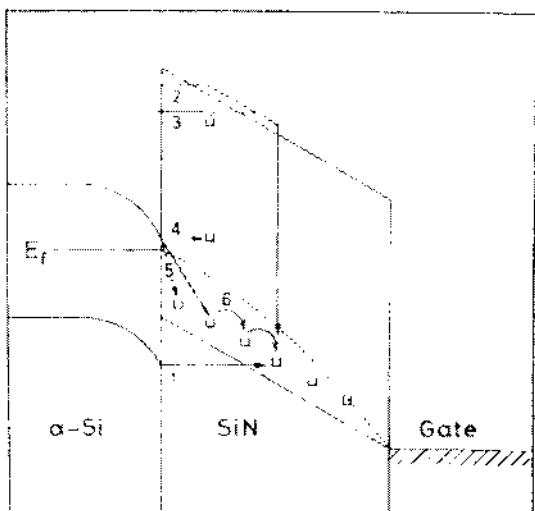


FIGURE 3.41 Charge injection mechanisms from a-Si into a-SiN_x:H gate insulator: 1—direct tunneling from the valence band; 2—Fowler–Nordheim injection; 3—trap-assisted injection; 4—constant-energy tunneling from conduction band; 5—tunneling from conduction band to insulator Fermi level (phonon assisted or via surface states); 6—hopping at the Fermi level. (From Ref. 90.)

Libsch and Kanicki found they could adequately model all their bias-temperature-stress (BTS) data, regardless of the magnitude of the stress bias, its polarity, or the temperature at which the stress was applied, using the following stretched-exponential equation [88,91]:

$$|\Delta V_T| = |\Delta V_o| \left\{ 1 - \exp \left[- \left(\frac{t}{\tau} \right)^\beta \right] \right\} \quad (3.45)$$

where $\tau = \tau_o \exp(E_\tau/kT)$ represents the characteristic trapping time of carriers, and $|\Delta V_o|$ is approximately the voltage drop across the insulator, given by $\sim |V_G - V_{To}|$, where V_{To} is the initial threshold voltage. In this model, the thermal activation is given by $E_a = E_\tau \beta$, with β being the stretched-exponential exponent; $E_\tau = E_d/\beta$ is interpreted as the average effective energy barrier that carriers in the a-Si:H channel need to overcome before they can enter the insulator, and τ_o is the thermal prefactor for emission over the barrier. For short stress times, lower-stress fields, or low stress temperatures, carriers hop or inject directly into lower-energy states located at the a-Si:H/a-SiN_x:H interface and into a transitional layer in the nitride close to the interface. At longer stress times, higher-stress fields, and higher temperatures, a larger fraction of states in the insulator near the interface are filled, leading to an increased probability of emission from these states. The model proposes that the amorphous structure of the a-SiN_x:H gate insulator will lend itself to an appreciable number of band-tail states, which act as transport states for the emitted lower-energy trapped charge, and this distribution of multiple trap levels yields the time-dependent power law in the argument of the exponent of Eq. (3.45). Threshold voltage shift data at a gate bias of + 25 V for temperatures ranging from 22°C to 125°C are fitted by the model in Figure 3.42.

Further modeling of the bias-temperature stress-induced threshold voltage shift has been proposed, unifying the effect of the stress time and temperature [92]. It is based upon the thermalization energy $E = kT_{ST} \ln(\nu t_{ST})$, where k is the Boltzmann constant and ν is the attempt-to-escape frequency, taken in [92] as 10^{10} Hz for all stress temperatures. The authors have shown that the ΔV_T-E curves overlap perfectly for all stress temperatures, and have identified a characteristic energy (corresponding to the inflexion point of the ΔV_T-E curves) that is assumed to be associated with the most likely defect creation energy barrier. Similar experiments performed on a series of other devices, having different structures such as the ones discussed previously in this chapter required adjustment of the value of V and resulted in ΔV_T-E curves still exhibiting very significant temperature dependence, as shown in Figure 3.43a [93]. However, by using a semi-empirical method based on a many-body approach proposed by the authors, it was possible to identify a characteristic time t_{peak} from the $\Delta V_T-\text{Log}(t_{ST})$ curves and to establish normalized curves ΔV_T versus t_{ST}^* = t_{ST}/t_{peak} that were identical for all devices measured, as shown in Figure 3.43b.

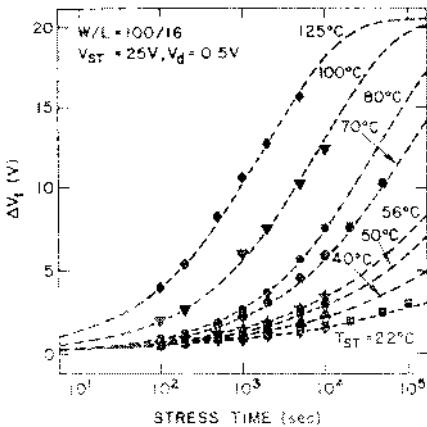


FIGURE 3.42 Threshold voltage shift ΔV_T versus time for a gate bias stress of +25V and for temperatures ranging from 22°C to 125°C. The symbols represent the data, and the dashed lines represent the fits to Eq. (3.45). (From Ref. 91.)

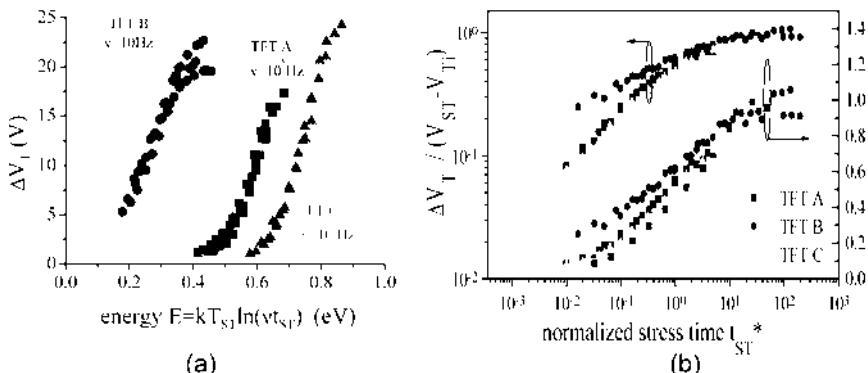


FIGURE 3.43 (a) Threshold voltage shift measured for different a-Si:H TFTs for a stress voltage of 30V and stress temperatures between 50 and 110°C as a function of the energy $E = kT_{ST} \ln(\nu t_{ST})$. The values of ν were determined to ensure, for each TFT, the best overlap of the ΔV_T - E curves for all stress temperatures. (b) Same data plotted under the form ΔV_T versus $t_{ST}^* = t_{ST}/t_{peak}$. (From Ref. 93.)

The success of all these models consists in their ability to ultimately predict future threshold shift behavior far out in time. However, all the models presented above address steady-state (DC) electrical stress, i.e. experiments during which the TFT gate voltage is constant. In AMLCDs, a-Si:H TFTs are under pulsed gate-bias addressing with a typical frequency of 60 Hz [94]. Therefore, from a practical point-of-view, to obtain a good estimation of the long-term reliability of a-Si:H TFTs in AMLCDs, it is necessary to understand the details of the electrical instability of a-Si:H TFTs under pulsed (AC) gate-bias stress conditions that are similar to a typical AMLCD addressing conditions. It has been pointed out that certain differences exist in ΔV_T between the steady-state and pulsed bias stresses [95,96]. Indeed, the investigation of the threshold voltage shift of bottom-gate back-channel-etched a-Si:H TFTs induced by pulsed BTS has shown that a significantly lower magnitude of threshold voltage shift was observed for negative AC BTS than for negative DC BTS [91]. The magnitude of the threshold voltage shift after negative AC BTS decreased with decreasing pulse width, as shown in Figure 3.44. A possible explanation is that the emptying of the traps and defect states that can occur during negative gate pulses occurs on a long time scale and

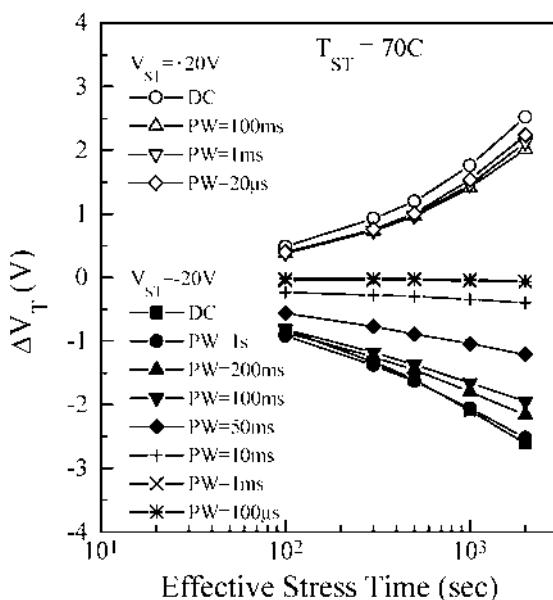


FIGURE 3.44 Threshold voltage shift versus effective stress time at different stress pulse-width for bottom gate a-Si:H TFTs under positive and negative BTS at $\pm 20V$, 70°C (from Ref. 88.)

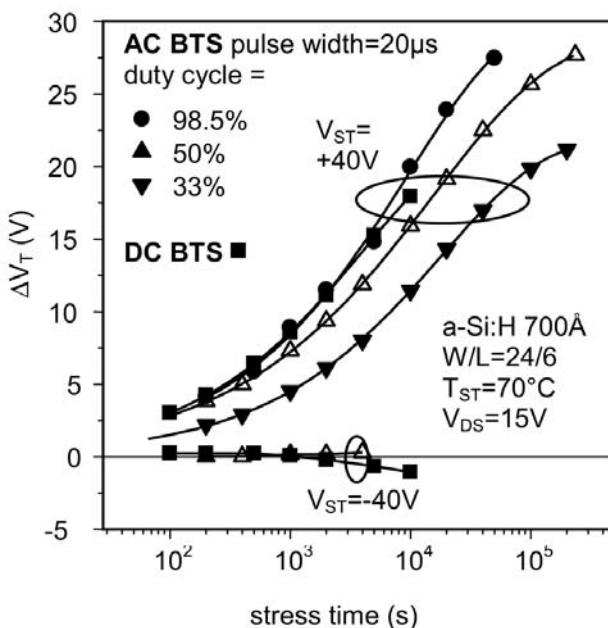


FIGURE 3.45 Threshold voltage shift for top-gate a-Si:H TFTs under BTS at 40V and 70°C, as a function of the effective stress time for different duty cycles (from Ref. 9).

is therefore affected by the duration of these gate pulses. Threshold voltage shift induced by positive AC BTS was only slightly lower than for DC BTS and pulse width-independent. It was reported previously that charge detrapping during pulsed operation could explain the smaller shifts induced by AC BTS [95]. In addition, relaxation of deep-gap defects during OFF-periods in the pulsed operation could also contribute to the threshold voltage shift differences [95].

For top-gate a-Si:H TFTs, observations have shown that the threshold voltage shift measured for positive AC BTS was lower than for positive DC BTS and decreased with decreasing duty cycle, as shown in Figure 3.45. On the other hand, negative DC and AC BTS experiments resulted in comparable, and very small, threshold voltage shifts [97]. The difference in the behaviors of these top- and bottom-gate a-Si:H TFTs has not been clearly explained, although it could be associated with the different nature of the a-Si:H/a-Si:N_x:H interface and/or the different characteristics of the materials used in both types of devices.

To address AMLCDs, the gate signals consist in a sequence of positive and negative pulses of different widths. It was established that the superposition

of positive and negative AC BTS will result in a net increase of the TFT threshold voltage. For AMLCD manufacturers, BTS modeling and threshold voltage shift calculation is a standard method of assuring adequate voltage margin over the lifetime of the active matrix. Margin in this sense is defined as the largest tolerable TFT threshold shift before current drive becomes insufficient to charge up a pixel during its scan time. By modeling accelerated threshold voltage shift results under higher temperature and/or different duty cycle and replotting the model under standard panel operational conditions, manufacturers can calculate whether their TFT process has adequate margin to meet their particular panel lifetime specification e.g. 60,000 hours (about 10 years). For the bottom gate TFTs above mentioned, a method of estimating ΔV_T of a-Si:H TFTs under pulsed bias-stress having both positive and negative gate-voltage cycles was proposed [88]. It resulted, for typical SXGA AMLCD driving conditions, in a TFT threshold voltage shift of about 3 V after about 10 years of operation at 70°C. The study of top-gate a-Si:H TFTs has indicated that threshold voltage shift would be larger than for the bottom-gate a-Si:H TFTs above mentioned but no final estimation has been proposed for the threshold voltage shift resulting from pulsed bias-stress representative of AMLCD driving scheme [97].

3.6 CONCLUSION

The results described in this chapter have addressed different aspects of a-Si:H TFT technology and may serve as a reference to the amorphous semiconductor community. In addition, the analysis and conclusions of this work and their significance could be a useful reference in the development of next-generation thin-film transistors based on organic semiconductors, which are discussed in subsequent chapters of this book.

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4

Technology of Polysilicon Thin-Film Transistors

A. T. Voutsas

Sharp Laboratories of America, Camas, Washington, U.S.A.

M. K. Hatalis

Lehigh University, Bethlehem, Pennsylvania U.S.A.

4.1 INTRODUCTION

The fabrication of polycrystalline silicon TFTs (poly-Si TFTs) encompasses many of the steps commonly encountered in MOSFET fabrication for integrated circuits. Despite the similarities, however, a number of key differences exist. These differences emerge primarily from the fact that the substrate of TFTs is no longer a single-crystal silicon wafer, but rather a typically (but not always) heat-sensitive material such as glass. This means that, unlike MOSFET devices, the TFT active layer needs to be formed on such amorphous host material and, furthermore, that the temperature of all associated processing has to be constrained within the allowable range prescribed by the materials characteristics of the substrate. For current display-glass substrates, the maximum processing temperature needs to be kept below $\sim 650^\circ\text{C}$. Even after considering possible exceptions to this maximum temperature (typically encountered during rapid thermal processing), the temperature range for fabrication on glass is severely constrained with respect to that on Si. This limitation affects critical process steps, such as the gate-insulator forma-

tion and the activation of the doped regions of the device. These processes have to be reconsidered and optimized for TFT fabrication on glass.

The substrate dissimilarity, however, has an even more immediate impact on the process flow of TFTs. Unlike MOSFETs, where the device active layer is part of the substrate, in the case of TFTs the active layer needs to be separately formed on the host substrate. The common way of doing that, for poly-Si TFTs, is by deposition of an amorphous Si (a-Si) film on the host substrate and the subsequent transformation of the a-Si film to poly-Si by means of an appropriate annealing step. Both of these steps affect the microstructural quality of the resulting poly-Si film, which means that the final poly-Si TFT performance will be critically affected by the selection of techniques and operating parameters for the deposition and crystallization of the thin Si film. It should be further noted that these steps are also constrained, as far as maximum temperature, per our earlier discussion.

In this chapter we present and discuss in detail process technologies that have been developed to address the unique issues of poly-Si TFT devices. Out of the many processing steps encountered in a typical poly-Si TFT fabrication flow, we have identified four key areas that deserve special consideration: thin-silicon-film deposition, amorphous silicon crystallization, gate insulator formation, and doping activation. However, before we address these process steps we will present, in Section 4.2, an overview of AMLCDs and the requirements they place on the TFT device. This overview will provide some foundation for better understanding the features of the various process steps we will cover. Sections 4.3–4.6 will then address the four process steps. Finally, Section 4.7 will discuss a typical polysilicon TFT fabrication flow.

4.2 OVERVIEW OF AMLCDs AND LOW-TEMPERATURE POLYSILICON TFT LCDs: PRINCIPLES AND TYPES OF ADDRESSABLE TWISTED NORMATIC LCD LIGHT VALVES

A typical twisted nematic (TN) addressable liquid crystal display (LCD) consists of an array of addressable liquid crystal (LC) pixels. Each pixel has LC material “sandwiched” between two electrodes that are covered with polarizers positioned as cross Nicols (i.e., staggered by 90°C). The LC molecular orientation changes the polarization state of the light that enters the LC cell through one of the two polarizers. This molecular orientation can be controlled by the electric field that is applied between the two electrodes, which contain the LC material. Therefore, depending upon the “twist” imposed on the polarization of the incoming light, it will either be allowed to pass through or be blocked by the polarizer at the

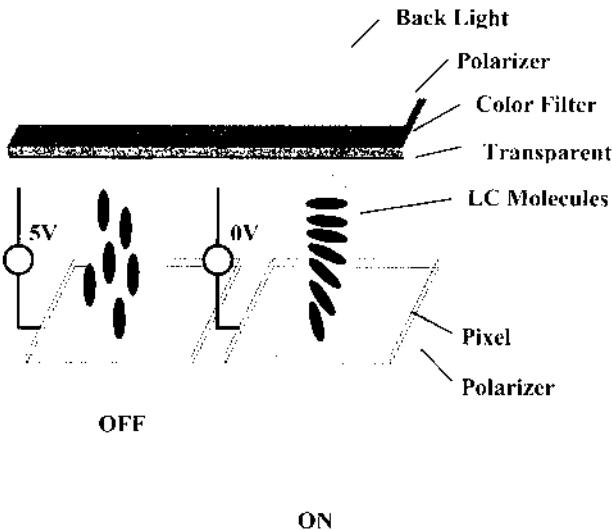


FIGURE 4.1 Twisted nematic LCD light valve (shown in “normally on” mode).

opposite side of the cell (see Fig. 4.1). In the example of Figure 4.1, light is allowed to pass when no field is applied between the two electrodes [1], whereas light is blocked when an appropriate voltage is applied between the two electrodes. This mode of operation is referred to as *normally-on* mode (as opposed to *normally-off* mode when light is blocked for zero applied field).

Addressable LCDs are separated into two types, passive matrix (PM) and active matrix (AM). Passive matrix is typically restricted to small display sizes due to issues with image quality (i.e., contrast ratio and crosstalk) that arise as the size and resolution of the display increase. Several improvements on the LC material and the associated addressing schemes have extended the applicability range of PM addressed panels beyond the limits predicted by conventional technologies [2,3]. Despite such improvements, however, the intrinsic limitations of PM technology have restricted the application range of PM panels and positioned active-matrix addressing as the technology of choice for high-end display applications. Active-matrix addressing uses independent electronic switches to individually control the state of each pixel. In this manner, the display performance (i.e., image quality) is decoupled from the shortcomings of PM addressing schemes and becomes a function of the type and performance of the pixel electronic switch. For high-performance displays, such switches are typically three-terminal devices and most notably thin-film transistors (TFTs) [4]. Depending upon the technology

used to fabricate TFTs, we distinguish between amorphous-Si TFTs (a-Si TFTs) and poly-Si TFTs. Poly-Si technology presents advantages over a-Si technology on the achievable size-versus-resolution limits for the display, as well as the opportunity to monolithically integrate additional functionality on the panel (i.e., beyond the pixel matrix). The advantages of poly-Si technology stem primarily from the significant performance gains of poly-Si TFTs over a-Si TFTs and its compatibility with CMOS fabrication. CMOS technology enables monolithic integration of peripheral drivers on panel as well as opportunities for the addition of other value-added components on the display [5,6]. Figure 4.2 shows a map of display application areas as a function of AMLCD technology [7]. Figure 4.3 presents the relationship between TFT performance (i.e., mobility) and TFT process technology (i.e. expressed by maximum process temperature).

4.2.1 Driver Requirements

The ability to integrate driver circuits on active-matrix TFT display panels (the term “LTPS TFT LCDs” has been coined for low-temperature poly-Si TFT LCDs)

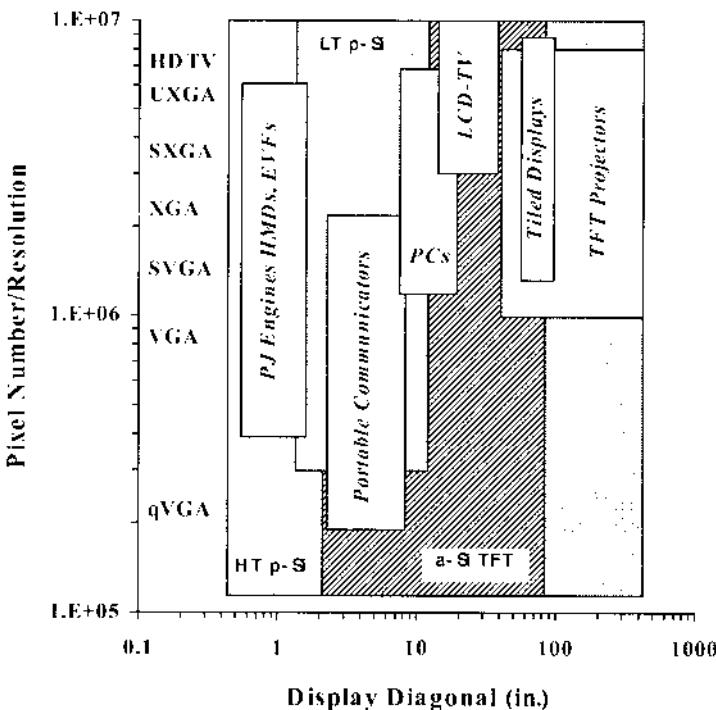


FIGURE 4.2 Display application areas as a function of AMLCD technology.

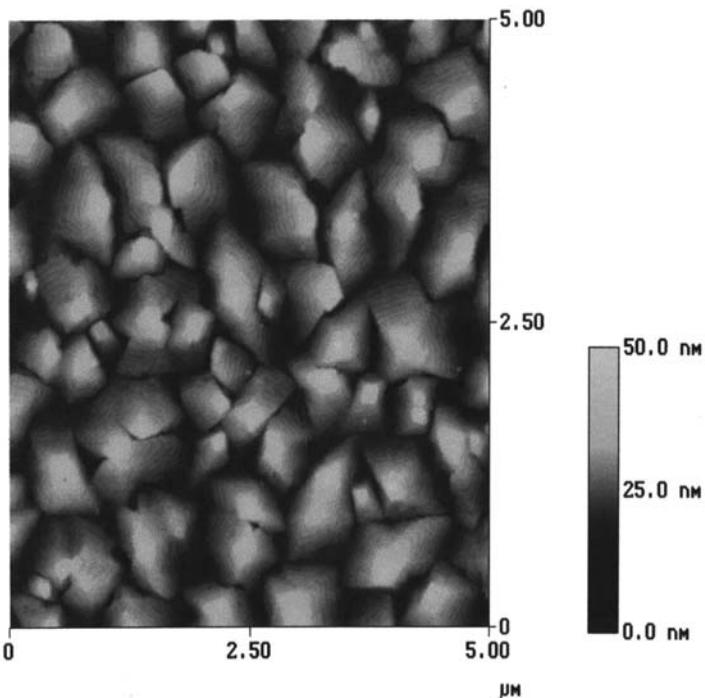


FIGURE 4.3 Illustration of TFT performance versus TFT process technology.

can lead to more rugged displays with lower cost because of the reduction in the number of external driver chips and driver interconnects. Driver integration can be matched to an analog display interface or to a fully digital display interface. In the former case, key circuit components, such as buffers, shift registers, and steering gates, are required. In the last case, digital-to-analog converters (DACs) as well as analog-signal amplifiers (opamps) are needed, in addition to the components listed for the analog interface scheme (see Fig. 4.4).

Advance in low-temperature poly-Si technology as well in the development of wide-process margin circuits have enabled manufacturers to push the level of on-the-panel integration of display drivers circuits [8,10]. One motivation for higher integration is the reduction of the power consumption of the panel. Power consumption is critically dependent on the driving voltage of the panel. The most effective way to reduce the power consumption is to lower the voltage of the driving circuit¹¹ (see Fig. 4.5). However, the performance of the poly-Si devices limits the extent of such reduction in two ways: (1) The operating speed of the

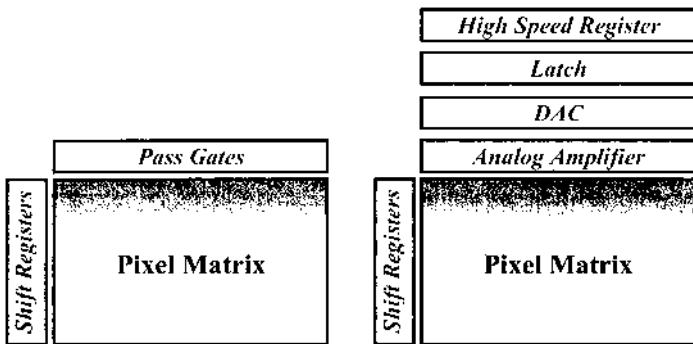


FIGURE 4.4 Block diagram for a display with integrated drivers with (left) analog interface or (right) digital interface.

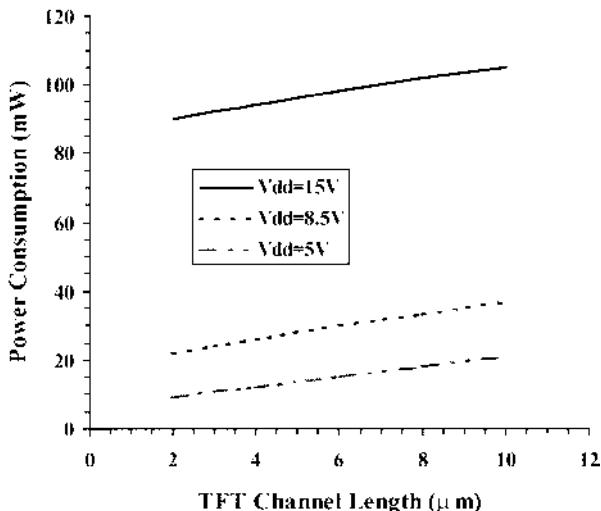


FIGURE 4.5 Estimated power consumption for a 2-in. LTPS LCD TFT panel (with an assumed TFT mobility of $120\text{ cm}^2/\text{V}\cdot\text{s}$), as a function of circuit driving voltage and TFT channel length. (From Ref. 11.)

circuit also decreases as the driving voltage decreases. This can be compensated by raising the mobility of the poly-Si devices and/or by decreasing the channel length (the latter approach being much more effective than the former). (2) The TFT threshold voltage is critically related to the minimum driving voltage. As the driving voltage decreases, it imposes very severe requirements not only on the absolute value of the device threshold voltage but, even more critically, on the acceptable scattering of the threshold voltage around its mean. Therefore, both high-quality poly-Si material (which enables the realization of high mobility and low threshold voltage) and advanced fabrication technology (which produces reliable, short-channel devices with superior uniformity) are needed to meet such demands.

Digital display interface circuits are very attractive from the point of view of increasingly sophisticated system integration (i.e., for mobile applications), as well as low power consumption. It is expected that, in the near future, LTPS TFT LCDs with built-in DACs will be mainstream technology [12]. To achieve integration of DACs with sufficient bit depth, the device design rule needs to decrease. For example, near-micron device rules will be required to accommodate the integration of 6-bit DACs on panels featuring resolutions of better than 150 pixels per inch (ppi) (see Fig. 4.6). Memory-on-pixel is another technology that aims to reduce power consumption, especially for mobile devices (when operating

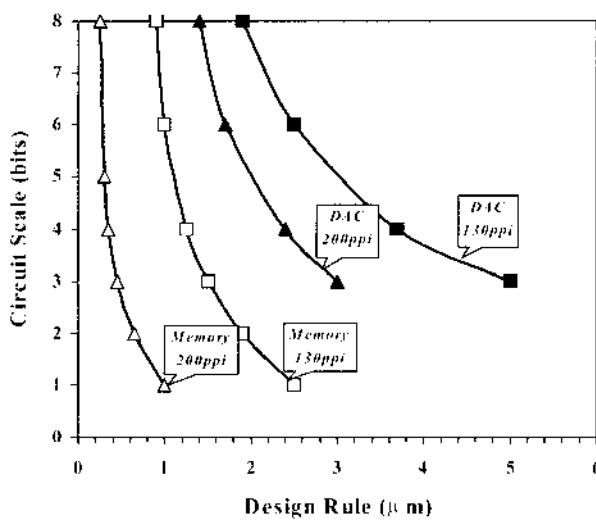


FIGURE 4.6 Relationship between TFT design rule and stage of circuit integration. (From Ref. 11.)

in still-picture mode). In a similar fashion to DACs, the development of “smart” pixels depends upon the generation of design rules. For example for near-micron design rules, [Figure 4.6](#) suggests that 1 bit on-pixel-memory can be built on a display that features a resolution of 200ppi.

The improvement in poly-Si TFT characteristics as well as the increased sophistication in the TFT fabrication process will also enable the on-the-panel integration of high-speed timing controllers. [Figure 4.7](#) shows results from simulations of the operating frequency of shift registers as a function of TFT mobility and channel length [11]. These results suggest that in order to push the clock operating frequency to an appropriate range compatible with driving displays with at least VGA resolution, minimum mobility of $\sim 200 \text{ cm}^2/\text{V}\cdot\text{s}$ is needed, in addition to 2- μm design rules. As the panel resolution increases beyond VGA, even smaller design rules are required to meet the theoretical specifications.

The analysis of the performance requirements for the various circuit components indicates that gradual improvement is needed in three key parameters of the LTPS TFTs. These are: (1) TFT mobility, (2) TFT threshold voltage, and (3) TFT design rules. Even though each of these areas has a unique impact on circuit performance, it is practically impossible to significantly vary one of these parameters without impacting (intentionally or unintentionally) the other two. This is the result of the complex relationship between these parameters and the materials

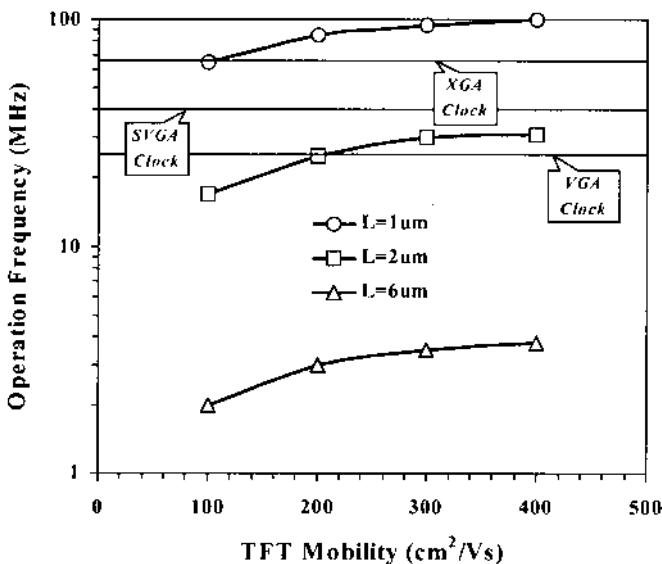


FIGURE 4.7 Simulation of shift register operating frequency as a function of TFT mobility and TFT channel length.

characteristics of key layers of the TFT device coupled with the TFT fabrication sequence itself. The task of producing high-quality, low-power-consumption, on-panel circuits should be tackled first by improving the TFT mobility, followed by a parallel effort on reducing the threshold voltage and its distribution and adopting finer design rules. To accomplish these goals a massive effort is required in a number of different areas (material and process technology). Table 4.1 presents a composite technology roadmap for LTPS TFT LCDs [11,13,14]. The bolded block represents key technology areas that will be discussed in detail in the ensuing sections.

TABLE 4.1 LTPS Technology Roadmap

		Year (from 2001)		
		+1	+3	+8
Panel	Resolution	100 ppi	→	150–200 ppi → 200 ppi
Driver	Peripheral driver type	Digital/analog	→	Digital
	DAC integration	3–4 bit	→	6 bit → 8 bit
	Integration of built-in memory		1–2 bit	→ 2–3 bit
	Timing controller speed	QVGA	→	VGA → XGA
Device	TFT structure		Self-aligned top-gate GOLDD	
	Design rule	5 μm	→ 1.5 μm	→ <1 μm
	TFT mobility	150 cm ² /V-s	→ 300 cm ² /V-s	→ >400 cm ² /V-s
	TFT V_{th}	5 V	→ 2–3 V	→ <1.5 V
	V_{th} Deviation	±1 V	→ ±0.5 V	→ ±0.2 V
Process	Gate metal	Cr, Mo, MoW	→	Al, Cu
	Metal interconnect etching	Al Wet/dry	→ Dry	Cu
	a-Si Deposition	PECVD	→ Low-H ₂ PECVD	→ Low-H ₂ PECVD, sputtering
	Crystallization	Std. ELA, MILC	→	Adv. ELA
	Gate insulator	PECVD-TEOS	→	Stack for Si/SiO ₂ interface control
	doping	Ion Doping	→	Ion doping, ion implantation
	Activation	ELA, Furnace	→ RTA	→ Adv. RTA

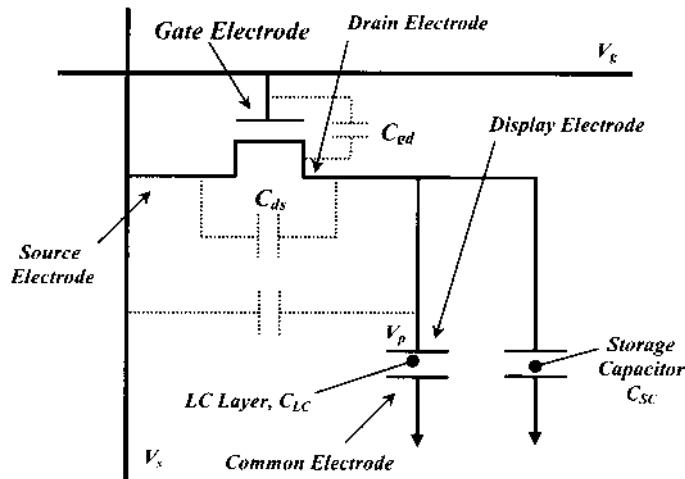


FIGURE 4.8 Equivalent circuit for an LC pixel.

4.2.2 Pixel Thin-Film Transistor Requirements

Figure 4.8 shows the equivalent circuit for a pixel in a TFT LCD panel. The liquid crystal layer and a storage capacitor are connected in parallel, as load to the TFT. Figure 4.9 explains the function of the TFT switch during the operation

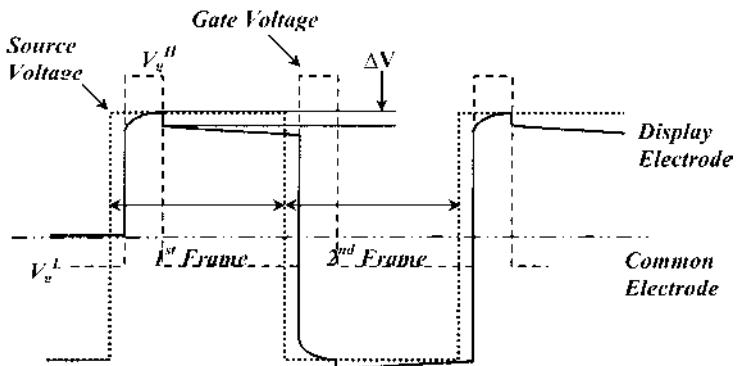


FIGURE 4.9 Display electrode voltage variation during typical pixel driving conditions (frame-reversal driving scheme is shown).

of the panel. The TFT turns on when a positive voltage pulse is applied to the gate electrode. As a result, the signal voltage (voltage applied to the source electrode) can be transmitted to the drain and, subsequently, to the liquid crystal layer and the storage capacitor that are connected as load to the TFT. During this operation, the pixel voltage (display electrode voltage) rises with the gate pulse, up to a maximum that, ideally, equals the source electrode voltage. This voltage will then be maintained in the pixel throughout the frame time, until another gate voltage pulse changes the state of the pixel. Typical frame times are on the order of 15–20 ms, while the time it takes to write a signal voltage is on the order of 20–30 μ s (i.e., three orders of magnitude lower). As a result, a storage capacitor is needed to maintain the proper voltage on the display electrode, until the next signal voltage is written on the pixel in the next frame. In practice, ideal pixel charging cannot be achieved due to the parasitic capacitive coupling between the various electrodes, as shown in [Figure 4.8](#). As a result, transient voltage changes (ΔV) occur in the waveform of the display electrode that produce an imbalance in V_p and give rise to image “sticking.” The value of ΔV depends critically upon the parasitic capacitance C_{gs} , as shown in Eq. (4.1). This relationship points out that to reduce signal distortion, one needs to either decrease the parasitic gate-to-drain capacitance or increase the denominator in Eq. (4.1). Regarding the latter approach, the only effective way to accomplish it is by increasing the capacitance of the storage capacitor. The price for doing that is usually in pixel aperture ratio, because to increase the C_{SC} capacitance one is forced to increase the area occupied by the capacitor. New high- k dielectric materials may allow increases in the C_{SC} capacitance without the associated drawback of real estate loss on the pixel. The most important measure, however, for reducing signal distortion is the elimination/reduction of the parasitic coupling between the gate and drain electrodes:

$$\Delta V = \frac{C_{gd}}{C_{gd} + C_{SC} + C_{LC}} (V_g^H - V_g^L) \quad (4.1)$$

As the resolution of poly-Si TFT displays increases, the area of the pixel decreases for a given display form factor. Therefore, the areas occupied by both the pixel-TFT and the associated storage capacitor need to be minimized. This translates to requirements for the pixel TFTs of high ON-current, to fully charge the pixel within increasingly shorter frame time, and low OFF-current, to reduce pixel charge leakage and enable reduction of the size of the storage capacitor. As mentioned, earlier, next generation “smart” pixels may integrate additional features, which necessitates careful management of pixel real-estate to maintain the display aperture ratio within an acceptable range.

4.3 METHODS FOR DEPOSITING THIN SILICON FILMS

Unlike crystal-Si MOSFETs, where part of the single-crystal silicon substrate becomes the device active layer, in the case of poly-Si TFTs the active layer

needs to be formed on the host substrate. The first step to accomplish this is the deposition of a silicon thin film. The microstructure of this silicon film can vary, depending upon the deposition method and conditions. Typically, the Si thin film is deposited in the amorphous phase and is transformed to poly-Si in a subsequent crystallization step.

The method of choice for the deposition of Si-precursor is plasma-enhanced chemical vapor deposition (PECVD). As the term implies, PECVD employs plasma to promote the chemical decomposition of appropriate gaseous species that eventually condense on the surface of the substrate to form a continuous film. In the case of Si deposition, silane (SiH_4) and hydrogen (H_2) gases are typically combined. Different reasons have led PECVD to be the method of choice for Si deposition. Silicon films deposited by PECVD typically feature high hydrogen content (i.e., $\sim 8\text{--}20$ at. %), which is beneficial for applications requiring a-Si thin films (such films are referred to as a-Si:H). Starting from solar cells and then to a-Si-based AMLCDs, the high hydrogen content in the film was essential for the fabrication of high-quality a-Si devices (i.e., to achieve high solar cell efficiency and high a-Si TFT mobility). As a result, significant effort has been placed on the development of sophisticated hardware to achieve high productivity and to eliminate manufacturing problems (e.g., particle formation, process repeatability). Over the years, a significant number of such pieces of equipment have been installed in LCD factories worldwide, providing a large installed base that allowed the technology to mature.

The maturity of PECVD and the associated “comfort” of manufacturers provide the impetus for its application in poly-Si technology. However, even from the beginning in the evolution of poly-Si TFT technology it became apparent that the deposition of the silicon film is intimately related to the quality of the resulting poly-Si microstructure [15,16]. Historically, low-pressure chemical vapor deposition (LPCVD) has been suggested as the optimal method for the formation of good-quality poly-Si films [16]. This was partly because LPCVD-formed Si films were easier to transform to poly-Si via a low-temperature annealing step following deposition [17–20]. Using the LPCVD method, a variety of as-deposited microstructures were possible, a fact that enabled different crystallization schemes to be implemented to enhance the properties of the resulting poly-Si microstructure (see [Fig. 4.10](#) and [Sect. 4.4](#) for more details).

The advent of the laser crystallization method freed, to a significant extent, the choice of Si-deposition method, for the localized film melting (made possible by laser annealing) erased the prior film-processing history. Laser crystallization, however, did not bode well with the high hydrogen content in the as-deposited a-Si:H films. The extremely high temperature gradients during laser annealing produced explosive out-diffusion of hydrogen from the film, resulting in the development of excessive porosity and surface roughness [21,22]. To alleviate this problem, an interim solution has been suggested consisting of an added step

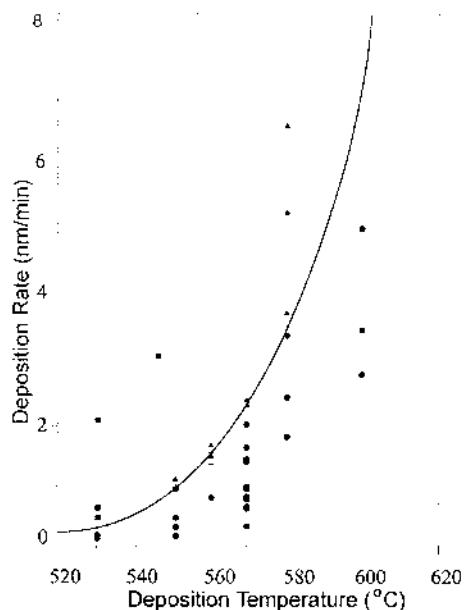
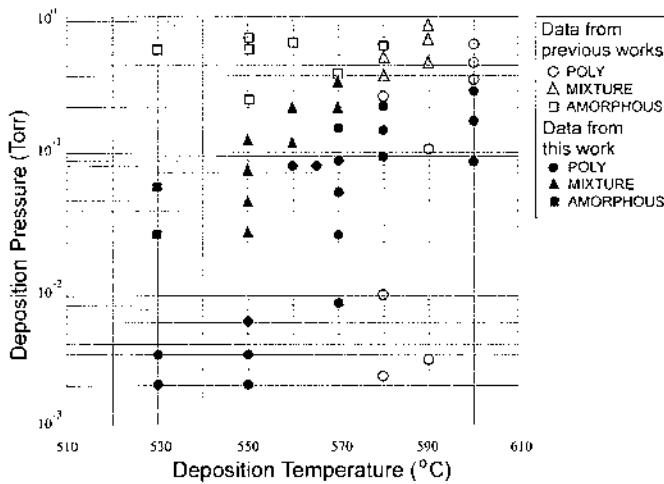


FIGURE 4.10 Phase diagram of as-deposited LPCVD Si films. (left) As-deposited film microstructure as a function of deposition temperature and pressure. (right) As-deposited film microstructure as a function of deposition temperature and rate. A clear delineation of the microstructure from poly-Si to mixed-phase Si to a-Si is observed as the rate increases at any given deposition temperature. (From Ref. 18.)

that aims to reduce the hydrogen content of the film to levels compatible with laser annealing. This process, so-called “dehydrogenation,” can be accomplished by a low-temperature (i.e., 400–500°C) thermal anneal or by laser annealing at gradually increasing fluence, starting from a very low fluence range [23] (i.e., close to the surface-melting threshold of the film). These tactics are effective in rendering a-Si:H films compatible with laser crystallization.

From the point of view of productivity, the additional dehydrogenation step is undesirable. This step may require an additional piece of equipment and adds unwanted overhead time to the manufacturing line. To address this issue, equipment makers are reassessing their conventional PECVD tool designs in an effort to produce tools that are better suited to the specific needs of poly-Si technology. Equipment makers such as AKT and ULVAC are developing new cluster tools (see, for example, Fig. 4.11) that feature technologies aiming to produce precursor-Si films with low hydrogen content. In the case of AKT, the heat chamber is specifically designed to perform dehydrogenation without additional time overhead.

Figure 4.12 shows the effect of substrate temperature on the film’s hydrogen content and the evolution of hydrogen content as a function of postannealing time. These data indicate that a-Si films with low hydrogen content [24,25] can

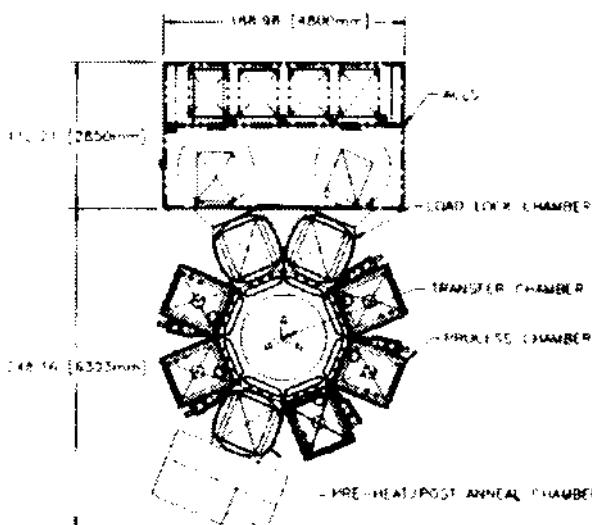


FIGURE 4.11 Cluster tool architecture for the deposition of dehydrogenated poly-Si film precursor. The preheat/postanneal chamber is redesigned to achieve substrate temperatures as high as 500°C. (From AKT and Ref. 24.)

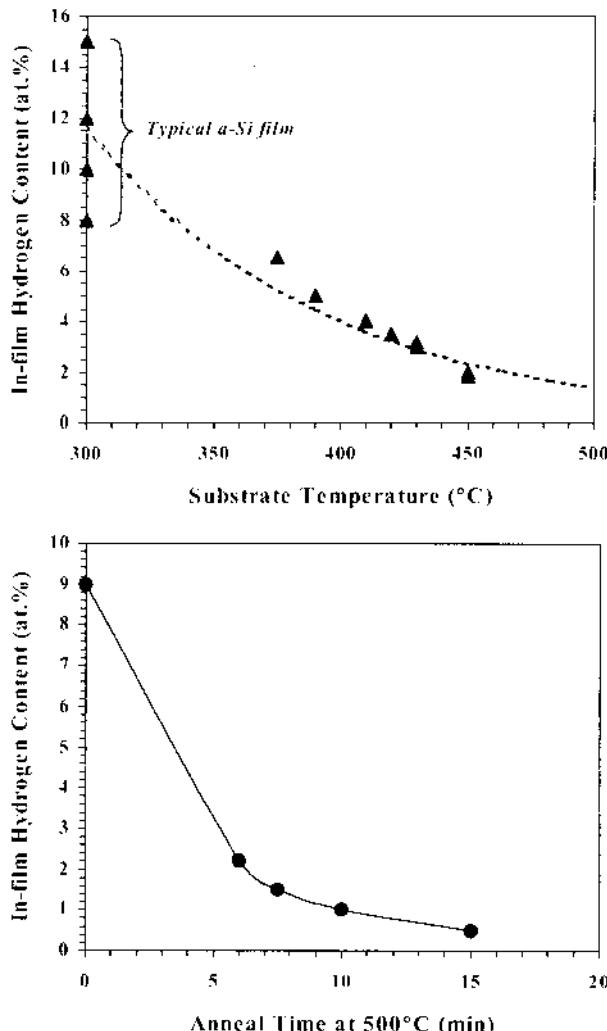


FIGURE 4.12 Hydrogen content in PECVD a-Si films. (left) In-film hydrogen content as a function of substrate temperature. (right) In-film hydrogen content as a function of annealing time at 500°C. (Data from Ref. 24.)

be obtained by merging the dehydrogenation process step on the same cluster tool that is used for the Si-film deposition. Other equipment makers opt for a different solution. In the case of ULVAC, gaseous species are decomposed in a high-frequency plasma (27.12 MHz instead of 13.56 MHz) to achieve low hydrogen content at a deposition temperature of \sim 400–450°C. Figure 4.13 compares the FTIR spectrum of a conventional a-Si:H to that obtained from the advanced process developed by ULVAC. It should be noted, however, that the effect of chemistry is much weaker than the effect of temperature when it comes to hydrogen content. In other words, it will be very difficult to achieve sufficiently low hydrogen content in a-Si films without raising the substrate temperature to at least 400°C.

The requirements for Si-precursor deposition are summarized in Table 4.2. Besides the PECVD method, physical vapor deposition (PVD) has also shown significant promise as far as meeting such requirements [26]. One of the key advantages of sputtering is the ability to form Si films with virtually zero hydrogen content. In addition, PVD technology eliminates explosive/pyrophoric gases, which are typically used with conventional Si deposition methods. A number of studies have assessed the performance characteristics of PVD-based poly-Si TFTs (see Table 4.3) [27–32]. The findings suggest that optimized PVD poly-Si films are similar in quality to PECVD Si films. One issue that requires consideration is the incorporation of Ar atoms in sputtered Si films (see Fig. 4.14, top). Such incorporation may negatively affect the TFT performance, and thus it needs to be restricted [33,34]. Particle formation is more pronounced in sputtering technology, due to poorer adhesion of Si and the lack of in situ chamber cleaning. However, recent results indicate that with proper chamber conditioning and imple-

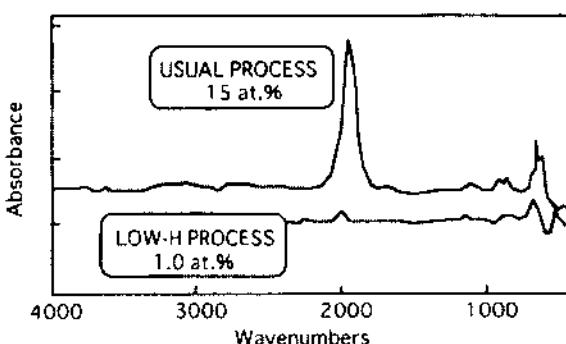


FIGURE 4.13 Comparison of FTIR spectra from a conventional a-Si:H film and from an advanced a-Si film obtained using ULVAC's low-hydrogen process. (Ref. 25.)

TABLE 4.2 Deposition Requirements for Si-Precursor and Comparison PECVD and PVD Techniques

Attribute	Target	PECVD	PVD
Throughput (for ~500-Å films)	<1 sub/min	○	○
Uniformity	< $\pm 5\%$ (600 × 700 mm ²)	○	○
Hydrogen content	<2 at.%	● → ○ (only by annealing at 500°C)	○
Sequential deposition of BC/a-Si layers	Process needed for interface control	○	Under development
Vacuum quality (for interface quality control)	Better vacuum may be needed for future applications	●	○
Particle formation		○	● → ○
Compatibility with plastic substrates	Desirable	●	○
Installed base COO		○	● Under evaluation

○ = good, ● = fair, ● = poor.

TABLE 4.3 Characteristics of nMOS p-Si TFTs Made with PVD Si-Precursor

Group [Ref.]	PVD method	T _{dep} (dep. only)	GI method	S/D doping	μ _{FE} (cm ² /V-s)	V _{th} (V)	T _{max} (flow)
Sharp [12]	DC	100–400°C	PECVD	I-I ^a	180	2	750°C
Sony [13]	RF	110°C	PECVD	P-D&ELA ^b	250	3	110°C
LLNL [14]	DC	RT	PECVD	P-D&ELA	60–100	6–8	150°C
LLNL[15]	DC	RT	LTO ^d	GILD ^c	200	2–3	350°C
UCB [16]	P-DC ^f	RT	HDP ^e	P-D&ELA	71	2.5	100°C
Intevac [17]	P-DC	70–100°C	PECVD		50–100	1–3	
NTT [18]	RF	200°C	RF-PVD	I-I	350	2	650°C

^aI-I: Ion implantation.

^bP-D&ELA: Plasma doping followed by ELA.

^cGILD: Gas-immersion laser doping.

^dLTO: Low-temperature oxide.

^eHDP: High-density Plasma (ECR).

^fP-DC: Pulsed-DC sputtering.

Source: Ref. 26.

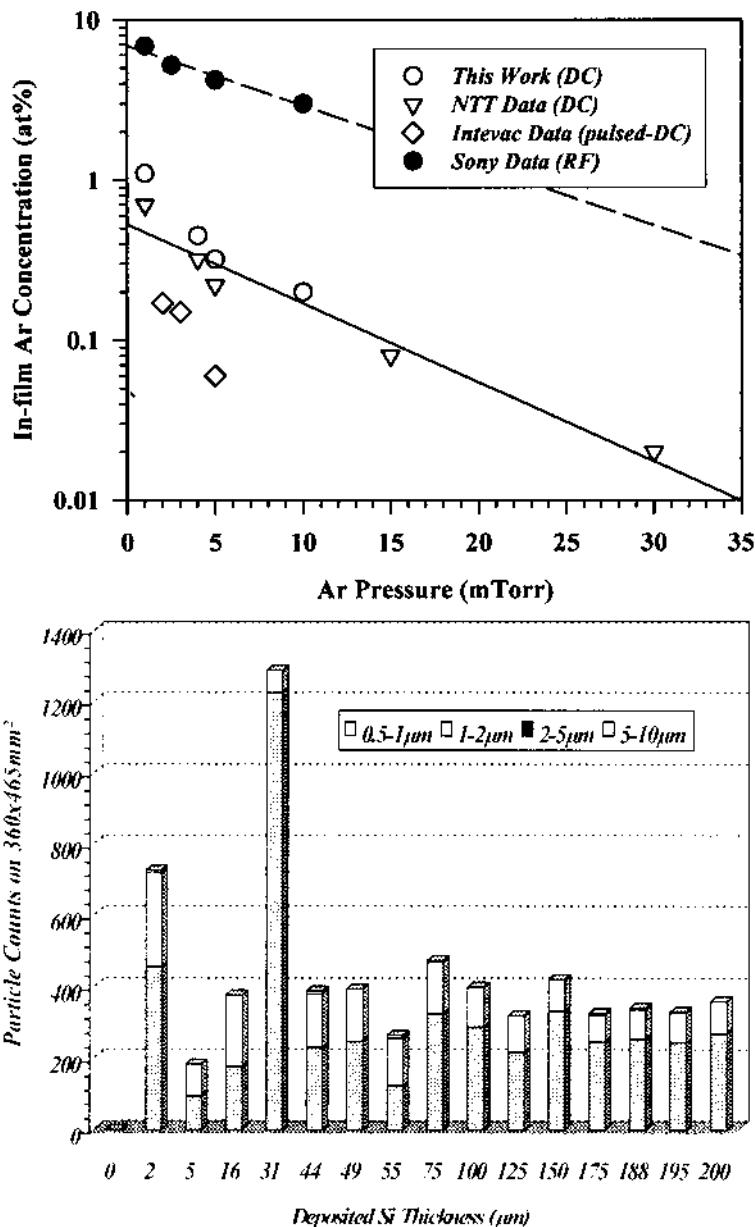


FIGURE 4.14 (top) In-film Ar content vs. Ar-pressure in sputtered Si films. (bottom) Particle counts vs. sputtered deposited Si-film thickness. (Data from Ref. 26.)

mentation of vertical geometry, particle levels can be kept within acceptable limits (see also Fig. 4.14, bottom). The advances in Si-sputtering technology and its promise can be epigrammatically summed up by the recent efforts of equipment makers to develop and market Si-sputtering tools for poly-Si TFT applications. This suggests that polysilicon technology is considered as being beyond the stage of a mere research curiosity.

In recent years another trend has emerged in which the Si-precursor deposition is “clustered” with a number of other deposition steps, including the crystallization process (specifically laser annealing) and/or gate insulator formation. This trend parallels analogous efforts in the IC industry as far as realizing cleaner interfaces between critical device layers (see Fig. 4.15). Such efforts have stemmed from research studies that have demonstrated a large performance improvement under conditions that promote high interface quality, especially for the poly-Si/GI interface [35]. ULVAC [25], Matsushita Electric [36], and Hitachi Ltd. with Kokusai Electric Co. [37] have all developed similar cluster tool architectures that merge the deposition and laser annealing steps. In such tools, base-coat (B/C) and a-Si films are deposited sequentially on the glass substrate, followed by laser crystallization and (optional) deposition of the gate dielectric film, without breaking vacuum. In this manner, high-quality devices have been fabricated that boast significant performance gains over their counterparts in which critical interfaces were exposed to air [35]. The one significant disadvantage of such cluster tools is the added complexity associated with their manufacture and maintenance, which translates to a higher cost of ownership (COO) for the display makers. In addition, there is currently no single supplier that has combined laser annealing and deposition expertise, which makes it more difficult to respond effectively to customer demands regarding process development, equipment maintenance, and failure recovery. If, however, such process integra-

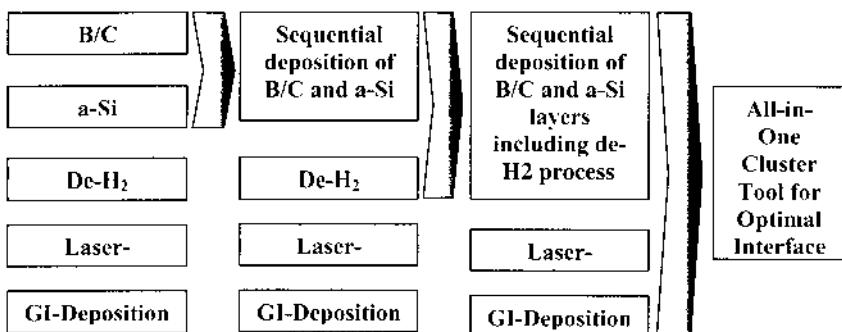


FIGURE 4.15 Trends in process integration within the same cluster tool.

tion has the merits that the various studies allude to, we can expect to witness a transformation in the equipment industry.

4.4 AMORPHOUS SILICON CRYSTALLIZATION

Within the context of poly-Si TFT technology, “crystallization” refers to the step (or steps, if more than one) that are required to prepare, from the as-deposited, precursor-Si material, the poly-Si material that will be used as the TFT active layer in the final device. Depending upon the selected method, the complexity of the crystallization process (hence its cost) can vary substantially. Similarly, the (electrical) performance of the resulting poly-Si film differs significantly, depending upon the crystallization scheme. Thirdly, the uniformity of the resulting microstructure (hence, to a large extent, the uniformity of TFT characteristics) is also a strong function of the applied crystallization method. Finally, the crystallization process needs to be compatible with the temperature-sensitive substrates that are typically used in display applications. These four constraints (performance, uniformity, temperature compatibility, and process economics) form the basis of our discussion of crystallization technology. Historically [38], solid-phase crystallization (SPC) was the first technology to produce poly-Si films for display applications, followed by laser annealing crystallization (LAC). Both technologies evolved significantly over the past 20 years, and state-of-the-art versions of each are finally finding their way to poly-Si TFT display manufacturing.

4.4.1 Solid-Phase Crystallization Process

The most direct method of obtaining poly-Si films from initially amorphous precursor-Si films is via SPC in a furnace environment. Amorphous silicon is a thermodynamically metastable phase possessing a driving force for transformation to polycrystalline phase given sufficient energy to overcome the initial energy barrier. Solid-phase crystallization can be accomplished within a wide annealing temperature range that requires a similarly wide range of annealing times (i.e., time required for complete transformation of the precursor-Si film to poly-Si). The relationship between annealing temperature and annealing time, however, is not unique. In other words, depending upon the microstructural details of the precursor-Si film, different annealing times have been observed at the same annealing temperature [18]. A key factor affecting crystallization is the nucleation rate in the precursor-Si film. The nucleation rate is strongly influenced by the selected deposition method and conditions [39,40]. The structural order/disorder in the precursor film affects the ability of the film to form supercritical nuclei (i.e., stable nuclei) when subjected to thermal annealing. The structural order is, in turn, affected by deposition parameters such as temperature and deposition rate [39,41,42] ([Fig. 4.16](#)). As the temperature decreases and the deposition rate

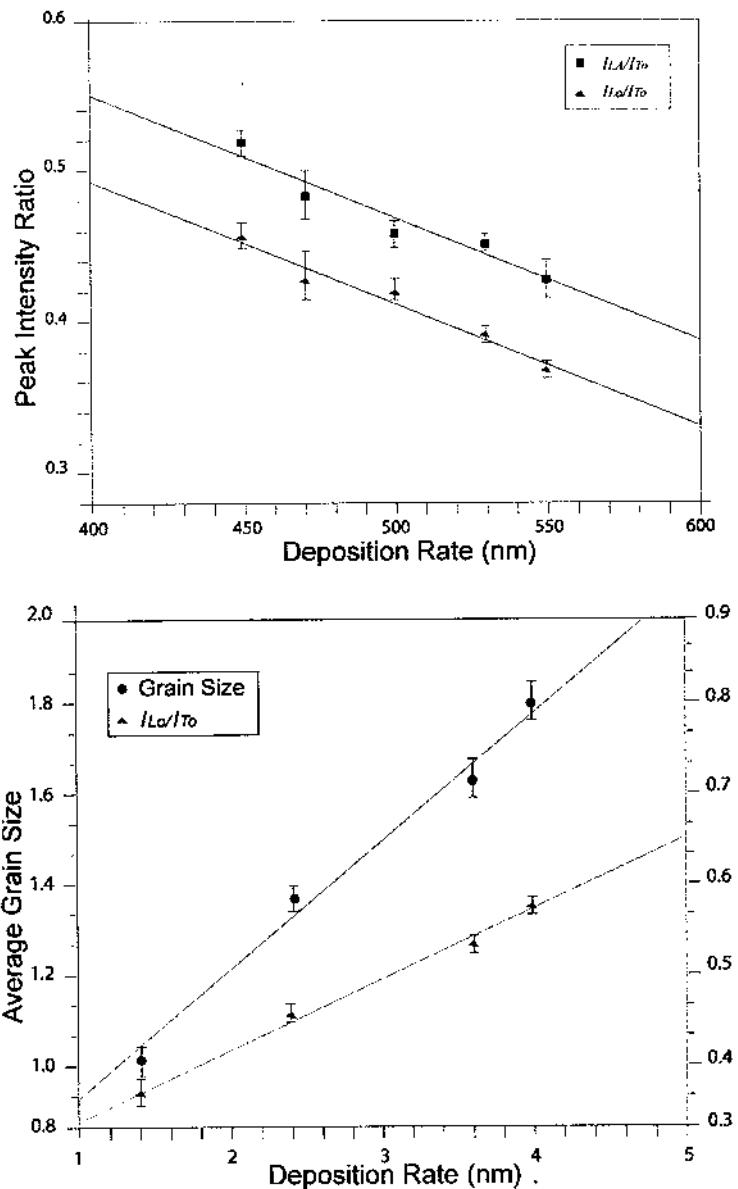


FIGURE 4.16 Correlation between a-Si Raman spectrum's LA, LO, and TO peak intensity ratios and film deposition temperature and rate. The higher values of LA/TO and LO/TO peak ratios are suggestive of a higher structural disorder in the silicon network of a-Si films. (From Ref. 44.)

decreases, films are formed having a higher degree of structural disorder (thus, more difficult to nucleate). Similar structural disorder also occurs upon implantation into the Si film. This concept has been used in the past to achieve selective preamorphization in Si films as a way to increase grain size [43,43]. It is noted that the same mechanism (amorphization induced by ion implantation) is believed to be responsible for the pervasive nucleation difficulty that, in general, characterizes a-Si films deposited by physical vapor deposition (i.e., sputtering) vis-à-vis other deposition techniques (Fig. 4.17).

One aspect that helps nucleation during SPC is the presence of pre-existing, supercritical nuclei clusters in the film. Such pre-existing clusters act as nucleation seeds, thereby eliminating the need for initial nucleation in the film. If the density of pre-existing crystallites in the as-deposited film is too high, the resulting grain size after crystallization will be correspondingly small. Therefore, the density of nuclei and the poly-Si grain size are inversely related to each other [40]. Typically, large and uniform grain size is sought in order to minimize the number of grain boundaries incorporated in the active layer of poly-Si TFTs. Therefore, a balance is needed between the number of nuclei generated within a given volume of material and their growth characteristics. Ideally, a small number of fast-growing

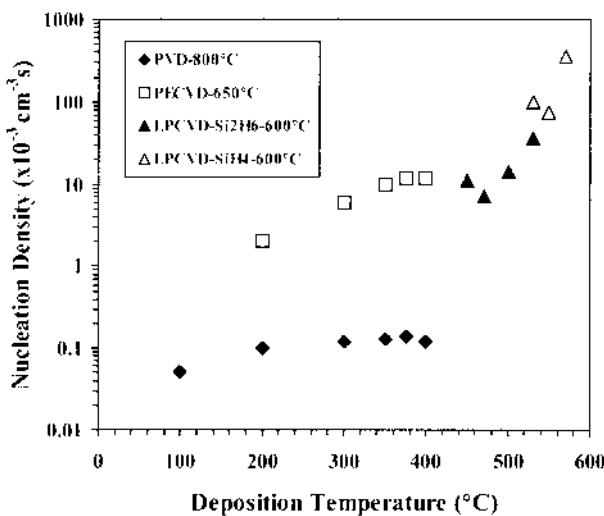


FIGURE 4.17 Nucleation rate in a-Si films as a function of deposition temperature and deposition method. Different annealing temperatures were used, as shown in the legend, due to inability of certain films to transform to poly-Si at low annealing temperatures.

nuclei are needed to maximize the grain size. However, the reality of the situation is that the probability that additional nucleation events will occur within the volume separating growing nuclei increases geometrically with the separation distance.

To meet this challenge, various schemes have been conceived to achieve the best of two worlds by combining methods aiming at yielding a microstructure where new nuclei events are relatively improbable and, at the same time, transformation is initiated from, and sustained by, the growth of crystallites that pre-exist in the as-deposited film. One such concept is the combination of a mixed-phase Si film (having crystallites embedded in an amorphous matrix) with an amorphous Si film [45]. In this configuration, the mixed-phase film is optimized for crystalline content (i.e., pre-existing nuclei density), whereas the a-Si film is optimized for “consumption” (i.e., is deposited at low temperature and high rate to ensure a very low nucleation rate) [46]. A rigorous mathematical treatment of the resulting average grain size of such “enhanced” poly-Si films is given in Ref. [41]. [Figure 4.18](#) shows an illustration of a “composite” Si film and the experimentally determined grain size and crystallization time resulting from varying the thickness of the amorphous component in a double-layer composite Si film deposited by LPCVD.

Despite the successes of traditional SPC methods in increasing grain size and reducing crystallization temperature, the crystallization time typically required for complete transformation tends to be rather long (i.e., 10–20 hr at 550°). The crystallization-time issue is further compounded by the use of PECVD as the deposition method for the precursor-Si film. The selection of this technique, even though suboptimal, has been driven by the prior application of PECVD technology in a-Si TFT fabrication. In an effort to shorten the crystallization time associated with the SPC process, two variations of SLC emerged and will be briefly discussed here.

4.4.1.1 Rapid Thermal Annealing (RTA)

This variation of the SPC process couples radiant energy, from either tungsten halogen or xenon arc lamps, directly to the Si film for short periods of time. The rapid thermal annealing concept has gained significant momentum ever since equipment manufacturers demonstrated production-worthy equipment suitable for large-area, glass substrates. In one case (RTP equipment made by Intevac), two linear xenon arc lamps are used to rapidly heat and crystallize the silicon film as it moves underneath the lamp housing. RTP technology promises higher throughout, lower cost, and better material uniformity.

The crystallization of amorphous silicon via the RTA process has been studied in detail through the use of statistically designed experiments [47]. [Figure 4.19](#) shows the relationship between the crystallization temperature of the RTA process and the resulting mobility of *n*-channel poly-Si TFTs. Figure 4.19, top,

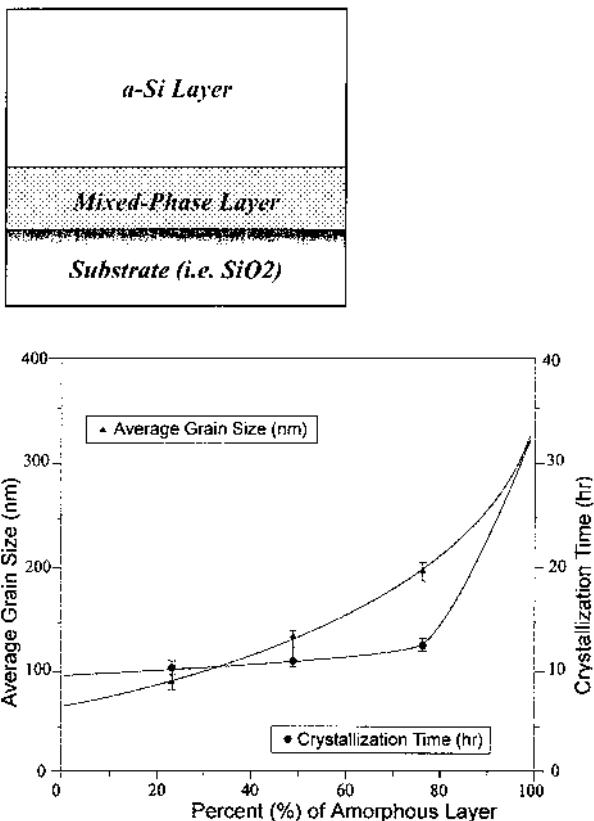


FIGURE 4.18 (top) Illustration of the “composite” layer concept for optimizing the microstructure and annealing time of SPC poly-Si films. (bottom) Experimental data on average grain size and crystallization time of composite, double-layer films as a function of the ratio (%) of amorphous to total film thickness. (From Ref. 46.)

emphasizes the effect of the deposition technique on the crystallization temperature and TFT performance. Typically, higher-mobility devices are obtained from crystallized-Si films deposited by low-pressure CVD (LPCVD) instead of plasma-enhanced CVD (PECVD). The performance of Si films deposited by LPCVD can be further classified depending upon the type of precursor gas used for the deposition. As shown in Figure 4.19, top films deposited with disilane gas enable higher mobility than films deposited with silane. This is traced back to the intrinsic properties of the as-deposited films, as a function of the gas precursor, which

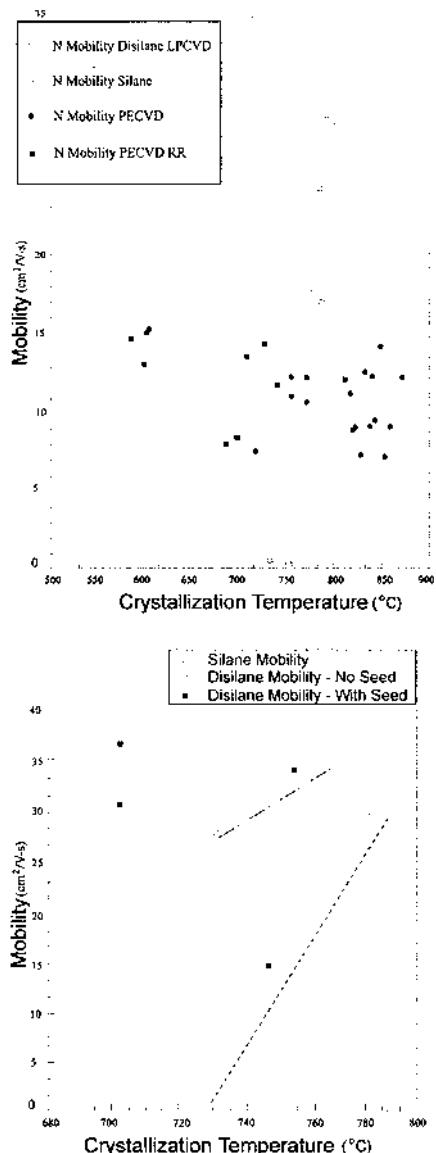


FIGURE 4.19 Correlation between crystallization temperature and *n*-channel TFT mobility for RTA-crystallized poly-Si films. (top) Effect of deposition technique. (bottom) Effect of process gas and “seed” layer. (From Ref. 48.)

have been characterized in detail in earlier studies [22,39]. In brief, disilane gas favors the formation of a-Si films with an increased degree of structural disorder that, in turn, yields poly-Si structures with larger grain size upon crystallization. The larger grain size is considered responsible for the increase in TFT mobility. The one drawback, however, is the typically higher crystallization temperature range required to effectively complete the phase transformation [39]. Addition of a “seed” layer has been found to alleviate this requirement, resulting in crystallization at lower annealing temperature, as shown in [Figure 4.19](#), bottom. The “seed” layer is essentially supplying nucleation sites and is a thin a-Si layer deposited at conditions that favor nucleation. Once nuclei are formed, they can then consume the a-Si film deposited by disilane gas without the need of nucleation within this layer. As discussed earlier, the concept of a composite layer was originally developed for furnace-annealing applications [45,46] but can be exploited in RTA crystallization as well.

The success of RTA, as far as reducing the crystallization time, is stained by the necessary increases in processing temperature. Even though the glass substrate stays at elevated temperatures for only short periods of time, the probability of deformation and/or breakage increases exponentially when the temperature is raised above a critical point. More expensive substrate (glass) may, thus, be needed to combine with RTA crystallization technology. Furthermore, RTA cannot resolve the other issue that typically plagues SPC poly-Si microstructure: the high intragrain (within grains) defect density that is observed in SPC-made poly-Si films. Such defects are commonly twin boundaries and microtwin formations ([Fig. 4.20](#)). In most cases, these grain defects are quite detrimental to the electrical characteristics of poly-Si films, for they generate energy barriers that inhibit free-carrier conduction. At least one report in the literature claims that a combined two-step annealing, consisting of low-temperature SPC followed by 30–45 seconds of RTA at 850°C, is effective in reducing the intragrain defect density [48]. However, there is very little certainty that (1) standard display glass will survive such high temperatures and (2) TFT performance gains from this process can outweigh the cost and other implementation problems of this annealing scheme. In fact, our TFT data made from poly-Si films annealed up to 850°C indicate no significant advantage over poly-Si films fabricated at lower crystallization temperatures (see [Fig. 4.19, top](#))

The main advantage of RTA technology in crystallization is process simplicity and microstructural uniformity. Even though RTA-crystallized poly-Si material will never compete head to head with poly-Si material obtained by other, more advanced crystallization methods (i.e., laser annealing), moderate mobility values in the range of 20–40 cm²/V-s with high uniformity can be useful in certain applications. One such application is found in the area of organic light emitting diodes (OLEDs), which can be fabricated in a matrix format and driven using active-matrix schemes. Since OLED TFTs are current-driven devices, they

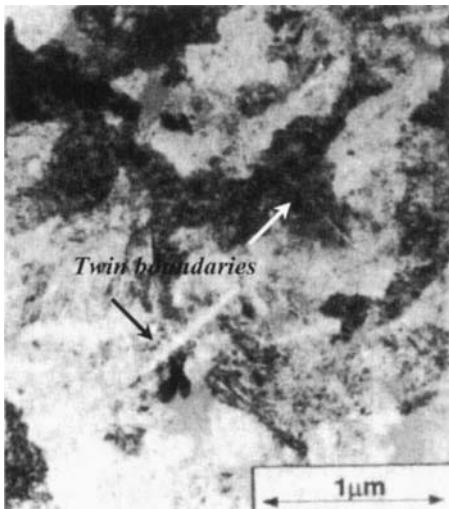


FIGURE 4.20 TEM photograph of the SPC poly-Si microstructure obtained by RTA or furnace crystallization of a-Si films. A large density of twin boundaries and microtwins is commonly observed within the dendritic poly-Si grains.

require uniform current to avoid brightness variations between pixels. In that case, RTA crystallization technology can provide a lower-cost alternative to meet such requirements.

4.4.1.2 Metal-Induced Crystallization (MIC)

The enhancement of c-Si growth in the presence of small amounts of a metallic phase has been known for more than 35 years [49]. Such enhancement has been attributed to an interaction of the free electrons of the metal with covalent Si bonds at the growing interface [50]. Furthermore, the growth enhancement has been reported for both elemental metals and metallic silicides. A nickel silicide system has received considerable attention for such application. When thin Ni is deposited on Si and annealed, Ni disilicide forms (NiSi_2) [51]. The disilicide has the cubic crystal structure and a very close lattice parameter match to c-Si (Δ of -0.4%). The disilicide is actually the species that mediates the transformation of a-Si to c-Si. The silicide-mediated growth of silicon occurs in three stages [52]. Initially (first stage), precipitation and growth of NiSi_2 occur in the temperature range of 325 – 400°C . The population of disilicide precipitates reaches a steady state, on arguments of a nucleation-excluded zone model that prevents additional nucleation around existing precipitates [52]. In the second phase, crystalline Si

nucleates on one or more of the eight {111} faces of the octahedral NiSi_2 . Finally, in the third phase, c-Si growth proceeds with a NiSi_2 precipitate at the planar advancing growth front. Figure 4.21 shows a schematic representation of the proposed NiSi_2 -mediated growth of c-Si. As a result of this growth mechanism, silicide-mediated poly-Si films demonstrate a fibrous microstructure, with each fiber attributed to c-Si growth from an individual disilicide precipitate.

In addition to Ni, other metals have been investigated as far as their effectiveness in enhancing Si crystal growth. These include Au, Al, Sb, and In, which form eutectics with Si [53,54], and Pd and Ti, which form silicides with Si [55]. However, in all of these cases several issues were reported pertaining to the actual enhancement of the growth rate at sufficiently low crystallization temperatures (i.e., 500–550°C) and the incorporation of metal impurities in the TFT active layer. As a result, Ni today remains the undisputed metal of choice for silicide-assisted crystallization. It should be noted that traces of NiSi_2 also remain within

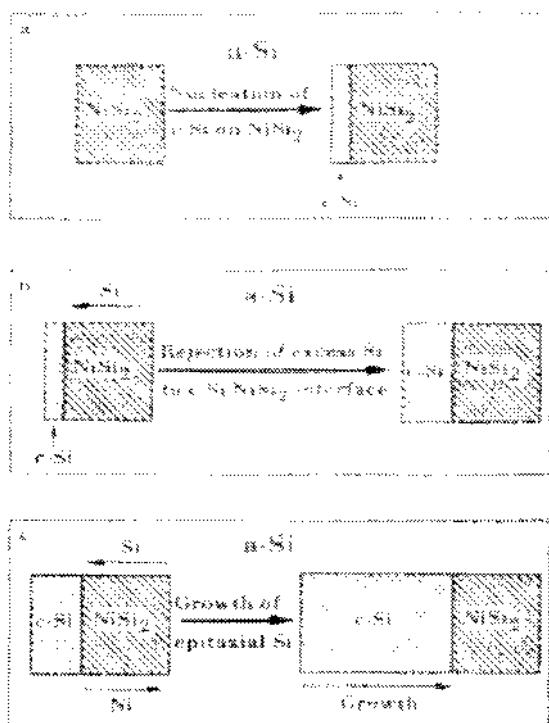


FIGURE 4.21 Schematic representation of the proposed NiSi_2 -mediated growth of c-Si. (From Ref. 52.)

the c-Si material that is left behind after the growth phase. This would have presented an insurmountable obstacle had it not been for the existence of an efficient gettering process [56]. This process utilizes the implantation of phosphorous, followed by low-temperature annealing (at $T < 550^{\circ}\text{C}$) to generate electrically inactive compounds. Previous studies have demonstrated the effectiveness of the gettering process in removing the remaining silicide in the film after Si crystallization [57].

In practice, the necessity to maintain a low processing temperature poses certain limitations on the quality of the poly-Si microstructure formed via the MIC process. One way to boost the material characteristics is by combining MIC with the laser annealing process [58,59]. This combination has been found to produce high-quality material while at the same time alleviating some of the issues associated with the conventional laser annealing process (discussed in more detail next). Figure 4.22 illustrates the Ni introduction and shows part of the poly-Si TFT fabrication flow for the MIC process developed and established by the Sharp Corporation [60].

In recent years, another variation of the MIC process has been proposed, to boost the Si-crystal growth rate and allow the additional reduction of the crystallization temperature. In this case, an electric field superimposed on the sample during MIC process was found to enable reduction of the crystallization temperature to as low as 380°C . Different models have been invoked to explain the increase in the crystal growth rate under the applied electric field [61]. Figure 4.23, left, shows the optimum field strength as a function of crystallization temperature [61]. It should be noted that the electric field is constrained by the Joule heating effect, which eventually causes the sample to crystallize by conventional

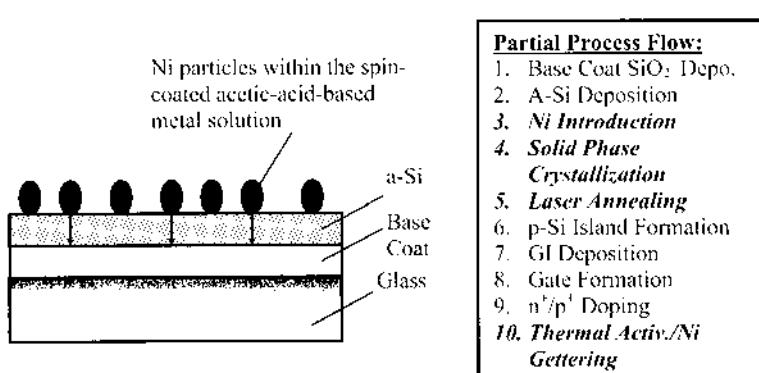


FIGURE 4.22 Illustration of the Ni introduction method and TFT fabrication flow. (From Ref. 60.)

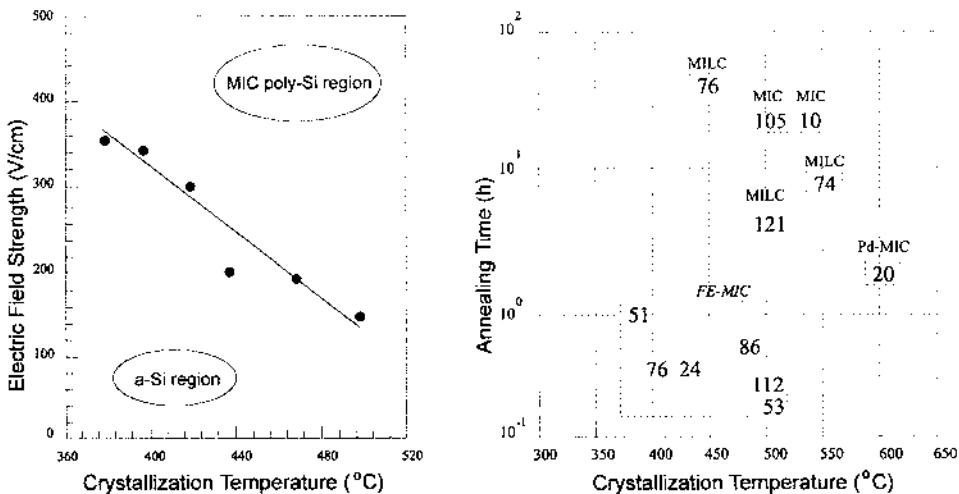


FIGURE 4.23 (left) Relationship between crystallization temperature and optimum applied electric field in the FE-MIC method. (From Ref. 48.) (right) Relationship between annealing time, crystallization temperature, and poly-Si TFT mobility for the MIC and field-enhanced (FE) MIC crystallization schemes [62]. Data indicated as “This work” and “Previous work” refer to FE-MIC samples. (From ref. 62.)

SPC. Figure 4.23, right plots the poly-Si TFT mobility as a function of annealing temperature and annealing time for MIC and field-enhanced (FE) MIC crystallization schemes [62]. Clearly, the advances in SPC made possible by the catalytic action of trace amount metals in silicon has enabled a tremendous improvement in both poly-Si TFT performance, as well as the reduction of the crystallization temperature.

4.4.2 Excimer Laser Crystallization (ELC)

Excimer laser is a type of gas laser where the lasing medium is composed of an inert atom and a halide atom (i.e., Cl, F, I). The name *excimer* itself is an abbreviation of “excited dimer,” meaning a diatomic excited molecule with the same atomic composition (e.g., Xe–Xe). However, the term *excimer* has also been extended to molecules (e.g., XeCl). Excimer lasers feature wavelengths in the UV range of the spectrum. For Si annealing applications, excimer wavelengths of 193 nm, 248 nm, 308 nm, and 351 nm have been used, corresponding to ArF, KrF, XeCl, and XeF gas mixtures, respectively. All of these wavelengths are well suited to Si crystallization, for a-Si absorbs very strongly in the UV range. Therefore, the energy in the incident laser pulse is strongly absorbed within only

the first few monolayers of the film (i.e., within 60–100 Å of the surface of the Si film), and this causes very rapid heating and melting to occur within the Si film. From productivity and cost considerations, the excimer laser of choice for Si crystallization is XeCl (308 nm). At this wavelength, a-Si absorbs very strongly (absorption coefficient is $\sim 10^6 \text{ cm}^{-1}$), whereas the cost and lifetime of the associated optics, which are used to shape and image the laser beam onto the surface of the Si film, are suitable for mass production operations. Typical excimer lasers operate in pulse mode, at frequencies around 300 Hz, with pulse duration in the range of 10–50 ns. The energy output of TFT production excimer lasers (e.g., Lambda Physic STEEL series [63]) is on the order of 0.6–2 J. It should be noted that very powerful XeCl excimer lasers, developed by the European maker SOPRA, have also been tested for Si annealing application [64]. In that case, the energy of the laser is $\sim 15 \text{ J}$, the pulse duration $\sim 220 \text{ ns}$, and the discharge frequency $\sim 1\text{--}5 \text{ Hz}$. It is now well understood that the pulse-to-pulse repeatability of the excimer laser is the most important key attribute of the laser equipment, followed by the discharge frequency, output energy, and pulse duration. It is convenient to use a simple classification scheme to understand the impact of each laser parameter to (1) productivity and (2) film quality. In that sense, pulse-to-pulse repeatability, discharge frequency, and output energy affect primarily productivity, whereas pulse duration affects primarily the film quality. As productivity tends to be the number-one priority in manufacturing operations, laser equipment featuring excellent repeatability and high discharge frequency (with reasonable output energy) are preferable. The pulse-to-pulse repeatability of state-of-the-art laser equipment configured for a Si annealing application is currently in the 6–9% (3σ) range. This number is expected to decline further to $\sim 4\%$ within 3 years.

4.4.2.1 General Overview

Analysis of the transformation scenarios associated with excimer laser crystallization show that one can categorize the ELC of Si films in terms of two major transformation regimes (occurring at low and high laser fluence, respectively) and one minor transformation regime in between (the so-called superlateral growth, or SLG) [65,66]. These scenarios are illustrated in figure 4.24.

The low-laser-fluence regime describes a situation where the incident laser fluence is sufficient to induce melting of the Si film, but it is low enough that a continuous layer of Si remains at the maximum extent of melting. For this reason, this regime is also referred to as the *partial melting* regime. For irradiation of a-Si films, this regime is characterized by a combination of explosive crystallization and vertical solidification. Explosive crystallization can be triggered at the onset or near the end of melting, respectively, depending upon the presence or absence of microcrystallites in the Si film [67].

The high-laser-fluence regime corresponds to the situation encountered when the laser fluence is sufficiently high to completely melt the Si film. For

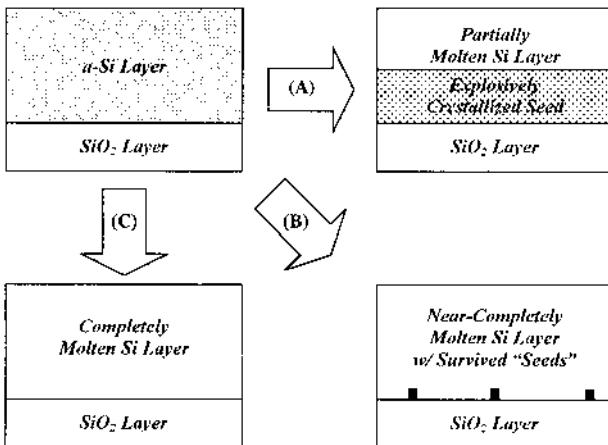


FIGURE 4.24 Illustration of transformation scenarios during the ELC process. Scenarios (A), (B), and (C) correspond to partial melting, near-complete melting, and complete melting of the initial Si film (see text for details).

this reason, this regime is also referred to as the *complete melting* regime. In most cases of laser annealing of thin Si films, the film is formed on top of an amorphous SiO_2 or SiN_x layer, which means that epitaxial regrowth from the surface of the substrate is impossible. Therefore, the situation necessitates nucleation of solids within the liquid for the formation of a stable solid–liquid interface that can be used to “accommodate” the liquid-to-solid conversion. The nucleation in this case takes place as a result of the unusually deep undercooling that occurs in the molten Si film. The term *undercooling* refers to the degree of deviation of the temperature of the molten Si from its melting point. In that sense, deep undercooling implies a liquid existing at a temperature substantially lower than its melting point. In the case of thin Si films irradiated by laser the deep undercooling [68] is the consequence of (1) the extremely rapid cooling of liquid Si (l-Si), (2) the relatively ineffective role of the 1-Si/underlayer (i.e., SiO_2 or SiN_x) interface, as far as catalyzing heterogeneous nucleation of crystal Si [69], (3) the statistical nature (both spatial and temporal) of nucleation, and (4) the small volumes associated with thin films. As a result of the copious nucleation that occurs within the undercooled molten Si, the grain sizes obtained in this regime are very small (typically on the order of tens of nanometers in diameter).

In addition to these two regimes, a third regime has been found to exist within a very narrow experimental window in between the two main regimes. Despite the small extent of this third region, it is nonetheless one with great

technological significance, because the poly-Si films formed within this region feature large-grained polycrystalline microstructures (i.e., grain sizes of several multiples of the film thickness). The transformation scenario associated with this regime has been modeled by Im et al. in terms of near-complete melting of Si films [65,70]. In particular it was argued that at the maximum extent of melting, the unmelted portion of the underlying Si film no longer forms a continuous layer, but instead consists of discrete islands of solid material separated by small regions that have undergone complete melting. For this reason, this regime is referred to as the *near-complete melting* regime. The practical implication of this model is that the unmelted islands provide solidification “seeds” from which lateral growth can ensue, thus propagating the solid–liquid interface within the surrounding undercooled molten Si (for this reason this regime has also been called the *superlateral growth*, or SLG, regime). In the ideal case, the lateral growth fronts coalesce and form a continuous matrix of similarly sized grains. This, however, is very difficult to control in practice because the laser fluence leading to the SLG regime needs to be precisely controlled. Small variations in the laser fluence (e.g., due to pulse-to-pulse energy variations) lead to either partial melting or complete melting conditions, with grave implications to the poly-Si microstructure, as discussed before. Therefore, within the SLG regime, the high quality of the resulting poly-Si material is usually compromised by difficulties in achieving this quality uniformly, across the irradiated film. Figure 4.25 shows the average grain size and corresponding poly-Si TFT performance associated with each of these three laser-crystallization regimes.

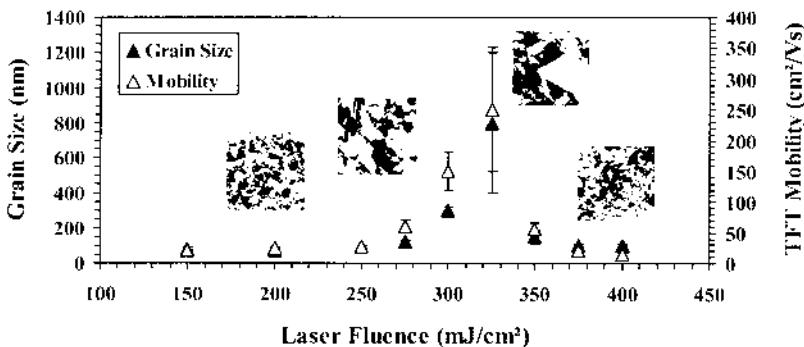


FIGURE 4.25 Grain size and corresponding poly-Si TFT mobility versus laser fluence for the conventional ELC process. The inset TEM photographs illustrate the poly-Si microstructure corresponding to (left to right) the surface melting, partial melting, near-complete melting, and complete melting regimes.

4.4.2.2 Conventional Eximer Laser Crystallization Method

In conventional laser crystallization, the substrate is scanned under the laser beam, which is typically homogenized to a “top-hat” profile. Other beam profiles have also been employed, in efforts to improve the uniformity of the resulting microstructure [71], but the top-hat profile is generally considered the industry standard. The aim of this process is to induce near-complete melting in the film and, by irradiating the same region multiple times, to improve the size and uniformity of the initially developed grains. This scenario has similarities to the conventional normal or secondary grain-growth process and has been previously discussed in detail [72]. In practice, this scenario can be achieved either by static irradiation of a region for multiple times (before moving to the next area) or, on-the-fly, by employing a sufficiently wide overlap between successive shots. The first approach is more suited to a large-area beam [73], whereas the second approach is commonly used with small-area, high-aspect-ratio beams [22]. Naturally, a limitation exists in the practical range of the number of shots (or the overlap distance) dictated in the low end by material quality considerations and in the high end by productivity (i.e., throughput) considerations. Figure 4.26 shows the variation of grain size with the number of shots on a given area.

One other drawback of multiple exposures is the increased probability of contaminant incorporation in the film. This necessitates the use of either vacuum

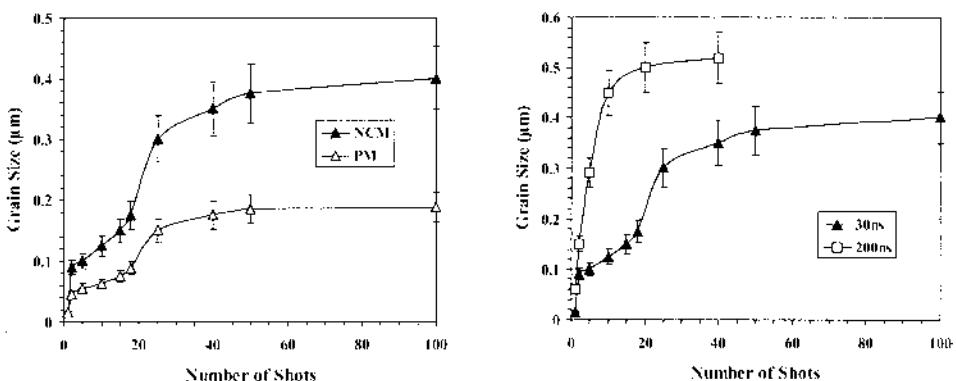


FIGURE 4.26 (left) Poly-Si grain size versus number of shots. NCM corresponds to irradiations at the near-complete melting regime. PM corresponds to irradiations at the partial melting regime. The number of shots (NS) relates to overlap (OL) by the simple relationship $OL = (NS - 1)/NS$. (right) Poly-Si grain size versus number of shots and laser pulse duration (all irradiations at the NCM regime).

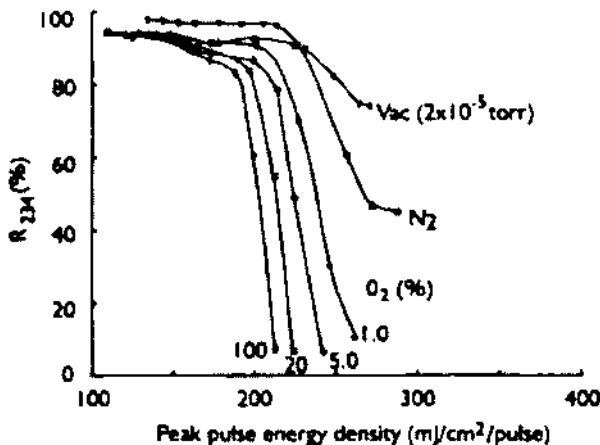


FIGURE 4.27 Effect of annealing ambient on poly-Si surface roughness at a pulse density of 20 pulses/mm. The surface roughness is assessed by the intensity of the normalized surface reflectance peak at 234 nm, with 100% reflectance corresponding to perfectly smooth surface. (Data from Ref. 74.)

or otherwise-controlled ambient to conduct the annealing process. Figure 4.27 shows the variation in laser-annealed poly-Si film surface roughness as a function of annealing ambient. As the oxygen content in the annealing ambient increases, stronger surface roughness develops [74,75]. Reduction and control of the poly-Si film surface roughness is necessary to match the requirements in device performance that dictate the use of increasingly thinner gate-insulator films.

The surface roughness in ELC poly-Si films is localized at the planes and points of congruence of grain boundaries. The mechanism for the formation of roughness is well understood and is attributed to the specific density difference between molten Si (2.53 gr/cm^3) and solid Si (2.30 gr/cm^3). In other words, as molten Si solidifies, it simultaneously expands. Solidification starts from neighboring “seed” areas, and the last region to solidify is the volume at the vicinity of the two colliding lateral fronts. As that happens, the generated solid Si (occupying more volume than liquid Si) can only expand upward (i.e., normal to the surface of the film), thus generating the ridge associated with the formation of a grain boundary at that location. In typical laser-annealing applications, the peak-to-valley surface roughness is equivalent to the thickness of the film. This means that for a 50-nm-thick film, a peak-to-valley surface roughness on the order of 50 nm should be expected. As mentioned previously, surface roughness can be additionally exaggerated by oxygen-rich ambient during annealing, presumably

due to additional stress relief initiated by the formation of surface suboxide complexes [75]. One solution to suppress surface roughness is the application of a multiple-irradiation scheme, in which one beam pass is used to crystallize the film at the optimum level of laser fluence, followed by a second (or more) pass(es) at a lower fluence aiming to “planarize” the surface by inducing only near-surface melting of the film. This method has been successful in producing ELC poly-Si films with low surface roughness [76,77] (Fig. 4.28b).

Development of the conventional ELC method has provided poly-Si material of higher quality than the conventional SPC method. This is attributed primarily to the melt-induced poly-Si growth. As a result of such growth, substantially fewer intragrain defects form within the grains of laser-annealed poly-Si films. This improvement seems to be more important than the improvement in the grain size itself, as evidenced by the trend in the TFT mobility of poly-Si films as a function of grain size and annealing method [78] (SPC or ELC) (see Fig. 4.29). However, the stable grain size of ELC poly-Si films is typically limited to 0.3–0.6 μm . Larger grain size is possible within the SLG window, but this regime is intrinsically unstable within the context of the conventional ELC process. One laser equipment attribute that improves the grain size within the stable regime is pulse duration. Longer pulse duration has been found to yield larger grain size (Fig. 4.26, right).

One disadvantage of the conventional ELC process relates to the difficulty in maintaining a proper balance between performance and process uniformity.

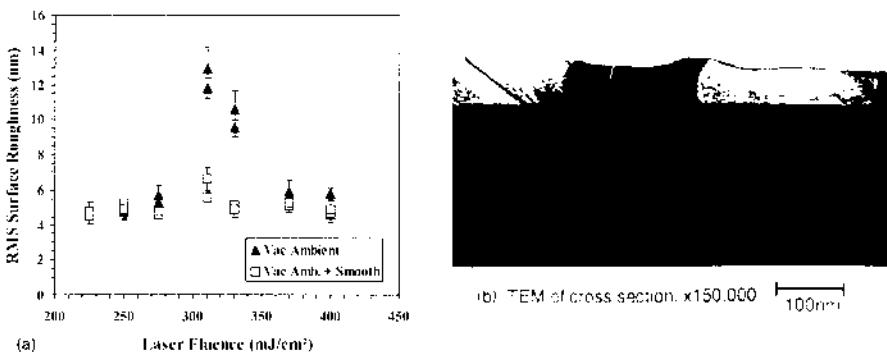


FIGURE 4.28 (a, left) Poly-Si film RMS surface roughness as a function of laser fluence in vacuum annealing ambient. Using a dual-irradiation scheme, with a 40% reduction in the laser fluence of the second pass, the surface roughness at the optimum grain size condition was decreased by more than a factor of 2. (b, right) Cross-sectional TEM of a poly-Si film irradiated with a dual scheme, showing large grain size and low surface roughness. (From Ref. 76.)

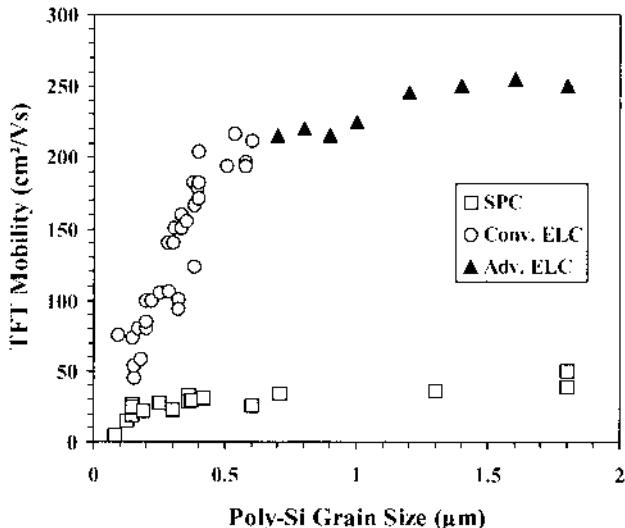


FIGURE 4.29 TFT mobility as a function of poly-Si grain size. For a given grain size, the ELC process enables superior TFT performance due to the significant reduction of defects within the poly-Si grains.

This comes about because the pulse-to-pulse repeatability (which is an equipment-related parameter) defines the process window where the laser fluence needs to be centered to avoid crossing over to other ELC regimes during annealing. This fluence window, in turn, defines the range of performance that can be expected from TFTs fabricated on such a poly-Si microstructure. In manufacturing operations, this kind of compromise typically translates to only mediocre TFT performance (e.g., $100 \text{ cm}^2/\text{V}\cdot\text{s}$) at the benefit of a wider process window. A second disadvantage of the conventional ELC process is the relative disparity between the average grain size and the TFT channel size (length). This means that unless the TFT channel becomes extremely small (i.e., $<0.5 \mu\text{m}$), it will be impossible to imagine the TFT channel consisting of a single grain. This problem is further exacerbated by the lack of tight grain size distribution in conventional ELC and the inability to precisely control the location of grain boundaries with respect to the TFT channel. Therefore, the application of the conventional ELC process is limited due to these issues and cannot be expected to provide a technology path for future devices. However, this is not to say that laser crystallization is not capable of resolving these issues and improving device performance. By rethinking the physics of laser crystallization and cleverly exploiting previous results, a number of elegant solutions have indeed been identified and developed over the

past few years, giving rise to a new generation of laser annealing crystallization technologies that will be discussed next.

4.4.2.3 Advanced Excimer Laser Crystallization Concepts

The key point that drives the development of advanced ELC concepts is the manipulation of the intrinsically unstable SLG phenomenon in a manner that permits flexible microstructural design of the resulting material while eliminating all the caveats associated with conventional ELC processing in the SLG regime [79]. In that sense, all such concepts can be classified under the general term *controlled SLG* (C-SLG) [80]. Figure 4.30 shows a classification tree for such advanced schemes.

The essence of the superlateral growth concept is the lowering of the free energy of a system, comprising a solid in contact with a metastable undercooled liquid, by the growth of the solid into the undercooled liquid region. By exploiting this concept, artificial situations can be devised that allow precisely controlled regions of the silicon film to be melted and left in contact with solid regions. These solid regions can then act as seeds for the lateral growth of material into the undercooled liquid. The most obvious advantage of the controlled SLG process is its relative insensitivity to variations in the laser fluence. In the case of C-SLG, the requirement is that the laser fluence is at least sufficient to completely melt the irradiated region, which is in contact with the solid region that will serve as the seed for lateral growth. Note that higher fluence than this minimum requirement will work equally well. This implies a wider process window than that of the naturally occurring SLG regime, where the objective is to leave a sufficient number of isolated solid islands by precisely controlling the fluence level within

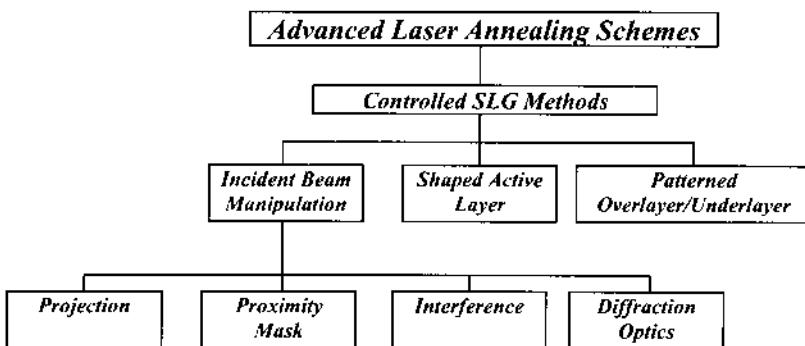


FIGURE 4.30 Classification of advanced laser annealing schemes.

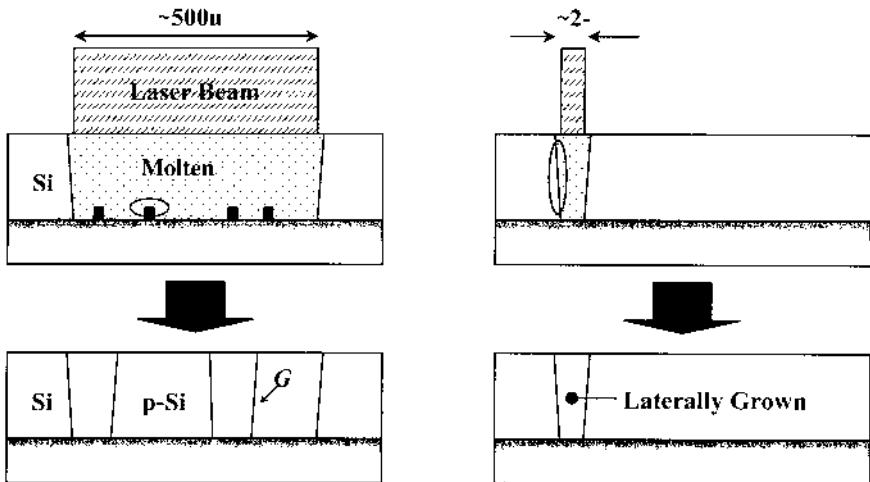


FIGURE 4.31 Comparison of SLG and C-SLG modes of growth. In SLG (left panels) growth initiates from seeds that survived the melting process at the Si/SiO_x interface. In C-SLG (right panels) the poly-Si microstructure forms by lateral epitaxy from seeds generated at the liquid/solid interface. Notice the difference between SLG and C-SLG in the width of the molten zone.

the irradiated area (see Fig. 4.31). To draw on a metaphor, this difference can be construed as similar to a sculptor trying to shape his creation with a chisel (C-SLG) versus a sledgehammer (SLG).

By controlling the shape and physical dimensions of the regions that undergo complete melting through various optical, photolithographic, and/or other means, the resulting microstructure can be tailored to yield controllable, predictable, and uniform grain size and structure. This point is the direct consequence of the relationship between the lateral growth distance (extending in the direction of lateral growth) and the width of the irradiated (completely molten) region. The growth distance of the lateral crystals is limited either by the onset of nucleation in the molten zone or by collision with the lateral grown crystals from the opposite side of the molten region. Therefore, by tailoring the width of the molten region that is formed during the laser irradiation to the lateral growth distance, the copious nucleation can be avoided. In this manner, a very uniform and large-grained microstructure can be generated over large areas.

Several techniques can be identified to carry out the task of preselecting the regions to undergo complete melting. These include varying the thickness or contour of the Si film, coating the Si film with a patterned overlayer that can act

as an antireflective, reflective, beam-absorbing, or heat-sink medium [81–83], and shaping the intensity profile of the incident laser beam via proximity or projection irradiation involving a shadow mask by inducing interference on the film surface or by using diffractive phase elements [84,85].

The concept of projection irradiation as the method of choice for defining the laterally grown domains has been extensively researched by Im's group at Columbia University [84]. Using the so-called sequential lateral solidification (SLS) scheme, laterally grown crystals can be elongated to any arbitrary length. This is achieved by translating either the sample or the incident beam with respect to each other. By moving at a distance less than the SLG distance, the Si film can be remelted in such a way that the molten region is left in contact with a portion of the laterally grown grains from the previous melting and solidification step (see Fig. 4.32). It is interesting to note that the relationship between the translation distance and the SLG distance opens up interesting variations as far as the details of the resulting microstructure [86]. It is then clear that the exploita-

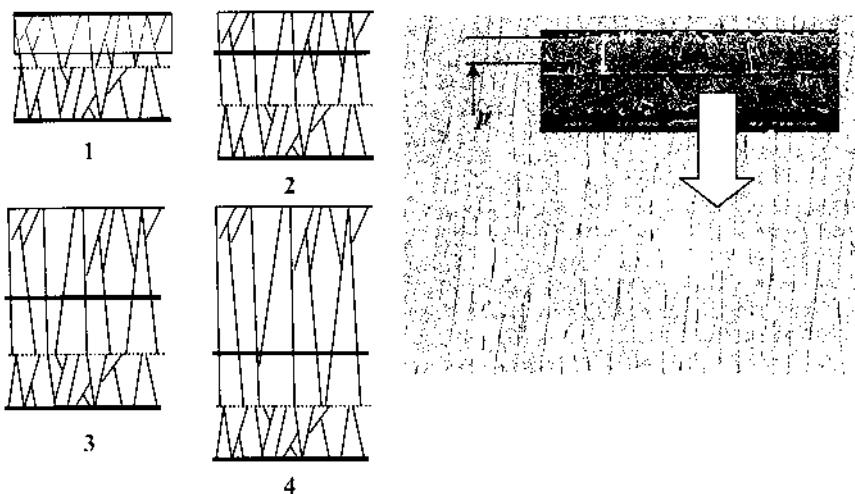


FIGURE 4.32 Illustration of the sequential lateral solidification method. The sequence on the left side illustrates the propagation of the lateral growth upon 4 successive irradiations with a pitch p shown by the shaded region in the upper part of vignette 1. The SEM image on the right side shows the actual microstructure after multiple translations of the single *beamlet* shown in the inset. The white arrow indicates the direction of the translation. For this type of structure, the pitch of translation p must be smaller than the SLG distance w .

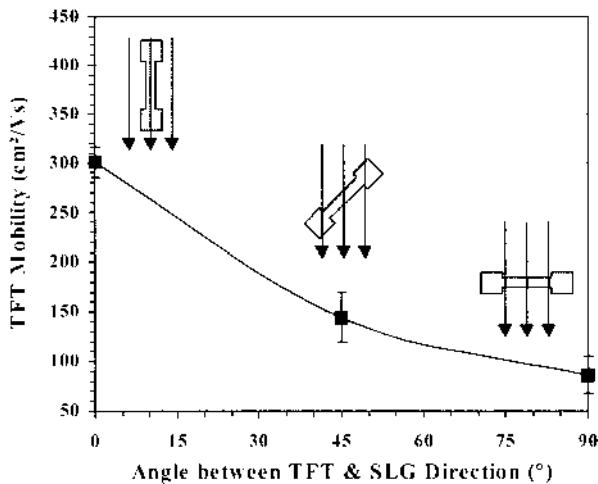


FIGURE 4.33 Poly-Si TFT mobility as a function of the angle between the direction of the TFT channel and the direction of lateral growth (SLG direction).

tion of the C-SLG phenomenon is the right path for creating high-quality, extremely uniform poly-Si microstructures. One disadvantage that is currently noted for directional solidification schemes is the existence of performance directionality. In other words, TFT characteristics demonstrate a strong dependence on the degree of misorientation between the direction of carrier conduction in the active layer and the lateral growth direction in the film [87] (see Fig. 4.33). Practical solutions to such problems are currently under development. Despite the occurrence of setbacks, however, one has to acknowledge that the application of advanced, laser-based crystallization processes in TFT fabrication makes possible the improvement in both performance and uniformity of poly-Si TFTs to levels not possible before (see Table 4.4 [88]).

4.4.3 Trends in Crystallization Technology

Figure 4.34 summarizes the typical performance data for the different crystallization technologies covered in this report. Historically, solid-phase crystallization was the first method to produce poly-Si films for TFT applications. Since that time, around the early 1980s, many other techniques have emerged that aim to improve the film quality and TFT characteristics to enable new, more demanding display applications.

Metal-induced crystallization (MIC) has provided a high-end SPC technology that has been shown capable of producing poly-Si TFTs with very high

TABLE 4.4 TFT Performance Characteristics vs. Type of Laser Annealing Process

Process	Style	Type	TFT Mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)			
			Channel //	Channel \perp	Unif.	Ref.
Std. ELA	Projection	Directional $(p < w)$	150	150	30%	
			370	150	10%	
		Periodical $(p > w)$	340	140	7.5%	87
			360	160	—	88
Adv. ELA	Projection	Periodical $(p > w)$	240	80	5%	
			220	90	3%	87

Poly-Si film thickness $\sim 1000 \text{ \AA}$

performance and uniformity, albeit with the need to combine SPC and conventional ELC methods to achieve that performance level. The main caveat of SPC technology, which is intragrain defects, seems impossible to effectively tackle, given the temperature constraints of common display-glass substrates. Therefore, the next evolution in crystallization technology points to laser technology, in some format, as the logical choice. It is fair to state that ELC technology has significantly improved and matured, on both process and equipment technology, over the past 20 years. However, it is only within the last decade that the accumulation of experimental data and related observations has lead to theoretical under-

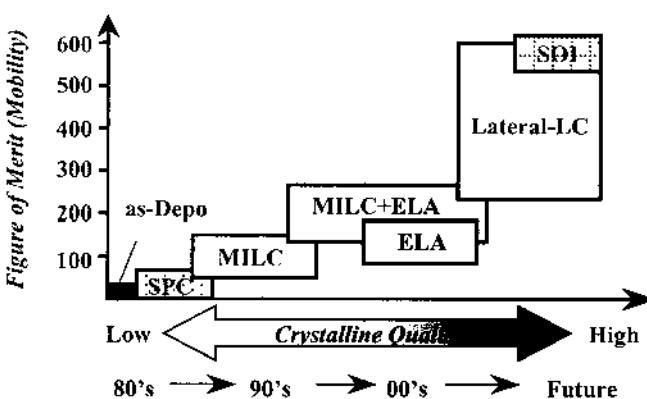


FIGURE 4.34 TFT mobility range versus poly-Si crystallization technique.

standing that has made possible novel crystallization scenarios. As a result, advanced laser annealing schemes, exploiting the SLG phenomenon, are already producing very high-quality, uniform poly-Si microstructures and are expected to produce material capable of performance rivaling that of single-crystal Si in the near future. It should be noted that, in addition to the sought high crystal Si quality, future processing schemes also need to consider the alignment of such crystal “islands” with the device active region. This need arises primarily from the realization that single-crystal Si quality may not be possible and/or necessary to achieve across the whole surface area of a display substrate. To that end, several efforts to develop “location control” crystallization schemes have already been shown, and others are currently under development [89,90].

4.5 GATE INSULATOR FORMATION

Silicon dioxide is the gate insulator of choice for poly-Si TFTs. Due to the temperature constraints in poly-Si TFT technology, the immense experience of the IC industry with thermally grown SiO_2 films cannot be applied directly to TFT LCDs on glass. The formation of a high-quality, silicon dioxide gate-insulator film poses a formidable challenge for poly-Si TFT technology. To some extent, it can be said that the effort to improve the dielectric film quality is now surpassing in strength and breadth the endeavor of improving the poly-Si microstructure, which until recently ranked #1. The reason for this challenge is that the formation of gate insulator (1) is intimately related to the preceding processing steps (most importantly the poly-Si formation method that controls surface roughness), (2) is constrained by temperature (thus tends to generate more defective material), (3) critically affects the interface between the poly-Si and the gate insulator (which also critically affects TFT parameters such as the threshold voltage), and (4) requires a deposition method that yields high productivity (i.e., high throughput), low cost, and scalability over very large substrate areas. As is usually the case, analysis of the requirements points out that some sort of compromises are necessary, for no single method exists (so far) that can simultaneously deliver all of the desired features without violating one or more of the constraints.

Typically, a gate-dielectric film (such as SiO_2) has an associated density of trapped charge [91]. Such charges (or simply “traps”) are generated in the dielectric film as a result of the deposition process and the manner at which the dielectric film forms an interface with the underlying poly-Si layer. These traps can be classified as “bulk” (N_b) or “interface” (D_{it}) traps. Bulk traps include mobile-ion charges (i.e., due to ionized alkali-atom impurities) and fixed charges (i.e., due to structural imperfections throughout the bulk of the dielectric). In good-quality thermal oxides, the bulk oxide traps are in the order of $5 \times 10^{16} \text{ cm}^{-3}$. Interface traps refer to charges due to electronic states at the Si/gate-insulator interface. This type of charge is less understood than any other oxide

charges. They are believed to be due to incomplete Si bonds and adsorption of foreign material at the silicon surface. Thermally grown SiO_2 has a unique property as far as terminating incomplete Si bonds at the Si/SiO_2 interface that otherwise would have generated interface traps. This is the main reason why it is the preferred gate insulator for Si (and poly-Si) technology. Typical values for D_{it} range from 5×10^9 to 10^{11} cm^{-2} (for thermally grown oxide), depending upon the Si orientation and the processing history [92].

Many studies have been performed to clarify the relationship between the trap density either in the poly-Si film or in the gate insulator and the poly-Si TFT characteristics [93–96]. It is well understood that the trapped charge affects primarily the TFT characteristics in the subthreshold regime (i.e., between the onset of depletion and the onset of strong inversion). Therefore, threshold voltage and subthreshold slope will be strongly affected by the trapped charge. Equations (4.2)–(4.6) describe mathematically the relationship between trap density and TFT parameters:

$$S = \frac{kT}{q} \cdot \ln 10 \cdot \left(1 + \frac{C_t}{C_{\text{ox}}} \right) \quad (4.2)$$

$$V_{\text{th}} = \phi_{ms} - \frac{Q_{\text{eff}}}{C_{\text{ox}}} + \psi_{s,\max} + \frac{Q_b}{C_{\text{ox}}} \quad (4.3)$$

with

$$C_{\text{ox}} = \frac{\epsilon_{\text{ox}} \cdot \epsilon_0}{t_{\text{ox}}} \quad (4.4)$$

$$C_t = qN_{b,\text{Si}} \cdot t_{\text{Si}} + qD_{it} \quad (4.5)$$

$$Q_{\text{eff}} = q \cdot \left(\int_{E_i}^{E_c} D_{it} dE + qN_b \cdot t_{\text{ox}} \right) - q \cdot t_{\text{Si}} \cdot \int_{E_i}^{E_c} N_{b,\text{Si}} dE \quad (4.6)$$

$$= \cdot N_{ox}^* - q \cdot t_{\text{Si}} \cdot N_{b,\text{Si}}^*$$

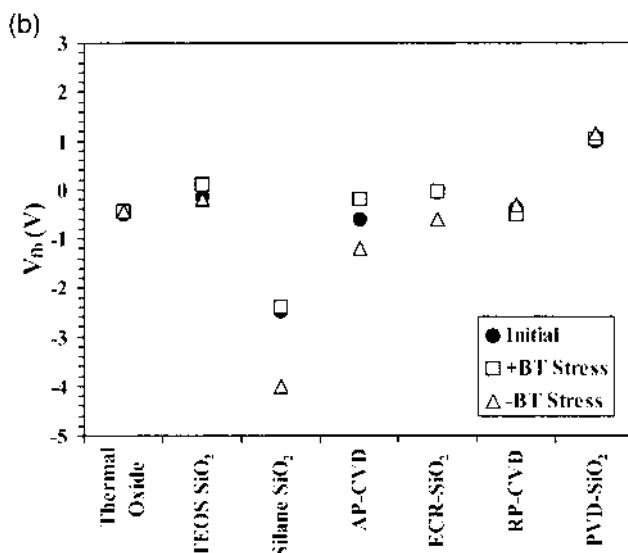
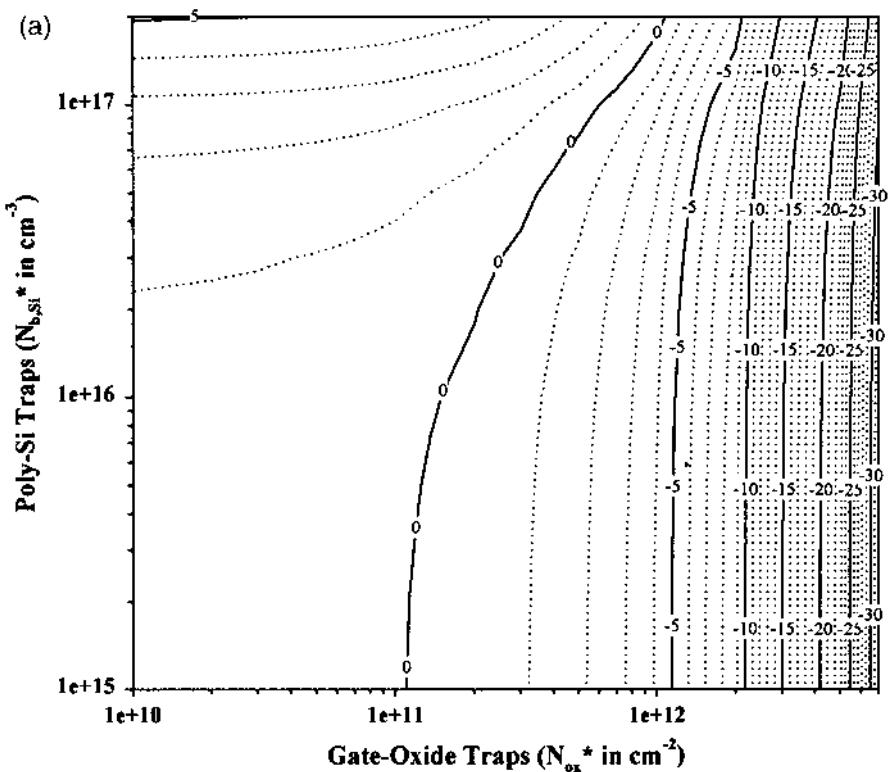
where V_{th} is the TFT threshold voltage (V) at the onset of strong inversion (at this condition, the surface potential $\psi_{s,\max}$ is approximately 0.7 V), S is the TFT subthreshold swing (dec/V), ϕ_{ms} is the metal–semiconductor work function difference (V), C_t is the trap-state capacitance per unit area (F/cm^2), ϵ_{ox} is the dielectric constant of gate SiO_2 , t_{Si} is the poly-Si film thickness (\AA), V_{fb} is the flat-band voltage (V), $N_{b,\text{Si}}$ is the trap density in the poly-Si layer ($\text{cm}^{-3} \text{ eV}^{-1}$), N_b is the density of bulk traps in the gate dielectric film (cm^{-3}), and D_{it} is the interface trap density at the poly-Si/gate-insulator interface ($\text{cm}^{-2} \text{ eV}^{-1}$), Q_b is the charge associated with ionized acceptor atoms within the depletion region of the poly-Si film and can be manipulated by the channel doping process. Q_{eff} is

an “effective” trapped charge (C/cm^2), combining traps in both the poly-Si film ($N_{b,Si}^*$ in cm^{-3}) and the gate-dielectric film (N_{ox}^* in cm^{-2}).

As can be seen from the analysis, the threshold voltage of poly-Si TFT devices can be manipulated in several ways and can become increasingly positive or negative depending upon the relative magnitudes of the various terms in Eq. (4.2). Generally, positive traps in the gate insulator tend to generate negative shifts, while increased trap density in the poly-Si layer itself (i.e., due to micro-structural deficiencies) tends to generate positive shifts. [Figure 4.35a](#) shows iso- V_{th} contours as a function of the trap density in the gate insulator and in the poly-Si film, calculated from the previous model, assuming 1000-Å-thick SiO_2 layer, 500-Å-thick (fully depleted) poly-Si layer, no substrate doping, and ϕ_{MS} of -0.2 V. The computed curves indicate that to reduce V_{th} below ± 1 V, the gate-oxide trap density must be reduced below $\sim 3 \text{eV} 1 \text{ cm}^{-2}$. In other words, the quality of the gate-insulator (GI) film must approach that of a thermally grown oxide.

Stability of characteristics is another sought after attribute for the gate-insulator layer. A measure of the stability is the deviation of the flat-band voltage upon subjecting the dielectric layer to a standard bias-temperature stress (BTS) sequence. [Figure 4.35b](#) summarizes the flat-band voltage values measured before and after positive and negative BTS as a function of GI deposition technology [97]. These data were obtained from MOS capacitors fabricated on Si substrates to alleviate interface-induced effects. A significant variation in the flat-band voltage response is observed as a consequence of the different trapping characteristics of each GI deposition method. It is expected that deposition methods that promote efficient decomposition of the oxygen-atom-carrying precursor can lead to better-quality SiO_2 films. The quality of the SiO_2 layer can deteriorate by plasma damage, due to intense ion bombardment during deposition. One way to prevent this is by separating the plasma generation from the reaction zone (e.g., via the remote plasma CVD method) [98]. Another method that is under development suggests the utilization of high-density plasma as a means of separately controlling the ion energy and the ion bombardment rate during deposition.

A second mechanism that degrades the quality of the dielectric film relates to the incorporation of atoms or chemical groups that generate trap states in the dielectric film. Typically, SiO_2 films are formed by the chemical decomposition of gaseous precursors that contain H and O atoms (e.g., TEOS, $\text{SiH}_2 + \text{N}_2\text{O}$, or $\text{SiH}_4 + \text{O}_2$ chemical systems). Therefore, oxides, which are formed under such conditions, tend to contain significant amounts of hydroxyl (—OH) groups, either in the form of Si—OH bonds or in the form of absorbed water. Such groups have been shown to adversely affect the quality of the GI film, to yield a high density of trapped oxide charges, and to be responsible for shifts in TFT threshold voltage [99,100]. Previous studies have shown that the quality and effectiveness of the dielectric film are significantly enhanced when it is deposited at conditions that favor reduction of such bonding configurations [101]. For example, [Figure 4.36](#)



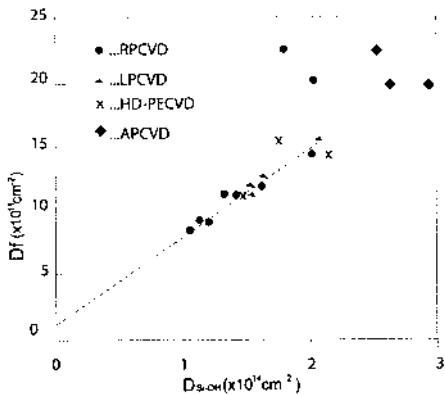


FIGURE 4.36 Relationship between fixed charge density and Si–OH bond density in the gate-insulator film. Data for different deposition methods are presented. The Si–OH bond density was measured by TDS. The trap density was assessed by from high-frequency C–V characteristics of MOS capacitors. (Data from Ref. 101.)

shows the correlation between fixed trapped density in the GI film and the density of Si–OH bonds (measured by thermal desorption spectroscopy). The conclusion of such studies is that care must be taken to eliminate the formation of hydroxylic groups in the gate insulator. This includes both water absorption (in other words, reduce the porosity of the deposited film) and contributions from the deposition chemistry. To that extent, GI deposition methods that reduce or completely eliminate the formation rate of Si–OH groups are preferable. Such methods include high-density plasma CVD (i.e., ECR, ICP, etc.), remote plasma CVD, and sputtering.



FIGURE 4.35 (a) Computed poly-Si TFT V_{th} as a function of trap density in poly-Si and gate-oxide layers. The threshold voltage was computed from Eq. (42) assuming 1000-Å-thick SiO_2 layer, 500-Å-thick poly-Si layer, no substrate doping, and a work function value of -0.2 V (this work). (b) Flat-band voltage as a function of GI deposition technology. Data are shown before and after bias-temperature stress (BTS) (positive or negative). The BTS conditions were 2.5 MV/cm , 150°C . “TEOS” stands for tetra-*ortho*-silicate, “Silane” refers to $\text{SiH}_4 + \text{N}_2\text{O}$ plasma chemistry, “AP-CVD” stands for atmospheric CVD, “ECR” stands for electron cyclotron plasma, “RP-CVD” stands for remote plasma CVD, and “PVD” stands for physical vapor deposition.

The reduction of the gate-insulator film thickness is another effective way to reduce the density of bulk traps. Previous studies have indicated that such reduction is analogous to a decrease in the threshold voltage shift, under DC bias, as a result of the reduction in the trapping volume within the dielectric film [102]. In addition, thickness reduction automatically improves process productivity, due to the associated decrease in deposition time. However, the minimum thickness of the gate-insulator film is intimately related to the surface roughness of the underlying poly-Si layer as well as to the capability of the deposition process to maintain film quality at reduced thickness. In the case of laser crystallization, the peak-to-valley surface roughness is of the order of the film thickness. Therefore, a gate-insulator thickness of 1000–1100 Å is required to cover ELC poly-Si films of ~500 Å to provide an appropriate margin for the crystallization-induced surface roughness. Clearly, reduction of the GI layer thickness requires improvements in the crystallization process. In addition, the capability of the gate-insulator-forming method needs to be reassessed as the GI layer thickness decreases.

The goals of a thin GI layer with excellent bulk quality and interface characteristics are difficult to meet with a single GI layer. The reason is the conflicting requirements of high deposition rate (i.e., high productivity), high film quality, and low process temperature. Therefore, one meaningful strategy is to divide the total GI film into two parts. The first layer is optimized for interface quality (and can thus be formed at a low deposition rate to yield good atomic arrangement at the interface), and the second layer is optimized for “bulk” properties (and can

TABLE 4.5 Recommended Targets for Gate-Insulator SiO₂ Films

Parameter	Value
<i>Electrical properties</i>	
<i>I</i> _{icak} at 10 V	<2 × 10 ⁻⁶ A/cm ²
Breakdown field	>8 MV/cm
Interface traps (<i>D_{it}</i>) at midgap	<5e10 cm ⁻² eV ⁻¹
Fixed traps (<i>N_b</i>)	<5e11 cm ⁻²
Absolute flat-band voltage <i>V_{fb}</i>	<1 V
<i>V_{fb}</i> shift after BTS	<0.2 V
<i>Physical properties</i>	
Deposition Rate	>17 Å/s
Refractive <i>n</i>	1.46 ± 0.02
Refractive <i>k</i>	<0.000
Etch rate in 10:1 BOE	<15 Å/s
FTIR @ 3450/cm (water)	Noise level
FTIR @ 3650/cm (SiOH)	Noise level

be formed at an appropriate deposition rate level to meet productivity requirements). Such “dual” dielectric layer schemes have already been tried in many configurations, depending upon the technology choice for the first and second layers. For interface control, techniques such as direct plasma oxidation [103], photochemical CVD [86], high-density plasma CVD [104], photo-oxidation [105], and others are being assessed. For bulk GI layer, TEOS-SiO₂ is currently the most prominent technology, with many others (see Fig. 4.35) being in different stages of evaluation. Nonetheless, regardless of the final technology (or combination of technologies) for GI formation, a set of generally acceptable qualifiers must be met. Table 4.5 shows such a set of desired attributes. As new technologies for GI formation emerge, they should be assessed against such a matrix of requirements before incurring the expenditure of significant development time.

4.6 DOPING/ACTIVATION

Two key process technologies for poly-Si fabrication are doping and activation. These processes refer to fabrication steps aiming at the formation of critical junctions in poly-Si TFTs (see illustration in Fig. 4.37). For reasons that will become apparent, it is beneficial to consider these two processes together, because the junction characteristics are affected equally by both. Fabrication of CMOS TFTs necessitates the integration of both types of TFT polarities (*n*-type and *p*-type) on the same substrate. As a result, both donor type (*n*-type) and acceptor type (*p*-type) doping is needed. For this reason, the *in situ* doping technology that has been traditionally applied in a-Si TFTs cannot be used for the fabrication of CMOS poly-Si TFTs. Instead, adoption and additional development of standard impurity incorporation techniques is needed.

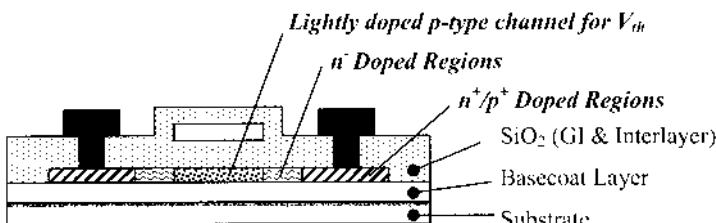


FIGURE 4.37 Cross section of a typical *n*-channel poly-Si TFT, showing the various regions that require some form of doping and activation process. Typically, light *p*-type doping (for V_{th} control) is used in the channel of poly-Si TFTs. Light *n*-type doping is used in *n*-channel TFTs for drain-field engineering and relief. Heavier *n*-/*p*-type doping is used for S/D formation in *n*-*p*-channel poly-Si TFTs.

TABLE 4.6 Summary of Doping and Activation Technologies

Dopant source	Doping species	Doping method	Activation	Application
Ion beam (mass separated)	P+, As+ B+, BF ₂ +	Ion implantation	FA, RTA (LA) FA, RTA, LA	LSIs TFTs
Ion beam (non mass separated)	P+, B+, H+	Ion doping	FA, RTA, LA (FA, RTA)	TFTs (LSIs)
Gas phase	POCl ₃	Deposition	FA	Power devices, ICs
	PH ₃	Plasma doping	FA, LA, RTA	TFTs (LSIs)
	B ₂ H ₆	Laser doping	LA	TFTs
Solid		Deposition & solid diffusion	FA	Power devices, ICs

FA = furnace annealing; RTA = rapid thermal annealing; LA = laser annealing.

Source: Ref. 76.

Table 4.6 summarizes the doping and activation techniques that have been commonly applied in semiconductor device fabrication. From the point of view of poly-Si TFT fabrication on glass substrates, there are a few specific requirements that contrast poly-Si TFT doping techniques to the traditional VLSI doping technology (i.e., ion implantation).

1. The low thermal conductivity of the substrate necessitates the use of “milder” doping conditions to alleviate heat damage to the photoresist.
2. A wide process window (in doping energy) is needed to facilitate the doping of thin Si films (i.e. <1000 Å) with or without a screen cap layer.
3. A relatively simple apparatus (low cost) capable of handling large substrates at a high throughput rate (i.e., 1 substrate/min) is required.
4. The doping process needs to be compatible with a low-thermal-budget activation process (suitable with glass substrates). Unlike VLSI, where high-temperature treatment can be used freely to restore the crystallinity in doped regions and activate the impurity atoms, in poly-Si TFTs the fabrication temperature is typically restricted to below ~650°C. This requirement is becoming even more severe in the case of plastic substrates (i.e., <200°C).

To satisfy such requirements, different doping and activation methods have been developed, as shown in [table 4.6](#). Among these we recognize methods where the ion energy may (i.e., ion doping) or may not (i.e., plasma doping, gas-phase induced laser doping) be actively controlled. In the former case, ions are generated by a Kaufman-type or non-Kaufman-type (e.g., RF, ECR) source and accelerated toward the substrate via an acceleration grid. In contrast to ion implantation, this is a non-mass-separation doping method, which, however, is capable of high-throughput, large-area doping when equipped with a Kaufman-type (bucket-type) ion source (Fig. 4.38) [106].

In the latter case, non-mass-separated ions (generated by a DC or RF plasma discharge) are used as the dopant source. These ions are driven and activated, typically by laser irradiation. In gas-phase Induced Laser Doping (GILD) [107] process, doping is achieved from a gaseous source that deposits the desired type of impurity on the surface of the poly-Si film. Deposition and activation are carried out simultaneously by exposure to laser irradiation. Both of these methods have a limited impurity penetration range and are, thus, compatible only with bare-doping schemes. The GILD process has been successfully used for poly-Si TFT doping on plastic substrates. Overall, ion doping is accepted as a more “mainstream” doping technology for poly-Si TFTs on glass, whereas GILD is a

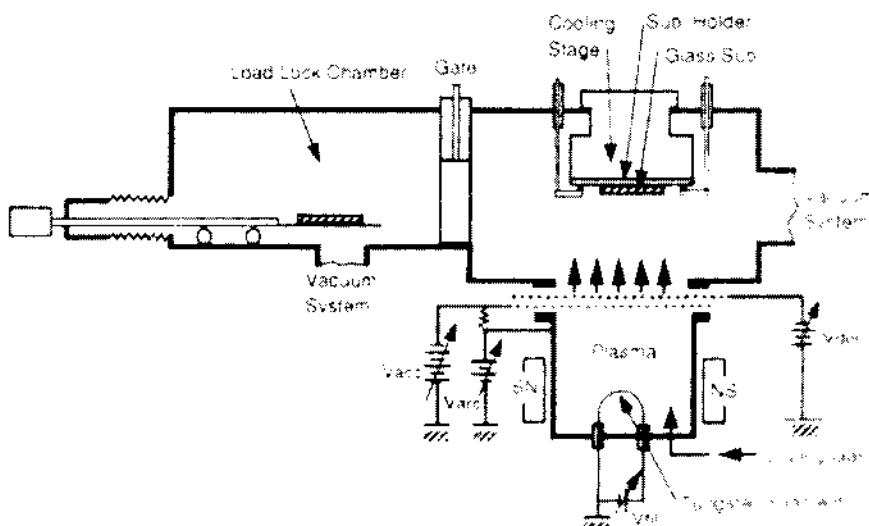


FIGURE 4.38 Illustration of a bucket-type ion-doping apparatus.
(From Ref. 76.)

technology that has found a niche application in the relatively young field of poly-Si TFTs on plastics.

As mentioned earlier, activation is equally important to doping as far as affecting junction characteristics (i.e., dopant profile and sheet resistance). To achieve good junction characteristics, low sheet resistance is required (see Table 4.7). In addition, the sheet-R specifications need to be achieved at a thermal budget compatible with glass substrates. Table 4.7 shows typical expansion and warpage specifications for glass substrates. As poly-Si technology is pushed to finer transistor geometry, such specifications are bound to become tighter.

Traditionally, activation has been performed by furnace annealing, a natural extension of early VLSI technology to poly-Si TFTs. This choice, however, may not be the best from the point of view of activation efficiency and cost effectiveness. The choice of activation technology is a rather complicated process that needs to take into consideration process integration issues to meet a variety of criteria. The complexities in the choice of technology arise from preferences in TFT fabrication technology, such as bare doping versus through-oxide doping (see Fig. 4.40) and gate–metal material selection (i.e., high-conductivity, low-melting-point metal such as Al/Al-alloys versus higher-melting-point metal that has lower conductivity).

Taking the cue from VLSI, rapid thermal annealing (RTA) has been actively investigated for application in poly-Si TFT technology. Even though the initial aim of RTA was in the precursor crystallization area, it was soon realized that this technology could have an alternative, if not better, fit in the activation area. However, it was not until the advent of mass-production-worthy equipment that the technology was established as a serious contender in this field [108]. Current RTA equipment employs different thermal strategies that all aim to rapidly raise and subsequently maintain the temperature of the substrate at moderate temperatures (i.e., 675–850°C) for a very short period of time (i.e., 5–200s). Typically, the substrate is initially, gradually preheated to a “safe” temperature range (i.e., <650°C) before rapidly ramping up the temperature to the target zone to reduce

TABLE 4.7 Recommended Targets for Activation Process

Parameter	Target
Sheet-R for n^- region (for LDD or GOLDD architectures)	<100 kW/sq
Sheet-R for n^+ region	<1 kW/sq
Sheet-R for p^+ region	<1 kW/sq
Substrate warpage	< \pm 2 ppm
Substrate expansion	< \pm 20 mm

the thermal shock that it would otherwise experience. Similarly, the temperature of the substrate is brought down in a gradual manner to avoid shattering and to keep the substrate deformation and shrinkage within specifications. The temperature history of the substrate is usually dependent upon the equipment design and is to some extent adjustable. Table 4.8 shows selected attributes and performance data for large-area RTA equipment.

[Figure 4.39](#), shows the sheet resistance of ion-implanted, *n*-type poly-Si films as a function of the annealing temperature (in furnace for $T_{\text{anneal}} < 700^{\circ}\text{C}$ and by RTA for $T_{\text{anneal}} > 700^{\circ}\text{C}$). As shown, sheet resistance values below 3 k Ω/sq can be obtained at relatively low temperatures (i.e., $< 750^{\circ}\text{C}$) only by the bare-doping method (see [Fig. 4.40](#) for an illustration of bare doping versus the through-oxide doping scheme). This result is attributed primarily to the more extensive structural damage in the poly-Si film when doped through the oxide layer and, to a lesser extent, the retardation in the crystal reconstruction rate due

TABLE 4.8 Comparison Between Large-Area RTA Equipment

	Maker			
	A	B	C	D
Typical temperature profile				
Lamp configuration	IR lamps for preheating 2 xenon arc lamps for annealing	Resistive heating for preheating 4 halogen lamps for annealing	(no separate preheating) 3 near, IR lamps for annealing	Temp. is controlled only by IR lamps
Development stage	Mass production	Experimental tool	Preliminary stage	R & D use for PDP and IC packaging
Substrate size	Up to 600 × 720 mm ²	Up to 600 × 720 mm ²	N/A	Up to 700 × 900 mm ²
Throughput	~ 33 sub/hr	~20 sub/hr	N/A	Depends on temp. profile
<i>Sheet-R</i>				
Poly-Si film <i>n</i> + counter-doped <i>p</i> +	1000 ohms/sq 3000 ohms/sq	1000 ohms/sq N/A	1000 ohms/sq N/A	N/A

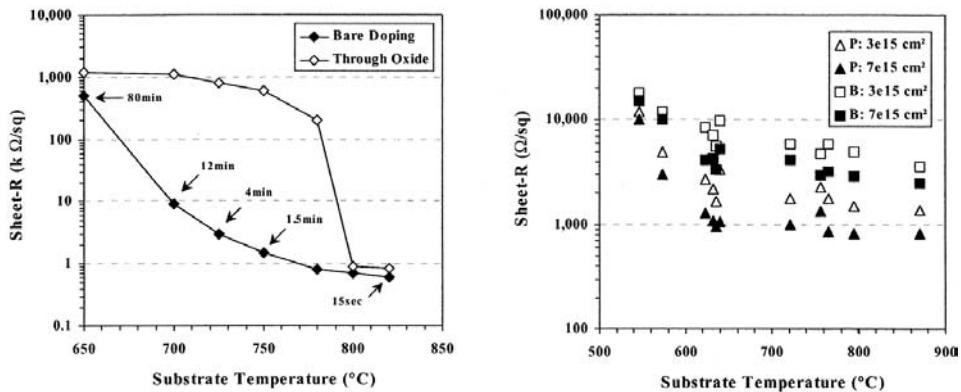


FIGURE 4.39 (left) Sheet resistance of ion-implanted samples as a function of substrate temperature and doping scheme. All samples were implanted with P^+ at $1e16$ at/cm (squared) and 90 keV (through oxide) or 20 keV (bare doping). The annealing time is also shown for selected conditions. (right) Sheet resistance of ion-doped samples as a function of substrate temperature, dopant type, and dose.

to incorporation of oxygen atoms in the implanted region. The ion-doping (I/D) method presents a more effective way to reduce the poly-Si sheet resistance. Sheet resistance values for ion doping are shown in Figure 4.39, right, as a function of substrate temperature and doping level (for through-oxide doping). The main reason for the easier activation of I/D samples at low annealing temperatures, seems to relate to the hydrogen-bearing species that are used in conjunction with the ion-doping method (see Table 4.6). It is speculated that the hydrogen that is codoped in the films catalyzes the reconstruction of the crystalline micro-

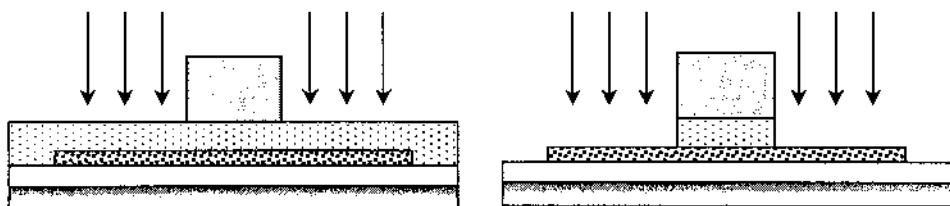


FIGURE 4.40 Illustration of through-oxide doping scheme (left) and bare-doping scheme (right).

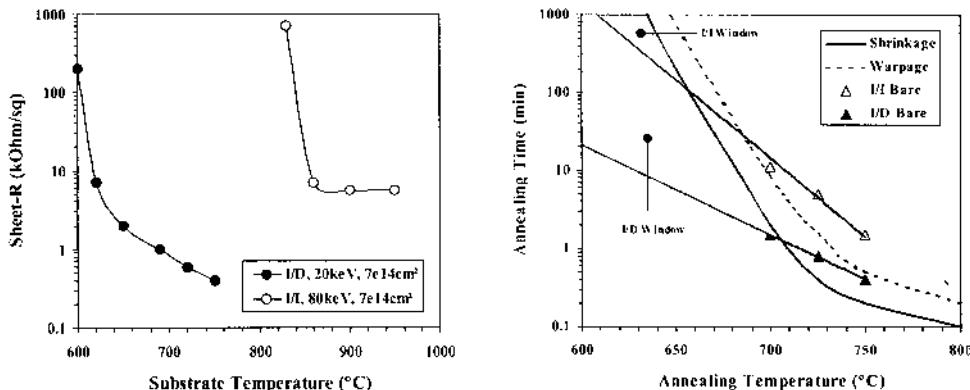


FIGURE 4.41 (left) Comparison of the ion-implantation (I/I) and ion-doping (I/D) methods. (right) Temperature–time annealing process domain showing glass shrinkage and warpage constraints.

structure, thus enabling faster activation at lower annealing temperatures [109]. Results from a number of studies (see, for example, Fig. 4.41, left) indicate that the ion-doping method can be combined with temperatures as low as 650°C to yield doped poly-Si films with sheet resistance values in the range of 1 kΩ/sq [108]. This is important because, as Figure 4.41, right, indicates, the process window in the temperature–time domain for typical display glass substrate is severely limited by shrinkage and warpage constraints.

Poly-Si TFT technology promises the fabrication of CMOS circuits. However, to achieve CMOS configuration, the number of lithography steps needs to increase by 2, due to the necessity of the coexistence of *n*-type and *p*-type TFT devices on the same substrate. This addition of lithography steps, however, can compromise the advantage of poly-Si TFTs due to increased fabrication costs. Therefore, different approaches have been considered to achieve one-mask CMOS process flow by employing a counter doping scheme in which all transistors are initially made *n*-type, followed by counter doping (using a *p*-type impurity) to define the *p*-type TFTs. One way to accomplish this flow is illustrated in Figure 4.42. In this case, ion doping is used for both *n*-type and *p*-type impurities, followed by laser processing to activate the dopant atoms [76].

Activation by laser annealing is historically placed before RTA technology. However, the cost and complexity associated with laser annealing have impeded its industry-wide acceptance (see Table 4.9 for a comparison of the activation process costs). The advantages of laser activation are high junction quality (i.e., low sheet resistance) and low-temperature processing compatible with practically

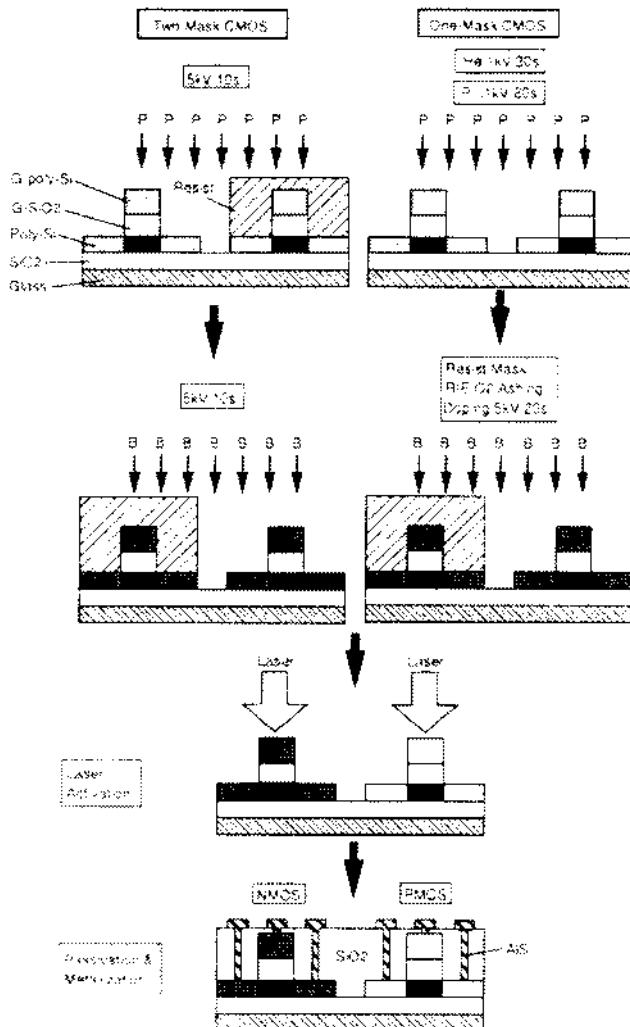


FIGURE 4.42 Comparison of two-mask and one-mask CMOS TFT fabrication flow.

TABLE 4.9 Comparison of Activation Process Costs (for a Nominal Glass Substrate Size of $600 \times 720 \text{ mm}^2$)

	Type			
	RTA Maker		Laser	Furnace
	A	B		
Equipment price	Cheap	Cheap	Expensive	Cheap
Throughput (No. of tools for same productivity)	Fast (1)	Mid (1)	Slow (2)	Slow (2)
Maintenance cost	1	1	20	1
Total cost for 5-year operation	1	N/A	8	2
<i>Sheet-R</i>				
$n^+ 1$	1000 Ω/sq	1000 Ω/sq	700 Ω/sq	1500 Ω/sq
$p^+ 1$	1000 Ω/sq		700 Ω/sq	1500 Ω/sq
Counter doped p^+	3000 Ω/sq		700 Ω/sq	8000 Ω/sq

any display substrate. Beyond the cost issue, other disadvantages of laser activation are the activation uniformity, the difficulty in controlling lateral diffusion of impurity atoms in the device channel, as well as the gate “shadowing effect.” Based on earlier reports, this phenomenon may prevent the thorough activation of the area at the channel edge (i.e., immediately under the gate) in self-aligned TFT architectures that is also amorphized during the doping process and requires crystalline reconstruction during activation [110].

Figure 4.43 shows sheet resistance data for ion-doped samples that were activated by an optimized laser annealing process [76]. As shown in Figure 4.43, left, the sheet resistance of laser-activated films varies little with the laser fluence (once the fluence exceeds the surface-melting threshold) and can easily reach very low levels (i.e., $<300 \Omega/\text{sq}$), depending on the dopant concentration in the film. As shown in Figure 4.43 right, the final sheet resistance also depends critically upon the microstructure of the predoped poly-Si film. This is especially true for n -type doping, for phosphorous atoms are much heavier than boron atoms (typically used for p -type doping) and tend to disrupt more effectively the Si crystal matrix upon doping. This is the reason the activation of n -type films shows significant dependence on both the initial microstructure and the applied laser fluence for activation.

Junction formation in poly-Si films is a very important step for the fabrication of reliable, high-performance TFTs. As the device geometry shrinks to

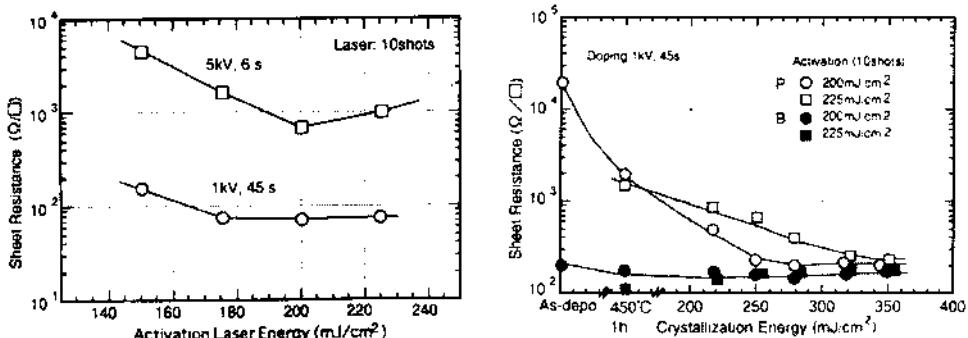


FIGURE 4.43 Typical sheet resistance values for laser-activated, ion-doped poly-Si films. (left) Variation of sheet resistance as a function of laser fluence and P-dose. (right) Variation of sheet resistance of *n*-type and *p*-type poly-Si films as a function of the predoping poly-Si microstructure and the activation conditions. (Data adapted from Ref. 76.)

smaller sizes, better control on the lateral extent of the junction and its uniformity will be required. Such control is difficult to achieve with traditional methods, such as furnace anneal. Additionally, laser-based activation may suffer from similar problems. Therefore, one important technology for activation will be rapid thermal annealing. For this technology to come to fruition, doping schemes that enable rapid activation at relatively low temperatures are also needed. Ion doping is one such method. Therefore, the combination of ion doping and the RTA process is expected to play an increasingly important role in the future of low-temperature poly-Si TFT technology on glass.

4.7 TYPICAL POLYSILICON TFT FABRICATION FLOW

As already discussed, a key advantage of poly-Si TFT technology is the ability to integrate the driving circuit with the pixel TFT array on the same substrate [111]. Although poly-Si material is the principal building block of the various TFTs found on such monolithically integrated displays, the exact architecture may vary depending upon the functionality of different TFTs on the panel. This need for differentiation stems from the different operational characteristics that need be satisfied from driver and pixel poly-Si TFTs. For example, a critical requirement for pixel TFTs is low leakage current. On the other hand, for driver TFTs, high reliability and high ON-current are needed. To meet such diverse requirements, poly-Si TFTs with drain relief features have been proposed

[112–114]. The following illustration shows a representative process flow for the simultaneous fabrication of pixel TFTs and CMOS driver TFTs on the same display substrate. This particular process flow yields self-aligned, top-metal-gate poly-Si TFTs with GOLDD (gate-overlapped lightly doped drain) configuration for *n*-channel TFTs. The GOLDD configuration is used to suppress leakage current in the case of pixel TFTs and to improve the reliability (i.e., the resistance to hot carrier degradation) of *n*-channel, driver TFTs. The process is outlined next and shown schematically in [Figure 4.44a](#) through [4.44t](#).

Typical Process Flow for Self-Aligned Top-Metal-Gate poly-Si TFTs

1. Sequential deposition of basecoat and a-Si film on the glass substrate
2. a-Si dehydrogenation (if necessary)
3. Low-temperature crystallization of a-Si film to obtain poly-Si film (Fig. 4.44a)
4. (Optional: Light channel doping for V_{th} adjustment)
5. **Mask #1:** Poly-Si island definition
6. Deposition of gate dielectric layer (Fig. 4.44b)
7. **Mask #2:** Doping mask (for lightly doped drain regions) (Fig. 4.44c)
8. Gate metal deposition
9. **Mask #3:** Gate definition
10. **Mask #4:** n^+ source/drain doping
11. **Mask #5:** p^+ source/drain doping
12. S/D activation (Fig. 4.44d)
13. Deposition of interlayer dielectric film
14. **Mask #6:** S/D contact hole definition
15. Source metal deposition
16. **Mask #7:** Source metal definition (Fig. 4.44e)
17. Deposition of final passivation layer
18. Deposition of planarization layer
19. **Mask #8:** Through-hole definition
20. Pixel ITO deposition (Fig. 4.44f)

After the TFT substrate and the color filter substrate (fabricated independently) are both completed, they are aligned and attached to each other. The resulting structure is an empty cell, which will be filled with LC material (typically by vacuum injection) and sealed. These additional steps complete the fabrication of the LCD panel.

As can be expected, many variations on the representative TFT process have been proposed and developed. Often, additional steps are inserted to accommodate processing schemes that are proprietary to specific display manufacturers. As a general trend, fewer processing steps (including reduced mask count) are preferable, for cost reduction. Therefore, significant effort has been placed on

 : poly-Si

Figure 4.44a



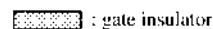
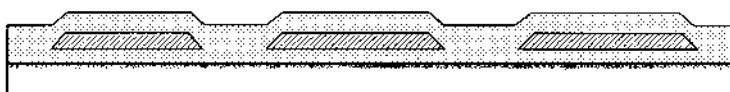
 : gate insulator

Figure 4.44 b



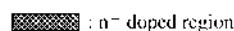
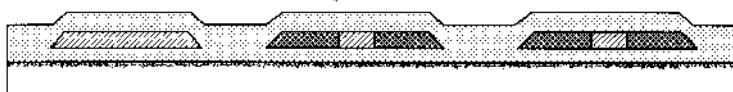
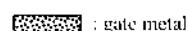
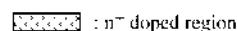
 : n⁻ doped region

Figure 4.44 c



 : gate metal

 : n⁻ doped region

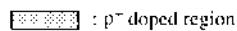
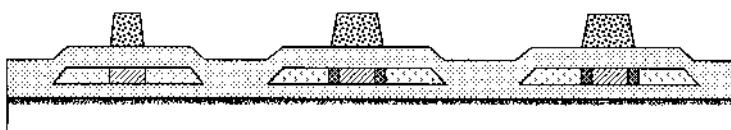
 : p⁻ doped region

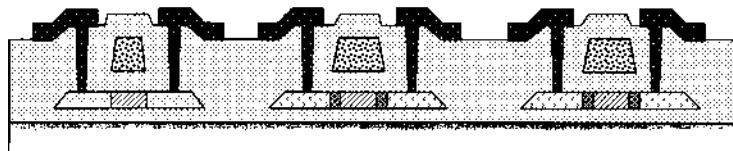
Figure 4.44 d



 : interlayer dielectric

 : source metal

Figure 4.44 e

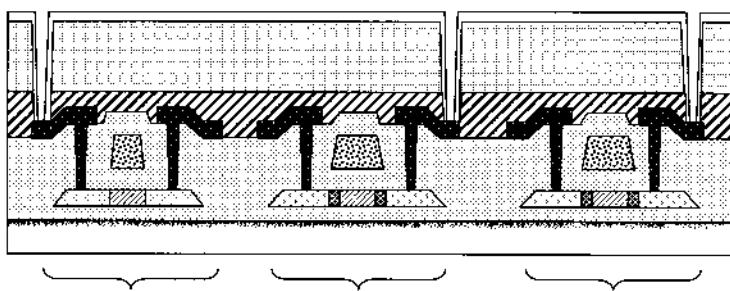


 : passivation layer

 : planarization layer

 : pixel ITO layer

Figure 4.44q



Driver p-ch TFT

Driver n-ch GOLDD

Pixel n-ch GOLDD

FIGURE 4.44 Process flow for top-metal-gate poly-Si TFTs with GOLDD (gate-overlapped lightly doped drain) configuration.

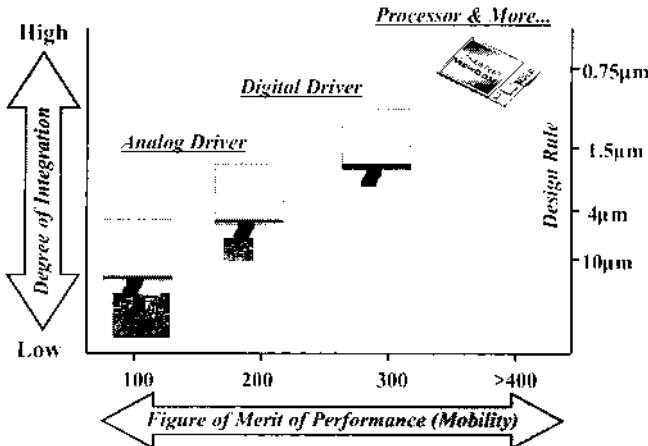


FIGURE 4.45 Evolution of LTPS displays and systems.

identifying ways to simplify, combine, and eliminate process steps without causing adverse effects on device performance. To reduce the mask count, particular emphasis has been placed on the simplification of LDD formation and the investigation of counterdoping process schemes [7]. For process reduction, emphasis has been placed on sequential processing, elimination of the dehydrogenation step after a-Si deposition, and in situ channel doping [115]. Continuing improvements of all processing steps is essential for the realization of the future generation of LPTS TFT LCDs and the realization of fully functional systems on a panel as depicted in Figure 4.45.

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5

Thin-Film Transistors in Active-Matrix Liquid Crystal Displays (AMLCDs)

Frank R. Libsch

IBM T. J. Watson Research Center, Yorktown Heights, New York, U.S.A.

5.1 ACTIVE-MATRIX DESIGN AND FABRICATION

Active-matrix liquid crystal displays (AMLCDs) remain the most mature and prevalent technology for notebook computers, portable computers, projection light valves, and miniature displays, due to their viewing characteristics (brightness, contrast, viewing angle, flicker-free images), low power consumption, light weight, and IC process compatibility. AMLCDs have even penetrated into the desktop monitor market and are competing with CRTs. The TFT performance, array design, and fabrication are dependent on the display product and market. For example, desktop monitor engineering specifications may emphasize higher visual performance, such as higher spatial resolutions, higher pixel content, wide viewing angle, NTSC (National Television System Committee) or larger color gamut, large area, and higher brightness, at a moderate price. Another large-area display product, such as HDTV (high definition television), would emphasize lower cost while accepting a lower-spatial-resolution lower-pixel-content display. The portable notebook computer display products emphasize low power and low weight. These three display products show that the competitive cost and pricing of the display is relative to the existing display products servicing that market. Therefore, reducing the total display module cost is always a key issue for success.

Given that passive-matrix arrays exist and are slightly less expensive to fabricate than active-matrix arrays, it would be prudent to understand when a passive-matrix array design is sufficient and when an active-matrix array design is necessary. Figures 5.1 and 5.2 show the electrical schematic and functional cross-sectional diagram of a passive matrix and an active matrix, respectively. It should be noted that the difference in passive- and active-matrix fabrication process costs has diminished in recent years due in a large part to the greater reduction in the number of processing levels for the active matrix as well as the realization

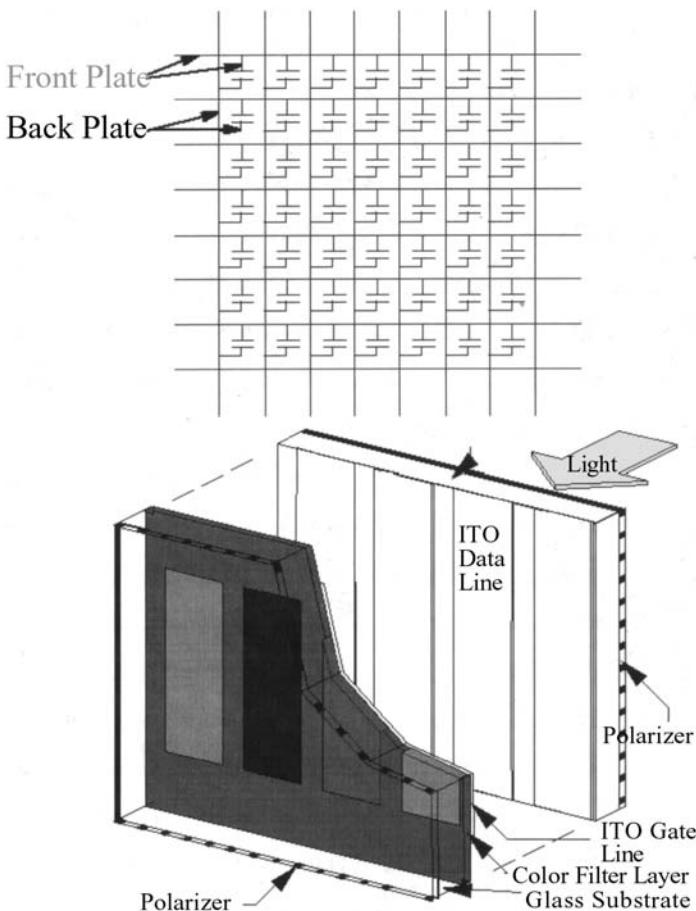


FIGURE 5.1 Electrical schematic showing a 7×7 array (top) and four-subpixel cross section (bottom) of a passive-matrix LCD.

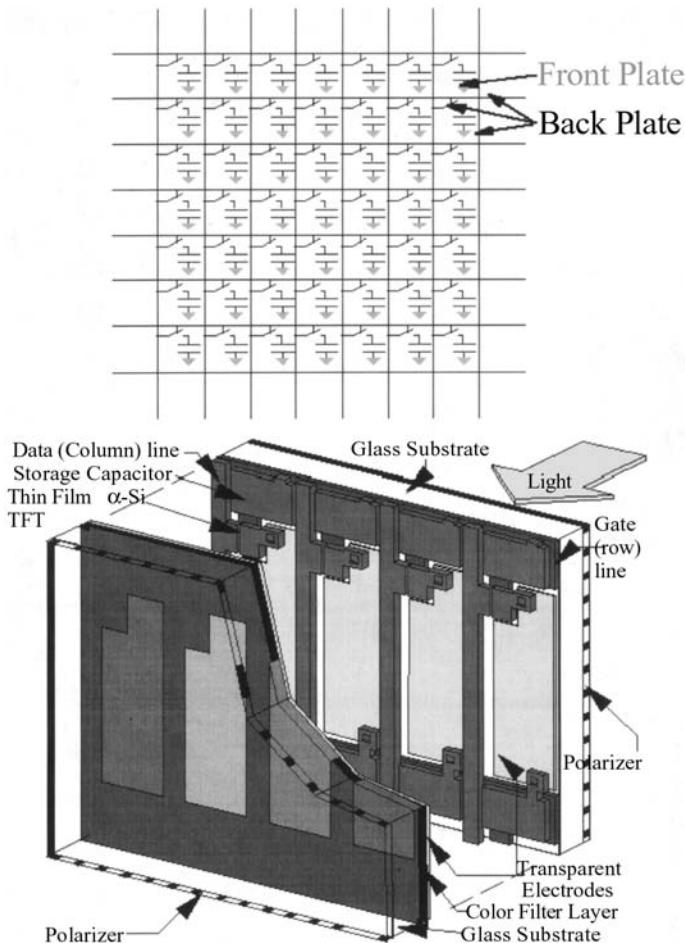


FIGURE 5.2 Electrical schematic showing a 7×7 array (top) and four-subpixel cross section (bottom) of an active-matrix LCD.

of higher yields in manufacturing. It is not uncommon to find a-Si TFT active-matrix manufacturers that employ a four-lithographic-step process with yields in the upper 90th percentile [1]. A passive-matrix array consists of two sets of electrically isolated conducting ITO bus lines (row and columns) arranged orthogonally to form the two LC-capacitor-pixel electrodes at each intersection, and connected to integrated circuit drivers that supply the necessary voltage and timing sequence. Normally, the display is scanned or multiplexed row by row from

the top to the bottom at a rate sufficient to produce flicker-free images (>60 Hz). The LC material follows the root mean square (rms) of the voltage over time. When the proper voltage difference is generated across a row and column intersection, an LC capacitor pixel is selected. A result of this arrangement is that the nonselected pixels unintentionally also receive some fraction of the voltage, or passive-matrix crosstalk. The LC molecules in the unselected pixels are partially aligned by the electric field, reducing the contrast between the OFF and ON pixels in the display. For example, a normally white LC passive-matrix display with N_s scanned rows, with only one row being activated at any given time and with a row voltage amplitude of V_r every T_f/N_s time, where T_f is the frame time, and the column lines with a voltage amplitude extreme of either $+V_c$ for a nonswitched white pixel (normally white LC display) or $-V_c$ for a pixel to be switched to a black state, the activated row of pixels have voltage amplitude extremes across the LC capacitor, V_p , being either

$$V_p = V_r + V_c \quad \text{for a nonswitched white pixel} \quad (5.1)$$

or

$$V_p = V_r - V_c \quad \text{for a switched black pixel} \quad (5.2)$$

Likewise for the $(N_s - 1)$ nonactivated rows at potential 0 V, the voltage extreme across the LC capacitor cells is

$$V_p = \pm V_c \quad (5.3)$$

The rms voltage of the nonswitched pixel during T_f is

$$\begin{aligned} V_{\text{white}} &= \frac{1}{\sqrt{T_f}} \sqrt{\frac{T_f}{N_s} (V_r + V_c)^2 + \frac{T_f}{N_s} (N_s - 1)V_c^2} \\ &= \frac{1}{\sqrt{N_s}} \sqrt{(V_r + V_c)^2 + (N_s - 1)V_c^2} \end{aligned} \quad (5.4)$$

and for the switched pixel is

$$V_{\text{black}} = \frac{1}{\sqrt{N_s}} \sqrt{(V_r - V_c)^2 + (N_s - 1)V_c^2} \quad (5.5)$$

The ratio $V_{\text{white}}/V_{\text{black}}$ is a maximum for

$$\frac{V_r}{V_c} = \sqrt{N_s} \quad (5.6)$$

resulting in a black-state-to-white-state voltage ratio of

$$\frac{V_{\text{white}}}{V_{\text{black}}} = \sqrt{\frac{\sqrt{N_s} + 1}{\sqrt{N_s} - 1}} \quad (5.7)$$

As can be seen, $V_{\text{white}}/V_{\text{black}}$ of Eq. (5.7) approaches 1 for large N_s . For example,

for $N_s = 100$, Eq. (5.7) gives a maximum voltage ratio of 1.11. Equation (5.6) provides $V_r = 10V_c$. For a 5-V LC, $V_o = \pm 2.5$ V, resulting in a rather high voltage for $V_r = 25$ V. The maximum number of row lines acceptable under passive array addressing and/or the contrast ratio can be somewhat increased by other means, such as (1) introducing a chiral additive to the LC to produce a super twisted nematic liquid crystal (STNLC) (270°) that exhibits a steepening of the voltage-contrast response curve, (2) implementing the dual scanning of one row at a time from the top half of the display while simultaneously scanning one row at a time from the bottom half of the display, provided the column lines are not continuous through the center of the display, and (3) “active” addressing to optimize nonsequential row and column scanning to minimize crosstalk. However, these means have some drawbacks; namely, the STNLC requires increased precision in fabrication, only lower color quality is possible, and a relatively slower response time exists that is subpar for video images. Obviously, the dual-scan mode now has twice the number of column lines and requires twice the number of column drivers and associated costs, as well as requiring additional bezel area to accommodate the double side (top and bottom) column drivers. Also, “active” addressing of a passive matrix requires additional cost in system hardware and control software. Active-matrix addressing is thus required when the number of display row lines exceeds approximately 250 ($\sim \frac{1}{4}$ VGA pixel content) to ensure an acceptable display LC on/off contrast ratio; this was first quantified by Alt and Pleshko [2].

Active-matrix addressing overcomes the half-select passive-matrix crosstalk limitation by integrating switching devices at the cross point of the row (scan or gate) and column (data or video signal) lines, and thereby isolating the off pixels from these select voltage lines. These switching devices consist of either two-terminal or three-terminal devices. The two-terminal device is typically a Schottky or PIN diode that passes current one way, usually made of amorphous silicon, or a bidirectional current-passing metal–insulator–metal (MIM) structure, usually with the an insulator film composed of PECVD-deposited silicon nitride (SiN_x), diamond-like carbon (DLC), or tantalum pentoxide (Ta_2O_5) [3,4]. The three-terminal array switches are field-effect transistors (FETs), such as crystalline Si metal oxide–semiconductor field-effect transistors (MOSFETs) or thin-film transistors (TFTs). Costs and lithography-stitching limits dictate that the crystalline Si active-matrix chips be restricted to small size (≤ 1 in.²), high-resolution displays, such as head-mounted displays and light valves commonly used in projection displays. When TFTs are used in AMLCDs, the TFT channel semiconductor film is composed of either amorphous Si, various degrees of recrystallized a-Si (polysilicon), or CdSe, and most recently, even organic materials, such as pentecene, are being considered [5]. The TFT active-matrix array designs are commonly optimized using computer simulations to analyze electrical performance based on statistically extracted TFT and fabrication process parameters.

While this approach is the most accurate way to predict the statistical mean and variance in display performance, it is more instructive to carry out a simple, physically based parameter analysis to identify functional dependencies, performance limits, and minimum requirements, and it is this analysis that will be employed for insight where possible in this chapter [6]. The analysis presented here is applicable to any kind of TFT processing technology.

5.1.1 AMLCD Array Requirements and TFT Specifications

Table 5.1 lists the major TFT AMLCD design factors. The pixel size, the TFT geometry, and the desired fill factor will determine the amount of parasitic capacitance to the adjacent rows and columns, while the display size and pixel content will dictate the resistance of the row and column lines. The number of rows and the frame time will determine the charging time of the pixel capacitance, which includes the LC capacitor, and the charge retention time. The number of gray levels will determine the minimum TFT on-current to accurately charge up the pixel. The LC mode will determine the pixel voltage. The allowable gray bit error rate, along with specifications for flicker, will determine the TFT and pixel off-current. [Table 5.2](#) specifically summarizes what the TFT performance requirements need to be for TFT AMLCDs, with [Figure 5.3](#) showing an I_{ds} vs. V_{gs} TFT characteristic, with the corresponding requirements labeled; these are specified in greater detail in Sections 5.1.1.1 through 5.1.1.5. The variation in TFT temperature dependence is as a function of TFT film quality and composition, device structures, and fabrication processing, and as such it is understood that the worst-

TABLE 5.1 Major TFT/AMLCD Design Factors

TFT AMLCD design factors	Examples
Display size	Diagonal (14'', 15'', 18'', 20'', 40'', etc.)
Light modulator/mode	(TNLC-NW, TNLC-NB, IPS, FELC, etc.)
Illumination conditions	Contrast ratio (2:1, 300:1, etc.), maximum brightness (100 cd/m ² , 250 cd/m ² , 500 cd/m ² , etc.), ambient illumination (dark room, room light, sunlight readable, etc.)
Display format (number of lines)	Content (VGA, SVGA, XGA, SXGA, UXGA, QUXGA-W, etc.),
Frame time	Film, 1/24 s; video, 1/30 s; data 1/60 s; etc.
Number of gray levels	6-bits (262K colors), 8-bits (16.8M colors), etc.
TFT geometry	Bottom-gate staggered BCE, I-stopper, top gate, etc.
Fill factor	30%, 60%, 75%, 100%

TABLE 5.2 TFT Performance Requirements in AMLCDs

Requirements	Typical numerical values from Figure 5.3
<i>Static requirements</i>	
$I_{\text{off}} < I_{\text{off}} (\text{max})$ over dV_{gs} (off), $V_{dl} \leq V_d \leq V_{dh}$	$I_{\text{off}} < 2 \times 10^{-13} \text{ A}$
$I_{\text{on}} > I_{\text{on}} (\text{min})$ at V_{dh} , over dV_{gh} (<i>Margin</i>)	$I_{\text{on}} (\text{min}) > 2 \times 10^{-7} \text{ A}$ for $V_{dh} = 10 \text{ V}$
$I_{\text{on}} / I_{\text{off}} \gtrsim 4 \times 10^6$ for SXGA, 8 bit linear, $\frac{1}{2}$ LSB error	$I_{\text{on}} / I_{\text{off}} > 10^6 \text{ A}$ for V_{dh}
dV_{gs} (off) $\gtrsim \Delta V_t + \Delta V_{dh}$	dV_{gs} (off) = 17 V
dV_{gh} (<i>Margin</i>) $\gtrsim \Delta V_t + d\Delta V_p$	dV_{gh} (<i>Margin</i>) = 8.5 V
dV_g (max) $\gtrsim dV_g$ (Driver) – dV_g (comp)	dV_g (max) = 35 V dV_g (Driver) = 40 V dV_g (comp) = 5 V
<i>Dynamic requirements</i>	
C_p (max) chargeup in nt_s , $n \approx 5$ (6 bit) $n \approx 6$ (8 bit linear) $n \approx 7$ (8 bit nonlinear)	Pixel layout and technology specific ($u, W, L, C_{gs}, R_s, R_d$)
$C_{gs} \leq C_p$ (max) [ΔV_p (max)/ ΔV_g (max)]	Pixel/TFT layout

case I_{ds} vs. V_{gs} TFT characteristics, over the display's operating temperature range, must be measured and applied to the TFT requirements. I_{on} is defined for the highest data-line voltage, V_{dh} , since this allows the least amount of TFT gate drive (V_t) and thereby determines the longest pixel charge-up time. Note that the I_{off} (max) must be ensured over a range of dV_{gs} (off) $\gtrsim \Delta V_t + V_{dh}$; even though the scan driver gate voltage will not be this value, allowances must be made for the source (or drain) voltage being at the maximum voltage of V_{dh} . Since ΔV_t , the TFT threshold voltage shift, is discussed in an earlier chapter, it will not be discussed here. There is a complete set of data and knowledge in the literature [7]. The key TFT scaling equations explicitly detailing technology and geometry parameters are given in the following sections.

5.1.1.1 Dynamic TFT Requirements ($I_{\text{on}}/I_{\text{off}}$ Ratio, Pixel Charge-up Time, and Voltage Feed-Through Switching Errors)

The charging requirements are dictated by the light-modulator load of the pixel. In the analysis to follow, it will be understood that the light modulator used as the example will be the twisted nematic liquid crystal (TNLC), such as a normally

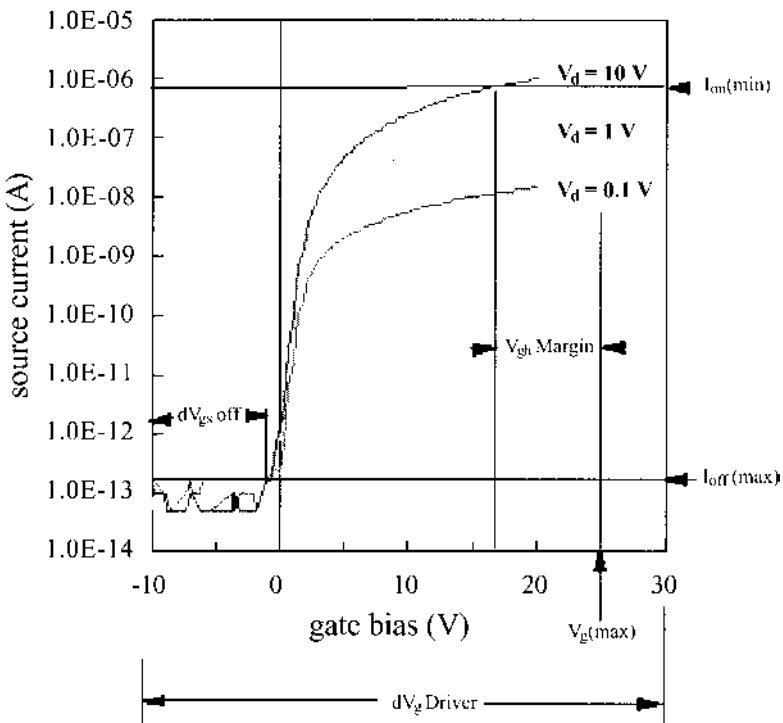


FIGURE 5.3 A-Si TFT input I - V characteristics of $W/L = 1$, with drain voltage as a parameter, logarithmically stepped, defining AMLCD TFT requirement terms.

white mode with a typical transmission vs. data voltage as shown in Figure 5.4. The trend toward higher-grayscale-resolution AMLCDs implies controlling the voltage at each pixel location to an equivalent voltage of less than half the least significant bit (LSB) over a frame time.

Figure 5.4 shows a normally white-mode TNLC characteristic with the relative transmittance varying with the applied bias, where white (100% transmission), black (0% transmission), and gray (50% transmission) levels are given by 1.2, 2.15, and 4.06-V, respectively. As a point of illustration, if the liquid crystal threshold voltage is 1.2 V and a full ON-voltage is 4.06 V, then there are 256 voltage steps of approximately 11 mV (linear 8-bit signal driver, or $[(4.06\text{ V} - 1.2\text{ V})/256]$) each to span the transition region from ON to OFF. Pixel charge-up to one-half LSB, or ~ 5.5 mV from the opposite polarity, produces voltage error rates of approximately 0.23%, 0.13%, and 0.07%, respectively, for white

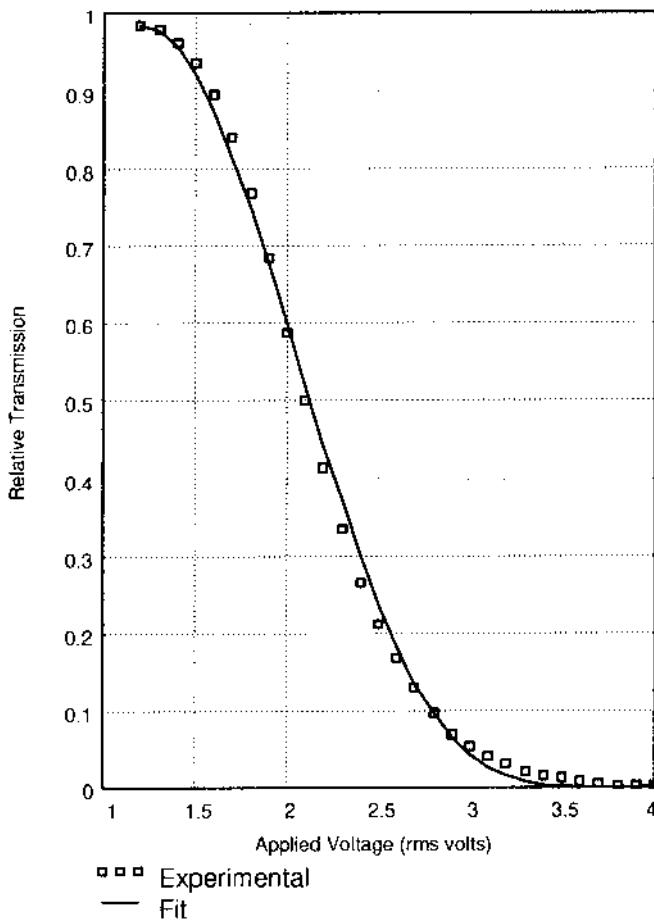


FIGURE 5.4 Transmission of a normally white TNLC display versus applied voltage across the cell (solid line) with overlay of simulations for gamma = 2.2 (squares).

(100% transmission), midgray (50% transmission), and black (0% transmission) levels. Pixel charge-up during the available scan time to an error rate between $\sim 0.09\%$ and $\sim 0.25\%$ requires six time constants. However, the resulting luminance steps are not linear. If linear luminance steps are desired, however, additional considerations must be invoked to determine the voltage precision required. Not only is the transmission–voltage (T – V) curve of the TNLC cell nonlinear, but the desired luminance vs. grayscale code (l vs G) of the display is also

nonlinear (a power function). That is, the “gamma” of the display wants to be approximately 2.2.

$$l = l_0 + kG^\gamma, \quad \gamma = 2.2, \quad G = 0, 1, \dots, 255 \quad (5.8)$$

The voltage requirements can be estimated by first fitting the T - V curve with a mathematical function. The voltage region of interest is from the LC threshold voltage, V_{th} to the full ON-voltage V_{on} . The T - V curve is perceptually flat below V_{th} and above V_{on} (by definition). Using two points [$T(V_{\text{th}})$ and $T(V_{\text{on}})$] and one adjustable parameter (K), a fit to the experimental data is also shown in [Figure 5.4](#). This fit is sufficient to estimate the voltage precision requirements. The function used for the fit is given by the following expression:

$$T = T(V_{\text{on}}) + T(V_{\text{th}}) \cos^4 \left[K \frac{\pi}{2} (V - V_{\text{th}})(V_{\text{on}} - V_{\text{th}}) \right] \quad (5.9)$$

where $V_{\text{th}} = 1.2$ V, $V_{\text{on}} = 4.06$ V, $K = 1.09$, $T(1.2$ V) = 0.985, and $T(4.06$ V) = 0.001. Using Eqs. (5.8) and (5.9) and the fact that the luminance of a display is proportional to its transmission, an expression for the LC voltage as a function of the desired grayscale code can be written. This relationship is obviously nonlinear, but the particular item of interest here is how large the voltage steps between levels are if one desires 256 gray levels of equal steps in luminance. Figure 5.5 shows the voltage steps between levels for 256 levels and a gamma of 2.2. Notice that the steps will be smaller near midtransmission or midluminance, with the minimum step approximately 6.6 mV and the maximum step an order of magnitude larger.

The result is interesting for a few reasons. First, the *nonlinear* 8-bit driver that produces equal-luminance steps has approximately one-half the minimum

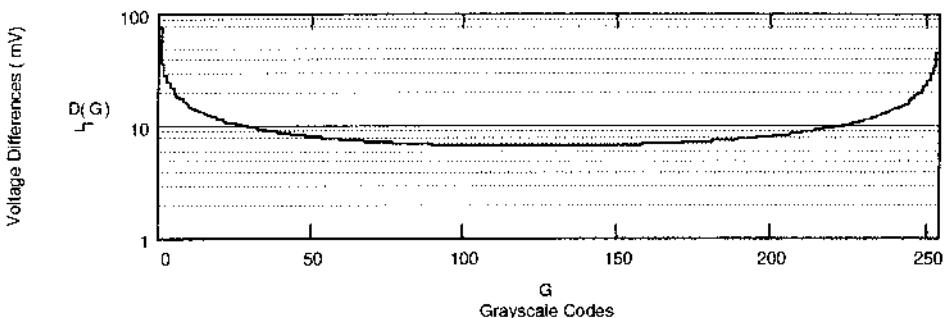


FIGURE 5.5 Applied voltage difference of the normally white TNLC display cell of [Figure 5.5](#) versus 256 grayscale levels equally stepped in luminance.

gray-level step size, compared to the *linear* 8-bit driver, that produces equal gray-level voltage steps (6.6 mV versus 11 mV). Second, pixel charge-up during the available scan time to an error rate of one-half LSB would require seven time constants, versus six time constants, respectively, for the nonlinear 8-bit driver versus the linear 8-bit driver. Third, the one-half LSB voltage error of approximately 3.3-mV steps for midgray (50% transmission), or 0.08% ($\sim 3.3 \text{ mV}/4.3 \text{ V}$) charging data voltage error, corresponds to a luminance error of $1/(256 \times 2) \times 100\%$, or approximately 0.2%. The AMLCD front-of-screen luminance limit of error detection by a human is dependent on many factors, such as display contrast, brightness, and image, but in general is closer to a 0.5% luminance error, or an approximate corresponding 0.25% charging data voltage error at midgray.

The pixel time constant can be approximated by using the equivalent pixel resistance, which translates to the TFT resistance, and the total capacitance of the subpixel. As shown in Figure 5.6, during pixel charging, as the gate pulse is increased, the TFT goes from an off-state, through the subthreshold region, through saturation since the data-line pulse temporally precedes the scan-line pulse ($V_{ds} > V_{gs} - V_t$), and into the linear regime ($V_{ds} < V_{gs} - V_t$). Since most of the pixel charging time, especially the final pixel voltage value, takes place with the TFT in the linear region, the TFT channel current, I_c , is model subject to the gradual channel approximation, with the channel current in the accumulation layer given by [8]

$$I_c = W\mu C_{\text{gate}} (V_{gs} - V_t - \phi) \frac{d\phi}{dx} \quad (5.10)$$

over the channel range, x , shown in the TFT cross section of Figure 5.7, where

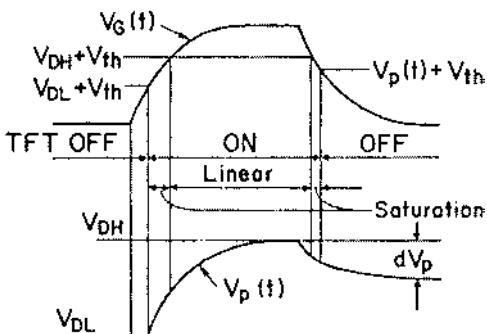


FIGURE 5.6 Dynamic response of an AMLCD pixel TFT during pixel retention (TFT off) and pixel write times as a function of the scan line, data line, and pixel storage node voltage waveform. (From Ref. 92.)

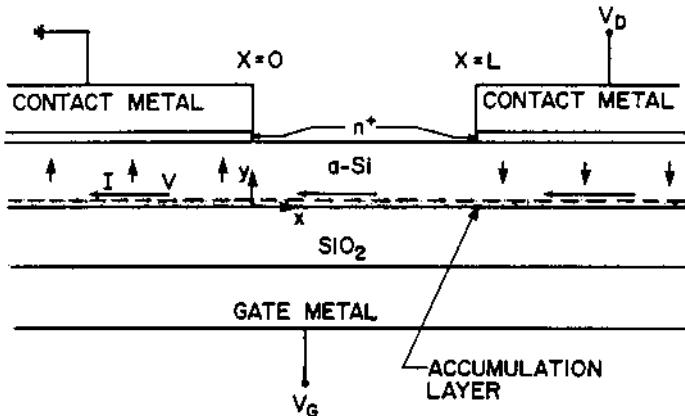


FIGURE 5.7 Vertical cross section of a typical bottom-gate staggered TFT illustrating the two-dimensional current flow across the a-Si layer from the drain contact, through the intrinsic TFT channel, to the source contact. The source and drain metal edges are defined at $x = 0$ and $x = L$, respectively.

W is the width of the channel, μ is the effective channel carrier mobility, C_{gate} is the gate capacitance (per unit area) of the insulator separating the gate from the channel, V_t is the threshold voltage, V_{gs} is the gate-to-source voltage, and ϕ is the surface potential in the accumulation layer. The channel mobility can be written as

$$\mu = \mu_0 \left(\frac{V_{gs} - V_t}{V_{gso} - V_t} \right)^r \quad (5.11)$$

where the exponent r accounts for the band-tail states, as discussed in earlier chapters, and μ_0 is the mobility at a particular gate voltage V_{gso} , such as the peak gate-line (i.e., scan-line) voltage. By assuming a good TFT with ohmic source and drain contact, thereby neglecting for now the bias-dependent series resistances at the source and drain (this TFT parasitic will be addressed in Section 5.15), the TFT channel current from Eq. (5.10), over the channel range $0 \leq x \leq L$, can be written as

$$I_{ds} = \mu C_{\text{gate}} \left(\frac{W}{L} \right) \left(V_{gs} - V_t - \frac{V_{tds}}{2} \right) V_{ds} \quad (5.12)$$

where L is the length of the channel and V_{ds} is the drain-to-source voltage. The TFT channel-on resistance for the usual case of array operation in the linear region, $(V_{gs} - V_t) > V_{ds}$, is written as

$$R_{tf}(on) = \frac{V_{ds}}{I_{ds}} \approx \frac{L}{\mu C_{gate} W(V_{gs} - V_t - V_{ds}/2)} = \frac{L}{\mu W Q_n} \quad (5.13)$$

where Q_n is the charge density (in C/cm^2) of the carriers in the channel. This approximation is, of course, not valid during the time the TFT is off or during the turn-on- and turn-off-transients, where the TFT operation is briefly in sub-threshold and the saturation region, as shown in [Figure 5.6](#). Due to the nonzero value of $R_{tf}(on)$, the TFT requires a nonzero time to charge or discharge the pixel capacitance through the on-TFT. An additional requirement of the LC, in order to avoid a DC-voltage offset across the pixel, is that the polarity of the video signal information alternate every frame time, T_f . Therefore, the available pixel scan time is $T_s = T_f/N_s$, where N_s is the number of scan lines in a display. Full grayscale implies controlling the voltage at each pixel location to an equivalent voltage of less than half the least significant bit (LSB) over a frame time. Note that this is a requirement not only on the video signal drivers but also on the uniformity of the array to render images to this precision. Pixel charge-up during the available scan time to an error rate between $\sim 0.09\%$ and $\sim 0.25\%$ requires six time constants. For a six-time-constant charging condition, the charging resistance can be written as

$$R_{tf}(on)(C_{LC} + C_s + C_{par}) \leq \frac{1}{6} T_s = \frac{1}{6} \frac{T_f}{N_s} \quad (5.14)$$

or

$$R_{tf}(on) \leq \frac{T_f}{6N_s(C_{LC} + C_s + C_{par})} \quad (5.15)$$

C_{LC} is the LC capacitance between the common electrode and the pixel electrode and C_s is the storage capacitance between the pixel electrode and either the adjacent gate line or separate C_s line. The total pixel parasitic capacitance, C_{par} , is given by

$$C_{par} = C_{PG} + C'_{PG} + C_{GS} + C_{PD} + C'_{PD} \quad (5.16)$$

C_{PD} and $C_{PD'}$ are the data-line and adjacent-data-line-to-pixel electrode coupling capacitance, respectively, C_{PG} and C'_{PG} are the gate-line- and adjacent-gate-line-to-pixel electrode coupling capacitance, respectively, and C_{GS} is the TFT gate-to-source parasitic overlap capacitance, as shown in [Figure 5.8](#). The data-line-to-pixel electrode coupling capacitance, C_{PD} , includes the contribution of drain-to-source and drain-to-gate TFT capacitances, C_{DS} and C_{DG} , respectively. The six-time-constant TFT on-time charging criteria used earlier represents an acceptable level in preventing visible front-of-screen nonuniform grayscale artifacts and within the capability of the 8-bit gray-level video signal drivers used in

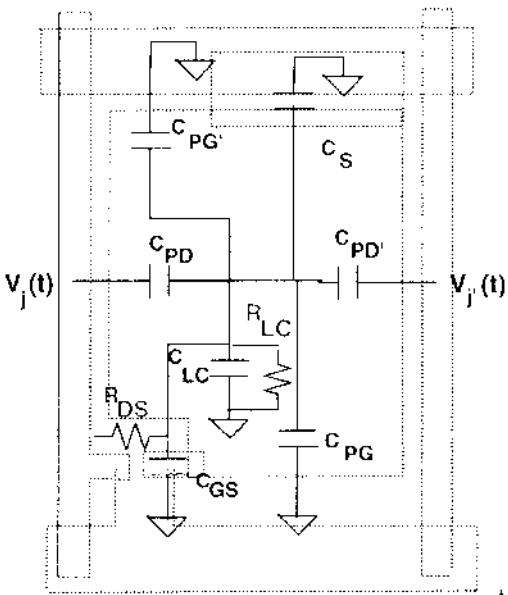


FIGURE 5.8 Equivalent TFT AMLCD pixel circuit for dynamic pixel response analysis (mutual capacitance of top-plate common electrode not shown) superimposed on pixel layout.

today's AMLCDs. From Eqs. (5.13) and (5.15), the minimum TFT mobility requirement is

$$\frac{W}{L} \geq \frac{6N_s(C_{LC} + C_s + C_{par})}{T_f C_{gate} (V_{gs} - V_t - \Delta V_t)} \quad (5.17)$$

If $N_s = 1280$ (SXGA pixel content), $(C_{LC} + C_s + C_{par}) = 500 \text{ fF}$, $T_f = 16.7 \text{ ms}$, $(V_{gs} - V_t - \Delta V_t) = (28 \text{ V} - 3 \text{ V} - 5 \text{ V})$, and $C_{gate} = 1.2 \times 10^{-7} \text{ F/cm}^2$, then $\mu(W/L) \geq 0.1 \text{ cm}^2/\text{V-s}$, a condition easily fulfilled by today's p-Si, a-Si, and even some organic TFT technologies. Typical a-Si TFT mobility in manufacturing today shows a mean value of $0.75 \text{ cm}^2/\text{V-s}$. ΔV_t accounts for the threshold voltage shift due to semiconductor and gate-insulator charge-trapping and bond-breaking mechanisms prevalent in many TFT technologies, over the life of the display.

In a similar manner, to avoid flicker that may result from a pixel DC voltage inducing a net luminance change between the positive and negative data-polarity cycles, as can be brought about by pixel charge leakage during the TFT off-time, the TFT off-current must satisfy

$$I_{ds}(\text{off}) \leq \frac{(C_{lc} + C_{\text{par}}) \Delta V_p(\text{min})}{T_f} \quad (5.18)$$

Here, $\Delta V_p(\text{min})$ is the change in V_p , representing the minimum pixel voltage just below detectability in either the pixel brightness (luminance) due to either the display fabrication uniformity, the human detectability, or the minimum gray-level increment of the video signal driver. For example, if $\Delta V_d(\text{min})$ is dictated by the video signal driver and is one-half LSB for an 8-bit *linear* driver, then the pixel off-time constant can be written as

$$R_{tf}(\text{off})(C_{lc} + C_s + C_{\text{par}}) \geq 2N_g T_f \quad (5.19)$$

or

$$R_{tf}(\text{off}) \geq \frac{2N_g T_f}{C_{LC} + C_s + C_{\text{par}}} \quad (5.20)$$

In general, Eq. (5.19) can be written

$$R_{tf}(\text{off})(c_{lc} + C_s + C_{\text{par}}) \geq \frac{T_f}{\text{greyscale error rate}} \quad (5.21)$$

The TFT on/off ratio requirement for an 8-bit linear driver, with one-half LSB error rate, is obtained by combining Eqs. (5.15) and (5.20), giving

$$\frac{R_{tf}(\text{on})}{R_{tf}(\text{off})} \gtrsim 12N_g N_s \quad (5.22)$$

Note that the R_{tf} (on)/ R_{tf} (off) ratio is directly proportional to the number of gray levels and the number of scan lines, dictating that higher-resolution and/or higher-gray-level-performance displays require larger TFT on/off ratios. For 256 equal gray-level voltage steps (8-bit linear) and an SXGA ($N_s = 1280$) pixel content display, Eq. (5.22) gives

$$\frac{R_{tf}(\text{on})}{R_{tf}(\text{off})} \gtrsim 4 \times 10^6 \quad (5.23)$$

In an ideal case, where the TFT's a-Si film dominates leakage, off-current is given by

$$I_{\text{off}} \approx \frac{\sigma_D dWV_{ds}}{L} \quad (5.24)$$

where σ_D is the dark conductivity of the a-Si. Since σ_D decreases with decreasing a-Si thickness, d , a-Si TFT AMLCD manufacturers minimize the a-Si film thickness. The typical I-stopper trilayer TFT structure's a-Si film thickness found in manufacturing is approximately 500 Å, with the BCE being slightly thicker ($\gtrsim 1000$ Å) to allow for the added etch-bias margin in forming the source/drain

contacts by etching through the $n+$ a-Si layer and stopping in the intrinsic a-Si layer.

Generally speaking, a:Si:H TFTs meet the requirements dictated by Eq. (5.22). If $d = 500 \text{ \AA}$, $W/L = 1$, and $\sigma_D \approx 10^{-9} \Omega\text{-cm}$, then the minimum a-Si TFT off-resistance possible calculated with the aid of Eq. (5.24) gives $R_{off}(\text{off}) \approx (V_{ds}/I_{off}) \approx 2 \times 10^{14} \Omega$, or $I_{off} \leq 5 \times 10^{-14} \text{ A}$ for $V_{ds} \leq 10 \text{ V}$. The required TFT off-current of Eq. (5.18) is plotted with the TFT off-current determined only by the a-Si film dark conductivity of Eq. (5.24) in Figure 5.9.

It should be mentioned that some AMLCDs, for example, vehicular, space, and aviation displays, need to operate in extremely challenging environments, such as a wide operating temperature range from subzero temperatures ($\sim -40^\circ\text{C}$) to elevated temperatures that exceed 80°C , bright sunlight ambient (8,000–10,000 fC) to pitch-black darkness, high humidity (up to 100% relative humidity), large mechanical stresses due to shock and vibration as encountered in automotive and aircraft operation, and mission-critical superior image quality and reliability [9,10]. The TFT resistance is both temperature and brightness (off-ratio only) sensitive. In full sunlight ($>50,000$ lux), the eye seems to be more sensitive to contrast than to brightness, so it may be preferable to enhance the contrast rather than the brightness, where a 2:1 contrast ratio is the minimum for acceptable viewability. For avionic displays, standard test specifications such as DO-160

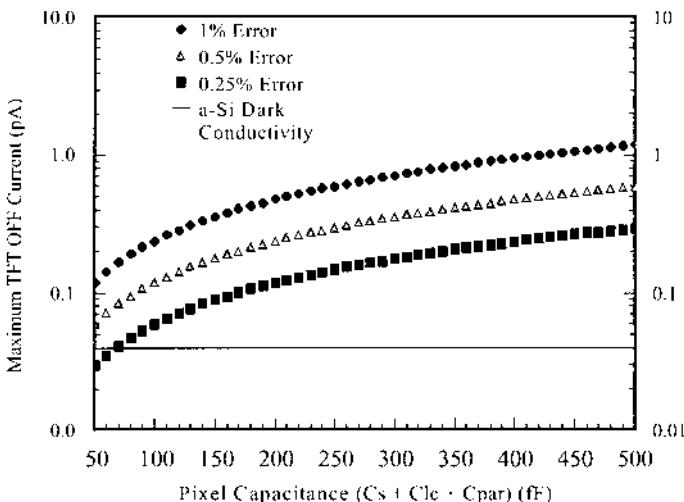


FIGURE 5.9 Maximum pixel off-current tolerated versus pixel capacitance as a function of pixel voltage error. The solid line denotes the minimum intrinsic (dark state a-Si conductivity) TFT leakage as a reference.

and MIL-STD-810 are used to qualify the display for environmental performance. The AMLCD design and performance parameters for these displays often involve a lower TFT threshold voltage shift, lower TFT and LC off-current, lower photo-sensitivity with the help of black matrix shielding, lower pixel voltage offset, and grayscale and temperature compensation drive. Of specific interest to the active matrix is the temperature dependence of the ON/OFF requirement, which is given by [11]

$$\frac{R_{tfi}(\text{on})}{R_{tfi}(\text{off})}(T) \approx \frac{R_{tfi}(\text{on})}{R_{tfi}(\text{off})}(T_0) \exp \left[\frac{E_a}{k_B} \left(\frac{1}{T_0} - \frac{1}{T} \right) \right] \quad (5.25)$$

where k_B is Boltzmann's constant and T_0 and T represent the temperature of measurement for the ratio $R_{tfi}(\text{on})/R_{tfi}(\text{off})$ and the display operating temperature, respectively. Some numbers reported in the literature [9] claim a decrease in the relative on to off-current ratio as a function of temperature, assuming an activation energy, E_a , of 0.7 eV [12]. Figure 5.10 shows that the a-Si TFT off-current increases approximately one order of magnitude for every 20°C increase in temperature, while the on-current increases by approximately a factor of 2, as a function of increasing temperature, and the ratio $R_{tfi}(\text{on})/R_{tfi}(\text{off})$ is decreasing.

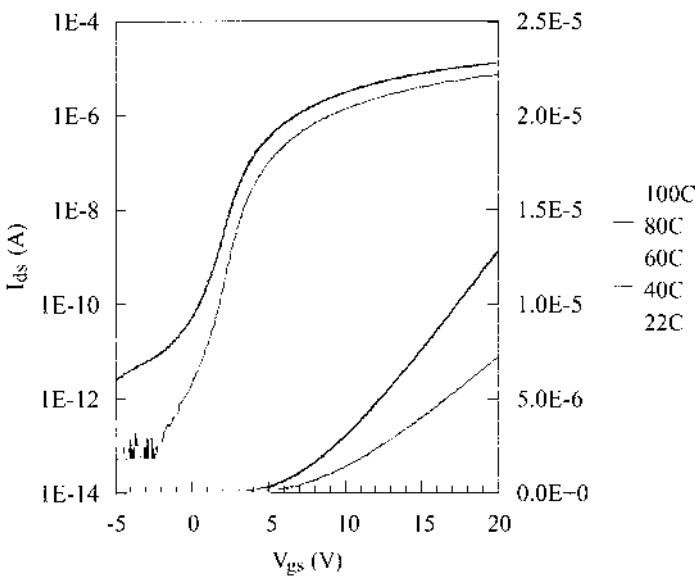


FIGURE 5.10 a-Si TFT I_{ds} versus V_{gs} temperature response. The curves on the left and the right correspond to the left-hand log (I_{ds}) and the right-hand linear (I_{ds}) vertical axes, respectively.

5.1.1.2 Off-Currents

After the pixel TFT is turned off, the pixel capacitance charge, representing a gray-level luminance, may unintentionally change due to leakage and photogenerated currents. Several sources for leakage currents may exist, such as TFT drain-to-source leakage, I_{ds} , TFT channel photogenerated currents, I_{phot} , low-resistivity storage capacitor insulator film, I_{l1} , or bulk LC material, I_{l2} , namely,

$$I_{\text{total(off)}} = I_{ds}(\text{TFT}) + I_{phot}(\text{TFT}) + I_{l1}(C_s) + I_{l2}(LC) \quad (5.26)$$

Of particular interest here is the maximum total leakage current that can be tolerated before a noticeable change is observed by the viewer of the display.

By assuming the condition that the only source of leakage current is I_{ds} of the TFT, we have established the absolute maximum TFT leakage current allowed. In actuality, this is a typical assumption, since LC materials with bulk resistivities in the range of $10^{12}\text{--}10^{13} \Omega\text{-cm}$ are commercially available, storage capacitor insulators, typically of SiO_x and/or SiN_x , are less than 1 nA/cm^2 , and black matrix light shielding can satisfactorily achieve low enough levels of photo-generated currents approaching 10^{-13} and $10^{-14} \text{ A}/\mu\text{m}$.

The stored video signal of the pixel is

$$V_p(t) = V_p(0^+) \exp\left(\frac{-t_1}{T_f}\right) \quad (5.27)$$

and the root-mean-square (rms) voltage across C_{LC} is

$$\begin{aligned} V_{prms} &= \left[\left(\frac{1}{T_f} \right) \int_{0^+}^{T_f} \{V_p(t)^2 dt\} \right]^{1/2} \\ &= V_p(0^+) \left[\left\{ 1 - \exp\left(-\frac{2T_f}{t_1}\right) \right\} \frac{t_1}{2T_f} \right]^{1/2} \end{aligned} \quad (5.28)$$

Here it is approximated that $t_s \ll T_f$, and $V_p(0^+)$ is the pixel voltage just after completion of pixel charge-up, $V_p(t)$ is the time-dependent pixel voltage, t_s is the row scan time, and t_1 is the pixel charge decay time constant, written as

$$t_1 = \left[\frac{R_{ds}R_{lc}}{R_{ds} + R_{lc}} \right] (C_{lc} + C_{par}) \quad (5.29)$$

As was illustrated and derived in Section 5.1.1.1, a maximum error rate of one-half LSB is usually targeted for high-performance AMLCDs, which, as we recall, results in a V_{rms} equal to 11 or 5.5 mV, respectively, for a linear- and nonlinear 8-bit video signal driven AMLCD. Equation (5.29) shows that the pixel charge decay time constant is proportional to the resistance of the leakage path (i.e., R_{lc} or R_{ds}) and to the pixel charge holding capacitance. C_s is usually the dominating pixel capacitance and is an important AMLCD design parameter. To help demon-

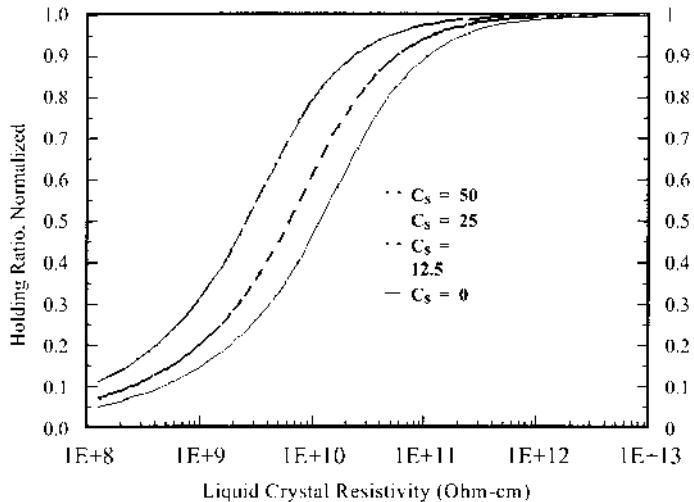


FIGURE 5.11 AMLCD pixel holding ratio versus liquid crystal resistivity as a function of added storage capacitance, ranging from 0 (left most curve) to 50 (right most curve). The added storage capacitance is normalized by the pixel area, or divided by $aF/\mu\text{m}^2$ ($10^{-18}\text{F}/\mu\text{m}^2$).

strate the importance of C_s , Figure 5.11 shows the holding ratio, which is defined as the ratio of V_{rms} ([Eq. (5.28)] for a frame time divided by the initial peak pixel electrode voltage, $V_p(0^+)$, for the example where the liquid crystal dielectric constant $\epsilon_{lc} = 8$ and the liquid crystal cell gap thickness $d_{lc} = 5 \mu\text{m}$. C_s is normalized to the pixel area, where $C_s = 50$ may represent a storage capacitance of 500 fF if the pixel area is $1 \times 10^4 \text{ cm}^2$ ($100 \mu\text{m} \times 100 \mu\text{m}$). When a pixel LC leakage path dominates, pixel discharge is typically to V_{com} , or across a voltage drop of $(V_p - V_{\text{com}})$. The effects of LC leakage currents on pixel voltage is shown in Figure 5.12 across a pixel bias drop of $(V_p - V_{\text{com}})$. When a pixel TFT leakage path dominates, pixel discharge is typically through the TFT channel to the video signal (data) line, or across a pixel bias $(V_p - V_D)$, where V_D is image dependent, since the data-line voltage changes with each scan time.

For a pixel dominated by the LC leakage currents, $R_{ds} \gg R_{ls}$, the pixel charge decay time constant can be approximated as

$$t_1 \approx R_{lc} (C_{lc} + C_s + C_{\text{par}}) \quad (5.30)$$

For a pixel dominated by the TFT off-current leakage through the TFT channel (I_{ds}), the pixel charge decay time constant can be approximated as $R_{ds} \ll R_{lc}$, or

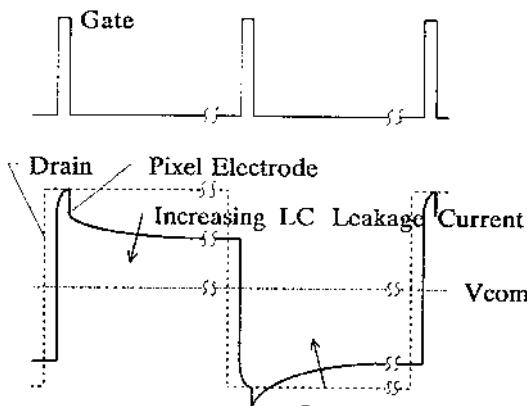


FIGURE 5.12 Gate-line, drain-line, common electrode, and pixel storage capacitance node waveforms corresponding to a large LC leakage current.

$$t_1 \approx R_{ds} (C_{lc} + C_s + C_{par}) \quad (5.31)$$

As seen from Eq. (5.18) and plotted in Figure 5.9, the maximum allowed TFT off-current is proportional to the pixel capacitance. In addition, differences in TFT fabrication technologies, device structure, and physical layout dimensions, such as channel width and length, influence the TFT off-current. Furthermore, the TFT off-current is a function of the TFT bias point as dictated by the AMLCD driving method, the front-of-screen image, and the location of the pixel in the display. The effects of the TFT leakage currents on pixel voltage is shown in Figure 5.13, resulting from the front-of-screen image and the pixel proximity in the display. Figure 5.14a shows the TFT off-current, I_{ds} , as a function of TFT drain-to-source and gate-to-source bias points; Figure 5.14b shows the TFT bias points assuming the frame inversion driving method and a video signal representative of a black state (black state of 2 V or 12 V). Note the bidirection I_{ds} current flow during TFT turn-on after regions B and D. Note the need for biasing V_g in the off-state less than -12 V to ensure no TFT turn-on during regions A and B. V_{com} is assumed with minimum DC offset at 7 V.

5.1.1.3 Nonideal Source and Drain Ohmic Contacts

A significant parasitic is the TFT source and drain resistance that can substantially limit pixel capacitance charging. In c-Si MOSFETs, and some previous TFT derivations in device current [13–15], the extrinsic MOSFET or TFT consists of an intrinsic device with series resistors added to its source and drain terminals. These boundary conditions give excellent results in MOSFETs where, at least in

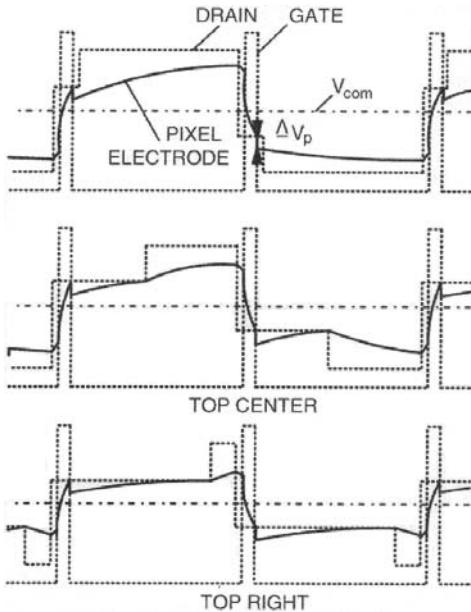


FIGURE 5.13 Gate-line, drain-line, common electrode, and pixel storage capacitance node waveforms corresponding to a large TFT off-current leakage, as a function of data-line voltage. The example illustrated corresponds to a pixel written in the white state (normally white LC), with the remaining column of pixels written mostly in the black state, 50% in the white state, and 50% in the black state, and mostly in the white state, for the top, center, and bottom group of waveforms, respectively.

the linear region of operation, the sheet charge actually connects to the source and drain diffusions. However, series resistance cannot account for the current crowding frequently observed near the contact electrode of the output characteristics of a staggered-electrode TFT. In the staggered TFT, the source and drain diffusions do not directly contact the channel. Powell and Orton [16,17] have simulated current crowding by adding the current–voltage characteristics for an $n^+ - i - n^+$ structure in series at the source and drain of an “ideal” a-Si staggered-electrode TFT, where the space-charge-limited currents (SCLC) were calculated assuming a constant density of deep states and a linear density of tail states. However, it was shown [8] that the current–voltage characteristics for an equivalent lumped series element, as derived from the two-dimensional current flow under the source and drain contacts, can have a significantly different behavior than the characteristic for the one-dimensional current flow in an $n^+ - i - n^+$ struc-

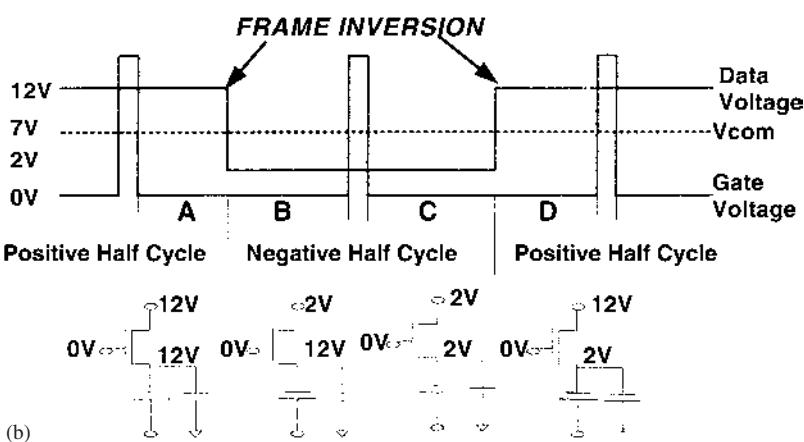
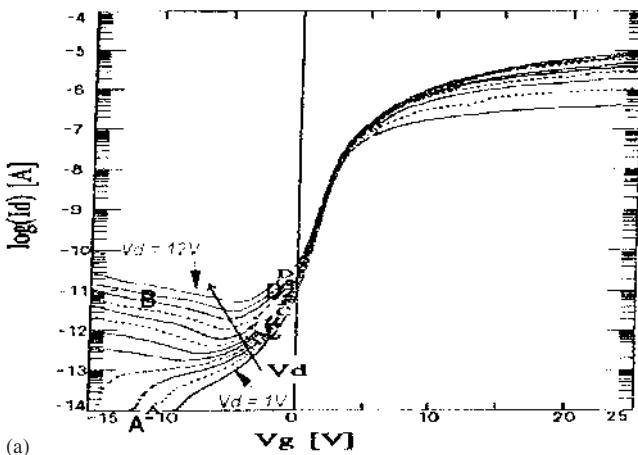


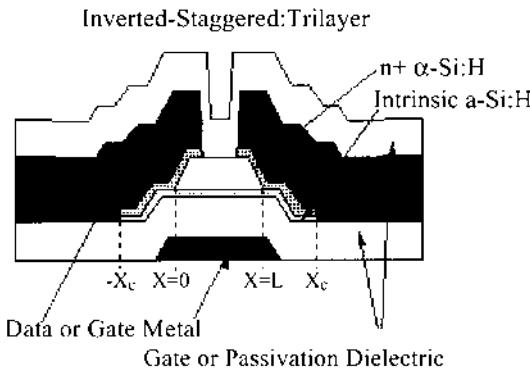
FIGURE 5.14 The influence of the data line voltage on the pixel's a-Si TFT off-state voltage. (a) $\log (|I_d|)$ versus V_g showing four points (labeled A, B, C, and D) of operation during the TFT off-state for frame inversion. (b) The gate-line, drain-line, and common electrode waveforms and simplified equivalent pixel circuit corresponding to the four points (A, B, C, and D). The pixel is written in the black state (5 V, normally white LC) with the remaining column of pixels written in the black state.

ture. Possin et al. [18] investigated the effects of SCLC on staggered-electrode TFT characteristics by measuring the one-dimensional SCLC behavior in an $n^+ - i - n^+$ structure, fitting this data to a polynomial and then combining these characteristics with the standard equations for MOSFET current under the source contact. Their analysis accounts for a finite overlap of the source contact to the gate electrode, and they clearly show that overlaps of less than 2 μm can reduce the available current. However, they neglected SCLC under the drain contact, which also reduces current in TFTs operating in the linear region, and they also neglected the gate voltage dependence of mobility. A model [19] has been developed that accounts for a gate-dependent mobility in a manner similar to Ref. 6 and for two-dimensional current flow under both source and drain contacts as in reference [20], but numerical analysis is needed.

Nonetheless, for good-quality TFTs, as is typically found today in production, current conduction through the a-Si film is linear at low injection levels and, when processed properly, the source and drain contacts of a staggered TFT can exhibit ohmic behavior at low drain-to-source bias. [Figure 5.15](#) illustrates two types of source and drain contacts frequently used in TFT fabrication, which were discussed in an earlier chapter. In general, the trilayer TFT structure, shown in [Figure 5.15a](#), has a lower source and drain series resistance than the BCE TFT structure, shown in [Figure 5.15b](#), due to the thicker a-Si film needed in the BCE TFT to allow for etch bias selectivity during fabrication. The following analysis models the staggered TFT with an intrinsic TFT, defined as the region $0 \leq x \leq L$ in [Figure 5.15b](#), with bias-dependent series resistance at the source and drain electrodes and with gate-bias dependent mobility [21]. The channel current was given by Eq. (5.1) over the range $-x_0 \leq x \leq L + x_0$, where x_0 is the magnitude of the source or drain electrode length contacting the a-Si film and the origin $x = 0$ is located at the inside edge of the source contact. The gate-bias-dependent mobility was given by Eq. (5.11). Under the source contact there is vertical current flow from the accumulation layer to the source electrode, whereas the intrinsic channel current ($0 \leq x \leq L$) is constant without a vertical current flow. At high gate drive, the electron distribution in the accumulation layer is not affected by a small voltage drop across the intrinsic a-Si film, and it is assumed that for vertical current flow the accumulation layer behaves similarly to an n^+ a-Si layer. Measurements on $n^+ - i - n^+$ structures have shown that current conduction through the film is ohmic when the voltage drop across the film is small, so over the range $-x_0 \leq x \leq 0$,

$$\frac{dl_c}{dx} = \frac{W\phi}{R_c} \quad (5.32)$$

where R_c is the effective contact resistivity to the accumulation layer. The boundary conditions on channel current under the source contact are $l_c(x = x_0) = 0$



Inverted-Staggered: Back-Channel Cut

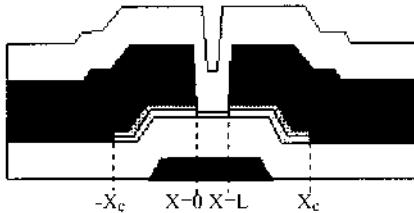


FIGURE 5.15 Cross sections of staggered bottom-gate TFTs used in commercial AMLCDs.

and $I_c(x = 0) = I_{ci}$, where I_{ci} is the channel current for the intrinsic TFT. Solving Eqs. (5.10) and (5.32), subject to the mentioned boundary conditions, yields

$$I_{ci} = W \sqrt{\mu C_{\text{gate}} (V_{GS} - V_t)/R_c} V_{s'} \tanh(x_0/\gamma_s) \quad (5.33)$$

where the characteristic length for current decay at the source contact is

$$\gamma_s = \sqrt{R_c \mu C_{\text{gate}} (V_{gs} - V_t)}$$

and $V_{s'} = \phi(x = 0)$ is the effective source voltage of the intrinsic TFT. Thus, the net effect of current collection at the source is to add a series resistance,

$$R_s = \frac{V_{s'}}{I_{ci}} = \frac{R_c}{W\gamma_s \tanh(x_0/\gamma_s)} \quad (5.34)$$

at the source terminal of the intrinsic TFT. When the gate-to-drain overlap is

also x_0 , there is an equal series resistance R_D at the drain terminal of the intrinsic TFT, and a valid approximation for identical processing and symmetrical contacts is to assume $R_D \approx R_S$. To obtain a more general expression, integrating Eq. (5.10) from $x = 0$ to $x = L$ yields a second expression for the intrinsic TFT current, which gives the channel resistance at high gate drive as

$$R_{ch} = \frac{V_{D'} - V_{s'}}{I_{ci}} = \frac{L}{W\mu C_{gate} (V_{gs} - V_t)} \quad (5.35)$$

where $V_{D'}$ and $V_{s'}$ are the effective drain and source voltages, respectively, for the intrinsic TFT and V_D and V_S are the external drain and source voltages, respectively, as defined in the lumped model of Figure 5.16. For a small drain-to-source voltage V_{ds} at high gate drive, the resulting TFT current flow is then

$$I_{ds} = \frac{V_{ds}}{R_s + R_{ch} + R_d} \quad (5.36)$$

For the asymptotic series resistance for large characteristic lengths, where $x_0 \ll \gamma_s$, Eq. (5.34) can be approximated as

$$R_s \approx \frac{R_c}{Wx_0} \quad (5.37)$$

Notice that R_s depends only on the contact resistance normalized by the contact area and is independent of gate voltage. For large electrode contact lengths, where $\gamma_s \ll x_0$, Eq. (5.34) can be approximated as

$$R_s \approx \sqrt{\frac{R_c}{C_{gate}\mu_0 W^2}} (V_{gso} - V_t)^r (V_{gs} - V_t)^{-\left(\frac{r+1}{2}\right)} \quad (5.38)$$

For comparison, the calculated result of Eq. (5.34) is shown in [Figure 5.17](#) by

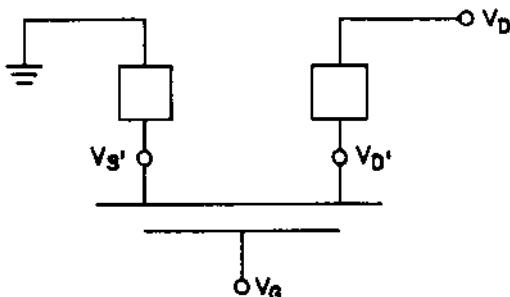


FIGURE 5.16 Electrical schematic of TFT consisting of intrinsic (ideal) TFT with source and drain (parasitic) series elements.

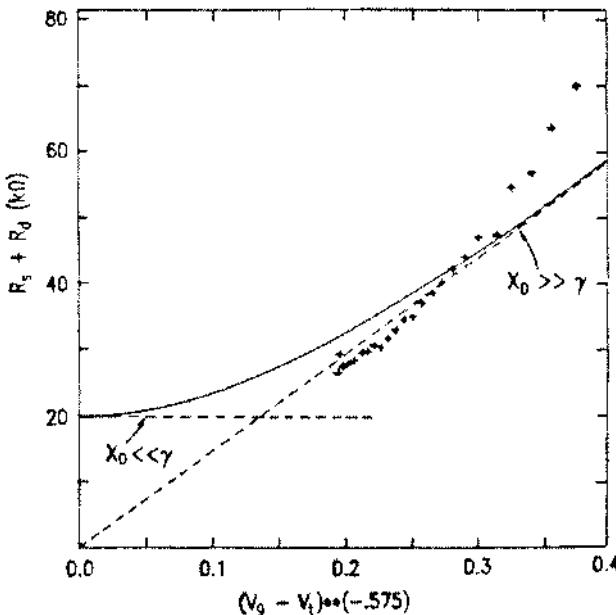


FIGURE 5.17 Determination of TFT source and drain effective contact resistance, R_c . The solid line is calculated from Eq. (5.34), using the extracted TFT parameters listed in Table 5.4. The dashed lines are asymptotic limits calculated from Eqs. (5.37) and (5.38) for very large ($x_0 \gg \gamma_s$) and very small ($\gamma_s \ll x_0$) characteristic lengths, respectively. (From Ref. 21.)

the solid line. The asymptotic series resistance for large characteristic lengths, Eq. (5.37), is $20 \text{ k } \Omega$, for a TFT with extracted values of $R_c = 0.5 \text{ } \Omega\text{-cm}^2$, $W = 1000 \text{ } \mu\text{m}$, and $x_0 = 5 \text{ } \mu\text{m}$, and is plotted with dashed lines. Some example extracted TFT parameters are summarized in Table 5.4.

As an example, three output characteristics ($V_g = 5, 10, 15, 20, 25 \text{ V}$) and their associated differential conductance plots are shown in Figure 5.18 [22]. The TFT parameters extracted are (1) long-channel $W/L = 50 \text{ } \mu\text{m}/50 \text{ } \mu\text{m}$, $\mu = 0.42 \text{ cm}^2/\text{V}\cdot\text{s}$, $V_t = 3.0 \text{ V}$, $R_s = R_d = 0 \text{ } \Omega$ (ideal source and drain contacts) for Figure 5.18a; (2) the same parameters except $R_s \approx R_d \neq 0 \text{ } \Omega$ for Figure 5.18b; and (3) short-channel $W/L = 50 \text{ } \mu\text{m}/4.5 \text{ } \mu\text{m}$, $\mu = 0.12 \text{ cm}^2/\text{V}\cdot\text{s}$, $V_t = 0.0 \text{ V}$, and approximately the same quality contacts with $R_s \approx R_d \neq 0 \text{ } \Omega$ for Figure 5.18c. Compared to Figure 5.18a (ideal $R_s \approx R_d \approx 0 \text{ } \Omega$), Figure 5.18b differential conductance shows distinct hooking for low drain bias and indicates source and drain electrode current crowding. Figure 5.18a shows no hooking. Figure 5.18c

TABLE 5.3 Example Extracted TFT Parameters

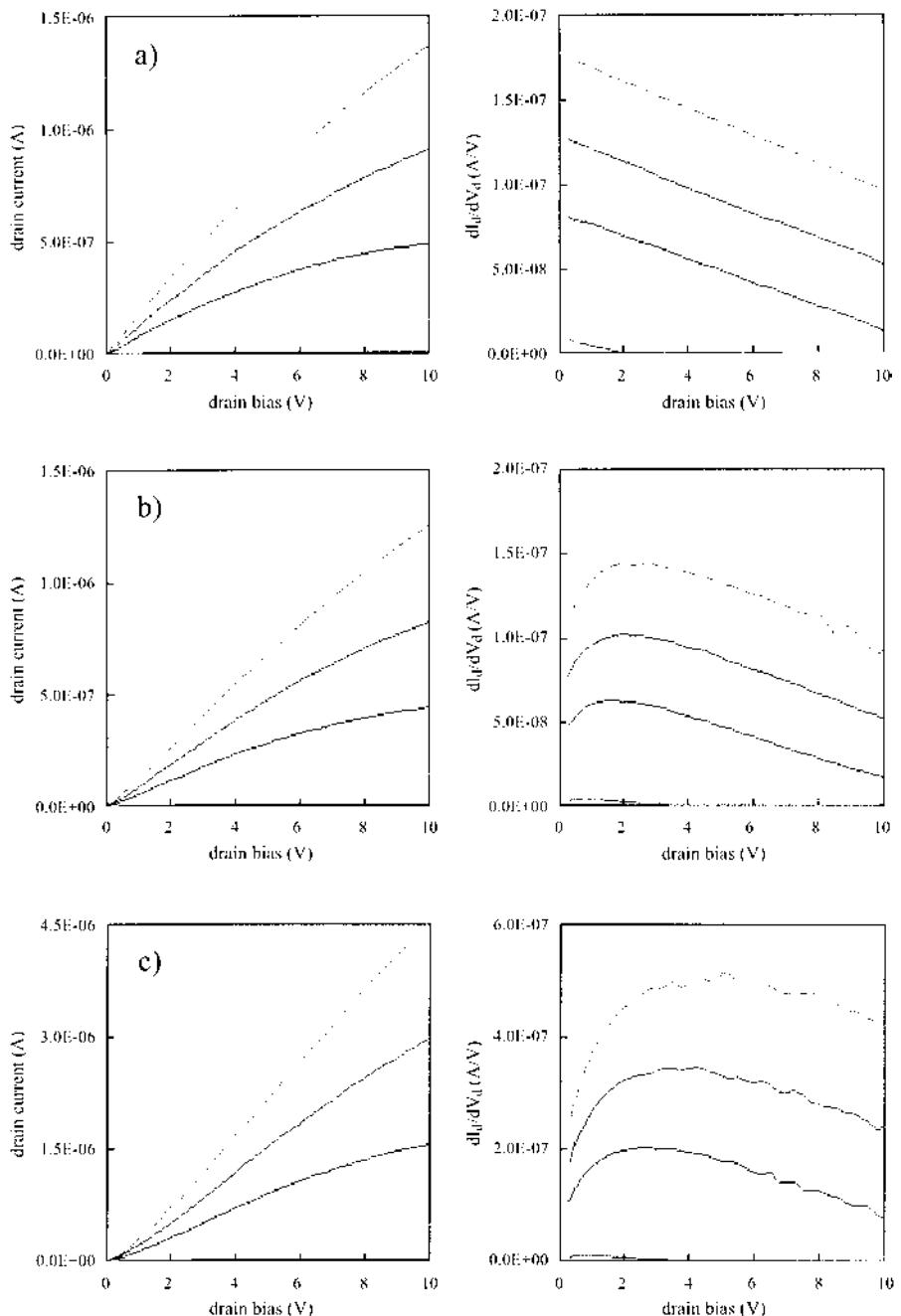
Operating environment	Environment range	Display design consideration
Dark to direct-sunlight readable	8,000–10,000 fC	Black matrix, low pixel off-current to handle 350–850 cdm/m ² , CR > 2:1
Residual image	Static screen	TFT temperature dependence, stability
Large operating temperature range	~−40–70°C	require lower levels of I_{off}
Large storage temperature range	~−50–85°C	
Electromagnetic compatibility (EMC)	~[0.4–1000 MHz]	May require additional ITO ground plane to ensure Narrowband(max) ~ 15–35 dBu-V/m Broadband(max) ~ 28–48 dBu-V/m
Humidity requirements	100% RH, possibly salt air	
Color performance	SMPTE 170–1994 coordinates	
Grayscale	6–8 bits/subpixel	
Viewing cone	~160 degrees	
Contrast ratio	~300–400	
Video response	30 Hz refresh rate	
Lifetime	~ 10K–20K hours	

shows an increase in I_{ds} of only $3\times$ despite the $11\times$ increase in W/L ratio. The effective linear parameters extracted for the short-channel TFT were $\mu = 0.12 \text{ cm}^2/\text{V}\cdot\text{s}$ and $V_t = 0.0 \text{ V}$. The loss of performance due to contact resistance is apparent not only in the parameters but also in the extreme hooking of the differential plot of [Figure 5.18c](#). Both effects of lowered mobility and extreme hooking (nonlinear behavior) at low V_{ds} need to be taken into account in the pixel-charging simulations.

Pixel charging is easily simulated by recalling the following:

$$Q_p \approx C_{\text{gate}}(V_p - V_{gs}) + C_s(V_p - V'_{gs}) + C_{LC}(V_p - V_{\text{com}}) \quad (5.39)$$

$$I_{ds} = \frac{dQ_p}{dt} \quad (5.40)$$



where Q_p is the charge on the pixel, V_{com} is the common voltage on the top plate forming the top LC electrode, and V'_{gs} is the adjacent neighboring gate line. Assuming no change in total pixel capacitance over the charging time, we have

$$\int_0^t dt = C_p \int_{V_i}^{V_f} \frac{dV_p}{I_{ds}} \quad (5.41)$$

The integral on the right-hand side may be numerically solved, provided the operational I - V characteristics of the TFT (biased as it would be in the actual AMLCD) are known, either by direct measurement or by extraction from calculated output characteristics, which include the current-crowding-effect model, such as the earlier model.

For example, for a 13.3" XGA, AMLCD TNNW LC 6-bit gray-level design, typical values of $C_p = 400 \text{ pF}$, $V_G = 24 \text{ V}$, $2V \leq V_d \leq 12 \text{ V}$, $V_{\text{com}} \approx 7 \text{ V}$ (ΔV_{com} assumed 0 V for this example) were used in the following measurements and simulations [22]. The operational curves are merely the loci of I_{ds} (V_{gs} , V_{ds}) points for a particular set of bias conditions. For the purpose of numerical integration consistent with Eq. (5.41), the voltage axis has been reversed (since $V_p = V_D - V_{ds}$) and experimental curves have been fitted to better than $R^2 = 0.9999$ using a cubic polynomial regression. The analytical function was then used to generate steps of decreasing size over which numerical integration could be achieved with the required precision.

Results of the pixel-charging simulations are shown in Figures 5.19 and 5.20 for a long-channel and a short-channel TFT, respectively. Table 5.5 summarizes the results for pixel charge levels to 95% and 9.2%, as well as the % charge written to the pixel in 21.7 μs , which represents the maximum possible XGA scan-line time. The 99.2% level represents approximately 1 linear bit (78 mV) of the available 5-V liquid crystal technology switching data polarity for midgray ($V_p \approx V_{\text{com}} \pm 2.5 \text{ V}$), or a pixel-charging rate of approximately five time constants, which must be met to make full use of 6 bits.

It is useful to consider the results of Figure 5.19, since a device with $W/L = 1$ serves as a useful starting point for a-Si TFT design. Consider first the ideal linear device with $\mu = 0.42 \text{ cm}^2/\text{V}\cdot\text{s}$ and $V_t = 3.0 \text{ V}$. According to our specification that the XGA pixel charge at least to within 78 mV, we see that an increase



FIGURE 5.18 TFT output characteristics ($V_g = 5, 10, 15, 20, 25 \text{ V}$) and corresponding differential conductance data for TFT of (a) long channel length and ideal ($R_s = R_d = 0\Omega$) contacts, (b) long channel length and nonideal ($R_s = R_d \neq 0\Omega$) contacts, and (c) short channel length (reduced mobility) with similar nonideal contacts to (b). (From Ref. 22.)

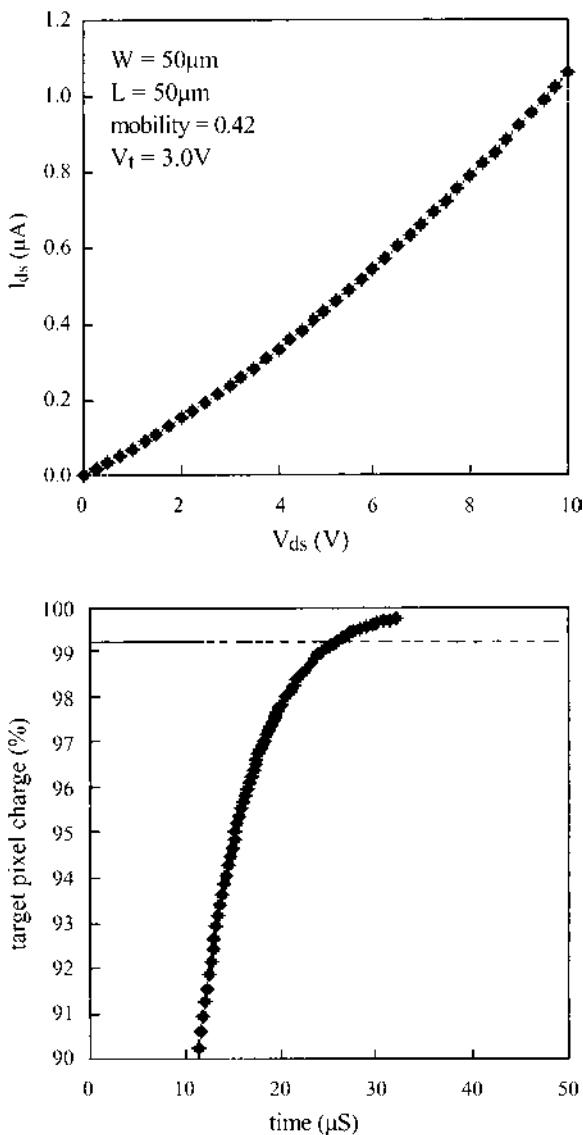


FIGURE 5.19 (a) TFT dynamic output characteristics [$V_g(t = 0\text{ s}) - V_{th} = 21\text{ V}$] and (b) corresponding dynamic pixel charge-up for long channel length with ideal ($R_s = R_d = 0\Omega$) contacts (solid squares) and nonideal ($R_s = R_d = 0\Omega$) contacts (open squares) charging a pixel capacitance of 400 fF . (From Ref. 22.)

TABLE 5.4

Parameter	Value
V_t	2.5 V
μ_0	0.57 cm ² /V-s
V_{GO}	20 V
r	0.15
R_c	0.5 Ω-cm ²
X_0	5 μm
W	1,000 μm
C_i	25 nF/cm ²

in transconductance by roughly 20% is called for, due either to an increase in μ or W or to a decrease in L . Mobility is typically determined by the process technology chosen, and it is not prudent to rely on this parameter in a conservative design. Increasing W also increases the parasitic capacitance C_{gs} while negatively impacting aperture ratio in high-resolution designs, and so a maximum value is typically specified by these design elements. Consider a design where W/L is chosen to be 1.5 so as to meet the charging target and to allow a safety margin, e.g., for a $\pm 20\%$ variance in I_{ds} resulting from a cumulative variance in fabrication-influenced parameters such as μ , W , L , and C_{gs} . In the ideal case this should be sufficient margin. However, if the TFT has even the slight degree of current crowding shown for the actual TFT in [Figure 5.20](#), it will not be sufficient to meet the specification; this would require $W/L = 1.9$ just to meet the target *without* allowing for any loss of device mobility!

Recall that [Figure 5.20](#) shows the effective mobility of the short-channel ($L = 4.5$ μm) TFT just under 30% of its long-channel value. Obviously this is more than offset by the $11\times$ increase in W/L , so a designer might rest assured that there is more than sufficient gate drive, and in the ideal case this would be correct. In fact, width could easily be cut in half to 25 μm and the target could still be met in the ideal case, even if the mobility should fall to $\mu = 0.10$ cm²/V-s! Note, however, that the effect of the contacts in this case is much more severe; for the actual $W = 50$ μm device it takes over *twice* as long to reach the 99.2% target ([Table 5.5](#); 16.6 μs versus 7.4 μs). This is a result of the nonlinear I_{ds} vs. V_{gs} at low V_{ds} bias brought about by highly nonlinear contacts. Failure to include the effects of the source and drain resistance, and proceeding with plans of scaling the device width to half, as described earlier, would result in substantial pixel charge-up error. The result for the cell would be an asymmetric drive where the target pixel voltage is met for the negative cycle but not for the positive cycle.

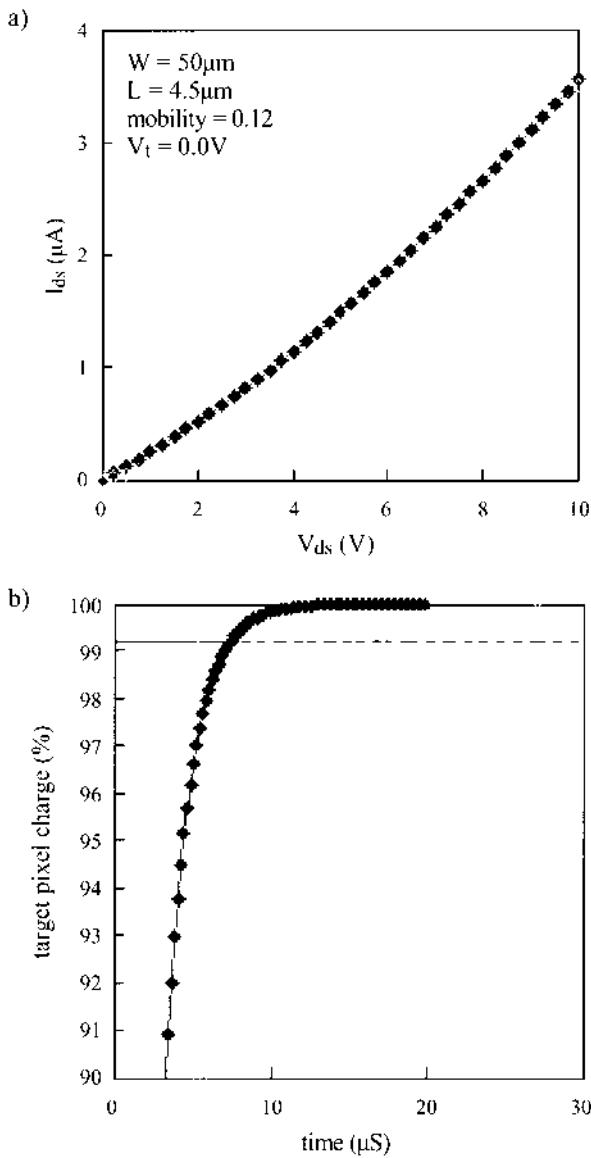


FIGURE 5.20 (a) TFT dynamic output characteristics [V_g ($t = 0$ sec) = V_{th} = 24 V] and (b) corresponding dynamic pixel charge-up for short channel length (reduced mobility) with ideal ($R_s = R_d = 0\Omega$) contacts (solid squares) and nonideal ($R_s = R_d \neq 0$) contacts (open squares) charging a pixel capacitance of 400 fF. (From Ref. 23.)

TABLE 5.5

TFT/cell parameter	Ideal $R_s = R_d = 0 \Omega$	Actual $R_s = R_d \neq 0 \Omega$	Ideal $R_s = R_d = 0 \Omega$	Actual $R_s = R_d \neq 0 \Omega$
W/L	50/50	50/50	50/4.5	50/4.5
Linear mobility	0.42 cm ² /V-s	0.42 cm ² /V-s	0.12 cm ² /V-s	0.12 cm ² /V-s
V_t	3.0 V	3.0 V	0 V	0 V
Time to reach 95% pixel charge	15.2 μ s	21.7 μ s	4.4 μ s	8.2 μ s
Time to reach 99.2% (6 linear bits)	25.8 μ s	40.8 μ s	7.4 μ s	16.6 μ s
Pixel charge reached in 21.7 μ s (XGA line time)	98.4%	95.0%	100.0%	99.7%

5.1.1.4 Pixel Voltage Error Due to Parasitic Capacitance of the TFT and Active-Matrix Structure

The TFT in the pixel operates as an analog switch, whereby, when the gate of the TFT is turned on, it is desired that the TFT accurately transfer a precise data-line video voltage to either a MIM or MOS capacitor, in parallel with the TNLC pixel capacitor. The available precision of charging up the total pixel capacitance to the data-line video voltage depends on many factors, most of which are physical dimensions related to the fabrication and layout design process. The parasitic capacitance of a pixel can be divided into two groups: those that are dependent on the TFT (e.g., C_{DS} , C_{DG} , and C_{GS}) and those that are dependent on the active-matrix layout (e.g., C_{PD} , $C_{PD'}$, C_{PG} , and $C_{PG'}$), where the various capacitances have been defined in relation to Eq. (5.16) and are as shown in Figure 5.8. The TFT parasitic capacitances C_{DG} and C_{GS} are determined by the overlap area between the drain and gate electrodes and the source and gate electrodes, respectively. The channel charge also contributes to the TFT capacitance, as shown in Figure 5.21. The example shown is for $W = 11 \mu\text{m}$, $L = 9.5 \mu\text{m}$, $V_t = 3.5 \text{ V}$, $V_{gl} = -5 \text{ V}$, $V_{gh} = 25 \text{ V}$, and $\Delta L = 1.75 \mu\text{m}$. The smaller the L , the larger the percent contribution from contact overlap capacitance. Therefore, the TFT parasitic capacitance is minimized by making the area of the drain, source, and gate electrodes as small as possible or by increasing the insulator film thickness between the electrodes. The active-matrix parasitic capacitance is minimized by

TABLE 5.6 Today's Competing Test Methods

Test method	Optical inspection	Digital image processing	Continuity test	Admittance sensing	Voltage imaging	Electron beam	Charge sensing
<i>Company</i>	KLA Insystems	Dalsa	Tokyo Cathode	Genrad	Photon Dynamics	AKT, Shimadzu	IBM
<i>Measured quantity</i>	Visual pattern anomaly	Visual pattern anomaly	Line conductivity	Transfer admittance	Pixel/line voltage	Line voltage/ pixel charge	Line voltage/ pixel charge
<i>Test coverage</i>	Visible defects only	Visible defects only	Line faults only	Most line and static pixel faults	Most line and pixel faults	All line and pixel faults	All line and pixel faults and pixel parameters
<i>Operational test conditions</i>	No	No	No	No	No	Yes	Yes
<i>Test options:</i>							
Before LC fill	Yes	Yes	Yes	Yes	Yes	Yes	Yes
After LC fill	No	Yes	Yes	Yes	No	No	Yes
FOS test	Not possible	Not possible	Not possible	Not possible	Not possible	Not possible	possible
<i>Number of probe contacts (SXGA)</i>	None	0-5	Up to ~5000	Up to ~5000	3-5	0-2	Up to ~5000 reduced with NGAT
<i>Post fab repair system vectoring</i>	>4 μm if visible	>4 μm if visible	To one line	To one pixel	To one pixel	To one pixel	To one pixel
<i>SXGA test time (~4 Mp) w/o load/unload</i>	2–10 min (5 cm^2/s @ >4 μm)	2–10 min	Possibly <1 min	3–5 min step/repeat	4 min step/repeat	> 2 min (~1 Mp/60s)	< 0.5 min (~2Mp/1.5s)
<i>ESD/EOS protection</i>	Not required	Not required	Resistive or diode pair	Resistive or diode pair	Shorting bar, resistive or diode pair	Shorting bar, resistive or diode pair	Resistive or diode pair

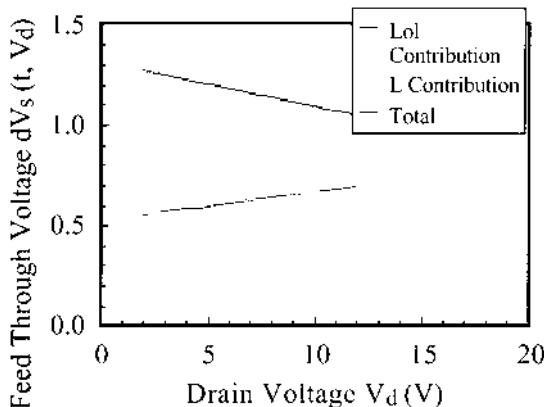


FIGURE 5.21 Pixel feed-through voltage error as a function of drain voltage from the individual component contributions due to (1) the intrinsic TFT channel capacitance, and (2) the parasitic TFT overlap capacitance.

choosing minimum data and scan-line widths and overlaps and maximum spacing between the data line and scan lines and by maximizing the LC thickness or choosing the minimum-LC-dielectric-constant material. Obviously, other constraints may dictate a trade-off. For example, the larger resistive nature of the TFT contacts may require a larger contact area, which increases the parasitic capacitance associated with the TFT, or a desired brighter display may dictate a larger aperture ratio, often achieved by maximizing the LC electrode area through minimizing the use of area elsewhere, such as minimizing the spacing between data lines and scan lines.

A few general points associated with the TFT and pixel parasitic capacitance will be considered here, and points associated with the gate signal delay and distortion will be considered in Section 5.2.1.1. The pixel TFT operation is relatively large signal (for example, during turn-on operation, typically $(dV_d \approx 0 \text{ to } \pm 2V_D(\max), dV_s \approx 0 \text{ to } \mp 2V_D(\max), dV_g \approx 35 \text{ to } 40 \text{ V})$ and intended to operate as a bidirectional switch $[V_d(t = 0) = V_{\text{com}} \pm V_D, V_s(t = 0) = V_{\text{com}} \mp V_D]$) to ensure an rms average for the LC. In other words, when the LCD image (or pixel's gray-level luminance) is not altered, the TFT drain voltage is only larger than the source voltage every other frame at pixel turn-on ($t = 0$). From the equivalent circuit of Figure 5.8, the gate capacitance C_{gs} is of special importance, since the pixel impedance is capacitive ($C_{LC} + C_s + C_{\text{par}}$), and C_{gs} forms a voltage divider of transfer ratio $C_{gs}/(C_{LC} + C_s + C_{\text{par}})$. When the gate bias is on [$V_g = V_g(\max)$], the pixel capacitance minus C_{gs} stores charge $C_p V_d$ and the TFT gate-to-source feed-through capacitance, C_{gs} , stores charge $C_p(V_d -$

$V_g(\max)$). When the gate potential is lowered to turn the TFT off, charge is conserved and shared with the total pixel capacitance. The gate-switching feed-through effect from the drop of the gate voltage, $V_{gs}(\max)$, results in a DC voltage drop across the liquid crystal capacitance, V_{LC} , given by

$$\begin{aligned} V_{LC} &= - \left(\frac{C_{gs}[V_D - V_{gs}(\max)] + \frac{C_p[V_D]}{C_{gs}}}{C_{LC}(V_D) + C_s + C_{par}(V_D)} \right) \\ &= V_D - \left(\frac{C_{gs}V_{gs}(\max)}{C_{LC}(V_D) + C_s + C_{par}(V_D)} \right) \end{aligned} \quad (5.42)$$

and

$$\Delta V_{LC} = \frac{C_{gs}V_{gs}(\max)}{C_{LC}(V_D) + C_{par}(V_D)} \quad (5.43)$$

In this expression, all capacitances except C_s are a function of the twisted nematic liquid crystal dielectric constant, which is data-line video signal dependent, so an accurate compensation of ΔV_{LC} is difficult. A compensation pulse introduced from the previous scan line coupled through the voltage divider C_s -on-scan line capacitance can substantially offset the error of Eq. (5.43) if the compensation pulse, V_{comp} , is equal to $V_g(C_{gs}/C_s)$. The parentheses, (V_D) , denote voltages for which the capacitance is a function of the data line voltage, and the brackets, [], denote a multiplicative operation. Note that the storage capacitance is included in the design of the pixel for several reasons, one of which is to reduce the magnitude of the error ΔV_{LC} . Another reason, discussed in more detail in Section 5.1.1.2, is to lessen the percentage of pixel charge loss when leakage currents are present during the TFT off-time. As noted earlier, C_{LC} is a function of the video signal voltage due to the anisotropic dielectric constant of the liquid crystal material. The twisted nematic liquid crystal dielectric constant is lowest ($\epsilon = \epsilon_{\perp}$), and, hence, the liquid crystal capacitance is minimal when in the white mode (lowest voltage across C_{LC}) for a normally white mode display, and is highest ($\epsilon = \epsilon_{\parallel}$) as the voltage across C_{LC} is increased. Typical values are $2\epsilon_{\perp} \approx \epsilon_{\parallel} \sim 8$. As an illustration, the difference in ΔV_{LC} between a white (data-line voltage V_{d1}) and a black pixel (data-line voltage V_{d2}), for the same polarity, is given by

$$\begin{aligned} d\Delta V_{LC(2-1)} &= (V_{d2} - V_{d1}) - \left(\frac{C_{gs}[V_{gs}(\max)]}{C_{LC}(V_{d2}) + C_s + C_{par}(V_{d2})} \right) \\ &\quad - \left(\frac{C_{gs}[V_{gs}(\max)]}{C_{LC}(V_{d1}) + C_s + C_{par}(V_{d1})} \right) \end{aligned} \quad (5.44)$$

V_{com} , the front-plate common electrode voltage, typically includes the offset by $-|d\Delta V_{LC}|/2$ to minimize flicker, as discussed in the next section.

Properly treated, C_{gs} has two components, the gate-to-source overlap capacitance, producing the displacement currents and resulting voltage divider, discussed earlier, and the gate-to-channel capacitance, resulting in the channel current. The drop in gate voltage by $-\Delta V_{gs}$ and turning the gate off forces the channel charge to drift and/or diffuse to the source and drain contacts. The implications of these two components implies that C_{gs} depends not only on the gate voltage fall time, $\Delta V_{gs}(t)$, producing the capacitive displacement component, but also on the data voltage amplitude, V_d , producing the TFT channel charge. For example, Figure 5.22 shows the measured ΔV_{LC} ($C_{LC} = 0$) as a function of V_d and $\Delta V_{gs}(t)$.

Equation (5.42) can also be calculated by conservation of charge in the TFT. During the gate fall time, a fraction of charge, δ , in the TFT channel, ΔQ , drifts and/or diffuses to the source (pixel) node; the expression can be written as

$$\Delta V_{LC2} = \frac{\Delta Q}{C_{LC}(V_{d2}) + C_s + C_{par}(V_{d2})} = \frac{Q_n W (L + 2 \Delta L)}{\delta([C_{LC}(V_{d2}) + C_s + C_{par}(V_{d2})])} \quad (5.45)$$

where $2 \Delta L$ is the source- and drain-to-gate overlap. δ is typically $1/2$ for the TFT operating in the linear region and $2/3$ for the TFT operating in the saturation region, where the channel charge is nearly voltage independent and is assigned

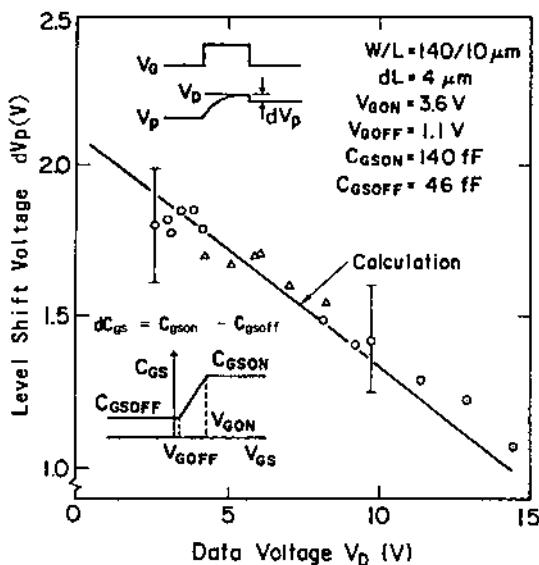


FIGURE 5.22 Pixel feed-through voltage error as a function of gate-line time constant. (From Ref. 92.)

mainly to the source. Substituting $C_{LC} + C_s + C_{par}$ from Eq. (5.15) into Eq. (5.45) and then eliminating $R_{ff(on)}$ with Eq. (5.13) yields

$$\Delta V_{LC2} = \frac{6N_s L(L + 2\Delta L)}{\delta T_f \mu} \quad (5.46)$$

Note that this equation is derived using Eq. (5.13), which assumes that ΔV_{LC1} is determined mainly while the TFT is in the on-state, and therefore Eq. (5.46) involves no dependence on W . This assumption has a greater degree of validity for longer gate-pulse turn-off times, higher-mobility TFTs, and shorter channel lengths, where the TFT channel charge is allowed to decrease while the TFT is still on and the drain and source terminals are still at equipotentials. The equation is useful in demonstrating the important TFT scaling aspects to reducing ΔV_{LC1} , even though compensation pulse coupling for C_s , formed with an electrode from the previous gate line, can substantially decrease the feed-through error associated with C_{gs} . Concerning TFT scaling, the largest reduction in ΔV_{LC2} is accomplished by a reduction in channel length ($\Delta V_{LC2} \propto L^2$), perhaps followed by an improvement in mobility and reduction in the source- and data-to-gate overlaps. Self-aligned TFTs offer an additional benefit in that they result in a more reproducible and uniform ΔV_{LC2} , providing a means to accept larger values of ΔV_{LC2} . Today's a-Si TFT is capable of an inexpensive, high-yield, very uniform four-photolithographic active-matrix fabrication process that produces fully self-aligned source- and drain-to-gate electrodes ($\Delta L \sim 0$), high mobilities ($\mu \sim 1$ V/cm²-s), and small channel lengths ($L \sim 3$ μ m) [23].

5.1.1.5 Flicker

Flicker is an annoying artifact that competes with the intended grayscale luminance data of the image. Human-perceived display flicker is the eye's temporal response to a periodicity change in display luminance, often associated with the display data-refresh period. The perception of flicker by the human visual system is a function of three principal parameters: the observed image, average brightness, and frequency [24]. In general, a normal eye can follow flicker up to approximately 60 Hz. For CRTs, the screens and data-refresh rates are the same and must exceed 60–80 Hz to suppress flicker. For LCDs, flicker is caused by any change in the pixel's grayscale voltage between refresh rates.

The spectrum of any periodic time function $f(t)$ may be calculated by Fourier analysis [25], defined as

$$f(t) = C_0 + \sum_{n=1}^{\infty} A_n \cos(n\omega t) + \sum_{n=1}^{\infty} B_n \sin(n\omega t) \quad (5.47)$$

and

$$A_n = \frac{1}{\pi} \int_0^{2\pi} f(t) \cos(n\omega t) dt \quad (5.48)$$

$$B_n = \frac{1}{\pi} \int_0^{2\pi} f(t) \sin(n\omega t) dt \quad (5.49)$$

$$C_n = \sqrt{A_n^2 + B_n^2} = \text{amplitude of } n^{\text{th}} \text{ harmonic, for } n > 1 \quad (5.50)$$

C_0 is the average voltage on the pixel and $\omega = 2\pi/T_f$.

The asymmetrical pixel pulse train is defined in Figure 5.23, where the assumed exponential pixel voltage decay is small over one frame time

$$\left\{ V_1 \ll V_{p1} \left(\frac{T_f}{2} \right), \quad V_2 \ll V_{p2} \left(\frac{T_f}{2} \right) \right\}$$

and the expansion reduces to a linear decay in time; i.e.,

$$V_{p1}(0) \left[1 - \exp \left(- \frac{T_f}{\tau_1} \right) \right] \approx V_{p1}(0) \left(\frac{T_f}{\tau_1} \right) \quad (5.51)$$

$$V_{p2}(0) \left[1 - \exp \left(- \frac{T_f}{\tau_2} \right) \right] \approx V_{p2}(0) \left(\frac{T_f}{\tau_2} \right) \quad (5.52)$$

The DC component representing the average voltage, C_0 , the first harmonic, C_1 , of period $2T_f$, and the second harmonic, C_2 , of period T_f is found by Fourier analysis using Eqs (5.47) through (5.50) to be

$$C_0 = V_p \left(\frac{T_f}{2} \right) \quad (5.53)$$

$$C_1 = \left(\frac{4}{\pi} \right) \sqrt{\Delta V_{\text{com}}^2 + \frac{(dV_{p1} - dV_{p2})^2}{\pi^2}} \quad (5.54)$$

$$C_2 = \frac{dV_{p1} - dV_{p2}}{\pi} \quad (5.55)$$

where dV_{p1} and dV_{p2} are the voltage parameters representing the pixel-holding

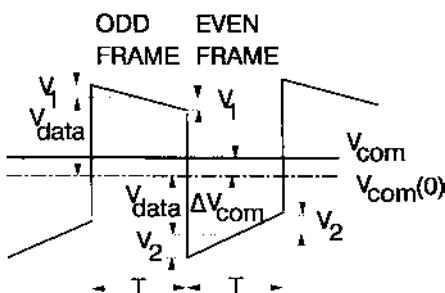


FIGURE 5.23 Asymmetrical exponential pixel pulse train across the liquid crystal cell and corresponding terminology used in determining flicker.

characteristics in the odd and even frames, respectively, $\Delta V_{\text{com}} = V_{\text{com}} - V_{\text{com}}(0)$, V_{com} is the actual counterelectrode voltage and $V_{\text{com}}(0)$ is the ideal counterelectrode voltage when the average pixel voltages in the odd and even frames have the same value

$$\left\{ V_{p1} \left(\frac{T_f}{2} \right) = V_{p2} \left(\frac{T_f}{2} \right) = V_p \left(\frac{T_f}{2} \right) \right\}$$

The amplitude of the higher harmonics in the Fourier series has little of no effect on the perception of flicker, provided the fundamental frequency (first harmonic), C_1 , is greater than approximately 20 Hz, since the second harmonic is then greater than 40 Hz and all other harmonics are above 60 Hz, where the observer has no sensitivity to flicker.

The flicker component (the first harmonic), defined as a percentage of the average DC value, can be expressed as

$$\text{Flicker percent} = \frac{C_1}{C_0} \times 100 \% \quad (5.56)$$

Figure 5.24 plots the flicker percentage against ΔV_{com} .

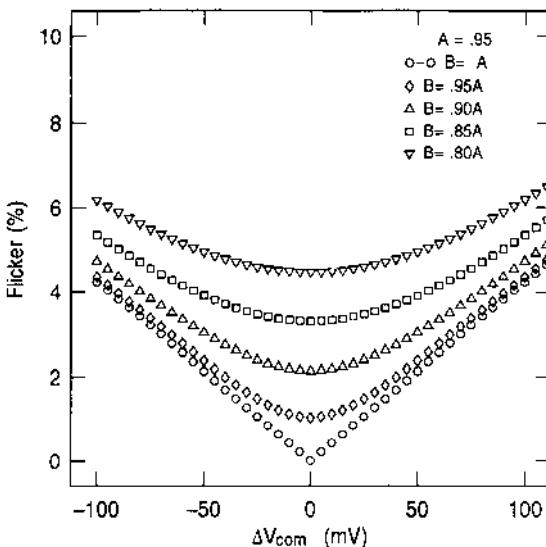


FIGURE 5.24 Flicker component percent versus common voltage offset as a function of the pixel-holding ratio, A/B .

$$A = \frac{V_p (T_f/2) - dV_{p1}}{V_p (T_f/2) + dV_{p1}} \quad \text{and} \quad B = \frac{V_p (T_f/2) - dV_{p2}}{V_p (T_f/2) + dV_{p2}}$$

are the parameters indicating the voltage-holding characteristics for positive-polarity and negative-polarity frames, respectively. The stepped parameter is the voltage amplitude ratio of the top positive-polarity waveform to the bottom negative-polarity waveform, where the parameter is stepped in 5% increments, and the initial value of $A = 0.95$, or is a 5% voltage-holding ratio decay over one frame time. Several insights can be obtained from the plot. First, for a given ΔV_{com} , each additional 5% flicker component translates to approximately an additional 1.5% flicker. Second, for a given voltage-holding ratio, A/B , the minimum flicker is always at $\Delta V_{\text{com}} = 0$. Lastly, if the positive- and negative-polarity frame pixel waveform is not symmetrical ($A \neq B$), flicker will always be present.

Therefore, the smaller the change in the pixel's capacitance, the longer the refresh rate allowed before flicker is detected. Namely, flicker can be reduced or eliminated by maximizing C_s and minimizing the following: the DC offset (ΔV_{com}) during polarity inversion, C_{gs} through a source/drain-to-gate self-aligned TFT, TFT channel length, the TFT and pixel off-current, and scan-line distortion through the incorporation of 3- or 4-step scan-line compensation driving scheme. The data-refresh rates below 30–40 Hz in AMLCDs are possible, but they may then depend solely on the quality of perceived motion necessary for a particular purpose, such as 24 and 30 frames per second, for film projection and video, respectively.

5.1.2 Storage Capacitor Pixel Configurations

There are two dominant pixel configurations used in today's a-Si and p-Si TFT AM TNLC displays, the C_s -over-previous-gate-line and separate C_s line. A typical a-Si process cross section of each photolithographic step is shown in Figures 5.25 through 5.29. The left-hand and right-hand sides show the top view of the C_s -over-previous-gate-line and separate C_s line process steps, respectively. The bottom center shows the side view of cross section A–A', which is a bottom gate staggered inverted a-Si TFT. The process shown consists of the following photolithographic steps; (1) gate metal deposition and process; (2) trilayer (gate insulator, a-Si, back-channel passivation) LPCVD deposition and passivation layer patterning; (3) N+ a-Si LPCVD deposition and patterned down to the gate insulator; (4) ITO deposition and patterning; (5) via patterning outside of array, if required; (6) data metal deposition and patterning, followed by data metal and N+ a-Si etch; and (7) array passivation deposition and patterning, if required. There are several advantages and drawbacks to each. The C_s -over-previous-gate-line can employ C_{gs} compensation driving schemes, does not require separate C_s connection and support electronics, contains fewer crossovers, and leads to a higher aperture-ratio cell. The separate C_s line has less scan-line capacitance and

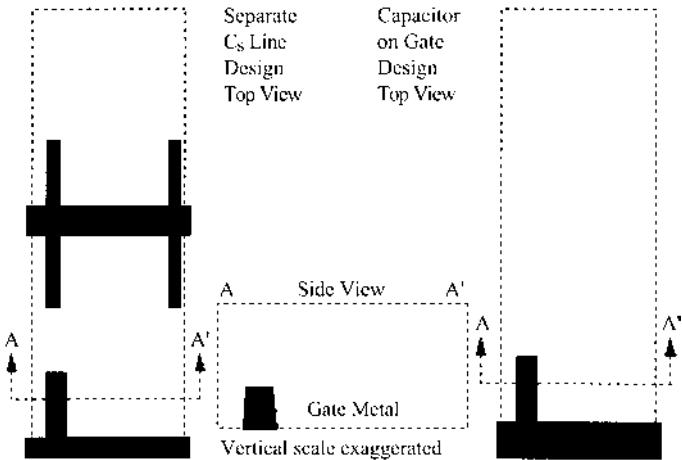


FIGURE 5.25 Trilayer TFT array fabrication step: gate metal deposition by sputtering and patterning.

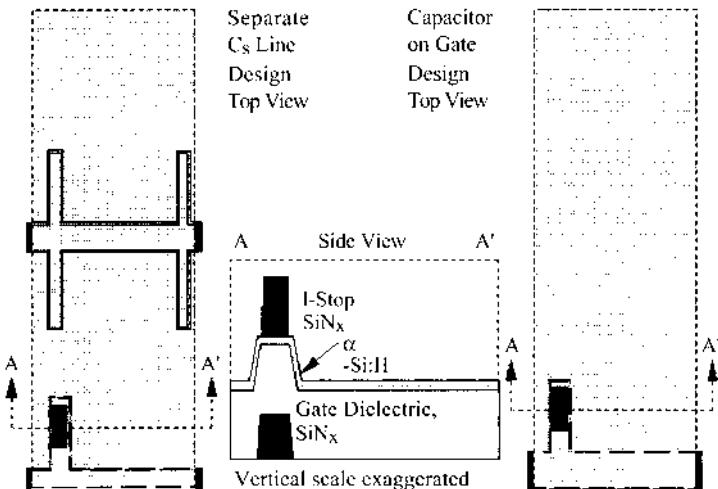


FIGURE 5.26 TFT active-matrix pixel fabrication step: trilayer deposition (SiN_x gate insulator, a-Si, SiN_x I-stop layer) I-stop layer patterning.

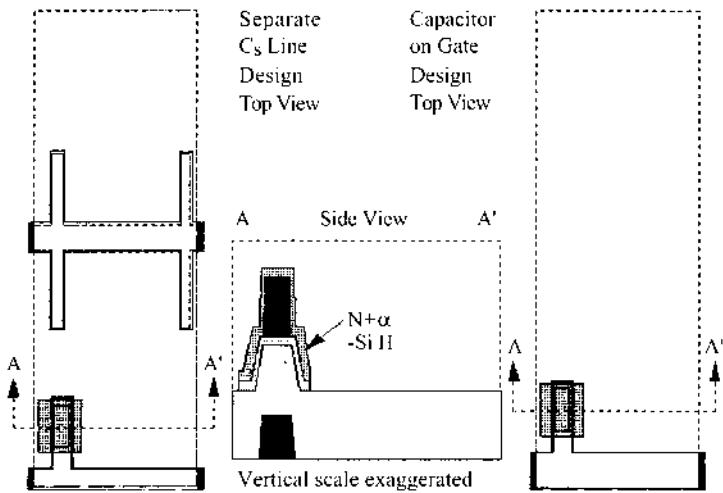


FIGURE 5.27 TFT active-matrix pixel fabrication step: $n +$ a-Si deposition, "island" patterning down to gate insulator.

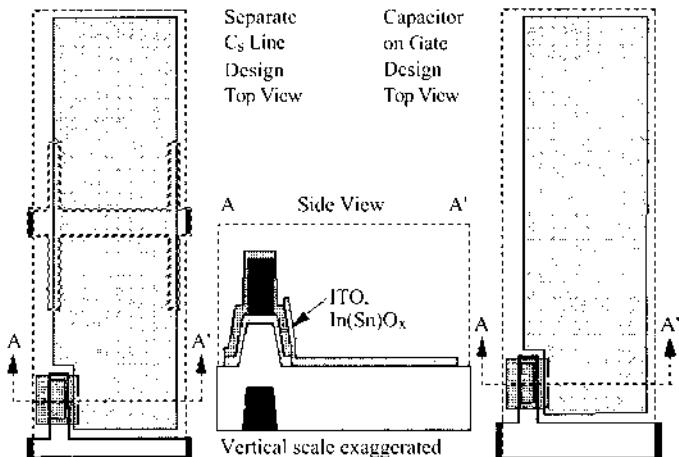


FIGURE 5.28 TFT active-matrix pixel fabrication step: ITO deposition by sputtering and patterning.

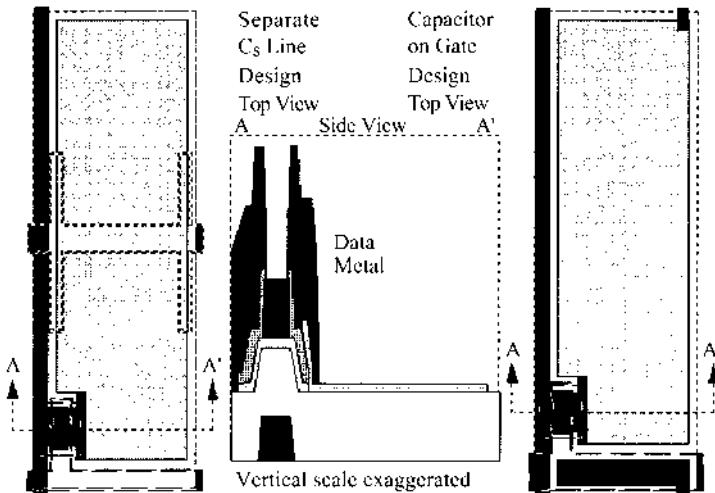


FIGURE 5.29 TFT active-matrix pixel fabrication step: via patterning (outside of array), data bus and TFT *S/D* metal deposition by sputtering, data metal etch, $n +$ a-Si etch. Final step of passivation deposition and patterning not shown.

may incorporate a transparent (ITO) C_s line to minimize the impact on aperture ratio. Today's state-of-the-art a-Si TFT process may employ as few as four photolithographic active-matrix fabrication processes that produce fully self-aligned source- and drain-to-gate electrodes with high mobilities, as is necessary for large and higher-content displays [26,23]. Other LC-dictated pixel designs exist, such as for the in-plane-switching (IPS) LC display that finds use in nonbattery-operated displays, such as monitors, due to the relative wide viewing angle, but higher data-driver voltages, as discussed in a subsequent section.

5.1.3 Electrical Overstress/Electrostatic Discharge (EOS/ESD) Protection

To increase TFT/LC display throughput, the industry has been moving to a larger number of display starts by increasing the glass substrate size while simultaneously decreasing the turnaround fab time through quickened and/or shortened processing steps. However, large-area insulating (glass) substrates traveling at higher velocities between inline processing levels is a direction that decreases electrical overstress/electrostatic discharge (EOS/ESD) immunity, thus making high-yield production challenging. In addition, the quickened in-line testing that

mandates probing of all gate and data pads simultaneously with quick substrate loading and unloading may increase the rate of electrostatic charge transfer to the substrates. Furthermore, TFT LC displays are moving to larger-diagonal and higher-resolution-content displays. The limited pixel-charging capability at shorter scan times necessitates the reduction of scan-line delay through the use of higher conductivity gate-line materials, and reduction of gate and crossover parasitic capacitance through self-aligned TFTs and scaling of ground rules. The reduced RC time constant, i.e., lower impedance, of the scan and video signal lines leads to a greater susceptibility to ESD damage. The purpose of EOS/ESD protective circuitry is to prevent the destruction or degradation of the electrical characteristics of the device from EOS and ESD during the AMLCD fabrication and assembly process. Three basic protective networks have been incorporated in TFT LCDs [27,28], namely, (1) gate line-to-data line low-resistance shorting ring (LLLO) [29], (2) gate line-to-data line high-impedance shorting ring (LLHI) [30], and (3) gate line and data line-to-TFT resistive network-to-low-resistance shorting ring (LLTFT) [31]. The ideal EOS/ESD protective circuitry is completely transparent (this translates into either opens or shorts, depending on the design) for the intended line waveforms, and completely blocking for voltages and charge above normal operating values.

The LLLO network relies on a low-impedance (usually metal) ring shorting together all the scan lines and video signal lines, as shown in [Figure 5.30](#); LLLO provides the best low-impedance path and, hence, a very good ESD protection network independent of ESD pulse width (fast or slow discharge). Also, the substrate is protected early on in the array process after the first metal-level step. One not-so-minor drawback is that the gate line-to-data line shorting ring needs to be removed during or after cell fill process, and the now-unprotected panel must still chart its course through several potential ESD exposures, such as glass substrate size cutting, LC rubbing alignment and electrostatic spacer ball spraying, driver pad cleaning and tabbing, and polarizer attachment.

By contrast, the LLHI does not offer ESD protection as early in the fab process, since the high-impedance shorting ring is not complete until the a-Si:H level, as shown in [Figure 5.31](#). However, for a top-gate TFT poly-Si technology, the LLHI poly-Si-formed shorting ring can offer early array process ESD protection, since the poly-Si level precedes the metal levels [32,33]. Unlike the LLLO network, the LLHI network can remain permanently connected to the data and gate lines, since the impedance is set high enough not to load any attached TFT LCD drivers. Note that the trade-off in a higher-impedance ring will add to the ESD protect network's response time constant and consequently not filter out some of the higher-frequency ESD waveforms. The higher-impedance ring will also act as an unwanted voltage divider, which is problematic when larger-amplitude ESD waveforms are present.

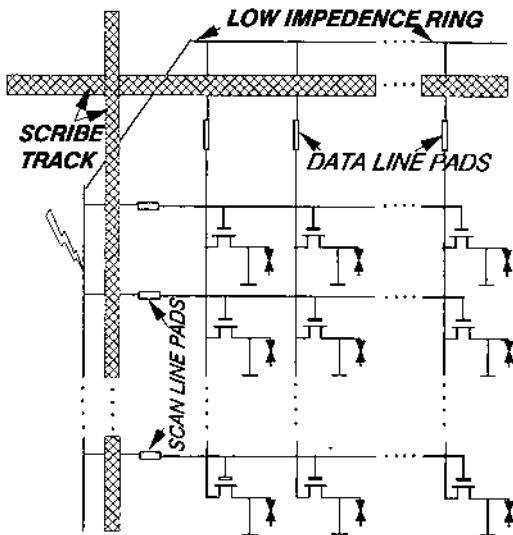


FIGURE 5.30 ESD/EOS protection using a gate line-to-data line low-resistance shorting ring (LLLO).

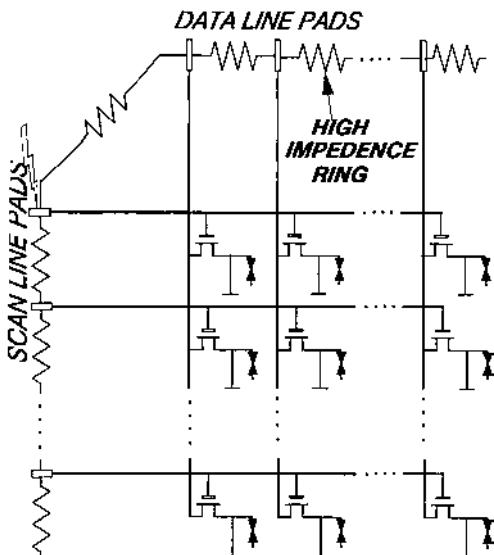


FIGURE 5.31 ESD/EOS protection using a gate line-to-data line high-impedance shorting ring (LLHI).

The LLTFT protect network probably offers the least amount of ESD/EOS protection during array processing, since it relies on the TFT fabrication levels being complete, but the LLTFT protect network is completed before the first array testing of the finished panel, as is shown in Figure 5.32. Like the LLHI protect network, the LLTFT protect network remains intact through module process completion. The LLTFT offers the additional advantage of a dynamic resistance dependence on pulse amplitude; the higher the pulse amplitude, the lower the resistance path in shunting to the ground ring. It is advantageous to have a high dynamic impedance during normal panel operation and a low impedance during ESD events. A TFT response time in the submicrosecond range can be expected, as calculated by the gain-bandwidth product $g_m/2\pi C_{gate}$, where g_m is the TFT transconductance. Simulation based on the voltage diffusion equation [Eq. (5.65)], given in [Figure 5.33](#), calculates the ESD pulse amplitude vs. pixel location distance as a function of time for a VGA display with TFT response time of 150 ns. The ESD pulse was introduced at the edge of the display, labeled “pixel location 0.” Note that ample TFT ESD pulse-shunting ability to the ground ring for times greater than 150 ns is possible but that there is a lack of ESD protection below 150 ns. It is also seen that a relatively high number of pixels

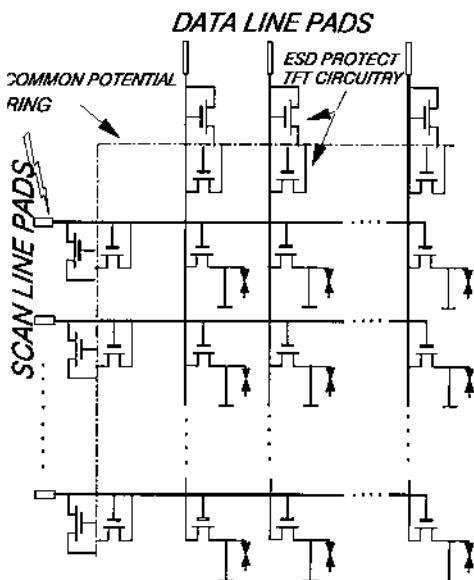


FIGURE 5.32 ESD/EOS protection using a gate line and data line-to-TFT resistive network-to-low-resistance shorting ring (LLTFT).

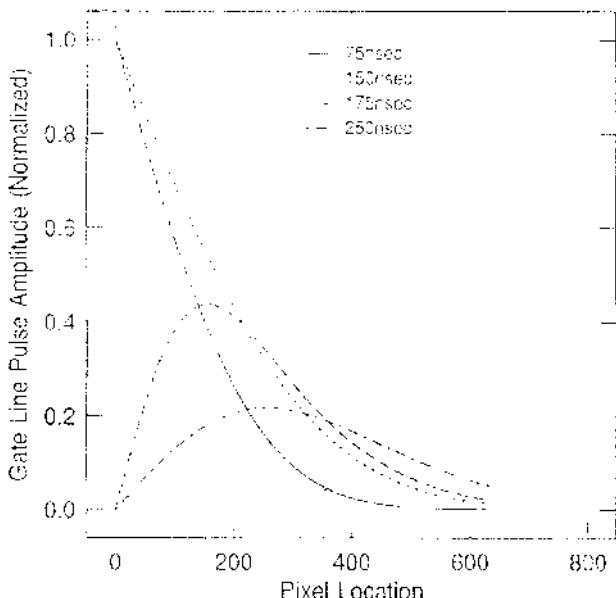


FIGURE 5.33 Simulation of 150-n ESD voltage pulse transient penetration from edge of gate line into array as a function of time. Simulation based on the voltage diffusion equation [Eq. (5.65)] for a VGA display with distributed RC of $50\ \Omega$ and $66\ fF/pixel$. (From Ref. 27.)

(31) will see greater than 90% of the ESD pulse amplitude before the shunting ability of the LLTFT protect network responds. The ESD pulse shape is 99% dissipated within five time constants (750 ns). To make the LLTFT protect network more robust, a short-time-constant discharge network of metal-level needle-like “spark gaps” has been used [27], one or more (for redundancy) placed in parallel with the existing ESD protect TFT in the LLTFT protect network. The single-metal “spark gaps” can be formed during the first metal-level array process step, and thus can offer in-line array process protection. The minimum sparking potential to jump pads $10\ \mu m$ apart is about 350 V but can be lowered through a field enhancement geometry.

The three EOS/ESD protective network attributes just discussed are summarized in Figure 5.34.

5.1.4 Active-Matrix Array Testing

The success (and profits!) of a flat panel product in the market is influenced in two main ways. One is the ramp-up time to market during the development of

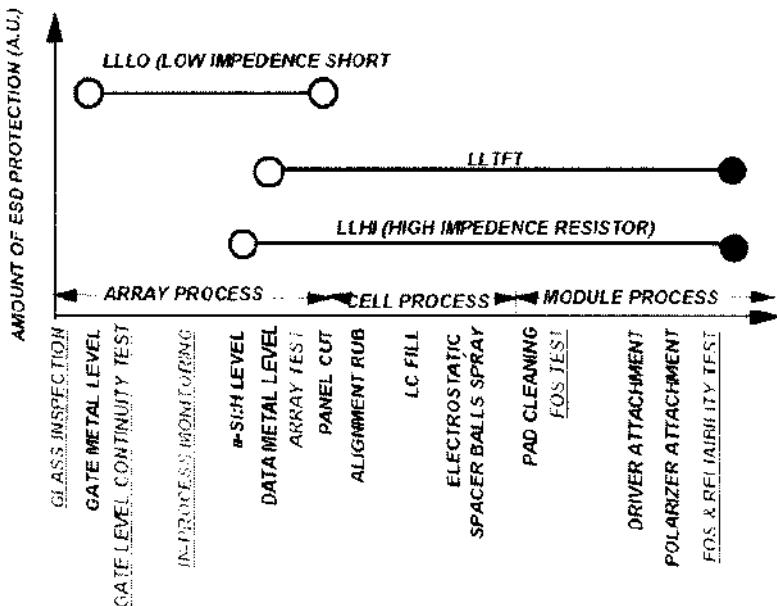


FIGURE 5.34 In-process ESD/EOS protection coverage. Closed circle indicates that the ESD/EOS protection circuit remains in place during AMOLED product operation. (From Ref. 27.)

the panel. The second is the impact of yield improvement in production. Although both phases require testing, the first phase emphasizes detailed analytical and pixel device parameter extraction flexibility while the second phase emphasizes high-throughput screening for defective panels early in the panel fabrication cycle.

While certain aspects of the manufacturing processes for flat panel displays (FPDs) are similar to manufacturing processes for semiconductor devices, materials costs represent a substantially higher percentage of the cost of an FPD as compared to semiconductor devices. As a result, the need for array test and inspection of FPDs goes beyond the need to improve yields as FPD manufacturers also seek to identify defects early in the manufacturing process either to avoid investment in further materials cost or to repair the defect before further manufacturing steps make it less accessible. Therefore, *a test strategy that is emerging in industry is to have a system capable of (1) detailed analytical and pixel device parameter extraction, (2) high-throughput screening for defective panels, and (3) some defect repair.*

Today's competing testing methods are compared in **Table 5.6** [34–36]. The boldface entries are the best of breed for the row attribute listed on the left-

hand side. One requirement for keeping the testing time per display constant or even to decrease it for future larger-image-content and/or higher-spatial-resolution AMLCDs is to have a testing system that can increase the pixels per time tested. This requirement imposes an additional specification for testing systems that also rely on mechanically (not electrically) scanning the display surface. To mechanically scan larger displays while keeping the testing time per display constant requires having a servo mechanism that can increase the velocity (and acceleration) of stage travel with equal or better mechanical stability (and possibly better precision for the higher-spatial-resolution displays).

5.1.4.1 Optical Pattern (Fourier Transform) Inspection

Optical inspection uses an optical system that can immediately see pattern abnormalities without image processing, thus providing quick testing times. The panel-testing throughput is dependent on the resolution selected; higher resolution reduces the maximum single-shot exposure size (cell) as well as decreasing the cell-to-cell scan speed. Furthermore, as with most optically based systems, no probe contacts are required. The substrate under inspection is illuminated with laser light (coherent and collimated). The light incident on the substrate is diffracted and converged via a coherent optical Fourier transformation lens. A spatial filter eliminates the regular pixelated pattern, allowing only nonperiodic particle and pattern defects through the filter, which are captured by a fast analog detector. Defect type classification error rate is one of the highest, due to undetectable electrical defects such as buried interlevel metal crossover shorts (see Table 5.7,

TABLE 5.7 Defect Types

Defect	Defect type description
1	Break in gate line
2	Break in data line
3	Short between data and gate lines
4	Break in shorting bus
5	Short between pad and shorting bus
6	Drain-to-gate short
7	Source-to-gate short
8	Drain-to-source short
9	Short in storage capacitor
10	Poor TFT connection
11	Pixel-electrode-to-gate-line short
12	Pixel-electrode-to-data-line short
13	Short between pixel electrodes
14	Storage capacitor variation
15	Pixel electrode variation

described in upcoming See. 5.15, defect type 3), dielectric pinholes leading to shorts in storage capacitors (defect type 9), and malfunctions in active elements like poor TFT conduction (defect type 10). However, this technique can be applied at various levels before the active matrix is completed.

5.1.4.2 Digital Image Processing

Several manufacturers' testing systems use pattern-recognition and image-processing algorithms to isolate the periodic array pattern from the nonperiodic defects. The image capture is through charge-coupled device (CCD), analog-to-digital converted, and stored for algorithm manipulation. As with the case of optical inspection, testing throughput is dependent on the resolution selected; higher resolution reduces the maximum single-shot exposure size (cell) and increases the number of step and repeats. Defect type classification limitations are similar to the optical inspection technique just discussed.

5.1.4.3 Continuity Test

The simplest (and least expensive) electrical test to perform and interpret is inter- and intrashorts/continuity testing by measuring the line resistance at two possible steps in the AMLCD process: after the gate line, and after the data-line formation. Intralevel shorts/continuity testing (testing within a process layer) implementation is simple, requiring a set of mechanical probes to be placed either (1) at opposite ends of the gate or data line(s) for continuity testing or (2) on adjacent gate or data line(s) for shorts testing (defect types 1 and 2). Interlevel shorts/continuity testing (testing between layers) requires a set of mechanical probes simultaneously contacting data and gate line(s) for shorts testing (defect type 3). Increased throughput is usually accomplished by connecting all odd gate lines to one common shorting ring, all even gate lines to a second common shorting ring, all odd data lines to a third common shorting ring, and all even data lines to a forth common shorting ring. Note that the common-shorting-ring connection scheme sacrifices individual line identification: No TFT characterization or detection of individual pixel defects is possible (like defect types 5 through 15).

5.1.4.4 Transfer Admittance Sensing

The transfer admittance method contacts all data and gate lines and applies a voltage to the gate lines (and to the C_s line if there is one) and detects currents on the data lines [34]. The system measures the complex admittance, output current divided by input voltage, whose phase components give conductance and capacitance. A DC voltage is also applied to the active gate line to turn the pixel TFTs in that row both on and off, and admittance measurements are made under both conditions. The difference in admittance between the on- and off-states is compared to standards (good pixels in the subarray vicinity) for defect type detec-

tion. However, tight limits from spatially localized pixels must be established for the detection of soft (leakage-induced) defects. The ability to detect these soft faults depends on how small their effect is and on the sensitivity of the system. The latter is limited by noise and possibly can be improved by taking more time (averaging) to make the measurements. This may be insufficient in high-content and/or high-resolution AMLCDs and remains to be shown. If a protective guard ring is present, this method requires the resistance between the test pads and the guard ring to be high enough to allow a large enough DC voltage to turn the pixel TFTs on and measure the output currents without excessive attenuation and noise from the ground ring. This method allows all line and pixel defect type characterization.

5.1.4.5 Voltage Imaging

Voltage-imaging tests make use of the Pockels effect of a crystal (a linear electro-optical effect, or where the induced birefringence of a crystal is proportional to the applied voltage) by scanning the AMLCD surface in close enough proximity ($10\text{ }\mu\text{m}$) to sense the pixel voltages [35]. Obviously, this method cannot be applied after the LC cell assembly, since the pixel voltages are now shielded by the top-plate common-voltage transparent conductor. The pixel voltages originate from relatively few probes (3–5) placed onto shorting rings. The lines are driven at the same time with the same signals impressed between the on- and the off-states (100% modulation). The TFT substrate patterns are compared, to isolate both line and pixel defects. However, next-generation high-resolution panels will contain smaller pixel storage capacitance-to-parasitic capacitance, and the resulting adjacent pixel-coupling effects will be greater. In addition, all the pixels are driven with the same waveform at the same time, adding to the coupling term, with the outcome not yet tested. Furthermore, as display size increases, the electro-optical crystal will need to travel over a larger range, which will negatively impact testing speeds. Care must also be taken to avoid mechanical damage from close-proximity scans and to avoid particles.

5.1.4.6 Electron-Beam Testing

There are two modes of test offered by the electron beam [36]. One uses the electron beam purely as a measurement probe and operates the LCD substrate with external control signals via mechanical contacts to the matrix. The other mode uses no external control signals and uses the electron beam for both, the writing of charge within the array and the probing of the resulting internal signals. Substantial characterization of lines and pixel elements can be accomplished. However, the electron-beam operation requires a high-vacuum test environment, which must be taken into account when considering throughput. In addition, since the signal measurement is accomplished by detection of the kinetic energy of secondary electrons originating from the voltage difference between the pixel

and the detector, passivation layers on the pixel electrode or lines will attenuate the measured signal. For this reason, this measurement cannot be applied after LC cell assembly. A newer version uses several electron beams operating simultaneously but spatially separated, in an attempt to improve testing throughput.

5.1.4.7 Charge Sensing

Voltage waveforms are applied to the gate and data lines to perform the Write (charging of the pixel capacitance to the voltage on the data line), the Hold (charge storage within the pixel for a specified amount of time, such as a frame rate, 1/60 second), and the Read of the pixel charge [37–39]. The test coverage is extensive (all defect types), owing to the fact that each data and gate line is probed. In addition, panels with partially or fully integrated drivers may be tested the same way. However, in this case the gate and signal lines are controlled directly by the integrated drivers, with the flexibility of the array tester controller providing the necessary driver timing waveforms needed by the integrated drivers.

A next-generation array testing (NGAT) method is now available for higher-resolution and higher-content TFT LCDs with a substantially lower-cost probe using fewer probes with larger pitch. The number of probes is reduced by integrating multiplexer-like circuits in the peripheral of the TFT array on a glass substrate. The integrated circuits may consist of a-Si or poly-Si TFTs and bus lines. Figures 5.35 and 5.36 show a circuit schematic and layout diagram, respectively, of a 13.3" XGA a-Si-TFT array and the integrated testing circuit for NGAT. In Figure 5.36, each data (column) and gate (row) line has two TFTs, with one TFT (selector) providing low-impedance connection between probe pad and the data or gate line, and the second TFT (holder) providing low-impedance connection between common off-voltage and the data or gate line. The array tester charge-sensing circuits are attached via probes to the panel probe pads. The sensing circuit can write (W) charge on any individual pixel in the TFT array through the selector TFTs, hold (H) the charge on the pixel for a predetermined length of time during the holder TFT on, and then read (R) the charge from the pixel through the selector TFTs. The multiplexer (selector and holder) TFTs are turned on and off by additional control signals described as V_{mux} in Figure 5.36. The number of probes required is a function of display contents and the multiplexing ratio of the integrated circuit. Figure 5.37 shows the relations for several classes of display contents. The NGAT has the utility for using one compatible probe head for multiple AMLCD products of different designs. In addition, the NGAT can perform multiple panel testing per substrate simultaneously with easy probe contact. Furthermore, multiple line measurements at a given time are possible by multiple addressing of the multiplexing TFTs simultaneously. These potentials are very effective at reducing manufacturing cost and increasing testing throughput. The NGAT has been successfully implemented into a-Si TFT LCD product at various companies' manufacturing sites. And the NGAT has also been

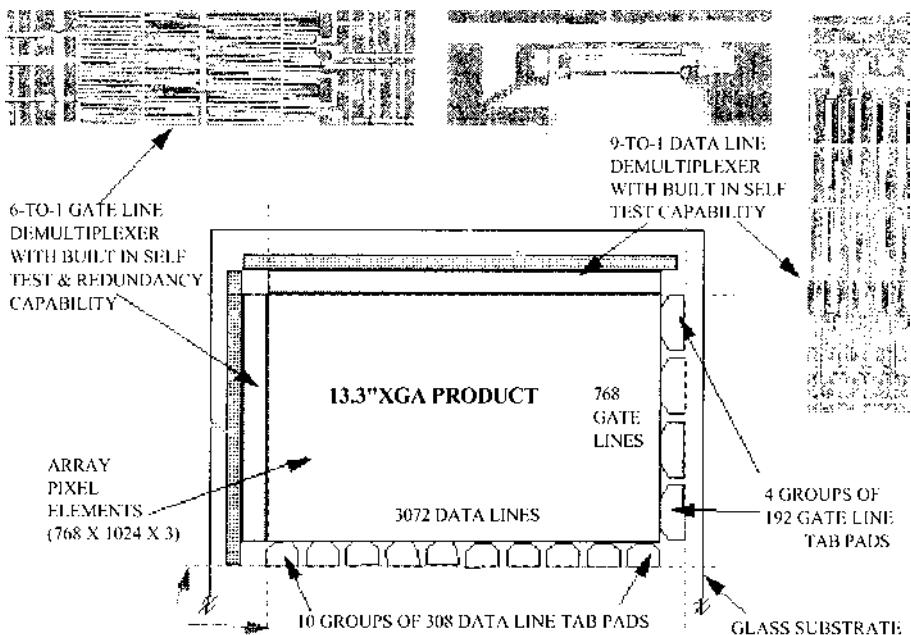


FIGURE 5.35 13.3" XGA TFT-array layout detailing ESD/EOS TFT protection network and the integrated testing circuit for NGAT.

implemented into the highest-resolution (204 ppi), highest-content (QSXGA and QUXGA-W with 5.2M and 9.2M subpixels, respectively) AMLCD to date [40]. A sample defect map and statistics are shown in Figure 5.38. The upper-left chart is the charge pixel map, where the vertical lines represent data-line defects, the black points represent the pixel defects, and the pixel charge value color is coded by the index to the right. The upper-right charge histogram depicts two scans (W/H/R) with a hold time of 5 ms and 16.7 ms, taken to evaluate charge loss versus hold time (2% charge loss), for a 1.48-pC mean pixel charge with standard deviation of 0.06 pC. Pixel charge versus charge time (right) yields a pixel-charging time constant of 1.20 μ s for a 24-V write gate voltage. I_{off} is measured over the range $-5V \leq V_{gs} \leq 1V$. Other pixel parametric tests are possible, such as the pixels' TFT μ and V_T , ESD $I-V$ network characteristics, etc. A defects type chart is in the lower left. This experimental plate is good for evaluating the test system but clearly has too many defects for product use.

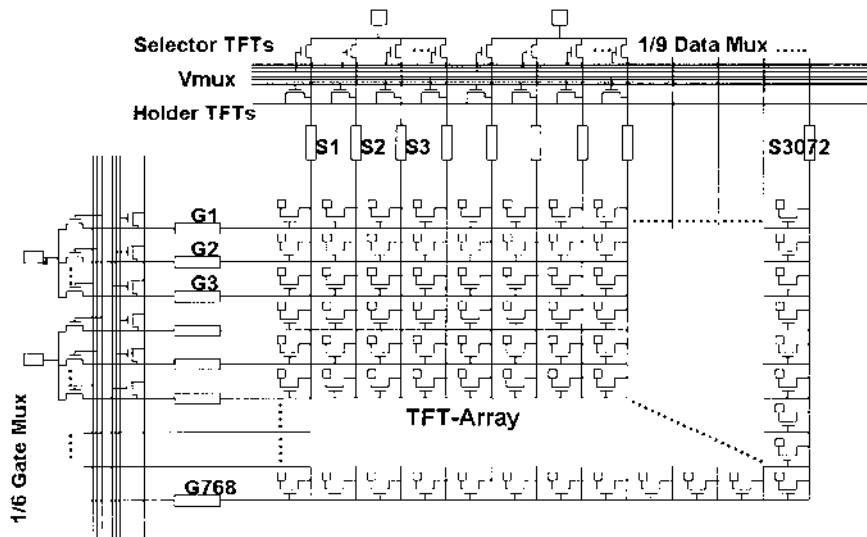


FIGURE 5.36 Circuit diagram of a TFT-array and the integrated circuit on substrate for NGAT. The array tester charge-sensing circuits are attached via probes to the panel probe pads. (From Ref. 37.)

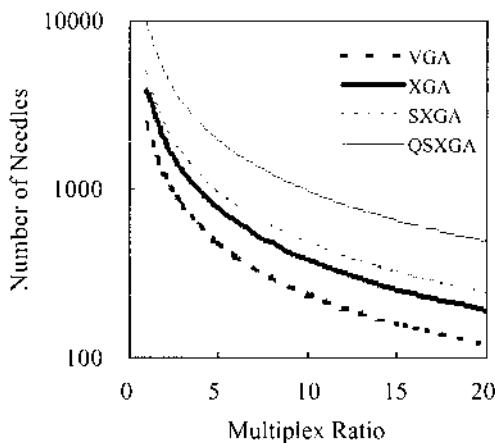


FIGURE 5.37 The number of NGAT probes required is a function of display contents and multiplexing ratio of the integrated circuit. (From Ref. 37.)

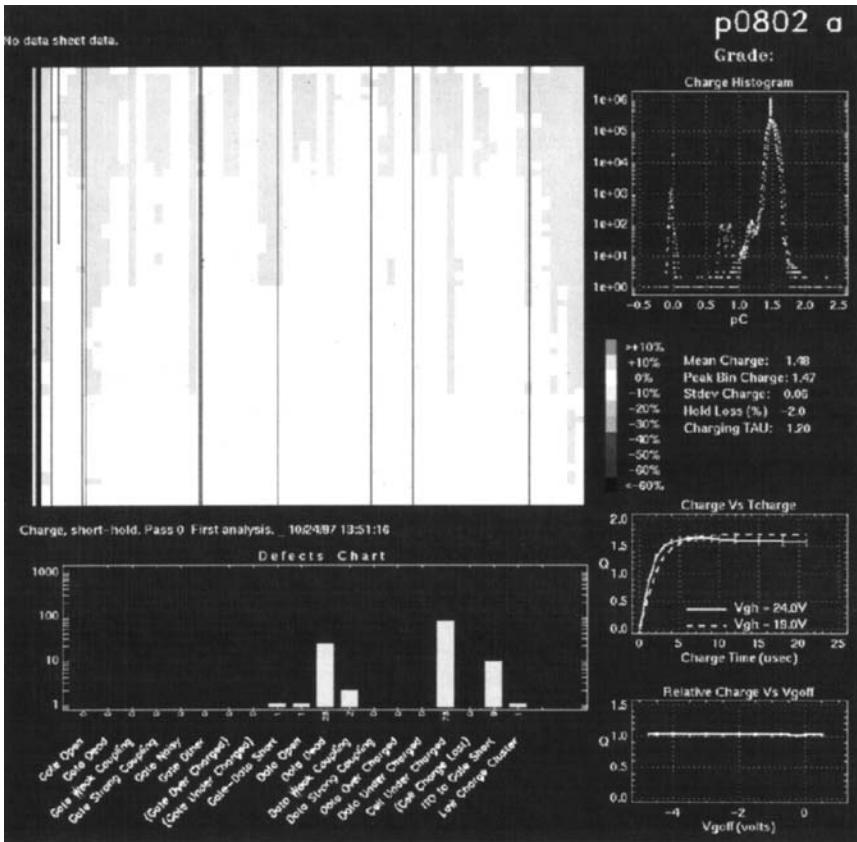


FIGURE 5.38 Sample defect map and statistics obtained using NGAT. (From Ref. 37.)

5.1.5 Good TFT Array Yield

Figure 5.39 shows a schematic of the more common possible AMLCD defects, including line defect types, 1 through 4, and pixel (point) defect types, 5 through 15. These defects are tabulated in Table 5.7. Some possible defects, such as to the top plate, pixel capacitance variation, and various pixel- and TFT-charging variations, are more technology dependent and are omitted.

As previously mentioned, one influence in the success of a flat panel product after initial ramp-up in development is the impact of yield improvement on production. The heart of accurate yield forecasting is the accumulated testing data-

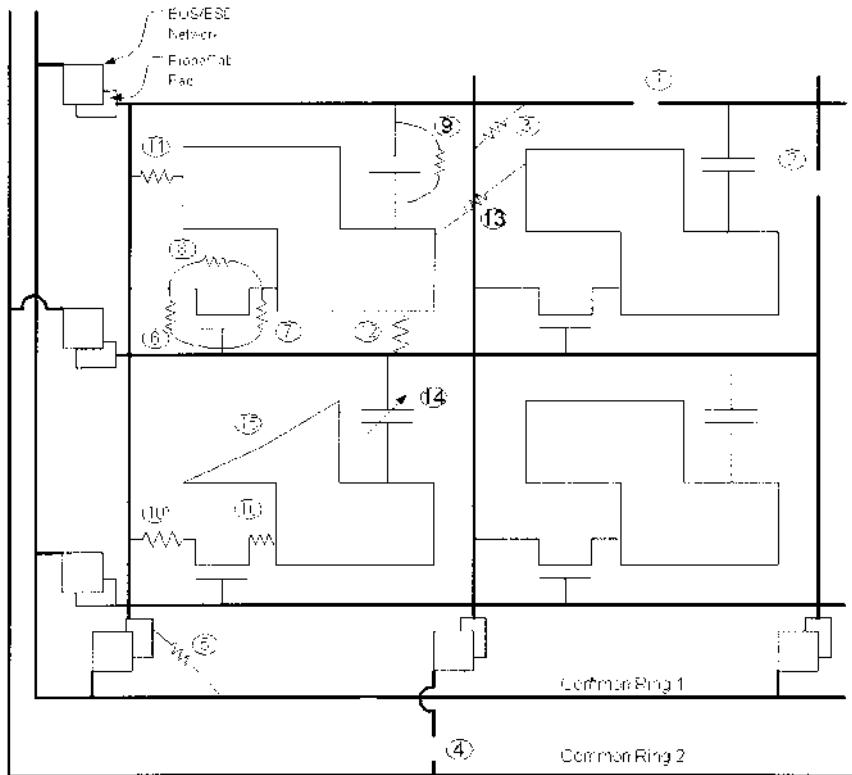


FIGURE 5.39 Possible line and pixel defects corresponding to Table 5.7, superimposed on an electrical schematic of a 2×2 -pixel corner portion for a TFT AMLCD. (From Ref. 37.)

base that contains the individual panel defect list, detailing the types of defects, and the correct correlation to the fabrication step(s) or process parameter variation inducing that defect. For example, a single-cell defect type, like a short between a pixel storage capacitor and the gate line (defect type 9), may be induced by the CVD tool process parameter drift that results in an abnormally large insulator pinhole density. Another single-cell defect type, like a source-to-drain short in the signal metal line (defect type 8), may be induced by a higher-than-normal ambient particle count that prevents photolithographic exposure, develop, and subsequent metal etch for the signal line. Both of these single-cell defect types produce a high-leakage path that prevents transfer of the desired data voltage onto the cell's capacitance, but the correlation to that out-of-spec fabrication

process step that caused the defect is quite different. From such a database, a fault distribution can be developed into a successful-yield model.

Several studies have made an analysis of defects and proposed yield models [41–43]. For example, if one is interested in describing a clean, well-controlled manufacturing process that produces many displays and few faults, i.e., a process where the probability of the fault is very small and assumed equally probable to occur over the entire display for a large sample size, a Poisson fault distribution can be applied [44,45]. Yield forecasts for large-area AMLCDs indicate that, in the absence of repairability, perfect plates will require total fault densities to be less than $0.2/\text{cm}^2$ to qualify a manufacturing line and $0.01/\text{cm}^2$ or lower for substantial yield [44]. This requirement can be relaxed if a small number of random single-cell faults are allowed or some form of redundancy is incorporated. Tolerance to open data and gate lines and to interlevel shorts may require some form of repair and/or redundancy. The probability that a display has exactly y faults, with λ_{fault}^y average number of faults per display, is given by the Poisson distribution:

$$P_{\text{fault}}(y) = \frac{\lambda_{\text{fault}}^y}{y!} \exp(-\lambda_{\text{fault}}) \quad (5.57)$$

In general the probability of simultaneously allowing exactly y_{gl} open gate lines, y_{dl} open data lines, y_{is} interlevel shorts, and y_{sc} single-cell faults is given by $P_g(y_{gl})P_d(y_{dl})P_{is}(y_{is})P_{sc}(y_{sc})$, since these faults are independent events. For example, Table 5.8 shows permissible fault levels for panels that can allow five random gate- and data-line repairs for a specific case of two open gate-line faults. Note that a guaranteed 50% yield with no tolerated single-cell faults ($y_{sc} = 0$) requires that, in addition to the assumed two open gate-line faults ($y_{gl} = 2$), the average data-line open faults must be fewer than six ($y_{dl} \leq 5.6$) and the average interlevel shorts fewer than nine ($y_{is} \leq 8.7$).

The correlation of the panel defect to the fabrication process that induced the defect will dictate the in-line type of test and testing frequency necessary for

TABLE 5.8

Yield	Average faults/display		
	Gate line open	Data line open	Interlevel short
10%	2	9.3	13.5
50%	2	5.6	8.7
90%	2	3	4.9

minimum panel cost. In other words, there is an optimum cost trade-off between scrapping a partially processed defective panel and increasing the panel yield at the expense of longer fab process time per panel that results from the additional testing and repair time.

5.1.5.1 Redundant Structures

There have been various degrees of redundancy efforts, repairable designs, and fault-tolerant designs, ranging from pixel TFT redundancy [46] and data- & gate-line redundancy to peripheral driver redundancy (p-Si) [47]. The TFT redundancy schemes have often been used in conjunction with additional data- and gate-line redundancy, such as dual TFTs per pixel with (1) data and source connected in parallel and driven from different gate lines adjacent to the pixel, or (2) gate and source in parallel and driven from different data lines adjacent to the pixel. The different adjacent gate and data lines just mentioned can involve complete duplication of lines. For completeness, it should be mentioned that redundancy may also involve a dual film, such as a dual metal bus line or partial of full line length stitching through vias contacting another subsequent metal level, or crossover insulator or a simple bilevel (clad) metal bus line [48]. The dual insulator film provides some level of isolation protection, since pin holes in one insulator film have a small probability of alignment with pin holes in the second insulator film. The bilevel metal bus provides more tolerant processing from such exposures as wet- and/or dry-etch-induced line breaks. In addition, bimetal gate lines, which are one of the first lithographical processing steps in the active-matrix process, are often employed as a means of introducing a shallow angle edge profile, a step coverage yield enhancement for subsequent steps.

5.1.5.2 Repairs

Active-matrix repairs can be done with or without redundant structures. Today's a-Si TFT active matrix for high-volume, cost-sensitive displays often do not incorporate redundant pixel TFTs or additional data and gate lines, since not only are typical yields in the upper 90th percentile before repair, but the repair pixel's gray-level luminance quality must also be undetectable by the human visual system. Additional considerations involving the possible defect impact (pixel, cluster, line, or large portion of array) of not incorporating redundancy versus overall panel yield decrease with redundancy for an otherwise-high-yielding process may be best determined by a yield model, as described previously. The most common repair methods employed after fabrication are various types of integrated laser equipment, which can accept defect position vectors from the testing system [49–52]. Unintended metal-line breaks, such as defect types 1, 2, and 4, can be laser-ablated (selective removal of a film layer, for instance, the top passivation layer) and laser-deposited metal reforming a conductive path between the break. The unintended interlevel (crossover) shorts, such as defect type 3, can be laser

cut above and below the short, transforming the short into a break, such as defect type 1 or 2, and repaired, as outlined earlier, by laser metal deposition. Other unintended intralevel shorts, such as defect types 5 and 13, and interlevel shorts 11 and 12, only need electrical isolation and can be remedied through laser cutting. Defects involving the TFT or storage capacitance, such as defect types 6–10, usually are less successfully repaired by laser equipment and will result in a point (pixel) defect. The success of the repaired defect depends in large part on the laser system's capabilities and the product design.

Active line repair (ALR) is an alternative to using laser metal deposition; it provides an electronic means to supply the appropriate data signal to the broken line (defect type 2) and the isolated segment of the data line [53]. However, unlike laser metal deposition, which can be applied only before cell assembly, ALR can be applied during and after cell and module assembly. The intended voltage to the broken segment of the data line is stored in a buffer and retrieved at a later time to be supplied to the broken line segment. The mechanical and electrical connection to the broken line segment can be completed, for example, by laser welding of an appropriate interlevel metal crossover or by ultrasonic ball bonding across two pads: The first metal line or pad is connected at the far end of the data line, and the second metal line or pad is connected to added traces leading back to the extra outputs of the last column driver chip. In addition to data line opens, other line defects, such as crossover shorts (defect type 3) or top-plate shorts, can be repaired with this technique via laser isolation cuts of the data line above and below the defect. And ALR implementation costs are minimal, stemming from the sum of the ALR circuit panel costs (PROM, FIFOs, and controller circuits), costs for the minimum fixed capital equipment (ultrasonic bonder and defect isolation tools), cost to implement ALR, and any additional costs from yield and throughput loss due to plate handling.

5.2 DISPLAY SYSTEM ISSUES

5.2.1 TFT Active-Matrix Driving Schemes

TFT active-matrix driving schemes can serve several purposes: to provide the scan- (gate-) and data-line voltage waveform coordination for (1) turning on the pixels' TFTs and charging the pixel capacitance, and turning off the pixels' TFTs and preserving the pixel capacitance; (2) compensating for various visual artifacts; and (3) providing added performance, such as power reduction. The AMLCD pixels are charged sequentially, one scan line at a time. Scan lines control the opening and closing of the pixels' TFT via a gate pulse, while data lines supply the equivalent grayscale voltages to the pixels to be charged. Almost all commercial notebook and desktop AMLCDs are currently addressed progressively, but different subpixel layout designs are used that affect the addressing scheme. Earlier

designs for lower-resolution TNLC (twisted nematic liquid crystal) displays and today's IPS-LC (in-plane-switching–Liquid Crystal) displays use a separate line in parallel to the rows (gate lines) to form the storage capacitor or, in an IPS cell, the common electrode that is connected in the periphery to a constant potential.

Undesired visual artifacts are manifested when the intended root mean square (rms) grayscale voltage across the LC is altered by the following mechanisms: (1) incomplete pixel-charging current due to such factors as unequal data driver loading, low TFT transconductance, and line waveform distortion and delay; (2) leakage current from the pixel through the TFT or LC; and (3) displacement currents caused by parasitic capacitive coupling of the pixel electrode to both adjacent signal-line voltage changes. Note that mechanism 1 occurs during the scan time of the pixel TFTs' on-state, while mechanisms 2 and 3 occur during the pixel TFTs' off-state. *The interdependent remedies to these three mechanisms are based on material selection and fabrication process conditions, device design and layout, and driving schemes.* Low data-line-to-scan-line-crossover-capacitance layout designs and selection of higher-conductivity metals, such as Al ($\sim 3.5 \mu\Omega\text{-cm}$) and Cu ($\sim 2 \mu\Omega\text{-cm}$) scan lines (mechanism 1), can minimize incomplete pixel charging from line waveform distortion and delay, and will be examined in greater detail in a later section. Likewise, incomplete pixel charging from low-transconductance TFTs can be improved by several means, such as through the use of minimum-channel-length TFTs, process-related mobility improvements, self-aligned TFT designs, and low source and drain ohmic contacts. To alleviate mechanism 2, properly designed and fabricated TFTs with integrated black matrix light shielding can satisfactorily reduce backlight and room ambient photogenerated currents, while ground plane shielding and the use of higher-resistivity LC materials in the range of $10^{12}\text{--}10^{13} \Omega\text{-cm}$ can reduce parasitic leakage currents, where a target total off-current level approaching $10^{-13}\text{--}10^{-14} \text{ A}/\mu\text{m}$ range is desired. Finally, the displacement currents caused by parasitic capacitive coupling are an increasingly troublesome byproduct of scaling to smaller lithographic ground rules, and will also be examined in greater detail in a later section.

5.2.1.1 TFT Active-Matrix Driving Method for Scan-Line RC Delay Compensation

Equation (5.44), with the corresponding section, describes the video-signal-dependent pixel voltage error induced during TFT turn-off. This error is a direct result of the parasitic capacitance, C_{gs} . The other pixel voltage error induced during TFT turn-off described in this section is the one resulting from the distributed and finite RC of the scan line, which introduces a different scan-time pulse delay and distortion for each pixel. Obviously, the larger the display and/or the higher the display pixel content, the larger the scan-line pulse delay and distortion due to a higher RC value for the total, now-longer scan-line length (directly

proportional to L_s , the scan-line length) and/or the shorter scan-line pulse width (inversely proportional to N_s).

Data-line pulse delay and distortion is usually not as important for several reasons. First, the fabrication process for large displays is dominated by a-Si TFT AMLCDs, where the data-line formation is one of the last fabrication steps in the inverted-staggered TFT structure and, as such, presents fewer complications from the use of higher-conductivity metals such as aluminum. For example, the highest-temperature ($\sim 300\text{--}350^\circ\text{C}$) processing associated with the deposition of the gate insulator and a-Si semiconductor is done prior to data-line metal-level processing, so the remaining subsequent lower processing temperatures ($\leq 234200^\circ\text{C}$), hillock formation temperatures ($\geq 325^\circ\text{C}$), associated with Al metal integration is more likely to be avoided. In contrast, scan-line formation is one of the first fabrication steps, prior to the deposition of the gate insulator and a-Si semiconductor. In addition, the scan-line thickness is limited in most technologies ($\leq 3500\text{ \AA}$) to avoid subsequent insulator film- and data-line-to-scan-line step height coverage yield loss from shorts and opens. Second, the capacitance of the data line is typically less than the scan-line capacitance. The data-line capacitance is from each pixel's contribution of the TFT gate-to-data parasitic capacitance, the scan-line-to-data-line crossover capacitance, and the V_{com} -to-data-line crossover capacitance associated with the LC. The scan-line capacitance is not only from each pixel's contribution of the TFT gate-to-drain parasitic capacitance, the scan-line-to-data-line crossover capacitance, and the LC-associated V_{com} -to-scan-line crossover capacitance, but also from the TFT gate-to-source parasitic capacitance, the TFT channel capacitance, and typically the dominant capacitance value, which is from the storage capacitance when the C_s -over-scan-line layout and driving compensation are implemented. Additional data- and/or scan-line capacitance may result from the ITO coupling and, when used, the black matrix overlap. Third, the scan-line length is $\sim 1/3$ or $\sim 2/3$ longer when the typical 4-to-3 or 16-to-10 width-to-height display size format is used. Forth, the data-line video-signal pulse is typically designed wider than the scan-line pulse so that the video-signal pulse precedes and follows the rise and fall of the scan line.

The coupled equations describing voltage and current of the R - and C -dominated differential line model in [Figure 5.40](#) are given by

$$\frac{\partial V_{\text{scan}}(x,t)}{\partial x} = - C_{\text{scan}} \frac{\partial V_{\text{scan}}(x,t)}{\partial t} \quad (5.58)$$

$$\frac{\partial V_{\text{scan}}(x,t)}{\partial x} = - R_{\text{scan}} I_{\text{scan}}(x,t) \quad (5.59)$$

where R_{scan} is the scan-line resistance per unit scan-line length, C_{scan} is the scan-line capacitance per unit scan-line length, and V_{scan} and I_{scan} are the scan-line voltage and capacitance, respectively. Combining these two equations yields the voltage diffusion equation:

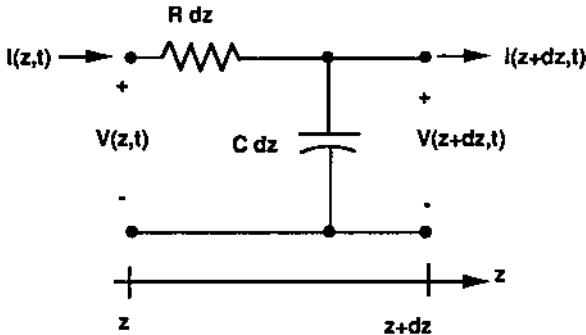


FIGURE 5.40 Electrical schematic of the differential resistance and capacitance line model.

$$\frac{\partial^2 V_{\text{scan}}(x,t)}{\partial x^2} = R_{\text{scan}} C_{\text{scan}} \frac{\partial V_{\text{scan}}(x,t)}{\partial t} \quad (5.60)$$

Laplace transform of the voltage diffusion equation from the time domain in the s domain gives

$$\frac{\partial^2 V_{\text{scan}}(x,s)}{\partial x^2} - sR_{\text{scan}} C_{\text{scan}} V_{\text{scan}}(x,s) = -V_{\text{scan}}(x,0) \quad (5.61)$$

The homogeneous equation has the general solution given by

$$V_{\text{scan}}(x,s) = A(s)_{\text{scan}} \exp\left[-\sqrt{sR_{\text{scan}} C_{\text{scan}}}\right] + B(s)_{\text{scan}} \exp\left[\sqrt{sR_{\text{scan}} C_{\text{scan}}}\right] \quad (5.62)$$

where $A(s)_{\text{scan}}$ and $B(s)_{\text{scan}}$ are constants. Assuming the gate pulse is rectangular and can therefore be represented by the time-domain Heaviside step function, $U(t)$, given by

$$V_{\text{scan}}(0,t) = V_g(0)[U(t) - U(t - t_s)] \quad (5.63)$$

for the case of an infinite RC line ($x \rightarrow \infty$) and where $V_{\text{scan}}(x \rightarrow \infty, t)$ is finite, gives a boundary condition $B(s)_{\text{scan}} = 0$ in Eq. (5.62). With the help of Laplace's second translation theorem, the resulting s-domain function is

$$V_{\text{scan}}(z,t) = \frac{V_g(0)}{s} \left\{ \exp\left[-\sqrt{sR_{\text{scan}} C_{\text{scan}}}\right] - \exp[-t_s s] \exp\left[-\sqrt{sR_{\text{scan}} C_{\text{scan}}} z\right] \right\} \quad (5.64)$$

The inverse Laplace transform, $\mathcal{L}^{-1}\{f(s)\}$ [53], may now be applied to obtain the solution:

$$V_{\text{scan}}(x, t) = V_g(0) \left\{ \operatorname{erf} c \left(\frac{x}{2} \sqrt{\frac{R_{\text{scan}} C_{\text{scan}}}{t}} \right) U(t) - \operatorname{erf} c \left(\frac{x}{2} \sqrt{\frac{R_{\text{scan}} C_{\text{scan}}}{t-t_s}} \right) U(t-t_s) \right\} \quad (5.65)$$

$$R_{\text{scan}} = \frac{\rho_{\text{scan}} L_{\text{scan}}}{W_{\text{scan}}} \quad (5.66)$$

$$C_{\text{scan}} = C_{\text{Ascan}} W_{\text{scan}} L_{\text{scan}} \quad (5.67)$$

$$\tau_{\text{scan}} = \frac{\rho_{\text{scan}} C_{\text{Ascan}}}{L_{\text{scan}}^2} \quad (5.68)$$

$$\frac{x}{2} \sqrt{\frac{R_{\text{scan}} C_{\text{scan}}}{t}} = \frac{x}{2L_{\text{scan}}} \sqrt{\frac{\rho_{\text{scan}} C_{\text{Ascan}}}{t}} = \zeta \quad (5.69)$$

where C_{Ascan} is the scan-line capacitance per unit area, ρ_{scan} is the scan-line sheet resistance, τ_{scan} is the scan-line characteristic time constant, and $\operatorname{erf} c(y)$ is the complementary error function. The scan-line current result corresponding to the scan-line voltage result can be obtained simply by substitution of Eq. (5.65) into Eq. (5.59). To help us interpret the voltage diffusion dependency of Eq. (5.65), we may fix the voltage value of the scan line as

$$V_{\text{scan}}(\zeta) = V_g(0) \operatorname{erf} c(\zeta) \quad (5.70)$$

The rearrangement of Eq. (5.69) yields

$$x = 2L_{\text{scan}} \zeta \sqrt{\frac{t}{\rho_{\text{scan}} C_{\text{Ascan}}}} \quad (5.71)$$

This relates the scan-line pulse movement in space x as time t increases (Fig. 5.41). As can be noted from this equation, the scan-line pulse movement in space x is proportional to the square root of time (hence giving rise to the name *voltage diffusion*). Also, an increase in the gate-line resistivity or gate-line capacitance will hinder pulse movement in space x proportional to the square root of these values.

As a further aid, note that the complementary error function is related to the error function, $\operatorname{erf}(y)$, as follows

$$\operatorname{erfc}(z) = 1 - \operatorname{erf}(z) = 1 - \frac{2}{\sqrt{\pi}} \int_0^z \exp(-y^2) dy \quad (5.72)$$

Values range from

$$\operatorname{erfc}(\infty) = \operatorname{erf}(0) = 0 \quad (5.73)$$

to

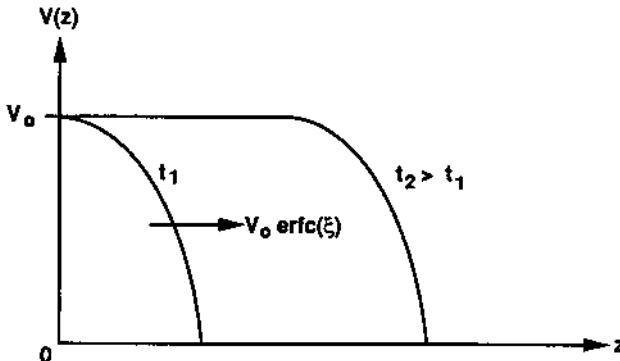


FIGURE 5.41 Voltage diffusion Eq. (5.70) versus line distance as a function of elapsed time.

$$\operatorname{erfc}(0) = \operatorname{erf}(\infty) = 1 \quad (5.74)$$

and the standard normal density distribution, $F(z)$, which is tabulated in many probability tables, is related to the error function by

$$F(z) = \frac{1}{2} \left[1 + \operatorname{erf} \left(\frac{z}{\sqrt{2}} \right) \right] \quad (5.75)$$

[Figure 5.42](#) shows the electrical schematic for (a) the pixel in the upper left most corner of the array, closest to the scan and data drivers, and (b) the pixel in the lower right most corner of the array, furthest from the scan and data drivers. The scan and data lines are modeled as a distributed series resistance and parallel capacitance. [Figure 5.43](#) shows the example of three normalized scan-line pulses calculated by Eq. (5.65) for an SXGA panel with a scan-line time of approximately 16 μ s, with one pulse labeled “Pixel 1,” corresponding to [Figure 5.42a](#) with $R_{\text{scan}} = C_{\text{scan}} = 0$ (no gate-line delay) and the remaining two scan-line pulses labeled “Pixel 1024($\times 3$)”, corresponding to Figure 5.42b. It should be noted that the scan line employing the largest-resistivity metal (“scan metal B”) exhibits the smallest scan pulse height in addition to the largest rise and fall times but that the area under the pulse (integral of the product of scan voltage versus time) is equivalent to the other two pulses, since scan-line charge is conserved, and, as we saw from Eq. (5.65), only delayed in time. Pixels with “scan metal A” and “scan metal B” have resistivity values typical for displays employing Mo and Ta. Allowable scan-line delays are approximately 10% of the scan-line time, where larger delays result in pixel voltage distortion at the end of the scan-line time.

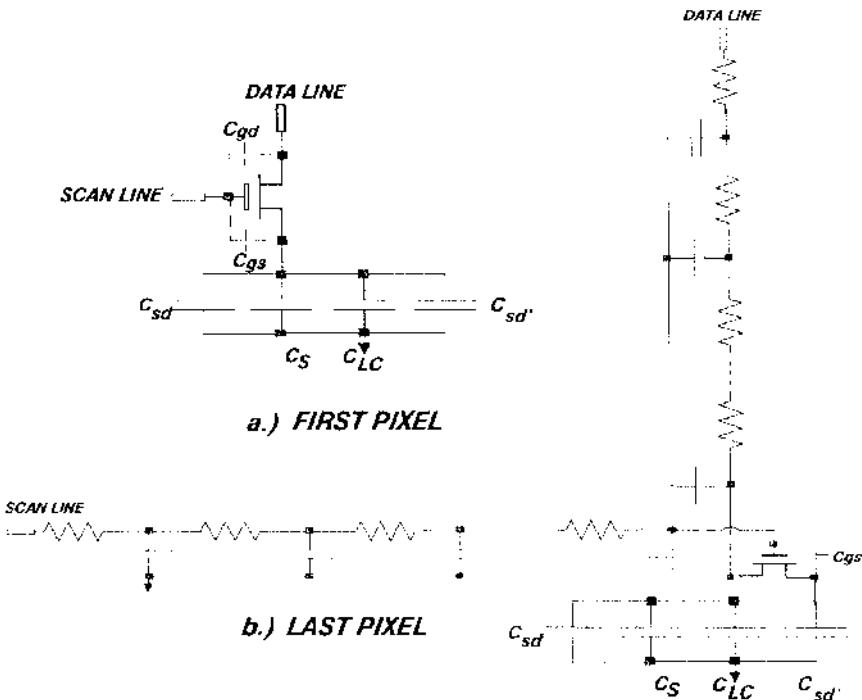


FIGURE 5.42 Equivalent line and pixel circuit model for calculating the two extreme pixel charge-up conditions resulting from minimum (a) and maximum (b) scan-line pulse delay and distortion.

Several solutions help minimize the line delay and distortion: increasing the metal-level conductivity, implementing a gate delay compensation driving scheme, and driving the lines from both ends. Increasing gate-level metal conductivity or driving from both sides lowers the overall scan-line pulse delay and distortion effects, whereas a compensation driving scheme can spatially tailor the compensation pulse to match each pixel's different amount of pulse delay and distortion so as to minimize or eliminate over- or undercompensation, thus avoiding different DC errors in the horizontal direction of the display and leaving the scan-line resistivity unchanged.

The gate metallurgies first introduced were the high-melting-point metals, such as Cr ($\sim 30 \mu\Omega\text{-cm}$), Ta ($\sim 25 \mu\Omega\text{-cm}$), and Mo ($\sim 12 \mu\Omega\text{-cm}$), and bimetals, such as Mo Ta ($\sim 36 \mu\Omega\text{-cm}$) and MoW ($\sim 15 \mu\Omega\text{-cm}$), which are resistant to heat treatment and to processing chemicals from subsequent processing steps that

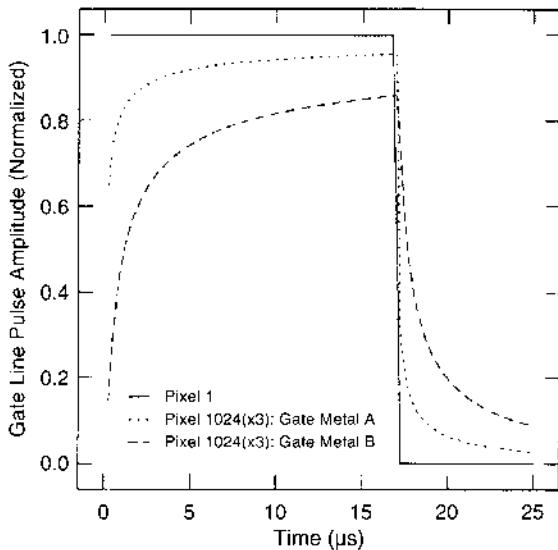


FIGURE 5.43 Normalized scan pulse amplitude versus time showing scan-line pulse delay and distortion for three scan-line metals (ideal, MO, and TA).

have evolved. The initial thermal stability process integration problems of Al metal, such as formation of whiskers and hillocks, have been circumvented by various means, such as anodic oxidation (Al_2O_3) of the Al lines, capping over- and underlayers (Mo/Al, Mo/Al/Mo, Ta/Al, Cr/Al, etc.) or the trace amounts ($\sim 1\text{--}3\%$) of metal impurities (Al-Nd, Al-Zr, Al-Ni, Al-Y, etc. ($\sim 4\text{--}6 \mu\Omega\text{-cm}$)). The cost-sensitive market drove AMLCD manufacturers to integrate the various higher-conductivity Al processes only when electrically necessary. Recently, Cu ($2 \mu\Omega\text{-cm}$) low-temperature reactivity has been solved and Cu metal gate-line displays demonstrated for very high-resolution (157 and 204 ppi) and high-pixel content (SXGA and QSXGA) displays [55].

Driving the scan line from both sides results in a $4\times$ decrease in the RC -line time constant, but this requires an extra kerf area and additional costs associated with twice the number of scan drivers.

The gate delay compensation driving scheme [56] provides the C_{gs} feed-through compensation [error described by Eq. (5.43)] and the DC voltage component due to the anisotropy in the liquid crystal dielectric constant [error described by Eq. (5.44)] compensation. For example, a conventional driven display exhibiting $C_{gs}/C_s = 0.2$, $C_s/C_p = 0.2$, $\Delta V_{LC} = 1.2$ V, and $d\Delta V_{LC}$ shows a DC variation equal to 120 mV and 200 mV for scan-line delays of 5 μs and 10 μs , respectively.

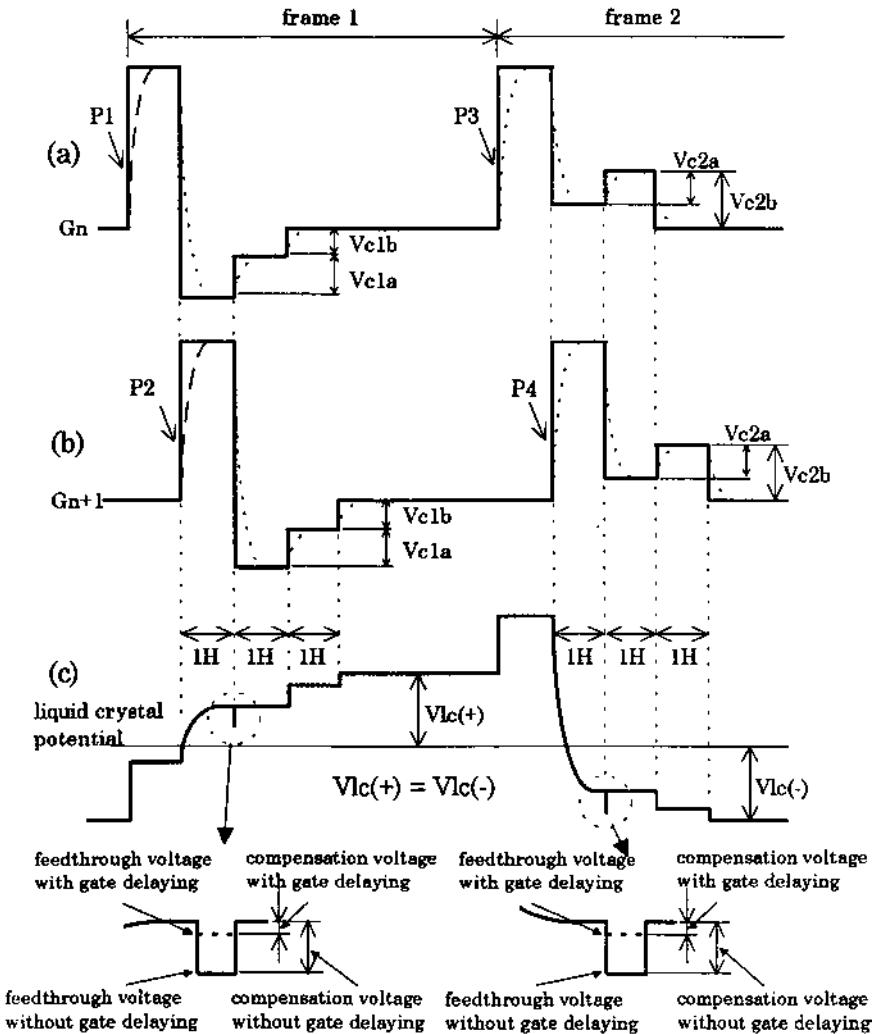


FIGURE 5.44 Gate-line delay compensation driving scheme waveforms for two consecutive scan lines [G_n in (a) and G_{n+1} in (b)] and the corresponding liquid crystal potential, V_{lc} (c). The solid and dashed lines are the waveforms nearest to the supply side and the terminal side of the scan-line driver, respectively, with the corresponding two levels of feed-through voltage and compensation (bottom), and correspond to the two locations shown in the electrical schematic of [FIGURE 5.42](#). (From Ref. 57.)

The gate delay compensation driving scheme is able to suppress the DC variation ($d\Delta V_{LC}$) to approximately 20 mV for scan-line delays of 5 and 10 μ s, a reduction by a factor of 6–10, respectively. Shown in [Figure 5.44](#) is the gate delay compensation driving scheme waveforms for two consecutive scan lines and the corresponding liquid crystal. The solid lines and dashed lines are the waveforms nearest to the supply side and the terminal side of the scan-line driver, respectively, and correspond to the two locations shown in the electrical schematic of [Figure 5.42](#). Recall that $d\Delta V_{LC} = V_{LC}(+) - V_{LC}(-)$, and shown in the figure is $V_{LC}(+) \approx V_{LC}(-)$,

5.2.1.2 TFT Active-Matrix Driving Method for Vertical Crosstalk Compensation

The parasitic coupling capacitance's between the LC pixel electrode and the data lines are the source of the data-line-to-pixel (vertical) crosstalk, whereby information in one row of the display can affect the image in other rows. The parasitic capacitive coupling ratio between the pixel-to-data-line (α) region and the pixel-to-adjacent-data-line (β) region is shown in the layout of a typical pixel of [Figure 5.45](#). From the crosstalk capacitance equivalent circuit of [Figure 5.8](#), α and β can be written as [57]

$$\alpha = \frac{C_{PD}}{C_{LC} + C_S + C_{PG} + C_{PG'} + C_{GS} + C_{PD} + C_{PD'}} \quad (5.76)$$

$$\beta = \frac{C_{PD'}}{C_{LC} + C_S + C_{PG} + C_{PG'} + C_{GS} + C_{PD} C_{PD'}} \quad (5.77)$$

where the capacitances are as have been defined previously in connection with Eqs. (5.15) and (5.16). Note that the data-line-to-pixel-electrode coupling capacitance, C_{PG} and $C_{PG'}$, are not fixed and are a function of the twisted nematic liquid crystal state. The twisted nematic liquid crystal dielectric constant is lowest, and, hence, the liquid crystal capacitance is minimal when, for example, it is in the white mode (lowest voltage across C_{LC}) for the normally white mode display, and in that state the corresponding data-line- and adjacent-data-line-to-pixel-electrode couplings, i.e., α and β , are usually increased. Note also that all capacitances except C_s in Eqs. (5.76) and (5.77) are a function of the twisted nematic liquid crystal dielectric constant and that specific values are needed to calculate whether α and β will increase or decrease.

[Figure 5.46](#) shows the worst-case ($C_{LC\min}$) calculated C_{PG} and $C_{PG'}$ design values illustrating the trade-offs in data-line width/liquid-crystal-cell-gap thickness, W_D/H , and pixel electrode spacing/liquid crystal cell gap, S/H . Further scaling trends toward smaller lithographic ground rules will diminish the data-line width (W_D) and the pixel-to-data-line spacing (S). The calculations assumed the display cross section shown in [Figure 5.47](#), where a conducting ITO plane (com-

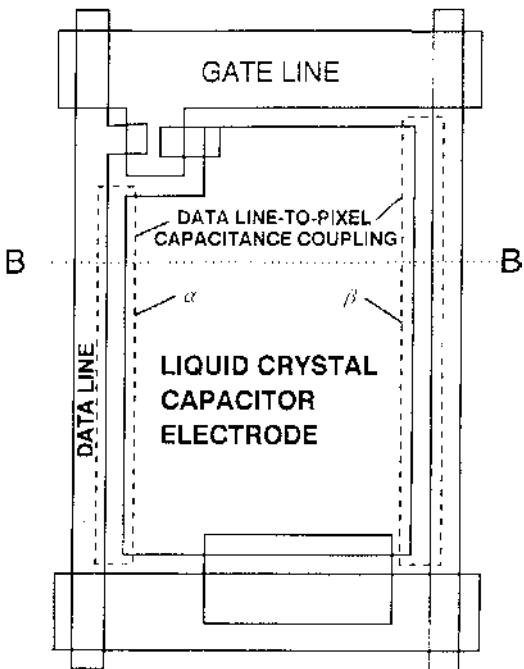


FIGURE 5.45 Top view of a typical pixel layout for a TFT AMLCD, showing the pixel-to-data-line (α) and pixel-to-adjacent-data-line (β) parasitic capacitance coupling regions. (From Ref. 58.)

mon electrode) is assumed to exist a dimension H above the data line and the pixel electrode, and the data line and pixel electrode are treated as coupled microstrip lines separated by dimension S . The anisotropic property of the liquid crystal produces a voltage-dependent dielectric constant, typically giving a corresponding bulk dielectric value ranging between $4\epsilon_0$ and $8\epsilon_0$, where ϵ_0 is the permittivity of vacuum. The values calculated in Figure 5.46 assume a coupled microstrip structure with a film thickness of 100 nm for the data metal and the pixel electrode and a dielectric constant of $4\epsilon_0$ for the liquid crystal and the insulating glass substrate. The coupling capacitance is reduced as the electric constant for the liquid crystal increases relative to the dielectric constant of glass. Thus, the analysis of only the two-lined coupled structure (no field sharing accounted from other conductors) with surrounding dielectrics of equal dielectric constants would yield a good baseline (worst case) for cross talk cancellation design purposes.

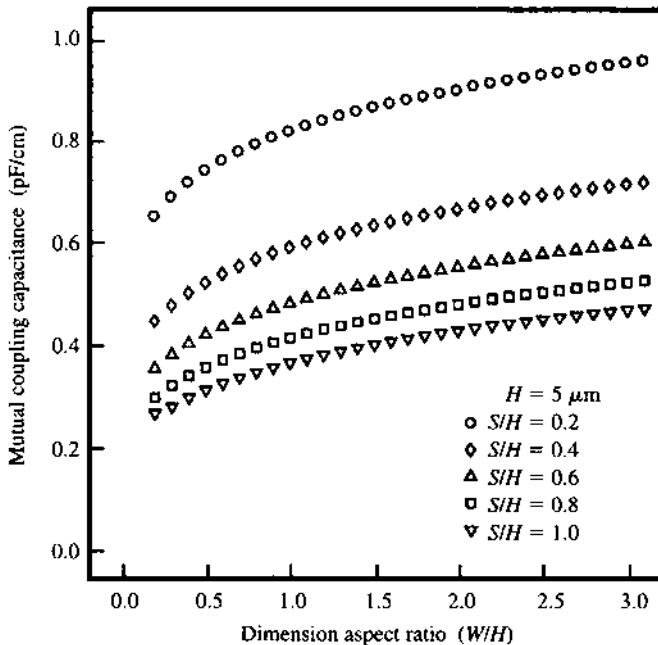


FIGURE 5.46 Asymmetrical microstrip-line model crosstalk capacitance value versus data metal and common electrode dimensions. (From Ref. 59.)

Figure 5.48 shows the calculated parasitic data-lines-to-pixel coupling ratio values from Eqs. (5.76) and (5.77) as a function of pixel width scaling, where $\alpha' = \alpha + \beta$, $W_D = 8 \mu\text{m}$, $H = 5 \mu\text{m}$, a constant aperture ratio of 0.45, and a stripped vertical RGB color pixel arrangement where the pixel length is trice the pixel width. The upper and lower set of 5 curves are calculated with the storage and parasitic gate-line coupling capacitance (C_S , C_{PG} , $C_{PG'}$, C_{GS}) equal to zero and $3C_{LC}$, respectively. In the near future, the trend toward lithographic ground rules will shrink and technology enhancements will probably not keep pace with the desire for pixel width scaling (high-resolution displays), resulting in a decreasing pixel aperture ratio and an even larger coupling coefficient. Therefore Figure 5.48 calculates the most optimistic (smallest) expected α' given the worst case, as previously calculated in Figure 5.46. Clearly the increasing α' with pixel width reduction must be addressed if successful crosstalk elimination is to take place. One approach for minimizing α is to increase C_s . Another approach is to provide ground plane shielding beneath the data line. Both of these approaches require added pixel area, usually at the expense of a smaller aperture ratio. A third ap-

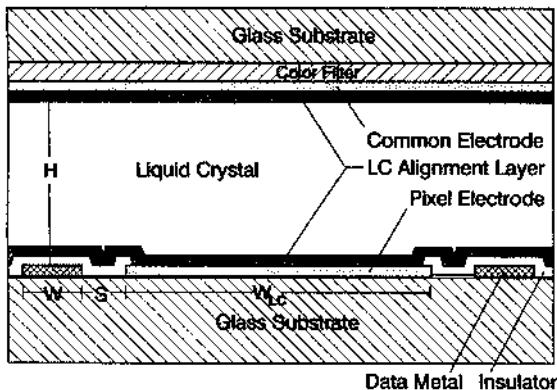


FIGURE 5.47 Cross-sectional view at location B-B' in [FIGURE 5.45](#), detailing the metal lines and electrode dimensions used in the calculation of (α) and (β) for a pixel pitch of $W + 2S + W_{LC}$. (From Ref. 59.)

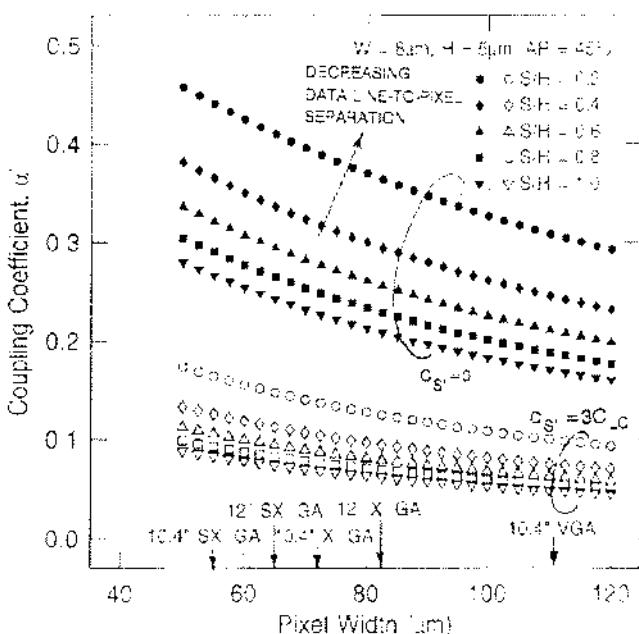


FIGURE 5.48 Crosstalk coupling coefficient versus pixel width as a function of metal lines and common electrode dimensions with two sources of storage capacitance. (From Ref. 59.)

proach, that of providing an appropriate data driving scheme, will leave unaltered the pixel layout and fabrication technology and may provide the least expensive and most straightforward approach to further pixel scaling.

The four conventional driving methods are shown in Figures 5.49 through 5.52, and, unlike the precharge compensation method driving scheme discussed later, they do contain a first-order crosstalk term and are therefore dependent upon the front-of-screen image. All driving methods incorporate data polarity inversion every frame time. Since the relative amounts of crosstalk to a pixel is dependent on the column-line video-signal coupling during one frame, the optimization choosing a driving method for crosstalk cancellation is image dependent. The frame inversion driving method shown in Figure 5.49, involves only one polarity for all signal video data per frame and in general does the least amount of crosstalk cancellation where top-to-bottom variation of the display may be noticed. The scan-line inversion driving method shown in Figure 5.50 alternates the data polarity each scan time and as a result does well with vertical crosstalk cancellation. The column inversion driving method shown in Figure 5.51 alternates the data polarity by column and as a result does well with horizontal crosstalk cancellation. The dot inversion driving method shown in Figure 5.52

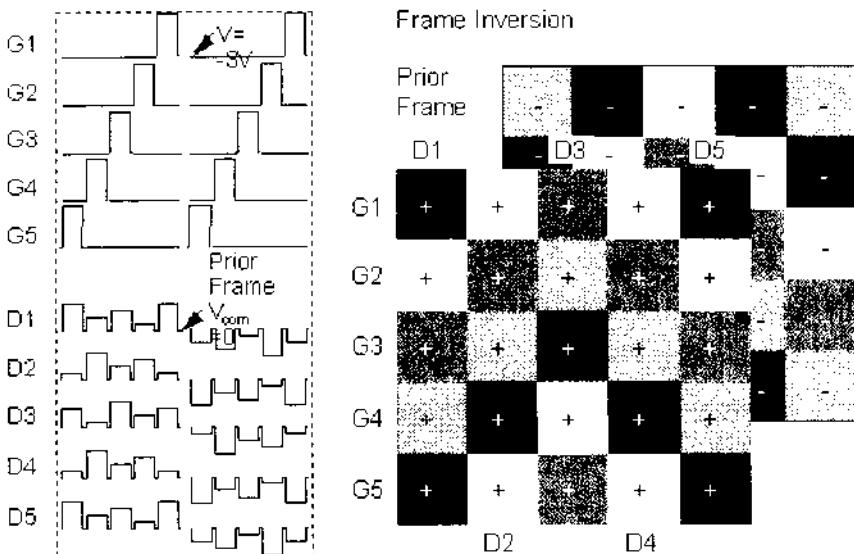


FIGURE 5.49 Frame inversion driving method detailing an example of pulse waveforms for five gate lines and the corresponding data lines (right) with the pixel voltage polarity (+, -) (right), for two frames.

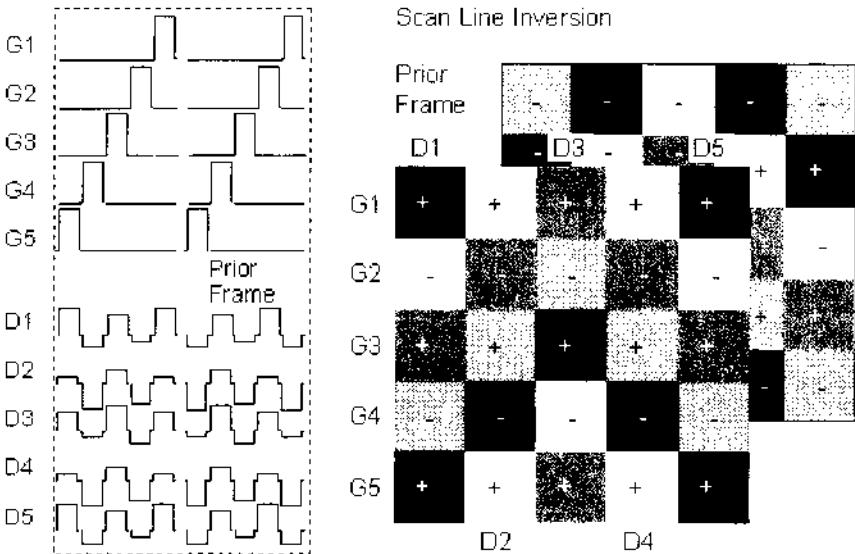


FIGURE 5.50 Scan-line inversion driving method detailing an example of pulse waveforms for five gate lines and the corresponding data lines (right) with the pixel voltage polarity (+, -) (right), for two frames.

alternates the data by both column and scan line and as a result generally does best cancelling both the horizontal and vertical crosstalk. Figure 5.53 shows crosstalk for each driving method, assuming crosstalk is proportional to the left and right neighboring data lines (specific case where $\alpha = \beta$). This specific example shows that column inversion performed the best crosstalk cancellation. Note that for a given scan time, the column and dot driving methods, video signal drivers must supply both polarities of the data voltage, and therefore they will exhibit higher amounts of power consumption. The precharge compensation method (CC) [58] driving scheme shown in Figure 5.54 provides the best crosstalk compensation driving method and consists of one extra data-line precharge pulse of amplitude $\pm V_m \mp V_j$, during the initial part of the scan time, where V_m and V_j is a fixed compensation voltage and the negative of the previous video-signal voltage, respectively [59]. Note that this scheme uses the entire scan line to charge the pixel. Unlike the four conventional driving schemes, the precharge compensation method eliminates the first-order crosstalk term and is not dependent upon the front-of-screen image pattern.

In terms of future panel-scaling directions, for a given active-matrix design and fabrication technology, larger panel sizes translate to less scan-line time,

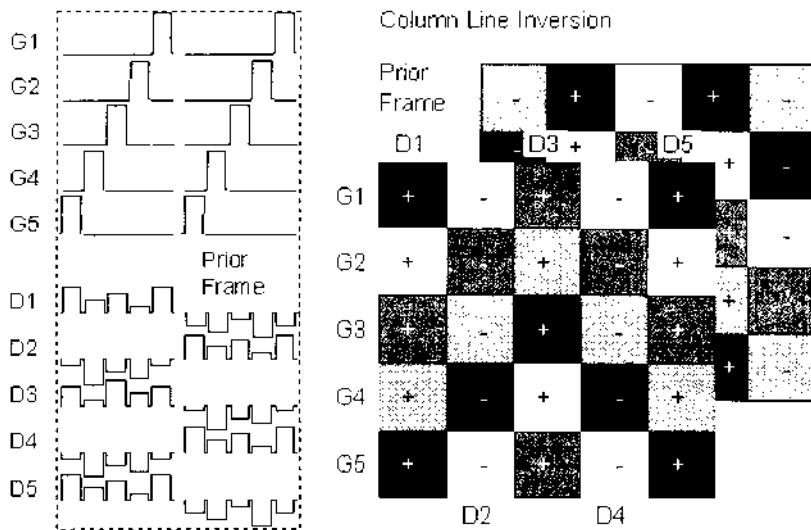


FIGURE 5.51 Column inversion driving method detailing an example of pulse waveforms for five gate lines and the corresponding data lines (right) with the pixel voltage polarity (+, -), for two frames.

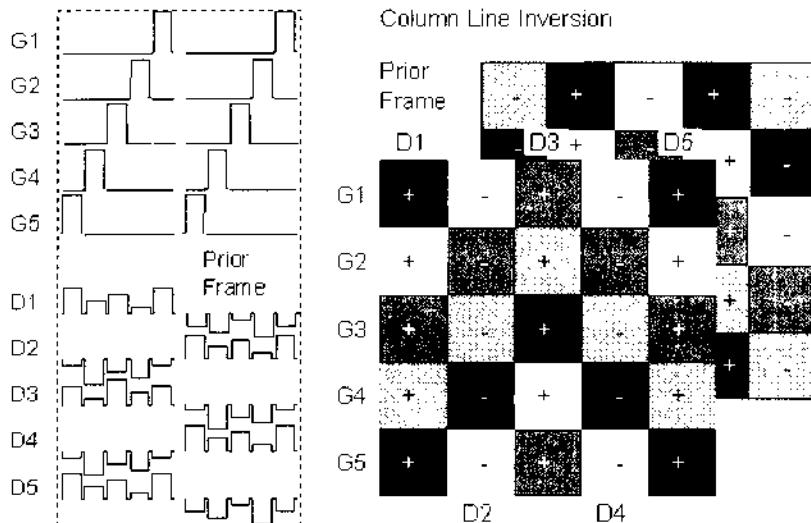


FIGURE 5.52 Dot inversion driving method detailing an example of pulse waveforms for five gate lines and the corresponding data lines (right) with the pixel voltage polarity (+, -), for two frames.

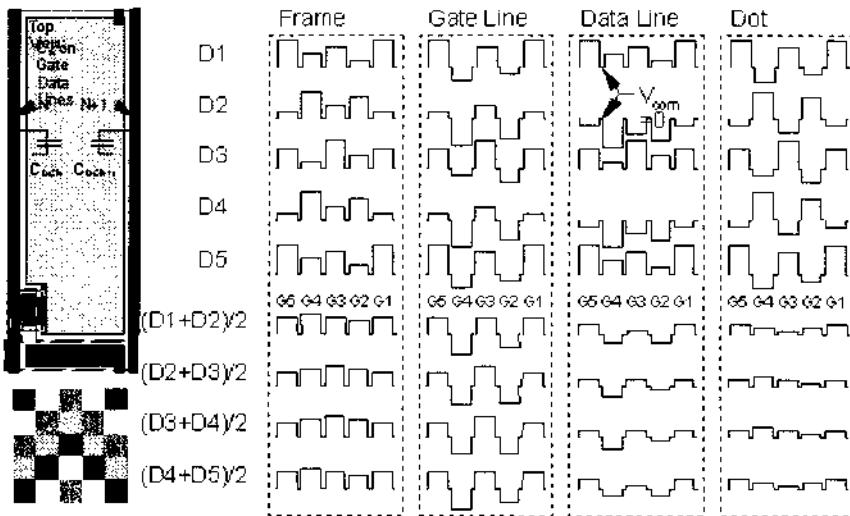


FIGURE 5.53 Frame, scan, column, and dot inversion driving methods showing typical pulse waveforms for five gate lines and data lines and the corresponding crosstalk coupling voltage for the example of $\alpha = \beta$.

resulting in less complete pixel charging due to such factors as additional gate waveform delay and attenuation for a given frame-refresh rate, the higher-pixel-content panels will further shorten pixel charging by diminishing the scan-line time available. For a given TFT active-matrix design and fabrication technology, larger panel sizes translate to larger local common electrode voltage distortions (horizontal crosstalk), an increased viewing angle given a constant screen viewing distance, as well as less complete pixel charging due to such factors as additional gate waveform delay and attenuation. For a higher aperture ratio and also the capability to compensate for the gate-delay-dependent voltage feed-through onto the subpixel electrode [60], the storage capacitor is formed by overlapping with the preceding row (“ C_s -on-gate design”) in TNLC displays [61]. With this design using the compensation driving method, full-color TNLC QSXGA displays at 60-Hz frame rate have been demonstrated [62]; these will be described in further detail in Section 5.3. For low power consumption in notebooks, multifield driving schemes have been developed [63,64] while producing minimum increases in crosstalk.

5.2.2 Display Driver Chips

There are numerous display drivers available to the industry today. The two drivers for TFT AMLCDs are row (scan) and column (signal video) drivers.

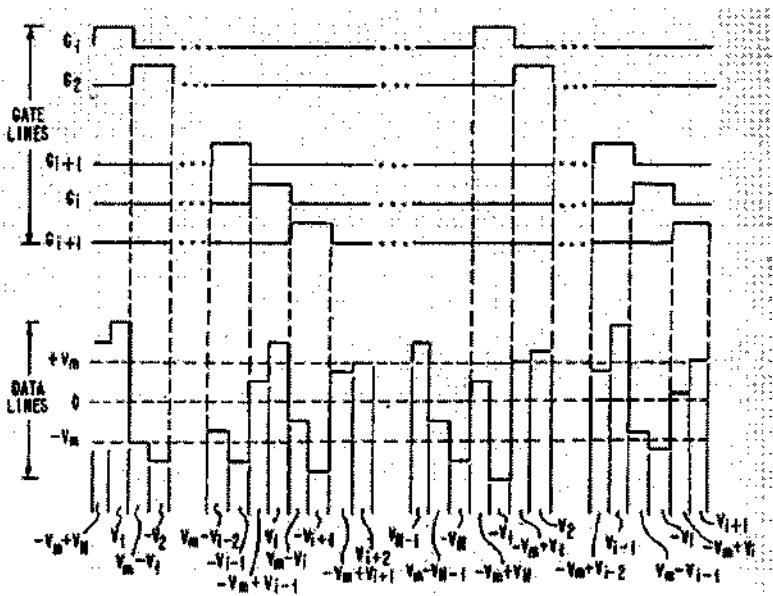


FIGURE 5.54 Precharge compensation driving scheme gate-line and data-line waveforms for the example where the data voltage is alternated for every adjacent row and the pixels are precharged. (From Ref. 59.)

Today's signal video driver chips for AMLCD in notebooks can produce at least 6-bit grayshades within 5-V dynamic output voltage range, have at least 309 outputs on a 65- μm TAB, and do row inversion with front-plane modulation. More grayshades with the same 6-bit drivers can be achieved by dithering and FRC (frame rate control). The 5-V dynamic range places added emphasis on low-power driving methods for battery-dependent mobile displays such as notebooks. The high-image-quality AMLCD desktop market has been driven to 8-bit data drivers, with some allowing even nonlinear voltage interpolation between bits, with a typical dynamic output voltage range of 10 V. The 384–420 outputs and usually column inversion is supported, so desktop AMLCDs can therefore be driven in dot inversion for optimum crosstalk cancellation. For IPS-AMLCD drivers, the dynamic output voltage range maximum is 18 V. The main engineering challenge for drivers as LCDs become larger and have a higher pixel content is in handling the higher driving voltage and frequency, which increases EMI noise. The time line of increase in TFT/LCD display information capacity as a function of video signal grayscale is plotted in [Figure 5.55](#).

Today's row drivers are available with simple 2-level gate drivers for various small and low-end notebook AMLCDs, as well as with 3-level or 4-level

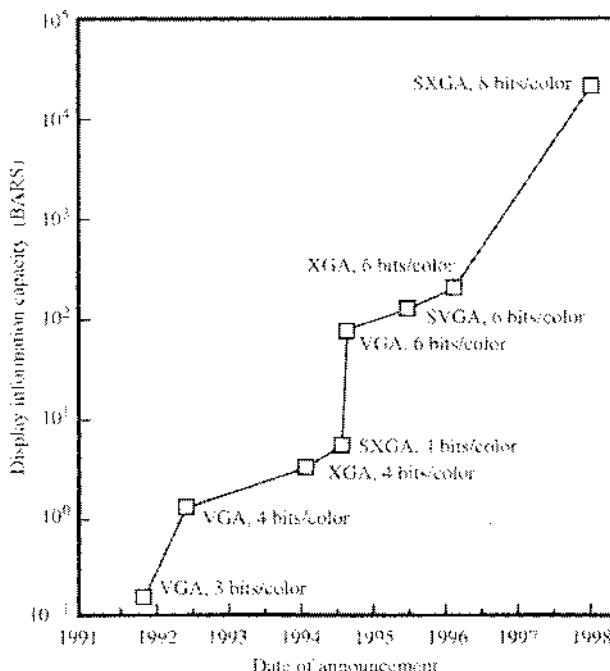


FIGURE 5.55 AMLCD information capacity rate of increase (pixel count times number of gray levels) versus year.

(in case of front-plane modulation) gate drivers that are increasingly used for improved image quality by feed-through voltage compensation in higher-performance AMLCDs. The dynamic range of gate drivers is usually limited to 40 V. In spite of the fact that output stages are fabricated with a high-voltage c-Si process, the logic circuitry of the driver is usually fabricated with a 3.3 V process. Overall, the scan driver chip is at least a factor of 2 cheaper per output channel, compared to the video signal driver. Some AMLCDs are now being introduced with the attempt of reducing the c-Si chip video-signal driver outputs, and thereby the cost, by multiplexing a given data driver output over two or more array data lines [65].

5.2.3 Integrated Drivers and Functions

Integrated drivers can be categorized into three main technologies: high-temperature polysilicon on quartz, low-temperature polysilicon on glass and flexible sub-

strates [66,67], and CMOS crystal silicon technology on silicon wafers. High-temperature polysilicon, low-temperature polysilicon, and crystalline silicon have achieved 8-bit integrated drivers with both analog and digital interfaces. All three are currently cocompeting in the projection display market, and low-temperature polysilicon is present in the smaller notebook AMLCD market [68–71]. Most of the projection light valves and viewfinder AMLCDs are produced by using a high-temperature polysilicon process. On the other hand, many companies are involved in crystal silicon AMLCD processing, and they see the future in integrating not only the driver chips but also more complex functionality in the direction of system on a chip. Furthermore, the smallest light valves are available in this technology, up to a resolution of $2\text{K} \times 2\text{K}$ pixels [72,73].

5.2.4 System Electronics

With respect to system electronics, AMLCDs prefer to be addressed progressively and with the option of a lower frame rate than CRTs, due to less screen flicker brought about by charge storage capabilities of the active matrix. If the display shows motion video, it must run at some multiple of 30 Hz.

Nevertheless, most graphic controllers are still not only based on driving a CRT with the provision of a full analog path but also based on a timing preference that necessitates the inclusion of a horizontal and vertical retrace time each frame time. Digital graphic cards are emerging as AMLCDs gain more market share in the desktop monitor market. In 2002, for the first time, revenue generated by AMLCD monitor products should exceed revenue generated by CRT monitors. These AMLCD graphic cards would be fully digital and would provide a complete digital path from the computer to the AMLCD. Without analog devices, those graphic cards or even a system-on-a-chip solution [74] will be low in cost and will implement digital controls for the monitor [75]. In order to complete the digital data path from the graphics card to the AMLCD, three competing standards [76] are currently available: GVIF (Gigabit Video Interface, from Sony) [77], OpenLDI (Open Low-Voltage Differential Signaling Display Interface, from National Semiconductor, relying on an LVDS interface {Low-Voltage Differential Signaling}) [78], and DVI (Digital Video Interface, from Silicon Image, based on TMDS {Transition Minimized Differential Signaling}) [79]. In addition to these standards, upper-layer protocols have been developed using data compression techniques such as delta transmission and spatial compression [80]. All of these approaches compete in terms of cost, power consumption, EMI, and display resolution support. Currently LVDS is widely used in notebooks, and DVI seems to be a favorite in desktops. Both allow larger physical distances between the system unit and the display unit.

Although Open LDI supports resolutions up to QXGA, DVI up to UXGA, and GVIF up to XGA, for higher resolutions, such as QSXGA and QUXGA,

multihead graphic cards segment those displays in four vertical stripes or four quadrants in order to meet the bandwidth requirements. To meet this challenge in higher-resolution displays, a variable scalability next-generation video interface, called Digital PV Link [81], is currently being codeveloped by four AMLCD companies. Digital PV Link is based on a protocol of packetized video data that is independent of the physical hardware layer so as to be able to support daisy-chaining of multiple display systems simultaneously via one DVI line [82]. In this manner, new AMLCD system architectures can be implemented that contain built-in frame buffers so that only the data packets for pixels being updated are sent; hence, the signal-video bus bandwidth can be greatly reduced. In addition, the need for good visibility of icons and menu scalability is critical when displays of different pixel content and resolution are interfaced. Preferably this will be done on the operations system level, but some scalability can be integrated into the graphics card.

5.3 STATE-OF-THE-ART HIGH-RESOLUTION HIGH-PERFORMANCE LARGE-AREA AMLCDs

The array design points for AMLCDs are dependent on many aspects, some of which are dictated by the display resolution and size, which together determine pixel content, and the LC mode and desired application-dependent response sought after.

For small displays (≤ 6 inches diagonal), the high-resolution array limit is dictated by the lithography ground rules to produce pixels with workable aperture ratios, but practically it has been restricted by the driver chip attachment pitch ($\geq 40 \mu\text{m}$) and/or kerf area. Poly-Si TFT arrays have found popularity for small displays, since partially or fully integrated drivers can decrease the array connections and eliminate the driver chip attachment pitch limitations. Larger displays generally exhibit increased scan-line *RC* loads and demand higher grayscale precision performance and uniformity that make none but c-Si drivers feasible. Compared to low-temperature p-Si (LTPS) integrated drivers, C-Si driver technology utilizes submicron technology with less transistor parasitics and better uniformity, lower voltage and power logic, higher bandwidth and increased current drive, and usually at lower cost. Cost comparisons must take into account all cost differences, including the driver chip, packaging and modular attachment costs for c-Si versus the increase in LTPS (usually *p*- and *n*-channel p-Si TFTs) processing steps, throughput and tooling depreciation, over the *n*-channel a-Si TFT process, and yield costs for LTPS.

For very large-area displays (≥ 28 – 40 inches diagonal) with moderate pixel count, such as specified for HDTV formats, the array limit is dictated by the scan-line resistivity ($\approx 2.5 \mu\Omega\text{-cm}$ for Cu and ≈ 4 – $6 \mu\Omega\text{-cm}$ for Al alloy with up to a few percent secondary metal), which in turn dictates the *RC* delay and

distortion of the scan lines but practically has been limited by the manufacturing glass size ($\leq 1 \text{ m} \times 1 \text{ m}$ generation 5 glass). [Table 5.10](#) summarizes the pixel and array parameters of a recent 40-inch diagonal WXGA (1280×769) a-Si TFT-LCD TV display [83,84], which is the maximum size achievable from a 730-mm \times 920-mm glass substrate.

For large displays ($\approx 15\text{--}25$ inches diagonal), of high pixel content, such as specified for high-end monitors, the array limit is dictated by the TFT charge-up time, but practically has been limited by the data rate bandwidth burden on the system electronics ($\leq 1\text{--}9$ Gbps). Figure 5.56 shows the feasibility of large-size and high-resolution a-Si, with the upper-right gate-metal boundary curve assuming 2500-Å-thick gate metal, metal lines driven from both ends at 60-Hz refresh rates [85], TFT channel length and mobility of 6 μm and 0.7 $\text{cm}^2/\text{V}\cdot\text{s}$. [Figure 5.57](#) shows attainable aperture ratio versus panel resolution for various pixel layouts dictated by the LC modes [86].

Here we introduce today's start-of-the-art highest-pixel-content displays, as an example of what the highwater mark is. Pixel density has grown by a factor of 2 in the horizontal and vertical directions from the conventional display, with about 100 ppi (pixels per inch). At 200 ppi, the human visual system has reached its limit to resolve pixels for 20/20 visual acuity and sitting at normal viewing

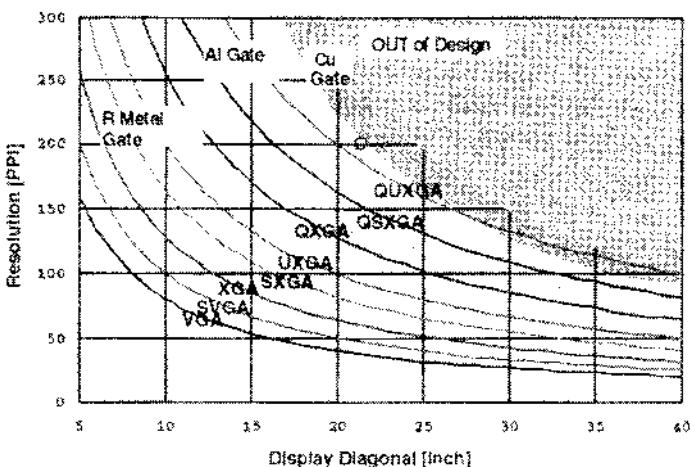


FIGURE 5.56 AMLCD resolution and display size possible as a function of display content and gate-line metal. The Darkest circle marks the highest-pixel-content AMLCD achieved to date. (From Ref. 84.)

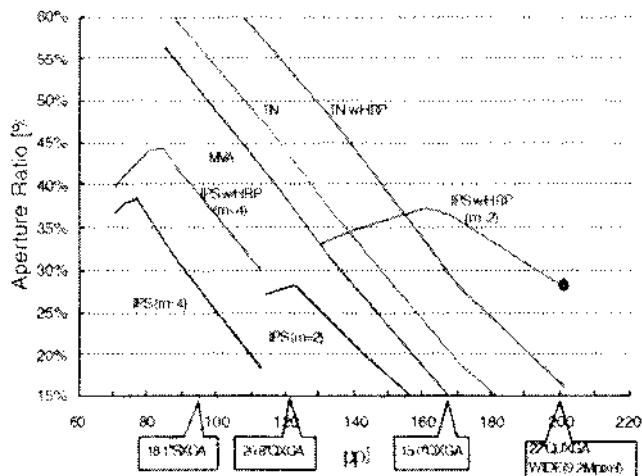


FIGURE 5.57 Pixel aperture ratio and resolution possible as a function of various wide-viewing-angle LC technologies, such as in-plane switching (IPS), multidomain verticle alignment (MVA), TN, and TN and IPS, with high-resolution process array build incorporating a low-dielectric-organic film that allows ITO electrode overlap of data bus line (TN w/HRP, IPS w/HRP). (From Refs. 84 and 85.)

distances from the display (>18 inches). In addition, pixel content is now sufficient, for the first time, for showing digitally compressed full-color Kodak CD images having a 3000×2000 pixel format. Ironically, we find that the pixel content and performance may in fact be, just as much determined by the system electronics as by the TFT array performance, so much that it has taught the industry to rethink the CRT monitor analog graphics adapter interface approach with an all-digital interface, and is only now motivating graphics adapter card manufacturers. Table 5.9 shows the history of high-resolution TFT LCD monitors. The T221 Display, a 9.2-million-pixel monitor with a pixel density of 204 ppi, incorporates an array of advanced technologies developed over several prototypes, with the AMLCD specifications listed in Table 5.11.

Some of the advance array technologies include aluminum-niobium ($3\text{--}5 \mu\Omega\text{-cm}$) scan-line metallurgy to shorten delay time; dual scan-line drive; TFT channel lengths shortened to $6 \mu\text{m}$; mobility increased to $0.75 \text{ cm}^2/\text{V}\cdot\text{s}$; minimum C_{gs} parasitics through self-aligned source/drain electrodes to gate electrode; minimum pixel capacitance to ensure pixel charge-up in $\sim 6\text{-}\mu\text{s}$ scan-line time; precise LC cell gate uniformity with integrated spacer posts [87,88], and polymer film

TABLE 5.9 History of High-Resolution TFT LCD Monitors

Year introduced	Diagonal (in.)	Pixel content	Resolution (ppi)	Company	Array technology
1995	16.1	SXGA	94	IBM	a-Si TFT
1996	10.5	SXGA	157	IBM	a-Si TFT
1998	13.3	UXGA	177	NEC	a-Si TFT
1998	16.3	QSXGA	202	IBM	a-Si TFT
1998	20	QUXGA	200	Toshiba	a-Si TFT
1999	9.4	UXGA	211	NEC	a-Si TFT
2000	22	QUXGA-W	204	IBM	a-Si TFT
3820 × 2400					

on array planarization process to eliminate crosstalk while maximizing the aperture ratio. The LC mode of dual-domain in-plane switching (DD-IPS) was used for a high-voltage holding ratio, even in the low resistivity of the LC, and for applying a new, highly uniform nonmechanical rubbing process based on one-drop LC fill and diamond-like carbon film-alignment layer followed by ion beam alignment. The IPS mode has less LC capacitance than TNLC mode; hence, less storage capacitance is needed, leading to a higher aperture ratio and less gate-

TABLE 5.10

AMLCD specification	40-in. XGA-W
Year introduced	2002
Rows × columns	768 × 1280 × 3
Resolution (ppi)	37
Subpixel dimension ($\mu\text{m} \times \mu\text{m}$)	227 × 681
Contrast ratio	600 : 1
Liquid crystal mode	PVA (plus viewing angle)
Max. luminance (cd/m^2)	500
Gate-line metalization	AL-Nb (<5 $\mu\Omega\text{-cm}$)
TFT W/L ($\mu\text{m}/\mu\text{m}$)	60/4.5
Gate-line time constant	2 μs
Data-line time	4.14 μs
Pixel capacitance	3 pF
Viewing angle	>170
LC response time (ms)	12

delay-dependent voltage feed-through to the subpixel. In addition, the array contains no fewer than 27.6 million TFTs, requires more than 16,000 input connections, and has array wiring that extends 5.0 km without a single break.

Obviously, in-line testing and repair play a pivotal role in increasing yield and reducing costs. All three panels listed in Table 5.11 had the benefit of an array tester charge sensing method (described in Sec. 5.1.4.7) with integrated a-Si TFT circuits, to reduce the probe numbers contacting the data and gate lines [89], as well as ALR repair. The array tester results not only provide high-throughput panel diagnostics (100% pixel-level testing time < 20 s/array), but feeds the data-mining database with in-line process diagnostics for continuous process and design improvements.

TABLE 5.11

Item	10.5" SXGA	16.3" QSXGA	22" WUXGA-W
Year introduced	1996	1998	2000
Rows × columns	1024×1280 × 3	2048×2560 × 3	2400×3840 × 3
Resolution (ppi)	157	202	204
Subpixel dimension ($\mu\text{m} \times \mu\text{m}$)	54×162	42×126	41.5×124.5
Aperture ratio (%)	35	27.3	28
Subpixel grayscale (bits)	6	8	8
Contrast ratio	130:1	230:1	400:1
Liquid crystal mode	TNLC-NW	TNLC-NW	IPS-DD
Maximum refresh rate	60 Hz	60 Hz	41 Hz
Max. luminance (cd/m^2)	120	230	235
Gate-line metalization	Al or Cu	Al-Cu or AL-Y	AL-Nb (<5 $\mu\Omega\text{-cm}$)
TFT W/L ($\mu\text{m}/\mu\text{m}$)	10/6	10/6	10/6
Array process			
lithographic steps	6	6	5–6
TFT mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)	0.4	0.4	0.75
Viewing angle (CR > 15)			>170
Allowed pixel leakage (A)		$<1 \times 10^{-12}$	$<1 \times 10^{-12}$
LC Response Time (msec)		20	16
Backlight power (W)	3	42	75
Timing, controller, uP, Drivers, display (W)	26		
Display adapter (W)	~8		
Total system power (W)	37	75	115

Different system electronics consist of four graphics adapters with synchronized data output (genlocked) for meeting the data rate bandwidth, or reducing the data bandwidth, which reduces the EMI generation. Several graphics cards support the T221 for the PCI and the Accelerated Graphic Port (AGP) bus, with digital outputs from one to four channels. Figures 5.58 and 5.59 show the system architecture of four graphics adaptors driving a 2048×640 pixel strips for 16.3-in. QSXGA display, and the four 1280×1024 pixel quadrants for the 22-in. Quadruple Ultra Extended Graphics Array—Wide format (QUXGA-W) [90]. In addition, the ATI FireGL4 card offers two single-channel DVI outputs that drive the panel into vertical stripes of 1920×2400 pixels at a refresh rate of 24 Hz, while the Matrox G200MMS card has four DVI outputs driving the panel in four vertical stripes of 960×2400 pixels at a data-refresh rate of 41 Hz. Still another, the ATI Radeon 8500 card, has a single DVI output channel, driving the panel at full 3830×2400 pixel resolution at a maximum data-refresh rate of 15 Hz [91]. The T221 monitor is fully digital since at a refresh rate of 41 Hz, the video data rate to the pixel exceeds 1.1 Gbps, which would otherwise lead to unacceptable analog driving artifacts. The digital input uses a Digital Visual Interface (DVI) standard. For CRTs, the screen- and data-refresh rates are the same and must exceed 80 Hz to suppress flicker. By minimizing C_{gs} through a source/drain-to-gate self-aligned TFT and minimizing channel length and TFT off-current, as well as minimizing scan-line distortion through the incorporation of double-ended scan-line driving and minimum C_s on the adjacent scan line

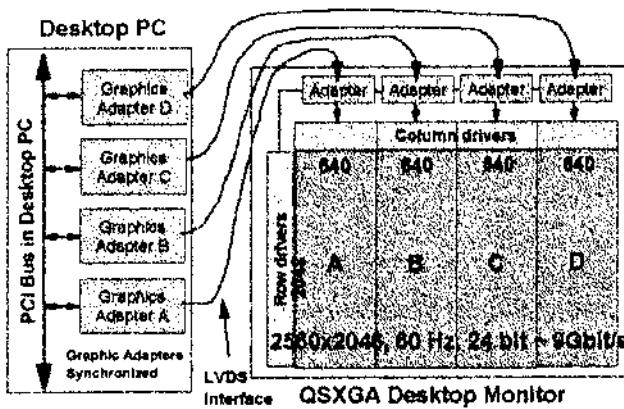


FIGURE 5.58 High-resolution AMLCD system architecture employing parallel, modular, and synchronized graphics adapters to provide the necessary data bandwidth. Example illustrating driving a 2048×640 pixel strips for a 16.3-in. QSXGA display. (From Ref. 89.)

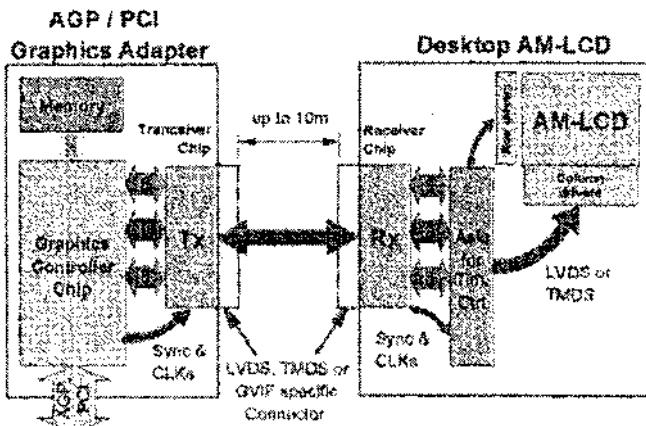


FIGURE 5.59 Example illustrating a complete digital data path from the graphics adapter to the $2400 \times 3840 \times 3$ WUXGA-W 22-in. AMLCD. (From Ref. 89.)

through the incorporation of a lower LC-IPS mode, a flicker-free display is designed. The data-refresh rate requirements depend solely on the quality of perceived motion necessary for a particular purpose, such as 24 and 30 frames per second, respectively, for film projection and video.

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6

Organic-Based Thin-Film Transistors

Francis Garnier

Laboratoire des Matériaux Moléculaires, Thiais, France

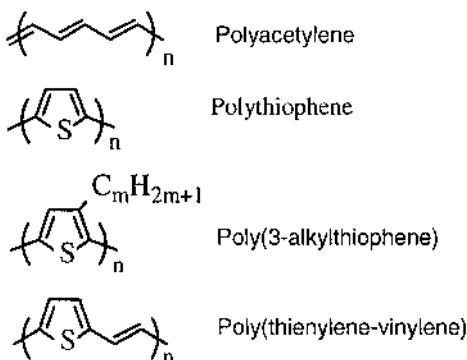
6.1 INTRODUCTION

Semiconductors have been at the origin of the most important industrial revolution of the 20th century, which has been dominated by the development of electronics. One of its basic components, the transistor, was initially proposed in the 1940s and based on germanium [1]. This was a bipolar device, a structure still in use in amplifiers. Another device structure, the field-effect transistor, FET, was developed later and used as a building block in electronic components such as logic circuits and microprocessors [2]. Field-effect transistors are unipolar devices in which the current flowing between two electrodes is controlled by the voltage applied at a third electrode, which recalls the mode of operation of the vacuum triode that was used in earlier radio and TV sets.

Various semiconducting materials have been used up to now for the fabrication of transistors, depending on the area of application of these devices. Besides their amplification characteristics, one critical parameter concerns their frequency of operation, in other words the time required for switching between their off- and on-positions. Thus, the power of a computer is linked directly to the number of basic operations accomplished per second. With this aim, high-speed transistors have been developed that are able to perform billions of operations per second. In terms of semiconducting material characteristics, this speed of operation is

directly proportional to the mobility μ of the charge carriers in the semiconductor. Whereas conductivity σ is the significant parameter for electrical conductors, the carrier mobility μ is the parameter that defines semiconductors. After the large amount of work devoted to inorganic-based semiconductors over the past 50 years, a deep knowledge, both experimental and theoretical, has been acquired on these materials. Direct band-gap semiconductors, such as monocrystalline gallium arsenide, GaAs, are known to exhibit among the highest values of mobility ($10^4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$), from which very high-speed devices can be built. An indirect band-gap semiconductor, such as monocrystalline silicon, shows a slightly lower mobility, of the order of $10^3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, but one still compatible with the requirements of high-speed electronics. These monocrystalline materials, however, are expensive to obtain in an electronic-grade purity, and their costly processing is not compatible with the production of large-area devices, such as required in an active-matrix liquid crystal displays. These flat panel displays consist of some millions of pixels, with each one being switched on and off by a particular transistor, which thus demands a cheaper technology. Fortunately, this last important industrial application does not require a high switching speed, for the response time of the human eye lies in the range of tens of milliseconds. In this context, inorganic-based semiconductors with much lower carrier mobilities are employed, such as polycrystalline silicon ($\mu = 10 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) and amorphous hydrogenated silicon, a-Si:H ($\mu = 0.1\text{--}1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$). Although possessing a much lower carrier mobility, this last semiconductor has been widely used for three decades in electronic devices that do not need a high operation speed (tags, display, smart cards), due to its much lower cost of fabrication and to its easier processing. Conventional inorganic-based electronics are thus characterized by a set of semiconducting materials with carrier mobilities ranging from 0.1 to $10^4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ that respond to the demands of various areas, from expensive, fast computers to displays and to low-cost, low-end electronics.

On the other hand, organic semiconductors have been studied since the early 1950s [3], dealing essentially with small molecules, e.g., condensed hydrocarbons and dyes. However, their semiconducting characteristics were poor and their reproducibility very low, which made these ill-defined materials incompatible with any real device development. A relatively minor fundamental interest was maintained in organic materials until the 1970s, when the first world energy crisis launched a renewed interest in organic-based semiconductors, aimed at the development of cheap, flexible, large-area organic-based solar cells. However, after a decade of intense research, both in universities and in private enterprise (Kodak, Xerox), results showed that organic semiconductors suffer from severe limitations, linked to the existence of a very high density of defects and traps, as well as to a very low carrier mobility [4]. The interest in organic-based semiconductors faded until the late 1970s, when a new class of materials was proposed in the literature, conjugated polymers, with their prototype polyacetylene [5].



These polymers were shown to exist in two states, one oxidized, possessing an intrinsic electrical conductivity, and the second neutral, with a less defined electrical behavior, ranging from insulating to semiconducting. The very high instability of polyacetylene under air restricted its characterization, and work was focused mainly on the electrical behavior of its oxidized state. One first example of an organic FET based on polyacetylene was reported in the literature in 1983, but in addition to its instability, the mobility obtained was also very low, on the order of $10^{-5} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [6]. The real development of organic-based devices required, first, air-stable organic semiconductors (e.g., conjugated polymers) to be synthesized, achieved in 1982 in the form of polythiophenes, which could be electrochemically synthesized as thin films on a conducting substrate (electrode) [7]. Solar cells and transistors were built using an electrochemically synthesized polythiophene film as the active layer, but the device characteristics obtained were also low [8,9]. Polyphenylenevinylene, PPV, was also shown to be air stable, but its field-effect mobility still lay in the range from 10^{-4} to $10^{-5} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [10]. Small molecules, phthalocyanines, had also been proposed in the late 1980s, but they did not bring a significant improvement in the semiconducting characteristics [11]. Although significant experimental effort was invested during the 1980s, the inability to increase significantly the carrier mobility above this low value of about $10^{-4} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ led many research groups to question the real potential of organic-based semiconductors for use as active layers in electronic devices.

Answers came in 1990, when it was shown that relatively short conjugated oligomers, e.g., sexithiophene, showed a mobility of the order of 10^{-1} $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, almost matching that of a-Si:H [12]. This result, together with the simultaneous first demonstration of a light-emitting diode fabricated from PPV [13], marked the birth of very intensive work on organic-based devices, in both university and private-sector laboratories, which led to a blossoming of organic-based devices. Before describing the actual state of the art in this area, we will

describe the basic principles underlying the mode of operation of field-effect transistors.

6.2 BASIC PRINCIPLES AND MODE OF OPERATION

The basic function of a field-effect transistor is to modulate the current flowing in a conducting channel between two source and drain electrodes by means of a variable voltage applied at a third electrode, the gate (Fig. 6.1). What is the origin of a field effect? Consider a plane-parallel condenser whose plates are a metal and a *p*-type organic semiconductor (SC), in which holes are the majority carriers. When no potential is applied to the plates, the free carriers are homogeneously distributed within the entire layer of the organic semiconductor. Owing to their low density, the conductance of the layer is very small and the current between the source and drain electrodes is very low. Now, when polarizing the gate negatively, an excess of holes will be attracted at the surface of the *p*-type semiconductor and will be concentrated there within a very thin layer. The density of charge carriers in this very thin layer will be largely increased, allowing a significant conductivity to be created in this conducting channel. On the other hand, when

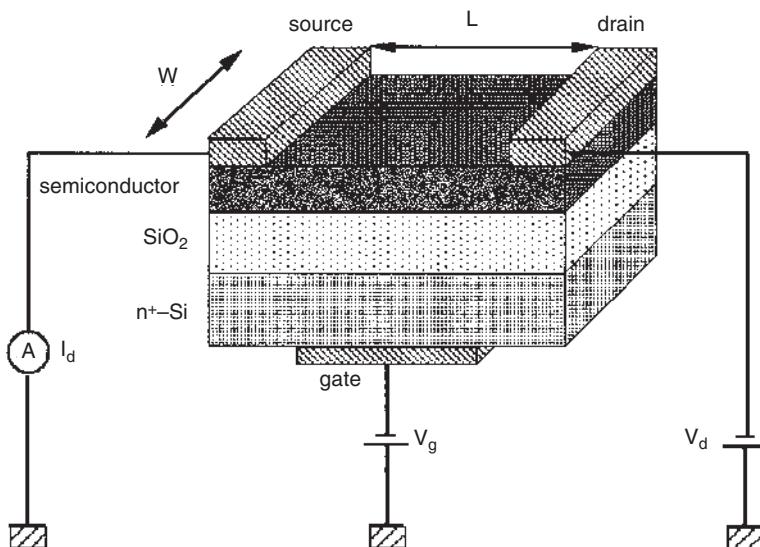


Figure 6.1 Schematic view of an organic field-effect transistor. W and L are the channel length and width, respectively.

applying a positive bias on the gate, a depletion of charge carriers occurs in the semiconductor, which, under sufficiently high gate voltage, can be extended over the whole thickness of the semiconducting layer. Thus the external voltage applied to the gate allows either the accumulation of charge carriers at the semiconductor–insulator interface or the depletion of this interface, leading to a modulation of the charge carrier density in this conducting channel. This modulation of the carrier density in the conducting channel is read by two other electrodes, source and drain, as shown in [Figure 6.1](#). A field-effect transistor, FET, is thus a three-electrode unipolar device that allows one to monitor, through the gate bias, the conductance of a thin channel at the semiconductor–insulator interface.

Among the different device architectures that have been proposed for this device, one of the most popular is the insulated-gate field-effect transistor, or Thin-Film Transistor, TFT. The development of this structure has been hampered by the fact that localized bound states are present at the surface of the SC, which trap a significant part of the induced charges and limit the conductivity modulation. Later, Weimer proposed the use of a very thin layer of a solid dielectric instead of air as the insulating medium between the condenser plates. The high density of charges induced at the SC surface by the high capacitance allowed the complete saturation of the surface states and the creation of the required conducting channel. Today TFTs are actually fabricated mainly from hydrogenated amorphous silicon as the semiconductor, a-Si:H, and are very widely employed in various applications, such as flat panel displays, in which they are used to switch on and off the liquid crystal–based pixels.

In order to analyze the potential of organic semiconductors as the active layer in transistors, a relatively simple device construction has been adopted ([Fig. 6.1](#)). It starts with a highly doped silicon substrate, which is conducting and used as the gate electrode. A thin layer of silicon oxide is thermally grown, forming the insulating layer. The semiconductor is then deposited as a thin layer by various methods that will be described later. Finally the device is completed by the evaporation of the source and drain electrodes, which form an ohmic contact with the semiconductor. In the case of a *p*-type semiconductor, a high-work-function metal, e.g., gold, is generally used as electrode material.

The mode of operation of such insulated gate field-effect transistors, or TFTs, has already been analyzed, following the knowledge developed for crystalline semiconductors and generalized to amorphous and polymer-based semiconductors [[14,15](#)]. The source electrode is grounded, and the insulated gate electrode is polarized negatively in the case of *p*-type semiconductors ([Fig. 6.1](#)).

The critical parameters of TFTs are the channel width, W , the channel length, L , and the capacitance per unit area of the insulator layer of thickness d , $C_i = \epsilon\epsilon_0/d$. Two main regimes are observed when plotting the drain current as a function of the drain voltage, at constant gate voltage ([Fig. 6.2](#)). At low drain voltage, V_d , the drain current increases proportionally to the drain voltage; when

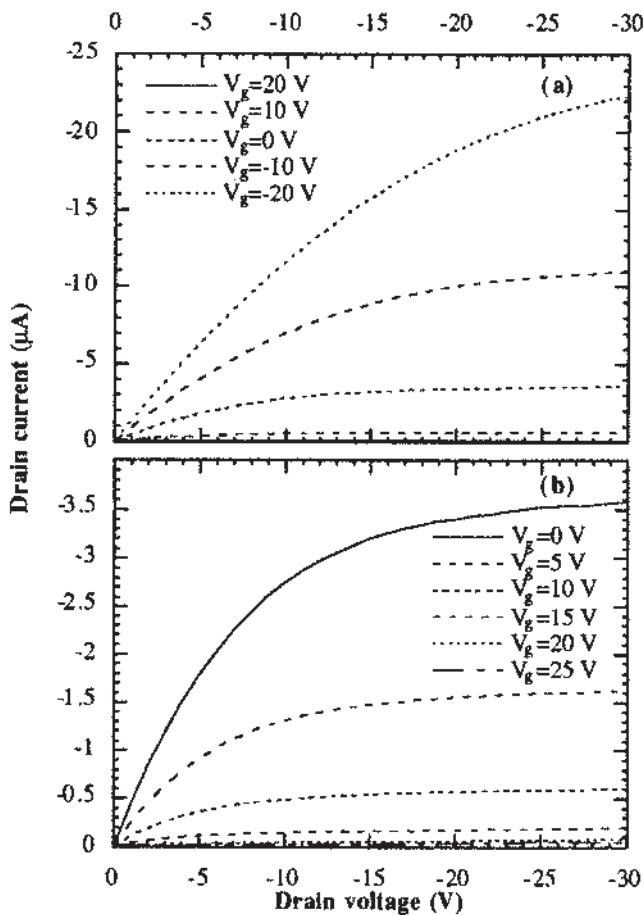


Figure 6.2 Experimental output $I_d = f(V_d)$ obtained with an organic FET, realized on glass substrate, with a polymethylmethacrylate insulating layer ($C_i = 10 \text{ nF}$), a sexithiophene semiconducting layer (25 nm thick), and gold source and drain electrodes ($W = 5 \text{ mm}$, $L = 50 \mu\text{m}$). (a) In accumulation regime (negative gate bias); (b) in depletion regime (positive gate bias).

V_d reaches the gate voltage, the voltage between drain and gate approaches 0, resulting in the pinch-off of the channel, which causes the saturation of the drain current. The basic equation relating the drain current I_d to the applied gate voltage V_g and to the drain voltage V_d for the linear regime is

$$I_d = \left(\frac{W}{L}\right)\mu C_i \left[(V_g - V_T)^2 - \left(\frac{1}{2}\right)V_d^2 \right] \quad (6.1)$$

where μ is the field-effect carrier mobility, V_T is the threshold voltage, given by $V_T = (qdp_0)/C_i$, where q is the absolute electron charge and p_0 is the hole density at zero voltage and d is the semiconducting film thickness. An important parameter of such a device is the transconductance, g_m , which is used to calculate the field-effect mobility, μ , generally carried out at a low V_d value.

$$g_m = \left(\frac{dI_d}{dV_g}\right)_{V_d = cst} = \left(\frac{W}{L}\right)\mu C_i V_d \quad (6.2)$$

For higher values of V_d , after pinch-off of the channel, the saturation regime is described by

$$I_{d,\text{sat.}} = \left(\frac{W}{2L}\right)\mu C_i (V_g - V_T)^2 \quad (6.3)$$

Equations (6.1) to (6.3) show that the value of the carrier mobility μ is a critical parameter defining semiconductors, for it directly controls the level of current output of these devices.

Whereas the accumulation regime, described by Eqs. (6.1) to (6.3), is generally observed under negative gate bias for p -type organic SCs, the occurrence of a depletion regime has seldom been characterized. The principle of the depletion regime is quite similar to that occurring in MESFETs. Under positive gate bias, holes are depleted from the semiconducting layer, the thickness of the depletion layer, W_{sc} , varying with the gate bias following this equation:

$$W_{sc} = \left(\frac{\epsilon}{C_i}\right) \left[1 + \frac{2C_i^2(V_g - V_{fb})}{(qN\epsilon_s)^{1/2}} - 1 \right] \quad (6.4)$$

where ϵ_s is the dielectric constant of the semiconductor, V_{fb} is the flat band potential, and N is the dopant concentration. The thickness of the depletion layer, W_{sc} , can be increased up to the total thickness of the semiconductor, d , which is reached at a “pinch-off” voltage V_p given by

$$V_p = \left(\frac{qNd^2}{2\epsilon_0\epsilon_s}\right) \left(1 + \frac{2C_s}{C_i} \right) \quad (6.5)$$

where C_s is the dielectric capacitance of the semiconducting layer. This equation

is particularly interesting, for it shows that the dopant concentration, N , can be obtained by the determination of the pinch-off voltage V_p .

The drain current observed in the depletion regime, given by this equation,

$$I_d = \left(\frac{Wdq\mu}{L} \right) \left[1 - \frac{V_g - V_{fb}}{V_p} \right] V_d \quad (6.6)$$

allows very low drain current values to be reached for these TFTs, which are needed for obtaining a high dynamic ratio.

Experimental output $I_d = f(V_d)$ obtained in the accumulation and depletion regimes, with TFTs involving sexithiophene as the semiconductor, are presented in [Figures 6.2a](#), and b, respectively [22]. These as-obtained experimental curves, shown without any correction, confirm the relevance of organic-based TFTs.

Besides the drain current obtained, I_d , reaching the regime of tenths of microamps, a very important characteristic of such a device concerns the dynamic range, or I_{on}/I_{off} ratio, which must be as high as possible and exceed 10^7 for practical applications where the TFT operates like a switch. Classical TFT structures involve, as source and drain contacts, back-to-back barriers formed either by Schottky barriers or by n^+ - p junctions. Under these conditions, a very low current is obtained at 0 gate voltage. On the other hand, in the case of organic-based TFTs, source and drain electrodes are generally ohmic contacts, made from gold directly, in contact with the organic SC. In organic devices, a large gate voltage is often needed for creating an accumulation layer at the semiconductor–insulator interface, which, owing to the bulk conductivity of the semiconductor, induces a significant ohmic contribution to the drain current observed in the TFT [17]. This current, which flows in the bulk of the semiconductor parallel to the channel, is not blocked by the ohmic electrodes and forms a leakage current that can mask the saturation of current at high drain voltages. These considerations allow one to point out that high field-effect mobility is not the only parameter that defines the relevance of a semiconductor. High mobility indeed is necessary for high current output for the device in its “on” position, from Eqs. (6.1) to (6.3), but a low conductivity is at the same time a prerequisite for ensuring low I_{off} currents and thus a high dynamic I_{on}/I_{off} ratio for the device. In fact, when considering the characteristics of amorphous hydrogenated silicon as a goal for such organic SCs, it must be remembered that its mobility reaches $1 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ but that its conductivity is very low, around $10^{-8} \text{ S} \cdot \text{cm}^{-1}$, which ensures the high dynamic I_{on}/I_{off} ratio, of the order of 10^7 – 10^8 , for a-Si:H based devices.

Finally, a last important parameter of TFTs concerns their switching time, which is often expressed through the transit time, $t = L^2/V_d \mu$ [14]. Besides the channel length W , a geometrical parameter that is fixed by the technology used for device construction, the value of the carrier mobility also controls the switching time of a TFT, and hence the area of application, as previously described.

The experimental determination of the intrinsic parameters describing a semiconductor, the mobility μ and the doping level N , can be performed through the electrical characterization of TFTs by the use of Eqs. (6.1) to (6.6). The field-effect mobility obtained differs, however, from the intrinsic, or microscopic, mobility of the semiconductor, μ_0 , due mainly to the presence of surface states and of traps in the bulk of the semiconductor, in which field-induced charges are distributed with a temperature-dependent profile. The presence of such traps leads to an effective mobility value, μ_{FET} , that is much lower than the microscopic mobility, μ_0 . The knowledge of μ_0 is, on the other hand, of importance, because it represents the limiting value of the carrier mobility that can be expected for a given material under ideal conditions. An analysis has been carried out, taking account of the presence of a shallow trap level, at an energy depth ΔE_t and at a concentration N_t . Under such conditions, a thermal equilibrium exists relating the free charges to the trapped charges:

$$\theta_0 = \left(\frac{N_v}{N_t} \right) \exp \left(\frac{-\Delta E_t}{kT} \right) \quad (6.7)$$

where N_v is the density of states near the top of the valence band. Because current is dependent on the density of free charges, the consideration of such distribution of charges represented by Eq. (6.7) leads to a modification of Eq. (6.3) representing the saturation current, where the mobility becomes $\mu_0\theta_0$. This situation holds for low gate voltages, but, as V_g is increased, the density of field-induced charges may exceed the trap density N_t . All traps being filled, any additional field-induced charge can be considered free, and the carrier mobility observed under such conditions becomes close to the microscopic mobility μ_0 . This analysis of trapping effects has been formalized in terms of a multiple trapping and release mechanism for describing the charge transport in conjugated materials [18].

Various architectures have been proposed for the construction of field-effect transistors; in the case of organic-based TFTs [16], the inverted-staggered TFT ([Fig. 6.3a](#)) and the inverted coplanar TFT ([Fig. 6.3b](#)) are the most frequently used, owing to the thermal and mechanical fragility shown by organic materials.

6.3 SCOPE AND LIMITS OF ORGANIC SEMICONDUCTORS

Various methods and materials have been used for fabricating organic-based TFTs. But before analyzing the experimental results, it is important to comment on the particular properties of *molecular* semiconductors, as opposed to *covalent* semiconductors, represented by silicon. This discussion will in fact allow one to set some theoretical limit for the field-effect mobility that can be expected for organic-based semiconductors.

As a matter of fact, inorganic semiconductors, e.g., silicon, present a three-dimensional architecture, in which silicon atoms are tightly held together by

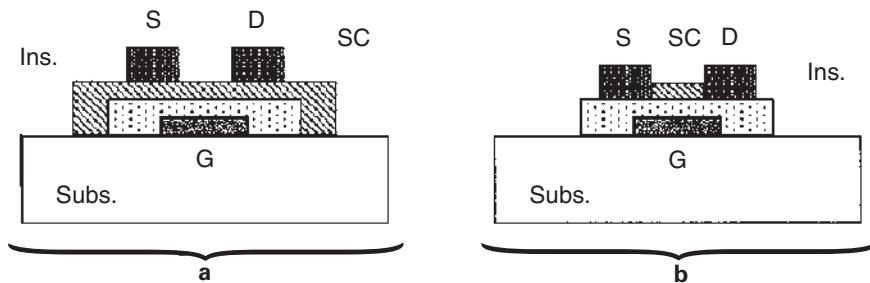


Figure 6.3 Schematic representation of field-effect transistor geometries generally used in organic-based devices. (a) Inverted-staggered; (b) inverted-coplanar. Subs. = substrate, Ins. = insulator, SC = semiconductor, G, S, D = gate, source, and drain electrodes.

strong covalent bonds, with energies on the order of $70 \text{ kcal-mole}^{-1}$ for Si–Si bonds. Semiconductivity appears then as a collective property that develops with the constitution of the 3D material. Owing to the strong interatomic bonds, the width of both the conduction and the valence bands is large, from which one may expect large carrier mobility values. These materials are very sensitive to chemical impurities, which constitutes the principle of doping of these materials, and they are also marked by the presence of dangling bonds at their surface, leading to the high sensitivity of their electrical properties to surface states.

On the other hand, organic semiconductors can be analyzed according to their classification as (1) conjugated polymers or (2) small molecules and short conjugated oligomers. Although it is agreed that charge transport within a perfectly conjugated macromolecular chain is highly efficient, it has also been well established that, due to lack of sufficient control of the polymerization reactions, the effective conjugation length in a conjugated polymer backbone is variable, rarely exceeding a length of 20–30 monomer units, i.e., a few nanometers. Conjugated polymers consist of long macromolecular chains, each one containing a random distribution of conjugated segments of different conjugation length separated by structural kinks, mainly sp^3 carbon atoms. Although charge transport within a conjugated segment can be considered very efficient, the transport over all the material sample then requires a hopping of the charge between conjugated segments located on adjacent macromolecular chains. This hopping mechanism over a variable and often large interchain distance has a low efficiency and thus forms the limiting step for charge transport in conjugated materials, all the more because conjugated polymers are structurally highly disordered (like a plate of noodles). One way to improve this efficiency is to create a high degree of molecular order and a tight packing of all the conjugated segments, in order to ensure

the largest possible overlap of their pi orbitals. This allows one to understand the importance of using well-defined monodisperse conjugated molecules, from which it can be expected that well-ordered materials can be realized. Thus small molecules, especially short conjugated oligomers, have been used as model compounds for discussing the structural factors that control the mobilities of carriers in organic compounds and their expected limit.

When now considering organic semiconductors based on such short conjugated molecular materials, the conjugated segments are held together only by weak van der Waal forces, of about $10 \text{ kcal-mole}^{-1}$. The electronic properties of these molecular solids are already present in the individual molecules, as shown, for instance, by the closeness of the absorption spectra of the individual molecules and of the solid. These features indicate that charge transport in molecular solids will operate mainly through individual states and furthermore that the width of the valence bands and of the conduction bands (when assuming validity of such representation) will be small and hence that only low carrier mobilities can be expected in these molecular solids. Theoretical considerations, as well as some time-of-flight measurements on monocrystalline compounds, have provided limiting values in the range of about $10 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for organic semiconductors at room temperature [3,19], lower by some three orders of magnitude than in their inorganic counterparts. A final but important point concerns the chemical inertness of the conjugated molecules and, hence, their very low sensitivity toward chemical impurities, together with the quasi-absence of dangling bonds, which prevents a high sensitivity to surface states. Owing to their much lower sensitivity to surface states and to impurities, one can reasonably hope that organic semiconducting films will be able to reach mobility values of the order of $1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, equivalent to that of a-Si:H. Due to their room-temperature processing and to the ease of realizing large-area films, organic-based semiconductors thus open a potentially interesting type of devices, challenging some applications of amorphous inorganic semiconductors.

6.4 DEVICES, MATERIALS, AND RESULTS

A large variety of conjugated molecules and polymers have been used over the years for constructing organic-based transistors. For describing the materials used and the results obtained, one of the most significant parameters distinguishing the various types of devices concerns the technique used for the deposition of the organic semiconductor. As a matter of fact, the most attractive goal offered by organic-based devices concerns their potential for opening up a new era of electronics, characterized by the unique properties of flexibility, light weight, low cost, large area, and even transparency. Owing to their organic nature, these semiconductors are potentially soluble in organic solvents and are thus amenable to deposition at room temperature on plastic substrates, by the use of a low-cost

spin-coating or casting technique, avoiding the use of high temperatures and of costly vacuum evaporation steps. On the other hand, vacuum evaporation has provided the most well-defined and reproducible films of semiconductors, which have allowed one to make decisive steps in understanding charge transport in organic materials. The different approaches proposed for the fabrication of organic-based TFTs will be reviewed.

6.4.1 Electropolymerization of Polythiophene

One of the first attempts to realize an organic-based transistor involved the electropolymerization of a conjugated polymer film on top of the source and drain electrodes [9]. The fabrication of these first devices closely followed conventional silicon-processing technology, with the substrate being made out of a highly doped silicon chip acting as the gate electrode. An oxide layer, SiO_2 , was thermally grown on silicon, forming the insulator. The source, S , and drain, D , gold electrodes were then deposited on the gate oxide, using either conventional lithography techniques with chemical etching or lift-off techniques. This substrate was then introduced in an electrochemical cell containing a monomer (pyrrole, thiophene), which was electropolymerized onto the two source and drain electrodes, until the two growing polymers merged and formed a continuous layer between the two electrodes. The thin films, e.g., polypyrrole or polythiophene, were obtained in their oxidized conducting state and had to be electrochemically undoped to their neutral semiconducting state. Although this method allowed some control of the polymer film thickness, calculated from the electrical charge used for the electropolymerization, and although some control existed on the remaining doping level in the semiconducting polymer, these semiconducting films suffered from many drawbacks. Electrochemically grown conjugated polymers possess a high density of structural and conjugation defects, which act as efficient traps for the free charges. Furthermore, once obtained in their oxidized state, these electrochemically grown polymers cannot be completely undoped, and the remaining dopants form charged mobile species that are incompatible with long-term operation of a device. The experimental results obtained on these first devices were deceiving in terms of the carrier mobility, which lay in the range of $10^{-5} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, and also of the dynamic ratio, which was hampered by the existence of a large ohmic current flowing between the source and drain electrodes [9]. This method for the fabrication of TFTs is no longer used.

6.4.2 Vacuum Evaporation of Oligothiophenes, Pentacene, and other Small Molecules

The high density of structural and conjugation defects in conjugated polymers, together with their very limited processability, led in the late 1980s to the use of vacuum evaporation for realizing thin organic semiconducting films. This tech-

nique consists of heating the organic material, using the Joule effect, in a tungsten boat under low vacuum, 10^{-5} – 10^{-6} Pa, with the substrate placed some centimeters above the boat. Vacuum evaporation has been shown to have many advantages for realizing thin semiconducting films, owing to the fine control exerted on the experimental conditions for film deposition, e.g., the vacuum level, the rate of evaporation, and the substrate temperature. Therefore, the purity of the evaporated material can be increased up to the crystalline level, the thickness of the layer can be precisely controlled, and the morphology of the molecular film can be tuned by the use of a temperature controlled substrate stage and further characterized by X-ray techniques. This method using vacuum evaporation has up to now afforded the highest field-effect mobility values.

A significant step was thus taken in the late 1980s with the study of well-defined short conjugated oligomers, e.g., oligothiophenes, as organic semiconductors (Fig. 3.4) [20]. The work aimed at the characterization of the relationship between molecular order and charge transport in these molecular materials. The very fine tuning of the structural characteristics of the semiconducting layer in the early 1990s allowed an understanding of the key relationship between carrier mobility and long-range order in organic-based semiconductors [21,22].

It must be recalled that the current in a TFT flows from source to drain, which means that the required directionality for charge transport in the semiconductor must be parallel to the semiconductor/insulator plane, i.e., parallel to the substrate plane. On the other hand, it is known that the charge transport within the organic conjugated semiconductor occurs through the overlapping pi orbitals of the conjugated molecules, i.e., along the stacking axis of the conjugated oligomers. This consideration means that the most efficient molecular organization

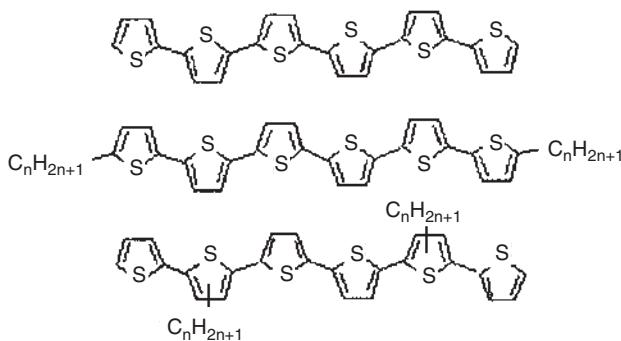


Figure 6.4 Molecular structure of sexithiophene, 6T, and its α,ω - and β -alkylated derivatives.

requires the pi orbitals to be perpendicular to the substrate plane, and in the case of conjugated oligomers it means that their long molecular axis must stand perpendicular to the semiconductor/insulator interface. Long-range molecular ordering is also needed, because any disruption acts as a grain boundary. How is such an organization achieved?

Various routes have been followed for an à priori control of the structural organization of the molecules in the oligomer-based semiconducting film, considered as a molecular assembly. Among them a physical approach involved either the modification of the experimental conditions used for film deposition or a film treatment. Another route, a chemical approach, aimed at tailoring the molecules in order to induce molecular self-assembly. Finally, the ultimate step involves the growth of a single crystal of the organic semiconductor, whose properties can be considered the achievable limit for charge transport. This work has been carried out on sexithiophene, 6T, chosen as the organic semiconductor.

6.4.2.1 Oligothiophenes

The structural organization of the organic material deposited as a thin film on a substrate can be controlled by the temperature of the substrate as well as by the rate of evaporation. A detailed study has been carried out on sexithiophene, 6T, which was deposited as 2- to 3- μm -thick films on Si substrates, held at temperatures varying from 77 K to 260°C [22]. Film deposition was performed either at a low evaporation rate, ranging from 1 to 5 Å/s, and also at high rate, of –100 Å/s, for a sample at room temperature. The structure and morphology of these films were analyzed by X-ray diffraction, XRD θ -2 θ scanning, and polarized UV-visible spectroscopies [23], as well as scanning electron microscopy [22].

X-ray diffraction results showed that 6T is a polymorphic molecule whose organization is highly dependent on the experimental conditions of film deposition. When deposited on a substrate held at 77 K, the molecular motions are frozen on the substrate. The first deposited 6T molecules nucleate and crystallize preferentially with their long axis lying parallel to the substrate plane. At room temperature and at high deposition rates, an additional peak is observed at low angle, which corresponds to a (001) reflection, indicating the presence of a new molecular orientation, with crystallites having their long *c*-axis perpendicular to the substrate plane. When deposited at room temperature and low deposition rates, the diffraction spectrum is different from the one obtained with high deposition rates, with a shift of the small-angle diffraction peak thus showing the existence, at room temperature, of two molecular organizations. One organization is a thermodynamically favored form, with molecules perpendicular (almost) to the substrate; another is kinetically favored, similar to that obtained at 77 K, with molecules parallel to the substrate plane. When deposited at 190°C, films of 6T exclusively show several orders of meridional (001) reflections, which means that a great majority of crystals are grown with their *c*-axis perpendicular to the

substrate plane. The adsorbed molecules stand up and crystallize in a self-organized way with a single preferential (002) orientation, corresponding to another crystalline phase. When further heating of the substrate to 260°C, the XRD spectrum reveals only low-angle (001) reflections, indicating that 6T films are entirely crystallized, with the (*a*, *b*) face parallel and the *c*-axis perpendicular to the substrate plane. These experimental results are evidence for the polymorphism of 6T, depending on the experimental conditions of film deposition. Polarized UV-visible spectroscopy was carried out on these films deposited at various substrate temperatures [22,23]. Absorption spectra were recorded at an incidence angle of 80°, using *s*-polarized light, with electrical field oscillating parallel to the substrate plane, and *p*-polarized light, containing both parallel and perpendicular components to substrate plane. Owing to the rigid all-trans planar conformation of the 6T molecule in the solid state, one can infer its $\pi-\pi^*$ electronic transition to be polarized along the long axis of this molecule. When increasing the substrate temperature from 77 K to 260°C, the absorption in the visible range under *s*-polarized light decreases strongly, with a simultaneous increase of the dichroic ratio. The spectra obtained at 260°C closely resemble those obtained by Egelhaaf et al. on monolayer films [23]. These results thus confirm the very high orientational order obtained when depositing these films on substrates held at elevated temperature. Finally, the morphology of these films has been analyzed by the use of scanning electron microscopy [22]. Results show that films deposited at 77 K present a uniform surface consisting of small crystallites (10–30 nm). When deposited at room temperature, the size of the crystallites increases to some 50 nm in diameter, with an isotropic distribution. When the substrate is held at 190°C, the crystallites show an elongated shape, with larger dimensions reaching 30×200 nm², with a close packing arrangement. On the last sample realized at 260°C, the 6T layer shows a discontinuous surface, arising from possible cellular growth. Long lamellae, 50 nm wide, are observed, most of them interconnected, giving rise to a network over the film surface. These results confirm that the control of substrate temperature allows one to monitor the grain size and shape, together with the homogeneity of structural organization. In particular, the development of lamellar crystals, with possible interconnection resulting from their coalescence, provides highly organized molecular layers, with a lower concentration of grain boundaries and thus largely enhanced electrical characteristics.

Another method that has been described for improving the structural organization involves the annealing of a film of conjugated material. Sublimed films of 6T are polycrystalline, with isotropic grain size of about 50 nm. Annealing has been performed by heating the film for a very short time at the melting temperature of 6T, 310°C. The crystallite size increased significantly, up to several microns [24].

In conclusion, these structural characterizations confirm that the control of the substrate temperature and of the evaporation rate for film deposition, together

with the annealing of the film, allowed control over the structural organization of oligothiophene molecules in the solid state.

A parallel large improvement with structural organization is observed in the charge transport properties of these materials [22]. The conductivity parallel to the substrate surface has been measured using the four-probe technique, and the perpendicular conductivity from a sandwich-type structure, with two gold contacts forming Au-6T-Au. Importantly, an increase in the anisotropy of conductivity has been observed, which indicates an increase in molecular ordering perpendicular to the substrate surface, as previously shown from structural characterizations and in full agreement with the proposed charge transport process occurring along the stacking axis of the 6T molecules. The field-effect mobility has been measured from TFTs realized on glass substrates fabricated by the successive vacuum deposition of an aluminum gate electrode, the spin-coating of a thin (0.5-mm) PMMA insulating layer, and the vacuum deposition of two gold source and drain electrodes. The device, constructed according to an inverted-staggered architecture ([Fig. 6.3a](#)) was completed by the vacuum deposition of the oligothiophene-based semiconductor, with a thickness of about 30 nm. Large channel geometries were used, $W = 5$ mm and $L = 50$ μm , owing to the conventional shadow-masking technique employed for this TFT fabrication. Field-effect mobility was calculated in the linear regime of I_d-V_d curves, from Eq. (6.2). The lowest value of μ ($= 2 \times 10^{-3} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) is obtained for a film deposited at room temperature, which has been shown to be the less organized one, with two orientations of crystallites, one parallel to the surface and the other perpendicular to the surface, confirming that a high density of grain boundaries is very unfavorable for charge transport. A slight increase in μ is observed when cooling the substrate at 77 K ($\mu = 6 \times 10^{-3} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) which can be attributed to the higher homogeneity of the film, with a main population of molecules lying parallel to the substrate plane. Although the stacking axes of molecules in this last film are not oriented parallel to the substrate plane along the source-drain electrode axis, the higher observed mobility, as compared to room-temperature 6T, points out the extreme importance of grain boundaries in charge transport. When the 6T film is deposited on a heated substrate, the observed field-effect mobility increases rapidly, by more than one order of magnitude, and values between 0.03 and 0.05 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ have been obtained for the field-effect mobility of unsubstituted 6T [22,24]. These results are clear confirmation of the predominant role played by the structural organization of the semiconducting film and also of the control that can be exerted by the experimental conditions used for the film deposition.

6.4.2.2 Chemical Engineering of Alkylated Oligothiophenes

Chemical engineering of these oligothiophenes may also represent an interesting alternative route to controlling the molecular organization in the film. As a matter of fact, micellar chemistry has already shown the large potential of various chemi-

cal substitutions, using, for instance, alkyl or alkoxy groups, for inducing a mesoscopic organization of molecules. Following this concept, various oligothiophenes substituted at their α, ω end positions have been described in the literature. Alkyl groups have been used, such as methyl and ethyl on terthiophene to sexithiophene, or hexyl groups on sexi and octathiophene [21,25]. In addition, end-capped oligothiophenes, in which the terminal 4,5 positions are blocked with a trimethylene bridging unit, have also been intensively studied [26]. These oligomers, mainly alkyl-substituted oligothiophenes, have been the object of the most intense structural characterizations, and the relevance of crystal structure on charge transport has been intensively reviewed [27].

The crystal structure for short substituted oligomers (dimethylterthiophene and dimethylquaterthiophene) has been determined by X-ray diffraction on single crystals [27], whereas dihexylsexithiophene and dihexyloctithiophene, which do not crystallize, have been characterized as thin films by θ -2 θ scanning XRD [21]. Detailed spectroscopic studies under polarized light have also been used for analyzing the structural organization of films. Results have shown that, even when deposited on substrates at room temperature, films of dihexylsexithiophene, DH6T, are highly structured. Numerous high-order (001) reflections are observed, up to the 34th order, in agreement with results obtained on dimethylquaterthiophene, which indicates that the crystallites with a monoclinic unit cell have their long *c*-axis perpendicular to the substrate plane. Furthermore, structural organization at the mesoscopic level has been obtained from X-ray pole figures, which confirmed the existence of almost a single population of molecules standing up on the substrate plane with their (*a*, *b*) face as a contact plane. The analysis of the molecular organization in these films has led to the schematic representation shown in Fig. 6.5 [21]. The almost complete organization of molecular layers, realized on a susbrate at room temperature, must be associated with the highly improved stacking properties produced by the terminal alkyl groups, which are already known for inducing long-range ordering and mesophases.

These films can be described as a liquid crystal-like superstructure imposed by the terminal alkyl groups for the whole molecular assembly. Alkyl–alkyl recognition, based on lipophilic–hydrophobic interactions, produce a strong driving force for a close packing of the conjugated sexithiophene backbones and also, most importantly, for a long-range molecular ordering. The most remarkable feature realized through α, ω -dialkylsubstitution thus concerns the obtained meso-phase-type structure of the film. A lower concentration of grain boundaries can be expected in these films, which fulfills the requirements for improved charge transport properties.

The electrical characteristics show that α, ω -dialkyloligothiophenes present an increased parallel conductivity, which reflects the longer-range order and fewer defects existing in layers of these last conjugated materials. More significantly, the field-effect mobility increases dramatically, as confirmed by the range of

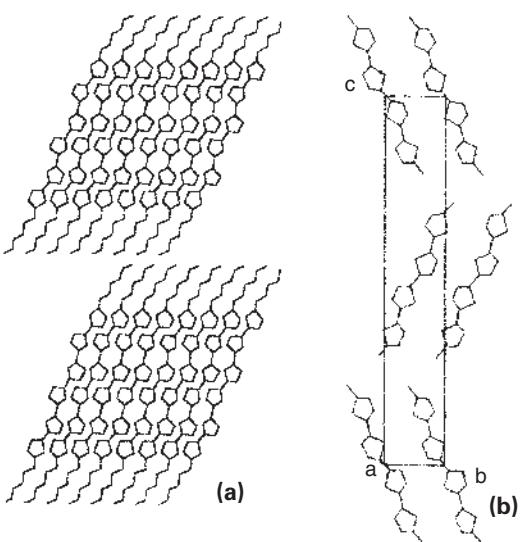


Figure 6.5 Packing mode of a vacuum-evaporated α,ω -dihexylsexithiophene film.

mobility values obtained for α, ω -dihexylsexithiophene, DH6T, $\mu = 0.08\text{--}0.13 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, the highest value being reported by the IBM Yorktown group [21,28]. This result deserves some comment: (1) The mobility value of DH6T deposited at room temperature is higher than that reported for unsubstituted sexithiophene, even when 6T is deposited on a heated substrate ($0.05 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$). Furthermore, (2) it is very close to that measured on a single crystal of 6T ($0.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) (see later).

An important conclusion can be drawn concerning the potential interest of the chemical approach for controlling the structural organization of oligothiophene films. As a matter of fact, the chemical engineering of oligothiophene molecules, involving end-substitution by alkyl groups, is an elegant and powerful way to induce long-range self-assembly of the oligothiophene molecules. This approach, which can in principle be extended to any molecular-based semiconductor, reveals that one of the most promising advantages offered by organic-based semiconductors is structural organization.

6.4.2.3 Pentacene

Besides oligothiophenes, a large set of studies have been devoted to pentacene (Fig. 6.6), which belongs to the family of polyacenes. Pentacene has been depos-

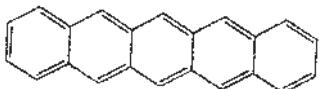


Figure 6.6 Molecular structure of pentacene.

ited as a thin film by various techniques, such as vacuum evaporation and a pulse-laser technique, for realizing organic-based FETs. The mobilities obtained have been shown to be highly dependent on the purity of the material. The values initially obtained, on the order of $2 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [29], have risen progressively to the important value of $1.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, recently obtained in FETs with these films [30–33]. The scattering of the recently obtained mobility values, ranging from 0.3 to $1.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, must be attributed to the variable size of the pentacene crystallites in the film.

The highest mobility values have been obtained by heating the substrate to high temperature during film deposition, affording micron-sized pentacene crystallites that statically matched the micron-sized channel lengths of the FET device. Large $I_{\text{on}}/I_{\text{off}}$ ratios, up to 10^8 , have been reported for pentacene-based transistors [32], but it must be noted that these values have been obtained by sweeping the gate voltage over a very large potential range, from +100 V to -100 V, which is very far from the voltages used in microelectronics.

Importantly, a comparable mobility value has recently been obtained by the research group of Lucent Bell Labs via the use of a single crystal of pentacene, which confirms the closeness of the carrier mobility observed in polycrystalline materials and in a single crystal. The structural characterization of pentacene single crystals showed the existence of parallel-packed planar molecules in a herringbone packing, as in the case of oligothiophenes [35]. In addition, pentacene was used by the IBM Yorktown group for analyzing the interaction between charge carriers and localized trap levels in the gap. This elegant work emphasizing the role played by the insulator will be described later.

These results show that pentacene and other fused ring molecules, such as benzodithiophene [34], are potentially interesting molecules for their strong tendency to pack into parallel layers and to stand perpendicular on many substrates, fulfilling the requirements for high carrier mobility.

6.4.2.4 Phthalocyanine and Other Electron-Rich Molecules

Small π electron-rich molecules, such as scandium, lutecium, and thullium diphthalocyanines, ScPc_2 , LuPc_2 , and TmPc_2 [11], nickel and zinc phthalocyanines, NiPc and ZnPc [36], and tetracyanoquidinomethane, TCNQ [37], were used for fabricating the first TFTs. Owing to their cage structure, phthalocyanines, which

were among the first reported organic semiconductors [3], can incorporate different metal atoms M (Fig. 6.7), which allows their electronic properties to be tuned and to exhibit either *p*- or *n*-type behavior [36,38]. In addition, phthalocyanines possess a two-dimensional structure with a high driving force to form columnar stackings for which charge transport is highly favored along the stacking axis. Mobility values of the order of 10^{-4} – $10^{-3}\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ have been observed, and the origin of the semiconducting behavior of these molecular materials has been well discussed [36].

Later it was recognized that the directionality of charge transport, i.e., the stacking axis of phthalocyanines, should be parallel to the substrate plane, as required by the position of the source and drain electrodes (Fig. 6.1). Phthalocyanines molecules must therefore be deposited standing on their edge in order to meet this requirement. The group at Lucent Bell Labs recently succeeded in facing this challenge and reported a mobility value of the order of $10^{-2} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [39]. Although phthalocyanines are attracting semiconducting materials, they have been shown to be very sensitive to oxygen, which is a limiting factor for their use [40].

In conclusion, although vacuum evaporation is a costly process, which limits the potential interest of the corresponding devices, it must be mentioned that evaporation of an organic-based semiconductor can easily be performed on a plastic-based substrate, such as a polyimide sheet, on which the gate electrode and a polymer insulating film, e.g., PMMA, have already been deposited. Further vacuum evaporation of the gold source and drain electrodes affords (besides the metallic electrodes) an all-polymer flexible device whose construction and characteristics were first demonstrated in 1990 [12].

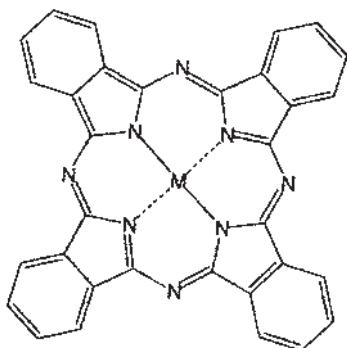


Figure 6.7 Molecular structure of phthalocyanines. M is a metal atom or H₂.

6.4.3 Single Crystals of Sexithiophene and Pentacene

An ultimate molecular organization can be expected from the use of single crystals of conjugated molecules as active materials in organic-based FETs. The main interest of these structures lies in the fact that the structural order of molecules is maximized in these crystals, and they thus represent the model compounds that should afford the highest mobility value accessible for organic-based semiconductors, as in the case of the parent inorganic-based compounds. This work has also to be considered in light of the very intense experimental and theoretical work that has been devoted to charge transport in single crystals of condensed hydrocarbons, in which the carrier mobility has been determined very rigorously using, for instance, time-of-flight measurements [19].

Large single crystals of sexithiophene have been grown and characterized by X-ray diffraction, which showed that the conjugated molecules are fully planar and tightly packed in a herringbone structure (Fig. 6.8) [41]. Field-effect transistors were fabricated from these crystals, with a carrier mobility value of the order of $0.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [42,43]. This is significantly higher than that observed on polycrystalline 6T ($0.05 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) and on dihexylsexithiophene ($0.13 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$), which suggests that grain boundaries in these latter materials are at the origin of the observed lower mobilities. However, due to difficulties in device construction, the value of $0.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ cannot be ascertained. As a matter of fact, the single crystal, of around 10-microns thickness, was just deposited on top of the PMMA insulating layer. The high resistance of the crystal and the bad definition of the semiconductor/insulator interface could have led to an underestimated value of the mobility in this single crystal.

On the other hand, the Lucent Bell Labs group has been able to propose clear evidence of the morphological origin of the very high field-effect mobility in pentacene-based thin film transistors [44].

6.4.4 Solution-Processed Polyalkylthiophenes

Solution processability at room temperature is certainly the most attractive aspect of organic-based semiconductors, offering the widest potential of applications in

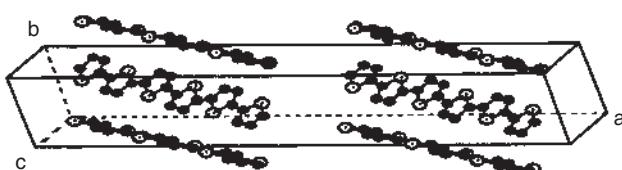


Figure 6.8 Structure of a sexithiophene single crystal.

the new field of polymer electronics. As a matter of fact, spin-coating is a very well-mastered technology that yields thin films of very high homogeneity and controlled thickness. This technique, however, requires a high solubility of the material (polymer, oligomer, or small molecule), of the order of grams per liter, a level that exceeds by four or five orders of magnitude that of conjugated derivatives. In order to overcome the almost complete insolubility of conjugated polymers, various approaches were proposed in the late 1980s. In the case of PPV, a soluble precursor polymer was deposited as a thin film, which was then converted to PPV by the use of a thermal or chemical treatment [10,47]. Such treatment, however, induced the presence of impurities and defects in the conjugated polymer film, with various consequences concerning its semiconducting characteristics. Whereas light-emitting diodes, as well as field-effect transistors on a qualitative aspect, could be demonstrated with such thin films of PPV, the carrier mobility values calculated from the TFT characteristics were very low, of the order of $10^{-4} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

A much more attractive way to overcome insolubility involves the grafting of solubilizing alkyl or alkoxy groups along the conjugated polymer chain, e.g., on polythiophene or polyphenylenevinylene, which affords highly soluble and film-forming conjugated polymers [48–51]. Small conjugated molecules, e.g., quaterthiophene, phthalocyanines or pentacene, that do not show a high solubility have also been chemically modified in order to increase their solubility and allow them to be cast from solution [52,53]. The most significant work was carried out on alkylated conjugated polymers, and the first experiments concerned the use of nonregioregular poly(3-alkylthiophene), a polymer structure that does not allow a tight and ordered packing of the conjugated chains. These polymers were spin-coated on top of various insulators, but the results in terms of carrier mobility were deceiving when compared to those obtained with vacuum-evaporated oligothiophenes, with the observed mobilities lying in the range 10^{-5} – $10^{-4} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

After the demonstration that structural organization of the conjugated chains plays a determining role for the efficiency of the charge transport, it became apparent that long-range order was a key toward high carrier mobilities. Furthermore, the active part in the semiconducting film, i.e., the conducting channel, is located as an ultrathin layer at the surface of the semiconductor in contact with the insulator. It was also recognized that this interface had to be mastered. Thus, work was achieved in two directions. First, regioregular-substituted conjugated polymers, e.g., poly(3-alkylthiophenes), have been synthesized that show a very high solubility and film-forming properties [54,55]. X-ray characterizations confirmed the long-range order and the homogeneous dense-packing of conjugated segments in these films. The second area is concerned with the poor wetting properties of the organic semiconductor on the insulator surface, particularly on an inorganic one (SiO_2), which also strongly disturbs the structure and homogene-

ity of the deposited semiconducting film. A pretreatment of the surface by the use of various molecules, e.g., hexamethyldisilazane, alkylthiols, or alkylsilanes, has been shown to be successful.

Interesting mobility values have been obtained, of the order of $0.01 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ [54], and a value of 0.1 has even been claimed [55]. It seems, in fact, that the semiconducting properties of these solution-deposited films are highly sensitive to the pretreatment of the insulator surface and also to the purity of the regioregular polyalkylthiophene. The existence of even very few nonregioregular monomer units within the polymer chain appears, in fact, sufficient for altering the required long-range order in the deposited film.

Various substituted conjugated polymers and smaller soluble molecules have thus been deposited as thin films on TFT substrates, using a solution process, and it is noteworthy to compare the results obtained with the previously reported results. Thus, when comparing thiophene-based or pentacene-based devices, the obtained mobility values, whatever the molecules or the pretreatment, are always smaller by at least one order of magnitude than those obtained when using a vacuum-evaporated semiconducting film, confirming that the problems of material purity and of surface pretreatments are not yet solved.

A solution-related method is the Langmuir–Blodgett technique, which has also been proposed for depositing molecular-scale films on various substrates [56–58]. Excellent control of the thickness and of the internal structure of the film can be expected from such a technique, provided that the semiconductor molecules, which are generally hydrophobic, have been grafted with a hydrophilic group in order to obtain an amphiphilic molecule. Interesting transistor characteristics have been obtained by the use of mixed layers of an oligothiophene, quinquethiophene, and arachidic acid, but the necessary presence of an electrically inactive component (arachidic acid) lowers the transistor characteristics [56–58].

In terms of solution-processed semiconductors, a recent innovative work must be acknowledged that concerns organic–inorganic hybrid materials, accomplished by the IBM Yorktown group. Hybrids based on perovskite structure have been crystallized from solution, leading to well-oriented molecular stacks composed of alternating organic and inorganic sheets. The conducting channel formed by such a structure benefits from the high performance of the inorganic counterpart, together with the film-forming properties from the organic counterpart. Thus a solution of the semiconducting perovskite $(\text{C}_6\text{H}_5\text{C}_2\text{H}_4\text{NH}_3)_2\text{SnI}_4$ can easily be spin-coated, forming a thin film that shows promising TFT characteristics, with a carrier mobility of $0.6 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and a current modulation value larger than 10^4 [59].

6.4.5 All-Organic Devices Fabricated via Printing Techniques

Special attention should be given to all-organic devices, which must be considered an ultimate goal of this new emerging domain of polymer electronics. The organic

origin of all its components should allow an organic-based TFT to be fabricated at room temperature merely by the use of printing techniques, opening up the field of low-cost, flexible, lightweight electronics. The first step in this direction was reached in 1990, when an all-organic flexible TFT was realized on a polyimide substrate, involving PMMA as the insulator and sexithiophene as the organic SC; but the three electrodes were still metallic [12]. It was then shown for the first time that the TFT characteristics remained unchanged under mechanical bending of the polymer-based flexible device. Later, in 1993, a work appeared describing a flexible light-emitting diode fabricated from an organic-based substrate and semiconductor but also fabricated with metallic electrodes, which claimed to be the first flexible all-organic device.

The decisive step was taken in 1994, when an all-polymer device was fabricated for the first time by using only printing techniques, of organic-based materials that included electrodes made from carbon-based conducting ink [58]. The device was fully flexible, and its electrical characteristics, equivalent to those of a classical organic-based TFT, remained unchanged during and after severe mechanical treatments. Significant efforts are actually being invested in this direction by private enterprise and university labs, with the aim of using various inkjet-printing devices. Thus, the very active group at Lucent Bell Labs has also built an all-printed device based on a ITO-coated polyester substrate, followed by the deposition of a polyimide insulator layer, a semiconducting poly(3-alkylthiophene), and conducting ink-based source and drain electrodes [61]. A further step was achieved by this same group via a microfabrication technique. Micromolding has been realized in capillaries, MIMIC. Lithographic techniques are employed to realize an elastomeric micromold into which a solution of conducting polymer, polyaniline, is deposited onto the semiconductor layer, yielding the source and drain electrodes. With a channel length of 25 μm , this all-organic device showed a mobility of about $0.05 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, which represents a very promising value [62]. Finally, attempts have also been made at Philips Laboratories, starting with a polyimide substrate on which a poly(vinylphenol) insulating layer, a polythienylenevinylene semiconducting layer, and polyaniline-based electrodes were successively spin-coated, leading also to an all-organic device. A photoinitiator was used in addition to the polyaniline, in order to pattern the electrodes via UV exposure through a mask. The problem concerned the use a series of materials with different solubility properties in order to prevent the dissolution of the underlying layers at each deposition step. The mobilities obtained, of the order of $3 \times 10^{-4} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, although low due to the nature of the semiconductor used, were still sufficient to generate a 5-bit mechanically programmable code generator combining 326 organic TFTs [63].

All-organic devices have a real promising future, although it must be remembered that this approach is limited by the spatial resolution offered by the printing techniques, of the order of tens of microns. Only large and even oversized

TFT geometries are achievable, but applications for “low-end electronics” exist, and improvement in the resolution of printing techniques can also be expected.

6.4.6 *n*-Type Semiconductors

As previously described, the quest toward *n*-type semiconductors aims at the realization of *pn* junctions that would allow a large on/off ratio in the TFT current output, analogous to inorganic-based junctions. On the other hand, the vast majority of organic-based semiconductors are *p*-type materials, which are not intentionally doped. Some conjugated polymers, e.g., polyacetylene, have been deliberately *n*-doped via ion implantation (Li^+), but the doping level is low (less than 10^{17} cm^{-3}), their distribution is difficult to control in the material, and, most importantly, these small doping ions are mobile when in the presence of an external field, which is incompatible with any device operation. The absence, or at least the very low long-term stability, of *n*-type materials is linked to the fact that radical anions are chemically much less stable than radical cations. The first examples of *n*-type materials, e.g., TCNQ, C_{60} , C_{70} , have confirmed their high reactivity toward oxygen, which has not allowed their use in devices operating under air. The concept of organic-based *n*-type materials however, largely evolved in the 1980s during the work devoted to light-emitting diodes, where electron-transporting materials were developed in order to increase the efficiency of such organic-based devices [64,65]. An *n*-type semiconductor corresponds to an electron-transporting material, possessing a high electron affinity, and many molecules have been proposed in this regard, such as napthalene tetracarboxylic dianhydride, NTCDA, and a large series of perylene derivatives, such as perylene tetracarboxylic dianhydride, PTCDA [66]. In other words, the concepts of *valence* and *conduction band* can be replaced in these molecular materials by the terms *highest occupied molecular orbital*, HOMO, and *lowest unoccupied molecular orbital*, LUMO.

This approach has been used for designing new types of semiconductors, obtained by tuning the electron affinity of known (macro)molecules. Thus, the full substitution of a phthalocyanine with fluorine substituents allowed the Lucent Bell Labs group to propose a highly stable *n*-type semiconductor [67,68]. In terms of these results, the carrier mobility was also shown to be highly dependent on the structural organization of the organic film, and mobility values of the order of $10^{-2} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ have been reported by the Lucent Bell Labs group for perfluorinated phthalocyanines and for C_{60} in high vacuum. Stable *n*-type organic semiconductors with high carrier mobility are still a very important challenge for chemists.

6.4.7 Effect of the Insulator on the Carrier Mobility

The effect of the nature of the insulator, and particularly of its dielectric constant, was recognized early, although not well understood. In fact, the very high carrier

mobility observed in 1990 with sexithiophene-based TFTs, $\mu = 0.1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [12], must be attributed to the use of cyanoethylpullulan as the insulator, which possesses a fairly high dielectric constant of about 18. The effect of the insulator has recently received much more attention, particularly by the group IBM Yorktown [67].

As shown by Eqs. (6.1) to (6.4), the electrical characteristics of a TFT are also governed by the capacitance C_i of the insulating layer, which directly controls the density of carriers in the conducting channel. This carrier density plays a key role in the mode of operation of TFTs. As a matter of fact, a high density of localized states exists in the energy gap, and under no or low gate bias the carrier transport occurs through hopping between these localized states. When increasing the gate bias, the quasi-Fermi level moves toward the nearest delocalized band edge, with the localized states becoming gradually filled. Above a gate voltage threshold, the injected carriers become free to move, the transport occurring now in a delocalized band resulting in an abrupt increase in mobility. This threshold in gate voltage can be rationalized through a threshold in carrier density for filling all the localized states. This particular state can be generated either by an increase in the gate voltage, which is difficult to achieve in practice, or by an increase in the capacitance C_i , i.e., by an increase in the dielectric constant of the insulator.

Interesting steps have been made in this regard by the research group of IBM Yorktown [69], which performed an elegant analysis of the effect of a large set of high-dielectric amorphous inorganic-based oxides as well as organic polymers (parylene-c), used as insulating layers on a pentacene-based TFT. They confirmed that the carrier mobility increased with the carrier density, easily reaching a value of $0.3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, and that the TFT saturation current was reached for the low gate-voltage value of 5 V, together with a current modulation of 10^5 .

6.5 CONCLUSION

The results described allow the following main conclusions to be drawn:

- 1.) the limiting value for the field-effect mobility in organic semiconductors based on conjugated molecules appears to meet that obtained with the technique of time of flight, of the order of $1\text{--}5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. This value is still about three orders of magnitude lower than that of their inorganic monocrystalline counterparts.
- 2.) On the other hand, it has also been shown that multiple methods exist for the molecular engineering of these molecular semiconductors, leading to highly organized films that show a carrier mobility very close to that of the crystalline state. Mobility values in the range of $0.1\text{--}1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ are within hand, which means that organic semiconductors are able to compete with a-Si:H. Owing to their room-temperature

processing, flexible, lightweight, and large-area devices represent a real opportunity for this new generation of devices.

- 3.) The limit of carrier mobility is still one order of magnitude higher, which means that there is still room to improve the actual experimental mobility values toward that of polycrystalline silicon, which could open up the field of amplifiers and drivers for organic-based TFTs.

Considering the actual state of the art, applications of organic TFTs can be envisioned in fields where conventional inorganic devices do not meet some new required characteristics. Compared to their inorganic counterparts, organic materials present many advantages—low cost, light weight, and room-temperature processing—which should open up the field of low-cost and large-area electronics. Additionally, organic materials present the unique possibility of tuning of their electronic, optical, thermal, and mechanical properties through subtle chemical modifications of their chemical structure. The a priori control of mechanical and optical properties also opens up the possibilities for flexible and even transparent electronics. In fact, a parallel can be made with the field of conventional polymers, whose spectacular development in our everyday life was linked to the possible chemical design of their properties. Although they are at a very early stage, organic-based electronics possess all the bases for à la carte electronics, and thus they promise to have a very interesting future.

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7

Vacuum-Deposited Organic Thin-Film Field-Effect Transistors Based on Small Molecules

Christos D. Dimitrakopoulos

IBM T. J. Watson Research Center, Yorktown Heights,
New York, U.S.A.

7.1 INTRODUCTION

Until recently, organic semiconductors had not had a significant practical impact on optoelectronic applications, although they have been studied for more than half a century [1]. Initially, industrial applications of organic semiconductors were limited to the exploitation of their photoconductive properties in xerography. The broader potential of organic semiconductors for optoelectronics applications has become clear in recent years, with the demonstrations of organic electroluminescent diodes [2,3] and organic thin-film field-effect transistors (OTFTs) [4–6], that continue to improve in performance and efficiency [7,69,8–10]. This chapter will focus on OTFTs that comprise a vacuum-deposited channel. We describe the most commonly used vacuum-deposited organic semiconductors and the various deposition processes, device designs, and applications of OTFTs, emphasizing recent developments. Older papers that have made important contributions to the progress of the OTFT field will also be mentioned, but the early period is covered in more detail in a number of previously published review papers [11–17].

Reported results from single-crystal organic field-effect transistors (OFETs) define the foreseeable upper limits of performance for OTFTs and describe the current understanding of the underlying charge transport mechanism(s). The OTFTs based on vacuum-deposited organic semiconductors with potential for practical applications in large-area electronics will most likely comprise polycrystalline thin-film channels rather than single-crystal channels. The presence of grain boundaries seriously affects charge transport through the channel, but understanding transport through each crystallite is the foundation for elucidating the charge transport mechanism in polycrystalline thin films. Devices with polycrystalline thin-film channels usually have better performance than disordered polymeric OTFT channels, due to the better and more consistent molecular orbital overlap between neighboring molecules in the former compared to the latter, as described later in detail. This has been the driving force behind the extensive use and study of vacuum-deposited polycrystalline OTFT channels.

Organic semiconductors function as either *p*-type or *n*-type channels in OTFTs. In *p*-type organic semiconductors, the majority charge carriers are holes; in *n*-type organic semiconductors, the majority charge carriers are electrons. Reports of *p*-type OTFTs are more common in the literature since they have relatively superior environmental stability. However, in the last decade, several papers on OTFTs based on *n*-type organic semiconductors have appeared, and some of these *n*-type OTFTs are environmentally stable.

The OTFTs are potential viable alternatives to more traditional, mainstream thin-film transistors (TFTs) based on inorganic materials. And OTFTs have relatively low mobility (μ is of the order of $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and cannot rival the performance of field-effect transistors based on single-crystalline inorganic semiconductors, such as Si, Ge, and GaAs, which have charge carrier mobilities (μ) up to three or more orders of magnitude higher [18], or polycrystalline Si films, for which μ is of the order of $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (see [Chap. 4](#)). Consequently, OTFTs are not suitable for use in applications requiring very high switching speeds. However, since organic semiconductors may be processed at low temperatures compatible with plastic substrates, OTFTs may be competitive candidates for novel or even existing TFT applications requiring large-area coverage, structural flexibility, and especially low cost. Such applications include back planes for active-matrix flat panel displays (AMFPDs), based on liquid crystal pixels (AMLCDs) and organic light-emitting diodes (AMOLEDs), and “electronic paper” displays, based on pixels comprising either electrophoretic ink-containing microcapsules [19] or “twisting balls” [20]. Additionally, organic sensors [21], low-end smart cards, radio-frequency identification (RFID) tags, and electronic tickets consisting of organic integrated circuits have been proposed. Each application has different performance requirements for OTFTs. At present, the entrenched technology in large-area electronics applications, especially for back planes of backlit AMLCDs, is based on hydrogenated amorphous silicon (a-Si:H)

TFTs (see [Chap. 5](#)). In contrast to OTFTs, the high processing temperatures used during a-Si:H deposition (ca. 360°C), precludes the fabrication of an AMLCD on a transparent plastic substrate using a-Si:H TFT back planes. This is an application uniquely tailored to OTFT processing.

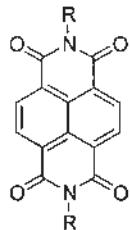
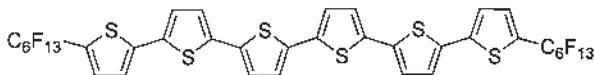
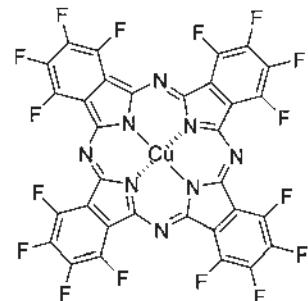
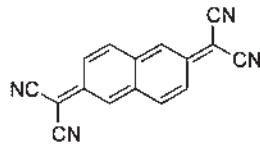
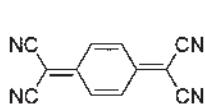
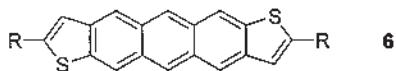
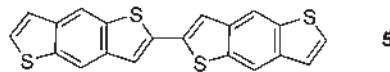
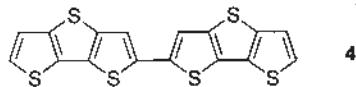
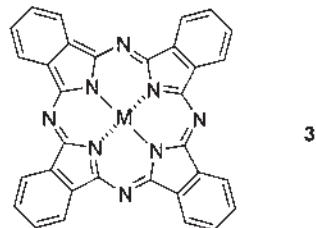
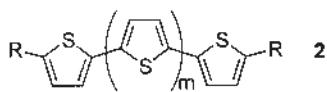
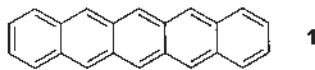
For OTFTs to compete with a-Si:H TFTs in existing applications, they should exhibit device performance characteristic of a-Si:H TFTs, i.e., field effect mobility $\mu = 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, and current modulation (or on/off ratio, $I_{\text{on/off}}$) of 10^6 or higher at a maximum operating voltage of about 15 V. Additionally, they should be environmentally stable for a long time and should not exhibit large threshold voltage shifts.

The best known *p*-type and *n*-type organic semiconductors are shown in [Figure 7.1](#). The numbers representing each molecular structure correspond to the numbers in column 4 of [Tables 7.1](#) and [7.2](#).

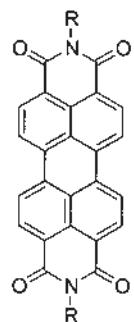
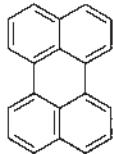
7.2 OTFT FABRICATION METHODS USING VACUUM SUBLIMATION OF ORGANIC MOLECULES

Small-molecule organic semiconductor films can be deposited by sublimation in a variety of vacuum deposition systems utilizing various methods. The deposition parameters can vary widely from method to method. And OTFTs with good charge carrier transport characteristics have been fabricated using most versions of vacuum sublimation and deposition. The base pressure of the deposition system and the pressure during deposition are important process parameters, since they determine, among other things, the mean free path of the sublimed organic semiconductor molecules and the presence of impurity atoms and molecules in the vicinity of the substrate surface during film formation. Base pressure ranges from less than 10^{-9} torr, in ultrahigh vacuum (UHV) organic molecular beam deposition (OMBD) [7a,61,22–25], to about 10^{-7} torr, for common high-vacuum (HV) deposition systems using rubber O-ring seals [26,53–55,93], to more than 1 millitorr, for simple, glass-wall vacuum sublimation systems [27]. Substrate temperature and deposition rate are two other deposition parameters that can dramatically influence thin-film morphology and thus the transport characteristics of OTFTs [61,28].

The purity of the organic source material and the cleanliness of the gate dielectric surface in large part determine the performance of an OTFT. The latter is very important since the carrier accumulation layer is located in the first few monolayers of the organic semiconductor at the interface with the insulator [52,53]. Impurities can affect the mobility, the on/off ratio, and, in some cases, even the polarity of the OTFT. For example, iodine-doped pentacene is a *p*-type semiconductor [29], while alkaline metal-doped pentacene is an *n*-type semiconductor [30].

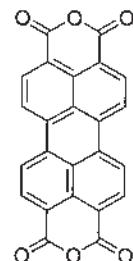


11 $R=CH_2C_7F_{15}$
12 $R=CH_2C_6H_4CF_3$
13 $R=C_8H_{17}$



14

15 $R=C_8H_{17}$



16

In addition to the vacuum sublimation systems, organic sublimation systems that employ a carrier gas for transporting organic molecules from the source to the substrate have also been used [31–34]. Depending on the specific process parameters (carrier gas flow rate, pressure during deposition, organic deposition rate, substrate temperature, etc.) and deposition system design, the method is named either *organic physical vapor growth* (OPVG) [31,32] or *organic vapor-phase deposition* (OVPD). [33,34]. The OPVG technique has been used extensively to form single crystals of organic semiconductors [31,32], whereas OVPD is more appropriate for deposition of polycrystalline or amorphous organic semiconductor thin films [34]. The process parameters normally used in OVPD result in much higher growth rates than the ones employed to form single crystals with OPVG. In this respect, OVPD is better suited for large-scale applications of organic semiconductor film deposition. The pressure during deposition via OVPD is typically below 10 torr [34], but varies with the organic material and the desired properties of the deposited film. One or more organic materials can be deposited on a substrate using a single source or multiple sources, respectively. Usually, the deposition chamber is a Pyrex or quartz tube, inserted in a three-zone furnace. The tube is supplied with carrier gas at one end (where the source is located) and pumped out at the other end (where the substrate is located). The heating element at zone I is used to sublime the source material, and zone II is kept at a temperature that precludes deposition of the source material on the reactor walls. The substrate temperature is adjusted via the heating element of zone III and/or by water-cooling to a temperature that is lower than that of the other two zones so that a film of the desired morphology and structure is deposited [35].

Polymeric organic semiconductors, while commonly deposited by solution-based methods (see [Chap. 9](#)), may also be deposited via vacuum methods. Such a method has been used previously for the vacuum deposition of the insulating polymer poly-(4,4'-oxydiphenylenepyromellitimide). Such polyimide films result from the codeposition and subsequent solid-state reaction of the monomers 1,2,4,5-benzenetetracarboxylic anhydride or pyromellitic dianhydride (PMDA)



Figure 7.1 Molecular structures of common *p*-type and *n*-type organic semiconductors. (1) pentacene; (2) α - ω -dialkyl-oligothiophene, $m = 2$ –6, R = C_nH_{2n+1} , $n = 0$ –8; (3) metal-phthalocyanine; (4) bis(dithienothiophene); (5) bis(benzodithiophene); (6) dialkyl-anthradithiophene; (7) tetracyanoquinodimethane; (8) 11,11,12,12-tetracyanonaphtho-2,6-quinodimethane; (9) Cu-hexadecafluorophthalocyanine; (10) α - ω -diperfluorohexyl-sexithiophene; (11), (12), (13) N-substituted naphthalene-1,4,5,8-tetracarboxylic di-imides (the various substituents are listed in the figure); (14) perylene; (15) *N,N'*-dioctyl-3,4,9,10-perylenetetracarboxylic diimide; (16) 3,4,9,10-perylenetetracarboxylic di-anhydride.

and bis-(4-aminophenyl) ether or oxydianiline (ODA), which is in turn followed by heat-treatment of the film to form the polyimide [36]. In this method, two effusion cells, one containing PMDA and the other ODA, generate two molecular beams that deposit a stoichiometric amount of the two monomers on a rotating substrate, resulting in the formation of a film containing mostly PMDA-ODA dimers that, after annealing, produce a polyimide film [3]. Another deposition method—chemical vapor deposition (CVD) via pyrolysis of a dimer molecule [38]—has been used successfully to deposit poly(*p*-phenylene vinylene) (PPV) films [38,39]. A stream of the sublimed organic dimer is converted to reactive monomer radicals by passing through a high-temperature pyrolysis chamber and then is deposited on a substrate held at or close to room temperature (usually below 100°C) [38,39]. It eventually polymerizes to form a conjugated polymer film upon heating to 200°C in vacuum [39].

7.3 CHARGE TRANSPORT MECHANISMS IN SMALL-MOLECULE ORGANIC SEMICONDUCTORS

The upper limit of microscopic mobilities in organic molecular crystals, measured at 300 K by time-of-flight experiments, falls between 1 and 10 $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, as summarized in Ref. 1. The intermolecular forces in organic semiconductors are typically van der Waals interactions with energies smaller than 10 kcal mol⁻¹. These weak intermolecular interactions may be responsible for this upper limit of charge carrier mobility in organic semiconductor crystals, since the vibrational energy of the molecules approaches the magnitude of the intermolecular “bonding” energies close to room temperature. In contrast, in inorganic semiconductors such as Si, Ge, and GaAs, the atoms are held together by very strong covalent bonds. For example, in the case of Si, the bond energy is as high as 76 kcal mol⁻¹. Charge carriers in single crystals of inorganic semiconductors move as highly delocalized plane waves in wide bands, with very high mobility at room temperature ($\mu \sim 10^3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$). As the temperature increases, their mobility is reduced by lattice vibrations (phonons) that scatter the carriers.

Band transport is not applicable to disordered organic semiconductors, where charge carrier transport takes place by carrier hopping between localized states, where they are scattered at every step. Carrier hopping is a thermally activated process. It is assisted by phonons, and the mobility increases with temperature, though it typically remains very low overall ($\mu \ll 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$). The boundary between band transport and hopping is defined by thin films of materials having room-temperature mobilities on the order of 1 $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [1,16,40]. Polycrystalline thin films of highly ordered organic semiconductors, such as several members of the acene series, including pentacene, have room-temperature mobilities in this intermediate range [64,40,41]. In some cases temperature-independent mobility has been observed [1], such as in some polycrystal-

line thin films of pentacene [40]. This observation was used to argue that a simple thermally activated hopping mechanism can be excluded as a transport mechanism in high-quality polycrystalline thin films of pentacene, despite the fact that in some samples containing a large concentration of traps, related to structural defects and chemical impurities, the mobility increases with temperature [40]. Trapping at the grain boundaries in polycrystalline films of pentacene and the dependence of trap concentration on film deposition conditions has been suggested as the main cause of the observed variability of the temperature dependence of mobility.

Understanding the transport mechanism in single crystals of organic semiconductors facilitates our understanding of transport in the technologically more relevant polycrystalline thin films of these materials. At low temperatures, coherent bandlike transport of delocalized carriers becomes the prevalent transport mechanism in single crystals of pentacene, tetracene, and other acenes. Very high mobility values have been measured using time-of-flight experiments (up to $400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for holes in single crystals of naphthalene at 4.2 K) [42,43]. The hole mobility increases from its room-temperature value of approximately $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ to about $400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 10 K following a power law ($\mu \propto T^{-n}$, $n = 2.79$). This is clear evidence of band transport, at low temperatures, in such crystals. In 1974, Burland observed cyclotron resonance of holes in high-quality single crystals of anthracene at 2 K, the first time such an observation was made in a wide-band-gap molecular crystal [44,45]. From the reported values of the effective mass of holes, m^* , in these crystals, determined to be $11m_e$, where m_e is the free electron mass, and the hole scattering time, τ , measured to be $\sim 7 \times 10^{-11}$ and 4×10^{-10} s, respectively, in two different anthracene crystals, one could calculate hole mobility values of about 11,200 and 64,000 $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, using the formula $\mu = (e/m^*) \tau$, where e is the elementary charge. This was the first time that evidence of such extremely high charge carrier mobility values in organic semiconductors was presented [44].

The temperature dependence of the electron mobility in naphthalene single crystals below 100 K also follows a power law, although with a lower exponent ($\mu \propto T^{-n}$, $n \approx 1.5-1.7$) [42,46,47]. However, between 100 K and 300 K the electron mobility remains practically constant [47,48]. The $\mu(T) = \text{constant}$ region has been described phenomenologically as the superposition of two independent carrier mechanisms. According to one interpretation, the first mechanism is described using the concept of an adiabatic, nearly small molecular polaron (MP) [47]. According to this model the carriers are treated as heavy polaron-type quasi-particles, which are formed as a result of the interaction of the carriers with intramolecular vibrations of the local lattice environment and move coherently via tunneling. In this model the mobility follows the power law $\mu_{\text{MP}} = aT^{-n}$ [47]. The second mechanism involves a small lattice polaron (LP), which moves by thermally activated hopping and thus exhibits a typical exponential dependence

of mobility on temperature: $\mu_{LP} = b - \exp[-E_a/kT]$. The superposition of these two mechanisms can reproduce the experimentally measured temperature dependence of mobility from just a few degrees Kelvin to room temperature [47].

From the work just presented it is apparent that extremely high-quality, ultrapure single crystals of organic semiconductors are required to obtain such high mobilities and observe coherent bandlike transport of delocalized carriers. This behavior is rather impossible to observe in polycrystalline films, in which traps attributed to structural defects, such as grain boundaries, dominate transport.

In the following sections we will discuss carrier transport in various polycrystalline thin films of organic semiconductors, assuming that transport in individual crystallites in the film takes place according to the mechanisms described in this section.

At this point we can propose two possible ways for the elimination of the potential fundamental upper limit of about $10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for the room-temperature mobility of organic field-effect transistors (FETs). One is to strengthen the weak intermolecular forces acting between nearest-neighbor (nn) molecules. This can be done by creating a stronger chemical bond between them. However, this has to take place without breaking the conjugation of the molecules and without reducing the intermolecular overlap between nn molecules. Stronger intermolecular interactions would result in more rigid crystalline structures, and thus it would take temperatures higher than room temperature to generate substantial scattering of highly delocalized carriers by lattice vibrations (phonons). Using such a strategy, one, in effect, could produce, at room temperature, mobility values comparable to the high mobility that exists at very low temperatures in crystals of the acene series, or at least considerably higher than their room-temperature mobilities. The second way involves a drastic change in the conduction path and mechanism. It involves carrier transport via a single molecule or an array of parallel molecules, such as polymer chains or shorter molecules, whose length would bridge the gap between the source and drain electrodes of an FET. In such devices, intermolecular transport, which is the transport mechanism in traditional organic FET devices, is replaced by intramolecular transport. This would require a severe reduction in the size of the FET channel from microns to nanometers so that it becomes shorter than the length of a single molecule. Successful implementations of any one of the strategies just described could demonstrate that the presently foreseeable performance limit in organic FETs (OFETs) is partially imposed either by the specific choice of organic molecule and the structure of the layer that it forms or by the design of the OFET device (specifically the relation of the length of its channel vs. the length of the specific organic molecule used) and is not due to a general and fundamental property of all organic molecules.

7.4 ORGANIC TRANSISTOR OPERATION AND MODELING

Figure 7.2 shows two common device configurations used in OTFTs. The I–V characteristics of OTFTs can be adequately described by models developed for inorganic semiconductors [49], as shown earlier [7a,14,16,61,50,51]. Polycrystalline pentacene OTFTs are used here to demonstrate typical I – V characteristics of OTFTs and the methods used to calculate the field-effect mobility and other device parameters, such as the current modulation (the ratio of the current in the accumulation mode, I_{on} , over the current in the depletion mode, I_{off} , also referred to as I_{on}/I_{off} ratio), and the threshold voltage, V_T . Polycrystalline pentacene OTFTs exhibit *p*-type behavior (the majority carriers are holes). Thus, when the gate electrode is biased positively with respect to the grounded source electrode, they operate in the depletion mode, and the channel region is depleted of carriers, resulting in high channel resistance (off-state). When the gate electrode is biased negatively, they operate in the accumulation mode and a large concentration of carriers is accumulated in the transistor channel, resulting in low channel resistance (on-state). For *n*-type TFT operation, the electrode polarity is reversed and the majority carriers are electrons instead of holes. The accumulation layer is

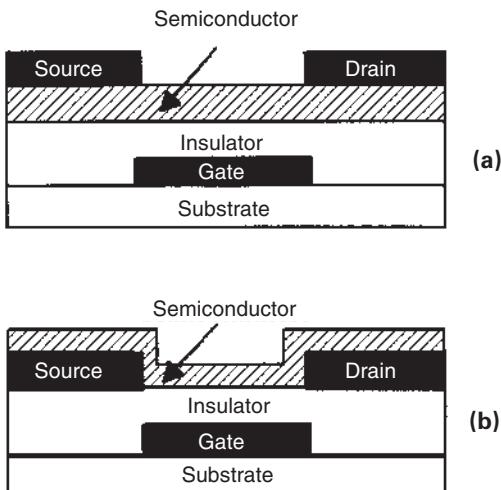
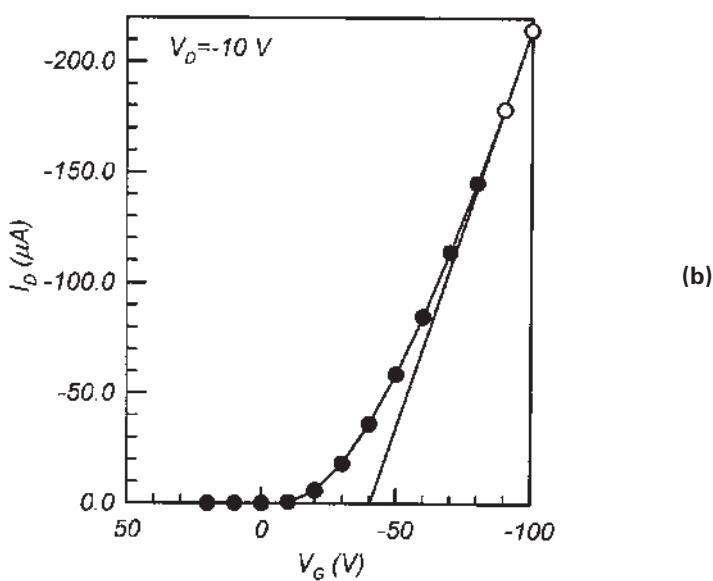
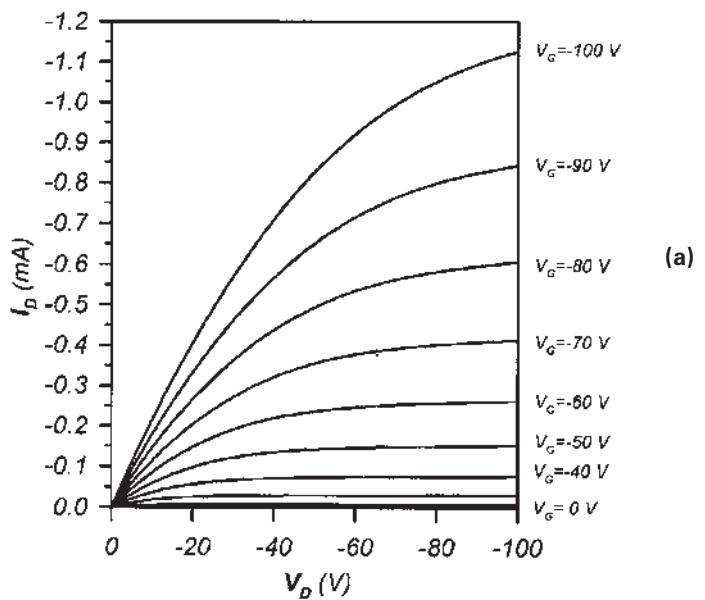


Figure 7.2 OTFT device configurations: (a) Top-contact device, with source and drain electrodes evaporated onto the organic semiconducting layer. (b) Bottom-contact device, with the organic semiconductor deposited onto the gate insulator and the previously fabricated source and drain electrodes.



limited to the first few organic monolayers at the organic semiconductor/insulator interface, since it has been shown that organic layer thickness equivalent to only few such monolayers is sufficient for proper transistor operation and that additional film thickness does not substantially increase I_{on} [52,53].

A typical plot of drain current I_D versus drain voltage V_D at various gate voltages V_G is shown in [Figure 7.3a](#), which corresponds to a top-contact OTFT ([Fig. 7.2a](#)) using a polycrystalline pentacene film as the semiconductor, 5000-Å thermally grown SiO_2 as the gate insulator, a heavily doped n -type Si wafer as the gate, and gold source and drain electrodes. At low V_D , I_D increases linearly with V_D (linear regime) and is approximately determined from the following equation:

$$I_D = \frac{WC_i\mu}{L} \left(V_G - V_T - \frac{V_D}{2} \right) V_D$$

where L is the channel length, W is the channel width, C_i is the capacitance per unit area of the insulating layer, V_T is the threshold voltage, and μ is the field-effect mobility. The field-effect mobility can be calculated in the linear regime from the transconductance,

$$g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D=\text{const.}} = \frac{WC_i}{L} \mu V_D$$

by plotting I_D versus V_G at a constant low V_D , with $-V_D \ll -(V_G - V_T)$ and equating the value of the slope of this plot to g_m . [Figure 7.3b](#) shows such a plot of I_D versus V_G at $V_D = -10$ V. The calculated linear mobility value is $0.53 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The value of V_D is chosen so that it lies in the linear part of the I_D versus V_D curve. The channel dimensions were $L = 15.4 \mu\text{m}$ and $W = 1.5 \text{ mm}$. This device was stored in a nitrogen box for more than 2 years before it was tested.

Figure 7.3 (a) Plot of drain current I_D versus drain voltage V_D at various gate voltages V_G from a top-contact OTFT using a polycrystalline pentacene film as the semiconductor, 5000-Å thermally grown SiO_2 as the gate insulator, a heavily doped n -type Si wafer as the gate, and gold source and drain electrodes. The channel dimensions were $L = 15.4 \mu\text{m}$ and $W = 1.5 \text{ mm}$. (b) Plot of I_D versus V_G at $V_D = -10$ V for the same device. The calculated linear mobility value is $0.53 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The value of V_D is chosen so that it lies in the linear part of each I_D versus V_D curve in [Figure 3a](#).

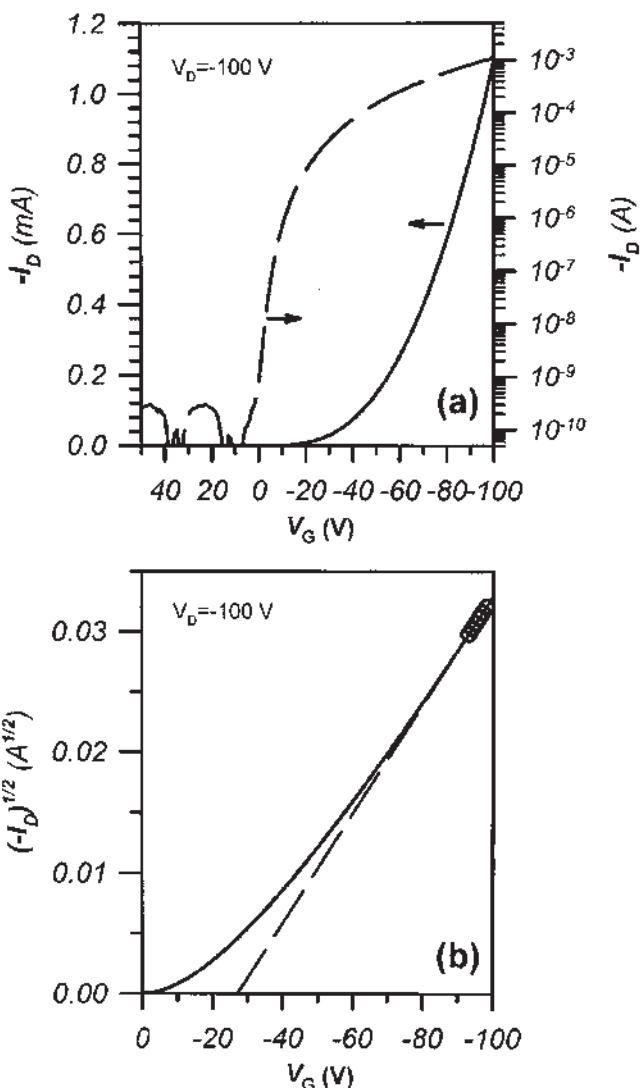


Figure 7.4 (a) Semilogarithmic plot of I_D versus V_G (right axis) and linear plot of $|I_D|$ versus V_G (left y-axis) from the same device as in [Figure 7.3](#) (b) Plot of $\sqrt{|I_D|}$ versus V_G corresponding to the same device. The field-effect mobility μ , calculated in the saturation regime, is $0.64 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at $V_D = -100 \text{ V}$.

For $-V_D > -(V_G - V_T)$, I_D tends to saturate (saturation regime) (Fig. 7.3a) due to the pinch-off of the accumulation layer, and is modeled by the equation

$$I_D = \frac{WC_i\mu}{2L}(V_G - V_T)^2$$

Figure 7.4a shows a graph that contains plots of I_D (left y-axis) and $\log(-I_D)$ (right y-axis) versus V_G at a constant $V_D = -100$ V (saturation regime), from the same device as in Figure 7.3. In the saturation regime, μ can be calculated from the slope of the plot of $\sqrt{|I_D|}$ versus V_G (Figure 7.4b). The mobility calculated in the saturation regime was $0.64 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is slightly larger than the linear regime mobility. This result is comparable to reported hole mobilities from OTFTs with polycrystalline pentacene film channels grown on SiO_2 using a substrate temperature (T_{sub}) of 120°C during deposition. [54] The $I_{\text{on}}/I_{\text{off}}$ ratio was approximately 10^7 for a V_G sweep from -100 to $+5$ V. The turn-on voltage for this device was less than about $+5$ V. It is important to note that the W/L ratio must be at least 10 in order to minimize the effects of fringe currents flowing outside the channel on the calculated mobility value; otherwise this value is overestimated. Alternatively, accurate mobility measurements could be obtained by patterning the semiconductor layer such that its width does not exceed the width W of the OTFT channel.

The mobility values of pentacene OTFTs most often reported in the literature are calculated in the saturation regime [63,64,40,54]. Typically, the mobility calculated in the saturation regime is much higher than the mobility calculated in the linear regime, because the linear-regime mobility is more negatively affected by departures from linearity in the I_D versus V_D curves, at low V_D . Gold and other metals with even higher work functions (e.g., Pd, Pt) that are most commonly used for source and drain contacts in *p*-type OTFTs form ohmic contacts with pentacene, in the top-contact configuration at least (Fig. 7.2a), as expected by comparing gold's work function to the valence-band (or HOMO) energy level of pentacene crystals. The large differences between the two mobilities in polycrystalline pentacene OTFTs could, however, arise from the existence of a large concentration of trap states in the TFT channel (e.g., related to grain boundaries).

7.5 ORGANIC TRANSISTOR PERFORMANCE

7.5.1 Progress in Performance of *p*-Type OTFTs

Table 7.1 lists the highest field-effect mobility (μ) values measured from *p*-type OTFTs as reported in the literature, annually from 1984 to the present time, for each one of the most promising *p*-type organic semiconductors. For each *p*-type

TABLE 7.1 P-type OTFTs

Year	Mobility ^a (cm ² V ⁻¹ s ⁻¹)	Material	Compound no.	$\frac{I_{ON}^b}{I_{OFF}}$	$\frac{W}{L}$	Ref.
1964	NR ^c	Cu-phthalocyanine (first demonstration of field effect in small organic molecules)	3	NR	NR	55
1984	1.5×10^{-5}	Merocyanine		NR	7000	5
1988	10^{-3}	Phthalocyanine	3	NR	3	56
1989	10^{-3}	α -Hexathiophene	2, <i>m</i> = 4	NR	NR	57
1992	0.027	α -Hexathiophene	2, <i>m</i> = 4	NR	100	58
	2×10^{-3}	Pentacene	1	NR	NR	58
1993	0.05	α - ω -Dihexyl- hexathiophene	2, <i>m</i> = 4	NR	100–200	59
1994	0.06	α - ω -Dihexyl- hexathiophene	2, <i>m</i> = 4	NR	50	60
1995	0.03	α -Hexathiophene	2, <i>m</i> = 4	$>10^6$	21	53
	0.038	Pentacene	1	140	1000	61
1996	0.02	Phthalocyanine	3	2×10^5	NR	62
	0.62	Pentacene	1	10^8	11	63
1997	1.5	Pentacene	1	10^8	2.5	64
	0.13	α - ω -Dihexyl- hexathiophene	2, <i>m</i> = 4	$>10^4$	7.3	7a
	0.04	Bis(benzodithiophene)	5	NR	NR	65
	0.05	Bis(dithienothiophene)	4	10^8	500	66
1998	0.23	α - ω -Dihexyl- quaterthiophene	2, <i>m</i> = 2	NR	1.5	67
	0.15	Dihexyl- anthradithiophene	6	NR	1.5	68

^a Measured at room temperature.^b Values for I_{on}/I_{off} correspond to different gate voltage ranges and thus are not thus are not readily comparable to one another.^c NR = not reported.

organic semiconductor that already has a data entry in Table 7.1 and Figure 7.5 for a previous year, a new mobility value is entered only if it is higher than the value of the preceding entry. There is an impressive increase in mobility, which is the result of either improvements in the processes used for the fabrication of OTFTs or the synthesis of new organic semiconductor materials. A typical path to performance increase could be described as a three-stage process: (1) a new organic semiconductor is synthesized or a known one is used for the first time

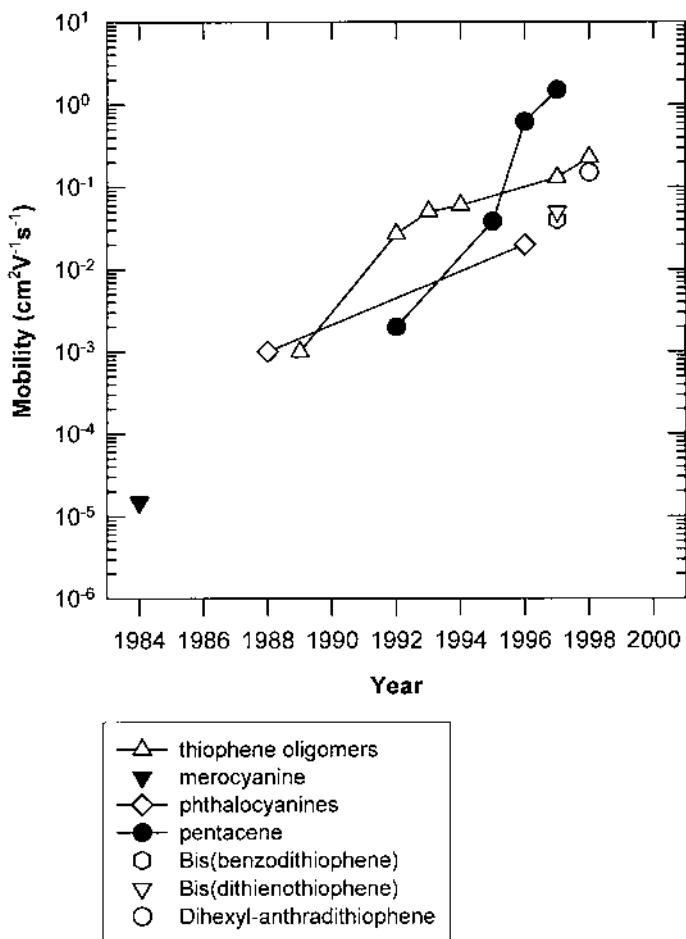


Figure 7.5 Evolution of field-effect mobility of holes measured from OTFTs based on the most common *p*-type organic semiconductors. The various *p*-type materials are grouped together into classes of similar molecules using as a classification criterion only the core part of each molecule.

as the active layer in an OTFT; (2) the film deposition parameters for the semiconducting organic layer are optimized to obtain the most advantageous structural and morphological characteristics for improved performance until no further improvement seems possible; (3) injection from the source and drain contacts is optimized. After this point, another incremental improvement in mobility is usually obtained from the synthesis and/or first OTFT application of a new organic semiconductor. Today, the field has reached an important point in the performance versus time plot. The most widely used organic semiconductors, such as pentacene, thiophene oligomers, and regioregular poly(3-alkyl-thiophene), seem to have reached “maturity” in their performance. Their individual performance versus time curves seem to have saturated (when a new, higher value is not reported in the years following the last entry for a material, it means that there was no improvement in mobility during those years). In the past, each time such a performance saturation occurred, a new material was introduced whose performance broke the temporarily established upper limit in performance (see, for example, the mobility vs. time curve for OTFTs based on oligothiophene oligomers in [Fig. 7.5](#) and the emergence of pentacene OTFTs at the time that the performance of the former started to saturate).

The synthesis, fabrication, and characterization of OTFTs based on polycrystalline, vapor-deposited α - ω -hexathiophene [57,58] and α - ω -dihexyl-hexathiophene [59] films by Garnier, Horowitz, and coworkers played a very important role in the evolution of the field of organic transistors, as evidenced by the large number of entries in [Table 7.1](#). That work showed that relatively high mobilities are attainable in TFTs having polycrystalline organic semiconductors as the semiconducting channel. Later, the work of Dodabalapur, Torsi, and Katz showed that OTFTs with current modulation of 10^6 were attainable by carefully purifying the evaporation source material [53]. Note that OTFTs based on thiophene oligomers are covered in detail in [Chapter 6](#).

Pentacene thin-film transistors (TFTs) have produced the highest field-effect mobility values reported for OTFTs. From 1992 (first use of pentacene in an OTFT) [58] to 1997 the mobility was raised from 2×10^{-3} [58] to 0.038 [61] to 0.62 [63] to 1.5 [64] $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. Today’s maximum hole field-effect mobility lies in the range expected for the room-temperature field-effect mobility for holes in single crystals of the acene series ($1\text{--}10 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, see discussion in previous section).

7.5.2 Relation Between Morphology and Electrical Properties

The fabrication of OTFTs based on polycrystalline, vapor-deposited α -hexathiophene [57,58] and α - ω -dihexyl-hexathiophene [59] films by Garnier et al. not only showed that relatively high mobilities are attainable in TFTs having poly-

crystalline organic semiconductor channels, but also delineated the strategies that should be followed in order to increase the performance of OTFTs. In the case of chain- or rodlike molecules, such as thiophene oligomers, large π -conjugation length along the long axis of the molecule and close molecular packing of the molecules along at least one of the short molecular axes (π -stacking) are two important conditions for high carrier mobility. Carrier transport is easiest parallel to the π -stacking direction, thus this direction should be parallel to the gate insulator surface in OTFTs, which means that each molecule should be positioned with its long molecular axis almost perpendicular to this surface. α - ω -Dihexylhexathienophene films grow with the molecules oriented almost perpendicular to the substrate surface. There is also a large anisotropy in conductivity between the directions parallel and perpendicular to the π -stack (and therefore the substrate surface), with the conductivity being much higher parallel to the π -stack.

These principles are also important in the operation of OTFTs based on polycrystalline, vapor-deposited pentacene thin films [58,61,63,64]. [Figure 7.6](#)[69] contains proof of the foregoing claims. By growing amorphous films of pentacene, which is achieved by keeping the substrate temperature at -196°C during deposition, a film that is practically insulating is produced [61]. The overlap of the molecular orbitals of nearest-neighbor molecules is very limited because of the disorder in the solid. When the substrate temperature is kept at room temperature (27°C) during deposition, a highly ordered film is deposited and the mobility measured at room temperature is $0.6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. [69] The well-defined X-ray diffraction peaks correspond to $(00l)$ reflections, with a d -spacing of about 15.4 \AA , which corresponds to a crystalline structure with the long axis of the pentacene molecule being almost perpendicular to the substrate surface. The structure of this thin film is different than the structure of single crystals of pentacene; thus we must distinguish between the “thin-film phase” [61,28] and the “single-crystal phase” [70] of pentacene. One of the main differences between these phases is in the d -spacing of the $(00l)$ reflections. It is slightly smaller (14.5 \AA) in the “single-crystal phase”; thus in this phase the long axis of the pentacene molecule makes a larger angle with the substrate surface normal than in the “thin-film phase.” When a mixture of the thin-film phase and the single-crystal phase is grown [61] at higher deposition temperatures, the mobility is very low, possibly due to the high defect concentration resulting from the coexistence of the two phases. It is important to mention again here that the resulting film morphology is also dependent on the deposition rate. Hence, both parameters (temperature and deposition rate) have to be controlled accurately when trying to produce a specific morphology. In the earlier discussion, the deposition rate was controlled within a narrow range ($0.025 \text{ nm/s} < \text{DR} < 0.1 \text{ nm/s}$), in order to isolate the effects of substrate temperature on film morphology. The single-crystal phase is favored by higher substrate temperatures and lower deposition rates.

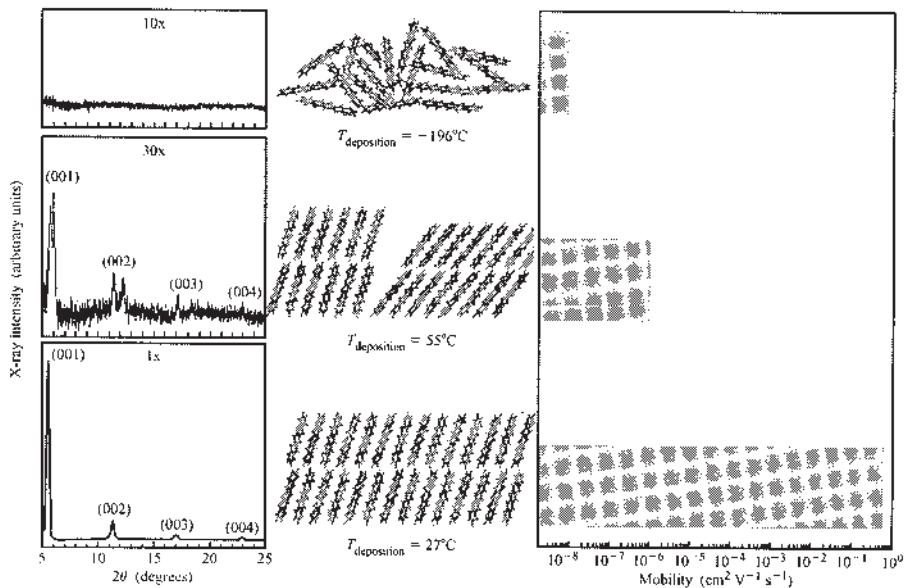


Figure 7.6 X-ray diffractograms, schematic representations of structural order, and field-effect mobilities, corresponding to three different thin films of pentacene. *Top:* An amorphous phase was deposited using a low substrate temperature ($T_{\text{sub}} = -196^{\circ}\text{C}$) and a deposition rate, DR, of 0.5 \AA s^{-1} . *Bottom:* A single “thin film phase” was deposited at $T_{\text{sub}} = 27^{\circ}\text{C}$ and DR = 1 \AA s^{-1} . *Middle:* At $T_{\text{sub}} = 55^{\circ}\text{C}$ and with DR = 0.25 \AA s^{-1} , a film consisting of two phases, the “thin-film phase” and the “single-crystal phase,” was deposited. (Reprinted from Ref. [69]. Original structural data was partially published in Ref. [61].)

Figure 7.7 shows the morphology of a pentacene film grown on SiO_2 at room temperature [71]. We observe that pentacene forms single-crystal islands with a size up to more than 1 micron. Subsequent layers growing on top of these islands are smaller in size, leading to a terrace-and-step morphology. Similar morphology is observed even when a self-assembled monolayer of a molecule such as the 1-diethoxy-1-silacyclopent-3-ene is grown on the SiO_2 surface [72]. The angles formed by the sides of some of the uppermost pentacene islands are consistent—at the extent of accuracy that the photograph permits—with the angles of the **ab** plane of the triclinic unit cell of pentacene [70]. Recently, photoelectron emission microscopy (PEEM) was employed to study pentacene thin-film growth in real time, and the resulting understanding contributed significantly to

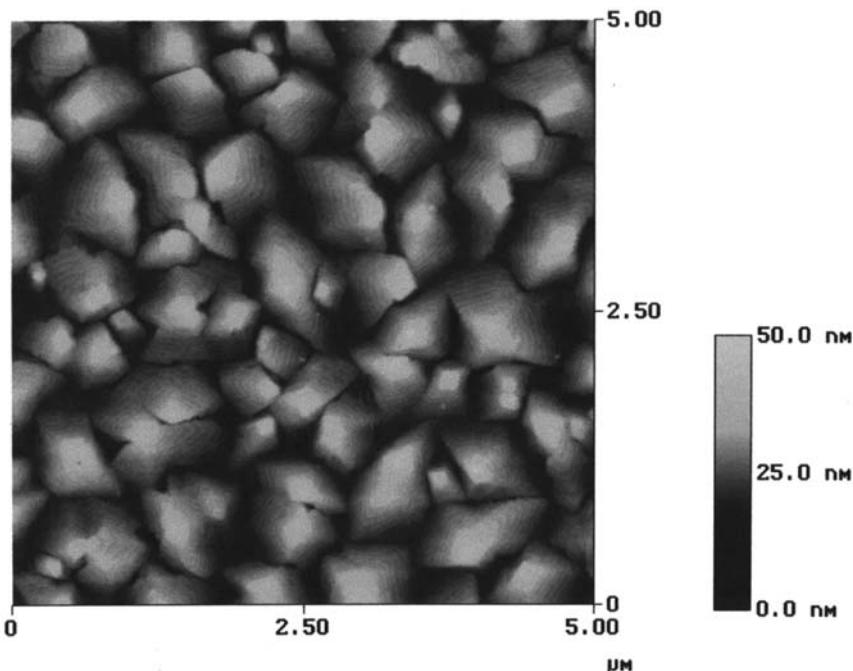


Figure 7.7 Morphology of a pentacene thin film grown at room temperature on SiO_2 , as shown in a $5\text{-}\mu\text{m} \times 5\text{-}\mu\text{m}$ AFM micrograph. The grayscale of the height bar corresponds to a range of 50 nm.

the identification of the pentacene growth mechanism on various surfaces [73]. Polycrystalline films of pentacene with grain sizes approaching $100\text{ }\mu\text{m}$ were fabricated on clean Si(001) surfaces passivated with a cyclohexene layer [73]. Such large grain growth can be attributed to the relatively low nucleation density of pentacene grains on the surfaces used and under the conditions used, which is of the order of $10^{-3}\text{ }\mu\text{m}^{-2}$, and to the absence of heterogeneous nucleation sites on the carefully cleaned Si substrates [73]. The nucleation density of pentacene grains on SiO_2 was reported to be 100 times higher than on Si(001) and cyclohexene-modified Si(001) surfaces, under the same deposition conditions [73]. Higher nucleation density generally translates to smaller grain sizes.

In two other interesting reports, the effect of the gate-insulator surface structure on the order and orientation of pentacene [74,75] and other organic semiconductor [75] films and the effects on device performance were investigated.

7.5.3 Dependence of Mobility on Gate Voltage

As mentioned earlier, up to the present time, pentacene OTFTs have shown the highest hole mobilities among TFTs with an organic semiconducting channel (see [Table 7.1](#)). However, the operating voltage required to produce such performance (approximately 100 V) is often considered too high, especially for portable, battery-powered device applications. The required maximum voltage depends on the thickness of the gate insulator, but because the subject matter of OTFT applications is large-area electronics, we should take into account that there is a minimum in the thickness of the gate insulator, imposed by reliability considerations such as the requirement for pinhole-free films with good step coverage and low leakage currents. It would probably be impractical to reduce the thickness of the dielectric below 100 nm, with a more realistic thickness being 300 nm. We have studied the gate-voltage dependence of the mobility of pentacene devices and used our understanding to demonstrate high-performance pentacene TFTs exhibiting mobility up to $0.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at low operating voltages ($\sim 5 \text{ V}$) [[41,76sa](#)].

In order to lower the operating voltage of pentacene OTFTs we have employed gate insulators with a relatively high dielectric constant (ϵ), such as metal oxide films of barium zirconate titanate (BZT) [[41](#)] or barium strontium titanate (BST) [[76](#)]. Additionally, we have demonstrated the full compatibility of low-operating-voltage OTFTs with transparent plastic substrates by making devices on polycarbonate substrates using an all-room-temperature process sequence [[41](#)]. Later, Gundlach et al. demonstrated pentacene OTFT devices on plastic with mobility up to $1.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at an operating voltage of about 25 V [[77](#)].

[Figures 7.8a](#) and [7.8b](#) show the dependence of field-effect mobility, μ , on the charge per unit area on the semiconductor side of the insulator, Q_s , and the gate field, E , respectively [[76](#)]. Both E and Q_s are proportional to V_G . The black circles correspond to a pentacene-based device with a 1200-Å-thick SiO_2 gate insulator thermally grown on the surface of a heavily doped *n*-type Si wafer that acted as the gate electrode. The open circles correspond to a similar device with a 5000-Å-thick SiO_2 gate insulator. The mobility for the SiO_2 -based devices is calculated in the saturation regime using a gate sweep, as explained in [Figure 7.4](#), and is then plotted against the maximum V_G used in each gate sweep. The maximum V_G is varied from -20 to -100 V . During all sweeps, V_D is kept constant at -100 V in order to eliminate any effects that source and drain contact imperfections might have on our results. The mobility increases linearly with increasing Q_s and E and eventually saturates ([Figs. 7.8a and 7.8b](#), respectively). Q_s is a function of the concentration of accumulated carriers in the channel region (N). Since the accumulation region has been shown in the past to be two-dimensional and confined very close to the interface of the insulator with the organic semiconductor [[52,53](#)], all of this charge is expected to be localized within the first few semiconductor monolayers from this interface, screening the field out

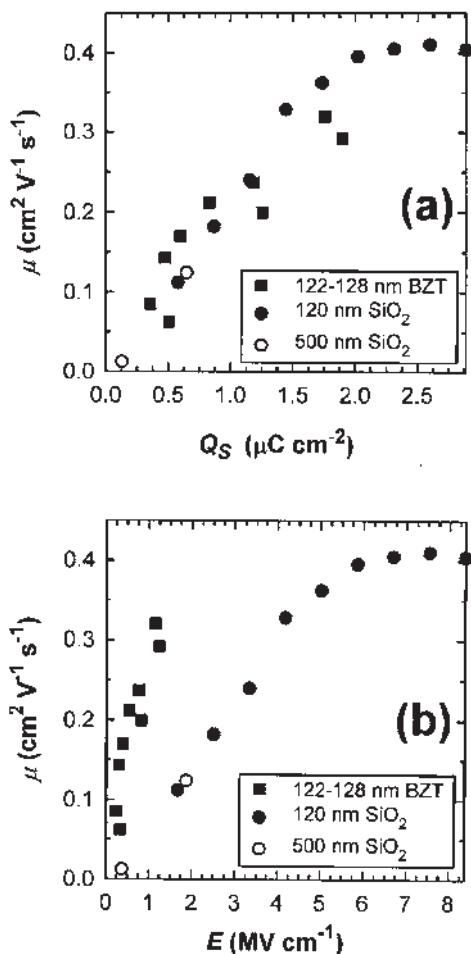


Figure 7.8 (a) Dependence of field-effect mobility of holes, μ , on charge per unit area, Q_S . (b) Dependence of μ on gate field, E . 500-nm-thick thermally grown SiO_2 (open circles); 120-nm thermally grown SiO_2 (filled circles); 122–128-nm-thick sputtered BZT (filled rectangles). (Adapted from Ref. 76.)

of the rest of the pentacene thickness. By replacing SiO_2 with an insulator having a similar thickness but a much higher dielectric constant, an accumulated carrier concentration similar to the SiO_2 case could be attained at much lower V_G , and hence E , with all the other parameters being similar. The black squares in [Figure 7.8](#) correspond to devices comprising a room-temperature sputtered BZT film as the gate insulator, with a thickness between 1220 and 1280 Å. From [Figure 7.8b](#) it is obvious that in devices with a BZT gate insulator, the applied gate field used to obtain mobility values similar to those of the devices with a SiO_2 gate insulator was about five times lower. High fields are not required to obtain high mobility. Thus, the gate-voltage dependence of mobility in these devices is due to the higher concentration of holes accumulated in the channel. [Figure 7.8a](#), which plots μ against charge per unit area, Q_s , corroborates this conclusion. The values of Q_s and N required to reach a certain mobility value are practically the same for devices with SiO_2 and BZT gate insulators, although very different gate voltages and gate fields were required to obtain this mobility in each case.

The gate-voltage dependence of vacuum-deposited pentacene OTFTs was first reported in Ref. 61. A similar behavior was later reported for pentacene OTFTs deposited from solution via a tetrachlorobenzene-containing precursor of pentacene [78]. The multiple trapping and release (MTR) model [80], which is widely used to model the behavior of a-Si:H TFTs, explains reasonably well the observed characteristics in vapor-deposited polycrystalline films of pentacene. This model, which is based on the assumption that the intrinsic charge transport mechanism is one involving extended states, has been successfully used in the past to model the field dependence of mobility in α -6T and DH6T OTFTs [16,41,76,80–82]. According to this model, a distribution of traps exists in the forbidden gap above the valence-band edge. At low gate bias, most of the holes injected in the semiconductor are trapped into these localized states. The deepest traps are filled first and carriers can be released thermally. As the negative gate bias increases, the Fermi level approaches the valence-band edge as more traps are filled (*p*-type material). At an appropriately high gate voltage, all trap states are filled and subsequently injected carriers move with the microscopic mobility associated with carriers in the delocalized (valence) band [41,76]. Several trap levels have been reported for thin polycrystalline vapor-deposited films of pentacene at depths ranging from 0.06 eV to 0.68 eV [83], which could account for the traps described in the MTR model. Traps can be linked to impurities and various structural defects in the crystalline structure of the pentacene film, including point defects, dislocations, and most importantly grain boundaries [84]. The concept of charged grain boundaries has been used to explain the gate-voltage dependence of mobility in polycrystalline oligothiophene [82,85] films. An energy barrier is created at the grain boundaries and is a function of the charged trapping states at the boundaries, the carrier concentration within the grains, and

the temperature. The effective mobility in a polycrystalline organic semiconductor film is given by

$$\frac{1}{\mu} = \frac{1}{\mu_G} + \frac{1}{\mu_{GB}}$$

where μ_G is the single-crystal mobility (intragrain mobility) and μ_{GB} is the mobility across the grain boundary [82,85]. At high temperatures the charge transport is dominated by thermionic emission over the potential barrier at the grain boundary. At low temperatures transport is dominated by tunneling of charge carriers through the potential barrier at the grain boundary. Chwang and Frisbie have shown that carrier transport in α,ω -dihexyl-hexathiophene (6T) OTFTs is limited by the presence of grain boundaries in the channel [86]. Their experiments involved transport measurements through single grain boundaries in vapor-deposited 6T and showed that transport is dependent on carrier concentration exhibiting decreasing activation energy with increasing carrier concentration. Another important conclusion of that work is that larger threshold voltages in OTFTs correlate with larger trap densities at grain boundaries [86].

In the case of OTFTs comprising amorphous organic semiconductor channels, the experimentally obtained gate-voltage and temperature dependence of the field-effect mobility has been studied and successfully modeled theoretically [87]. The mobility dependence on temperature in such OTFTs exhibits a simple Arrhenius behaviour, with a gate-voltage-dependent activation energy. Yu et al. have proposed a model that successfully explains field and carrier density dependences of the mobility in films of conjugated organics, both in low-field/high-carrier-concentration cases (OTFTs) and in high-field/low-carrier-concentration cases (organic diodes). Their model was based on the assumptions that thermal fluctuations modify the energy levels of polaronic electronic states and that the primary restoring force for these fluctuations is steric, which leads to spatial correlation in the energies of the localized electronic states [88].

7.5.4 Effects of Device Configuration on Pentacene Transistor Performance

Pentacene transistor drain–source contacts can be made in one of two configurations, as discussed before (Figs. 7.2a and 7.2b): top-contact and bottom-contact. It is well established that the performance of pentacene devices with the bottom-contact configuration is inferior to that of devices with the top-contact configuration. Consequently, most high-performance pentacene TFTs reported in the literature have the top-contact configuration, and shadow masking is generally used to pattern the source and drain contacts on top of the pentacene. Unfortunately, this is a process that cannot be used in manufacturing; hence a protocol that allows the patterning of the source and drain electrodes on the insulator before

the deposition of pentacene, according to the schematic shown in [Figure 7.2b](#), had to be developed. This should be done either with photolithography or with some other patterning technique, such as microcontact printing, stamping, or screen-printing. Furthermore, the performance of devices fabricated with such a process should be similar to if not better than that of top-contact devices ([Fig. 7.2a](#)).

[Figure 7.9](#) shows a pentacene layer as it was grown on SiO_2 and a Au electrode [89]. The edge between SiO_2 and Au is marked by the end of the white area in the middle photograph that corresponds to Au (due to variations in image contrast, the pentacene-covered Au appears different in the top two pictures). On SiO_2 , far away from the Au edge, pentacene consists of fairly large grains (having sizes between 0.2 and 0.5 μm) (bottom photograph). On Au, the grain size is dramatically reduced (top photograph). This small crystal growth persists into the channel region (on SiO_2) [89–91]. Close to the Au edge, but on the SiO_2 side, there is a transition region where the grain size increases with increasing distance from the edge (middle photograph). It is the morphology of the pentacene film in the OTFT channel region close to the electrode edge that causes the performance limitation of the bottom-contact TFT. Right at the edge of the Au electrode, there is an area with very small crystals and thus a large number of grain boundaries. Grain boundaries are high-volume and low-order regions that contain many morphological defects, which in turn are linked to the creation of charge carrier traps with levels lying in the band gap. The creation of an unusually large concentration of defects in the region of the channel close to the electrode edge can be considered responsible for the reduced performance of bottom-contact pentacene TFTs. The reduction of their concentration to levels similar to those in the area at the center of the channel (lower part of [Fig. 7.9](#)) should result in bottom-contact devices with performance similar to or better than that of top-contact devices. In a typical bottom-contact pentacene TFT, the mobility is equal to or less than $0.16 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. We have used a self-assembled monolayer (SAM) of 1-hexadecanethiol to modify the surface energy of the Au electrode in an effort to improve the crystal size and ordering of the overgrown pentacene layer [91,92]. Mobilities calculated in saturation from such devices were up to $0.48 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is three times larger than the mobility of devices with untreated Au electrodes. Mobilities calculated in the linear regime were up to five times higher in devices treated with a SAM vs. untreated devices [91]. The pentacene layers for both devices were deposited in the same deposition run. [Figure 7.10](#) provides an explanation for the improvement in device performance [91]. The SAM deposited on Au resulted in a pentacene grain size on Au similar to the large grains grown on the SiO_2 in the center of the channel. There is no transition region at the Au edge; hence the trap concentration must have been drastically reduced.



Figure 7.9 SEM micrograph depicting the morphology of a pentacene layer grown on SiO₂ and a Au electrode (bottom-contact device configuration). *Top micrograph:* Pentacene on a polycrystalline Au layer. *Bottom micrograph:* Pentacene on a thermally grown SiO₂ layer. The grain size of pentacene is much smaller on Au than on SiO₂, far from the Au edge. *Middle micrograph:* Pentacene growth on both sides of the Au electrode edge. The pentacene grain size on SiO₂ in the region close to the Au edge is similar to that on the Au electrode, but it increases with increasing distance from the edge. (Adapted from Ref. [89].)

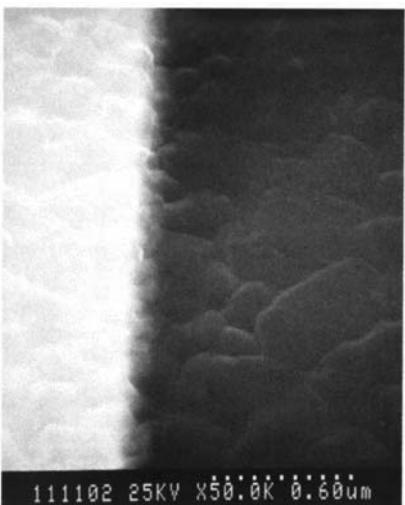


Figure 7.10 SEM micrograph depicting the morphology of a pentacene layer grown on SiO_2 and a Au electrode covered with a SAM of 1-hexadecane thiol. A similar grain size on both the SiO_2 and the Au/SAM surface is observed. The pentacene grain size transition region on SiO_2 in the region close to the Au edge (see Fig. 7.9) is eliminated. (Reprinted from Ref. [91], © 2001 IEEE.)

7.5.5 Progress in Performance of *n*-Type OTFTs

Reports of *n*-type OTFTs started appearing in the literature about 1990. Table 7.2 lists the highest field-effect mobility (μ) values measured from *n*-type OTFTs as reported in the literature, annually from 1990 to the present time, for each one of the most promising *n*-type organic semiconductors. Figure 7.11 conveys graphically most of the information contained in Table 7.2. The various *n*-type materials are grouped together, when possible, considering only the core part of each molecule and not the specific substituents.

Early papers reported some *n*-type OTFTs that had respectable performance, but they were unstable in air. Some materials provided devices with limited air stability, but charge transport properties were poor. More recently, researchers have been able to fabricate *n*-type OTFTs with fairly high mobility and current modulation as well as air stability.

An early study on *n*-type OTFTs was reported by Guillaud and coworkers and involved lutetium (Pc_2Lu) and thulium (Pc_2Tm) bisphthalocyanines [93]. In vacuum, electron mobilities between 2×10^{-4} and $1.4 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$

TABLE 7.2 N-type OTFTs

Year	Mobility ^a (cm ² V ⁻¹ s ⁻¹)	Material	Compound no.	$\frac{I_{ON}^b}{I_{OFF}}$	$\frac{W}{L}$	Ref.
1990	2×10^{-4}	Pc ₂ Lu		NR ^c	20	93
	1.4×10^{-3}	Pc ₂ Tm		NR	20	93
1993	5×10^{-4}	C ₆₀ /C ₇₀ (9:1)		NR	16,000	95
1994	3×10^{-5}	TCNQ	7	450	2,000	94
1995	0.08	C ₆₀		10^6	400	96
	0.3	C ₆₀		22	400	96
1996	1.5×10^{-5}	PTCDI-Ph		NR	100	108
	0.003	TCNNQ		NR	NR	98
	10^{-4}	NTCDI		NR	NR	98
	0.003	NTCDA		NR	21	98
1997	$10^{-41}\text{--}10^{-5}$	PTCDA	16	NR	21	109
1998	0.03	F ₁₆ CuPC	9	5×10^4	21	114
2000	0.06	NTCDI-C ₈ F	11	10^5	17	100
	0.1	NTCDI-C ₈ F	11	10^5	1.5	100
	0.12	NTCDI-BnCF ₃	12	NR	17	99
	0.16 ^d	NTCDI-C ₈ H	13	>100	17	99, 100
2001	0.02	DFH-6T	10	10^5	20	116
	0.6	PTCDI-C ₈ H	15	10^5	16	27

^a Measured at room temperature.^b Values for I_{on}/I_{off} correspond to different gate voltage ranges and thus are not readily comparable to one another. The reader is encouraged to read the details of the experiments in the cited references.^c NR = not reported.^d After pumping for 4 days in high vacuum. Tested in vacuum.

for both Pc₂Tm and Pc₂Lu were obtained. However, upon exposure to air, only *p*-type activity was observed.

Tetracyanoquinodimethane (TCNQ) was used as the active channel layer in *n*-type OTFTs by Brown and coworkers [94]. Bottom-contact OTFTs (**Fig. 7.2b**) were fabricated with gold source and drain electrodes. A mobility of 3×10^{-5} cm² V⁻¹ s⁻¹ and an on/off ratio of 4–450 ($I_{on/off}$ increased upon exposure to air) were reported.

C₆₀ and C₆₀/C₇₀ fullerenes were used as the active channel layer in *n*-type OTFTs initially by Kastner et al. [95], who reported mobilities up to 5×10^{-4} cm²V⁻¹s⁻¹. In a later report, Haddon et al. reported on C₆₀ OTFTs with improved transport characteristics [96]. In that work, the C₆₀ films were deposited by sublimation in UHV and consisted of random polycrystalline grains about 60

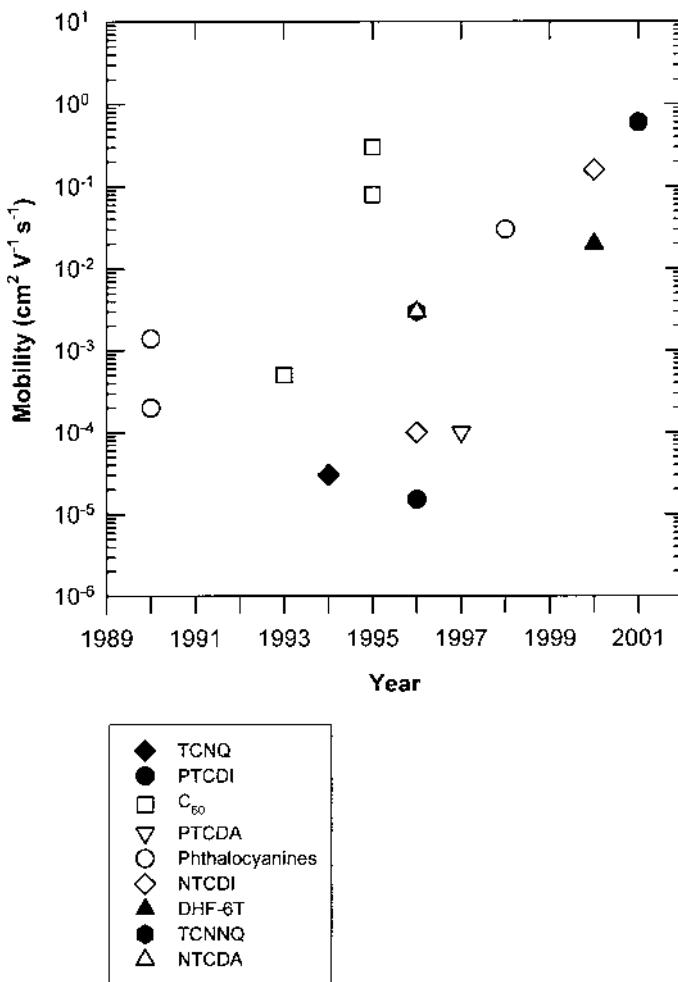


Figure 7.11 Evolution of field-effect mobility of electrons measured from OTFTs based on the most common *n*-type organic semiconductors. Some of the *n*-type materials (e.g., phthalocyanines) have been grouped together into classes of similar molecules, using as a classification criterion only the core part of each molecule.

\AA in size. C_{60} devices were shown to be sensitive to amine exposure and pretreatment of the substrate with tetrakis(dimethylamino)ethylene (TDAE) prior to the deposition of C_{60} , because these treatments shift the threshold voltage to negative values (the device becomes “normally-on”), increase the FET mobility from 0.08 to $0.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, and reduce the $I_{\text{on}}/I_{\text{off}}$ ratio. The resistivity of C_{60} OTFTs quickly increased by four to five orders of magnitude upon exposure to ambient atmosphere, but their transport properties could be restored upon placing the devices in UHV at elevated temperature for about 12 hours. Mobilities of $0.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ were measured from C_{60} single crystals [97] using time-of-flight measurements.

Compared to materials with anisotropic carrier transport properties (e.g., oligothiophenes), which require highly ordered structures with specific molecular orientations in order to produce high field-effect mobilities along a desired direction, transport characteristics in films of C_{60} are isotropic. This is probably the result of the approximately spherical shape of C_{60} , as opposed to the rigid rod or, more generally, elongated shape of many other organic semiconductors.

Katz and coworkers have used several materials based on the naphthalene framework (see Fig. 7.1) as OTFT channels [98,100]. Initially they explored 1,4,5,8-naphthalene tetracarboxylic dianhydride (NTCDA), in which mobilities of $1\text{--}3 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ were measured for films deposited onto substrates held at $T_{\text{sub}} = 55^\circ\text{C}$, but the mobility decreases by one to two orders of magnitude upon exposure to air. Lower mobilities are observed when devices are exposed to atmospheric moisture after sublimation. For devices with NTCDA deposited at $T_{\text{sub}} = 25^\circ\text{C}$, mobilities of $10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ were obtained. Although grain sizes (200 nm) were similar for films grown at both substrate temperatures, films deposited at 55°C were more continuous, which explains the higher mobility of the latter. Devices constructed from 1,4,5,8-naphthalene tetracarboxylic diimide (NTCDI) provided mobilities on the order of $10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. 11,11,12,12-Tetracyanonaphtho-2,6-quinodimethane (TCNNQ) OTFTs displayed higher mobilities ($10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) than Tetracyanoquino-dimethane [94] (TCNQ) TFTs (see above), while having better air-stability than NTCDA but it exhibited a lower on/off ratio. In a recent study, the transport characteristics of *n*-type OTFTs comprising a series of vacuum-deposited films based on N-substituted naphthalene-1,4,5,8-tetracarboxylic diimide derivatives (see Figure 7.1) were reported [99,100]. Transport properties and environmental stability varied greatly with substitution. Only the diimides with fluorinated end-substituents (NTCDI-C8F, NTCDI-BnCF₃, **11** and **12** respectively in Figure 7.1) showed high mobilities in air, whereas linear, alkyl functionalized diimides NTCDI-C8H (**13** in Figure 1), NTCDI-C12H, NTCDI-C18H, gave mobilities of 0.16, 0.005–0.01, and $0.005 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively, but only under vacuum. The highest mobility in air ($0.12 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) was obtained with NTCDI-BnCF₃, while the highest on/off ratio in air ($>10^5$) was achieved with NTCDI-C8F, which had mobility up to 0.1

$\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Mobilities were much higher when the material was deposited onto a substrate held at an elevated temperature. Alternative source and drain electrodes were tested and carbon electrodes gave similar results to gold electrodes, yet the former were not as reproducible as the latter. Carbon source and drain electrodes could be used in a bottom contact configuration (Figure 7.2b), whereas gold electrodes, even if cleaned with oxygen plasma, generally produced either low performance devices or devices that did not operate at all. Interestingly, aluminum electrodes did not provide active devices, despite the fact that aluminum has a lower work function than gold and thus should be more suitable for electron injection into these electron transporters. Although this is likely due to the oxidation of aluminum, which creates an insulating layer of aluminum oxide, another mechanism could be at work as well. In the following paragraph important results that shed some light on this issue are summarized.

The efficiency of injection of electrons (holes) from a metal contact into the conduction band or LUMO (valence band or HOMO) of an *n*-type (*p*-type) organic semiconductor depends on the energy barrier ϕ_{Be} (ϕ_{Bh}) that electrons (holes) have to overcome at the metal/organic semiconductor interface (see Fig. 7.12, taken from Ref. 103). At the metal/organic semiconductor interface, ϕ_{Be} and ϕ_{Bh} depend, respectively, on the position of the LUMO and HOMO relative to the Fermi level (E_F) of the metal. If the assumption of a common vacuum level at the metal/organic semiconductor interface (analogous to the Schottky–Mott limit for inorganic semiconductor interfaces) was valid, ϕ_{Be} would be the difference between the metal work function (ϕ_M) and the electron affinity of the organic semiconductor (E_A), and ϕ_{Bh} would be the difference between the ionization potential (IP) of the organic semiconductor and ϕ_M . For a long time this was considered a valid assumption, due to the generally weak interaction at metal/organic semiconductor interfaces. However, recent studies have shown that this assumption is not always valid [101–103]. These results indicate the existence of a vacuum-level shift at the metal/organic semiconductor interface that can be as high as 1.5 eV. The magnitude and sign of the shift depend on the specific metal/organic combination and can be attributed to an ultrathin, interfacial electric dipole layer [102–105]. To complicate matters, chemical interactions at the interface also affect charge injection barriers. Such interactions depend not only on the constituents of the interface but also on the sequence and method of formation of the interface [103,105]. In some organic semiconductors, such as 3,4,9,10-perylenetetracarboxylic dianhydride (PTCDA), the position of E_F in the band gap of the organic semiconductor is essentially pinned near the top of the band gap for several different metal contacts [103]. As a result, the electron injection barrier does not depend on the metal contact used.

It is obvious from the previous paragraph that simply trying to match the contact metal work function with the LUMO level (in *n*-type OTFTs) or the HOMO level (in *p*-type OTFTs) of the organic semiconductor is not always an

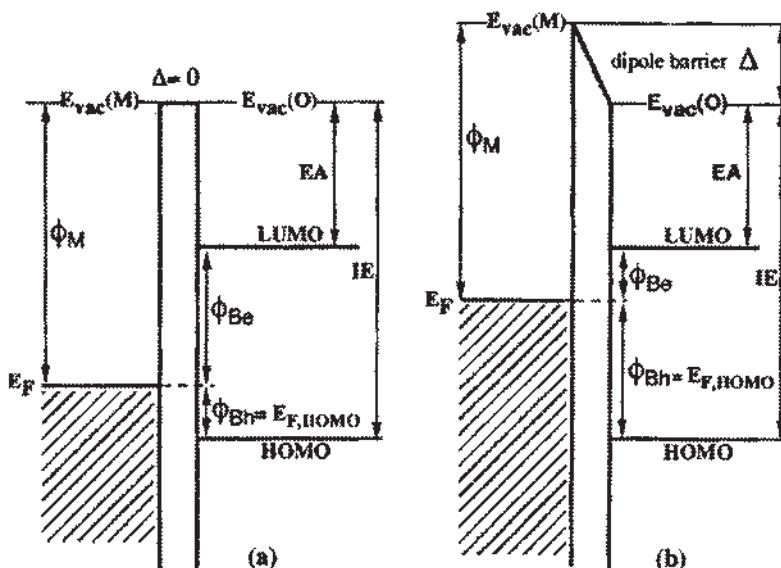


Figure 7.12 Schematic of an organic–metal interface energy diagram (a) without and (b) with an interface dipole Δ . ϕ_{Be} and ϕ_{Bh} are the electron and hole barriers, and $E_{\text{vac}}(\text{O})$ and $E_{\text{vac}}(\text{M})$ are the organic and metal vacuum levels, respectively. (Reprinted from Ref. [103].)

adequate device design rule. Most of the work done to date has employed gold electrodes as the source and drain. Gold has a work function of ~ 5.0 eV against vacuum; since many attractive *n*-type organic semiconductors have solid-state electron affinity levels of ~ 4.0 eV, this energy barrier of approximately 1 eV would be expected to severely limit charge injection into the semiconductor. This is often not the case. For example, in the case of *N,N'*-diphenyl-1,4,5,8-naphthyltetracarboxylic imide (DP-NTCDI), the vacuum level in the organic semiconductor side of the interface with Au moves downward by 0.9 eV, thus bringing the E_F of the gold very close to the LUMO of the DP-NTCDI and facilitating electron injection [102]. When Al is used as the metal contact, however, the vacuum level in the organic semiconductor side of the interface moves upward by -0.2 eV, which was attributed to charge transfer from Al to DP-NTCDI [102]. As a result, the electron injection barrier is higher for the Al contact than for the Au contact.

It has been shown in the past that the energy barrier for carrier injection between a metal and a conjugated organic material can be manipulated by the

insertion of an oriented dipole layer, such as a self-assembled monolayer, between the metal electrode and the organic semiconductor [104,104a]. The discussion in the previous two paragraphs explains this result. In their *n*-type OTFT work with N-substituted naphthalene-1,4,5,8-tetracarboxylic di-imide derivatives (see Fig. 7.1), Katz and coworkers tried this approach in order to obtain working bottom-contact OTFTs with Au electrodes, since devices with unmodified Au electrodes rarely produced transistor activity [99]. Good results were obtained using a 3,4-dichlorobenzyl mercaptan SAM. Relatively high currents (up to 100 μ A) were obtained from devices with NTCDI-BnCF₃ active channels, providing a mobility of approximately $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for bottom-contact devices ($T_{\text{dep}} = 90\text{--}100^\circ\text{C}$). It is possible that the modification of the energy barrier ϕ_{Be} by deposition of an appropriate thiol SAM on the surface of gold [104,104a] resulted in more efficient electron injection, which in turn improved device performance. Furthermore, the presence of the thiol SAM may also result in an increased grain size of the semiconductor on the electrode and in the channel area next to the electrode edge, such that the concentration of grain boundaries and thus charge carrier traps is reduced, as previously reported for pentacene devices (see discussion at the end of section 7.5.4) [91].

In NTCDI-C8F OTFTs, the gate and drain voltage could be cycled repeatedly in air without any serious deterioration of device performance until failure of the gold contacts occurred [100]. As mentioned earlier, OTFTs based on linear, alkyl-functionalized di-imides NTCDI-C8H, NTCDI-C12H, NTCDI-C18H, operated only under vacuum. Interestingly, reduction-potential data does not show a significant difference between fluorinated and nonfluorinated derivatives. Also, the potentials measured for NTCDI-C8F and other fluorinated NTCDI derivatives are formally outside the stability window described by de Leeuw et al. for *n*-type semiconductors [106,99], which indicates that air stability can be obtained even with materials that are expected to be thermodynamically unstable. Since molecular orientation and layer spacings are similar in thin films of fluorinated and nonfluorinated derivatives, by examining the structure of the thin films it was concluded [107] that in the case of NTCDI substituted with linear side chains, the denser packing of the fluorinated side chains vs. the aliphatic ones could provide a “kinetic” barrier to atmospheric molecules such as oxygen. Consistent with this hypothesis is the relatively lower stability of the less densely packed NTCDI-BnCF₃ derivative vs. NTCDI-C8F. However, such an argument is not so straightforward when comparing NTCDI-BnCF₃ to NTCDI-BnCH₃, in which the former provides relatively air-stable devices while the latter has mobilities on the order of $10^{-5} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ even under vacuum. All compounds appeared to have similar film morphologies [107]; thus the observed stability and performance differences cannot be attributed to differences in film morphology.

N-Type OTFTs with *N,N'*-diphenyl-3,4,9,10-perylenetetracarboxylic diimide (PTCDI-Ph) as the active layer have been fabricated and tested, and their

electron mobility was measured to be $1.5 \times 10^{-5} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [108]. Gold and aluminum source and drain contacts were used in a bottom-contact device configuration. The OTFTs with aluminum electrodes were found to have three-times-lower performance. Devices degraded rapidly in air. The field effect could not be observed after two to three days in air in devices with gold contacts and even faster in devices with aluminum contacts.

N-Type OTFTs based on 3,4,9,10-perylenetetracarboxylic-dianhydride (PTCDA) (see Fig. 7.1, **16**) have exhibited field effect mobilities of 10^{-4} – $10^{-5} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [109]. Films of PTCDA were found to grow quasi-epitaxially under specific conditions (especially low substrate temperature, $T_{\text{sub}} = 90 \text{ K}$) on various substrates, thus resulting in highly ordered films in which the molecular plane of PTCDA is approximately parallel to the substrate and the molecules pack in stacks that are almost perpendicular to the substrate [110,22]. It has been reported that the conductivity is very anisotropic in such films, with the in-plane conductivity being at least six orders of magnitude lower than the conductivity perpendicular to the film plane [110]. Thus, the low mobilities can be ascribed to limited electronic orbital overlap in the direction of transport, which in the case of OTFTs is parallel to the substrate. And PTCDA OFETs do not operate in wet air; yet in vacuo or under dry oxygen they operate as described earlier. The effect of moisture on the devices is reversible. Karl and Marktanner have shown, using time-of-flight experiments, that the electron mobility in polycrystalline thin films of PTCDA is inversely proportional to the width of the X-ray rocking curve from the thin film [111,112]. The maximum time-of-flight mobility reported for PTCDA thin films was $3 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for measurements performed under vacuum [111,112].

In perylene **14** single crystals, electron mobilities exceeding $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ have been observed at low temperatures ($\sim 25 \text{ K}$) using time-of-flight experiments [42,46,48]. The mobility exhibits a power law dependence on temperature ($(\mu \propto T^{-n}, n = 1.78 \text{ to } 1.87$, depending on the crystallographic direction along which transport takes place) [42]). At about 300 K the electron mobility is plotted to be slightly larger than $2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ parallel to the crystallographic **a** direction, [42] while it exceeds $5.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ parallel to the crystallographic **b** direction [46]. In perylene, electron mobility is much higher than hole mobility (e.g. hole mobility in perylene along the crystallo-graphic **b** direction is only $0.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [46]), and it seems that trapping states affect hole transport much more severely than electron transport, in contrast to what is usually observed in most other organic semiconductors.

Recently, it was reported that *N,N'*-dioctadecyl-3,4,9,10-perylenetetracarboxylic di-imide (PTCDI-C18H) forms several crystalline and liquid crystalline phases, as demonstrated by X-ray diffraction experiments that show a high degree of order in all three dimensions [113]. X-ray experiments on the liquid crystalline phases suggest a smectic phase, in which the linear alkyl chains are interdigitated.

Charge carrier mobilities measured by pulse radiolysis time-resolved microwave conductivity were higher than $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for LC phases and higher than $0.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for crystalline phases [113].

We have recently shown that OFETs based on *N,N'*-dioctyl-3,4,9,10-perylenetetracarboxylic diimide (PTCDI-C8H) (Fig. 7.1, **15**) as the organic semiconductor provides bottom-contact devices with mobilities as high as $0.6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in the saturation regime and current on/off ratios over 10^5 [27]. High threshold voltages ($>75 \text{ V}$) were observed, which can be attributed to the existence of traps related to structural defects, especially in the region of the channel close to the Au contacts. X-ray studies in reflection mode revealed a (001) plane spacing of approximately 20 \AA , which is consistent with a spacing of 21 \AA that resulted from a modeled structure based on interdigitated alkyl chains [27]. This structure is also consistent with the smectic ordering observed earlier for PTCDI-C18H [113].

The work of Bao et al. has explored a variety of fluorine-substituted metallophthalocyanines as channels in *n*-type OTFTs [114]. Mobilities were affected by the substrate temperature during deposition as well as the metal center of the phthalocyanine. Cu-hexadecafluorophthalocyanine (F_{16}CuPc) (Fig. 7.1, **9**) based OTFTs with the channel material deposited at $T_{\text{dep}} = 125^\circ\text{C}$ exhibited the best performance, with a mobility of $0.03 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and an on/off ratio in the range of 10^4 – 10^5 [114]. It is known that electron-withdrawing groups tend to lower the LUMO level of conjugated organic molecules. By fluorinating the phthalocyanine ring, the LUMO level drops by ca. 1.6 eV relative to the unsubstituted molecule, as shown by UPS measurements and UV-vis data. This makes it less susceptible to oxidation [1115]. Additionally, the lower LUMO level is more accessible for electron injection from metal contacts. The fluorinated metallophthalocyanine devices were very stable in air. They could be stored in air for half a year without showing any decrease in mobility or on/off ratio [114]. All fluorinated metallophthalocyanines adopt an edge on stacking configuration, effectively resulting in a fluorinated barrier at the film surface [114]. This could play an important role in the high air stability observed in these devices, effectively providing a barrier for the diffusion of oxygen toward potential oxidation sites, as discussed previously for NTCDI-C8F.

Recently, Facchetti et al. reported on the use of α,ω -diperfluorohexylsexithiophene (DFH-6T) (Fig. 7.1, **10**) as a novel *n*-type organic semiconductor. [116] Once again, a known p-type material (i.e. α,ω -dihexyl-sexithiophene-DH-6T) was converted to *n*-type by functionalizing it with appropriate electron-withdrawing groups. Although the band gap remains the same for both DFH-6T and DH-6T ($\sim 2.4 \text{ eV}$), redox studies reveal that both the HOMO and the LUMO levels are shifted by 0.27 eV below the corresponding levels of DH-6T. Elevated substrate temperatures produced larger grains, and pretreatment of the gate-insulator surface with $\text{CF}_3(\text{CF}_2)_5\text{CH}_2\text{CH}_2\text{SiCl}_3$ led to approximately 10% larger crystallite

size, and grain-to-grain and grain-to-substrate interconnectivity were considerably enhanced. Top-contact devices were prepared by pretreating SiO_2 surfaces with either hexamethyldisilazane (HMDS) or $\text{CF}_3(\text{CF}_2)_5\text{CH}_2\text{CH}_2\text{SiCl}_3$ prior to the deposition of DFH-6T to alter nature of the oxide surface. Mobilities of $0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and an on/off current ratio of 10^5 were obtained in the saturation regime from devices using gold source and drain electrodes, in nitrogen atmosphere. Similar results were obtained with aluminum electrodes. Air stability was not addressed. These devices were obtained via depositions where the substrate temperature was $80\text{--}100^\circ\text{C}$. However, mobilities of 10^{-4} were obtained when the substrate temperature during deposition was 50°C , and a reduced mobility was also obtained for $T_{\text{sub}} = 120^\circ\text{C}$. The turn-on voltage is fairly high ($25\text{--}35 \text{ V}$) and increases with time, yet it can be stabilized and reduced by postgrowth annealing of the film.

7.6 CONCLUSIONS AND OUTLOOK

The performance of OTFTs has improved substantially during the past 10–15 years. Such advances in OTFT performance have been the result of the introduction of novel materials obtained either by the chemical modification of existing molecules or by the synthesis of completely new ones, followed by optimization of their morphology and structural order.

The OTFTs comprising organic semiconductors, such as pentacene, deposited by vacuum sublimation, remain the highest performers due not only to their molecular electronic properties but also to their very well-ordered structures, which result from the use of this highly controllable deposition method. However, substantial improvements have taken place in solution-processed organic semiconductors too, and their field-effect mobilities are approaching those of vapor-deposited OTFTs [117]. There is a potentially important cost advantage associated with the solution processing of organic TFTs, for it eliminates the need for expensive vacuum chambers and lengthy pump-down cycles. However, for this advantage to be realized, all or at least most of the layers comprising the OTFT device should be deposited using methods that do not involve vacuum deposition. Roll-to-roll processing, which has obvious advantages over batch fabrication processes for reducing costs, can be applied to both vacuum- and solution-deposited organic semiconductors; but if one considers the ability to stamp, screen-print, or inkjet-print solution-based organics, thus eliminating traditional lithographic steps, then their potential cost advantage over vacuum-deposited organics becomes more apparent. Good device stability and long lifetimes are two other very important requirements that if satisfied may enable the full realization of the advantages of organic semiconductors. Encapsulation techniques can be used and have worked in the past, but they can substantially reduce the cost advantages that organic

semiconductors can offer if they are stable during processing and during operation.

The ability to synthesize custom-made organic semiconductor molecules to match the requirements of different applications is probably the major advantage of this technology. The future seems promising for inexpensive organic electronics that will address new and existing application needs.

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8

Organic Transistors: Materials, Patterning Techniques and Applications

John A. Rogers, Zhenan Bao and

Howard E. Katz

Bell Laboratories, Lucent Technologies, Murray Hill, New Jersey, U.S.A.

Ananth Dodabalapur

University of Texas at Austin, Austin, Texas, U.S.A.

8.1 INTRODUCTION

Advances in electronics will occur simultaneously along two different paths. One will focus on increasing the circuit speed and density through [1] the continued improvement of established materials and lithographic techniques and [2] the creative use of molecular or nanoscale building blocks for assembling critical circuit components from the bottom up [1]. The other path will involve developing completely new types of electronic systems based on unconventional materials and printing techniques [2]. This class of circuitry will be important (at least initially) not because of its potential for high speed, density, etc., but because it can be mechanically flexible, lightweight, durable, and easy to print rapidly over large areas. These plastic circuits will form the foundations for novel devices—electronic paper, wearable computers or sensors, disposable wireless ID

tags, etc.—that complement the types of systems that conventional electronics supports well (e.g., microprocessors, high-density RAM). This field is new (i.e., there are no entrenched technologies) and it has a strong materials content. As a result, there are considerable opportunities for innovation and basic scientific research. Progress in this area requires establishing new materials and patterning techniques for flexible circuits, developing a fundamental understanding of the chemistry and physics of organic semiconductors, designing component geometries that complement these systems, and inventing new ways to exploit the unique properties of these circuits in devices.

This chapter focuses on materials, patterning techniques, and applications for a fundamental element of complex active circuits: the thin-film transistor (TFT). Figure 8.1 shows cross-sectional views of two common geometries for TFTs. Both cases utilize a semiconducting layer that is electrically connected to source and drain electrodes. A thin insulating film isolates these electrodes and the semiconductor from an underlying gate electrode. The source/drain electrodes can be deposited on top of the semiconductor (top-contact TFT; Fig. 1b), or the semiconductor can be deposited on top of them (bottom-contact TFT; Fig. 1a). The region between the source/drain electrodes is known as the *channel* of the

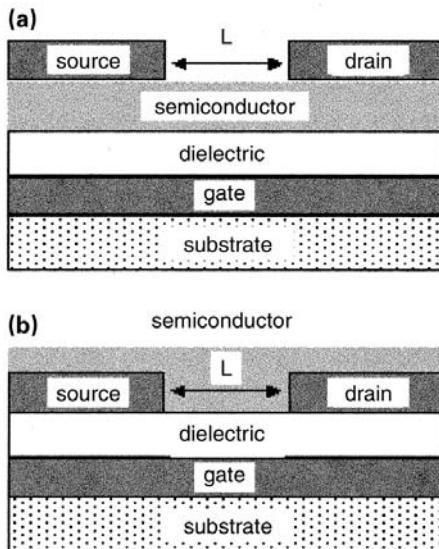


Figure 8.1 Schematic illustrations of two layouts of a thin-film transistor. (a) Geometry often referred to as “bottom-contact” because the source/drain electrodes lie beneath the semiconductor. (b) A “top-contact” device.

transistor. The separation between these electrodes defines the channel length, L ; their lengths define the channel width, W .

In an accumulation-mode device, the current flow between the drain and source electrodes is low when no voltage is applied between the gate and the drain electrodes. When the gate voltage is zero, the transistor is in its “off” state. When a voltage is applied to the gate, charges can be induced in the semiconducting layer at its interface with the gate dielectric. In this situation, current flows between the source and drain electrodes when there is a potential difference between them: The transistor is in its “on” state. The magnitudes of these “on” and “off” currents and the time required to switch between these two states determine the utility of a transistor in a circuit. The TFT must produce enough “on” current to activate or switch another part of a circuit, but it must not generate “off” currents that are large enough to cause unwanted switching.

The “on” current is typically measured in a regime where the source/drain voltage is larger than the gate voltage. Here the current, known as the *saturation* current, is independent of the source/drain voltage; it can be related to other characteristics of the device in the following way [3]:

$$I_{sd} = \frac{W}{2L} C \mu (V_g - V_T)^2 = \frac{W}{2L} \frac{\epsilon \epsilon_0}{t} \mu (V_g - V_T)^2 \quad (8.1)$$

where μ is the effective mobility of the semiconductor, ϵ is the dielectric constant of the gate dielectric, t is its thickness, and ϵ_0 is the permittivity of free space. V_g is the gate voltage and V_T is known as the threshold voltage. Transistors that have large “on” currents possess some combination of large μ , high ϵ , small t , small L , and/or large W . Limits on the overall physical size of a transistor for a particular application typically place an upper bound on W . The key properties therefore reduce to μ , t , ϵ , and L . The following sections describe chemistries of organic semiconductors that have relatively high μ and some basic physics of charge transport in them. Several promising materials for high-capacitance, low-leakage interlayer dielectrics that are compatible with these semiconductors are then presented. The next section reviews patterning approaches that have proven to be useful for manipulating these materials and forming functional circuits. The remainder of the chapter describes some realistic applications in electronic paper-like displays and plastic logic elements.

8.2 ORGANIC SEMICONDUCTORS

There are two classes of organic semiconducting compounds that meet both the performance and processing requirements for plastic electronics technology: conjugated polycyclic compounds of molecular weight under 1000, and polyheterocycles with much higher average molecular weight. The lower-molecular-weight

“small molecules” include heterocyclic oligomers, linear fused rings, and two-dimensional fused rings. Recently, oligomers containing both individual and fused rings have been prepared, as have hybrid materials consisting of inorganic networks and organic templates. While several prototypical semiconductors are commercially available, including the polyacenes and phthalocyanines, and others can seemingly be synthesized via trivial one-step conversions, optimized materials may require more complex synthetic methods. In the case of polymers, control of regiochemistry, molecular weight distribution, and end groups are necessary to ensure the needed chain overlaps and orientation. All of the organic semiconducting materials, including those synthesized by supposedly trivial means, need to be in highly purified forms, because impurities affect a host of physical properties, especially the on-and off-conductance, that bear on the ultimate utility of the compositions. In many cases, the choice of synthetic sequence is governed by the overriding consideration of final product purity, and the most direct pathways are not necessarily the ones most likely to ensure pure products.

There are a few essential kinds of steps relevant to the preparation of organic semiconductors: ring synthesis, ring linkage, substituent attachment, and refinement. These are of varying importance among the classes of compounds considered. Obviously, compounds based on widely available heterocycles, such as thiophene, do not require ring synthesis, while others are based on entirely new heterocycles whose synthesis was problematic. Linking and substitution reactions may be chosen from a voluminous literature and include the Stille, Suzuki, Kumada, and other organometallic coupling reactions [4,5]. These must often be tuned because of specific and unexpected side reactions associated with particular backbones or because of the need to avoid a particularly deleterious byproduct. While few of the reactions discussed here are entirely new, their selection and use are often quite material specific. Relevant thiophene chemistry has been reviewed by Bauerle [6], and the influence of ordering on the performance of these compounds has been reviewed by Fichou [7].

The prototypical semiconducting oligomers are α -6T and dihexyl- α -6T, as first described by the CNRS group. The first high-mobility and high-on/off ratio FETs were made from these compounds. The dihexyl derivative was also cast as an active film from solution. Side chains other than hexyl can also be incorporated, provided the corresponding anhydrides or acid chlorides are available. For example, we have prepared didodecyl- and dioctadecyl- α -6T [8]. The latter compound has FET activity even though a large volume fraction consists of insulating polyethylene-like chains, a tribute to the two-dimensional nature of the mobility in crystalline layered structure domains of these compounds. Another kind of side chain that we have appended to thiophene oligomers is alkoxyalkyl [8] (Fig. 8.2), where one of the methylene units of an alkyl chain is replaced by an ether oxygen. We have observed enhanced solubility of the thiophene hexamer with butoxypropyl end substituents (**6**, $n = 4$) relative to the dialkyl analogs [8].

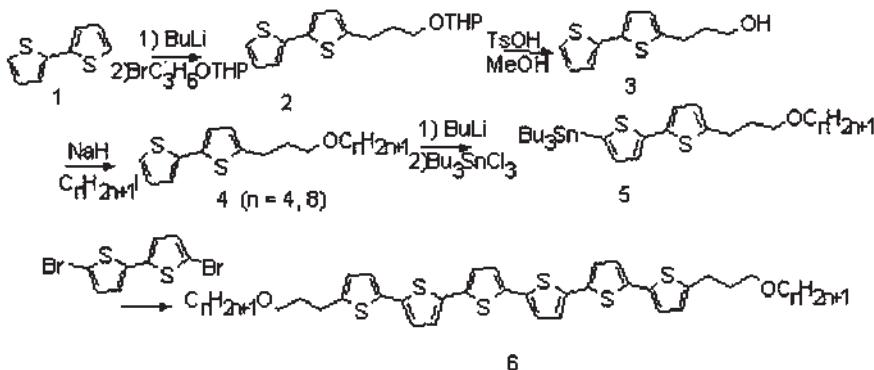


Figure 8.2 End-substituted oligothiophene synthesis.

Contrary to our expectations, we found that dihexyl- α -**4T** [9] **7** and **5T** [10] **8** (Fig. 8.3) had mobilities as high or higher than the 6Ts. This result is important because the greater solubility and volatility of the shorter oligomers allow easy deposition of films [11]. The shorter compounds are also slightly less prone to atmospheric doping, which diminishes the on/off ratio and alters the threshold voltage (the gate voltage where an FET is decidedly on). Another means of improving environmental stability without shortening the molecule is to incorporate a less oxidizable central subunit. We prepared bis(hexylbithienyl)bithiazole **9** and showed that its on/off ratio is higher than the all-thiophene analog, and its threshold voltage is markedly less susceptible to drift [10]. These effects are attributable to the substitution of just two atoms in an otherwise identical pair of molecules. Preliminary results suggest that similar beneficial effects are obtained by employing 1,4-phenylene as the central subunit in place of the bithiazole, as in **10** [12]. High on/off ratio devices were made from solution-cast films of this compound. Internal double bonds, on the other hand, were found to decrease compound stability, although one thiénylenevinylen oligomer, all-trans 2,5-bis(2-(2,2'-bithien-5-yl)ethenyl)thiophene **11**, has a measured mobility of 0.008–0.012 cm²/V-s as an evaporated film and 0.0014 cm²/V-s when spin-coated [13].

8.2.1 Linear Fused Rings

Pentacene **13** is one of the most widely studied organic FET semiconductors [14–17]. It is easily synthesized via quinone **12** [18] (Fig. 8.4), is commercially available, and displays the highest mobility in an easily realizable device. Pentacene is only moderately stable to oxygen as a dense solid and is considerably

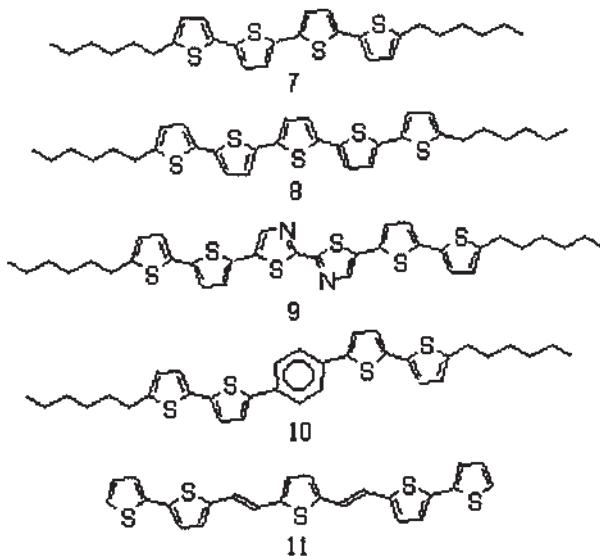


Figure 8.3 Thiophene oligomers and co-oligomers.

unstable as a high-surface-area solid or dispersion or under illumination. Pentacene is also very high melting and virtually insoluble, even in hot aromatic solvents. It was attractive to combine the molecular shape of pentacene, which leads to a favorable crystal packing geometry and orientation, with thiophene end groups that would increase stability and also provide points of attachment for solubilizing substituents. This led us to consider anthradithiophenes, whose parent compound had never been reported, though its dione precursor had been described.

The synthesis of unsubstituted anthradithiophene **16** via quinone **15** was analogous to that of pentacene [19]. It was presumably obtained as a mixture of syn and anti isomers, since the reaction should not have favored either of them, and there was no obvious way to separate them. The compound is lighter in color and more environmentally stable than pentacene. Its field-effect mobility is an order of magnitude lower than that of pentacene, about $0.1 \text{ cm}^2/\text{V}\cdot\text{s}$, but its on/off ratio is higher versus for zero gate. A highly ordered thin-film morphology was observed and is consistent with the electrical characteristics. Hexyl, dodecyl, and octadecyl disubstituted derivatives were also made (structure **21**), and the first two had higher mobilities than the parent compound, with increased solubility. The third still had significant activity, even though it consists mostly of

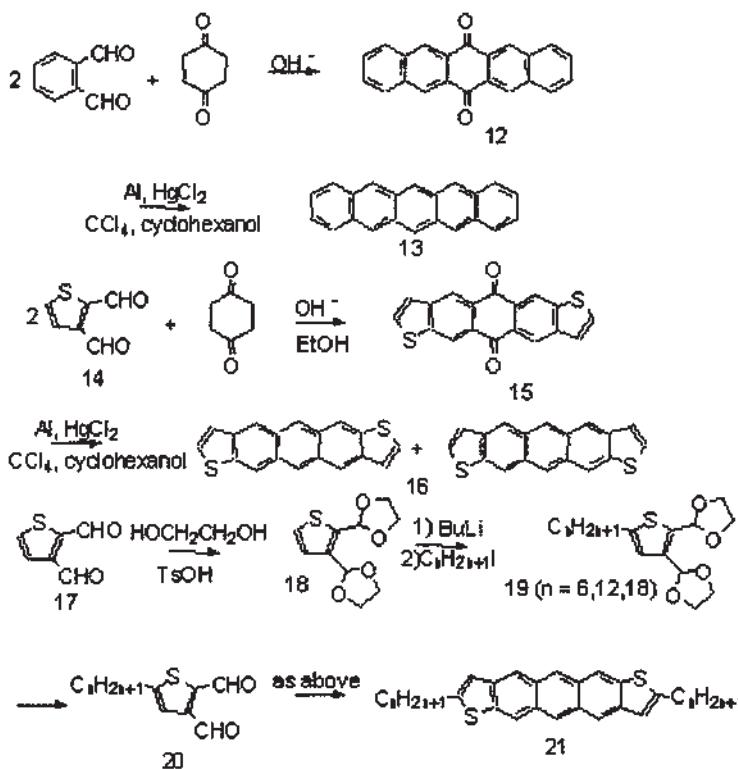


Figure 8.4 Linear fused-ring semiconductors.

nonconjugated carbons. The dihexyl derivative could be cast under certain conditions as an active film from solution, while pentacene has been solution cast only as a Diels–Alder adduct [20].

Other fused-ring subunits have been incorporated into semiconductors as well. The dimer of benzodithiophene was purified by vacuum sublimation to give a bright yellow compound with remarkable stability in air below 400°C and mobility of $4 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ when evaporated on a substrate at 100°C [21]. Dithienothiophene has been studied by the Cambridge group and is the first FET semiconductor with a stacked, rather than herringbone, crystal structure [22]. Oligofluorene derivatives **22** and **23** (Fig. 8.5) containing fluorenes substituted at the 5,5' positions of the bithiophene have been reported [23]. These oligomers showed mobility greater than $0.1 \text{ cm}^2/\text{V}\cdot\text{s}$ and exceptional stability. The incorporation of fluorene allowed the fine adjustment of the energy levels of the resulting

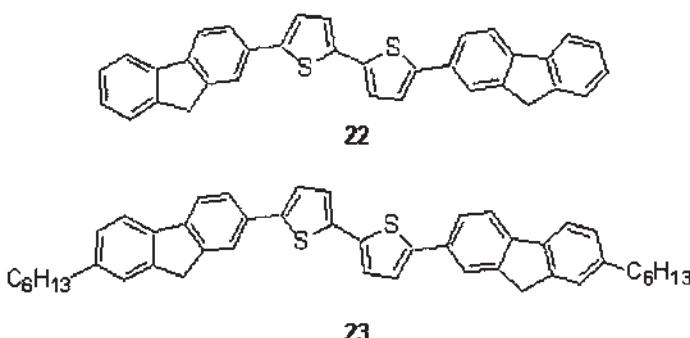


Figure 8.5 High-performance oligofluorene derivatives.

oligomers by controlling the twist angle between fluorene and the co-oligomeric unit.

8.2.2 Two-Dimensional Fused-Ring Compounds

The simplest two-dimensional fused rings that we have employed are NTCDI derivatives **25**. They are synthesized trivially from NTCDA **24** and amines [24] (Fig. 8.6) and can be easily purified by sublimation. Some of these compounds have the rare characteristic of high electron mobility [25,26]. The incorporation of fluoroalkyl groups on the side chains greatly stabilizes NTCDI solids for electron transport in air by a mechanism that is not yet fully understood [27]. Ring substitution by fluorine or other small electron-withdrawing groups would also be desirable but remains an unresolved challenge.

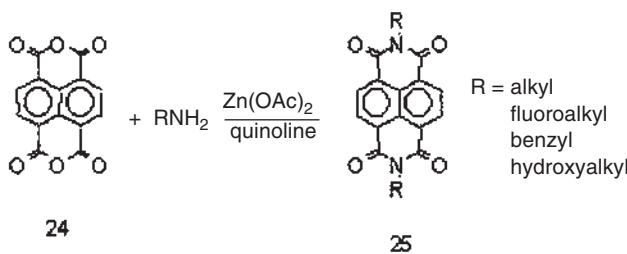


Figure 8.6 NTCDI synthesis.

The family of phthalocyanines **26** is another type of two-dimensional fused-ring system (Fig. 8.7). They are commonly used as organic semiconductors in numerous applications, such as solar cells, light-emitting diodes, and nonlinear optical materials [28]. Most of the unsubstituted phthalocyanines, coordinated with different metals, are commercially available and can be easily purified by vacuum sublimation. The most common and best-performing phthalocyanine for *p*-channel transistors is the copper phthalocyanine (CuPc). Mobility as high as $0.02 \text{ cm}^2/\text{V}\cdot\text{s}$ and on/off ratio greater than 10^5 have been reported [29]. The rare earth bis(phthalocyanines) were also shown to have relatively high *p*-type mobility (ca $0.015 \text{ cm}^2/\text{V}\cdot\text{s}$) [30]. In addition, *n*-type behavior was observed under vacuum [31].

The energy levels of phthalocyanine derivatives can be tuned by substitution with electron-withdrawing groups to give *n*-channel semiconductors (**26–28**) [32]. Several phthalonitrile derivatives with perfluoro- and perchloro-substitution are readily available and they can be used to form the corresponding phthalocyanines following standard literature procedures. The perfluorinated metallophthalocyanines are easily purified by vacuum sublimation, and highly ordered semi-

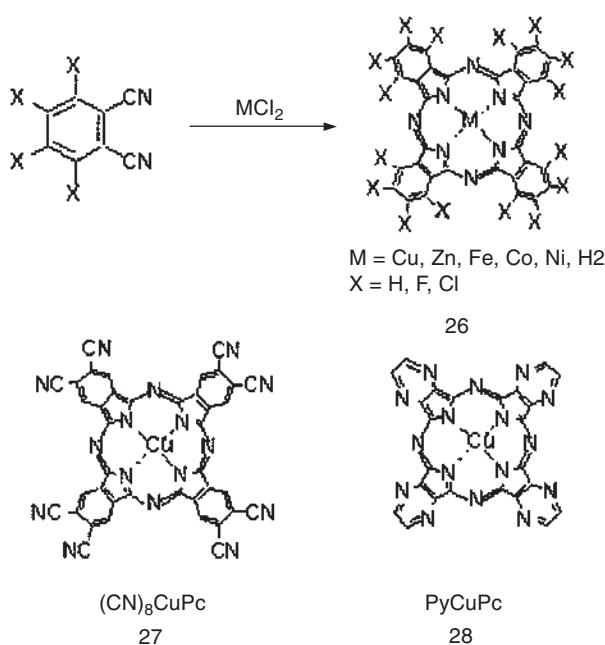


Figure 8.7 Phthalocyanine derivatives.

conductor films can be prepared [32–34]. The best transistor performance was reported with the copper complex [33]. The perchlorinated phthalocyanine showed surprisingly low crystallinity, and the resulting films had very low field-effect mobility.

8.2.3 Polymeric Semiconductors

Polymeric materials offer advantages of easy processing from solution and good film-forming properties. The family of polythiophene derivatives are the most studied polymers for transistor application. The low-mobility electrochemically polymerized polythiophene was used in the first organic field-effect transistor [35]. Solution-soluble regiorandom poly(3-alkylthiophene)s **36** used for transistor studies are usually prepared using FeCl_3 oxidative polymerizations from 3-alkylthiophenes **35**. Low mobilities were again reported and were attributed to the random structures and amorphous morphology in the solid state [36]. Attempts have been made to improve the molecular ordering of regiorandom poly(3-alkylthiophene)s by using Langmuir–Blodgett (LB) films [37–38]. However, a large amount of surfactant has to be incorporated in order to form stable LB films, and the resulting devices showed poor performance [38].

Regioregular poly(3-alkylthiophene)s **34** ([Fig. 8.8](#)) have been shown to have very different properties from their corresponding regiorandom polymers, such as smaller band gaps, better ordering and crystallinity in their solid states, and substantially improved electroconductivities [39]. The field-effect mobility of regioregular poly(3-hexylthiophene) (P3HT) is among the highest reported for polymer transistors [40–44]. Various synthetic approaches for P3HT are shown in [Figure 8.10](#)[44–51]. The polymer backbones adopt a preferred orientation in thin films, such that the hexyl side chains may be close to normal to the substrate and the backbone is essentially parallel to the substrate [40–43]. Such preferred orientation might account for the relatively high mobilities in P3HT, since it would place the transport direction (i.e., that between thienyl rings) parallel to the substrate.

Regioregular polythiophenes with various side chains can be readily prepared using the McCullough approaches (**34,37–39**, [Fig. 8.9](#)). The nature of the side chains has a great impact on transistor performance [40–41,50]. First, the length of linear alkyl substituents needs to be between 3 and 12 carbons [50]. If the alkyl chain is too long, the film matrix could be dominated by the insulating alkyl substituents, resulting in low mobilities of the films. On the other hand, if the alkyl chain is too short, the polymer has low solubility and it is difficult to form uniform smooth films. Second, the bulkiness of the side chains has a direct effect on the morphology and field-effect mobility of the polymer [41]. Poor molecular ordering and low crystallinity have been observed for regioregular polythiophenes with bulky or carboxylic-substituted sidechains (**38** and **39**), and

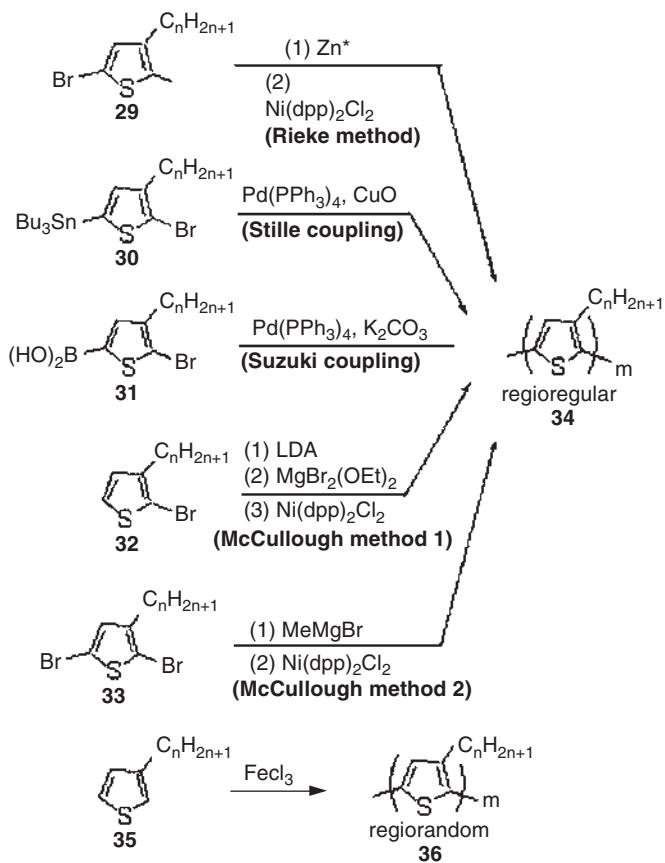


Figure 8.8 Polythiophene derivatives.

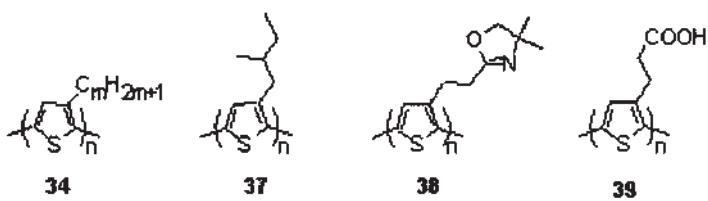


Figure 8.9 Synthesis of polythiophenes.

the resulting transistor devices also showed low field-effect mobilities (less than 10^{-5} – 10^{-4} cm 2 /V-s) [41]. In another example, a chiral alkyl-substituted regioregular polythiophene (**37**) has shown better crystallinity. However, the π – π overlap distance between the polythiophene backbones increases substantially [i.e., to ca. 4.3 Å vs. 3.8 Å for regioregular poly(3-hexylthiophene) (PHT)] after the introduction of methyl branches in the side chains. The field-effect mobility of this polymer is reasonably high compared to many solution-processable conjugated polymers (i.e., of the order of 10 $^{-3}$ cm 2 /V-s) but is still an order of magnitude lower than regioregular PHT [41]. These results indicate that the nature of the side chains has a critical impact on the self-assembly, crystallization, and semiconducting properties of regioregular poly(3-alkylthiophene) derivatives. High crystallinity and high transistor performance are obtained only with regioregular polythiophenes that contain non-sterically-hindered linear side chains.

Recently, Sirringhaus and coworkers reported the transistor performance of a liquid crystalline polymer [52]. It is an alternating copolymer of a bithiophene and a dioctylfluorene, and enhanced mobility was reported through chain alignment in its liquid crystalline phase. Mobility of 0.01–0.02 cm 2 /V-s for devices parallel to the alignment direction was obtained, while it is five to eight times lower perpendicular to the alignment direction. Another polymeric system involves a soluble precursor polymer that can undergo subsequent chemical reactions to give the desired conjugate polymer, such as poly(thienylene vinylene) ($\mu = 0.22$ cm 2 /V-s) [53]. Even though high field-effect mobilities have been reported, the on/off ratios often suffer due to partial doping of the material. Similarly, high mobilities and low on/off ratios have been reported for polypyrrole and polyaniline [54–55].

8.3 INTERLAYER DIELECTRICS

Although the semiconductor is a critical component of TFTs, there are other important elements. Interlayer dielectrics, for example, can affect the properties of a transistor in several ways. First, the current output of the transistor is linearly associated with the capacitance of the dielectric material, according to Eq. (8.1). Ultrathin dielectrics made out of materials with high dielectric constants are, therefore, important for producing transistors that can operate at low voltages. Second, the dielectric surface can impact the charge-trapping density and the orientation and growth of the semiconducting layer deposited on top of it. It has been shown that the performance of pentacene transistors can be as high as 2 cm 2 /V-s when the SiO₂ surface is treated with trichloro-octadecylsilane [56,57]. In another example, the intrinsic on/off ratio of regioregular PHT can reach as high as 10 6 when samples are prepared under a nitrogen atmosphere on hexamethylidisilazane-(HMDS)-treated SiO₂ dielectrics, overcoated with a reducing layer of SiO_x, and measured under vacuum [42]. Surface treatment with fluorinated

molecules can reduce the crystallization of oligomers and thereby enhance the uniformity of cast or evaporated films [58]. Third, the chemical nature of the dielectrics can also play an important role in the long-term reliability of the resulting transistors. Preliminary data suggest, for example, that polymer dielectrics with functional groups with relatively low reactivity toward the semiconductor tend to yield transistors with good long-term performance [59]. This observation may result from a reduction in interfacial reactions between the dielectric and semiconductor that could disrupt the integrity of this critical current-carrying layer.

Several types of dielectric materials have been explored for organic transistor applications. These include inorganic oxides, spin-on polymers, and self-assembled monolayers. Inorganic oxide dielectric materials offer high dielectric constants and low leakage. Various surface modifications are also easily carried out on oxides using silane chemistry. The most commonly used oxides are thermally grown SiO_2 and sputtered Al_2O_3 . These materials and other similar ones have the disadvantage, however, that they require vacuum processes and/or high temperatures, which make them incompatible with large-area plastic substrates and low-cost manufacturing. Anodized dielectrics, on the other hand, offer the possibility of solution-grown, ultrathin, low-leakage insulators of materials with high dielectric constants. Our recent work [60] demonstrates that anodizing Ta at room temperature in 0.01 M citric acid solution with a platinum foil counterelectrode generates uniform, ultrathin (~ 50 nm), defect-free (leakage currents $< 10^{-8}$ A/cm² at ± 1 MV/cm) layers of Ta_2O_5 ($\epsilon \sim 23$) (gate dielectric) on unreacted films of Ta (gate electrode). Organic *n*- and *p*-channel transistors printed onto these gate dielectrics/gate electrodes show good performance [60]. These devices can also be mechanically flexible: Transistors with anodized dielectrics formed on bendable supports show good performance even when flexed (Fig. 8.10). Anodization of other conductors (e.g., Si, Al) may also yield convenient routes to high-quality dielectrics with large capacitances. In addition to these materials, certain oxides prepared from sol-gel materials may be potentially promising as solution-processed inorganic dielectric materials.

Spin-on polymers, such as polyimides and polymethyl methacrylates, are also attractive candidates for transistor dielectrics. Uniform, mechanically flexible films can be deposited over a large area, and good transistor performance has been demonstrated. Organic polymers have the disadvantage, however, of relatively low dielectric constants. Ultrathin films of these materials are therefore required to achieve high-capacitance dielectrics for low-voltage operation. The fabrication of ultrathin pinhole-free polymer dielectric films remains challenging. Surface-initiated graft of polymers and layer-by-layer deposition of polymer electrolytes may represent promising approaches toward ultrathin dielectric layers with good leakage characteristics. Self-assembled monolayers (SAMs) are perhaps the thinnest possible type of organic dielectric. It has been shown that ~ 2 -

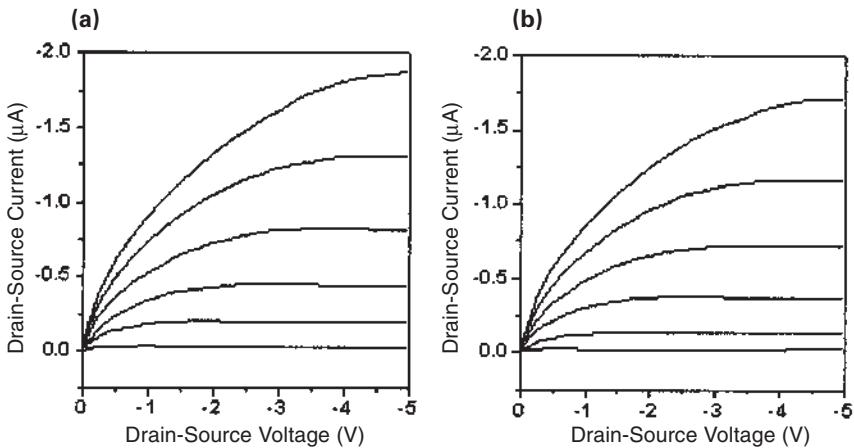


Figure 8.10 Current–voltage characteristics of a bottom-contact thin-film transistor printed onto an anodized gate dielectric (Ta_2O_5 ; 50 nm thick). The semiconductor is DH α 5T, the gate is Ta, and the source/drain electrodes are made of electroless silver (~100 nm thick) patterned with microcontact printing. The gate voltages vary from 0 V to –5 V in steps of –1 V. (a) Performance in the unbent state. (b) The same transistor operating when flexed with a bend radius of ~1 cm. Bending the transistor does not affect its performance.

nm-thick SAMs Si can yield working organic transistors with 30-nm channels [61]. This type of dielectric is likely to be important for nano-scale organic transistors.

8.4 PATTERNING TECHNIQUES

Organic materials are attractive for applications in electronics in part because films with good characteristics can often be formed simply by solution-casting or evaporation at relatively low temperatures. This capability, however, has practical advantage only when it is coupled with low-cost patterning approaches that can be applied directly to these materials or to those that are compatible with them. High-resolution patterning methods for defining the separation between the source and drain electrodes (i.e., transistor channel length, L) are particularly important, since this dimension determines current output [Eq. (8.1)]. Although conventional patterning techniques, such as photolithography and electron beam lithography, have the required resolution, they are not well suited to plastic electronics because they are expensive and generally require multiple processing steps with resists,

solvents, and developers that can be difficult to use with organic active materials. Nevertheless, recently described photolithographic processes that rely not on resists but on the photochemical conversion of polymers from nonconducting to conducting states or from luminescent to nonluminescent ones can yield impressively complex organic circuits [62] and patterned light-emitting devices [63]. Similar approaches will likely be important in the future, but they may also retain the high costs associated with photolithography and they may be less flexible than other methods in the materials that can be processed. Inkjet printing is another promising method that has been applied to organic transistors [64] and light-emitting diodes [65,66]. This section focuses on four other nonphotolithographic approaches [67] that have been demonstrated for patterning organic electronics: screen printing [50,68], micromolding in capillaries [69,70], microcontact printing [71,72], and a low-cost form of near-field photolithography [73,74]. It presents a brief overview of each these methods and describes their use for patterning organic TFTs. It also describes how these techniques might be combined and matched to form a complete system for patterning all layers in practical devices.

8.4.1 Screen Printing

Screen printing is a simple patterning method that uses a “doctor blade” to squeeze ink through predefined screen masks. It is a purely additive method in which an ink is deposited and patterned in a single step. The resolution depends on the properties of the inks and the substrate and the mask. It is generally difficult to form features smaller than $\sim 200 \mu\text{m}$ with this method. Transistors with printed gate, drain, and source electrodes were first described by Garnier and coworkers [68]. More recent work demonstrated high-performance plastic transistors in which all of the essential components were screen printed [50]. [Figure 8.11](#) shows the procedures used in this case. A poly(ethylene terephthalate) film serves as the plastic substrate, and a thin ITO layer acts as the gate electrode. A polyimide layer printed through a screen mask onto the ITO surface provides a gate dielectric. An organic semiconductor layer consisting of regioregular poly(3-hexylthiophene) (PHT) is then deposited by spin-coating, casting, or printing using chloroform as the solvent. Printing the drain and source electrodes using a conductive ink through another screen mask completes the transistor.

[Figure 8.12](#) shows the characteristics of a typical printed transistor fabricated in this manner. It is a p-channel device that can operate both in accumulation mode and depletion mode. The field-effect mobilities observed in transistors with screen-printed PHT are typically $\sim 0.03 \text{ cm}^2/\text{V}\cdot\text{s}$. Their characteristics are comparable to those devices achieved with PHT by using a Si substrate as the gate, SiO_2 as the dielectric layer, and photolithographically defined gold electrodes.

Most realistic circuit applications (e.g., displays) of existing organic semiconductors demand channel lengths in the range of $25 \mu\text{m}$ or less, which makes

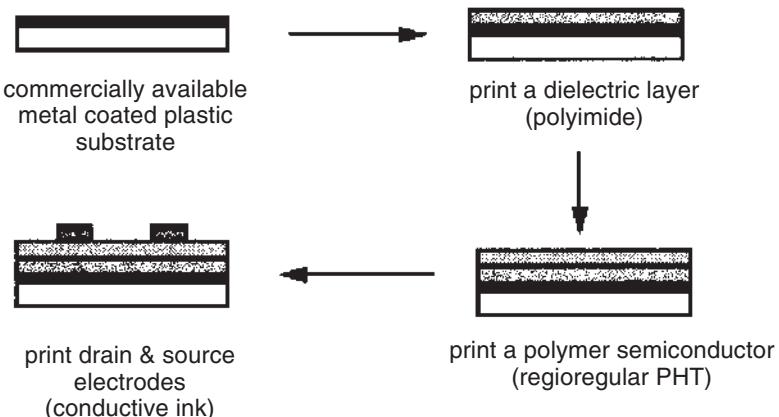


Figure 8.11 Schematic procedures for screen printing of plastic transistors.

screen printing unsuitable for patterning the source/drain electrodes. Screen printing is, however, a useful technique that it is already relatively well developed for applications similar to organic electronics. It is likely, therefore, that screen printing or a similar method will be useful for forming certain low-resolution components of an organic circuit. Other specialized techniques could then be used for the source/drain electrodes or other elements that demand high-resolution features. Some of our recent work focuses on developing methods for patterning features with a resolution that meets the requirements for the source/drain level. We studied, in particular, the suitability of techniques that use elastomeric stamps, molds, and conformable phase masks for this patterning task [75–77]. These soft lithographic [78] methods are attractive because they are low cost and have resolution that comfortably satisfies the requirements for many interesting applications of organic electronics. Although many aspects of these techniques are less well developed than those of screen printing, research applications of them to several areas of conventional microelectronics are emerging, primarily from the Whitesides group at Harvard [79,80] and the Nuzzo group at University of Illinois at Urbana, Champaign [81,82]. Our work in this area has focused on the use of these methods for plastic optical [77,83–86] and electronic systems [75–77]. These soft lithographic techniques rely on elastomeric elements that are formed by casting and curing a silicone prepolymer (polydimethylsiloxane) against a “master” structure of relief (Fig. 8.13). These elements are then used as stamps, molds, or near-field phase masks, as described in the following sections. Many elements can be generated from a single master; each element can be used many times.

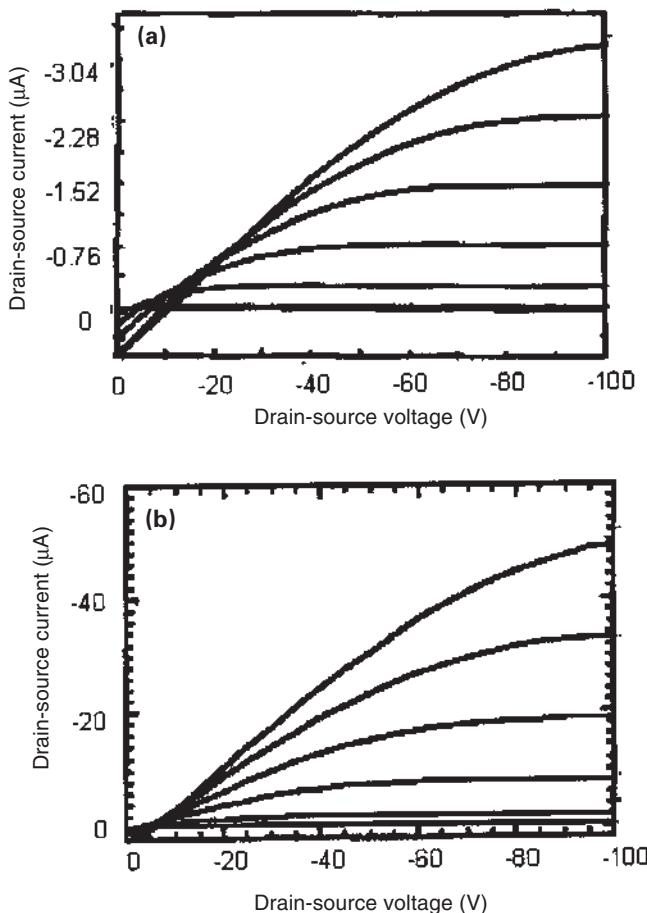


Figure 8.12 Current–voltage characteristics of (a) a screen-printed and (b) lithographically defined transistor.

8.4.2 Micromolding in Capillaries

Figure 8.14 illustrates how a technique known as micromolding in capillaries (MIMIC) [69] can be used to define source/drain electrodes. The elements illustrated in Figure 8.14 serve as molds in the MIMIC procedure. The mechanical flexibility of the mold enables conformal, liquid-tight sealing when it is brought into contact with the surface to be patterned. This conformal contact generates an array of capillary channels. Liquid applied to access holes in the mold wicks

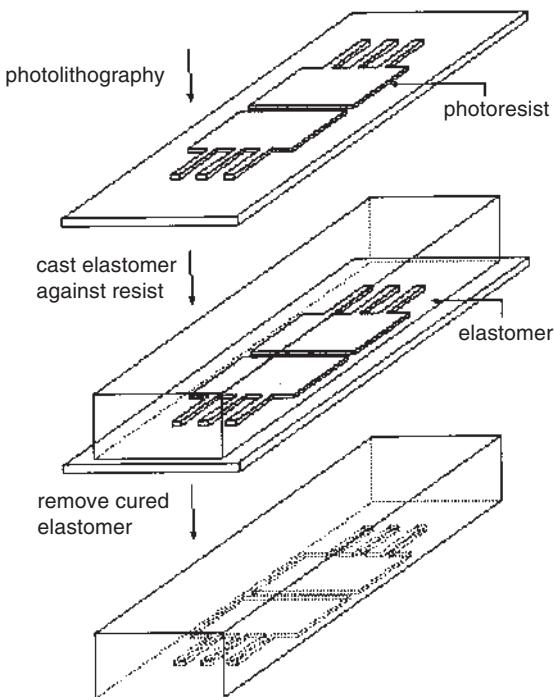


Figure 8.13 Method for generating elastomeric elements that can serve as stamps, molds, or conformable phase masks. Conventional lithographic methods, such as photolithography, produce a pattern of resist on a substrate. Casting and curing a prepolymer of a silicone rubber (e.g., polydimethylsiloxane) against this structure produces transparent elements with relief in the geometry of the resist. Many elements can be produced from a single master; each element can be used many times.

into the channels. In order for fluid to flow through them on reasonable time scales, the cross-sectional dimensions of the channels must be larger than a few microns and the inks must have a sufficiently low viscosity. The distance of separation between the source and drain electrodes (which is the most important dimension for this application), on the other hand, is not limited by this consideration, because this dimension does not affect the flow dynamics of the liquid that fills the channels: The transistor channel length can be substantially less than one micron.

We have used MIMIC to form electrodes of conducting carbon by using liquid carbon paint ($\sim 2\%$ solid carbon in ethanol) and of polyaniline (PA) by

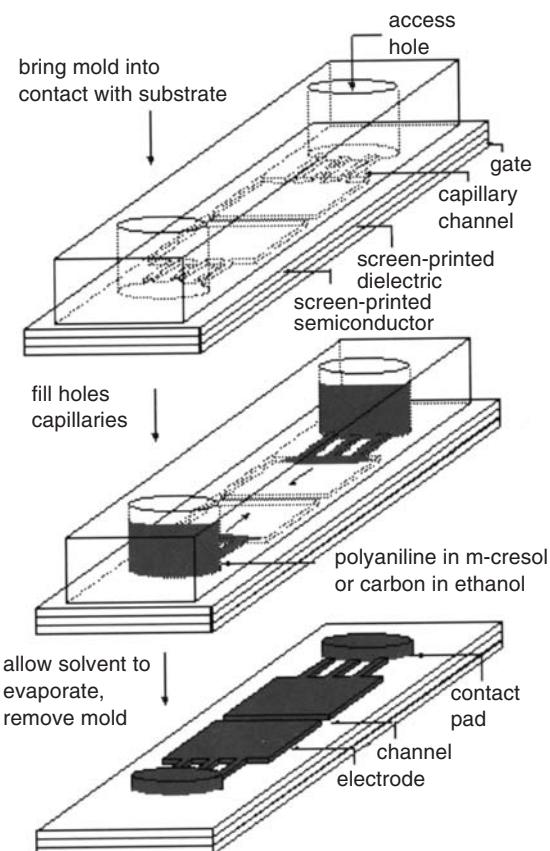


Figure 8.14 Illustration of steps in a micromolding technique for forming source/drain electrodes. Conformal contact of an elastomeric element with relief embossed on its surface forms an array of capillary channels next to the substrate. Placing liquids (e.g., carbon paint, polyaniline in m-cresol) into access holes or reservoirs that lead to entrances to these channels leads to capillary filling. After the liquids solidify to form conducting microstructures of carbon or polyaniline, the mold is removed from the substrate. The resulting nonphotolithographically fabricated organic transistors can have channel lengths as small as $\sim 1 \mu\text{m}$.

using solutions of polyaniline in m-cresol [70]. In both of these cases, evaporation of solvent from the filled capillary channels forces flow of solution from the reservoirs into the channels. If the channels fill with solids before solution from the reservoirs is exhausted, MIMIC produces solid microstructures of carbon or polyaniline in the geometry of the mold. Removal of the mold completes the fabrication. We used this approach to form source/drain electrodes on top of screen-printed dielectrics and organic semiconductors. In this way, we fabricated arrays of high-quality organic TFTs with micron feature sizes, without the use of photolithography [70]. Figure 8.15 shows an optical micrograph of an array of transistors formed in this manner; it also shows characteristics of one of the devices that has a channel width of $\sim 2 \mu\text{m}$. These devices have electrical properties that are consistent with TFTs fabricated using conventional photolithographic techniques.

Although the current version of MIMIC has sufficient resolution, additional research will be required to increase its speed and flexibility in patterning large-scale organic circuits (i.e., noninterconnected circuit patterns are difficult to form directly). One can, for example, conceive of extensions of the technique that use screen and inkjet printing to deliver inks to access holes strategically placed across a complex circuit pattern defined by a large mold. We are currently exploring this

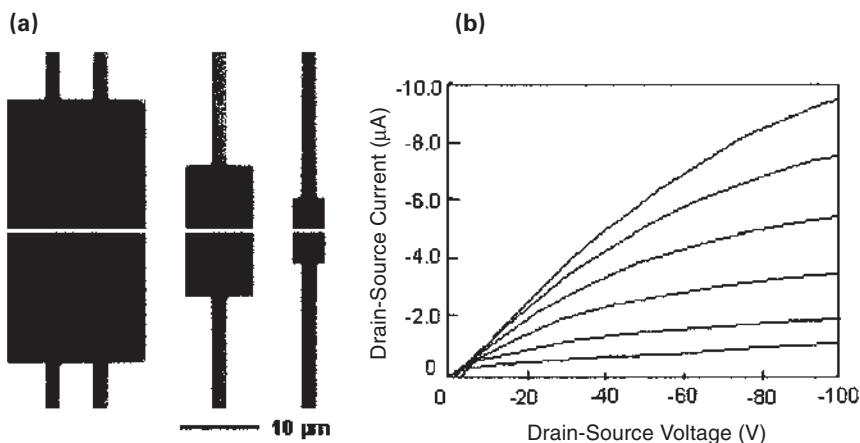


Figure 8.15 (a) Optical micrograph of an array of organic TFTs whose source/drain electrodes consist of polyaniline micromolded with the MIMIC technique. The channel lengths are $\sim 2 \mu\text{m}$. (b) Current/voltage characteristics of one of these transistors, which use solution-cast PHT as the semiconductor. The properties of these devices are consistent with measurements from systems that use silicon substrates and photolithographically defined electrodes.

and other approaches to overcome the limited flexibility in patterning that exists with the basic MIMIC technique; the same strategies may also increase the speed of patterning by reducing the total distance that ink must flow through and solidify in the capillary channels.

8.4.3 Microcontact Printing

The molds used for MIMIC can serve as stamps in a high-resolution form of rubber-stamping known as microcontact printing (μ CP) [71,78]. This technique has many characteristics necessary for the type of rapid, large-volume reel-to-reel processing that is often considered important for cost-effectively exploiting organics in microelectronics. Briefly, μ CP defines, by contact printing, patterns of self-assembled monolayers (SAMs) that can then be used as resists to prevent removal of material or as initiators to guide material deposition [78]. Generally, this technique yields the best results when inks of alkanethiols are used to define monolayer etch resists on the surfaces of ultrathin layers of gold ($<\sim 40$ nm) or silver ($<\sim 300$ nm) [71,78]. The resolution of features that can be etched into the underlying metal films in these cases is remarkably high: ~ 30 -nm features have been demonstrated in 15-nm films of gold [87,88]. Printing requires contact of the stamp for less than ~ 0.5 s, areas of many square centimeters can be stamped at once, and etching is completed in 0.5–5.0 min, depending on the thickness of the metal and the chemistry of the etchant. Although gold and silver are not particularly useful for conventional microelectronics, these materials can yield organic transistors with extremely good characteristics. In thin-film form, they can offer low-cost, low-resistance patterned conductors for source/drain electrodes and associated interconnections.

Our recent work [72,75–77,89–91] with μ CP demonstrates: (1) methods for using cylindrical “roller” stamps mounted on fixed axles for printing, in a continuous reel-to-reel fashion [72,77], high-resolution source/drain electrodes in ultrathin gold and silver deposited from solution at room temperature using electroless deposition [60,76,90,91]; (2) techniques for performing registration and alignment of the printed features with other elements of a circuit, over large areas [91]; (3) strategies for achieving densities of defects that are as good as those observed with photolithography, when the patterning is performed outside of cleanroom facilities [91]; (4) methods for removing the printed SAMs to allow good electrical contact of the electrodes with organic semiconductors deposited on top of them [72,76,89]; and (5) materials and fabrication sequences that can efficiently exploit these printed electrodes for working organic TFTs in large-scale circuits [91].

Figure 8.16 shows the most attractive processing steps for microcontact printing source/drain electrodes and for preparing them for use in organic TFTs. The semiconductors, dielectrics, and gate electrodes are deposited onto the printed electrodes by simply casting these materials from solution, an approach that is

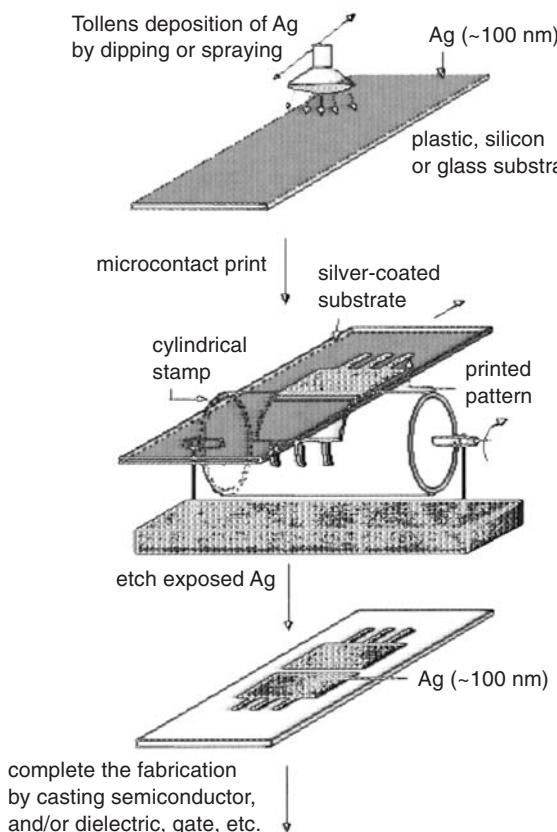


Figure 8.16 Sequence of steps for printing source/drain electrodes for organic TFTs. The procedure begins with solution deposition of a thin film of silver, using electroless chemistries. Printing a self-assembled monolayer on the silver using a roller-type stamp defines the geometry of the electrodes. Etching the unprinted areas of the silver and then removing the monolayer completes the fabrication.

clearly compatible with the screen and inkjet printing techniques described previously. The characteristics of TFTs formed using these techniques are equivalent to those of devices fabricated using photolithography ([Fig. 8.17](#)). In a manufacturing sequence that uses this approach, source/drain electrodes and appropriate interconnections could be printed onto a metallized plastic sheet; other solution-pro-

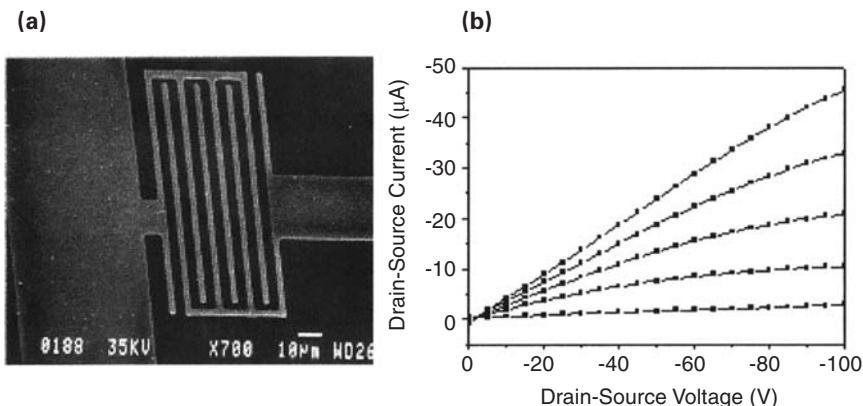


Figure 8.17 (a) Scanning electron micrograph of interdigitated source/drain electrodes formed by microcontact printing on a film of electroless silver. (b) Current–voltage characteristics of a transistor that uses these printed electrodes.

cessable components of the circuits could then be cast or printed on this sheet using relatively minor modifications of existing low-resolution techniques such as screen or inkjet printing. (Fig. 8.18) Electronic paper displays [91], which are described in a following section, illustrate how μ CP can be employed for large-scale, robust systems that use plastic circuits.

8.4.4 Near-Field Photolithography

In addition to their use in MIMIC and μ CP, the transparent elastomeric elements can be implemented as conformable photomasks in a type of near-field photolithographic method [73,93–95]. In this technique, elastomeric phase masks are allowed to “wet,” or come into conformal contact with, the flat surface of a spin-cast film of photoresist. Passing ultraviolet light through the elastomeric mask exposes the resist to the distribution of intensity that exists at the surface of the mask. The surface relief on elements like the one illustrated in Figure 8.13 modulates the phase of light that passes through it. In this mode, the elements act as simple binary-phase masks. If the depth of relief is chosen such that it causes a shift of the phase of the transmitted light by π , then nulls in the intensity appear at each step edge in the relief. The widths of these nulls are of the order of $\sim 0.1 \mu\text{m}$ when $\sim 365\text{-nm}$ light from a conventional mercury lamp is used [93–95].

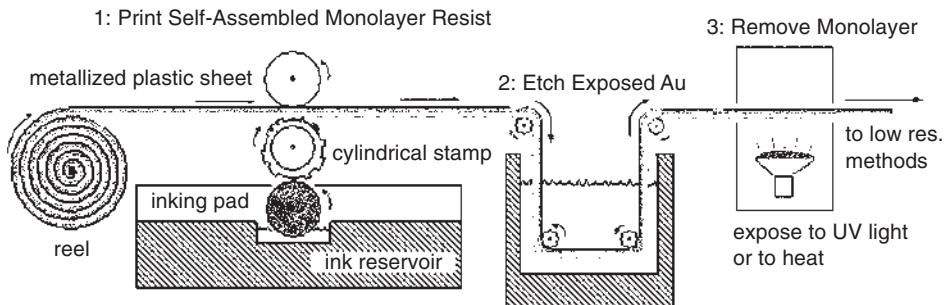


Figure 8.18 Schematic illustration of how microcontact printing might be used in a high-volume, reel-to-reel fabrication sequence for plastic electronics. Fine features (e.g., source/drain electrodes and interconnects) formed by printing could provide the basis for circuits that are completed by screen or inkjet printing the dielectrics, gates, and semiconductors.

These nulls produce, after exposure and development, $\sim 0.1\text{-}\mu\text{m}$ lines in positive photoresist. [Figure 8.19](#) provides an illustration.

Depositing a uniform thin layer of metal onto resist patterned in this manner and then removing the resist with acetone produces slits in the metal film. For applications in organic electronics, $0.1\text{-}\mu\text{m}$ slits in gold are useful for defining narrow separations between source and drain electrodes whose other dimensions are patterned using microcontact printing, for example [74]. [Figure 8.20](#) shows films of gold with a 100-nm slit formed with this technique; it also presents the electrical characteristics of an *n*-channel transistor formed using this structure and a sublimated layer of F_{16}CuPc as the semiconductor. The low-voltage operation of the device derives from its extremely small dimensions (and from a high-capacitance gate dielectric). Other characteristics of these devices and of complementary inverters that are formed with them are presented elsewhere [74]. Although this method suffers from the need to use photoresists and developers, it offers extremely high resolution, it is parallel in its operation, and it is inherently low cost. Its use could be important for applications that demand submicron channel lengths.

8.5 APPLICATIONS OF PLASTIC THIN-FILM TRANSISTORS IN FLEXIBLE DISPLAYS AND IN LOGIC CIRCUITS

8.5.1 Electronic Paper-like Displays

Large-area flexible display systems represent a compelling potential application of the materials and patterning techniques described in this chapter. This section

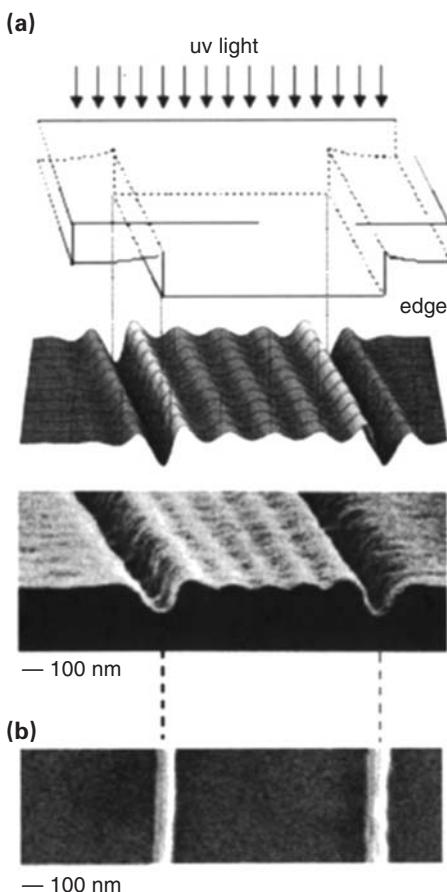


Figure 8.19 The top frame of part (a) shows a schematic illustration of an elastomeric element with relief on its surface. This structure forms a conformable binary-phase mask for a low-cost form of photolithography. The middle frame shows the computed distribution of intensity that exists near the surface of this element when ultraviolet light passes through it and when the depth of relief is such that the phase of the transmitted light is modulated by π . The bottom frame shows a structure in image-reversal photoresist; this pattern results from developing resist that has been exposed to ultraviolet light that passes through the element shown in the top frame. The relief in this resist provides an “image” of the intensity distribution, which agrees with calculation. The key features in these patterns are dips in intensity that exist at the edges of relief. These dips have widths of ~ 100 nm when 365-nm light is used. (b) Lines in positive-one photoresist that is developed after contact-mode exposure using a conformable phase mask similar to the one schematically illustrated in part (a).

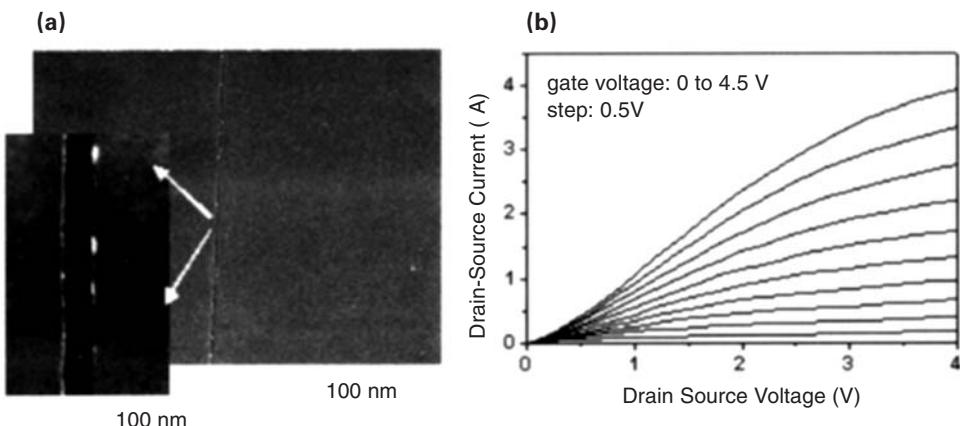
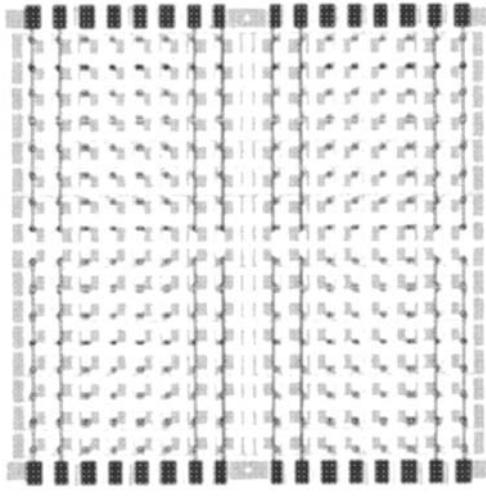


Figure 8.20 (a) Scanning electron micrographs of a narrow slit formed in a film of gold. This structure was formed by lift-off using a narrow line of photoresist patterned with a low-cost form of near-field photolithography. (b) Current–voltage characteristics of a nanoscale transistor that has a channel defined by the gap illustrated in part (a).

summarizes our work on printed organic active-matrix back-plane circuits (256 transistors) for large ($\sim 6'' \times 6''$), mechanically flexible sheets of electronic paper, an emerging type of display [91,92]. These circuits rely critically on (1) μ CP high-resolution ($\sim 1 \mu\text{m}$) circuits with low levels of defects and good registration over large areas, (2) achieving low leakage with thin dielectrics deposited onto surfaces with relief, (3) constructing high-performance organic transistors with bottom-contact geometries, (4) encapsulating these transistors, (5) depositing, in a repeatable way, organic semiconductors with uniform electrical characteristics over large areas, and (6) low-temperature ($\sim 100^\circ\text{C}$) annealing to increase the on/off ratios of the transistors and to improve the uniformity of their characteristics. The sophistication and flexibility of the patterning procedures, the high level of integration on plastic substrates, the large-area coverage, and the good performance of the transistors are all important features of these circuits. A type of electronic paper display can be formed by integrating these circuits with microencapsulated electrophoretic “inks,” as described next.

The back-plane circuit consists of a square array of 256 suitably interconnected *p*-channel transistors. Figure 8.21 shows the circuit layout. Figure 8.22 presents a cross-sectional illustration of a transistor and a top view of a unit cell. The completed display (total thickness ~ 1 mm) comprises a transparent front-plane electrode of indium–tin oxide (ITO) and a thin, unpatterned layer of flexible

(a)



(b)

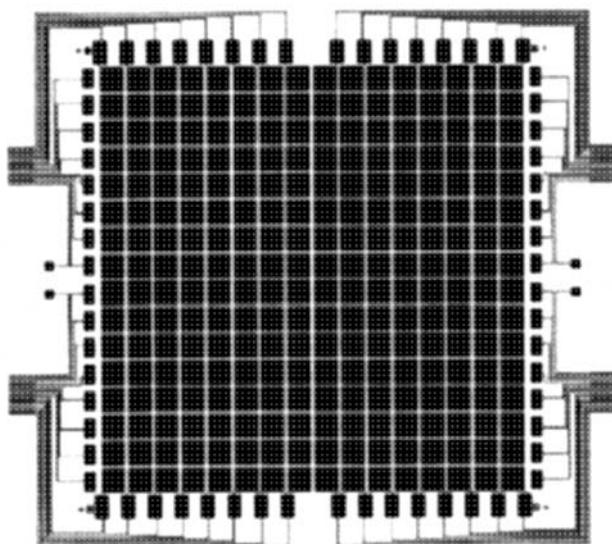


Figure 8.21 Layout of an active-matrix back-plane circuit for a electronic paper-like display. (a) Layout of the source/drain and gate levels. These conductors define an interconnected array of TFTs, each of which acts as a switch to control the color of a pixel in the display. (b) Array of pixel electrodes that connect to electronics on one side and to the optical component of the display (a microencapsulated electrophoretic ink) on the other side.

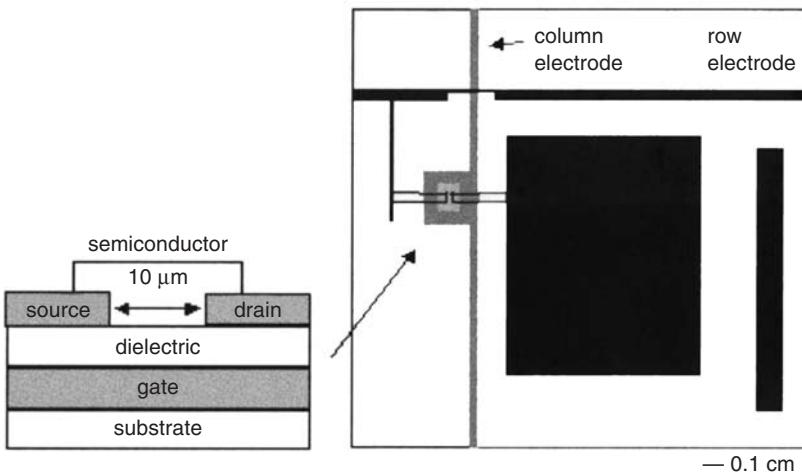


Figure 8.22 Schematic illustration of the cross section of a typical display transistor (left frame). The right frame shows components of a unit cell in a back-plane circuit. The TFTs are bottom-contact devices that use microcontact-printed source/drain electrodes. The unit cell includes a transistor, whose gate electrode is connected to other transistors in the same column and whose source electrode is connected to other transistors in the same row. The drain electrode connects to a large electrode that activates the pixel.

electronic “ink” mounted against a sheet that supports square pixel electrode pads and pinouts; these pixel pads attach, via a conductive adhesive, to the back planes. Each transistor functions as a switch that locally controls the color of the “ink,” which consists of a layer of polymeric microcapsules filled with a suspension of charged pigments in a colored fluid [96,97]. In each of the four quadrants of the display, transistors in a given column have connected gates and those in a given row have connected source electrodes. Applying a voltage to a column (gate) and a row (source) electrode turns on the transistor located at the cell where these electrodes intersect. Activating the transistor generates an electric field between the front-plane ITO and the corresponding pixel electrode. This field causes movement of pigment within the microcapsules, which changes the color of the pixel, as observed through the ITO: When the pigments flow to the ITO side of the capsules, the color of the pigment (white in this case) determines the color of the pixel; when they flow to the back, the pixel assumes the color of the dyed fluid (black in this case). Coordinated control of the transistors is achieved with external circuitry connected to the front plane and to pinouts that lead to the column and row electrodes.

A transistor can switch a pixel (0.8×0.8 cm, resistance ~ 75 M Ω) if it provides at least ~ 1 μ A of “on” current when the gate voltage (V_g) is -50 V and the source/drain voltage (V_{sd}) is -50 V. In order to avoid unwanted switching, the transistors must not produce more than ~ 30 nA of “off” current when $V_g = 0$ V and $V_{sd} = -50$ V, or more than ~ 30 nA of “leakage” current when $V_g = -50$ V and $V_{sd} = 0$ V. The driving scheme demands that the total capacitance associated with each pixel be sufficiently small to allow for millisecond switching times. (Although the refresh time of the entire display is ~ 1 s, the pixels are switched in an approach that requires the transistors to operate at 250 Hz.) This requirement places limits on the area of overlap of the transistor channels and conductors on the source/drain level with the gate level. For the materials choices described in the following sections, channel widths (W) and lengths (L) that satisfy $W/L \sim 10$ produce devices with comfortably more “on” and less “off” current than required. With 10- μ m wires and $L < \sim 20$ μ m, the overlap capacitance can be small enough for millisecond switching times.

These circuits used poly(ethylene terephthalate) (Mylar, ~ 0.1 mm thick) for the substrate and ITO (~ 100 nm thick) for the gate level (ITO-coated sheets of Mylar are commercially available from Southwall Technologies). Patterning a layer of etch resist on these substrates, followed by etching with concentrated hydrochloric acid (~ 30 s) defines the features in the gate level. We demonstrated μ CP (described later), conventional photolithography, and shadow masking to pattern these resists. Back-plane circuits with gates formed using each of these three methods showed identical performance. The resolution required for this level (~ 200 μ m) is relatively low.

A dielectric film deposited onto the patterned ITO insulates the gate and column electrodes from the other elements of the circuit. We used an organosilsesquioxane spin-on glass for this purpose because (1) it can be spin-cast into thin (< 1 μ m) films that show low electrical leakage; (2) it can be cured at low ($< 150^\circ\text{C}$) temperatures; (3) it is chemically compatible with a range of interesting organic semiconductors; and (4) it can be used with etchants employed in the μ CP procedures described in the next section. To minimize the probability of electrical shorting between the source/drain level and the gate level and to reduce the “leakage” currents, we designed the circuit to avoid significant overlap of conductors and semiconductors with features of ITO or their edges. We also used films (~ 0.8 – 1.0 μ m) thick enough for low “leakage” but thin enough to enable sufficient “on” current. Their capacitance was between 2 and 10 nF/cm 2 .

The source/drain level was patterned with μ CP. For the stamps, we used a large-area “master” formed in a thick layer (~ 20 μ m) of resist patterned using a direct-write photolithographic system. To minimize the effects of thermal expansion, we cured the PDMS at room temperature. The spin-on glass/patterned ITO/Mylar substrates were prepared for μ CP by depositing a thin layer of Ti (1.5 nm) as an adhesion promoter, followed by a film of Au (20 nm) using an

electron beam evaporator. Figure 8.23 shows the approach that we used for large-area μ CP. We first placed the stamp, printing side up, on a surface that allowed any residual elastic strains to relax (e.g., a thin layer of oil on a glass plate). Just before inking and printing, we cleaned the stamp using a conventional roller lint-remover. This simple procedure was extremely effective for quickly removing

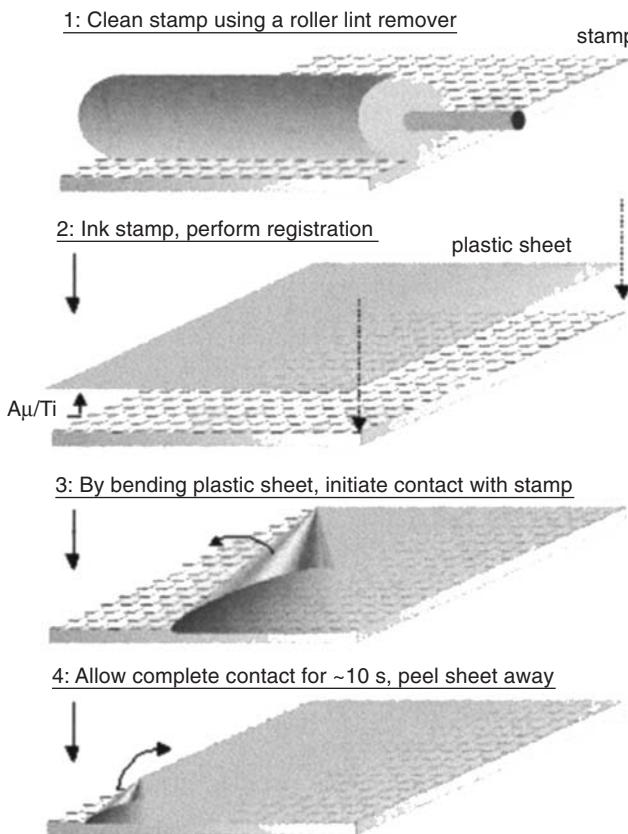


Figure 8.23 Steps for microcontact printing patterns with low defect densities and good registration over large areas. An adhesive roller-type lint remover eliminates dust from the surface of the stamp without contaminating its surface. Aligning, bending, and allowing the flexible substrate to contact the stamp from one edge to the other yields a pattern with low defects and distortions.

dust from the stamp without contaminating or damaging its surface. We then applied, with a pipette, a thin layer of a 2–3 mM solution of hexadecanethiol in ethanol over the entire surface of the stamp. After allowing this “ink” to remain on the stamp for a few seconds, we dried its surface with a stream of nitrogen. Matching crosshair alignment marks on the corners of one edge of the stamp with those patterned in the ITO brings the substrate into registration with the stamp. During this alignment, features on the stamp were viewed directly through the semitransparent substrate. By bending the Mylar sheet, we initiated contact with the stamp on the edge of the substrate that contained the crosshair marks. We then proceeded gradually to unbend the Mylar in order to allow contact to progress across the rest of the surface. This procedure for printing is attractive because it avoids distortions that can arise from mechanical manipulation of the flexible rubber stamp during printing; it also minimizes the number and size of trapped air pockets. The printed gold was etched with an aqueous ferro/ferricyanide solution, and the Ti exposed by removal of the gold was etched away with dilute HF. The substrates were baked on a hotplate at 150°C for 2 hr to remove the SAM.

Depositing a semiconductor on top of the printed substrates yields a functional back-plane circuit. We explored a range of organic materials for this purpose, including many of those described in Section 8.2. For the transistors in this display application, the mobility is not a particularly important characteristic of the semiconductor. The resolution provided by μ CP allows the source/drain electrodes to be designed to produce transistors with large enough “on” currents and sufficiently small overlap capacitance, even with semiconductors that have low mobilities. Also, the current requirement to switch the electronic ink pixel is quite low, on the order of 0.5 μ A/cm². The challenging electrical requirement is the one imposed on the on/off ratio, in order to prevent unwanted switching by residual “off” currents. We found that in many cases, annealing the transistors (e.g., 100°C for ~6 hr in a nitrogen environment) after depositing the semiconductor enabled good, uniform characteristics over the entire surfaces of the substrates. The primary effect of the annealing is to reduce the “off” currents (in some cases by more than 100 times); it also reduces transistor-to-transistor variations in the “on” currents.

Figure 8.24 shows an image of a full printed circuit; the inset displays a micrograph of a transistor. These circuits involve multilevel registration to an accuracy of ~50 μ m over the entire ~6" × 6" of the display circuit; the result easily meets the requirements of this application. Measurements of the number of electrically significant defects in the printed patterns show that typically more than half of the flaws in the printed patterns originate from defects introduced in the photolithography used to produce the masters for the stamps. In all cases (i.e., μ CP and photolithography), dust is the dominant cause of defects. (All processing was performed outside of a cleanroom in an open laboratory environ-

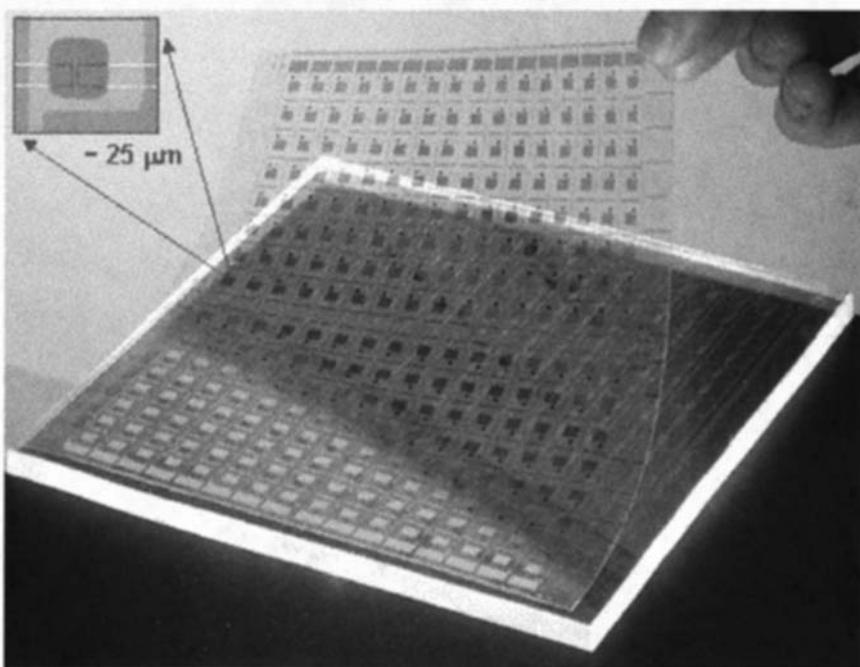


Figure 8.24 Image of a printed, plastic display circuit; the part at the front rests on a stamp that was used to define the source/drain level. The inset shows a top view of one of the transistors.

ment.) The simplicity and effectiveness of our approach to cleaning the stamp, which has no analog in the cleaning of conventional photomasks, as well as the ability of the stamp to conform to small dust particles, minimizes their effects on the printed patterns.

To examine the performance and uniformity of the devices, we probed selected transistors by establishing gate and source contacts at the edges of the circuits and drain contacts at the corresponding unit cell. Figure 8.25 shows, as an example, current–voltage characteristics in two typical transistors that use pentacene as the semiconductor. The gate voltage varies from 0 to -50 V, in steps of 10 V. It was possible to achieve comparable performance in all of the transistors of a complete circuit. Laminating this sheet of circuitry against an unpatterned layer of microencapsulated electrophoretic “ink” produces an electronic paper display. Figure 8.26 illustrates, in an exploded schematic view, all of the elements of these display systems.

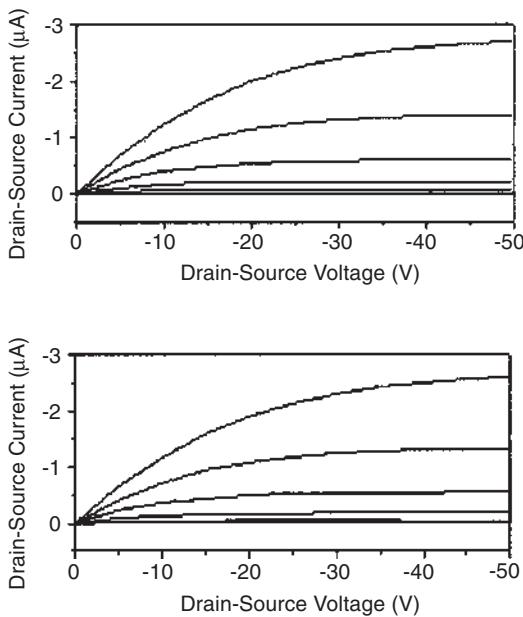


Figure 8.25 Current–voltage characteristics of two typical printed display transistors.

Figure 8.27 shows a sheet of electronic paper (total thickness ~ 1 mm and contrast ratio $>10:1$, significantly better than that of newsprint) that is operating while it is flexed; the bending does not affect its performance. Although these prototype displays do not have the number of pixels necessary for most consumer applications, many of the processing approaches can be extended to systems with more pixels and/or higher resolution. We are not aware, for example, of any fundamental obstacles that will prevent μ CP from being effective at patterning the source/drain and gate levels on length scales of $\sim 1 \mu\text{m}$ with low defect densities and registration to $\sim 5 \mu\text{m}$. This resolution should easily allow for pixels with dimensions of $\sim 100 \times 100 \mu\text{m}$, the smallest size necessary for high-information-content electronic paper.

8.5.2 Logic Circuits

8.5.2.1 Background

There have been several reports on logic circuits with organic transistors [62,98–100]. The approaches to design and build circuits can be broadly classified

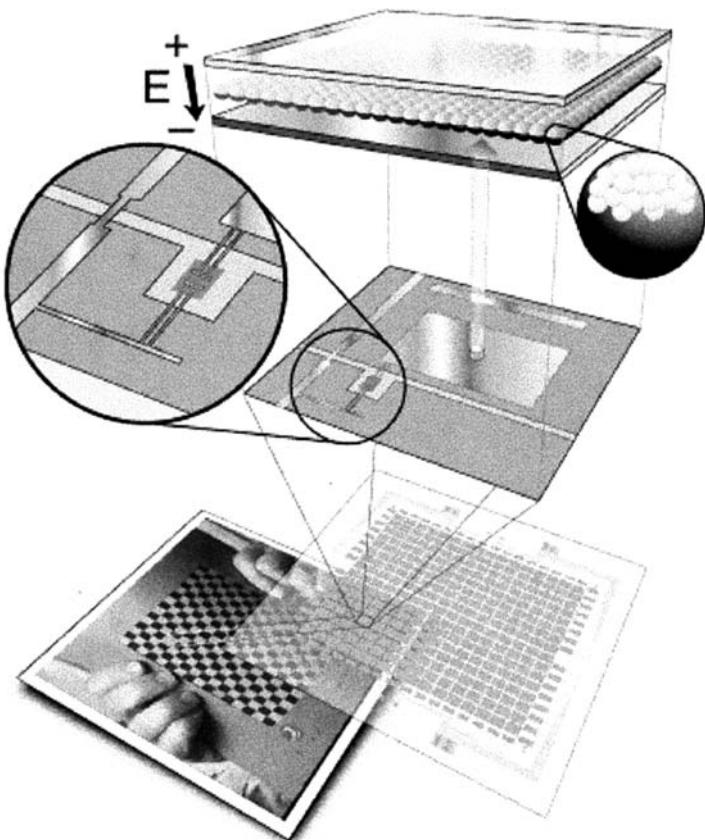


Figure 8.26 Exploded view of the various components of a flexible sheet of electronic paper. An image of an actual display appears at the bottom. The layout of the back-plane circuit is illustrated in the frame that is directly above the display. The middle frames show a unit cell and a closeup view of a transistor. The top frame shows the layer of microencapsulated electrophoretic ink.

into two categories: *p*-FET circuits and complementary circuits. In analogy with Si technology, *p*-FET circuits employ only *p*-channel transistors, whereas complementary circuits require both *p*-channel and *n*-channel transistors. The electronic paper displays described in the previous section are examples of *p*-FET circuits. The advantages of these two approaches will be compared later in this section. The fundamental building block of both types of logic is the inverter, shown

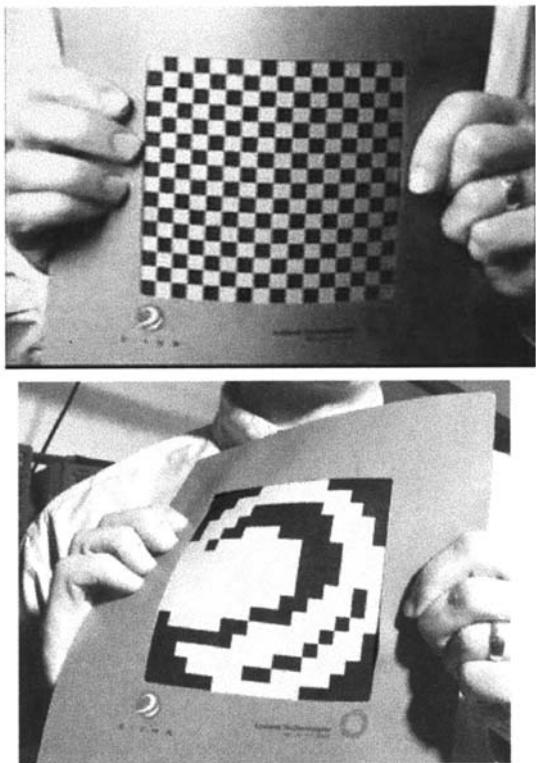


Figure 8.27 Electronic paper-like display, in operation while being bent. The performance and appearance of the display are not affected by bending or off-axis viewing.

schematically in [Figure 8.28](#). Construction of complex circuits requires the development of some more building blocks, also shown in Figure 8.28. For *p*-FET circuits as well as complementary circuits, NOR and NAND gates have been demonstrated. From such blocks, more complex sequential circuits, such as flip-flops, decoders, and shift-registers, can be built. In the case of complementary circuits, it is also possible to construct sequential circuits by using pass transistor logic, a common approach in Si technology. In pass transistor logic, a new element—a transmission gate—is used along with inverters. In general, for CMOS circuits, pass transistor logic-based circuits require fewer transistors and dissipate less power than circuits based on NOR/NAND gates and inverters. The relatively

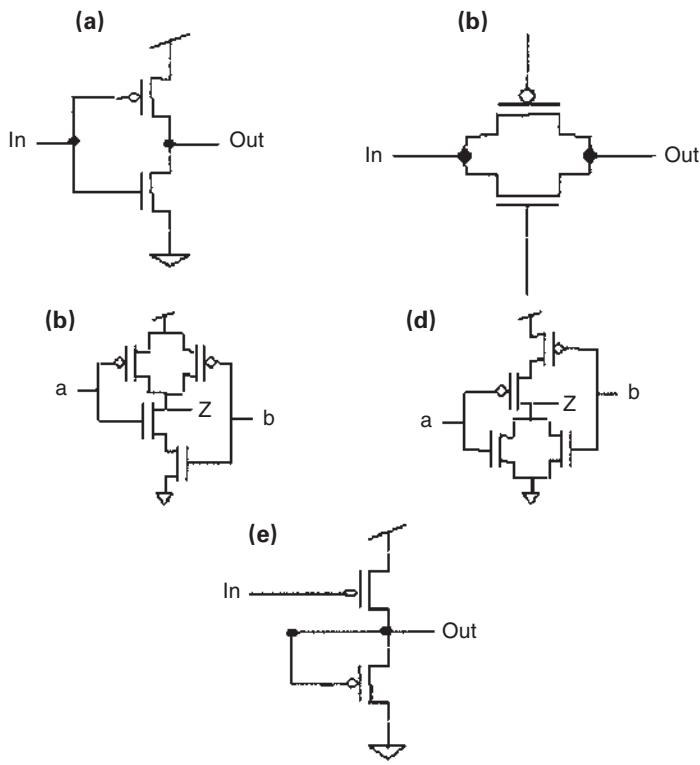


Figure 8.28 (a) A complementary inverter. The TFT on top is the *p*-channel device, and the one on the bottom is the *n*-channel device. These symbols are used throughout this chapter. (b) Complementary transmission gates, (c) Complementary NOR gates, (d) Complementary NAND gates, (e) *p*-FET inverters.

simple layouts of pass transistor logic are convenient for implementation on flexible plastic substrates.

8.5.2.2 Complementary Circuits

Ring oscillators are useful for on-circuit clock generation and also for determining the speed of a given design technology consisting of semiconductor, dielectric, and interconnect materials, and geometrical design rules. The schematic of a five-stage ring oscillator is shown in [Figure 8.29](#). In this demonstration, dihexyl quinquethiophene (DH₆5T) was used as the active material in the *p*-channel

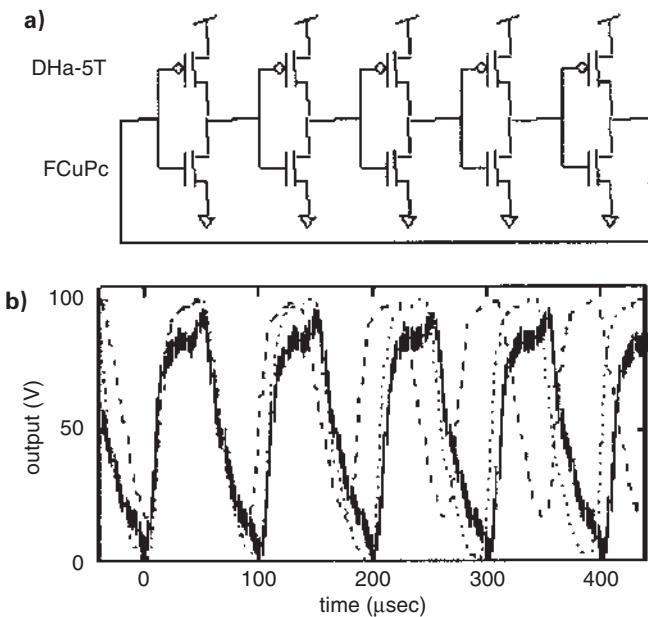


Figure 8.29 (a) Schematic of a five-stage complementary ring oscillator. (b) Response of the ring oscillator. Also shown are two sets of simulated responses described in the text.

FETs and hexadeca copper phthalocyanine ($F_{16}CuPc$) in the n -channel FETs. All transistors have $L = 7.5 \mu m$ and $W = 2 mm$, so an output buffer was not needed. Here low-output impedance is critical, so the free oscillation frequency of an unloaded circuit is measured. Loading the circuit will lower the oscillation frequency. An oscillation frequency of 10 kHz was measured, and voltage swings from 0 V to 95 V. The operating characteristics are also shown in Figure 8.29. This corresponds to a propagation delay per stage of 10 μs . The long dashed simulation used mobility and threshold voltage parameters obtained from discrete FETs near the ring oscillator on the substrate. Values were $\mu_{0p} = 1.76 \times 10^{-2} \text{ cm}^2/\text{V}\cdot\text{s}$ and $\mu_{0n} = 6.7 \times 10^{-3} \text{ cm}^2/\text{V}\cdot\text{s}$ and $V_{Tp} = 26.7 \text{ V}$ and $V_{Tn} = 6.3 \text{ V}$ for the DH_a5T p -channel FET and $F_{16}CuPc$ n -channel FET, respectively. The short dashed simulation used $\mu_{0p} = 1.6 \times 10^{-2} \text{ cm}^2/\text{V}\cdot\text{s}$ and $\mu_{0n} = 6.7 \times 10^{-3} \text{ cm}^2/\text{V}\cdot\text{s}$ and $V_{Tp} = 6.7 \text{ V}$ and $V_{Tn} = 6.3 \text{ V}$ for the DH_a5T p -channel FET and $F_{16}CuPc$ n -channel FET, respectively. This involves a small decrease in the p -FET mobility and a large decrease in its threshold voltage, and it provides much

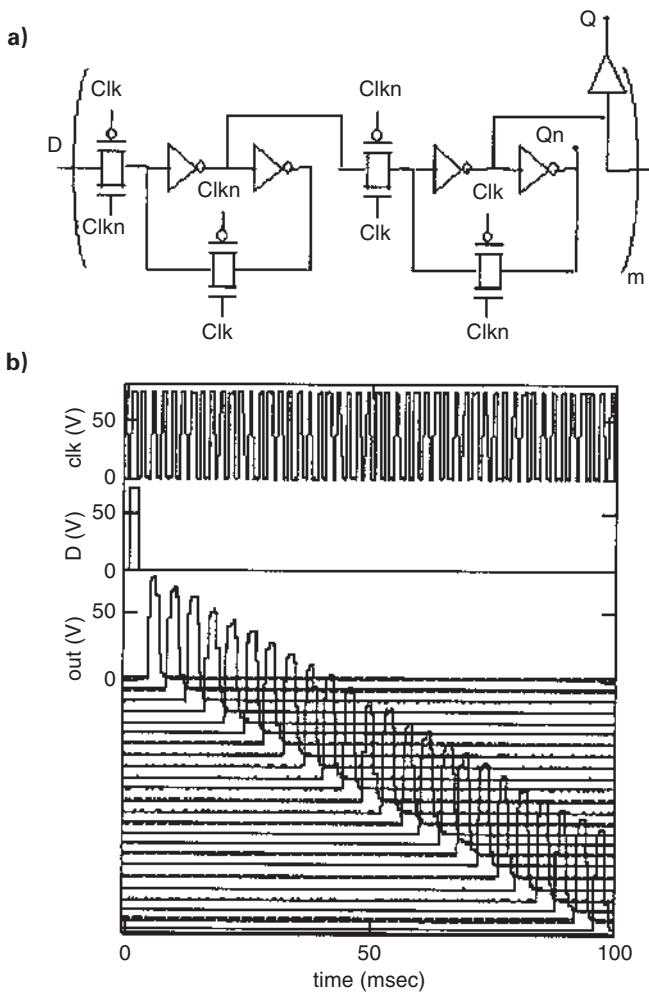


Figure 8.30 (a) Schematic of a multistage complementary shift register. (b) Characteristics of a 48-stage shift register. Only the responses of every other stage are shown.

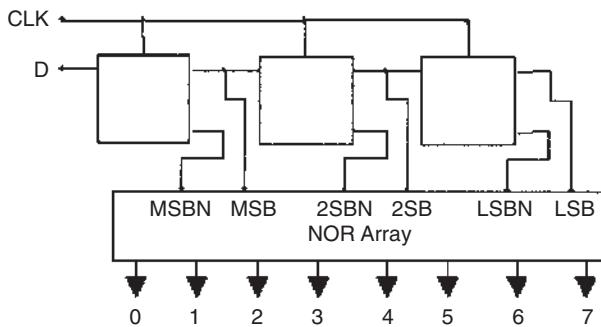
better agreement with the measured data. Improvements in ring oscillator speed can be obtained by increasing the current the FETs supply (for instance, by higher carrier mobilities or shorter channel lengths) or by decreasing the amount of charge needed to switch an inverter (for instance, by reducing the source/gate and drain/gate overlap capacitances or shorter channel lengths). The ultimate speed possible will be determined by the available materials parameters and the design constraints. It is expected that thin-film-based circuits will have a higher oscillation frequency as the carrier mobility is increased.

Complementary sequential logic circuits (circuits that are clocked) that have been implemented include row decoders and shift registers. The largest circuit that was evaluated was a 48-stage shift register with 24 output buffers. The total number of transistors in this circuit is 864, and the channel length of each transistor is $7.5 \mu\text{m}$. Each stage of the shift register is a D flip-flop, with the output of one stage connected to the input of the next. The clock and its complement drive all the stages. Every second stage has an output buffer, which consists of two inverters with large transistors to facilitate probing without loading the circuit. Shift registers are ubiquitous in digital systems and can perform many functions. One function is to shift a “bit” in an orderly and predictable manner from one stage to the next every clock cycle. The operation of the shift register just described is illustrated in [Figure 8.30](#) in which the clock, data, and output of the 24 output buffers are plotted as a function of time. The data consists of a single bit, which is sequentially shifted over all stages of the register. Two-stage shift registers have been operated at clock rates of up to 1 kHz. The operating voltage is 80 V because of the thick gate dielectric employed. Utilizing thinner or higher- k dielectrics [60,101], the operating voltage as well as the power dissipation can be reduced.

The static current drawn by the 48-stage register, including the output buffers, is $70 \mu\text{A}$, and that drawn by a smaller two-stage register (with one buffer/stage) is $7.6 \mu\text{A}$. In comparison, two-stage complementary shift registers based upon NOR/NAND gates required more than twice as many transistors as the two-stage pass transistor logic-based shift register and drew $20 \mu\text{A}$. The static current drawn by CMOS registers can be further reduced by reducing the off-current of the transistors. The lower power dissipation of complementary circuits will be an important factor in applications such as RF tags, which are powered by the ambient field.

The schematic of a three-bit row decoder is shown in [Figure 8.31](#). This decoder is designed so that a single serial input activates one of eight outputs. It consists of three D flip-flops and a NOR array. The output of the three flip-flops and their complements drive the NOR array, which is configured so that for any given set of inputs only one output is high. The characteristics of the decoder are shown in [Figure 8.32](#). The circuit used for the NOR array is significant for yet another reason. It can be seen that four transistors are serially connected

a)



b)

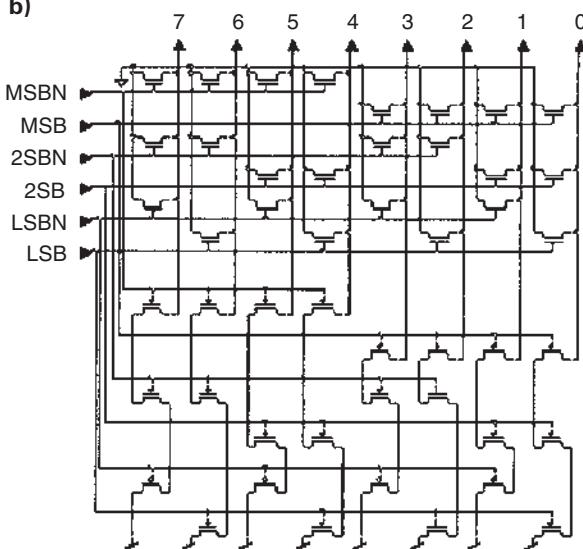


Figure 8.31 (a) Schematic of a three-bit row decoder. (b) Details of the NOR array.

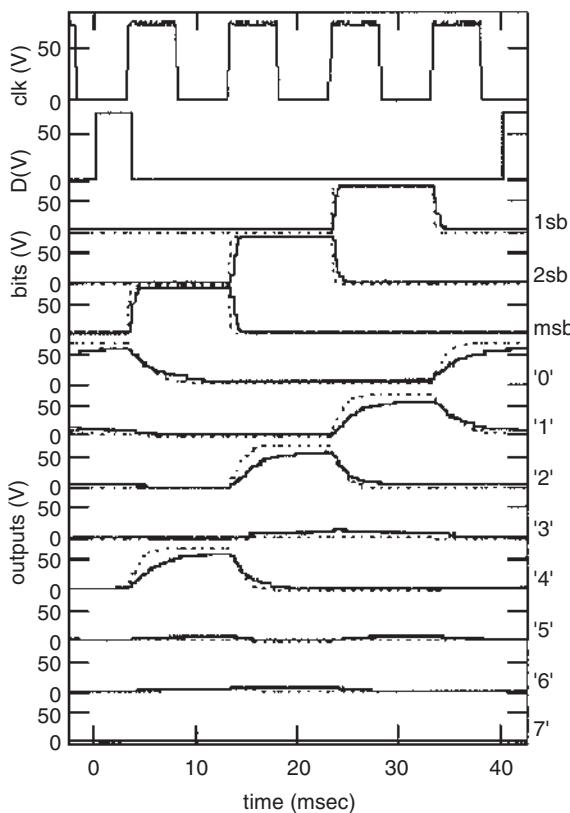


Figure 8.32 Measured response of the three-bit decoder. The clock, data, and three inputs are shown together with the eight outputs. Also indicated is the simulated response, in dashed lines.

between supply and ground. Such “four deep” connections are often employed in silicon arithmetic and logical unit (ALU) circuits. The fact that such a configuration has been shown to work for organic semiconductors suggests that complex logic gates such as those used in ALUs and simple microprocessors can be constructed out of organic TFTs.

There are other ways of implementing organic-based complementary circuits. One approach is the combination of inorganic *n*-channel FETs with organic *p*-channel FETs. Inverters [102] and ring oscillators [103] have been realized with this approach. Another technique is the use of transistors that can act as *n*-

channel or *p*-channel FETs, depending on the bias conditions. Such devices require that both electron-and hole-accumulation layers be formed in a single device. This method of building organic-based complementary circuits was proposed by Dodabalapur and coworkers [104].

We now address the question of comparing the performance of complementary and *p*-FET circuits. Clearly, *p*-FET circuits have the important advantage of simplicity; it is necessary to have only one active material. Complementary circuits require two types of active material and also patterning of the active semiconductor materials so that *p*-FETs are formed in selected areas of the circuit and *n*-FETs are formed in other areas of the circuit. Simulations indicate that the current drawn by shift registers based on *p*-channel transistors alone is greater than that of complementary shift registers of comparable transistor dimensions and speed. The static current drawn in *p*-channel TFT registers depends strongly on the nature of the load (whether enhancement or depletion), the on/off current ratio, and the ratio of the dimensions of the transistors that constitute the basic gates (NOR, NAND, and inverter). Simulations indicate that for devices with on/off current ratios of about 100, *p*-FET registers dissipate about 25 times more power than complementary circuits. The power dissipation difference between complementary and *p*-FET circuits increase with increasing on/off ratio.

Recent advances in the materials chemistry has made it possible, for the first time, to create a complementary circuit in which the two active materials are both deposited from solution [105]. This will make the fabrication of circuits much easier, for many low-cost, unconventional patterning methods [68] can be employed. This advance will also diminish the differences in fabrication complexity between *p*-FET circuits and complementary circuits, making complementary circuit designs more attractive for a variety of applications. There have been reports of the successful application of novel fabrication techniques, such as microcontact printing [91], that is likely to have a huge impact on the fabrication of organic circuits—both complementary and *p*-FET.

8.5.2.3 *p*-FET Circuits

p-FET-based organic circuits were pioneered by the Philips group [62]. The fastest switching speeds that have been obtained with this technology is a few kilohertz [100]. Integration scales have reached a few hundred transistors in a 15-bit code generator circuit. The basic building block—the inverter—can be configured in more than one way, depending on whether the transistors are depletion mode or enhancement mode. It is also possible to use resistor loads, although the inverter gain, defined as $\Delta V_{\text{out}}/\Delta V_{\text{in}}$ is reduced. In *p*-FET technologies, inverter gains as large as 12 have been demonstrated.

8.6 CONCLUSIONS

This chapter presented an overview of our recent work in the area of organic thin-film transistors, from materials to physics to patterning techniques to circuit

and device applications. These results and the progress of other groups in this field point to a promising future for plastic circuits, particularly in areas (e.g., paper-like displays) where they bring new capabilities (e.g., mechanical flexibility) to conventional electronic systems.

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9

Polymer Transistor Circuits Fabricated by Solution Processing and Direct Printing

Henning Sirringhaus and Richard Friend

Cavendish Laboratory, University of Cambridge, and Plastic Logic Ltd., Cambridge, United Kingdom

Takeo Kawase

Cavendish Laboratory, University of Cambridge, and Epson Cambridge Laboratory, Cambridge, United Kingdom

Lukas Buergi

Cavendish Laboratory, University of Cambridge, United Kingdom

9.1 INTRODUCTION

This chapter is focused on organic thin-film transistor (TFT) devices and circuits based on conjugated polymer semiconductor active layers. Its goal is to illustrate some of the key device fabrication and device physics issues that distinguish polymer TFTs from conventional thin-film silicon devices. These are related to the different methods of device manufacturing by solution processing and direct printing, as opposed to conventional vacuum deposition and photolithography,

and to the nature of charge transport in polymer semiconductors. For convenience, illustrative examples have been chosen mainly from work done in the Cambridge group, with reference made, where appropriate, to the excellent work of other groups. Related work on devices based on small molecular semiconductors and conjugated oligomers has been excluded deliberately because it is covered in depth in other chapters in this volume and elsewhere [1–3].

9.2 HISTORICAL OVERVIEW

The observation of field-effect operation in conjugated polymer TFT structures [4,5] was one of the key milestones in the field of polymer optoelectronics. It demonstrated, for the first time, clean, semiconducting device operation in undoped conjugated polymers and allowed controlled experimental investigation of the polaronic nature of charge carriers in conjugated polymers [5]. It led to the discovery of electroluminescence in conjugated polymer light-emitting diodes [6] and to other useful semiconductor device properties [7].

Polymer field-effect transistors have been fabricated in different device configurations, such as metal–semiconductor field-effect transistors with Schottky gates [8], grid triode structures [9], and bipolar devices [10,11], but the thin-film transistor architecture is the simplest and most common configuration. Following the initial demonstrations, a broad range of conjugated polymer materials was explored, such as polythiophene [4,12], polyacetylene [13], polythienylenevinylene [14], polyphenylenevinylene [15], polypyrrole [16], and polyaniline [17].

In most of these polymers, field-effect mobilities were reported to be less than 10^{-4} cm²/V-s. This is much too low for most practical thin-film electronic applications, and, until recently, research into polymer transistors remained motivated mainly by scientific interests. Only in cases where the polymer semiconductor was highly doped were mobilities on the order of 0.1 cm²/V-s achieved, resulting, however, in very low ON–OFF current switching ratios [14,17]. The low mobility values reflect the disordered, amorphous microstructure of most solution-deposited conjugated polymer thin films, and can be well understood by models developed for hopping transport in molecular organic materials used in xerography [18]. In such disordered hopping systems the mobility can be increased by doping, resulting in a reduction of the distance between hopping sites. However, this also increases the bulk conductivity, and the ON–OFF current switching ratio diminishes with increasing doping concentration. A “universal” relationship was observed between field-effect mobility and ON–OFF current ratio for doped, amorphous organic semiconductors [19]. The highest mobility reported for a polymer TFT with an undoped, amorphous polymer semiconductor of polythienylene vinylene has been on the order of 10^{-3} cm²/V-s [20].

It was recognized early that another way to enhance mobilities was to improve the degree of structural order of the polymer film. Various techniques

were used to affect the microstructure of the thin polymer film in the TFT device, such as Langmuir–Blodgett deposition [21,22], polymer alignment by mechanical rubbing [23], attachment of mesogenic end groups to the polymer backbone [24], and better structural regularity of the polymer backbone [25]. In these early experiments only modest improvements of mobility due to a higher degree of polymer alignment and structural order were observed. In a partially ordered hopping system the charge carrier mobility remains limited by the most difficult hopping events encountered by a carrier when moving from source to drain. Even if the degree of local order is enhanced, the mobility remains determined by the disordered regions of the film.

The first polymer TFT material in which a clear, dramatic correlation between microstructure and mobility was observed was self-organizing, highly regioregular, poly-3-hexylthiophene (P3HT), for which high field-effect mobilities of $0.045 \text{ cm}^2/\text{V}\cdot\text{s}$ were reported [26]. It was shown that in P3HT a very sensitive dependence of the mobility on the degree of head-to-tail regioregularity and the degree of micrococrystallinity exists, with mobilities of $0.1 \text{ cm}^2/\text{V}\cdot\text{s}$ achieved for regioregularities exceeding 95% [27,28]. Recently, even higher mobilities of $0.2 \text{ cm}^2/\text{V}\cdot\text{s}$ have been reported for regioregular P3HT in a top-gate configuration with a polymer dielectric [29]. Another, more recent example, for which a clear enhancement of field-effect mobility with polymer alignment has been seen, are self-organizing poly-dioctylfluorene-based copolymers, in which uniaxial polymer alignment was achieved by bringing the polymer into a thermotropic liquid crystalline phase on top of an alignment layer [30]. Using liquid crystalline self-organization in poly-dioctylfluorene-*co*-bithiophene (F8T2) mobilities of $0.02 \text{ cm}^2/\text{V}\cdot\text{s}$ were reported. These dramatic improvements in mobility by several orders of magnitude have allowed entrance to an interesting, new transport regime, in which the charge transport in the TFT is no longer dominated by the amorphous regions in the films and in which a direct correlation between microstructure and mobility can be observed.

In terms of practical applications, the highest mobility values achieved with polymer TFTs are still lower by about one order of magnitude than those of most other TFT technologies represented in this volume. At the present stage, polymer TFTs offer little or no performance advantages compared to thin-film silicon devices, but they have several unique processing attributes that distinguish them from other TFT technologies. For applications on flexible plastic substrates, where mechanical robustness and processing at temperatures below 150°C are required, conjugated polymer plastics that can be coated from solution at room temperature appear to pose fewer technological challenges than thin-film silicon devices that tend to require higher processing temperatures [31]. Thin polymer films can be deposited from solutions in common organic solvents by solution-coating techniques and are therefore attractive for large-area applications. Most importantly, polymers can be formulated into inks that are compatible with a range of direct

printing techniques. Whereas thin-film silicon TFTs are fabricated by a combination of vacuum deposition and photolithographic patterning, all-polymer TFTs, comprising polymer semiconductors as active, switchable layers, conducting polymers as electrodes and interconnects, and conventional polymers as gate and interlayer dielectrics, can in principle be manufactured by successive solution deposition and direct printing techniques. This opens the possibility of fabricating thin-film electronic integrated circuits by techniques similar to the printing of newspaper. If this becomes possible, it will result in a dramatic reduction in cost, enable thin-film electronic circuits on large areas, and open the way to a range of new thin-film electronic applications that are currently not viable due to the high costs and area limitations of conventional TFT manufacturing technologies.

Several approaches have been followed for solution-based fabrication of polymer TFTs and integrated circuits. All-polymer logic circuits consisting of a few hundred transistors were first demonstrated by a group at Philips Research Laboratories in Eindhoven, The Netherlands, who developed a photolithographic technique for patterning polyaniline conducting polymer electrodes by ultraviolet (UV) irradiation [32]. The UV light exposure reduces the conductivity of the polyaniline in the irradiated areas, defining a pattern of conducting source-drain and gate electrodes as well as interconnects. Recently, the group has reported on further process improvements, including the photochemical removal of the polyaniline in the irradiated areas as well as a photochemical definition of via-hole interconnects [33]. Programmable code generators consisting of 300 transistors were reported operating at a bit rate of up to 100 bits/s. Integrated logic circuits of similar complexity and impressive performance have also been demonstrated using small organic molecules deposited at the last stage of an otherwise conventional silicon process [34].

In addition to such more conventional manufacturing approaches, several nonconventional, direct printing approaches have also been developed. Screen printing has been used to pattern source-drain and gate electrodes of conducting inks with channel lengths on the order of 100 μm [35,36]. Soft lithographic techniques based on polydimethoxysilane (PDMS) stamps have been used to selectively deposit self-assembled monolayers onto thin films of gold that can be used as etch masks for the etching of gold source-drain electrodes [37,38]. Using PDMS stamps as phase-shift masks in a photolithographic process, gold source-drain electrodes have been defined with channel lengths of only 0.1 μm [39]. Selective solution deposition of polymer electrodes has been achieved by micromolding in capillaries (MIMIC) [40,41]. Recently, high-resolution inkjet printing techniques have been developed that allow fabrication of all-polymer TFT circuits with less than 5- μm channel lengths [42].

Due to these recent performance improvements and process developments, polymer TFTs are now an emerging TFT technology with serious potential in application areas where low-cost, low-temperature processing on flexible plastic

substrates or large-area capability are important requirements [43]. The first commercial activity in polymer electronics has recently been launched. Plastic Logic, a Cambridge-based startup company (www.plasticlogic.com), is developing novel manufacturing processes for printed polymer integrated circuits.

This chapter gives an overview of important issues that are specific to this class of TFTs. In Section 9.3, polymer TFT device physics and charge transport mechanisms are discussed. The interplay between TFT device performance and polymer self-organization is the topic of Section 9.4. In Section 9.5, a detailed description is given of the inkjet printing approach for the manufacture of polymer TFT circuits. Finally, in Section 9.6, the potential of polymer TFTs in different application areas is assessed.

9.3 DEVICE PHYSICS

Although the charge transport physics of conjugated polymers is in many respects different from that of inorganic thin-film silicon, polymer transistors exhibit device characteristics that are similar in many respects to those of thin-film silicon TFTs. [Figure 9.1](#) shows output and transfer characteristics of P3HT TFTs with two different channel lengths fabricated on a Si/SiO₂ substrate. The highly doped silicon wafer acts as the gate electrode and the thermal SiO₂ layer as the gate dielectric. Gold source–drain electrodes are defined either by photolithography prior to deposition of the polymer (“bottom source–drain contact” configuration) or by shadow-mask evaporation after deposition of the polymer by spin-coating (“top source–drain contact” configuration). This hybrid organic–inorganic device configuration is commonly employed because device fabrication is straightforward and the use of a well-characterized inorganic dielectric allows one to focus on the charge transport properties of the polymer semiconductor itself.

The field-effect mobility extracted from the transfer characteristics is 0.05–0.1 cm²/V·s, depending on the details of device preparation and device configuration. As for most polymer TFTs, the device operates in *p*-type accumulation mode. To the best of our knowledge, high-mobility TFTs operating in *n*-type mode have been reported only for carefully purified small conjugated molecules such as fluorinated copper phthalocyanines [34], oligothiophenes [44], and naphthalene tetracarboxylic dimides [45], but not for solution-processed polymers. This is attributed mainly to the role of impurities such as atmospheric oxygen acting as traps for electrons. The current in the output characteristics has been normalized via multiplication by the channel length in order to show channel-length-scaling behavior. The $L = 20\text{ }\mu\text{m}$ device exhibits characteristic long-channel operation, with a linear increase of the current at small source–drain voltages in the output characteristics ($V_{sd} \ll V_g$), good current saturation in the saturation regime ($V_{sd} > V_g - V_T$), and a low OFF-current on the order of 1 pA. The $L = 2\text{ }\mu\text{m}$ device exhibits features that are characteristic of short-channel

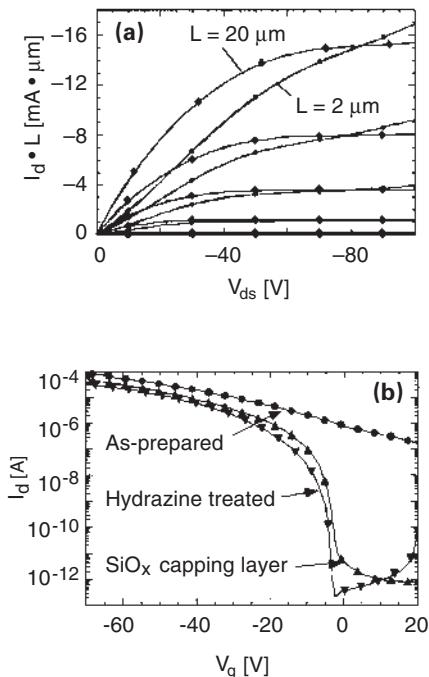


Figure 9.1 (a) Output characteristics of bottom-gate P3HT TFTs fabricated on a SiO_2/Si substrate with $L = 2$ and $20 \mu\text{m}$, respectively ($W = 1 \text{ cm}$). The output characteristics are normalized via multiplication by the channel length. (b) Transfer characteristics of an as-deposited device ($L = 20 \mu\text{m}$) fabricated in a N_2 atmosphere and of devices fabricated under the same conditions but subjected to an additional reductive treatment of the P3HT surface performed either by exposure to hydrazine or by deposition of a substoichiometric layer of SiO_x onto the surface of the device.

TFTs, such as a nonlinear increase in the current with source–drain voltage due to current limitations by parasitic contact resistance, finite slope of the output characteristics in the saturation regime, and an increased OFF-current compared to the long-channel device [46].

The device is normally on; i.e., a positive, reverse turn-on voltage $V_0 = 0\text{--}5 \text{ V}$ is required to turn the device off. This is believed to be caused by the combination of two effects. Firstly, the bulk of the P3HT semiconductor is extrinsically *p*-type doped due to residual impurities and the sensitivity of P3HT to doping by exposure to oxygen and moisture. A reverse voltage is required to

deplete the bulk of the polymer film. From a Mott–Schottky analysis ($1/C^2$ versus V) of the capacitance–voltage characteristics (Fig. 9.2a) we extract estimates of the acceptor concentration of $5 \cdot 10^{15} \text{ cm}^{-3}$ to $5 \cdot 10^{16} \text{ cm}^{-3}$, depending on the device preparation conditions and the batch of polymer. Secondly, the capacitance–voltage characteristics of the P3HT MIS diode shown in Figure 9.2a clearly indicate that the flatband voltage is positive; i.e., an accumulation layer exists at the polymer–dielectric interface even a zero gate voltage. From the difference

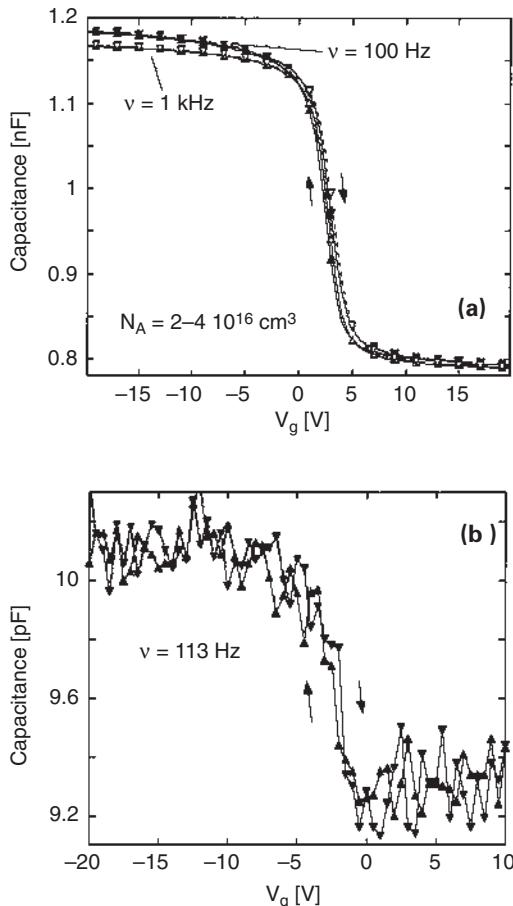


Figure 9.2 Capacitance–voltage characteristics of (a) n^+ Si-SiO₂-P3HT-Au and (b) PEDOT-PVP-F8T2-PEDOT metal–insulator–semiconductor diodes.

in work function between the n^+ -Si gate and the Au source–drain electrodes, a negative flatband voltage would have been expected. For comparison, [Figure 9.2b](#) shows corresponding capacitance–voltage characteristics of an all-polymer TFT device based on F8T2. F8T2 exhibits higher stability against doping by atmospheric oxygen and other impurities, and F8T2 TFTs tend to be normally off, with a negative turn-on voltage V_0 . In this case V_0 reflects the density of charge carrier traps in the F8T2 polymer semiconductor ($n_t \approx C_i - V_0 \approx 10^{11} \text{ cm}^2$) that need to be filled before an accumulation layer can be formed. The slope of the Mott–Schottky plots is similar to that of the P3HT devices, in spite of the higher stability of F8T2 against chemical doping. It is believed that this reflects the existence of localized electronic trap states in the energy gap that tend to stretch out the capacitance–voltage characteristics.

One of the critical steps to achieve the high ON–OFF current ratio in P3HT TFTs has been the reduction of unintentional residual extrinsic doping in the polymer film. Highly regioregular P3HT is sensitive to air and moisture exposure [26]. Devices prepared in air show very low ON–OFF current ratios on the order of 10–100. The ON–OFF characteristics can be improved by performing all solution-preparation and device-processing steps under dry nitrogen. However, even in N_2 atmosphere with a residual oxygen concentration of typically 2–4 ppm, some extrinsic doping is difficult to avoid. High reverse gate voltages are typically required to turn the as-prepared transistors off ($V_0 > 40 \text{ V}$), i.e., to deplete the bulk of the polymer film. When the films are exposed to a chemical reducing agent, the ON–OFF characteristics are dramatically improved ([Fig. 1b](#)). After deposition of a thin capping layer of substoichiometric SiO_x ($x < 2$) onto the surface of the polymer film or after exposure of the films to reducing hydrazine vapor, FETs tested under N_2 atmosphere exhibit a sharp turn-on around $V_0 = 0 \text{ V}$, with an ON–OFF current ratio exceeding 10^6 . Photothermal deflection spectroscopy (PDS) experiments, which allow a very sensitive measure of low coefficients of absorption, show that subgap optical absorption features between 1.3 and 1.8 eV below the $\pi-\pi^*$ absorption of the neutral polymer are significantly reduced during the reductive treatments [46]. These optical transitions are attributed to charge-induced absorption from extrinsic polaronic charge carriers. The increase in the ON–OFF current ratio is clearly correlated with the dedoping of the film. It is important to note that the mobility extracted from the transfer characteristics is not affected by the dedoping process [27,46]. It is not clear at present whether the sensitivity of P3HT to unintentional doping is caused by the intrinsic low ionization potential of the polymer or whether it is related to residual impurities left from the synthesis.

P3HT has been the first conjugated polymer in which it is possible to obtain simultaneously high mobilities of $0.1 \text{ cm}^2/\text{V}\cdot\text{s}$ and high ON–OFF current ratios over 10^6 . Previously this was achieved only in FETs of small-molecule and oligomer materials carefully purified by vacuum sublimation [47]. The high mobilities

obtained in P3HT TFTs cannot be explained by the “universal” relationship between conductivity and mobility that is seen in many amorphous polymer networks as a function of doping concentration [19]. The simultaneous demonstration of high mobilities and high ON–OFF current ratios in P3HT TFTs is an important step toward investigating the intrinsic transport properties of ordered conjugated polymers (see Sec. 9.4).

In the following we investigate in more detail the device physics of P3HT TFTs, in particular the dependence of the field-effect mobility on charge carrier concentration and electric field. The structural disorder in a polymer film gives rise to localized electronic states that result in a dependence of the field-effect mobility on the gate voltage, i.e., carrier concentration, and on the lateral electric field in the channel. Understanding quantitatively this dependence is important, particularly in the context of device modeling. Here we discuss two methods to determine experimentally the field and charge carrier concentration dependence of the mobility.

The first method is based on a careful analysis of the channel length and gate voltage dependence of the device characteristics. In order to extract the dependence of the mobility on gate voltage, we apply a model developed for a-Si TFTs [48]. The model takes into account an energy-dependent density of states with localized, low-mobility electronic states induced by disorder below a charge transport level (CTL) at which most of the current transporting carriers are located. In the gradual channel approximation, the TFT current in the linear and saturation regime is given by [48]

$$I_d(V_g, V_{sd}) = \frac{C_i \cdot W}{L} \mu_{\text{FET}}^{\text{in}}(V_g, V_{sd}) \cdot (V_g - V_T) \cdot V_{sd} \quad (9.1)$$

$$\frac{\partial I_{\text{sat}}(V_g)}{\partial V_g} = \frac{C_i \cdot W}{L} \mu_{\text{FET}}^{\text{sat}}(V_g, V_{sd}) \cdot (V_g - V_T) \quad (9.2)$$

where C_i is the insulator capacitance and W is the channel width. It is assumed that the charge carrier concentration induced by the gate field at the source electrode increases linearly with V_g above the threshold voltage V_T , that is, $n_{\text{ind}} = C_i(V_g - V_T)$. As in the case of a-Si devices, V_T is determined by fitting the transfer characteristics to a power law and extrapolating to zero current. The field-effect mobility can then be calculated from the measured values of I_d and dI_d/dV_g in the linear and saturated regimes, respectively. Note that in the case of a gate-voltage-dependent mobility, the saturation current does not simply increase with the square of the gate voltage. In order to obtain reliable mobility values using this method, the measured device characteristics need to be corrected carefully for source–drain parasitic resistance and short-channel effects [46].

The second, more reliable method to extract mobilities is based on spatially resolved Kelvin probe microscopy performed on operating TFT structures using an atomic force microscope (AFM) with a conducting cantilever [49,50]. The

AFM is operated in noncontact mode under ultrahigh vacuum conditions in a temperature range from 20 to 300 K. An oscillating electrical voltage is superimposed onto the tip bias voltage V_t and applied to the cantilever, and the resulting shift of the resonance frequency of the cantilever Δf_r is measured. This shift is proportional to the local gradient of the electrostatic force F_{el} between the sample and the cantilever tip:

$$\Delta f_r \propto \frac{\partial F_{el}}{\partial z} \propto \frac{\partial^2}{\partial z^2} C(\bar{x}, z) \cdot [V_t - V(\bar{x}) - \Delta\Phi(\bar{x})]^2 \quad (9.3)$$

where $C(x, z)$ is the capacitance of the tip-sample junction and $\Delta\Phi(\bar{x})$ is the work function difference between the TFT sample and the conducting AFM tip. By measuring the resonance frequency shift as a function of position along the channel of a TFT device under operating conditions, this technique allows one to obtain a direct map of the two-dimensional electrostatic potential profile $V(x)$ on the surface of the polymer film. We have shown that in contrast to inorganic semiconductors, where the technique is mainly *surface sensitive* due to the presence of a high density of surface dangling bond, in polymer semiconductors it allows one to probe directly the electrostatic potential in the TFT channel at the *buried interface* between the semiconducting polymer and the dielectric [50].

It can clearly be seen (Fig. 9.3) that for small source–drain voltage ($V_{sd} \ll V_g$), the electrostatic potential varies approximately linearly with the distance from the source electrode, as expected in the linear operating regime of the TFT. In the saturation regime, the profiles exhibit a characteristic increase in the electric field in the vicinity of the drain electrode. Since the current along the channel is constant, this lateral variation of electric field is required to compensate for the reduced charge carrier concentration near the drain terminal. These potential maps confirm the clean TFT operation mode of the devices. From the SKPM potential maps it can also be seen that there is a significant potential drop at the source and drain contacts, from which direct information about the parasitic contact resistance can be obtained (see later discussion). From the potential maps, we can extract accurate values of the local field-effect mobility. The current density per unit width in the TFT is given by

$$\begin{aligned} J &= \mu^{\text{TFT}}(V_g, E) \cdot n_{\text{ind}}(V_g, \bar{x}) \cdot E(\bar{x}) \\ &= \mu^{\text{TFT}}(V_g, E) \cdot C_i \cdot [V_g - V(x) - V_{fb}] \cdot E(\bar{x}) \end{aligned} \quad (9.4)$$

where J is measured during the AFM experiments and $V(x)$ and $E(x) = dV(x)/dx$ are extracted from the potential profiles (V_{fb} is the flatband voltage). Therefore, the local mobility can be measured directly as a function of carrier concentration, electric field, and temperature without the complications due to contact resistance and short-channel effect that need to be taken into account when extracting the mobility from the device characteristics.

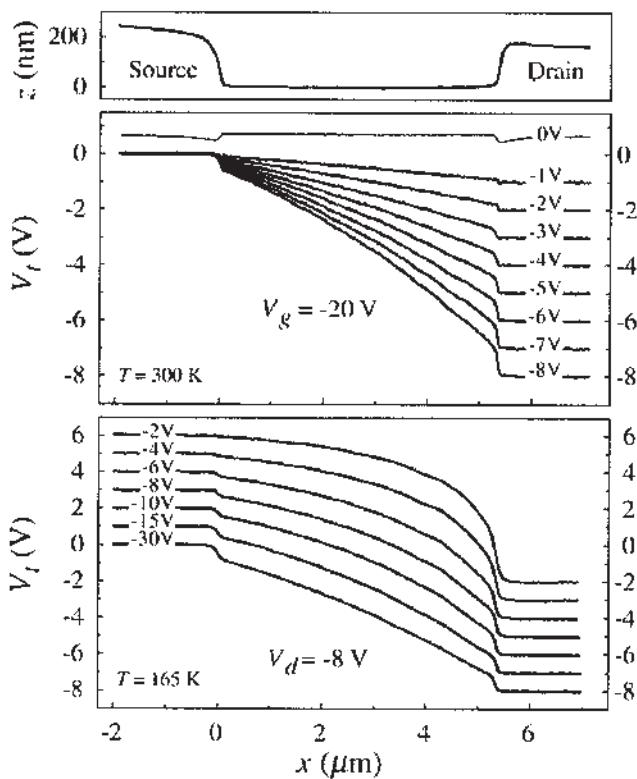


Figure 9.3 Electrostatic potential profiles $V_t(x)$ along the channel of a bottom-gate P3HT TFT fabricated on a SiO_2/Si substrate with Au/Cr source-drain electrodes as measured by scanning Kelvin probe microscopy (SKPM). (*top*) Noncontact AFM surface topography, (*middle*) Potential profiles at 300 K for different drain voltages as a function of the distance x from the source electrode (gate voltage $V_g = -20 \text{ V}$), (*bottom*) Potential profiles taken at 165 K for different gate voltages (drain voltage $V_d = -8 \text{ V}$).

Figure 9.4 shows the dependence of the field-effect mobility on the carrier concentration. The values extracted by the two methods are in good agreement with each other. The mobility of P3HT FETs increases approximately linearly with increasing gate voltage, that is, with the position of the Fermi level at the interface, $\mu \propto (V_g - V_0)^\gamma$, $\gamma = 1.0 \pm 0.2$. The gate-voltage dependence is interpreted as reflecting an energy-dependent density of states caused by residual disorder in the locally self-organized polymer film. As the carrier concentration

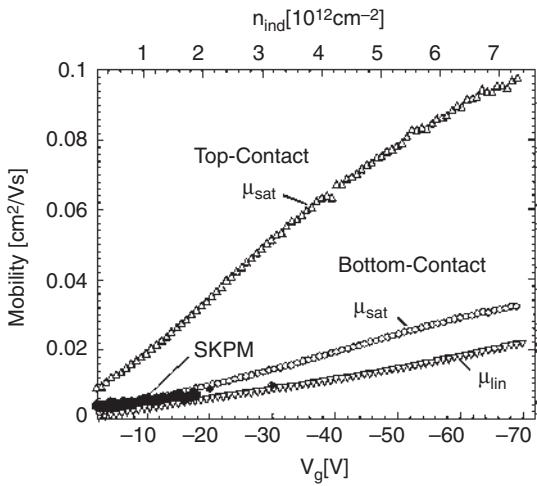


Figure 9.4 Dependence of the field-effect mobility of P3HT/SiO₂ TFTs on gate voltage, i.e., charge carrier concentration. Data extracted from the device characteristics of top and bottom source-drain contact TFTs as well as from SKPM on bottom source-drain devices are shown. For the SKPM measurements, the lateral electric field along the channel was similar to that for the device measurements in the linear regime.

increases, localized defect states are filled and the Fermi level approaches a region of the density of states of more extended electronic states with higher mobilities.

The linear field-effect mobility extracted from the device characteristics is lower by a factor of $\sim 2/(\gamma + 2)$ than the saturated mobility, where $\gamma \approx 1$ is the exponent of $\mu \propto (V_g - V_0)^\gamma$. This may be due to an inadequacy of the simple model in the case of a gate-voltage-dependent mobility. In a-Si TFT, modeling a so-called saturation parameter is introduced to account for a similar difference [51]. The highest mobilities of 0.05–0.1 cm²/V-s are observed in top-contact FETs. The mobility difference between bottom- and top-contact FETs of typically a factor of 2–3 is attributed to disruption of the self-organization process during spin-coating by the presence of the source–drain electrodes in the bottom-contact configuration [27]. Note that our Kelvin probe microscopy experiments were performed on bottom-contact devices.

Figure 9.5 shows the dependence of mobility on the lateral electric field along the channel as extracted from the two methods. The lateral field dependence has been extracted from the device characteristics by comparing devices with different channel lengths ($L = 2\text{--}20\ \mu\text{m}$). This is possible only in the linear

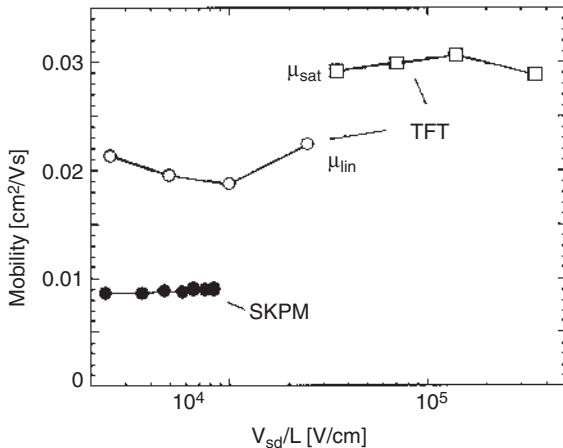


Figure 9.5 Dependence of the field-effect mobility of bottom-gate P3HT/SiO₂ TFTs on V_{sd}/L , which is a measure of the lateral electric field along the channel. Data extracted from the linear and saturation device characteristics of bottom source-drain contact TFTs with $L = 2\text{--}20 \mu\text{m}$ ($V_g = -60 \text{ V}$) as well as from SKPM on bottom source-drain devices ($V_g = -30 \text{ V}$) are shown.

regime, since in the saturation regime the electric field increases towards the drain (Fig. 9.3). Nevertheless, to illustrate the weak dependence of the mobility on channel length, we have included saturation mobilities extracted from devices with channel lengths L varying from 2 to 20 μm . We emphasize that V_{sd}/L can be regarded only as a very approximate measure of the electric field for these data points. This weak electric field dependence is confirmed by the more direct Kelvin probe microscopy measurements. Within the lateral field range of $10^3\text{--}10^4 \text{ V/cm}$, the mobility varies by less than 10%. This shows that in self-organized, high-mobility P3HT, the field dependence of the mobility is much weaker than in amorphous, low-mobility polymers, which is believed to be a manifestation of the more extended nature of the electronic wavefunctions of polaronic charge carriers in the microcrystalline domains of P3HT with strong $\pi\text{--}\pi$ interchain interactions (see discussion in Sec. 9.4).

Another important parameter governing the performance of polymer TFTs is the parasitic contact resistance at the injecting source-drain contacts. The contact resistance has been extracted by plotting the slope in the linear regime of the output characteristics for a given gate voltage as a function of channel length. The y-axis intercept of such plots yields the contact resistance as a function of gate voltage [52]. Alternatively, and more directly, we have determined the

gate-voltage dependence of the contact resistance in the same device configuration by directly extracting the potential drop across the source (or drain) contacts from the Kelvin probe potential profiles (Fig. 9.6). Values obtained from the two methods are in good agreement with each other. The small differences are most likely due to the fact that the two experiments were not performed on the same set of devices. The contact resistance in this bottom-gate configuration with Au/Cr source-drain electrodes patterned prior to deposition of the semiconductor decreases with increasing gate voltage. It was found that the source–drain contact resistance can be reduced significantly by depositing the gold source–drain electrodes directly onto the SiO_2 dielectric without the thin interfacial adhesion layer of Cr. Note that the Cr layer, which is in direct contact with the accumulation layer, has a lower work function than gold, and its surface is also likely to be oxidized on the side walls. The gate-voltage dependence of the contact resistance is believed to be due to a reduction of the potential barrier at the injecting contact with the applied gate field.

In this section we have shown that the device characteristics of polymer TFTs have many features in common with those of amorphous Si devices. Reliable values for the field and carrier-concentration dependence of the field-effect mobility have been determined. These are crucial input parameters for the simula-

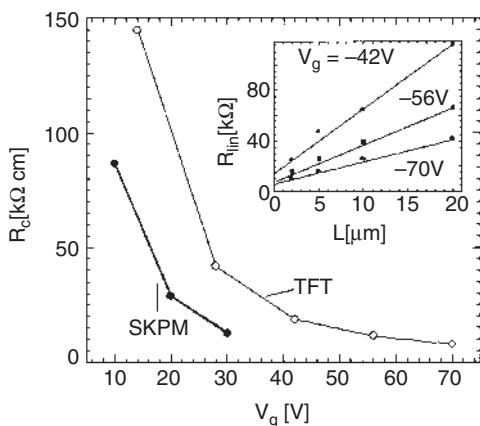


Figure 9.6 Dependence of the parasitic source–drain contact resistance of bottom-gate P3HT/SiO₂ TFTs with Au/Cr source–drain contacts on gate voltage. The resistance per contact is normalized to a channel width of $W = 1$ cm. Data extracted from the channel length scaling of the slope of the output characteristics in the linear regime (inset) as well as direct measurements by SKPM are shown.

tion of polymer TFTs with simple device models. Such device models are the basis for reliable simulation and design of more complex logic circuits based on polymer TFTs.

9.4 MOBILITY ENHANCEMENT THROUGH POLYMER SELF-ORGANIZATION

Over recent years, several factors have contributed to the rapid progress of polymer TFT performance and charge carrier mobility:

Polymer materials have become available with improved structural regularity and chemical purity.

Polymer self-organization mechanisms have been employed to control the self-assembly of ordered polymer structures from solution.

Methods for using aligning templates to promote the organization of the polymer and induce alignment/preferential orientation of polymer chains on a substrate have been developed.

In the case of polyalkylthiophenes, rapid progress was made when synthetic routes to regioregular, head-to-tail coupled polymers were developed by McCullough [53] and Rieke [54]. The two routes are based on the regioselective coupling of asymmetric dihalogen-substituted alkylthiophene monomers. Recently, a synthetically simpler but also highly regioselective route has been developed based on symmetrically substituted monomers [55]. Using these routes, poly-3-alkylthiophene polymers with head-to-tail regioregularity exceeding 98% have been synthesized.

Regioregular P3HT is a microcrystalline polymer forming highly ordered lamellar domains with two-dimensional conjugated sheets of conjugated backbones with cofacial $\pi-\pi$ interchain stacking separated by layers of alkyl side chains [56–58]. From the width of X-ray diffraction peaks, the typical crystallite size has been estimated to be on the order of 100–200 Å. These microcrystalline domains are separated by regions with more disordered microstructure. Under suitable processing conditions, a preferential orientation of the domains can be induced such that the two-dimensional (2D) conjugated lamellae are oriented in the plane of the film. This orientation is favorable for in-plane charge transport in a TFT device.

The field-effect mobility depends very sensitively on the degree of head-to-tail regioregularity of the polymer backbone (Fig. 9.7) [28]. Head-to-head coupling of alkyl chains on neighboring thiophene units gives rise to steric hindrance, inducing torsion of the polymer backbone and disrupting conjugation. The highest mobilities of 0.05–0.1 cm²/V·s were obtained for the polymer, with the highest head-to-tail regioregularity exceeding 98%. With decreasing regioregularity, the mobility drops by orders of magnitude. All but one polymer in Figure

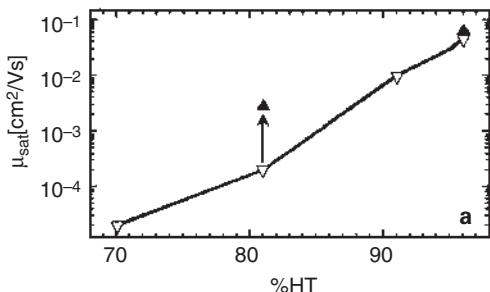


Figure 9.7 Dependence of the field-effect mobility of bottom-gate P3HT/SiO₂ TFTs on the degree of head-to-tail regioregularity. Devices were fabricated by spin-coating of the P3HT film (open symbols) and by slow casting (filled symbols). The different polymers were synthesized by the McCullough method, except for the polymer with the highest regioregularity, which was synthesized by the Rieke method. (From Ref. 28, with copyright permission from *Nature*.)

9.7 were synthesized by the McCullough route; the polymer with the highest mobility and regioregularity, as measured by nuclear magnetic resonance (NMR), was synthesized by the Rieke route. It is important to note that all polymers that are included in Figure 9.7 exhibit microcrystalline order, as evidenced by crystalline diffraction peaks in X-ray diffraction (XRD). Only if the regioregularity is less than 70% does P3HT become amorphous and is crystallization suppressed [59]. In XRD, the size of microcrystalline domains in the high- and low-regioregularity samples investigated in this study was in fact found to be comparable [28].

The sensitive dependence of mobility on regioregularity is attributed to a combination of two effects. Firstly, the regioregularity was found to affect directly the structural anisotropy of the microcrystalline film. In the high-regioregularity samples, the microcrystalline domains adopt a preferential orientation in which the conjugated planes are oriented favorably in the plane of the film, in which transport occurs. The orientation was inferred from wide-angle X-ray scattering (WAXS) images (Fig. 9.8a), in which the characteristic π–π stacking diffraction (010) is observed in the plane of this spin-coated film, whereas the different-order diffraction peaks associated with the stacking of lamellae (*n*00) are observed normal to the film. In films prepared under identical conditions from the lower-regioregularity polymers, a different orientation was observed (Fig. 8b) in which the microcrystalline lamellar domains are oriented normal to the plane of the substrate. This out-of-plane orientation of the lamellae is less

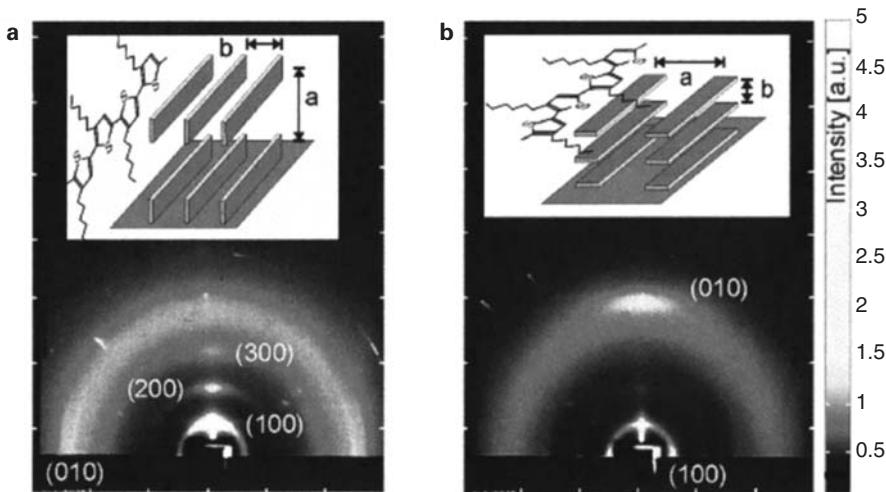


Figure 9.8 Representation of the two-dimensional distribution of scattered CuK_α wide-angle X-ray intensity from spin-coated, 70 to 100-nm-thick P3HT films with regioregularity of 96% (a) and 81% (b) on SiO_2/Si substrates. The vertical (horizontal) axis corresponds to scattering normal (parallel) to the plane of the film. The insets show schematically the different orientations of the microcrystalline grains with respect to the substrate. (From Ref. 28, with copyright permission from *Nature*).

favorable for in-plane TFT charge transport than the in-plane orientation of the lamellae.

More direct experimental proof for a correlation between the field-effect mobility and the preferred orientation of microcrystalline domains was obtained from experiments in which the domain orientation in films fabricated from the same polymer with a particular regioregularity was changed by the film deposition conditions. When films of the 81% regioregular polymer were deposited by slow-casting from solution, they were found to adopt the in-plane orientation of lamellae, with a corresponding increase in mobility by one order of magnitude compared to spin-coated films of the same polymer, which adopt the out-of-plane orientation [28]. As pointed out earlier, from a percolation point of view one might expect that even in self-organized polymers, the electronic transport properties in devices with micrometer dimensions would still be dominated by the most disordered regions of the film masking the beneficial effects of the self-organization. The important conclusion drawn from these experiments on P3HT is that the

self-organization is sufficiently pronounced that at least at room temperature, a direct correlation between mobility and polymer self-organization can be observed. P3HT is in fact one of the first semiconducting conjugated polymers for which such correlation could be established.

The second mechanism contributing to the sensitive dependence of mobility on regioregularity shown in [Figure 9.7](#) is more subtle and is related to the microscopic nature of the charge carriers. One of the main differences between inorganic semiconductors and conjugated polymers is that in the latter, strong electron–phonon coupling is known to result in polaronic relaxation when a charge carrier is injected onto a polymer chain. In the vicinity of the charge, the lattice is deformed and the configuration of the other electrons is perturbed. These polarization effects result in localization of the carrier. Experimental evidence for polaron formation in many conjugated polymers stems from optical spectroscopy experiments [60]. In a one-electron diagram, relaxation effects can be represented by a shift of the electronic levels of the charged molecule with respect to the neutral molecule. This shift can be detected in optical spectroscopy experiments as characteristic charge-induced absorptions that appear upon charge injection and are accompanied with corresponding bleaching features of the neutral polymer absorption. In order to characterize such relaxation effects of charge carriers in the accumulation layer of a TFT, we have applied charge modulation spectroscopy (CMS) [61,62]. This is an optical absorption experiment in which changes of the transmission of a semitransparent TFT or MIS device are detected when the charge carrier concentration in the TFT channel is modulated via modulation of the gate bias.

We have compared charge-induced absorption spectra of high-mobility, highly microcrystalline P3HT TFTs with those of low-mobility, amorphous P3HT TFTs in order to investigate on a more microscopic scale the origin of the correlation between mobility and microcrystallinity ([Fig. 9.9](#)). Amorphous films were obtained from P3HT polymers with a degree of regioregularity less than 70%. The spectra of the amorphous polymer exhibit two charge-induced transitions at 1.4 eV and 0.3–0.5 eV [63]. These solid-state transitions, which are often denoted C2 and C1, respectively, are very similar to those of radical cations on isolated short conjugated molecules [64] and polymers [65] in dilute solution. This similarity indicates that interchain effects are not felt by the charge carriers in such amorphous polymers. The spectra can be explained by considering the polymer as a disordered network of short isolated conjugated segments separated by conjugation defects [66]. Carriers are confined to individual segments, and interchain interaction effects are suppressed by disorder [67].

In contrast, the spectrum of the microcrystalline polymer ([Fig. 9.9](#)) exhibits several spectral features that cannot be explained in an isolated chain model: (1) A new charge-induced transition appears at 1.75 eV, close to the $\pi-\pi^*$ bandgap transition. A weak shoulder is observed at energies of 1.35 eV, close to the C2

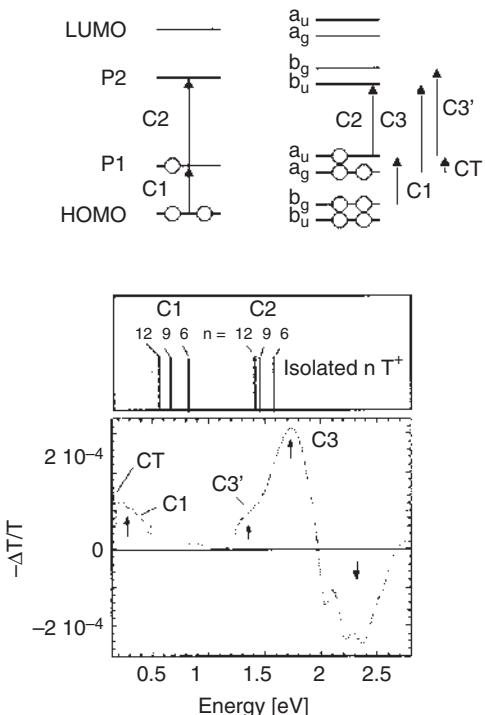


Figure 9.9 Optical charge modulation spectroscopy (CMS) of field-induced charges in the accumulation regime of high-mobility, high-regioregularity (HT = 96%) poly-3-hexylthiophene (P3HT) FETs from the mid-infrared to visible spectral range. (From Ref. 28, with copyright permission from *Nature*) (top) Schematic diagram of charge-induced transitions in a dimer formed by two conjugated oligomers, illustrating the effects of interchain interactions on the optical spectra.

transition energy of the amorphous polymer. (2) The C1 transition is red-shifted to energies around 0.25 eV, indicating a reduction of polaronic relaxation energy. (3) New low-energy transitions appear at energies below 0.15eV. The last are superimposed onto a set of sharp Fano-type (anti)resonances due to the overlap of the electronic transition with different types of vibrational modes [28,68]. These spectral features are interpreted as manifestations of interchain interaction effects in the 2D microcrystalline lamellae of P3HT. Recently, quantum mechanical calculations performed on a dimer of a conjugated oligomer have shown that for realistic strength of the $\pi-\pi$ interchain interaction, the wavefunction of the

carrier is completely delocalized over the dimer molecule; i.e., it is no longer confined to an individual chain. According to the calculations, this delocalization of the polaronic carriers is able to explain all three characteristic features observed in the optical spectra of high-mobility, microcrystalline P3HT TFTs [63]. The low-energy infrared transitions below 0.15 eV can be explained by “intraband” charge transfer transitions between electronic levels that are split by the intermolecular interaction (see schematic in Fig. 9.9). We believe that at higher charge carrier concentrations, these intraband transitions would develop into a Drude-type absorption observed in good metals.

From the point of view of the present discussion, the main conclusion from the optical experiments is that they indicate that the wavefunction of polaronic carriers in the 2D conjugated lamellae of microcrystalline P3HT is no longer confined to individual chains. Rather, as a consequence of strong $\pi-\pi$ interchain interactions, the wavefunction extends over several neighboring chains. It is possible that the extent of the wavefunction is limited only by the size of the microcrystalline domains, which is on the order of 100 Å. As a result of the more extended wavefunction, the polaronic relaxation energy is reduced and interchain transport is facilitated, which we believe is the microscopic reason for the dramatic improvement in charge carrier mobility reported in Fig. 9.7.

We now turn to a discussion of another self-organization mechanism by which the microstructure of solution-deposited polymers can be controlled. In P3HT we observed a pronounced preferred orientation of lamella domains normal to the plane of the substrate, but in the absence of any in-plane substrate anisotropy there is no preferred uniaxial orientation of the polymer chains in the plane of the film. P3HT can be aligned uniaxially by techniques such as stretch alignment [23] and Langmuir–Blodgett deposition [21], but these techniques have yielded only moderate device performance. The motivation for achieving uniaxial chain orientation parallel to the direction of transport in the TFTs is to make optimum use of the fast-charge intrachain transport along the polymer chain. Nematic or smectic liquid crystalline phases in rigid-rod polymers provide an elegant method of achieving such uniaxial orientation.

Rigid-rod polymers such as di-alkyl-fluorene based homo- and copolymers exhibit nematic, liquid crystalline (LC) phases at elevated temperatures [69]. By depositing the polymer onto an alignment substrate, monodomain samples can be fabricated in which polymer chains are aligned parallel to the director over macroscopic distances. This phenomenon has been used to demonstrate linearly polarized polymer light-emitting diodes (LEDs) [70]. In time-of-flight experiments, high charge carrier mobilities have been observed in conjugated polymer glasses obtained by quenching from nematic LC phases [71] and in the crystalline and LC phases of discotic [72] and smectic [73] small conjugated molecules. F8T2 is an example of a nematic, ordered copolymer that has been developed by the Dow Chemical Company. F8T2 possesses a thermotropic, nematic LC

phase above 265°C and can be oriented into a monodomain on an rubbed polyimide alignment layer [74].

We have developed a top-gate configuration that allows incorporation of such aligned polymer films into a TFT device [30]. The devices are fabricated on substrates coated with rubbed or photoaligned polyimide or other alignment layers. Inorganic metal source-drain electrodes such as gold are defined by shadow-mask evaporation (channel length $L = 20\text{--}200\ \mu\text{m}$) or photolithographic patterning ($L = 2\text{--}20\ \mu\text{m}$). A thin semiconducting polymer film is then deposited by spin-coating and is aligned by annealing in the LC phase at 275–285°C for several minutes under inert N₂ atmosphere. A nematic glass is prepared by quenching the sample to room temperature. During this quenching step the alignment of the polymer chains parallel to the alignment direction of the polyimide is preserved but crystallization is suppressed. Afterwards the device is completed by spin-coating a layer of polymer dielectric, such as poly-vinylphenol (PVP), as the gate insulating layer and shadow-mask depositing a gold gate electrode. Deposition of PVP from alcohol solvents such as isopropanol was found to overcome the critical problems of dissolution and swelling of the underlying F8T2 layer and to allow the formation of an abrupt active interface between two solution-deposited semiconducting and insulating layers. The process can be adapted easily to the fabrication of all-polymer devices, with conducting polymer source-drain and gate electrodes patterned by direct inkjet printing, which will be discussed in the next section.

The degree of polymer alignment can be quantified by polarized optical absorption spectra. In the spectral region of the F8T2 $\pi\text{--}\pi^*$ transition, the dichroic ratio $R = A_{\parallel}/A_{\perp}$ of the absorption coefficients for incident light polarized parallel (perpendicular) to the rubbing direction is 5–12, depending on film thickness and details of the annealing and rubbing procedure (Fig. 9.10). R is related to the distribution of azimuthal angles θ and polar angles ϕ of misalignment of polymer chains with respect to the director;

$$R \leq \frac{\langle \cos^2 \theta \rangle_{\theta}}{\langle \sin^2 \theta \rangle_{\theta} \langle \cos^2 \phi \rangle_{\phi}} \quad (9.5)$$

The inequality in Eq. (9.5) takes into account that the transition dipole moment may have a nonzero component perpendicular to the polymer backbone, such that R remains finite even for perfect alignment. An off-axis component is expected in F8T2 as the rings of the fluorene unit are bent away from the in-line catenation by an angle $\alpha \approx 22.8^\circ$. For thick (200-nm) films of F8T2, we can consider the film to be three-dimensional ($\langle \cos^2 \phi \rangle_{\phi} = 0.5$), and we obtain a lower-limit estimate for the structural order parameter

$$P_2 = \frac{1}{2} \cdot (3\langle \cos^2 \theta \rangle_{\theta} - 1) > 0.65\text{--}0.8$$

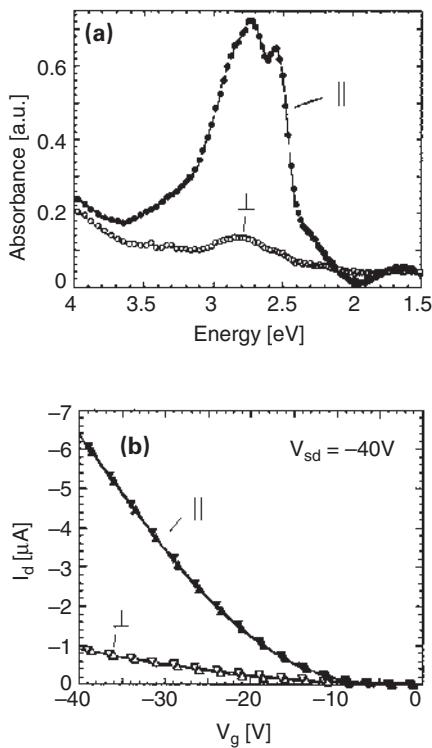


Figure 9.10 (a) Optical absorption spectra of a completed TFT device taken in the PEDOT-free substrate regions with incident light linearly polarized parallel (||) and perpendicular (⊥) to the direction of alignment of the F8T2 polymer. (b) Saturated transfer characteristics of inkjet-printed F8T2 TFTs fabricated on the same substrate on which the absorption spectra in (a) were taken. The channels were oriented such that current transport is parallel (||) and perpendicular (⊥) to the chain alignment direction ($L = 5 \mu\text{m}$).

Best use of the fast intrachain transport along the polymer backbone is made if the current flow in the TFT is along the direction of polymer alignment. In this direction, high mobilities of $\mu_{||} = 0.01\text{--}0.02 \text{ cm}^2/\text{V}\cdot\text{s}$ are obtained (Fig. 9.10). Significantly lower values of $\mu_{\perp} = 0.001\text{--}0.002 \text{ cm}^2/\text{V}\cdot\text{s}$ are measured for devices fabricated on the same substrate with current flow perpendicular to the alignment direction (⊥). Typical values for the anisotropy of the field-effect mobility are 5–8, varying between devices on the same substrate. The corresponding dichroic ratio measured on the same substrate tends to the slightly higher, R

$\approx 8\text{--}10$, but it is always of the same order of magnitude as the mobility anisotropy. Similar observations have recently been reported by Grozema et al. [75]. We have also fabricated devices in an isotropic multidomain configuration by subjecting the polymer to the same thermal treatment on a bare glass substrate without alignment layer. In the multidomain isotropic devices, the domain sizes are on the order of $0.1\text{--}1 \mu\text{m}$, as estimated from optical micrographs; that is, the TFT channel contains several LC domain boundaries. These isotropic devices (X) exhibit mobilities $\mu_x = 0.003\text{--}0.005 \text{ cm}^2/\text{V}\cdot\text{s}$; i.e., $\mu_\perp < \mu_x < \mu_\parallel$.

The mobility measured for the parallel-device orientation is of course not a direct measure of the intrachain mobility, since the typical persistence length L_p of polymer chains, that is, the characteristic length of a straight chain segment, is much smaller than the TFT channel length. For structurally similar F8, a value of $L_p \approx 8.5 \text{ nm}$ [69] has been determined. Even in devices in which the polymer chains are aligned parallel to the transport direction, the rate-limiting step is the interchain-hopping process between adjacent chains. The mobility enhancement in devices in which the current flow is along the direction of polymer alignment is due mainly to the reduced number of interchain-hopping events that carriers encounter between source and drain electrodes. A simple model has been suggested relating the mobility anisotropy μ_\parallel/μ_\perp to the optical dichroic ratio A_\parallel/A_\perp [30]:

$$\frac{\mu_\parallel}{\mu_\perp} = \frac{v_\parallel}{v_\perp} \cdot \frac{\langle X_{\parallel\perp}^2 \rangle}{\langle X_\perp^2 \rangle} = \frac{v_\parallel}{v_\perp} \cdot \frac{L_p^2 \cdot \langle \cos^2 \theta \rangle_\theta}{L_p^2 \cdot \langle \sin^2 \theta \rangle_\theta \cdot \langle \cos^2 \phi \rangle_\phi} = \frac{v_\parallel}{v_\perp} \cdot \frac{A_\parallel}{A_\perp} \quad (9.6)$$

where $\langle X_{\parallel\perp}^2 \rangle$ are the average square distances traveled parallel and perpendicular to the direction of alignment, respectively, per rate-limiting hopping step. The model explains the experimental observation that the mobility anisotropy is of the same order of magnitude as the optical dichroic ratio. This observation is remarkable, because the dichroic ratio reflects a spatial average of the degree of local alignment of the polymer on a length scale of the excitonic wavefunction, whereas the mobility in a disordered system is limited by the most difficult hopping processes that carriers encounter on their way from source to drain electrodes.

The model may be used to derive a very crude estimate of how much faster intrachain transport along the straight chain segments must be than the hopping process from one chain to the other. Obviously, if the time τ_h for an interchain-hopping process across a typical interchain-hopping distance of $a \approx 4 \text{ \AA}$ was comparable to the time τ_s , to travel the same distance across a straight chain segment of length L_p , the attempt frequency

$$v_\parallel \approx \left[\tau_s \left(\frac{L_p}{a} \right) + \tau_h \right]^{-1}$$

would be significantly smaller than $v_\perp \approx \tau_h^{-1}$; i.e., the mobility anisotropy would

be significantly less than the dichroic ratio. Experimentally, for the data shown in Figure 9.10, the mobility anisotropy is smaller by only 20% than the dichroic ratio, implying that ν_{\parallel} is only slightly smaller than ν_{\perp} ($\nu_{\parallel} \sim (4/5)\nu_{\perp}$) and that the microscopic intrachain mobility $\mu \propto \tau_s^{-1} \cdot a^2$ must be more than one to two orders of magnitude higher than the interchain mobility, depending on the value of L_p . This is, of course, only a very crude estimate. It neglects the presence of disordered regions in the film as well as the possibility of an off-axis component of the transition dipole moment. Similar estimates of lower limits for the intrachain mobility have been obtained from time-resolved microwave conductivity experiments [76]. For a more reliable determination of the intrachain mobility it will be necessary to perform measurements on devices with channel lengths that are comparable to the persistence length of polymer chains.

Our approach of using liquid crystalline phases to uniaxially align thin polymer films deposited from solution opens new possibilities for making better use of the fast intrachain transport along the polymer chain. This is yet another example of how charge carrier mobilities in solution-processed conjugated polymers can be enhanced significantly by controlling the microstructure of the polymer films through self-organization mechanisms.

9.5 DIRECT INKJET PRINTING OF POLYMER TRANSISTOR CIRCUITS

It is apparent from the preceding discussion that in spite of the significant performance improvements over recent years, polymer TFTs do not offer performance advantages over conventional inorganic TFT technologies at present. Interest in polymer TFTs as a potential commercial TFT technology stems primarily from the compatibility of polymers with innovative processing and manufacturing techniques based on solution processing and direct printing [35–41]. In order to illustrate some of the key features and challenges associated with the printing of active electronic circuits, we describe here in some detail our own approach, which is based on direct inkjet printing [42]. Inkjet printing has emerged as an attractive patterning technique for conjugated polymers in light-emitting diodes (LEDs) [77,78] and appears to be the technique that is going to enable full-color, high-resolution polymer LED displays [79].

One of the biggest challenges for direct printing of TFTs is to develop a manufacturable printing technique capable of achieving the micrometer-scale resolution and alignment accuracy that is required to define practical devices in a controlled and repeatable way. The most critical step of TFT fabrication is the definition of the source–drain electrodes that require channel lengths L with electrode separation less than 5 μm , in order to achieve adequate drive currents and switching speeds. Inkjet printing is normally not considered capable of achieving such high resolution. The resolution of inkjet printing is limited to

20–50 μm by statistical variations of the flight direction of droplets and their spreading on the substrate.

Our approach for overcoming these resolution limitations is to confine the spreading of water-based conducting polymer ink droplets on a hydrophilic substrate with a pattern of narrow hydrophobic surface regions that define the critical device dimensions (Fig 9.11). When water-based inkjet droplets of the conducting

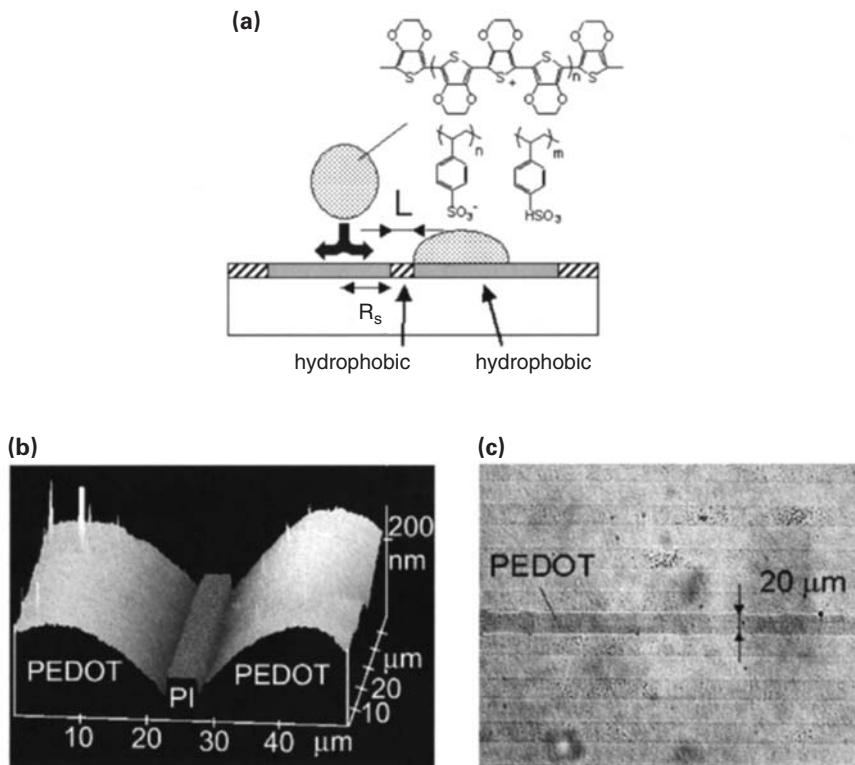


Figure 9.11 (a) Schematic diagram of high-resolution inkjet printing onto a prepatterned substrate. (b) Tapping-mode atomic force micrograph showing accurate pinning of inkjet-printed PEDOT/PSS source and drain electrodes at the boundary of a hydrophobic polyimide barrier with $L = 5 \mu\text{m}$. No deposition of PEDOT occurs on top of the barrier. (From Ref. 42, with copyright permission from *Science*.) (c) Optical micrograph of an inkjet-printed PEDOT line confined to a 20- μm -wide line by a self-assembled monolayer printed by soft lithography. (From M. Banach, C. Newsome, et al., to be published.)

polymer poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonic acid (PEDOT/PSS) are deposited into the hydrophilic surface regions at a distance R_s from the hydrophobic barrier, the droplets spread until they hit the repelling barrier. In this way it is possible to print two parallel source-drain electrode lines, with a separation of less than 10 μm , that are accurately aligned with the hydrophobic barrier [80]. No PEDOT deposition occurs on top of the barrier regions, even if the width of the barrier is much smaller than the droplet diameter. The unconfined boundaries of the printed lines are much more irregular, with a typical statistical roughness on the order of 10 μm . This roughness would have led to electrical shorts between source and drain electrodes had we attempted to define such a short channel ($L = 5 \mu\text{m}$) without a confinement structure. At present the resolution of the ink-confinement process is limited only by our photolithography setup. The shortest channel lengths that we have achieved in this way are devices with $L = 0.25 \mu\text{m}$. Note that the boundaries of printed PEDOT lines are accurately pinned at the edges of the hydrophobic barrier, suggesting that even higher-resolution printing might be possible.

The high-resolution surface free-energy pattern is prefabricated on the substrate prior to any of the TFT deposition and printing steps. A broad range of techniques may readily be used, since at this stage the substrate does not yet contain any of the radiation or chemically sensitive active layers of the devices. In our first demonstration the barrier was fabricated from a thin layer of hydrophobic polyimide polymer patterned by photolithography and etched in an O_2 plasma to expose regions of the bare, hydrophilic glass substrate. The polyimide film is on the order of only 500 Å thick. Since the spreading droplets in the liquid state have a much larger thickness of a few micrometers, the ink confinement must be caused mainly by the surface free-energy contrast, and does not require the hydrophobic barrier to have a pronounced topographic profile. We have also fabricated surface energy patterns by direct printing techniques. Ink confinement can also be achieved with a self-assembled monolayer (SAM) of hydrophobic alkyltrichlorosilanes. [Figure 9.11c](#) shows a printed PEDOT line that was confined accurately to a 20- μm -wide line from a droplet with a diameter of 50 μm with the help of a self-assembled hydrophobic monolayer. The patterned monolayer was printed onto the substrate by the soft lithography technique, in which a soft rubber stamp of PDMS with a surface relief structure is inked with the SAM and then brought into contact with the substrate to selectively transfer the SAM.

It is interesting to consider which physical processes may be the resolution-limiting factors for this surface-energy-assisted, high-resolution inkjet printing process, which is, of course, also applicable to other solution-based printing processes as well as simple dip-coating deposition. The maximum achievable resolution is expected to depend on whether the incoming droplets are repelled immediately when they impinge onto the hydrophobic surface energy barrier or whether the kinetic energy of the incoming droplets causes them to “spill over” by some

small distance into the hydrophobic barrier region before being attracted back into the hydrophilic surface region. In the former case it is possible that much higher, submicron resolution might be achievable. We have developed a hydrodynamic model comparing the surface energy force that is responsible for the repulsion of the incoming droplets with the inertial force due to the kinetic energy of the spreading droplet [80]. The simple model suggests that for a broad range of printing distances, the repelling surface energy force is at least two orders of magnitude larger than the inertial force. This explains why we have observed the droplet-confinement process to be robust with respect to variations of the droplet volume or the distance R_s , which are caused by external perturbations of the droplet flight direction or changing ejection conditions at the nozzle. Device yields in our experiments, which were performed in normal laboratory atmosphere, appear to be limited only by dust contamination. No evidence for accidental shorts between source and drain electrodes was found. The simple model also suggests that it may be possible to achieve significantly higher resolution via this method of ink confinement. Experiments to investigate resolution limits are under way.

After inkjet printing of source–drain electrodes, TFT devices are fabricated in the top-gate configuration described earlier by spin-coating a continuous film of the active semiconducting polymer. Next, the dielectric polymer, such as polyvinylphenol (PVP), is spin-coated on top from a solvent that does not dissolve/swell the underlying semiconducting polymer. Finally, a PEDOT/PSS gate electrode line overlapping the channel is inkjet printed in air (Fig. 9.12). In this device configuration the ink-confinement barrier can be used to achieve a dual purpose. It not only provides the high-resolution definition of the channel, but it also acts as the aligning template for the deposition of the self-organizing semiconducting layer, which is crucial for achieving high field-effect mobilities. By using a mechanically rubbed polyimide ink-confinement barrier in combination with a liquid crystalline semiconducting polymer such as F8T2, we have fabricated devices with uniaxial alignment of polymer chains in the channel of the TFT. The process sequence is essentially the same as described earlier. The alignment is evident in optical microscopy images observed under crossed polarizers (inset of Fig. 9.12b). The TFT channel regions appears bright, reflecting the monodomain alignment of F8T2 on top of polyimide, whereas in the source–drain electrode regions, where the F8T2 is in a multidomain configuration on top of PEDOT, the light is extinguished.

Figure 9.13 shows the output and transfer characteristics of an inkjet-printed, all-polymer F8T2 TFT. The device exhibits a high ON–OFF current ratio on the order of 10^5 , as measured between 0 and -20 V, and good threshold voltage stability. The hysteresis between characteristics measured with increasing and decreasing source–drain and gate voltage, respectively, is negligible. F8T2 has good stability against chemical doping by environmental oxygen or residual

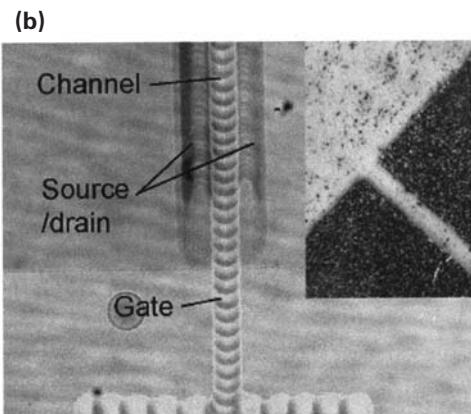
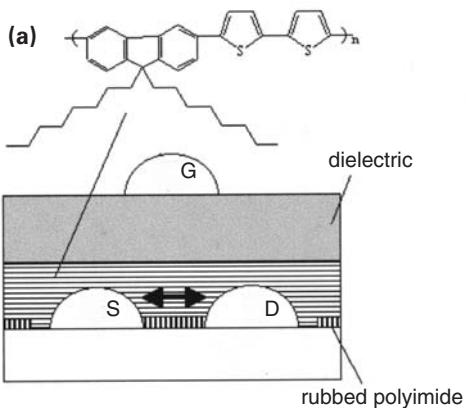


Figure 9.12 (a) Schematic diagram of top-gate inkjet-printed TFT with an F8T2 semiconducting layer (S = source, D = drain, G = gate). (b) Optical micrograph of an inkjet-printed TFT. The inset shows an enlargement of the channel region seen under crossed polarizers such that the TFT channel ($L = 5 \mu\text{m}$) appears bright due to the uniaxial, monodomain alignment of the F8T2 polymer on top of rubbed polyimide.

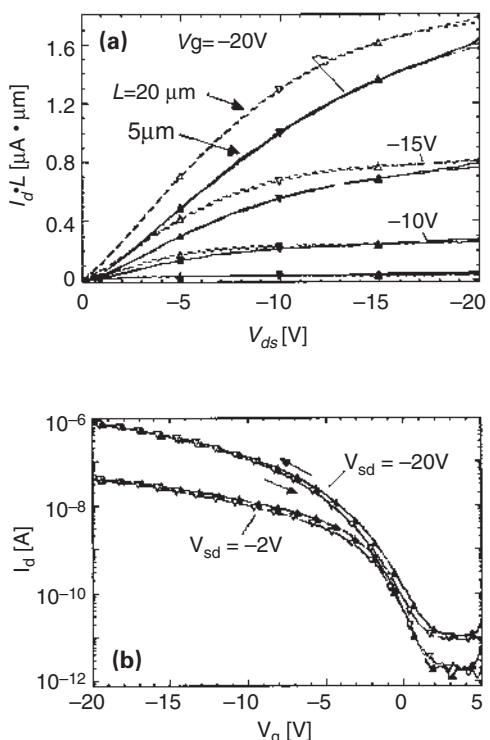


Figure 9.13 (a) Output characteristics of printed F8T2 all-polymer TFTs with $L = 5 \mu\text{m}$ and $L = 20 \mu\text{m}$. The current is normalized with the channel length. (b) Transfer characteristics of a printed F8T2 all-polymer TFT ($L = 5 \mu\text{m}$). Subsequent measurements under N_2 atmosphere with increasing (filled triangles) and decreasing (open triangles) source-drain and gate voltage, respectively, are shown.

impurities such as mobile sulphonic acid in the PEDOT/PSS ink. The highest mobilities of $0.01\text{--}0.02 \text{ cm}^2/\text{V}\cdot\text{s}$ were achieved in devices in which current transport is along the direction of polymer chain alignment. In general the performance of inkjet-printed, all-polymer F8T2 TFTs is by no means inferior to that of control devices fabricated in a conventional way with photolithographically defined gold electrodes. This shows that through careful choice of the sequence of solvents/polymers to avoid dissolution and swelling of underlying layers, our printing process maintains the critical integrity and abruptness required of the different polymer–polymer interfaces in a multilayer TFT device. Note that due to the low

bulk conductivity of F8T2, no patterning of the semiconducting layer is required. In principle, even higher field-effect mobilities up to $0.1 \text{ cm}^2/\text{V}\cdot\text{s}$ can be achieved with P3HT. We have attempted to print similar devices with P3HT as the active layer. However, printed P3HT TFTs showed high bulk conductivity and low ON-OFF current ratios. This is attributed partly to the poor stability of P3HT against doping by exposure to oxygen/water during the inkjet printing steps in air and partly to the direct contact between P3HT and PEDOT/PSS at the source/drain electrodes. PEDOT/PSS causes oxidative doping of conjugated polymers with low ionization potential. Polyfluorene polymers such as F8T2 exhibit much improved stability.

In order to incorporate discreet TFT devices into more complex integrated circuits, a variety of other circuit components needs to be developed as well. Ideally, the manufacturing process should allow fabrication of all components of an integrated circuit, including via-hole interconnects, resistors, and interconnect arrays, by successive solution deposition and printing steps in the same environment. Such a process would lend itself to continuous, reel-to-reel manufacturing, in which a continuous sheet of flexible substrate is passed through a series of processing stations.

We have fabricated resistors by printing lines of PEDOT/PSS with different compositions of PEDOT/PSS ink. The resistance depends very sensitively on the ratio of PEDOT to PSS. A particularly important component for a logic circuit are via-hole interconnects, which provide electrical connections between electrodes and/or interconnects in different layers. We have developed an efficient inkjet process for via-hole fabrication. To fabricate a via-hole through a dielectric layer such as PVP, we inkjet-deposit a sequence of droplets of a good solvent, which locally dissolve the dielectric polymer. Remarkably, upon drying of the solvent, the polymer redeposits only on the side walls of the region defined by the printed droplet, but not in its center ([Fig. 9.14](#)). This is repeated several times until the surface of the underlying layer is exposed, which also provides an automatic “etch stop.” Via-holes are then filled with PEDOT/PSS during the subsequent gate-electrode printing step.

The mechanism for via-hole formation is believed to be similar to that resulting in the familiar coffee-stain effect. In a drying droplet, the evaporation rate of solvent is higher at the edge of the droplet than in its center. This is because of the larger surface area per unit interface area and the larger surface curvature near the edge of the droplet. On a curved surface it is more likely that solvent molecules escape from the liquid phase than on a flat surface, where the probability for recapture is higher. In a regime where the position of the contact line is pinned, this implies that a flow of liquid from the center of the droplet to its edge is established to compensate for the enhanced evaporation rate. This flow takes any dissolved material with it, leading to the formation of a drying ring, with little or no material deposition in the center of the droplet upon drying [81].

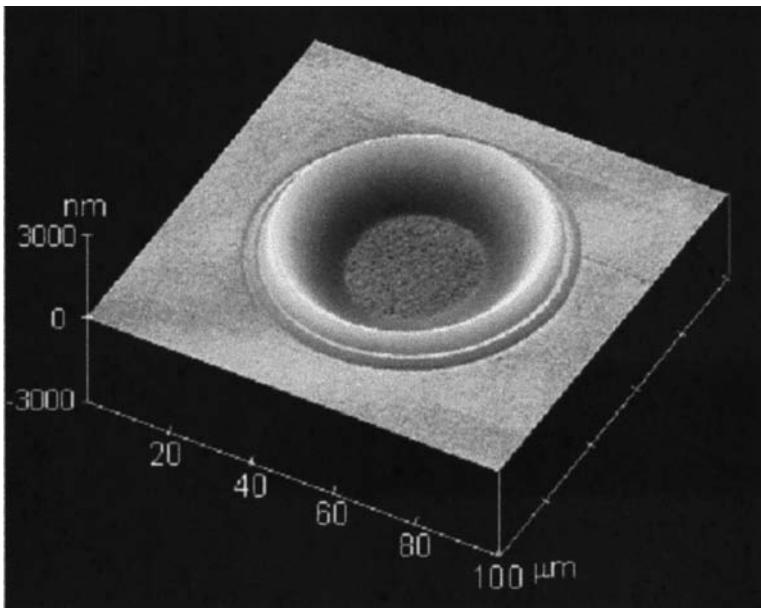


Figure 9.14 Tapping-mode atomic force micrograph of an inkjet-printed via-hole interconnection through a layer of PVP. (From Ref. 84, with copyright permission from Advanced Materials.)

Not surprisingly, we have found that when printing a good solvent onto the layer to be dissolved, the contact line is pinned. It can be shown that the velocity of liquid flow toward the edge is much higher than the velocity of molecule diffusion in solution [82]. Therefore, after drying of the printed droplets, the material is completely removed from the center of the droplet and the underlying layer is uncovered. The underlying layer also acts as an automatic “etch-stopping layer” because the layer sequence is built from an alternating sequence of polar and nonpolar polymer layers. This process can be repeated until the buried conducting layer to be contacted is exposed.

Combining the different components just described we have fabricated simple logic transistor circuits via inkjet printing (Fig. 9.15a). Inverters are the basic building blocks of a logic circuit. They can be implemented with two *p*-type transistors in either an enhancement-load or a depletion-load configuration [83], requiring via-hole interconnections in both cases. The enhancement-load configuration, in which the drain and gate of the load transistor are connected together through a via-hole is appropriate for normally-off transistors, whereas the deple-

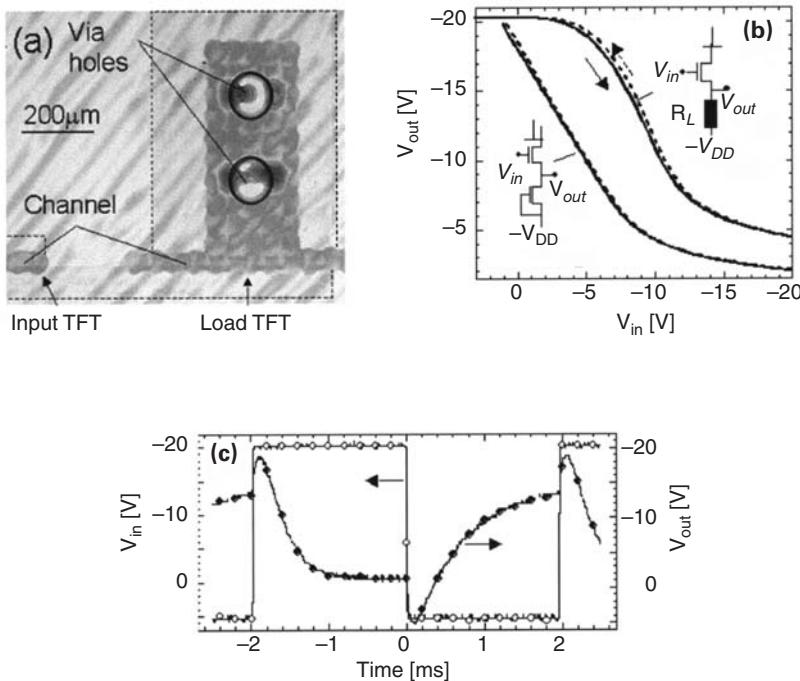


Figure 9.15 (a) Optical microscopy image of two inkjet-printed via-holes connecting drain and gate electrodes of the load TFT in an enhancement-load inkjet-printed inverter ($L = 5 \mu\text{m}$). (b) Static characteristics of an enhancement-load inverter ($L = 5 \mu\text{m}$, width of the input switching transistor $W_I = 2150 \mu\text{m}$, width of the load transistor $W_L = 450 \mu\text{m}$), and a resistance-load inverter ($L = 5 \mu\text{m}$, $W_I = 2150 \mu\text{m}$, $R_L = 47 \text{ M}\Omega$) measured with increasing (solid line) and decreasing (dashed line) input voltage V_{in} ($V_{DD} = 20 \text{ V}$). (c) Dynamic switching characteristics of the resistance-load inverter in (b) ($V_{in} = 250 \text{ Hz}$). The spikes of the output voltage after abrupt switching of the input voltage are induced by direct capacitive coupling on the TFT substrate between input and output electrodes. (From Ref. 42, with copyright permission from *Science*.)

tion-load configuration can be used only for normally-on devices with a negative turn-on voltage. Alternatively, inverters with a printed resistor as the load element have been used. In all three configurations, clean inverter action is observed for switching of the output between -20 V (“high”) and ~ 0 V (“low”) (Fig. 9.15b). The hysteresis of the characteristics is small, reflecting the stability of the transistor threshold voltage. An important requirement for switching a large number of subsequent stages in a more complex logic circuit is that the voltage gain $dV_{\text{out}}/dV_{\text{in}}$ of the individual inverter stage is larger than 1. For the resistor-load device shown in Figure 9.15b, the voltage gain is approximately 2. The depletion-load device exhibits a higher gain of 5–7, but its switching speed is lower than that of the other two device configurations, due to the small load current in normally-on F8T2 TFTs.

The switching performance of the inverter stages was tested by applying a squarewave input voltage and measuring the output voltage with an active probe with a load capacitance of ~ 20 pF. The probe capacitance is equivalent to a fan-out of 4–5; i.e., the source/drain-to-gate overlap capacitance of a discrete transistor as used for the input transistor in the inverters is 4–5 pF. The inkjet-printed inverters can be switched at frequencies up to a few hundred hertz, as shown in Figure 9.15c for the resistor-load device of Figure 9.15b. This switching performance is comparable to that obtained with polymer TFT inverters fabricated by photolithography [32,33], and it appears sufficient for some of the early applications (see Sec. 9.6). Further improvements are expected from increasing polymer mobility and PEDOT conductivity and reducing channel length and overlap capacitance. We have modeled the switching characteristics of the printed inverters using SPICE simulations based on a simple device model, with parameters extracted from the characteristics of discrete TFTs. Good agreement between the experimental and simulated switching characteristics was obtained. This indicates that inkjet fabrication allows controlled and accurate definition of the circuit components. We are currently working on fabrication and simulation of more complex logic circuits.

The inkjet printing process just described is an illustrative example of a solution- and printing-based manufacturing approach in which the necessary control and accuracy required for the fabrication of active electronic devices are achieved by solution self-assembly techniques that allow controlling flow and spreading of liquid droplets with micrometer resolution.

9.6 APPLICATIONS

In the previous sections we have shown that it is possible to fabricate high-performance polymer TFTs with mobilities of 10^{-2} – 10^{-1} cm 2 /V-s, ON–OFF current ratio exceeding 10^5 , and short channel lengths of $L = 2$ μm by high-resolution inkjet-printing techniques. In this final section we discuss potential

commercial applications for this emerging TFT technology. We begin by listing some of the attractive features of polymer TFTs.

Polymer TFT circuits can be fabricated by solution deposition and low-cost, high-volume direct printing techniques such as inkjet printing. Most inorganic TFT technologies are based on a combination of vacuum deposition and photolithographic patterning that involves higher equipment and manufacturing costs. In principle, direct printing is compatible with roll-to-roll processing, in which a continuous sheet of flexible substrate is fed through a series of deposition and patterning process stations. If it was possible to manufacture electronic circuits in an analogous way as printing of newspaper, active electronics would be able to enter new application areas that are currently prohibited due to high manufacturing costs.

Direct printing of polymer TFTs potentially provides a solution to the challenges associated with manufacturing of thin-film electronic circuits over large areas and on flexible, plastic substrates. Techniques such as inkjet printing have the capability of providing local registration, because the inkjet head can be aligned locally with respect to a previously deposited pattern, such that high registration accuracy can be maintained over a large substrate. This local alignment process can be automated by coupling the printhead to an automated pattern-recognition and position-feedback system. This is particularly important for flexible plastic substrates, which tend to distort between subsequent processing steps. These distortions are difficult to compensate for with photolithographic techniques using rigid, prefabricated photomasks.

With direct-write techniques such as inkjet printing, patterns can be formed without developing and subsequent cleaning steps, which in the case of a photolithographic process generate large amounts of waste solvent and wastewater. In a direct-write process, solvent volumes for ink formulations are kept to a minimum and a minimum amount of material is wasted. Therefore, a polymer TFT manufacturing process based on direct printing is potentially environmentally friendly.

In principle, polymer TFTs can be processed at low temperatures below 100°C, compatible with the use of plastic substrates. Many inorganic TFT technologies require processing temperatures exceeding 150–200°C in order to achieve high mobilities and good threshold voltage stability, although low-temperature processing approaches compatible with plastic substrates are currently an area of active research [31,84,85].

A direct-write technique such as inkjet printing opens new opportunities for fast customization of circuits and rapid prototyping applications. In principle it is possible to make every circuit that is fabricated different

via simple software modification of the circuit design. In contrast, in conventional manufacturing based on photolithography, a new set of photomasks needs to be designed and fabricated before a circuit can be altered.

There is a broad range of potential applications for polymer TFT technology. Here we discuss three illustrative examples.

9.6.1 Active-Matrix Displays

In an active-matrix liquid crystal display (AMLCD), each liquid crystal pixel capacitor is connected to its addressing line through a TFT. In the ON-state, the TFT is used to charge the pixel voltage to the correct value. In its OFF-state, the TFT decouples the pixel from the addressing line and holds the pixel voltage while other pixels of the array are addressed (Fig. 9.16a). Active-matrix addressing is required for large or high-resolution displays for which simple passive-matrix addressing would result in unacceptably large crosstalk, as well as for display technologies in which the optical state of the display element has a relatively smooth dependence on the pixel voltage, such as in polymer disperse liquid crystal displays (PDLCs). At present the majority of laptop computer liquid crystal displays is based on a-Si TFT technology.

One of the key TFT requirements for active-matrix display applications is the speed with which the capacitive display element can be charged to the correct voltage. In order to estimate the minimum TFT mobility required for sufficiently fast switching, we assume a simple square pixel with length equal to the width of the TFT; i.e., the TFT is integrated along one side of the pixel electrode. We assume that the display consists of N rows and is driven by the line-at-a-time addressing method. The total frame time T is assumed to be limited by the response time of the display element; i.e., $T \approx 10\text{--}100\text{ ms}$ for an LCD, and $T \approx 1\text{ s}$ for an electrophoretic ink display. The display element, such as a liquid crystal cell or a film of electrophoretic ink, can be represented by a capacitance $C_{de} \approx W^2 \cdot \epsilon_r \cdot \epsilon_0 / d$, where d is the cell thickness and ϵ_r is the relative dielectric constant of the display element. The requirement that the TFT be able to charge the pixel electrode to the correct voltage within a time T/N translates into a condition for the minimum mobility of the TFT:

$$\mu_{\text{FET}} > 4.6 \cdot \frac{L \cdot W \cdot \epsilon_r \cdot \epsilon_0}{C_i \cdot d \cdot (V_g - V_T)} \cdot \frac{N}{T} \quad (9.7)$$

The factor of 4.6 arises if we require that the pixel be charged to the correct voltage within 1% accuracy. For a 14-in. VGA display, for example, we estimate that the mobility needs to be on the order $1\text{ cm}^2/\text{V}\cdot\text{s}$ in order to drive an LC display with a frame time of 100 ms and on the order of $0.1\text{ cm}^2/\text{V}\cdot\text{s}$ for an

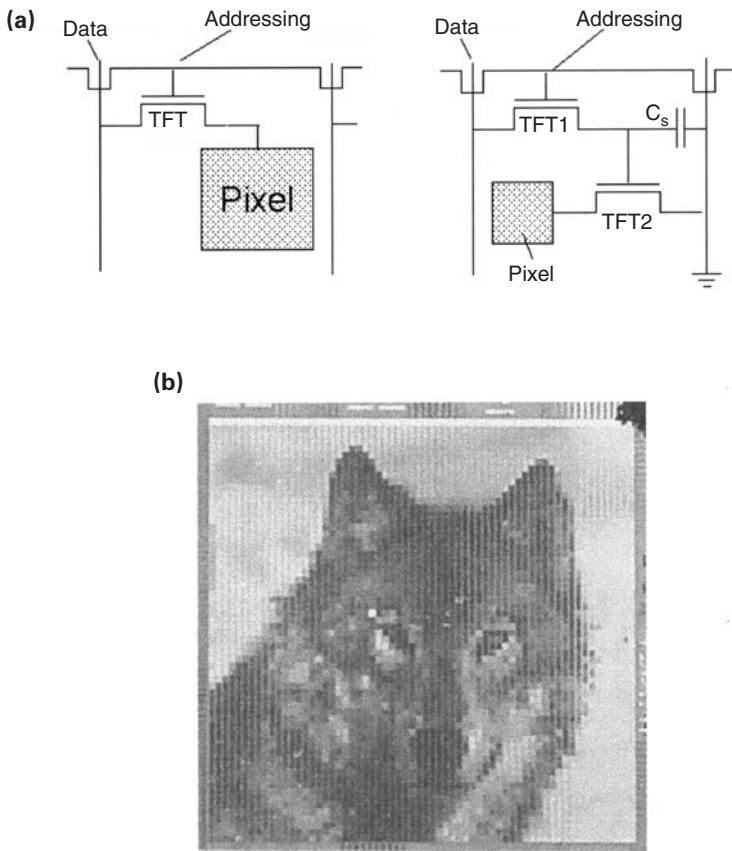


Figure 9.16 (a) Schematic diagram of an active-matrix voltage-driven liquid crystal pixel (left) and current-driven LED pixel (right). (b) Photograph of an 8-bit grayscale polymer disperse liquid crystal (PDLC) display with an active matrix of polymer TFTs. (From Ref. 89, with copyright permission from *Nature*.)

electrophoretic ink display with a frame time of 1 s, respectively. As shown earlier, mobilities of $0.1 \text{ cm}^2/\text{V}\cdot\text{s}$ can now be achieved with polymer TFTs.

In the case of LCDs, a second important requirement relates to the OFF-current of the TFT. I_{OFF} needs to be small enough that the drop of the voltage on the display pixel element V_{pixel} due to charge leakage from the pixel electrode during the frame time is less than some critical value. If we require that the pixel

voltage drop by less than 1% during the frame time, we obtain a condition for I_{OFF} :

$$I_{\text{OFF}} < \frac{C_{de} \cdot V_{\text{pixel}}}{100 \cdot T} \quad (9.8)$$

This implies that for a frame time of 100 ms, OFF-currents less than 0.1–1 pA are required. In principle it is possible to achieve such low OFF-currents with polymer TFTs. Polymer semiconductors tend to have lower photoconductivity than amorphous silicon. The residual extrinsic doping concentration in a conjugated polymer with good environmental stability, such as F8T2, is sufficiently low that the OFF-current in all-polymer F8T2 TFTs is limited only by gate leakage current through the polymer dielectric, which can be minimized by careful optimization of the dielectric. The condition for the OFF-current can be relaxed by adding a storage capacitor C_s in parallel with the pixel capacitor to increase the pixel capacitance to some desired value (which, of course, in turn increases the mobility required to drive the display).

There are other important TFT requirements for display applications, such as the stability of threshold voltage under bias stress conditions, device yield, and device lifetime. First data on threshold voltage stability of polymer TFTs have recently been reported [86], but more careful studies are required, and a discussion of these important engineering issues goes beyond the scope of the present work.

Recently, a polymer disperse liquid crystal (PDLC) display with an active matrix of polymer TFTs fabricated via photolithography on a glass substrate has been demonstrated by a group at Philips Research Laboratories in Eindhoven, The Netherlands [87]. The 64×64 display is a reflective display with gold pixel and TFT electrodes and 8-bit greyscale (Fig. 9.16b). A similar, but smaller, PDLC display has also been demonstrated by Mach et al. [88]. Similarly, in collaboration with E-Ink Corporation, a group at Bell Laboratories has reported an active-matrix electrophoretic ink display on a flexible plastic substrate based on the vacuum-sublimed small-molecule organic semiconductor pentacene [89].

Although these demonstrations are not yet fully based on direct printing manufacturing techniques, it appears now that the device performance of polymer TFTs is sufficiently close to that of amorphous silicon devices that early applications in simple liquid crystal or electrophoretic ink displays are becoming realistic.

9.6.2 Identification Tags

Polymer TFTs are also being considered for active electronic identification tagging as a replacement for optical barcode technology. A simple polymer tag would comprise an inductive, radiofrequency (RF) antenna, such as a metallic coil printed onto a plastic substrate, a rectifying element such as a diode, and a

polymer logic circuit, such as a code generator. Radio frequency radiation emitted from a base station would induce an oscillating voltage in the coil, which would be rectified by the diode and regulated to provide a DC power supply for the logic circuit consisting of a few hundred polymer TFTs, which can be printed onto the same plastic substrate as the antenna. When powered up by the RF radiation, the code generator reads the information code stored in the internal read-only memory (ROM) of the tag and transmits the code back to the base station. The data-transmission function can be realized by coupling the output of the code generator to the gate of a polymer TFT, the source and drain electrodes of which are connected in parallel to the antenna coil. When the TFT is turned on and off by the bit pattern stored in memory, the impedance of the RF antenna is modulated according to the stored bit pattern. This modulation can be detected by a reader in the base station as a modulation of the absorbed RF radiation. An internal clock implemented on the tag determines the data-transmission rate. Polymer TFT-based code generators operating at a bit rate of 100 bit/s have been reported [33].

One possible application of such simple identification tags would be the replacement of optical barcodes in supermarkets, which suffer from problems related to the requirement of direct line of sight and poor reliability. With active electronic tags it would be possible to register all goods in a cart automatically by pushing the cart through a checkout gate equipped with an RF base station and reader. Other, similar applications include electronic luggage labeling in airports and the concept of the electronic refrigerator. An “intelligent fridge” registers information about all products stored inside and automatically reorders fresh supplies from the supermarket when stock is running low or has exceeded its consumption date.

Applications of this type require very low-cost identification tags costing on the order of 1 cent per tag. Such low manufacturing costs appear to be difficult to realize with conventional silicon technology, due to the complex lamination and bonding process that is required to mount a silicon chip onto a plastic substrate comprising the antenna. Polymer TFTs fabricated by high-throughput direct printing and possibly roll-to-roll manufacturing are a promising candidate technology for such very low-cost tagging applications.

9.6.3 ALL-POLYMER OPTOELECTRONIC INTEGRATED CIRCUITS

At present, the main commercial application of conjugated polymers is in polymer light-emitting diode (PLED) displays. Due to the rapid progress of the performance and stability of PLEDs and the development of poly-Si TFT active-matrix addressing, PLED displays currently seem set to become competitive with main-

stream AMLCDs, offering better viewing-angle characteristics and lower power consumption.

In contrast to AMLCDs, active-matrix LED displays are not capacitively driven, the LEDs (Fig. 9.16) need to be supplied with a continuous drive current. This requires a more complicated pixel structure, with at least two TFTs per pixel. In the simplest configuration, shown in the right part of Figure 9.16a, TFT2 provides the drive current to the LED. The current is controlled with a voltage latch consisting of TFT1 and a storage capacitor C_s . In this simple pixel circuit the current is very sensitive to variations of the threshold voltages of TFT1, which is problematic if the threshold voltage varies across a display or shifts significantly under bias stress. To reduce the sensitivity to V_T variations, more complex pixel configurations can be used.

Although at present most groups working on PLED and small-molecule organic LEDs (OLEDs) appear to be using poly-Si TFT technology to satisfy the high-drive-current and low-drive-voltage requirements of PLEDs/OLEDs, it is conceivable that in the longer term, active-matrix addressing might be implemented using polymer TFT technology motivated by obvious simplifications in process integration. If the vision of flexible, wall-size PLED television screens is ever to be realized, a TFT technology will be required that allows large-area processing at low cost.

One of the main challenges to realize PLED displays driven by a polymer TFT active matrix is to satisfy the drive-current requirements of PLEDs. In order to achieve an LED brightness of 100 Cd/m^2 , a state-of-the-art PLED needs to be driven with a current density of $J_c \approx 10 \text{ mA/cm}^2$. If we assume that the polymer TFT is integrated along one side of the pixel, a condition for the minimum TFT mobility can be derived:

$$\mu_{\text{FET}} > \frac{L \cdot W \cdot J_c}{(V_g - V_T)^2 \cdot C_i} \quad (9.9)$$

For a TFT driven at a gate voltage of $V_g = -5 \text{ V}$ in the saturation region ($L = 5 \mu\text{m}$, $W = 300 \mu\text{m}$), we obtain minimum mobilities of $1 \text{ cm}^2/\text{V}\cdot\text{s}$. This is still higher than what can be achieved with polymer TFTs at the moment, but with future improvements of TFT performance and LED efficiency this may become realistic.

Integration of polymer TFTs driving polymer LEDs has been demonstrated using P3HT TFTs with a mobility of $0.1 \text{ cm}^2/\text{V}\cdot\text{s}$ [27]. The simple device configuration that was chosen for this proof-of-concept demonstration consists of a top source-drain P3HT TFT fabricated on a Si/SiO₂ substrate and a PLED stacked on top, with the drain electrode of the TFT acting as the hole-injecting anode of the LED. The TFT and, the LED are separated by a SiO_x interlayer dielectric layer with a via-hole opening that defines the active area of the LED on the drain

electrode of the TFT. All patterns were defined by shadow-mask evaporation (Fig. 9.17a and b).

Figure 17(c) shows the drive current supplied by the TFT and the brightness of the PLED as a function of the gate voltage applied to the TFT. The PLED is fabricated from a green-emitting derivative of polyfluorene and a hole transport layer. When the FET is switched on, the current flows from the FET source layer

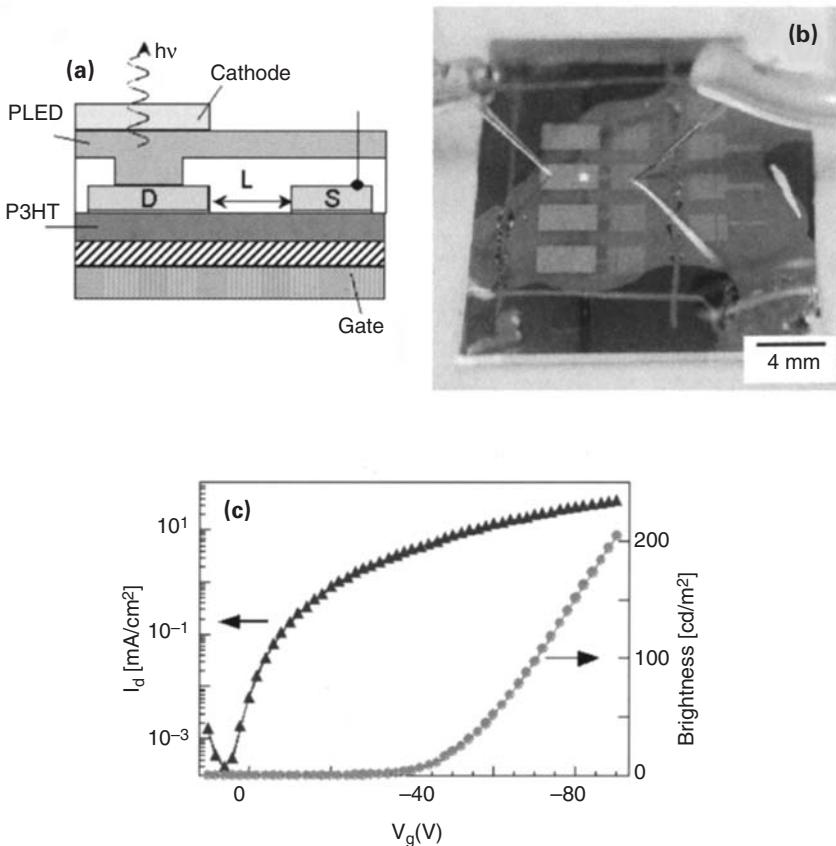


Figure 9.17 (a) Schematic cross section of the multilayer configuration of the integrated TFT-LED pixel. (b) Photograph of a polymer LED driven by a P3HT polymer transistor. (c) Brightness of the LED and drain current supplied to the LED by the TFT as a function of the gate voltage on the TFT ($V_{sd} = 60$ V). I_d is normalized to the area of the LED ($A = 430 \mu\text{m} \times 400 \mu\text{m}$, $L = 75 \mu\text{m}$, $W = 1.5 \text{ mm}$).

electrode to the LED cathode. Evidently, the LED can be switched on and off by the FET gate voltage V_g . At $V_g = -70$ V, the FET supplies a current density of ~ 10 mA/cm² to the LED, resulting in a brightness in excess of 100 cd/m². From the linear relationship between the FET current I_d and the detected photocurrent at sufficiently high FET currents, we estimate the external LED quantum efficiency to be on the order of $\eta_{\text{ext}} = 0.5\%$. This is still somewhat lower than in an optimized LED device configuration, for which efficiencies well above 1% can be obtained with this material. Similar devices have also been reported using a small-molecule OLED [90] and small-molecule TFTs [91]. For practical applications, the gate voltages that need to be applied to reach the required drive current are still too high. However, they can be lowered by reducing the gate-insulator thickness and TFT channel lengths ($L = 75$ μm in this case).

These TFT-LED devices are an example of a more general class of optoelectronic integrated circuits that can be envisioned by integrating polymer TFTs with other polymer devices, such as LEDs, photodiodes, and optical waveguides. Considering the successful demonstration of simple circuits of this type and the availability of direct printing techniques for controlled fabrication, it now appears possible that in the long term all-polymer integrated circuits and displays with combined electrical and optical information processing functions might become viable.

9.7 CONCLUSIONS

In this chapter we have reviewed recent rapid progress in the field of conjugated polymer TFTs. It is now possible to fabricate polymer TFTs by solution-processing techniques with a mobility on the order of 0.01–0.1 cm²/V-s and ON–OFF current-switching ratios exceeding 10⁶. This performance is approaching that of amorphous silicon TFTs. These improvements have been enabled by the exploitation of self-organization mechanisms, leading to better control of polymer microstructure, as well as by the availability of high-purity polymers with well-defined structural regularity. They have led to unexpected scientific discoveries and a deeper understanding of the requirements for high-performance polymer TFT materials. We believe that further future progress is likely, when polymer materials with properties tailored to this application area will be explored.

In parallel with the improvements of device performance, novel manufacturing techniques are being developed that allow fabrication of complete integrated polymer TFT circuits by a combination of direct printing and solution processing. While similar approaches are also being pursued for inorganic materials [92], polymers appear to be particularly well suited for such printing-based manufacturing approaches. Polymers are compatible with low-temperature and even room-temperature processing and show no degradation of device perfor-

mance when manufactured by a direct printing technique such as inkjet printing. Polymer TFT circuits fabricated by solution processing and direct printing are becoming a promising candidate for thin-film electronic applications where low-cost, large-area, and compatibility with flexible plastic substrates are key requirements.

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10

Organic–Inorganic Hybrid Thin-Film Transistors

David B. Mitzi and Cherie R. Kagan

IBM T. J. Watson Research Center, Yorktown Heights, New York,
U.S.A.

10.1 INTRODUCTION

Organic semiconductors continue to raise considerable excitement as potential alternative channel materials for traditional inorganic materials in thin-film transistors (TFTs). Progress in the synthesis and purification of organic semiconductors and in the processing of these materials into devices has enabled organic TFTs to be fabricated with field-effect mobilities of $\sim 1 \text{ cm}^2/\text{V}\cdot\text{s}$ and current modulation of $10^5\text{--}10^8$, comparable to those benchmarked by amorphous silicon [1,2]. The continued push to reduce the cost of electronic devices in existing applications and the opportunities and increasing demand to incorporate electronics in new applications have driven research in organic electronics. The reduced costs of organic devices originate largely from the simple, low-cost techniques by which organic materials may be deposited and patterned and by which devices may be fabricated. These are processes such as thermal evaporation and, preferably, solution-based techniques, including spin-coating, dip-coating, and screen, inkjet, or microcontact printing. The low-temperature conditions, at or near room temperature, employed by these techniques enable organic semiconductors to be deposited on a wider range of substrate materials than typically possible for

inorganic semiconductors, which opens opportunities to fabricate organic electronics on plastic substrates for flexible applications [3–7]. The combination of low-cost and low-temperature processing makes organic TFTs attractive for cheap, large-area, lightweight, and flexible applications, such as low-cost logic, identification tags, smartcards, and many form factors incorporating displays.

The versatility of synthetic organic chemistry has enabled both *n*- and *p*-type semiconductors to be designed and continues to allow new materials to be engineered. Organic semiconductors are solid-state materials consisting of conjugated small molecules [1,8,9], short-chain oligomers [2,10], or long-chain polymers [11–15] (see Chaps. 6–9). The molecules, oligomers, and polymers are held in sufficient proximity by weak van der Waals forces such that the π -orbitals on neighboring conjugated species overlap, giving rise to the semiconducting behavior of and charge transport in the organic solid [16]. The nature of charge transport in organic solids, however, is fundamentally limited by these weak intermolecular binding forces, giving rise to narrow valence and conduction bands, and by electron–phonon coupling. Scattering gives rise to short carrier mean free paths, in comparison to intermolecular distances, and typical room-temperature carrier mobilities are $\sim 1 \text{ cm}^2/\text{V}\cdot\text{s}$ for the best-known organic semiconductors. In addition, since charge transport arises from π -orbital overlap between adjacent conjugated species and is typically highly anisotropic in organic solids, ordered and oriented thin-film solids must be deposited to achieve good TFT performance.

Figure 10.1 shows the advancements made in the performance of organic TFTs, measured by the room-temperature field-effect mobility of devices, as new materials are prepared and device processing is optimized [17]. The best-performing organic TFTs have been fabricated by vacuum evaporation of small molecules, namely, pentacene (black squares) (see Chap. 7) and short-chain oligomers, such as oligothiophenes (black triangles) (see Chap. 6), since these materials form highly ordered and oriented thin films when deposited from the vapor phase. While vacuum evaporation of organic semiconductors has been used to prepare the best-performing devices to date, it is generally accepted to be a more costly route to the fabrication of devices than solution-based techniques. The most widely known soluble organic semiconductors are polymers, in particular polythiophenes (Fig. 10.1, black circles) (see Chaps. 8 and 9). However, these systems form more disordered films with lower carrier mobilities and are more difficult to purify, leading to lower current modulation [18]. The development of new synthetic approaches to prepare solution-deposited organic semiconductors with comparably good device performance has become a focus of the field. While organic semiconductors are attractive for a number of electronic applications, their carrier mobilities limit the achievable speed of TFTs and therefore the range of suitable applications.

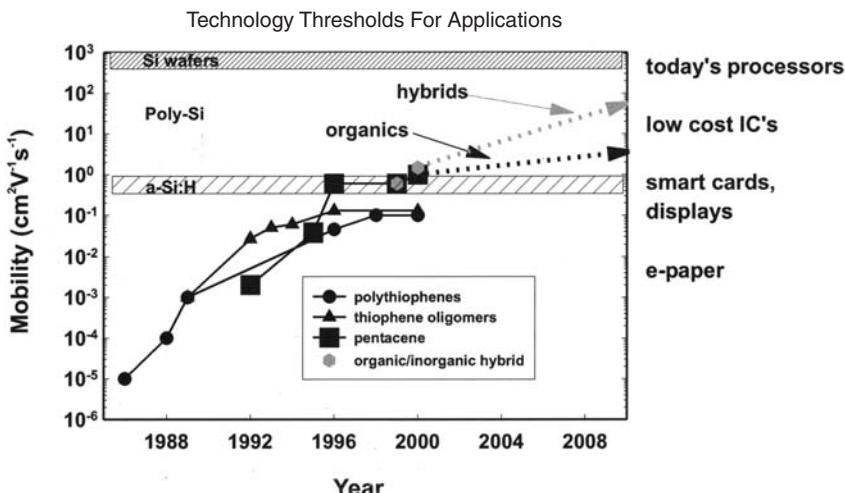


Figure 10.1 Yearly performance improvements in the field-effect mobility of thin film transistors having semiconducting channels consisting of organic small molecules, short-chain oligomers, long-chain polymers, and organic–inorganic hybrid materials. The right-side captions benchmark the required field-effect mobilities for targeted electronic applications. (From Ref. 17, with permission.)

Organic–inorganic hybrid materials combine the useful properties of both organic and inorganic materials within a single molecular-scale composite. While organic–inorganic composites have received attention for their superior mechanical properties [19–23] and optical properties [24–27], hybrid materials are also potentially very attractive for their electrical properties [28–32]. Inorganic solids are bound by strong covalent and ionic bonding, compared to the weak van der Waals attraction in the organic solid state, giving rise to the characteristically high carrier mobilities of inorganic semiconductors. Combining within a single material the desirable electrical properties of an inorganic component with the ease of processing common to organic materials provides unique opportunities with respect to the individual components.

While the interesting magnetic, optical, structural, and electrical properties of organic–inorganic hybrids have been of interest for many years, device possibilities of the hybrids for electronic and optical components have only recently begun to emerge [33]. One interesting optical material, for example, is created

by the successive vacuum deposition of amorphous copper phthalocyanine and titanium oxide layers, yielding a photoconductive composite with a response significantly larger than that observed in single layers of copper phthalocyanine, presumably because of the greater probability of charge separation at the organic–inorganic interface [34]. Electrostatically layered hybrid multilayer structures consisting of alternating layers of positively charged (protonated) poly(allylamine) or PPV and negatively charged CdSe nanocrystals have yielded a broad (nearly white) electroluminescence (EL) spectrum [35], which can be further refined and tailored by selecting nanocrystals of different size [36]. An electrically rectifying device (Zener diode) has similarly been prepared using a two-layer configuration consisting of a p^+ -doped semiconducting polymer [polypyrrole or poly(3-methylthiophene)] layer and an n -type multilayer structure of CdSe (capped with trioctylphosphine oxide) and 1,6-hexanedithiol. By controlling the level of doping in the p -doped polymer, an asymmetrically doped junction can be created, leading to rectifying behavior under forward bias and Zener breakdown in reverse bias [31].

In each of these examples, the functional organic–inorganic hybrid consists of at least one amorphous component. While the family of potential organic–inorganic hybrids is vast, this chapter will focus primarily on the metal halide–based perovskite family, since this is currently one of the most thoroughly studied crystalline hybrid systems with respect to potential electronic device applications. Crystalline hybrids are of particular interest because the crystalline nature facilitates correlating structure–property relationships, thereby providing a convenient mechanism for understanding and tailoring properties. Additionally, the solubility (in a number of common polar solvents) and relatively low melting and boiling points for the metal halide component of the hybrid perovskites provide for a range of low-cost routes for thin-film deposition. Dye-incorporated layered perovskites, for example, have been deposited by single-source thermal ablation (described later) and employed in organic–inorganic light-emitting devices (LEDs) [37]. Spin-coated hybrid perovskites have similarly been used as hole transport and emission layers in LEDs [38–40]. This chapter will focus on thin-film transistors (TFTs) that have been fabricated with spin-coated hybrid perovskite channel layers, yielding devices with carrier mobilities and current modulation similar to those achieved with amorphous silicon [33,41,42]. The long-term goal for the organic–inorganic TFTs (OITFTs) is to achieve potentially higher carrier mobilities (see [Fig. 10.1](#)) while at the same time preserving the low-cost, low-temperature processing capabilities of the organic semiconductors.

10.2 HYBRID PEROVSKITES

The basic layered perovskite structure [43] consists of a superlattice of corner-sharing metal halide sheets and organic cation bilayers or monolayers ([Fig. 10.2](#)).

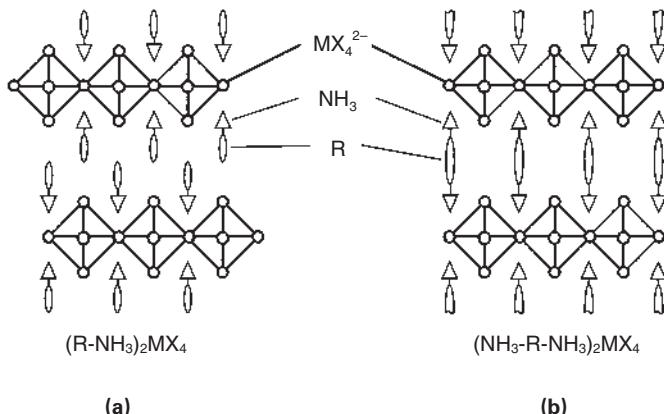


Figure 10.2 Schematic representation of single-layer (100)-oriented perovskites with (a) monoammonium (RNH_3^+) or (b) diammonium (${}^+ \text{H}_3\text{NRNH}_3^+$) organic cations. (Adapted from Ref. 46.)

The simplest perovskites consist of single MX_4^{2-} layers, where M is a divalent metal that adopts an octahedral coordination of anions (e.g., Cu^{2+} , Ni^{2+} , Co^{2+} , Fe^{2+} , Mn^{2+} , Cr^{2+} , Pd^{2+} , Cd^{2+} , Ge^{2+} , Sn^{2+} , Pb^{2+} , Eu^{2+} , or Yb^{2+}) and X is a halide (e.g., Cl^- , Br^- , I^-). Recently, the single-layer perovskite family has been extended to include higher-valence metal halide sheets, with the larger metal valence being enabled by the templating influence of certain organic cations and the incorporation of vacancies on the metal site [44]. The MX_4^{2-} layers are often referred to as “perovskite sheets” because they are conceptually derived from the three-dimensional AMX_3 perovskite structure by taking a one-layer-thick cut from along the $\langle 100 \rangle$ -direction of the three-dimensional crystal lattice. In addition to single-layer perovskite sheets, the structures can also be conveniently synthesized with multiple $\langle 100 \rangle$ -oriented sheets between the organic layers (Fig. 10.3a) [28,45], enabling control over the dimensionality of the inorganic framework, or with alternative orientations (e.g., $\langle 110 \rangle$ and $\langle 111 \rangle$ vs. $\langle 100 \rangle$) of the three-dimensional perovskite structure (Fig. 10.3b,c) [30,46]. The large repertoire of inorganic frameworks enables tailoring of the electronic (e.g., insulating, semiconducting, metallic), optical (e.g., luminescent, nonlinear optical), and magnetic (e.g., ferromagnetic, antiferromagnetic) properties.

The organic cation layer generally comprises molecules containing either one ($\text{R}-\text{NH}_3^+$) or two (${}^+\text{H}_3\text{N}-\text{R}-\text{NH}_3^+$) ammonium groups that tether to the

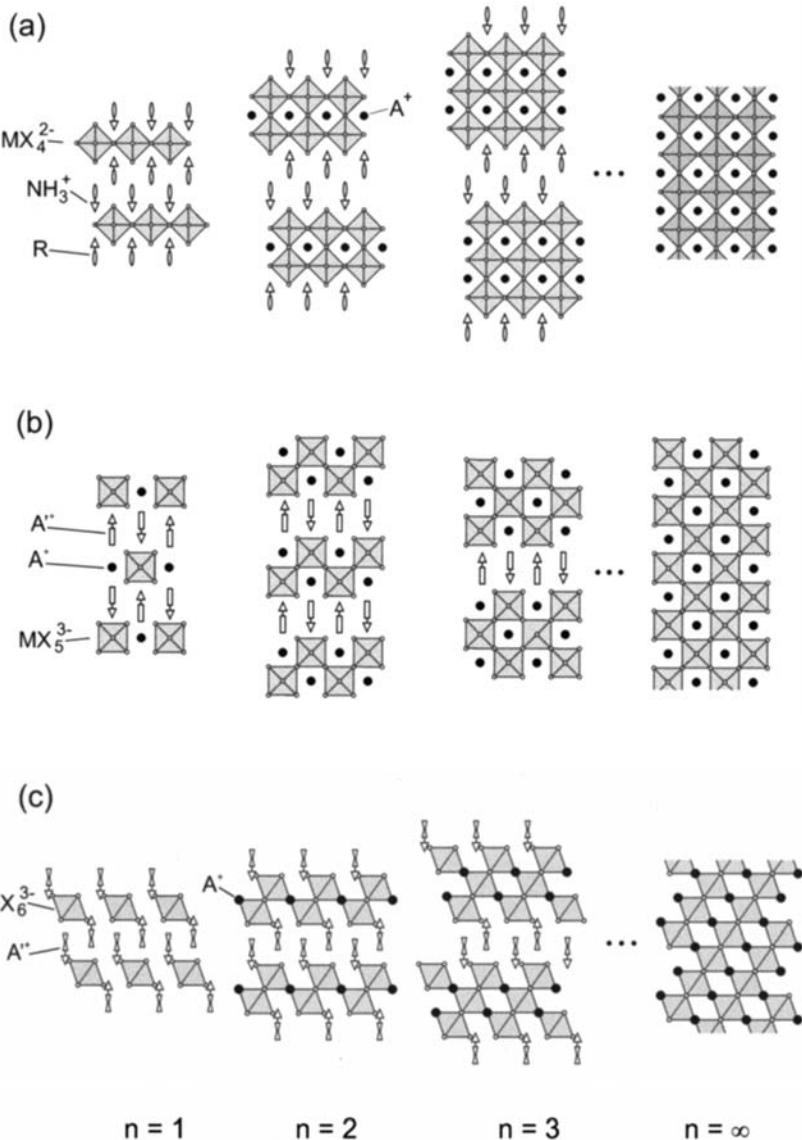


Figure 10.3 (a) Multilayer family of $\langle 100 \rangle$ -oriented layered perovskites, $(\text{RNH}_3)_2\text{A}_{n-1}\text{M}_n\text{X}_{3n+1}$, where R is an organic moiety, A is a small organic cation (or monovalent inorganic cation), M is a metal, and X is a halide. Other families of layered perovskites are also possible, including (b) the $\langle 110 \rangle$ -oriented family, $\text{A}'_2\text{A}_n\text{M}_n\text{X}_{3n+2}$, and (c) the $\langle 111 \rangle$ -oriented family, $\text{A}'_2\text{A}_{n-1}\text{M}_n\text{X}_{3n+3}$. In each of these latter cases, A' is a second organic cation.

halides in the inorganic sheets and an organic tail that extends within the space between layers. While the length of the organic cation can in principle be arbitrarily long, the width or cross-sectional area of the organic moiety is limited by potential steric interaction with nearest-neighbor organic cation sites. Given the distances between nearest-neighbor organic cation sites within the sheets of corner-sharing metal halide octahedra, the cross-sectional area is limited to $\sim 40 \text{ \AA}^2$ for inorganic frameworks based on some of the larger metal cations (e.g., Pb^{2+}) and halides (e.g., I^-). The organic R-group most commonly consists of an alkyl chain or a single-ring aromatic group. These simple organic layers help to define the degree of interaction between, and the properties arising in, the inorganic layers. In addition to the simple organic cations, the structural constraints on the organic component provide for significant flexibility to incorporate more complex functional organic cations within the hybrid structure. Recent examples include 5,5''-bis(2-aminoethyl)-2,2':5',2":5",2"--quaterthiophene [47], 2-naphthylmethylamine [48], 2-anthrylmethylamine [48], and 1-pyrenemethylamine [49].

The unique structural and chemical characteristics of the organic–inorganic perovskites provide for equally interesting and potentially useful physical properties. Many of the layered hybrid perovskites, especially those containing germanium(II), tin(II), or lead(II) halide sheets, are analogous to multilayer quantum well structures, with semiconducting, or even metallic, inorganic sheets alternating with wider band (i.e., HOMO-LUMO) gap organic layers (Fig. 10.4a) [33]. These self-assembling structures share many of the interesting properties of quantum well structures prepared by “artificial” techniques, such as molecular beam epitaxy (MBE). However, since the organic–inorganic perovskites can be grown as single crystals, the tendency for interfacial roughness between the well and barrier layers can essentially be avoided.

Note that in Figure 10.4a, the conduction band of the inorganic layers is substantially below that of the organic layers and the valence band of the inorganic layers is similarly above that of the organic layers. Therefore, the inorganic sheets act as quantum wells for both electrons and holes. In principle, other arrangements of organic and inorganic energy levels are possible [33]. If larger-band-gap metal halide sheets are integrated with more complex, conjugated (i.e., smaller HOMO-LUMO gap) organic cations, the well and barrier layers can be reversed (Fig. 10.4b). Alternatively, given appropriate constituents, the band gaps for the organic and inorganic layers can be offset (Fig. 10.4c), leading to a type II heterostructure in which the wells for the electrons and holes are in different layers. Making substitutions on either the metal or halogen site can modify the band gap of the inorganic layers. As a further example of flexibility, the width of the barrier and well layers can easily be adjusted by changing the length of the organic cations and the number of perovskite sheets between each organic layer. These important modifications can be implemented by simply changing the composition or stoichi-

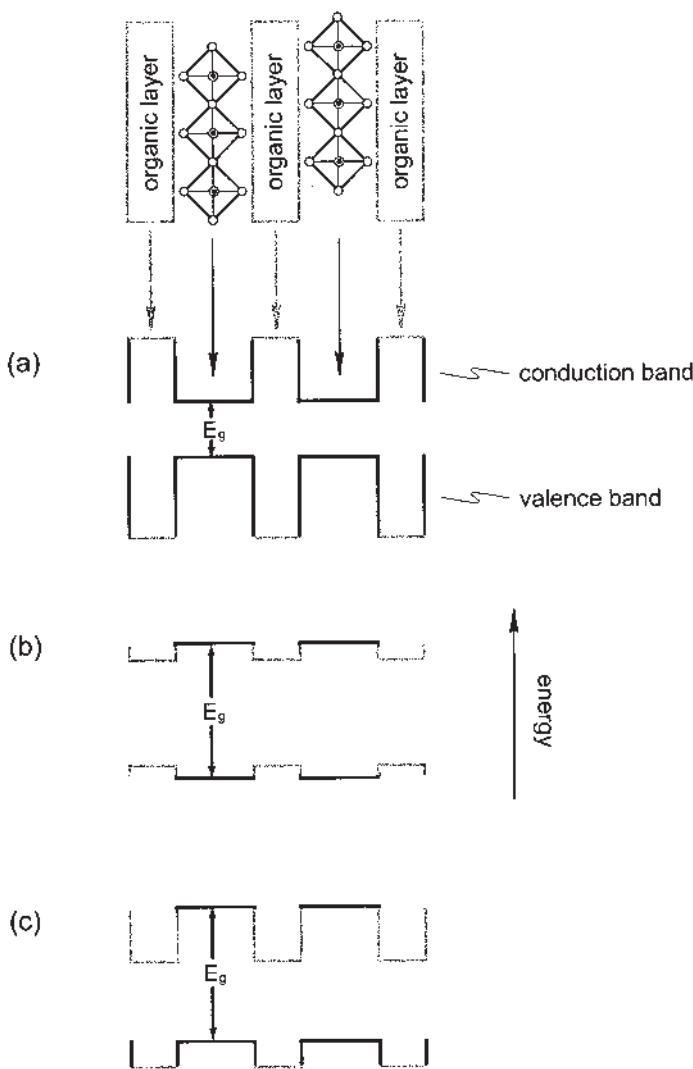


Figure 10.4 Schematic organic–inorganic perovskite structures and several possible energy-level schemes that can arise within these structures. The most common arrangement is shown in (a), where semiconducting inorganic sheets alternate with much wider-band-gap organic layers, resulting in a type I quantum well structure. In (b), wider-band-gap inorganic layers and organic cations with a smaller HOMO-LUMO gap result in the well/barrier roles of the organic and inorganic layers being switched. In (c), by shifting the electron affinity of the organic relative to the inorganic layers, a staggering of the energy levels leads to a type II quantum well structure. (From Ref. 33, with permission.)

ometry of the organic and inorganic salts in the solution used to grow the hybrid crystals or films.

The perovskite quantum well structures, with optically inert (i.e., large HOMO-LUMO gap) organic cations and semiconducting inorganic sheets [e.g., those based on germanium(II), tin(II), or lead(II) iodide or bromide], exhibit sharp resonances (Fig. 10.5) in their room-temperature optical absorption spectra, arising from an exciton state associated with the inorganic semiconducting layers. Since these excitons are associated with the band gap of the inorganic framework, the spectral positions of the transitions can be tailored by substituting different

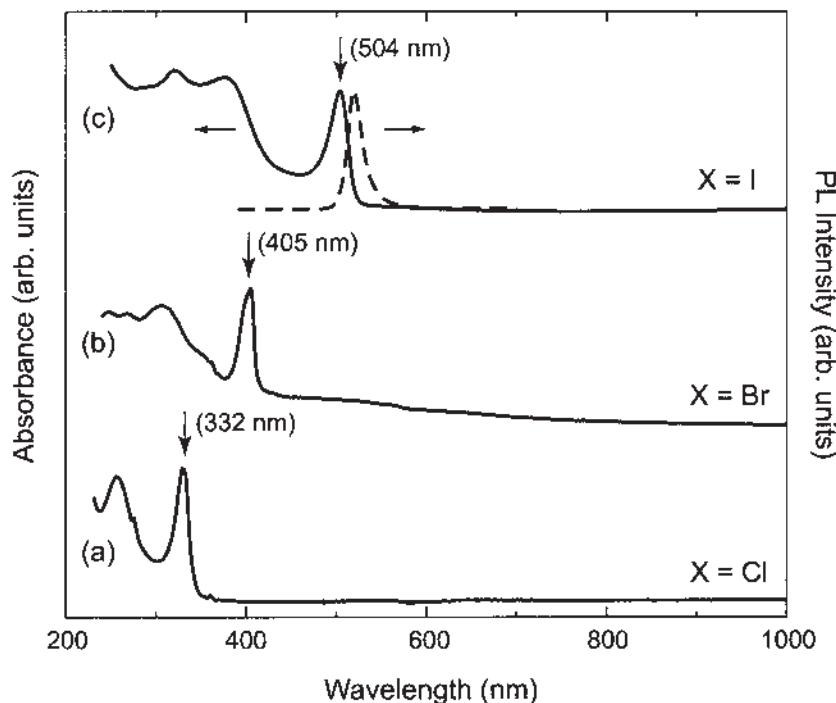


Figure 10.5 Room-temperature UV-vis absorption spectra for thin films of $(C_4H_9NH_3)_2PbX_4$ with (a) $X = Cl$, (b) $X = Br$, (c) $X = I$. In each spectrum, the arrow indicates the position of the exciton absorption peak (with the wavelength in parentheses). In (c), the corresponding photoluminescence (PL) spectrum ($\lambda_{ex} = 370$ nm) is indicated by the dashed curve. Note the small (~ 15 nm) Stokes shift between the absorption and emission peaks for the excitonic transition. (From Ref. 33, with permission.)

metal cations or halides within the inorganic framework [50,51]. The strong binding energy of the excitons, which enables the optical features to be observed at room temperature, arises because of the two-dimensionality of the structure, coupled with the dielectric modulation between the organic and inorganic layers [52]. In addition to the sharp transition in the absorption spectra, the large exciton binding energy and oscillator strength lead to strong photoluminescence, nonlinear optical effects [45], and tunable polariton absorption [53].

In addition to tailoring the position of the optical features by making substitutions on the metal or halogen sites, control over the specific structure of the metal halide sheets through the appropriate choice of the organic cation also provides a means of engineering the optical and electronic properties. This has been demonstrated [42] in the family of fluorine-substituted phenethylammonium tin(II) iodide compounds, $(n\text{-FPEA})_2\text{SnI}_4$, where $n\text{-FPEA}$ = n -fluorophenethyl-

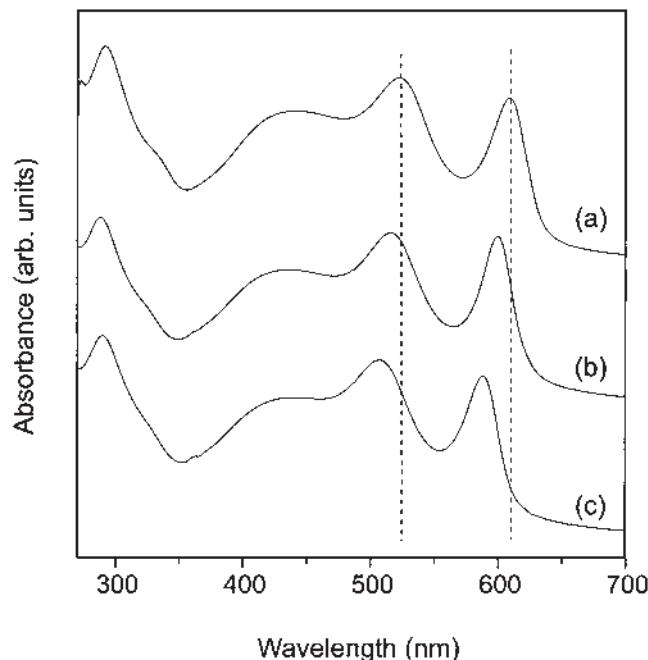


Figure 10.6 Room-temperature UV-vis absorption spectra for spin-coated thin films of (a) $(4\text{-FPEA})_2\text{SnI}_4$, (b) $(3\text{-FPEA})_2\text{SnI}_4$, and (c) $(2\text{-FPEA})_2\text{SnI}_4$ on quartz disks. The dashed lines are guides for the eye to highlight the shift in spectral feature position. (Adapted from Ref. 42.)

ammonium and $n = 2, 3$, or 4 . As n is shifted from 2 to 3 and 4 , the exciton peak shifts progressively from 588 nm to 599 nm and 609 nm , respectively (Fig. 10.6). A corresponding shift in the band edge is also noted. The lowest exciton state arises from excitations between the valence band, which consists of a hybridization of $\text{Sn}(5s)$ and $\text{I}(5p)$ states in the layered tin(II) iodide–based perovskites, and the conduction band, which derives primarily from $\text{Sn}(5p)$ states. The shifts in optical spectra are therefore correlated with changes in the detailed structure of the tin(II) iodide sheets (such as Sn—I—Sn bond angle and average Sn—I bond length), as a function of which organic cation is substituted into the structure. The control over the inorganic framework structure is provided by the organic cation through hydrogen-bonding interactions, which occur between the two components of the structure, as well as through steric constraints imposed by the organic cation on the inorganic sheets.

The electrical transport properties of the layered perovskites have also been examined, with an unusual semiconductor–metal transition being noted in the families, $(\text{R—NH}_3)_2(\text{CH}_3\text{NH}_3)_{n-1}\text{Sn}_n\text{I}_{3n+1}$ and $[\text{NH}_2\text{C(I)}=\text{NH}_2]_2(\text{CH}_3\text{NH}_3)_n\text{Sn}_n\text{I}_{3n+2}$, as a function of increasing perovskite layer thickness (i.e., increasing “ n ”—see Fig. 10.3) [28,30]. While most metal halides are good insulators, the tin(II) halide–based perovskites exhibit high carrier mobilities and, in some cases, even metallic conduction. The three-dimensional perovskite, $\text{CH}_3\text{NH}_3\text{SnI}_3$, for example (i.e., the $n \rightarrow \infty$ member of the previously mentioned families), is a low-carrier-density p -type metal with a Hall hole density of $1/R_h e \approx 2 \times 10^{19} \text{ cm}^{-3}$ and a Hall mobility of $\mu \approx 50 \text{ cm}^2/\text{V-s}$ at room temperature [29]. The relatively high mobility, combined with the ability to conveniently process the materials, renders the tin(II) iodide–based perovskites an interesting family to consider for use as TFT channel materials.

10.3 THIN-FILM DEPOSITION AND PATTERNING

Given the correct stoichiometry of the component organic and inorganic salts in solution or the vapor phase, the hybrid perovskite structure is generally the most stable phase to crystallize (either free-standing or on a substrate) at room temperature. The hybrid perovskites are often soluble in common polar solvents (e.g., water, aqueous acid, alcohols, acetone, acetonitrile), and both components will generally volatilize at relatively low temperatures. This enables the assembly of hybrid perovskite crystals or thin films using a number of simple processes [54]. The range of low-temperature options for thin-film deposition enables convenient deposition on a range of substrates, including those envisioned for flexible plastic displays and low-cost electronic devices.

10.3.1 Solution Processing

Spin-coating can be used to deposit thin films of the soluble organic–inorganic perovskites on a variety of substrates, including glass, quartz, sapphire, and silicon

[33,43,54]. The process involves finding a suitable solvent for the hybrid, preparing a solution with the desired concentration, applying a quantity of the solution to a substrate, and spinning the substrate. As the solution spreads on the substrate, it dries and leaves a deposit of the hybrid. Generally, the films are highly crystalline and oriented, with the plane of the perovskite sheets parallel to the substrate surface (Fig. 10.7). The relevant parameters for the deposition include the choice of substrate, the solvent, the concentration of the hybrid in the solvent, the substrate temperature, and the spin speed. Pretreating the substrate surface with an appropriate adhesion promoter may improve the wetting properties of the solution. Postdeposition, low-temperature annealing ($T < 200^\circ\text{C}$) of the films is also sometimes employed to improve crystallinity and phase purity. Spin-processed hybrid films are generally very smooth (mean roughness $\sim 1\text{--}2\text{ nm}$), suggesting their suitability for use in device structures.

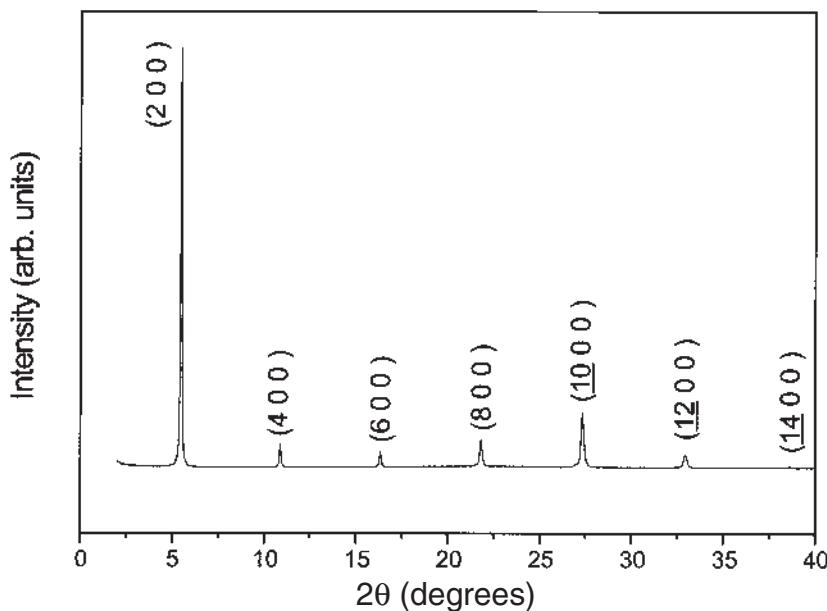


Figure 10.7 Room-temperature X-ray diffraction pattern for a spin-coated film of $(\text{C}_6\text{H}_5\text{C}_2\text{H}_4\text{NH}_3)_2\text{SnI}_4$. The film was spun at 1800 rpm onto a quartz disk, from a solution containing 33 mg of the phenethylammonium-based hybrid dissolved in 0.6 mL of methanol. The indices of the X-ray peaks are shown in parentheses, indicating the high degree of crystallinity and preferred orientation for the film.

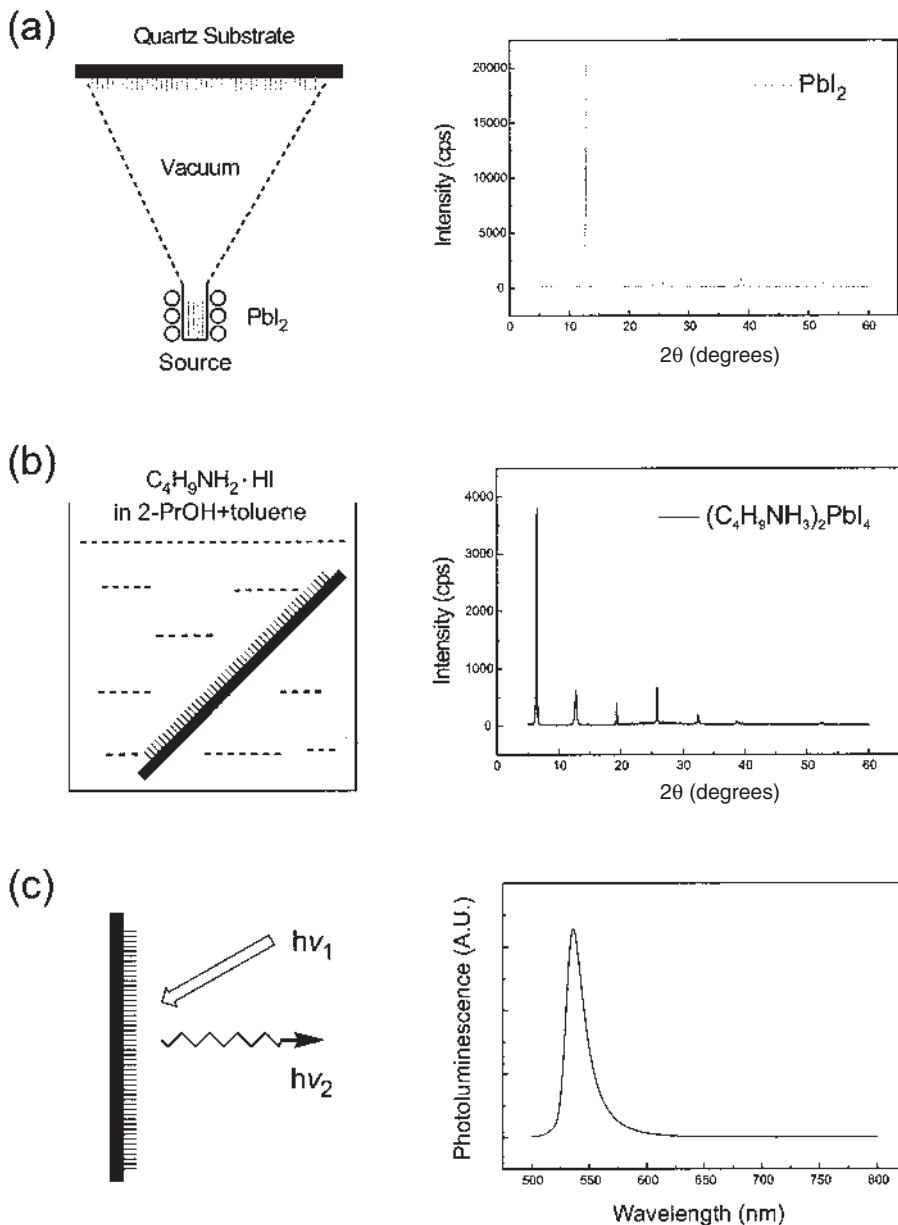
A second solution-based process involves layer-by-layer assembly using the Langmuir–Blodgett (LB) technique [55,56]. This technique involves compressing a close-packed monolayer of amphiphiles at a liquid (subphase)–gas surface using a movable barrier and then mechanically transferring the monolayer assembly to a solid support that is passed through the surface. The pressure applied by the movable barrier in the Langmuir trough enables the amphiphilic molecules at the liquid–gas interface to get close enough together for the relatively weak van der Waals interactions between the molecules to become important and to achieve a nominally close-packed monolayer. The most common interface at which to create the Langmuir monolayer is the air–water surface. Multilayer films are formed through repeated deposition cycles.

Organic–inorganic perovskites, based on a metal halide framework, have recently been formed using the LB technique [57]. A monolayer of docosylammonium bromide ($C_{22}H_{45}NH_3Br$) is spread on a subphase containing lead(II) bromide and methylammonium bromide. The docosylammonium cations are presumably arranged at the surface of the Langmuir trough, with the organic tails pointing out of the solution and the ammonium groups extending into the solution in association with the lead(II) bromide anions. After compressing the monolayer to 30 mN m^{-1} , vertical dipping is used to transfer the monolayer to a fused-quartz substrate, which has been made hydrophobic by treatment with hexamethyldisilazane. Only the single-layer perovskite structure is formed in this process (i.e., one in which a single lead bromide sheet alternates with a bilayer of organic cations), indicating that methylammonium cations are, for the most part, not incorporated into the structure.

In addition to spin-coating and Langmuir–Blodgett techniques, other solution processes for depositing the organic–inorganic hybrids include inkjet printing, stamping, and spray-coating, thereby opening up the possibility of depositing these materials under a wide range of conditions and on many different types of substrates (including flexible plastic). All of these techniques require a suitable solvent for the organic–inorganic hybrid.

10.3.2 Intercalation Reactions

In some cases, a suitable solvent cannot be found for a self-assembling organic–inorganic hybrid. This may arise when the organic and inorganic components of the structure have incompatible solubility requirements or when a good solvent for the hybrid does not wet the substrate surface. Recently, a dip-processing technique [58] has been described (Fig. 10.8) in which a predeposited (vacuum-evaporation- or solution-deposited) metal halide film is dipped into a solution containing the organic cation. The solvent for the dipping solution is selected so that the organic salt is soluble but the starting metal halide and the final organic–inorganic hybrid are not soluble. In the case of the organic–inorganic



perovskites and related hybrids, for which there is generally a large driving force toward the formation of the perovskite structure relative to the organic and inorganic components, the organic cations in solution intercalate into and rapidly react with the metal halide on the substrate and form a crystalline film of the desired hybrid.

For the perovskite family $(R-NH_3)_2(CH_3NH_3)_{n-1}M_nI_{3n+1}$ (R = butyl, phenethyl; M = Pb, Sn; n = 1, 2), for example, toluene/2-propanol mixtures work well as the solvent for the organic salt, and the dipping times are relatively short (several seconds to several minutes, depending on the system) [58]. A film of $(C_4H_9NH_3)_2PbI_4$ was formed from a vacuum-deposited film of PbI_2 (Fig. 10.8a) by dipping it into a butylammonium iodide solution (Fig. 10.8b). The dipping time for the reaction was 1–3 minutes, depending on the thickness of the lead(II) iodide film (2000–3000 Å). After dipping, the films were immediately immersed in a rinse solution of the same solvent ratio as the initial dipping solution (but with no organic salt) and dried in vacuum. The resulting films exhibit the characteristic $(00l)$ X-ray diffraction pattern for the organic–inorganic perovskite (Fig. 10.8b) as well as the characteristic photoluminescence spectrum (Fig. 10.8c).

The three-dimensional perovskite $CH_3NH_3PbI_3$ has also been made using a similar two-step dipping technique [58]. However, in this case, the required dipping times are longer (1–3 hr). Presumably, the longer dipping times are required as a result of the absence of a van der Waals gap in the three-dimensional structure. In $(C_4H_9NH_3)_2PbI_4$ and related layered systems, butylammonium cations can readily diffuse to the boundary with the unreacted PbI_2 through the van der Waals gap within the organic bilayer of the reacted material at the film surface. In the three-dimensional compound, this pathway is not operative and therefore the reaction proceeds at a much slower rate. Note that layered perovskites with diammonium cations (which also lack a van der Waals gap) similarly require a longer period for the reaction to complete. The primary requirements for the two-

Figure 10.8 Schematic representation of the two-step dipping technique. In (a), a film of the metal halide (in this case, PbI_2) is deposited onto a substrate using vacuum evaporation, yielding an ordered film with the characteristic X-ray pattern. The metal halide film is then (b) dipped into a solution containing the organic cation (in this case, $C_4H_9NH_3^+$). The solvent (e.g., a mixture of 2-propanol and toluene) should be a good solvent for the organic cation but not for the metal halide or the resulting hybrid. The resulting film after dipping has the characteristic X-ray pattern for the hybrid perovskite, as well as (c) the characteristic room-temperature photoluminescence spectrum. (Reproduced with permission from Ref. 54. Copyright 2001 American Chemical Society.)

step dipping process therefore include a strong thermodynamic driving force for the formation of the hybrid and a means for the organic species to diffuse through the resulting hybrid so that it can progressively interact with the unreacted inorganic material below the reacted surface layer of the film.

The dip-processing technique eliminates the need for a simultaneously suitable solvent for the organic and inorganic components of the structure (as would be required for solvent techniques) or the need to heat the organic component (as would be required for thermal evaporation techniques). Furthermore, dipping the inorganic film into a solution containing multiple organic cations can readily create mixed organic cation hybrid films. The dipping technique may also provide a promising pathway for patterning, since, prior to the dipping step, the surface of the film can be coated with a resist so that only selected areas will be exposed to the organic cation in solution. It should be noted, however, that during the reaction of the organic cation with the inorganic film, there is often substantial grain growth, potentially leading to morphologically rough films.

An analogous version of the two-step dipping process involves subjecting a metal halide film (predeposited by vacuum deposition) to a vapor of the organic salt [59]. Lead(II) bromide films, for example, can be exposed to alkylammonium bromide, vaporized by heating at a base pressure of 10^{-5} torr. As for the two-step dipping technique, wherein an organic salt in solution can intercalate into and react with a metal halide film, in this case essentially the same process happens, with the organic salt intercalating from the vapor phase. After the organic molecule enters the structure it then reacts with the metal halide framework by a solid-state reaction between the metal halide and the intercalated alkylammonium bromide molecule. Both the solution-based and vapor-phase techniques demonstrate the strong driving force favoring the formation of the perovskite hybrids.

10.3.3 Thermal Evaporation

Upon gradual heating of an organic–inorganic perovskite in a vacuum or under an inert atmosphere, the organic component generally decomposes or dissociates from the system at a significantly lower temperature or more rapidly than the metal halide component [60]. This apparent temporal or thermal incompatibility with evaporation-based deposition techniques has been overcome using two different processes. The first involves heating the organic and inorganic salts separately under vacuum and balancing the evolution rate of the two species by controlling the temperature of each source. The second technique, a single-source thermal ablation (SSTA) technique, involves heating the hybrid perovskite as a composite to a sufficiently high temperature and at a sufficiently fast rate that the organic and inorganic components evolve from the source at essentially the same time and before the organic component has the opportunity to decompose. Both processes can yield crystalline films of the desired hybrids.

Films of the lead(II) iodide–based perovskites, $(C_6H_5C_2H_4NH_3)_2PbI_4$ and $(CH_3NH_3)PbI_3$, have been successfully created using the two-source thermal evaporation process [61]. For the phenethylammonium compound, PbI_2 and $C_6H_5C_2H_4NH_2\cdot HI$ were simultaneously deposited onto a fused-quartz substrate under a base pressure of $\sim 10^{-6}$ torr. During the deposition, the substrates were allowed to remain at room temperature. The resulting films demonstrated the characteristic absorption spectrum and X-ray pattern for the hybrid perovskite. Film growth is proposed to occur through the intercalation of organic ammonium iodide into the simultaneously deposited PbI_2 film. The previously discussed (Sec. 10.3.2) demonstration that hybrid perovskite films can be formed through vapor-phase intercalation of alkylammonium bromide into predeposited lead(II) bromide films provides further support for this mechanism [59].

While the metal halide component of the hybrid evaporates in a well-defined fashion in the two-source process, the organic salt deposition is often difficult to control. In addition, given the relatively long times required for evaporation, high-vacuum conditions are required during these depositions. Recently, a single-source thermal ablation technique has been reported [62] that employs a single evaporation source and very rapid heating. The prototype SSTA apparatus ([Fig. 10.9](#)) consists of a vacuum chamber, with an electrical feed-through to a thin tantalum sheet heater. A starting charge is deposited on the heater in the form of crystals, a powder, or a concentrated solution (which is allowed to dry before ablating). Insoluble powders are ideally placed on the heater in the form of a suspension (in a quick-drying solvent), since this enables the powder to be in better physical and thermal contact with, as well as being more evenly dispersed across, the sheet. After establishing a suitable vacuum, a large current is passed through the heater. While the sheet temperature reaches approximately 1000°C in 1–2 s, the entire starting charge ablates from the heater surface well before it incandesces. The organic and inorganic components reassemble on the substrates (positioned above the tantalum sheet) after ablation to produce optically clear films of the desired product. The initial volume of material placed on the heater determines the resulting film thickness deposited on the substrate (generally, 10 to over 200 nm).

The key aspect to this process is that the ablation is quick enough for the organic and inorganic components to leave the source at essentially the same time and before the organic component has had a chance to decompose. In many cases (especially with relatively simple organic cations), the as-deposited films are single phase and crystalline, indicating that the organic–inorganic hybrids can reassemble on the substrate at room temperature. A number of organic–inorganic hybrids have been deposited using this technique, including $(C_6H_5C_2H_4NH_3)_2PbBr_4$, $(C_6H_5C_2H_4NH_3)_2PbI_4$, $(C_4H_9NH_3)_2SnI_4$, as well as $(C_4H_9NH_3)_2(CH_3NH_3)Sn_2I_7$ [62]. The successful deposition of $(C_4H_9NH_3)_2(CH_3NH_3)Sn_2I_7$ films demonstrates that mixed organic-cation systems can be deposited. An atomic force

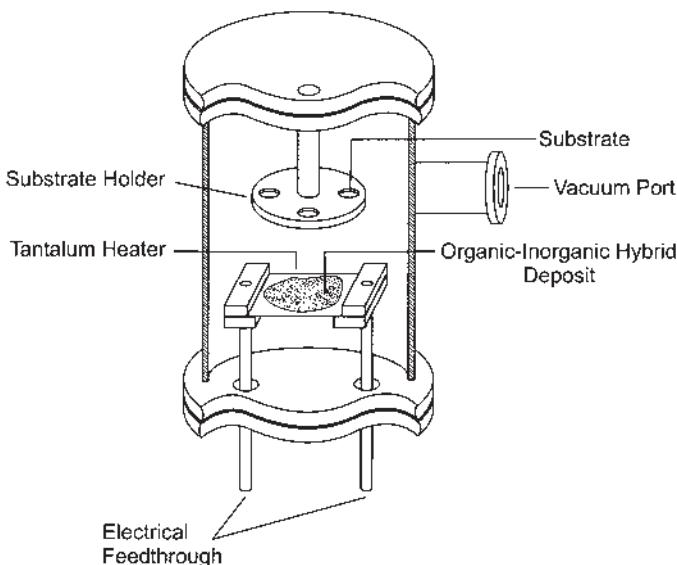


Figure 10.9 Schematic cross section of a single-source thermal ablation chamber. (Reproduced with permission from Ref. 54. Copyright 2001 American Chemical Society.)

microscope (AFM) study of an as-prepared (i.e., unannealed) $(C_6H_5C_2H_4NH_3)_2PbI_4$ film demonstrates a mean roughness of approximately 1.6 nm, similar to the values observed for spin-coated films of the same material. The thermally ablated films also exhibit a relatively small (<75 nm) grain size. X-ray diffraction patterns (Fig. 10.10) demonstrate that the as-deposited films are single phase, crystalline, and highly oriented (as for spin-coated films of the same material).

Deposition of organic–inorganic perovskite films with more complex organic cations, especially those containing diammonium-based cations, sometimes requires a short (~15 min), low-temperature (<250°C) postdeposition anneal to achieve crystalline films. Films of $(H_2AETH)PbX_4$ {X = Br, I; AETH = 1,6-bis[5'-(2"-aminoethyl)-2"-thienyl]hexane}, for example, have been deposited using the SSTA technique [63]. However, the as-deposited films do not exhibit a diffraction pattern, indicating the very fine-grained or amorphous nature of the films. Low-temperature annealing leads to progressive grain growth (as observed in X-ray diffraction patterns and AFM studies) and a bathochromic shift of the characteristic perovskite layer excitation peak in the absorption data. For the $(H_2AETH)PbI_4$ system, the optimal annealing condition for achieving a well-

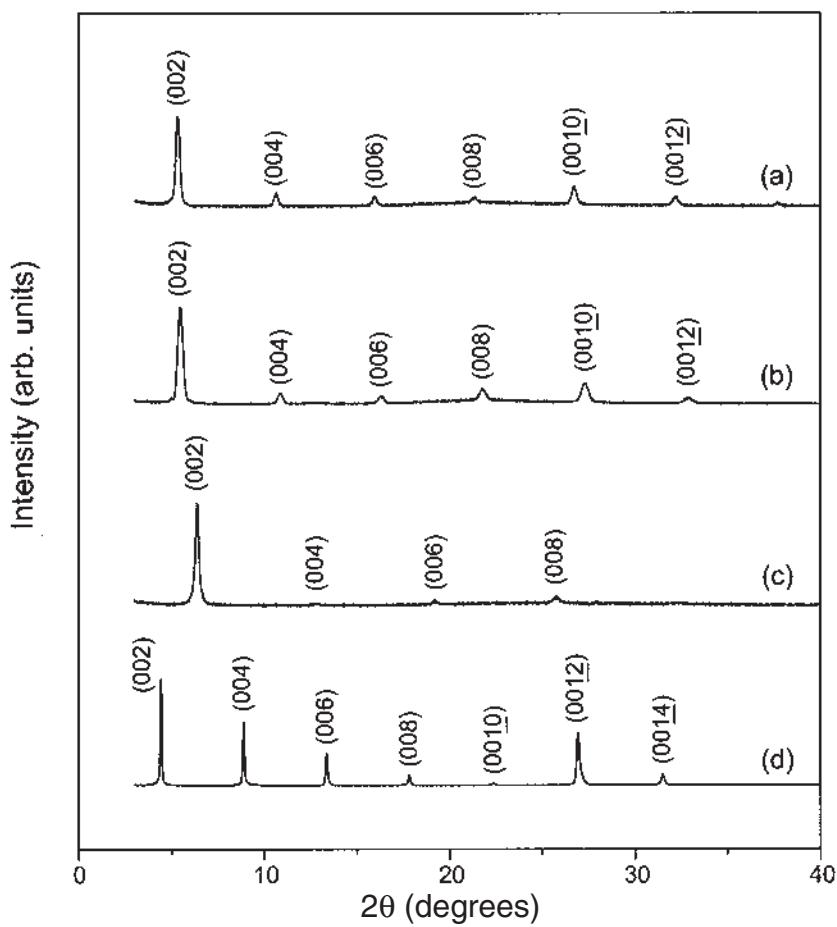


Figure 10.10 Room-temperature X-ray diffraction data for unannealed SSTA-deposited films of the organic–inorganic perovskites (a) $(C_6H_5C_2H_4NH_3)_2PbBr_4$, (b) $(C_6H_5C_2H_4NH_3)_2PbI_4$, (c) $(C_4H_9NH_3)_2SnI_4$, and (d) $(C_4H_9NH_3)_2(CH_3NH_3)Sn_2I_7$. (Reproduced with permission from Ref. 54. Copyright 2001 American Chemical Society.)

crystallized film is approximately 120°C for 15 min. Heating much above this temperature leads to the decomposition of the organic component of the film, leaving behind PbI₂.

As seen from these examples, single-source thermal ablation offers the ability to expeditiously produce high-quality films, without the need to find a suitable solvent for the hybrid (one that both dissolves the hybrid and wets the substrate surface) or to balance deposition rates from multiple evaporation sources. The rapid nature of the ablation process enables a quick turnaround time, with the rate-limiting step being the pump-down of the deposition chamber. The high quality of the resulting films and the ability to pattern the films during the deposition process suggests the applicability of the SSTA process for fabricating devices. As an example, light-emitting devices (LEDs) incorporating SSTA-deposited (H₂AEQT)PbCl₄ [AEQT = 5,5''-bis(aminoethyl)-2,2':5',2''-quater-thiophene] exhibit strong electroluminescence at room temperature [37].

10.3.4 Patterning

In order to fabricate electronic circuits, patterning of the semiconducting hybrid thin films is often necessary to define the active area of the device. The target niche of low-cost and flexible organic or hybrid electronics implies that similarly low-cost and low-temperature patterning processes must be developed. Subtractive processes involving photolithography, etching, or focused-beam (e.g., e-beam, ion-beam, laser-beam) techniques, commonly used to pattern inorganic thin films, are costly and may expose organic–inorganic hybrid thin films to harmful solutions and environments that may degrade the materials properties. Two approaches, inkjet printing and micromolding in capillaries, have been used to confine soluble semiconducting polymers to the channel of TFTs [64–67] (see [Chap. 8](#) and [9](#)). These approaches abandon spin-coating and dip-coating, well-established and commonly used solution-based thin-film deposition processes, and have been demonstrated only for a small number of materials.

Recently, a simple, low-cost, low-temperature, parallel, and additive process (detailed in [Fig. 10.11](#)) has been demonstrated, using microcontact-printed templates to pattern subsequently solution-deposited organic–inorganic hybrid materials [68]. Since this approach is an additive process, the organic–inorganic hybrid materials are not exposed to potentially harmful postdeposition processing. Molecular templates are deposited by microcontact printing “chemical inks” on the surface of TFT gate dielectrics, such as SiO₂ or high-dielectric-constant metal oxides used to achieve low-voltage TFT operation. Polydimethylsiloxane (PDMS) stamps are prepared with desired topographies according to previous reports [69]. A “master” consisting of an exposed and developed photoresist pattern is fabricated by photolithography. A 10:1 (w:w or v:v) mixture of PDMS-Sylgard Silicone Elastomer 184 and Sylgard Curing Agent 184 (Dow Corning Corp., Midland,

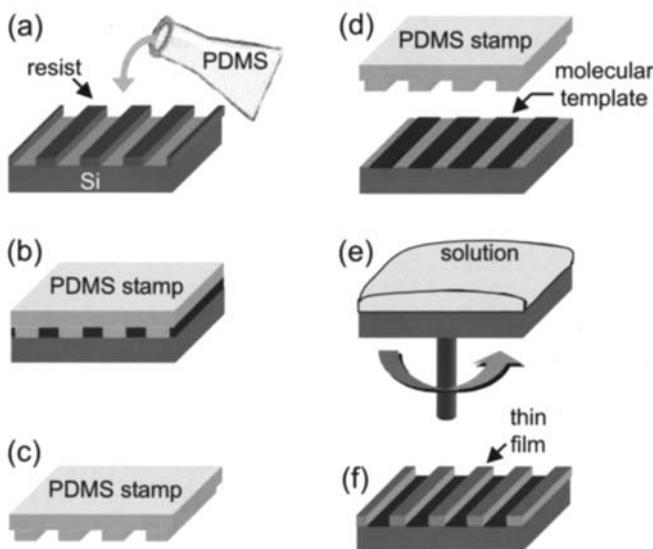


Figure 10.11 Schematic representation of the steps to form patterned solution-deposited thin films using microcontact-printed molecular templates. Polydimethylsiloxane is (a) cast and (b) cured on a photoresist-on-silicon master. (c) The cured PDMS is carefully removed to create the elastomeric stamp with the desired topography used for printing. (d) The PDMS stamp is immersed in a solution of “chemical ink” and brought into conformal contact with the substrate surface, transferring the molecular template in a topography defined by the stamp. (e) A solution of the thin-film material or its precursor is flooded across the substrate surface and spun, depositing the thin-film material only on the bare substrate surface (f). (Reprinted with permission from Ref. 68. Copyright 2001, American Institute of Physics.)

Michigan) is degassed under vacuum for about 10 minutes and then poured over the resist master (Fig. 10.11a). The PDMS is cured at 65°C for 60 minutes, cooled to room temperature (Fig. 10.11b), and carefully peeled from the resist, forming the stamp used in printing (Fig. 10.11c).

The PDMS stamp is “inked” by immersing it for 30 s in a 5 mM ethanolic solution of the chemical ink used to form the molecular template. The stamp is removed from the solution and blown-dry in a nitrogen stream. The “inks” are chosen to have head groups that bind to and tail groups that differentiate the chemical nature of the oxide surfaces: alkyl- and fluorinated alkyltrichlorosilanes are used on SiO_2 [70,71], alkylphosphonic acids are used on SiO_2 or ZrO_2 [72,73], and hydroxamic acids are used on ZrO_2 [73]. The inked PDMS stamp is brought

into conformal contact with the substrate surface for 30–60 s and removed, transferring the chemical ink to the oxide surface in a pattern defined by the stamp topography (Fig. 10.11d). Stamps inked with alkyltrichlorosilanes, fluorinated alkyltrichlorosilanes, and alkylphosphonic acids are heated for 5 min on a 110°C hot plate prior to spin-coating the hybrid material.

Crystals of the organic–inorganic hybrid material are dissolved in polar solvents, such as methanol, and flooded, as shown in Figure 10.11e, across the substrate surface covering both the hydrophobic molecular template and the hydrophilic, bare oxide surface. The hybrid material is deposited, as described earlier, by spinning the substrate at 2000 rpm for 1 min. While no patterning of the solution is observed prior to spin-coating, during spinning the organic–inorganic hybrid material dewets from the hydrophobic surface presented by the molecular template and forms self-assembled thin films of the hybrid material only on the hydrophilic bare oxide surface (Fig. 10.11f).

Figure 10.12 shows optical micrographs of two patterned thin films prepared using hexadecylhydroxamic acid as the molecular template on a

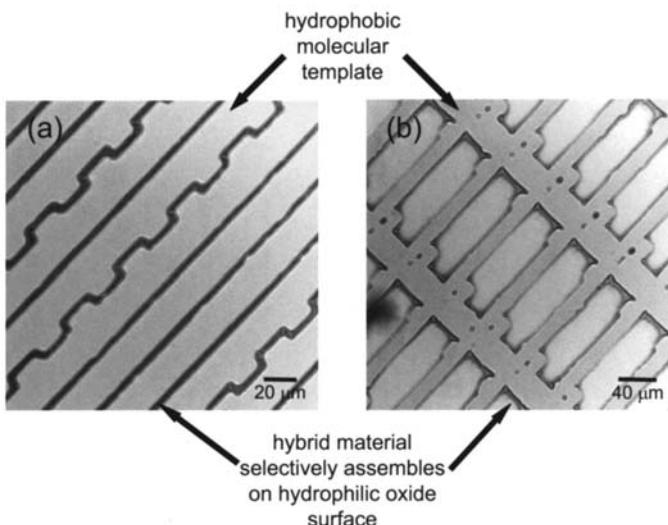


Figure 10.12 Patterned thin films of the organic–inorganic perovskite ($C_6H_5C_2H_4NH_3)_2SnI_4$ prepared by microcontact printing hexadecylhydroxamic acid on ZrO_2 prior to spin-coating the hybrid material. Thin films are deposited in the shape of (a) straight and zigzagged lines and (b) irregular rectangles with curves and dots as defined by the PDMS stamp topography. (Reprinted with permission from Ref. 68. Copyright 2001, American Institute of Physics.)

ZrO_2 surface and spin-coating the organic–inorganic hybrid material $(\text{C}_6\text{H}_5\text{C}_2\text{H}_4\text{NH}_3)_2\text{SnI}_4$. Thin films of the organic–inorganic hybrid material are patterned in the shapes of straight and zigzagged lines (Fig. 10.12a) and more complicated geometries, including irregular rectangles, curves, and dots (Fig. 10.12b). The hydrophobic molecular template appears a uniform gray in the optical micrograph, because the molecular template remains clean after spin-coating the hybrid material. The best resolution achieved to date is ~ 3 microns, as seen by the linewidth in Figure 10.12a.

This process is general to the patterning of solution-deposited thin films and to patterning thin films on different substrate surfaces. In Section 10.4, examples of patterning organic–inorganic hybrid materials using fluorinated alkyl-trichlorosilanes and alkylphosphonic acids on TFT SiO_2 surfaces are demonstrated. Thin films of organic–inorganic perovskites having different organic and inorganic components and perovskites with higher dimensionality, such as the $n = 2$ tin(II) iodides, have also been prepared. This approach can also be used to pattern thin films of metal–organic precursors used to form thin-film metal oxides and copolymers used as e-beam resists.

10.4 THIN-FILM TRANSISTORS

Organic–inorganic perovskites are attractive as a new class of alternative semiconducting TFT channel materials. The hybrid perovskites may be deposited and patterned by simple, low-cost, and low-temperature processes, as is common for organic materials. These materials self-assemble from solution or from the vapor phase to form ordered and oriented thin films of alternating organic and inorganic sheets. The inorganic sheets may be electrically conductive, as shown earlier for the family of tin(II) iodides, and are bound by strong covalent and ionic bonding, promising the high carrier mobilities characteristic of inorganic solids. The applicability of this class of organic–inorganic hybrids as channel materials for TFTs was first demonstrated by fabricating devices based on the semiconducting perovskite $(\text{C}_6\text{H}_5\text{C}_2\text{H}_4\text{NH}_3)_2\text{SnI}_4$ [33,41].

Figure 10.13 is a schematic of a typical TFT test structure used to evaluate the device performance of new materials. Highly doped, $n+$ silicon wafers with 400- to 5000-Å thermally grown silicon dioxide films serve as the gate electrode and gate insulator of the TFT, respectively. Source and drain electrodes are deposited by e-beam evaporation through silicon membrane shadow masks to define the transistor channel width and length. Since the tin(II) iodide perovskites form p -type semiconducting channels, as shown later, high work-function metals such as Pd, Au, Pt, and Ni are selected to form the source and drain electrodes. The organic–inorganic hybrid material is deposited by spin-coating (described in Sec. 10.3.1) on top of the device structure to form a TFT in bottom-contact geometry. While TFTs may be fabricated in top-contact geometry, depos-

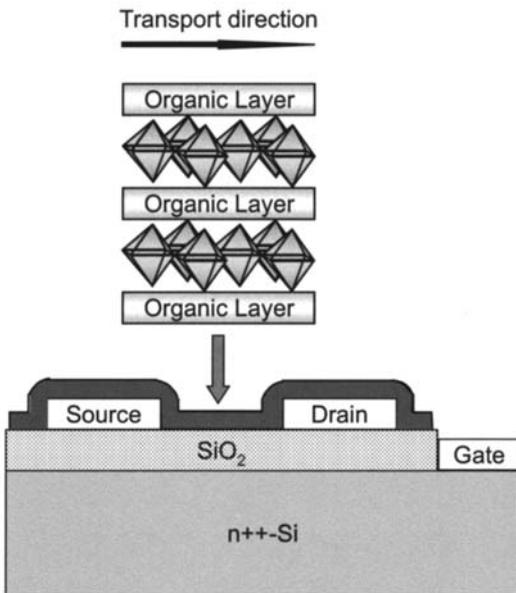


Figure 10.13 Cross section of a typical thin-film transistor test structure used to evaluate the performance of organic–inorganic hybrid semiconducting channel materials. (Adapted from Ref. 41.)

iting organic or organic–inorganic hybrid materials as the last step in device fabrication generally prevents exposure of these materials to potentially damaging deposition conditions during metallization.

Crystals of the organic–inorganic hybrid material, prepared as described earlier, are dissolved in polar solvents, such as methanol, and deposited by spin-coating on top of the device structure to form the semiconducting channel. Organic–inorganic perovskites with simple monoammonium organic cations crystallize from solution and assemble as thin films of the parent compound, with alternating organic and inorganic sheets oriented parallel to the substrate surface, as drawn in Fig. 10.13. The orientation of the extended inorganic framework is advantageous, for it lies in the direction of charge transport between source and drain electrodes. A typical X-ray diffraction pattern of a completed TFT with $(C_6H_5C_2H_4NH_3)_2SnI_4$ as the semiconducting channel, shown in Figure 10.14, reveals the high degree of orientation, because only sharp $(2h\ 0\ 0)$ reflections characteristic of the distance between alternating organic and inorganic sheets are observed. There are no signs of any off-axis peaks, with the only other reflec-

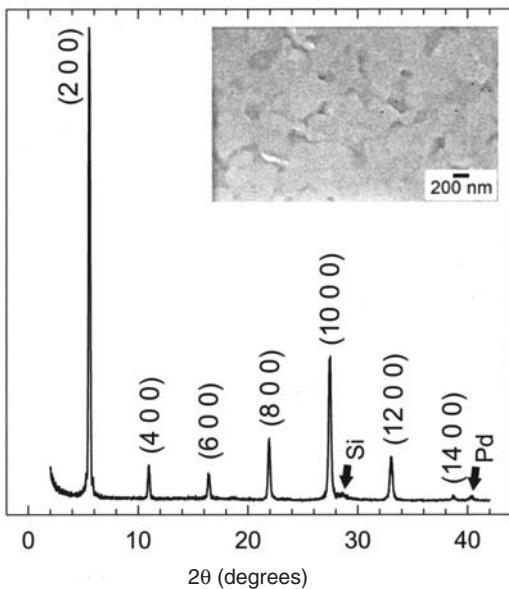


Figure 10.14 X-ray diffraction pattern of a completed $(C_6H_5C_2H_4NH_3)_2SnI_4$ thin-film transistor on a silicon test structure with Pd source and drain electrodes. Inset is a representative scanning electron micrograph showing the morphology of the $(C_6H_5C_2H_4NH_3)_2SnI_4$ thin films in devices. (From Ref. 33, with permission.)

tions being indexed to the Pd source and drain electrodes and the Si substrate. Spin-coating forms optically clear and smooth polycrystalline thin films with grain sizes of ~ 300 nm, as seen in the scanning electron micrograph (inset, Fig. 10.14). Optical absorption spectra of these thin films have an exciton peak at ~ 608 nm, characteristic of the extended inorganic framework of the $n = 1$ tin(II) iodide family. As in organic TFTs, all of the field effect from the gate electrode is in the semiconductor at the interface with the gate insulator. Thin films ~ 100 – 300 Å in thickness are sufficient to form smooth and continuous semiconducting channels that show good transistor behavior. Low-temperature annealing (~ 60 – 80°C) of the devices improves the device performance as the crystallinity of the thin films increases, as monitored by an increase in optical density/decrease in linewidth of the exciton peak in absorption or by a reduction in linewidth in X-ray diffraction. Since tin(II) iodides are sensitive to air, the materials are handled, deposited, and tested in an inert atmosphere.

Organic–inorganic perovskites with a tin(II) iodide inorganic framework and a simple aliphatic or aromatic organic cation show field-modulated conductance. Representative device characteristics, plotting drain current, I_D , as a function of (a) source–drain voltage, V_{DS} , and (b) applied gate voltage, V_G , for a TFT with $(C_6H_5C_2H_4NH_3)_2SnI_4$ as the semiconducting channel, 5000-Å SiO_2 as the gate insulator, and Pd source and drain electrodes are shown in Fig. 10.15. The tin(II) iodide–based perovskites are hole transporters, consistent with Hall measurements (discussed in Sec. 10.2), and form *p*-type semiconducting channels. Application of a negative bias on the gate electrode ($V_G < 0$) increases the number of majority holes in the hybrid semiconductor at the interface with the gate insulator and increases the conductance of the channel, contributing to the

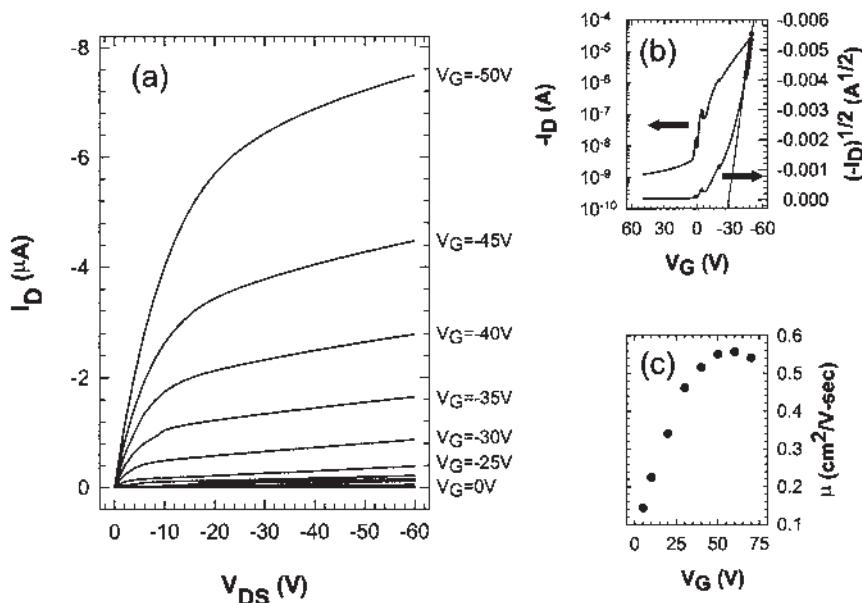


Figure 10.15 Representative device characteristics for an unpatterned $(C_6H_5C_2H_4NH_3)_2SnI_4$ thin-film transistor, deposited by spin-coating onto a device structure with a 5000-Å SiO_2 gate insulator and a channel width/length of 1000 μm /28 μm , as defined by Pd source and drain electrodes. (a) Drain current, I_D , versus drain–source voltage, V_{DS} , as a function of applied gate voltage V_G , (b) I_D and $I_D^{1/2}$ versus V_G at constant $V_{DS} = -100$ V used to calculate the current modulation and field-effect mobility, respectively, in the saturation regime. (c) Field-effect mobility, μ , as a function of V_G sweep at $V_{DS} = -100$ V. (Reprinted with permission from Ref. 41. Copyright 1999 American Association for the Advancement of Science.)

drain current I_D and turning the TFT ON. The devices show typical transistor behavior, with a linear increase in I_D with increasingly negative V_{DS} at low voltage and then saturating at large negative V_{DS} as the channel is pinched off near the drain electrode. For $V_G > 0$, the semiconducting channel is depleted of holes, reducing the conductance of the channel and turning the device OFF.

Organic–inorganic TFTs are modeled by the standard equations used for both inorganic and organic TFTs [74]. Field-effect mobility, μ , and current modulation, I_{ON}/I_{OFF} , are calculated in the saturation regime from plots of $I_D^{1/2}$ versus V_G and I_D versus V_G , respectively, as shown in Fig. 10.15b. For a sweep of ± 50 -V V_G at $V_{DS} = -60$ V, μ is $0.55 \text{ cm}^2/\text{V}\cdot\text{s}$ and I_{ON}/I_{OFF} is greater than 10^4 for the device shown. The field-effect mobility of organic–inorganic TFTs increases with increasing applied gate voltage (Fig. 10.15c), as is common for TFTs fabricated from semiconducting channel materials, such as α -Si and organic semiconductors, that have trap states tailing into the band gap [6,74–76]. For these p -type TFTs, as for the semiconducting tin(II) iodide perovskites, applying an increasingly negative V_G accumulates more majority holes in the semiconducting channel and fills traps localized within its band gap. At large negative V_G , the trap states are filled by accumulated holes and additional holes move with higher mobility characteristic of the delocalized valence band of the intrinsic hybrid semiconductor.

Reducing the thickness of the SiO_2 gate oxide may be used to achieve the same device performance at lower operating voltages, because more majority carriers will accumulate in the channel at lower applied V_G . Figure 10.16 shows I_D – V_{DS} and I_D – V_G curves for organic–inorganic TFTs fabricated with (a) 1500-Å-thick and (b) 400-Å-thick SiO_2 gate insulators. The device characteristics scale to lower applied voltages with (a) the 1500-Å SiO_2 gate insulator yielding $\mu = 0.62 \text{ cm}^2/\text{V}\cdot\text{s}$ at a ± 20 -V V_G sweep and $V_{DS} = -30$ V and (b) the 400-Å gate insulator yielding $\mu = 0.4 \text{ cm}^2/\text{V}\cdot\text{s}$ at a ± 5 -V V_G sweep and $V_{DS} = -10$ V. Alternatively, low-voltage operation in organic TFTs may be achieved by using high-dielectric-constant gate insulators to accumulate more carriers to fill the trap states with thicker gate insulators [6] (see Chap. 7). This same approach may be used to fabricate organic–inorganic TFTs that also operate at low voltage [77].

The devices shown in Figures 10.15 and 10.16 employ unpatterned hybrid semiconductor layers, enabling some leakage of current from the semiconductor to the back gate electrode [78]. Leakage current is measured by I_G on the semiconductor parameter analyzer, above the noise level of the probe station, and is seen by $I_D < 0$ for $V_{DS} = 0$. The leakage is particularly evident in the devices with thinner gate insulators (Fig. 10.16). This leakage current limits the achievable I_{ON}/I_{OFF} to $\sim 10^4$ in these devices. Patterning the semiconductor to the channel of TFTs eliminates the measured leakage current and increases I_{ON}/I_{OFF} . Figure 10.17 shows device characteristics for a $(\text{C}_6\text{H}_5\text{C}_2\text{H}_4\text{NH}_3)_2\text{SnI}_4$ TFT in which the

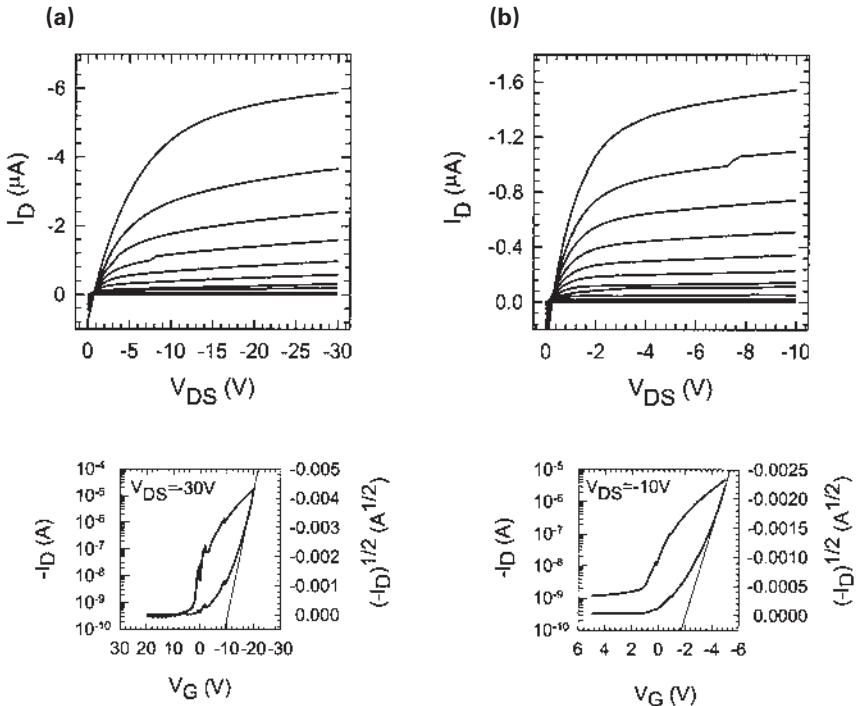


Figure 10.16 (top) I_D versus V_{DS} as a function of V_G and (bottom) I_D and $I_D^{1/2}$ versus V_G for unpatterned $(C_6H_5C_2H_4NH_3)_2SnI_4$ thin-film transistors fabricated on (a) 1500-Å-thick and (b) 400-Å-thick SiO_2 gate insulators.

semiconductor was restricted to the TFT channel by crudely removing the hybrid material near the edge of the wafer and between devices with a solvent-soaked cotton swab. The field-effect mobility remains unchanged from unpatterned devices at $\mu = 0.62 \text{ cm}^2/\text{V}\cdot\text{s}$, but I_{ON}/I_{OFF} is increased to $\sim 10^6$. The field-effect mobility and current modulation in solution-deposited organic–inorganic TFTs are comparable to those fabricated with α -Si and the best vacuum-deposited organic semiconductors as the channel materials. Recently, the field-effect mobility in the saturation regime has been further increased to $1.4 \text{ cm}^2/\text{V}\cdot\text{s}$, with $I_{ON}/I_{OFF} > 10^5$ and current densities greater than 400 A/cm^2 through refinement of the device fabrication [42,79]. Further purification of the starting hybrid by recrystallization and fresh distillation of the solvent (methanol) used for spin-coating apparently give rise to the improved performance.

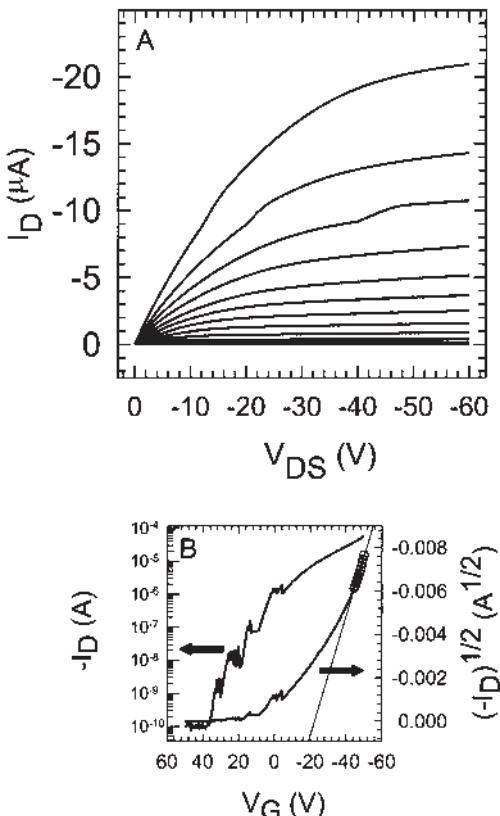


Figure 10.17 Device characteristics (a) I_D-V_{DS} as a function of V_G and (b) I_D-V_G and $I_D^{1/2}-V_G$ for a patterned thin-film transistor prepared by removing the hybrid material away from the transistor channel with a solvent-soaked cotton swab. The device has a 5000-Å SiO₂ gate insulator, and the channel length and width are 28 μm and 1000 μm, respectively, as defined by Pd source and drain electrodes. (From Ref. 33, with permission.)

While hand-patterning of the semiconductor to the channel using a cotton swab demonstrates the achievable device characteristics, using the patterning approach described in Section 10.3.4 enables a simple, low-cost, parallel, and additive process to pattern many devices [68]. Molecular templates are printed onto the device structures, as shown in Figure 10.18a, to restrict the hybrid semiconductor to the TFT channel. Figure 10.18b is an optical micrograph of an array of 16 patterned devices prepared by printing octadecylphosphonic acid as the

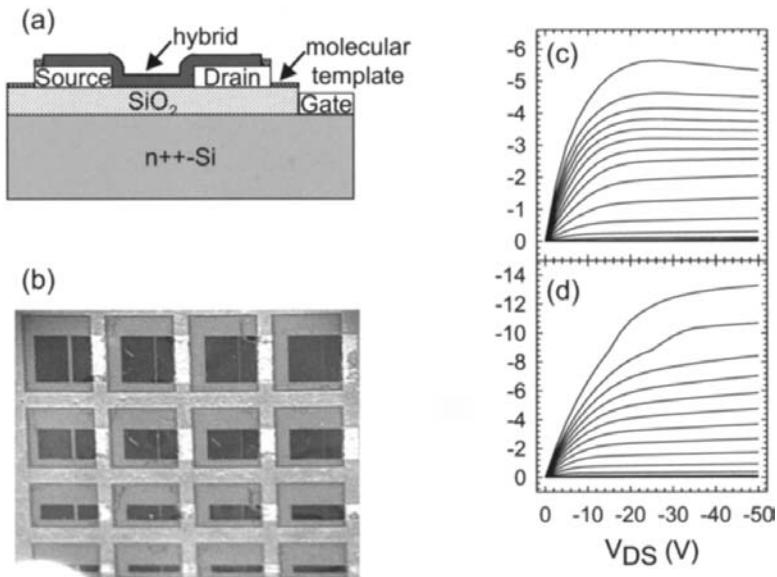


Figure 10.18 (a) Schematic of a thin-film transistor in which the semiconducting hybrid material is restricted to the channel of the transistor by a molecular template. (b) Optical micrograph of an array of 16 patterned transistors having varying channel length and width. $I_D - V_{DS}$ as a function of V_G for thin-film transistors patterned using (c) an octadecylphosphonic acid and (d) a fluorinated alkyltrichlorosilane molecular template. The channel length is 15.8 μm and width is 1000 μm for these TFTs, which have Pd source and drain electrodes and 5000-Å-thick SiO₂ gate insulators. (reprinted with permission from Ref. 68. Copyright 2001, American Institute of Physics.)

molecular template on the SiO₂ gate insulator of the TFT and spin-coating (C₆H₅C₂H₄NH₃)₂SnI₄. The hybrid material self-assembles on the device structure in the shape of rectangles, as defined by the troughs in the topography of the PDMS stamp, where the molecular template is not transferred to the surface.

Figure 10.18c and d shows device characteristics for transistors in arrays of (C₆H₅C₂H₄NH₃)₂SnI₄ TFTs patterned using this approach and (c) octadecylphosphonic acid and (d) (tridecafluoro 1,1,2,2-tetrahydrooctyl)trichlorosilane molecular templates. The field-effect mobility and current modulation for these devices are, for the phosphonic acid template (c) $\mu \sim 0.1 \text{ cm}^2/\text{V}\cdot\text{s}$ and $I_{\text{ON}}/I_{\text{OFF}} \sim 10^4$, and for the fluorinated alkyltrichlorosilane template (d) $\mu \sim 0.5 \text{ cm}^2/\text{V}\cdot\text{s}$ and $I_{\text{ON}}/I_{\text{OFF}} \sim 10^5$. These devices have no leakage current to the back gate electrode, as measured by I_G on the semiconductor parameter analyzer. The per-

formance of TFTs patterned with the silane is comparable to the device characteristics described earlier. The slightly lower mobility and current modulation for the phosphonic acid template may arise from incorporation of a small amount of the acid in the thin film or at an interface. On this device, the phosphonic acid template is visible on the substrate surface, indicative of multilayer formation, and, since the phosphonic acid has some solubility in the solution used to spin-coat the hybrid material, loosely bound molecules may be incorporated [80]. Synthesis of new chemical inks, such as fluorinated alkylphosphonic acids and fluorinated alkylhydroxamic acids, may prevent contamination and may provide a higher hydrophobic:hydrophilic contrast for better feature resolution.

Modification of the electronic structure of the $n = 1$ tin(II) iodide-based perovskites can be achieved by making substitutions on the metal or halogen sites [43]. Recently, the effects of organic cation substitution on the electronic characteristics of TFTs based on the hybrid perovskites have also been explored [42]. Using the same series of fluorine-substituted phenethylammonium-based compounds discussed in Section 10.2, TFT devices were constructed using each hybrid perovskite as the channel layer. [Figure 10.19](#) shows the TFT characteristics as a function of the position of fluorine substitution. Mobilities for the various fluorophenethylammonium tin(II) iodide channel layers are similar to those achieved in comparable phenethylammonium tin(II) iodide layers (typically $0.2\text{--}0.6 \text{ cm}^2/\text{V}\cdot\text{s}$). The peak current in a device with a channel that is $15.4 \mu\text{m}$ long and $1500 \mu\text{m}$ wide decreases across the series $(4\text{-FPEA})_2\text{SnI}_4$, $(3\text{-FPEA})_2\text{SnI}_4$, and $(2\text{-FPEA})_2\text{SnI}_4$, from $160 \mu\text{A}$ to $20 \mu\text{A}$, as the band gap of the hybrid increases. Perhaps equally interesting, the magnitude of the discontinuities in the I_D versus V_G curves decreases in the 4-FPEA sample relative to the previously discussed PEA_2SnI_4 samples. Furthermore, the 2-FPEA sample has much worse behavior in this respect. An atomic force microscope (AFM) examination of the morphology of the films used for these measurements ([Fig. 10.20](#)) indicates that despite the similar spin-coating conditions for the thin films deposited for this study, the grain structure is quite different for the distinct (but related) organic cations. The 3-FPEA- and 4-FPEA-based samples have the largest grains ($\sim 150\text{--}250 \text{ nm}$), whereas the 2-FPEA sample has substantially smaller grains ($<100 \text{ nm}$). The PEA-based sample has an intermediate grain size when deposited using the same conditions. The changes in film morphology might arise either from the different solubility of the organic cations as a function of the position of the fluorine substitution (2-FPEA is more soluble than 4-FPEA in many polar solvents) or from variations in the cation–substrate interactions (in this case, the fluorine atom should interact with the surface in the 3-FPEA and 4-FPEA systems but not in the PEA or 2-FPEA systems). Changing the solvent can have a dramatic effect on the grain structure and size. Methanol solutions were chosen in the studies described in this chapter because the resulting films consisted of reason-

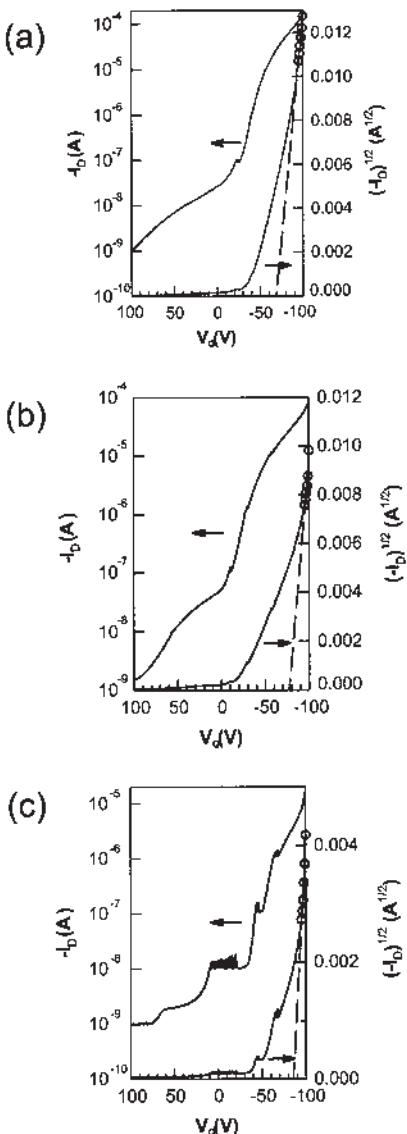


Figure 10.19 Plots of I_D and $I_D^{1/2}$ versus V_G at constant $V_D = -100$ V for TFTs with a spin-coated (a) $(4\text{-FPEA})_2\text{SnI}_4$, (b) $(3\text{-FPEA})_2\text{SnI}_4$, and (c) $(2\text{-FPEA})_2\text{SnI}_4$ channel, each of length $L = 15.4 \mu\text{m}$ and width $W = 1500 \mu\text{m}$. The gate dielectric in each case is 5000-Å SiO_2 . (Reproduced with permission from Ref. 42. Copyright 2001 American Chemical Society.)

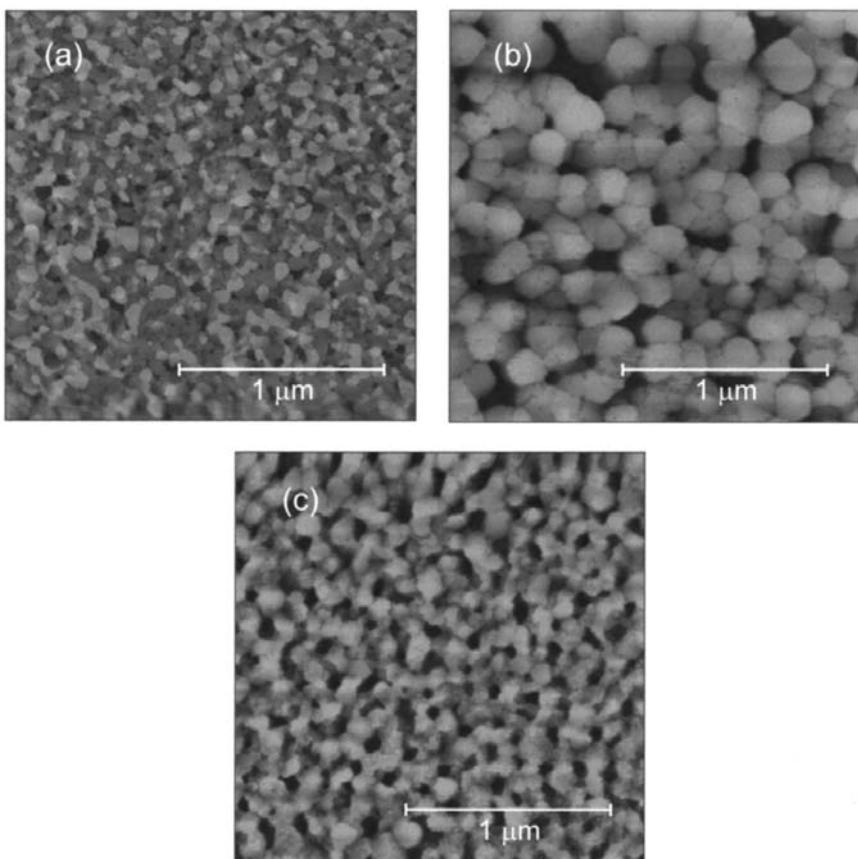


Figure 10.20 Atomic force microscope (AFM) topology images for spin-cast films of (a) $(2\text{-FPEA})_2\text{SnI}_4$, (b) $(3\text{-FPEA})_2\text{SnI}_4$, and (c) $(\text{PEA})_2\text{SnI}_4$ on silicon substrates with 5000 Å of thermally grown oxide. In each case, the spinning solution consisted of 20 mg of the recrystallized hybrid in 1.6 mL of freshly dried and distilled methanol. The spin cycle consisted of a 1-s ramp to 3000 rpm and 30-s dwell at 3000 rpm. Each film was imaged within the channel region of a similar TFT device. (Reproduced with permission from Ref. 42. Copyright 2001 American Chemical Society.)

ably sized and densely packed crystals and yielded the best results for the field-effect transport measurements.

The exploration of the flexibility of the organic cation layer to tailor the properties of the hybrid perovskites is only just beginning. In addition to the devices based on organic cations with a single ammonium-based tethering group, diammonium cations can also be employed to more intimately link adjacent metal halide layers. Besides the simple aliphatic and single-ring aromatic organic cations, more complex and potentially functional organic cations can also be employed. Organic cations with extended conjugated systems offer the possibility of charge transport in the organic layer of the structure instead of or in addition to the charge transport in the inorganic metal halide sheets. In these structures, the inorganic framework can be used to template the conformation and orientation of the organic cations, thereby influencing the properties observed in the hybrid structures.

10.5 CONCLUSIONS

Hybrid perovskites are a versatile family of compounds that enable incorporation of useful properties of organic and inorganic materials within a single crystalline molecular-scale composite. The inorganic component of the structure can be used to control the ordering and conformation of the organic cations and can accommodate a wide range of divalent and trivalent metals. Conversely, both simple and more complex organic cations can be used to template the structural configuration of the metal halide layers and contribute functionality to the hybrid material. The two components provide a unique opportunity to tailor useful materials for TFTs and other electronic devices.

Perhaps of equal importance to the structural flexibility, the hybrid perovskites can also be processed into single crystals or thin films using a number of simple techniques, including ambient-temperature solution-based techniques, which enable deposition on a variety of different shapes and types of substrates. The substantial processibility arises from the self-assembling nature of the hybrid perovskites. Self-assembly results from the integration of a broad range of interactions occurring within the solid—from strong covalent and ionic bonding within the inorganic framework, to ionic and hydrogen-bonding interactions between the organic cations and the metal halide anions, and weak van der Waals interactions between the organic moieties. Convenient processing is also facilitated by the compatible solubility requirements of the organic cation and metal halide components of the hybrid. Unlike most oxides and sulfides, the metal halides are generally soluble in a wide range of polar organic solvents, thereby enabling the solution processing of many hybrid perovskites into thin film form.

Structural/electronic flexibility and facile processing have enabled the demonstration of hybrid TFTs with the highest mobilities to date for solution-pro-

cessed materials. The mobilities are comparable to those achieved in analogous amorphous silicon devices. In principle, the covalent and ionic bonding of the inorganic framework should enable much higher mobility values than the ~ 1 cm²/V-s observed in the current devices. Hall-effect measurements on more three-dimensional hybrid perovskites have yielded Hall mobilities in the range of 50 cm²/V-s [29]. The first organic semiconductor devices attained mobility values only in the range of 10^{-5} cm²/V-s and required approximately 15 years of development before values on the order of unity could be achieved. It is therefore envisioned that with similar focused research on the organic–inorganic hybrids, substantially higher mobilities might be achieved, thereby opening up new opportunities for electronic applications of solution-processed semiconductors.

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