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Document Level: (For Engineering & Quality Document/工程暨品质文件专用)		
☐ Level 1 - Manual	☑ Level 2 – Procedure/SPEC/Report	☐ Level 3 - Operation Instruction
Security Level:		
☐ Security 1 - SMIC Confidential	☑ Security 2 - SMIC Restricted	☐ Security 3 - SMIC Internal

Document Change History

Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description
0T	0.1	2005-1-5	Lan Zhao	Initiate
1T	0.2	2005-02-02	Lan Zhao	Revise: AA.E10b Updated Item　　Unit　　Old　　New AA.E10b　um　1.6　3.30 Add notice of AA: Notice: For 16v Real_HVPMOS, it should be surrounded by N+AA as guarding for the rule AA.E10b of P+ inside DNW to DNW
2T	0.3	2005-3-4	Lan_Zhao	Revise: DRs　　　Old　　　New a) DNW.E01:　1.0um　　2.2um0 b) DNW.E03:　0 or 1.2um　0 or 2.0um c) TPW.E04b:　0um　　0.90um d) TPWE05:　0 or 1.0um　1.0um e) CT.05c　0.19um　　0.26um f) DNW.E08:　For DNW operating at >10v, a PW guarding MUST be added at DNW boundary, in which no 1) AA 2) GT is allowed. Any AA/GT on the PW MUST be put outside the PW guard-ring. Added: a) Add CT.05b, to define diffusion CT to Poly-GT on AA(5V) as 0.19um. b) Add CT.05d, to define diffusion CT to Poly-CG on AA as 0.22um. c) TPW.E07: For every TPW, a PW guarding MUST be added at TPW boundary, in which no 1) AA 2) GT is allowed. Any AA/GT on the PW MUST be put outside the PW guard-ring. Min. PW guard ring width TPW → 0.9um

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3T	0.4	2005-3-28	Lan Zhao	Revised: 1 DRs Old New AA.E02a 0.80um 0.90um Deleted: PF.E04.
4T	0.5	2006-02-24	EH TAN	Revised: Add MIM Design rule (refers to 7.12) Update MASK LAYER INFORMATION. (7.3.3)
5T	0.6	2006-04-05	Lan Zhao	Revised: MiM 17 Minimum space of MIM capacitor bottom(metal) Mn with VIA to below all metal layers. Added: MiM 18. The MIM structure is placed within top metal and next 1 metal.
6T	0.7	2006-8-24	Zhen Yang	Added: 7.3.2 CAP_BP (137) Dummy Layer for DRC/LVS purpose Capacitor Bottom Plate.

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Added
7.3.2
DMPNP   (134)   Dummy Layer for DRC/LVS purpose:
                                    Define 1.8v BJT Device.
7.4.2
Table1
Recommended layer for DRC/LVS
Table2
Recommended layer for DRC/LVS
7.7.6
CAP_BP(137) Description
7.7.7
DMPNP(134) Description
7.13.3.2
PIP.06   Space of CT to CT   0.40
PIP.07   CT on CG which stack on
                   GT is forbidden

PIP.08   If GT/CG of PIP be fully covered by SAB

                   Min/Max/ of CT width   0.36
PIP.09   Min/Max/ of CT width   0.22
PIP.10   Space of CT to SAB   0.22
PIP.11   Width of SAB enclosure GT or CG   0.25
7.13.4.1
BJT18 Design rule for 1.8v BJT
Delete
CT.E05   MIN/MAX Width of CT   0.36
CT.E06   MIN/MAX Space of CT   0.40
Updated
7.4.3.6   Device Spec Table
                   VSG(OLD)   VSG(NEW)
PG-VT   15.5   16.0
ER-VT   15.5   16.0
7.6.19   SAB
                         OLD   NEW
SAB.E06   merge if < 0.60   merge if < 0.52
7.13.3   Capacitor
Lay out example

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7T	0.8	2007-08-15	Zhen Yang	(1) Title: Update "1.8v/15.5v" to "1.8V/3.3V/5.0V/15.5V"
				(2) Add reference documents in item 5
				(3) Update 7.1.4 description,detail the reference document to TD-EE18-CL-2004; TD-EE18-CL-2001
				(4) Add Notice in 7.1.5 Use the table below for processing of various metal level options.
				(5) Add option layers in 7.3.1 table
				(6) Add option layers in 7.3.2 table; add 3.3v BJT Device to DMPNP
				(7) Add option layers in 7.3.3 table
				(8) Add new device layer decryption in 7.4.2 table: add PW1 to table 1; add HRP, stact PIP to table 2; divide BJT to 1.8V and 3.3V ;add notice content
				(9) Add new device application in 7.4.3
				    7.4.3.7 MIM : Fully compatible to MIM of SMIC 0.18um generic logic process
				    7.4.3.8 HRP : Fully compatible to HRP of SMIC 0.18um generic logic process
				    7.4.3.9 BJT : 1.8v/3.3v BJT
				    7.4.3.10 Native Device : 1.8v Native Device
				(10) Modify 7.6.3 TPW(18EE) table
				    TPW.E03 Minimum space between TPW to NW 0.78
				    TPW.E04b DNW Vop<10v, 3.3v or 5v devices 0.78
				    TPW.E05 Minimum space between TPW to PSUB 0 or 1.0
				(11) Modify 7.6.4 NW table
				    NW.E06 PW (for DRC/LVS) region is defined by " Not { (NW) or (DNW) or (PSUB) or (TPW) or (PWI)} "
				(12) Add Notice in 7.6.4 NW
				  Notice:
				  1. Hot NW: NW not connected to the most positive power supply (VDD).
				  2. Cold NW: NW connected to the most positive power supply (VDD).
				  3. To distinguish hot NW and cold NW in DRC, a VDD text label is needed to tag on cold NW net, using the metal layer on the top level. For example:
				  Two NW connected to VDD with M1, with text "VDD" using M1
				(13) Modify table in 7.6.5 AA AA.E13 Minimum space between DNW edge to (P+AA outside PSUB, NW, DNW) 1.18; Add some suggestion in 7.6.5 AA
				Some suggestion guidelines for decoder Well/Tube arrangement

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7.6.5.1 All HV MOS devices are suggested to use pickup AA guard ring to acquire good isolation and reliability.

7.6.5.2 HVNW , MVNW , LVNW arrangement (suggested)

7.6.5.3 HV device well arrangement example(suggested)

(14) Delete 7.6.19 SAB NOTE.1 SAB inside I/O device is blocked from DRC with DRC auxiliary layer RP94 and described in details on 7.7 "DRC AUXILIARY LAYERS"

(15) Modify 7.6.19 SAB NOTE.3 to For I/O and ESD, pls follow "0.18um EEPROM ESD/LatchUp Device Layout Guide Line" (TD-EE18-DR-2005)

(16) Add to 7.6.23 Metal n

The (Mn) layout layer is drawn to define the Metal-2,3,4 of 2P5M process.

The (Mn) layout layer is drawn to define the Metal-2,3,4,5 of 2P6M process.

(17) Modify description 7.6.24 Via-n

The (Vn) layout layer is drawn to define the Via-2,3 of 2P5M Process.

THE (Vn) LAYOUT LAYER IS DRAWN TO DEFINE THE Via-2,3,4 OF 2P6M PROCESS.

(18) Modify table in 7.6.24 Via-n

Vn.5 Vn can be fully or partially stacked on Vn-1, any stacked structure such as stacked Vn/Vn-1/…/V1/CT

(19) Modify description 7.6.25 Top_Via(VT)

The Top_Via (V4) layout layer is drawn to define Via-4, the last Via of 2P5M Process.

The Top_Via (V5) layout layer is drawn to define Via-5, the last Via of 2P6M Process.

(20) Modify table 7.6.25 Top_Via(VT)

(21) Modify description in 7.6.26 Top Metal-TM

The (TM) layout layer is drawn to define the last Metal layer, which is M5 for 2P5M process.

The (TM) layout layer is drawn to define the last Metal layer, which is M6 for 2P6M process

(22) Update 7.6 LAYOUT DESIGN RULE DESCRIPTIONS

7.6.23 Metal-m (m=2,3…n-1)

7.6.24 Via-x (x=2…n-2)

7.6.25 Via-y (y=n-1

7.6.26 TM

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(23) Add 7.7 DRC/LVS AUXILIARY LAYERS: ESDIO;HRP;HRPDMY

(24) Modify to 7.7.5 RESNW, RESP1, RESAA (GDS#95//96/97)

(25) Modify description DMPNP (GDS#134) to "To define 1.8/3.3V PNP for DRC&LVS" in 7.7.7

(26) Modify reference document in 7.10 to TD-EE18-DR-2005

(27) Modify 7.12 Title to Option Layer Drawing Rule

(28) Add 7.12.1 1.8v Native device design rule --- PWI

(29) Add 7.12.2 HRP DESIGN RULES

(30) Item 7.12.3 Change Mn to Mn-1; Add description MIM DESIGN RULES:

The (TM) layout layer is drawn to define the last Metal layer, which is M5 for 2P5M process.

The (TM) layout layer is drawn to define the last Metal layer, which is M6 for 2P6M process.

(31) Add 7.13.3.3 Stack Psub/POLY2 (CG) /ONO/POLY1(GT), Stack_P-i-P Capacitor

(32) Add 7.13.4.2 3.3v BJT

(33) Add 7.13.5 1.8v Native device --- PWI

(34) Modify 8.1 gds file to SMIC_18EE_1.8vRealHV_DeviceExamples_V3p0.gds

(35) Modify 8.2 Layer mapping file to SMIC_18EE_MAP_V3p0.map

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| 8T | 0.9 | 2008-06-27 | Zhen Yang | 1.In 7.3.2 the layer of EXCLU had been added wich layer num is 132.
2.In 7.3.3 MASK LAYER INFORMATION Table ,
1) the value of Mask Generation Formula for mask num:8 was changed from GT to SMICE218GE0.
2) the value of Mask Generation Formula for mask num:14 was changed from DDD to SMICE218GE0.
3) the value of Mask Generation Formula for mask num:18 was changed from SMICE218GE0 to SN.
3.For the 7.3.3 MASK LAYER INFORMATION Table,the Special Notice was changed from < If SN(198) is drawn layer please use input name SN instead of SMIC218GEO (which is logical operation generate) under the column "Mask Generation Formula".> to < SN should be drawing layer!!!>
4.The 7.4.3.11 had been added to 7.4.3 which content was
　　PIP Capcitor: 5.0v PIP capacitor
　　Applications: 5.0v PIP capacitor
5.For the 7.4.3.10 table(0.18 e-EEPROM Device Spec(@25C)),
　1) the Max Vpp(V) of PIP (ONO) was change from <9V to <5V.
　2) the first column for
　UV-Vt was changed from –0.8v to 0.2v
　PG-Vt from –1.0v to –0.65v
　ER-Vt from 3.2v to 3.9v
　IDSC-PG from 38 uA to 32 uA
　3) the cell operation(TD-EE18-CL-2005　0.18um e-EEPROM 2P4M (5M/6M) Salicide 1.8V/3.3V/5.0V/15.5V Cell Operation Condition Rule)bad been add too.
6.For the 7.7.4 table ,the DESCRIPTION of the layer of DRC.EE2 Was change from <Those covered by BITCEL only check BEOL DRC items, that is, from CT to PA.> to Those covered by BITCEL only check BEOL DRC items, that is, from M1 to PA.
7.The 7.7.10 had been added to 7.7 which content was
　　　　EXCLU (GDS#132)
EXCLU (GDS#209): Define un-DRC area
　　　a.) Define un-DRC area
　　　b.) If seal ring drawn by customer, pls add this layer in seal ring for un-DRC purpose
8.For the note of 7.9 ,the note(d .If seal ring drawn by customer, pls add layer EXCLU for un-DRC purpose in this area) had been added
9.Add 7.13.6 for SRAM
Only Metal_Cross SRAM is preferred |

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| 9T | 1.0 | 2009-02-11 | Zhen Yang | 1. Correct the reference file name and add the reference files in item 5
2. Add the note in item 7.1.1 & 7.4.3.1: 1.8v device character is same, but the poly gate GDS is different, for 0.18um Logic it is 30, for 0.18um EERPOM, it is 83.Pls note when use 18um Logic library in 18um EEPROM
3. Add table 7.3.1 a layer DSTR for LVS purpose and delete layer ESD1 in table 7.3.1 because process do not support
4. In 7.4.2 device table:
Add Table 3 for Resistor table 1 in spice model
Add Table 4 for Resistor table 4 in spice model
5. Delete GP.12 in 7.6.13 because pattern density rule not optimized, and the content about pattern density rule update in Part 7.6.27
6. Delete NLL.11 in "7.6.15 NLL" because of no NLH layer, NLL.11 Minimum space between NLL and NLH if two A As are overlapped 0
7. Delete PLL.11 in "7.6.16 PLL" because of no PLH layer PLL.11 Minimum space between PLL and PLH if two AAs are overlapped 0
8. Revise 7.6.27 part B: For detail description dummy pattern rule
9. Add 7.6.28 for dummy Metal/GT/GP rule
10. Modified MIM.13 in "7.12.3 MIM DESIGN RULES" change Minimum space between two Via on bottom metal (Mn-1) from 4.00 to 1.00. |

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10T	0.9	2010-01-14	Wade Ye	1. Title change to " 0.18um e-EEPROM 2P3M (4M/5M/6M) Salicide 1.8V/3.3V/5.0V/15.5V Process Layout Design Rule "

2. Update the reference title and add TD-EE18-DR-2003 in item5.

3. Make Rule scheme label and related rule item NO clear on 7.6.19 SAB label (Page 74), 7.6.20 CT label (Page 77) and 7.6.22 V1 label (Page 82).

4. Purpose change to " To provide SMIC 0.18μm embedded EEPROM 2P3M (4M/5M/6M) Cobalt-Salicide 1.8V/3.3V/5.0V/15.5V process layout design rule for customers use ".

5. Subject content for 3M process/PI/Slot rule item update.

6. Add 3LM process to Table 7.1.5.

7. Table 7.3.1 update for new layer PI / ESD2 / ESD3 added, Change layer DSTR to Table 7.3.2.

8. Table 7.3.2 update for new layers OPCBA/OPCBP/ OPCBM/ MIMDMY added.

9. Update the format of MASK LAYER INFORMATION and NLL and PLL information in mask layer mapping table, Add new layer PI / ESD 1/ESD2 / ESD3, and reference layer AADUM, TPW, HVPF, PSUB, BITCEL and PWI and add Special Notice "2: NLL/PLL can be drawn by customer or by logic operation generated" in item 7.3.3;

10. Update 7.6.23-7.6.26 notices for add 3M process;

11. Add 7.6.27 Polyimide for PI rule

12. Delete 7.6.28 B1 GT Density suggestion (20% - 40%), suggestion is not well define, that is not optimization. Then will cause CTM confuse

13. Delete 7.6.28 B2 GP Density suggestion (50% - 70%), suggestion is not well define, that is not optimization. Then will cause CTM confuse

14. Delete 7.6.28 B3 CG Density suggestion (15% - 35%), suggestion is not well define, that is not optimization. Then will cause CTM confuse

15. Delete 7.6.29.2 Dummy GT rule, exist in Dummy rule file (TD-EE18-DR-2003), so need put here

16. Delete 7.6.29.3 Dummy GP rule, exist in Dummy rule file (TD-EE18-DR-2003), so need put here

17. Update Table 7.7 for new layers added

18. Add the notice c) Since seal-ring is un-DRC area, pls kindly make sure it is fully meet the design rule if it is drawn by customer to 7.7.10.

19. Added OPC block layers 7.7.11;

20. Add 7.7.12 for MiM dummy recognized layer

21. Added 7.8.3 for metal slot rule

22. Added 7.9 e. seal-ring rule if it is drawn by customer

23. Add notice for 7.12.3 for 3M process in MIM design rule

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				24. Add 7.12.4 ESD2 Design rule 25. Add 7.12.5 ESD3 Design rule 26. Delete design rule BJT18.05 in 7.13.4.1, this rule in not necessary for this device, so can delete and no cause CTM confuse. 27. Update 7.13.6 the SRAM application description to SMIC library provide two type SRAM by Atison and Verysilicon library, Atison library compile SRAM is suggested, especially when customer adopt 2.88um^2 size EECell. 28. Correct the Tech Dev. Revision from 1.0 to 0.9;
11T	0.9	2010-08-26	Zhen Yang	1. Adding 7.3.1 4 layer name: HVBN, BITCEL, INST, CLPDMY 2. Adding 7.3.3 Mask HVBN 3. Delete table in 7.7.4, here list delete item DRC.EE1 Those covered by BITCEL are defined as EEArray BitCell regions DRC.EE2 Those covered by BITCEL only check BEOL DRC items, that is, from M1 to PA. DRC.EE3 SMIC provide EEArray BitCell with BITCEL for this DRC purpose. 4. Adding rule 7.7.13 INST(GDS#60) 5. Adding rule 7.7.14 CLPDMY(GDS#87) 6. Adding rule 7.12.6 HVBN(GDS#54) 7. Adding notice in 7.3.4.1 (Note2: 1.8v NMOS has two type, one is standard 1.8v NMOS, the other one is isolated by HVBN 1.8v NMOS) 8. Modify 7.6.28 CG pattern density from 10%~-55% to 10%~80%

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1. Title:

0.18um e-EEPROM 2P3M (4M/5M/6M) Salicide 1.8V/3.3V/5.0V/15.5V Process Layout Design Rule

2. Purpose :

To provide SMIC 0.18μm embedded EEPROM 2P3M (4M/5M/6M) Cobalt-Salicide

1.8V/3.3V/5.0V/15.5V process layout design rule for customers use.

3. Scope:

All SMIC Fabs

4. Nomenclature: N/A

5. Reference:

0.18um e-EEPROM 2P4M(5M/6M) Salicide 1.8v/3.3v/5.0v/15.5v ESD/Latch Up Layout Guide Line
(TD-EE18-DR-2005)
0.18um EEPROM 2P6M Salicide 1.8/3.3/5/15.5V SPICE Model (Version 1.6)
(TD-EE18-SP-2001)
0.18um e-EEPROM 2P4M Salicide 1.8V/3.3V/5.0V/15.5V Design Rule for Shrink Standard Memory Cell(2.88um2)
(TD-EE18-CL-2004).
0.18um e-EEPROM 2P4M Salicide 1.8/3.3/5/15.5V Design Rule for Standard EEPROM Cell (3.96um2)
(TD-EE18-CL-2001)
0.18um LOGIC 1P6M Salicide 1.8/3.3V Current Density Design Rules
(TD-LO18-DR-2006)
0.18um e-EEPROM 2P4M (5M/6M) Salicide 1.8V/3.3V/5.0V/15.5V Cell Operation Condition Rule
(TD-EE18-CL-2005)
0.18um eEEPROM 2p4m Salicide 1.8V/3.3V Dummy Rule
(TD-EE18-DR-2003)

6. Responsibility:

Technology Development Center and PIE

Semiconductor Manufacturing International Corporation

7. Subject Content:

SUBJECT CONTENT

7.1 PURPOSE AND SCOPE
7.2 LAYOUT INFORMATION
7.3 LAYOUT DRAWN LAYERS & MASK LAYERS
7.4 DEVICE TABLE
7.5 LAYOUT RULES DEFINITIONS
7.6 LAYOUT DESIGN RULE DESCRIPTIONS

7.7 DRC/LVS AUXILIARY LAYERS
7.8 METAL FUSE/ALIGNMENT MARK / METAL SLOT SUGGESTION FOR LASER REPAIR AND STRESS RELIEF

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7.9 ANTENNA/SCRIBE LINE SEAL GUARD RING/ BOND PAD OPENING RULES.
7.10 ESD/LATCH-UP PREVENTION LAYOUT GUIDELINES
7.11 CURRENT DENSITY RULES
7.12 OPTION LAYER FOR PWI / HRP / MIM DESIGN RULES
> 7.12.1 PWI   (OPTION LAYER)
> 7.12.2 HRP   (OPTION LAYER)
> 7.12.3 MIM   (OPTION LAYER)
> 7.12.4 ESD2   (OPTION LAYER)
> 7.12.5 ESD3   (OPTION LAYER)

7.13 DEVICE LAYOUT EXAMPLE

> 7.1 PURPOSE and SCOPE
> 7.1.1 This document provides the layout design rules to generate mask layers for SMIC's 0.18µm CMOS digital cobalt-salicide, double poly, four to six metal layers' embedded EEPROM technology operating at 1.8V(core)/15.5V(HV). The following device options are available:
> - 1.8v core N/PMOS, fully compatible to SMIC's 0.18um Generic Logic Process.
>   (Note : 1.8v device character is same, but the poly gate GDS is different, for 0.18um Logic it is 30, for 0.18um EERPOM, it is 83.Pls note when use 18um Logic library in 18um EEPROM)
> - 3.3v special MV N/PMOS, moderated for 3.3V I/O circuits.
> - 5v special HV N/ZMOS/Quasi-HVPMOS, moderated for 5V I/O circuits.
> - 15.5v HV N/ZMOS for high-voltage circuits.
> - 16v HV PMOS for high-voltage circuits.
> - ESD mask for I/O ESD protection circuitry (ESD implant optional)
> - MIM module.
> - Thicker top metal
> - Polyimide layer for Polyimide passivation
>
> 7.1.2 The layout design rules described here do NOT contain Mask Tooling and necessary Boolean Operation information for generating mask layers. To generate all mask layers (before in-house OPC/mask-bias operation), users need to finish the following 2 steps.
> - Finish device layout following this layout design rule.
> - Finish Boolean Operation following "0.18um e-EEPROM 1.8V/3.3V/5.0V/15.5V Mask Generation and Logic Operation Rules"
>
> 7.1.3 The dimensions stated in this document refer to the minimum allowed geometry or the window of allowed geometry. Deviations from these rules have to be approved by SMIC.
>
>
> 7.1.4 The EEPROM cell design rules do not contain in this document. User may refer to "0.18um e-EEPROM 2P4M Salicide 1.8V/3.3V/5.0V/15.5V Design Rule for Shrink Standard

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Memory Cell(2.88um2)   (TD-EE18-CL-2004)".
"0.18um e-EEPROM 2P4M Salicide 1.8/3.3/5/15.5V Design Rule for Standard EEPROM Cell
(3.96um2)   (TD-EE18-CL-2001)"

7.1.5   Use the table below for processing of various metal level options.

Levels of Metal	Top Metal
6LM	Use TM as top metal.
5LM	Skip V5, M5. Use TM as top metal.
4LM	Skip V5, M5, V4, M4 rules. Use TM as top metal.
3LM	Skip V4, M5, V4, M4, V3, M3 rules. Use TM as top metal.

Notice :
n=6 if 2P6M process adopted, and M6 is Top Metal, V5 is Top Via
n=5 if 2P5M process adopted, and M5 is Top Metal, V4 is Top Via
n=4 if 2P4M process adopted, and M4 is Top Metal, V3 is Top Via
n=3 if 2P3M process adopted, and M3 is Top Metal, V2 is Top Via

7.2   LAYOUT INFORMATION
7.2.1   This layout rules only define the necessary drawn layers, not include the Mask Generation
Boolean-Operation rules.
7.2.2   The layout rules defined in this document are expressed in microns (µm).
7.2.3   All drawn dimensions are targeted the same as the finished silicon dimensions.
7.2.4   There should not be any notches of geometry smaller than the allowed minimum spacing.
7.2.5   All drawings and schematics in this document are not drawn to scale.
7.2.6   Only 45° and 90° bends are allowed for poly and metal lines.
7.2.7   All dimensions in this document are considered minimum unless otherwise stated.

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7.3 LAYOUT DRAWN LAYERS & MASK LAYERS

7.3.1 The following drawn layers are necessary to generate related mask layers.

	Tech	Drawn Layer Name	Drawn Layer GDS Num	Description
1	18EE	PSUB	(85)	Define PSUB tube for HV N/ZMOS and EEPROM arrays.
2	18EE	DNW	(19)	Define 16v HVNW tube for Quasi-HVPMOS & Real-HVPMOS, and 3.3v MVNW tube for special 3.3v PMOS.
3	18EE	TPW	(16)	Define 3.3v MVPW tube for special 3.3v NMOS.
4		NW	(14)	Define NW tube for 1.8v PMOS
5		AA	(10)	Define Active Area
6	18EE	TIM	(27)	Define EEPROM FG transistor channel length and NCODE implant.
7	18EE	HVPF	(98)	Define HV-PField Implant Block Region: AAs of 5v/15.5V HVN/ZMOS and Psub Pickup must be covered by HVPF.
8	18EE	VTNH	(49)	Define HVNMOS and EEPROM Arrays VT Implant Region.
9	18EE	TOW	(55)	Define Tunnel Oxide Window Open
		CSD		
10	18EE	GT	(30)	Define HV Poly1 /Cell Select, Floating Gate
11	18EE	ONO	(56)	Define ONO covering regions: ONO must cover all GT and AA of HVPMOS (Quasi/Real), HVN/ZMOS, 3.3v MVN/PMOS, and EEPROM Arrays.
12	18EE	CG	(57)	Define EEPROM Cell Control Gate and PiP capacitor top plate: CG must be inside ONO region.
13		GP	(83)	Define 1.8v LV N/PMOS and Native Device Gate Poly: GP must be outside ONO region.
14	18EE	DDD	(84)	Define HVN/ZMOS DDD Implant Region.
15	Option	HRP	(39)	Define High Resistance Poly
16		NLL	(35)	Define 1.8v NLDD Implant Region.

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17		PLL	(38)	Define 1.8v PLDD Implant Region.
18		SN	(40)	Define N+ S/D Implant Region
19		SP	(43)	Define P+ S/D Implant Region
21		SAB	(48)	Define Salicide Block Region
22		CT	(50)	Define Contact Hole
23		M1	(61)	Define Metal-1
24		V1	(70)	Define Via-1 Hole
25		M2	(62)	Define Metal-2
26		V2	(71)	Define Via-2 Hole
27		M3	(63)	Define Metal-3
28	Option	MIM	(58)	Define MIM Top plate (optional)
29		V3	(72)	Define V3 Hole.
30		M4	(64)	Define Metal-4
31	Option	V4	(73)	Define V4 Hole
32	Option	M5	(65)	Define Metal-5
33	Option	V5	(74)	Define V5 Hole
34	Option	M6	(66)	Define Metal-6
35		PA	(80)	Define Pad Open
36	Option	PWI	(81)	Define 1.8v LV native device
37	Option	FUSE	(209)	Define fuse window
38	Option	PI	(82)	Define Polymide (Negative Resistor)
39	Option	ESD2	(42)	ESD Implant for 2
40	Option	ESD3	(51)	ESD Implant for 3
41	Option	HVBN	(54)	Burried N layer
42		BITCEL	(93)	Define EEArray bitcell
43		INST	(60)	Define Cell
44		CLPDMY	(87:1)	Define SMIC provide clamp diode(data type is 1)

7.3.2   The following drawn layers are RECOMMANDED for DRC/LVS & mask generation purpose.

	Tech	Drawn Layer Name	Drawn Layer GDS Num	Description
1	18EE	RESDMY	(90)	Dummy Layer For DRC/LVS purpose: Define resistors other than covered by Res_NW, Res_AA, Res_P1 CAD layers.
2		RLHVP	(91)	Dummy Layer for DRC/LVS purpose:

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	18EE			Define Real-HVPMOS
3	18EE	5VHVNZ	(92)	Dummy Layer for DRC/LVS purpose: Define 5V HVN/ZMOS
4	18EE	BITCEL	(93)	Dummy Layer for DRC/LVS purpose: Define EEArray BitCell
5		RESNW	(95)	Dummy Layer For DRC/LVS purpose: Define NW resistors.
6		RESP1	(96)	Dummy Layer for DRC/LVS purpose: Define non-Salicide Poly2-(GP) resistors.
7		RESAA	(97)	Dummy Layer for DRC/LVS purpose: Define non-Salicide Diffusion resistors.
8		CAPBP	(137)	Dummy Layer for DRC/LVS purpose: Capacitor Bottom Plate.
9		DMPNP	(134)	Dummy Layer for DRC/LVS purpose: Define 1.8v/3.3v BJT Device.
10		ESDIO	(133)	Dummy Layer for IO region DRC/LVS purpose: Define ESD/IO Device
11		HRP	(39)	Dummy Layer for HRP DRC/LVS purpose: Define High Resistor Poly Device
12		HRPDMY	(210)	Dummy Layer for HRP DRC/LVS purpose: Define High Resistor Poly Device
13		EXCLU	(132)	unDRC Area
14		DSTR	(138)	Define diode for LVS purpose
15		OPCBA	(100)	Blocking layer for DRC/LVS operation on AA
16		OPCBP	(101)	Blocking layer for DRC/LVS operation on GP
17		OPCBM	(102)	Blocking layer for DRC/LVS operation on M1
18		MIMDMY	(88,1)	Define the dummy MiM

7.3.3   MASK LAYER INFORMATION.

The mask layers generated with other layout drawn layers follow mask generation design rules in LOTA "SMICE218GE0".

Mask ID	Process Name	Dig. Area Tone	GDS No	Mask Generation Formula	Description	Optional
120	AA	D	10	SMICE218GE0	Active Area / SDG	Must
121	AR	C	11	SMICE218GE0	AA Oxide Define Reverse	Must
394	TIM	C	27	NA	Tunnel Implant	Must
292	DNW	C	19	NA	Deep N well imp for substrate	Must

noise suppression

318	HVBN	C	54	NA	1.8v NMOS isolated deep N layer	Option
396	Vtnh	C	49	NA	NCH HV VT adjust Implant	Must
391	PFLD	D	46	SMICE218GE0	Pwell Field Implant	Must
320	TOW	C	55	NA	Tunnel Oxide Window	Must
202	CSD	C	105	NA	Cell Source/Drain Implant	Optional
130	GT	D	30	SMICE218GE0	Poly Gate / Poly-1 / ONO Gate	Must
191	PW	D	20	SMICE218GE0	P-Well / P-Tub	Must
192	NW	C	14	NA	N-Well / N-Tub	Must
321	ONO	D	56	NA	ONO Layer Etch	Must
330	CG	C	57	SMICE218GE0	Control Gate (poly2)	Must
331	GP	D	83	SMICE218GE0	Gate Poly (Poly2)	Must
316	DDD	C	84	SMICE218GE0	DDD Implant	Must
116	NLL*	C	35	SMICE218GE0	NMOS LDD Implant for Low VDD	Must
113	PLL*	C	38	SMICE218GE0	PMOS LDD Implant for Low VDD	Must
198	SN	C	40	NA	N+ S/D Implant	Must
413	HRP	C	39	NA	High Resistant Poly Implant	Optional
197	SP	C	43	NA	P+ S/D Implant	Must
110	ESD1	C	41	SMICE218GE0	ESD Implant for 1	Optional
111	ESD2	C	42	NA	ESD Implant for 2	Optional
210	ESD3	C	51	NA	ESD Implant for 3	Optional
199	CODE	C	25	NA	Code Implant	Optional
155	SAB	D	48	NA	Resist Protect Oxide / Salicide Block	Must
156	CT	C	50	NA	CT Contact Hole (Metal to Si/Poly)	Must
160	M1	D	61	NA	Metal-1	Must

178	V1	C	70	NA	Via-1 Hole	Must
180	M2	D	62	NA	Metal-2	Must
179	V2	C	71	NA	Via-2 Hole	Must
181	M3	D	63	NA	Metal-3	Must
162	MIM	D	58	NA	Top Plate of MIM Capacitor	Optional
177	V3	C	72	NA	Via-3 Hole	Must
182	M4	D	64	NA	Metal-4	Must
176	V4	C	73	NA	Via-4 Hole	Optional
183	M5	D	65	NA	Metal-5	Optional
175	V5	C	74	NA	Via-5 Hole	Optional
184	M6	D	66	NA	Metal-6	Optional
107	PA	C	80	NA	Passivation / Pad	Must
106	FUSE	C	209	NA	Fuse Window	Optional
009	PI	D	82	NA	Polymide (Negative Resistor)	Optional
	AADUM		10;1	NA	AA Dummy Layer(For dummy AA insertion)	
	TPW		16	NA	Tripple Well	
	HVPF		98	NA	HV NCH Field	
	PSUB		85	NA	Psub area	
	BITCEL		93	NA	Dummy Layer for DRC/LVS purpose: Define EEArray BitCell	
	PWI		81	NA	VT IMP in PW	

Special Notice:
1.   SN should be drawing layer!!!
2.   NLL/PLL can be drawn by customer or by logic operation generated

7.4   DEVICE TABLE
The device table below defines the drawn layers used for specific device layout.
   7.4.1   Layout examples are described in Chapter 7.14 "Device Layout Examples"

7.4.2   User is RECOMMENDED to inform SMIC if other special device design is adopted.

Table.1: Transistors

0.18e-EEPROM Device Table & Layout Drawn Layer Description

Layer Name	Layer GDS#	Described in DRs ?	Description	1.8v CORE 1.8v nMOS	1.8v CORE 1.8v pMOS	1.8v Native Device	3.3v (Special) 3.3v nMOS	3.3v (Special) 3.3v pMOS	5v (Special) 5v HVNMOS	5v (Special) 5v HVZMOS	5v (Special) 5v Quasi-HVPMOS	15.5v HV 15.5v HVNMOS	15.5v HV 15.5v HVZMOS	15.5v HV 15.5v Real-HVPMOS
PSUB	85	Y	Define Psub tubes for HV n-channel devices						√	√		√	√	
DNW	19	Y	Define NW tubes for Quasi/Real HV, special 3.3v p-channel devices					√			√			√
TPW	16	Y	Define 3.3v MVPW tube for special 3.3v nMOS				√							
PWI	81	Y	Define 1.8v LV Native Device			√								
NW	14	Y	Define NW tubes for 1.8v LV p-channel devices		√									
AA	10	Y	Define device Active Area regions	√*	√	√	√	√	√	√	√	√	√	√
TIM	27	Y	Define regions that receive buried N- TIM implant											
VTNH	49	Y	Define regions that receive HV n-channel VT implant						√			√		
HVPF	98	Y	Define regions in PSUB that are blocked from HV n-channel field implant						√	√		√	√	
TOW	55	Y	Define tunnel oxide window open regions				√	√						
GT	30	Y	Define poly gate for HV N/ZMOS and Quasi/RealHVPMOS, EEPROM Select-Gate/Float Gate, and buttom-plate of PiP capacitor				√	√	√	√	√	√	√	√
ONO	56	Y	Define regions that ONO are left after ONO etch.				√	√	√	√	√	√	√	√
Poly2(CG)	57	Y	Define EEPROM Array control gate and top-plate of PiP capacitor											
Poly2(GP)	83	Y	Define 1.8v core device poly gate, and poly resistor	√	√	√								
DDD	84	Y	Define regions that receive HV n-channel DDD implant				√		√	√		√	√	
NLL	35	Y	Define regions that receive 1.8v LV n-channel LDD implant	√		√								
PLL	38	Y	Define regions that receive 1.8v LV p-channel LDD implant		√									
ESD1	41	Y	Define regions that receive P-ESD implant **(optional)**											
SN	40	Y	Define regions that receive S/D N+ implant	√		√	√		√	√		√	√	
SP	43	Y	Define regions that receive S/D P+ implant		√			√			√			Partial
SAB	48	Y	Define regions that are blocked from salicidation											Partial
RESDMY	90	Y	DRC/LVS auxiliary layer, define resistors other than 0.18 logic parts											
RLHVP	91	Y	DRC/LVS auxiliary layer, define 16v Real-HVPMOS											R
5VHVNZ	92	Y	DRC/LVS auxiliary layer, define 5V HVN/ZMOS						√	√				
BITCEL	93	Y	DRC/LVS auxiliary layer, define EEArray BitCell											
Res_NW	95	Y	DRC/LVS auxiliary layer, follow similar use of 0.18 logic process											
Res_P1	96	Y	DRC/LVS auxiliary layer, follow similar use of 0.18 logic process											
Res_AA	97	Y	DRC/LVS auxiliary layer, follow similar use of 0.18 logic process											
CAP_BP	137		DRC/LVS auxiliary layer, define PIP											
DMPNP	134	Y	DRC/LVS auxiliary layer, define 3.3v/1.8v v_BJT											

Table.2: Resistor/Capacitor/v-BJT

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0.18e-EEPROM Device Table & Layout Drawn Layer Description

Layer Name	Layer GDS#	Description	Resistor					Capacitor		BJT		Stack PIP	
			NW (on AA)	TIM (PSUB)	P+ Poly2(GP)	N+ Poly2(GP)	HRP	Tunnel Ox	PIP	1.8v	3.3v	HV GOX	TOW
PSUB	85	Define Psub tubes for HV n-channel devices		V					no limit			V	V
DNW	19	Define NW tubes for Quasi/Real HV, special 3.3v p-channel devices						V	no limit		V		
TPW	16	Define 3.3v MVPW tube for special 3.3v nMOS									V		
NW	14	Define NW tubes for 1.8v LV p-channel devices	V				V			V			
AA	10	Define device Active Area regions	V	V				V		V	V	V	V
TIM	27	Define regions that receive buried N- TIM implant		V				V				V	V
VTNH	49	Define regions that receive HV n-channel VT implant											
HVPF	98	Define regions in PSUB that are blocked from HV n-channel field implant		V								V	V
TOW	55	Define tunnel oxide window open regions						V			V		V
GT	30	Define poly gate for HV N/ZMOS and Quasi/RealHVPMOS, EEPROM Select-Gate/Float Gate, and buttom-plate of PiP capacitor		V				V	V			V	V
ONO	56	Define regions that ONO are left after ONO etch.		V				V	V		V	V	V
Poly2(CG)	57	Define EEPROM Array control gate and top-plate of PiP capacitor							V			V	V
Poly2(GP)	83	Define 1.8v core device poly gate, and poly resistor			V	V	V						
DDD	84	Define regions that receive HV n-channel DDD implant										V	V
NLL	35	Define regions that receive 1.8v LV n-channel LDD implant								V			
PLL	38	Define regions that receive 1.8v LV p-channel LDD implant								V			
ESD1	41	Define regions that receive P-ESD implant (optional)											
SN	40	Define regions that receive S/D N+ implant	Terminal	V		V	Terminal	V	V	V	V	V	V
SP	43	Define regions that receive S/D P+ implant			V					V	V		
SAB	48	Define regions that are blocked from salicidation	V		V	V	V					V	V
RESDMY	90	DRC/LVS auxiliary layer, define resistors other than 0.18 logic parts		R			V						
RLHVP	91	DRC/LVS auxiliary layer, define 16v Real-HVPMOS											
5VHVNZ	92	DRC/LVS auxiliary layer, define 5V HVN/ZMOS											
BITCEL	93	DRC/LVS auxiliary layer, define EEArray BitCell											
ResNW	95	DRC/LVS auxiliary layer, follow similar use of 0.18 logic process	R										
ResP1	96	DRC/LVS auxiliary layer, follow similar use of 0.18 logic process			R	R							
ResAA	97	DRC/LVS auxiliary layer, follow similar use of 0.18 logic process											
HRP	39	DRC/LVS auxiliary layer, follow similar use of 0.18 logic process					V						
CAPBP	137	DRC/LVS auxiliary layer, define PIP							R			V	V
DMPNP	134	DRC/LVS auxiliary layer, define 1.8/3.3v v_BJT								V	V		

Optional Device

R   **Recommend**

Notice :
1. Tunnel OX Capacitor is an optional device, its cap is 4.06e-7F/cm^2.
2. 1.8v/3.3v BJT pls follow spice model (TD-EE18-SP-2001)example
3. 3.3v BJT is 018EE device, it is not compatible with 0.18um Logic 3.3v BJT

Table.3: Resistor Table 1 in Spice

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Layer Name	Layer GDS#	Described in DRs ?	Description	Silicide N+ Diffusion (rndif)	Silicide P+ Diffusion (rpdif)	Silicide N+ Poly (rnpo)	Silicide N+Poly (three terminal) (rnpo_3t)	Silicide P+ Poly (rppo)	Silicide P+Poly (three terminal) (rppo_3t)	Silicide Nwell under AA (rnwaa)	Silicide Nwell under STI (rnwsti)	Non-Silicide N+ Diffusion (rndifsab)	Non-Silicide P+ Diffusion (rpdifsab)
PSUB	85	Y	Define Psub tubes for HV n-channel devices										
DNW	19	Y	Define NW tubes for Quasi/Real HV, special 3.3v p-channel devices										
TPW	16	Y	Define 3.3v MVPW tube for special 3.3v nMOS										
NW	14	Y	Define NW tubes for 1.8v LV p-channel devices		V			V	V	V	V		V
AA	10	Y	Define device Active Area regions	V	V					V	V	V	V
TIM	27	Y	Define regions that receive buried N- TIM implant										
VTNH	49	Y	Define regions that receive HV n-channel VT implant										
HVPF	98	Y	Define regions in PSUB that are blocked from HV n-channel field implant										
TOW	55	Y	Define tunnel oxide window open regions										
GT	30	Y	Define poly gate for HV N/ZMOS and Quasi/RealHVPMOS, EEPROM Select-Gate/Float Gate, and buttom-plate of PiP capacitor										
ONO	56	Y	Define regions that ONO are left after ONO etch.										
Poly2(CG)	57	Y	Define EEPROM Array control gate and top-plate of PiP capacitor										
Poly2(GP)	83	Y	Define 1.8v core device poly gate, and poly resistor			V	V	V	V				
DDD	84	Y	Define regions that receive HV n-channel DDD implant										
NLL	35	Y	Define regions that receive 1.8v LV n-channel LDD implant										
PLL	38	Y	Define regions that receive 1.8v LV p-channel LDD implant										
HRP	39	Y	Define High Poly Resitor										
ESD1	41	Y	Define regions that receive P-ESD implant **(optional)**										
SN	40	Y	Define regions that receive S/D N+ implant	V		V	V			partial	V	V	
SP	43	Y	Define regions that receive S/D P+ implant		V			V	V				V
SAB	48	Y	Define regions that are blocked from salicidation							V		V	V
RESDMY	90	Y	DRC/LVS auxiliary layer, define resistors other than 0.18 logic parts										
RLHVP	91	Y	DRC/LVS auxiliary layer, define 16v Real-HVPMOS										
5VHVNZ	92	Y	DRC/LVS auxiliary layer, define 5V HVN/ZMOS										
BITCEL	93	Y	DRC/LVS auxiliary layer, define EEArray BitCell										
ResNW	95	Y	DRC/LVS auxiliary layer, follow similar use of 0.18 logic process							V	V		
ResP1	96	Y	DRC/LVS auxiliary layer, follow similar use of 0.18 logic process			V	V	V	V				
ResAA	97	Y	DRC/LVS auxiliary layer, follow similar use of 0.18 logic process	V	V							V	V
CAPBP	137		DRC/LVS auxiliary layer, define PIP										
DMPNP	134	Y	DRC/LVS auxiliary layer, define 1.8/3.3v v_BJT										
DSTR	138		LVS layer to recognize resistor										

Table.4: Resistor Table 2 in Spice

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Layer Name	Layer GDS#	Described in DRs ?	Description	Non-Silicide N+ Poly	N+ Poly (three terminal)	Non-Silicide P+ Poly	Non-Silicide P+Poly (three terminal)	High Resistance Poly	High Resistance Poly (three terminal)	TIM
				rnposab	rnposab_3t	rpposab	rpposab_3t	rhrpo	rhrpo_3t	rtimsab
PSUB	85	Y	Define Psub tubes for HV n-channel devices							V
DNW	19	Y	Define NW tubes for Quasi/Real HV, special 3.3v p-channel devices							
TPW	16	Y	Define 3.3v MVPW tube for special 3.3v nMOS							
NW	14	Y	Define NW tubes for 1.8v LV p-channel devices			V	V			
AA	10	Y	Define device Active Area regions							V
TIM	27	Y	Define regions that receive buried N- TIM implant							V
VTNH	49	Y	Define regions that receive HV n-channel VT implant							
HVPF	98	Y	Define regions in PSUB that are blocked from HV n-channel field implant							
TOW	55	Y	Define tunnel oxide window open regions							
GT	30	Y	Define poly gate for HV N/ZMOS and Quasi/RealHVPMOS, EEPROM Select-Gate/Float Gate, and buttom-plate of PiP capacitor							V
ONO	56	Y	Define regions that ONO are left after ONO etch.							V
Poly2(CG)	57	Y	Define EEPROM Array control gate and top-plate of PiP capacitor							
Poly2(GP)	83	Y	Define 1.8v core device poly gate, and poly resistor	V	V			V	V	
DDD	84	Y	Define regions that receive HV n-channel DDD implant							
NLL	35	Y	Define regions that receive 1.8v LV n-channel LDD implant							
PLL	38	Y	Define regions that receive 1.8v LV p-channel LDD implant							
HRP	39	Y	Define High Poly Resitor					V	V	
ESD1	41	Y	Define regions that receive P-ESD implant **(optional)**							
SN	40	Y	Define regions that receive S/D N+ implant	V	V			V	V	V
SP	43	Y	Define regions that receive S/D P+ implant			V	V			
SAB	48	Y	Define regions that are blocked from salicidation	V	V	V	V	V	V	
RESDMY	90	Y	DRC/LVS auxiliary layer, define resistors other than 0.18 logic parts							
HRPDMY	210	Y	HRP dummy layer					V	V	
RLHVP	91	Y	DRC/LVS auxiliary layer, define 16v Real-HVPMOS							
5VHVNZ	92	Y	DRC/LVS auxiliary layer, define 5V HVN/ZMOS							
BITCEL	93	Y	DRC/LVS auxiliary layer, define EEArray BitCell							
ResNW	95	Y	DRC/LVS auxiliary layer, follow similar use of 0.18 logic process							
ResP1	96	Y	DRC/LVS auxiliary layer, follow similar use of 0.18 logic process	V	V	V	V			
ResAA	97	Y	DRC/LVS auxiliary layer, follow similar use of 0.18 logic process							
CAPBP	137		DRC/LVS auxiliary layer, define PIP							
DMPNP	134	Y	DRC/LVS auxiliary layer, define 1.8/3.3v v_BJT							

7.4.3   Below Table describes 0.18eEEPROM basic device performance and applications.

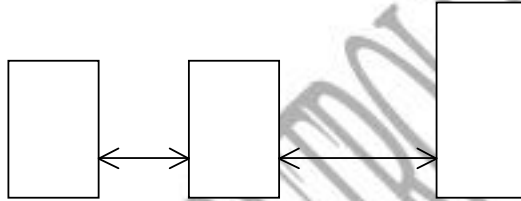## Semiconductor Manufacturing International Corporation

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Users are RECOMMENDED to refer to PCM spec & SPICE Model for more detailed information.

7.4.3.1   1.8v Core   : Fully compatible to 1.8v devices of SMIC 0.18um generic logic process.
         Applications   : 1.8v e-CPU, e-SRAM, e-ROM, PLL & other 0.18um generic logic, 1.8v IP/Libraries.
         (Note1 : 1.8v device character is same, but the poly gate GDS is different, for 0.18um Logic it is 30, for 0.18um EERPOM, it is 83.Pls note when use 18um Logic library in 18um EEPROM)
         (Note2 : 1.8v NMOS has two type, one is standard 1.8v NMOS, the other one is isolated by HVBN 1.8v NMOS)

7.4.3.2   3.3v MV   : Special 3.3v devices. Oxide thickness same as tunnel oxide.
         Applications   : 3.3v I/Os, USB1.1 transceiver…

7.4.3.3   5v HV   : Special 5v devices. Oxide thickness same as HV oxide.
         Applications   : 5v I/Os, voltage regulator…

7.4.3.4   16 HV   : 15.5v HVN/ZMOS, 16v HVPMOS.
         Applications   : e-EEPROM operation related HV circuitry.

7.4.3.5   TIM resistor   : Buried As-implanted n-type diffusion resistor.
         Applications   : Resistors for analog design.

7.4.3.6   Poly resistor   : Non-salicided n-type or p-type poly resistor.
         Applications   : Resistors for analog design.

7.4.3.7   MIM   : Fully compatible to MIM of SMIC 0.18um generic logic process
         Applications   : Capacitor for analog/RF design.

7.4.3.8   HRP   : Fully compatible to HRP of SMIC 0.18um generic logic process
         Applications   : High Resistance Poly for design.

7.4.3.9   BJT   : 1.8v/3.3v BJT
         Applications   : BJT device.

7.4.3.10   Native Device   : 1.8v Native Device
         Applications   : 1.8v Native Device

7.4.3.11   PIP Capcitor   : 5.0v PIP capacitor
         Applications   : 5.0v PIP capacitor

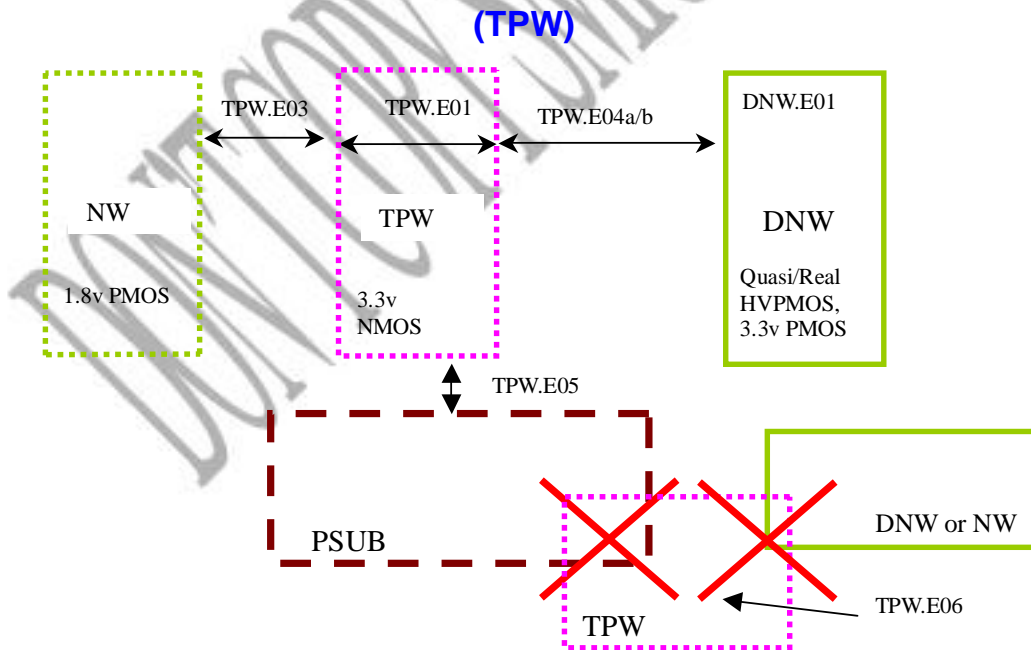Semiconductor Manufacturing International Corporation

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0.18 e-EEPROM Device Spec (@ 25C)

Tech Feature	CORE		I/O (3.3v MV)		I/O (HV Device)			HV-nMOS		HV-pMOS
1.8v/16v	V	V	V	V	V	V	V	V	V	V
	CORE (std 1.8v)		I/O (special 3.3v)		I/O (special 5v)			HV-nMOS		HV-pMOS
	n	p	n	p	n	n	p	n	n	p
Voperation (V)	1.8v	1.8v	3.3v	3.3v	5V	5V	5V	15.5V	15.5V	16V
Device-Type	nMOS	pMOS	80A MV	80A MV	HVN	HVZ	Quasi-HVP	HVN	HVZ	Real-HVP
Salicide(SA)	SA	SA	SA	SA	SA	SA	SA	SA	SA	CT-SA
GOX(A, as-dep)	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
GOX(A, acc)	42.0	44.0	80.0	89.0	263.0	263.0	270.0	263.0	270.0	270.0
Lpoly(um, drawn)	0.18	0.18	0.60	0.80	1.40	1.80	1.00	1.70	2.10	1.00
Vt.gm (V)	0.42	-0.50	0.78	-0.84	0.75	0.30	-0.80	0.75	0.30	-0.80
Ids@ Vcc (uA/um) @Vcc	600	-260	380 (3.3v)	155 (3.3v)	245 (5v)	250 (5v)	140 (5v)	210 (5v)	235 (5v)	115 (5v)
Ioff (norm) @ 1.1Vcc (pA/um)	<30	<30	<10	<10	<10	<10	<10	<10	--	<10
Ioff (max) @ 1.1Vcc (pA/um)			<100	<100	<100	<1000	<100	<100	--	<100
BV @ 0.1uA/um (V)	>3.6	<-3.6	>8	< -8	>8	>7	<-8	>15.5	>10	< -16
AA width (um) DR	0.22	0.22	0.60	0.60	0.60	0.60	0.60	0.60	0.60	1.62
AA-AA Space(um) DR	0.28	0.28	0.40	0.40	0.80	0.90	0.50	1.05	1.05	0.80

PiP Capacitor	Toxeff (A)	Cap (fF/um^2)	Max Vapp (V)	VC1 (ppm /V)	VC2 (ppm /V^2)	TC1 (ppm /C)	
PIP (ONO)	155	2.23	<5V	--	--	--	$C=C(V=0V) * (1+VC1*V+VC2*V^2)$ $C=C(T=25C)* (1+TC1* (T-25))$
MiM	345	1	<20V	-34.11	-14.89	-34.82	$C=C(V=0V) * (1+VC1*V+VC2*V^2)$ $C=C(T=25C)* (1+TC1* (T-25))$

EECell		VD	VSG	VCG	VS	VB	Note
UV-VT	0.2v						VT=Vcg@0.1uA, Vd/Vsg/Vb/Vs=1.5/3.3/0/0v
PG-VT	-0.65v	13.5	16	0	F	0	1ms pulse, VT@0.1uA, Vd/Vsg=1.5/3.3v
ER-VT	3.2v	0	16	15	0	0	1ms pulse, VT@0.1uA, Vd/Vsg=1.5/3.3v
IDSC-PG	32 uA	1.5	3.3	1.8	0	0	Vcg=1.8v 6
IDSC-ER	<100pA	1.5	3.3	1.8	0	0	

Electrical data only reference for design, spice model provide the accurate data

Notice :

Cell operation : TD-EE18-CL-2005 0.18um e-EEPROM 2P4M (5M/6M) Salicide 1.8V/3.3V/5.0V/15.5V Cell Operation Condition Rule

7.5 LAYOUT RULES DEFINITION

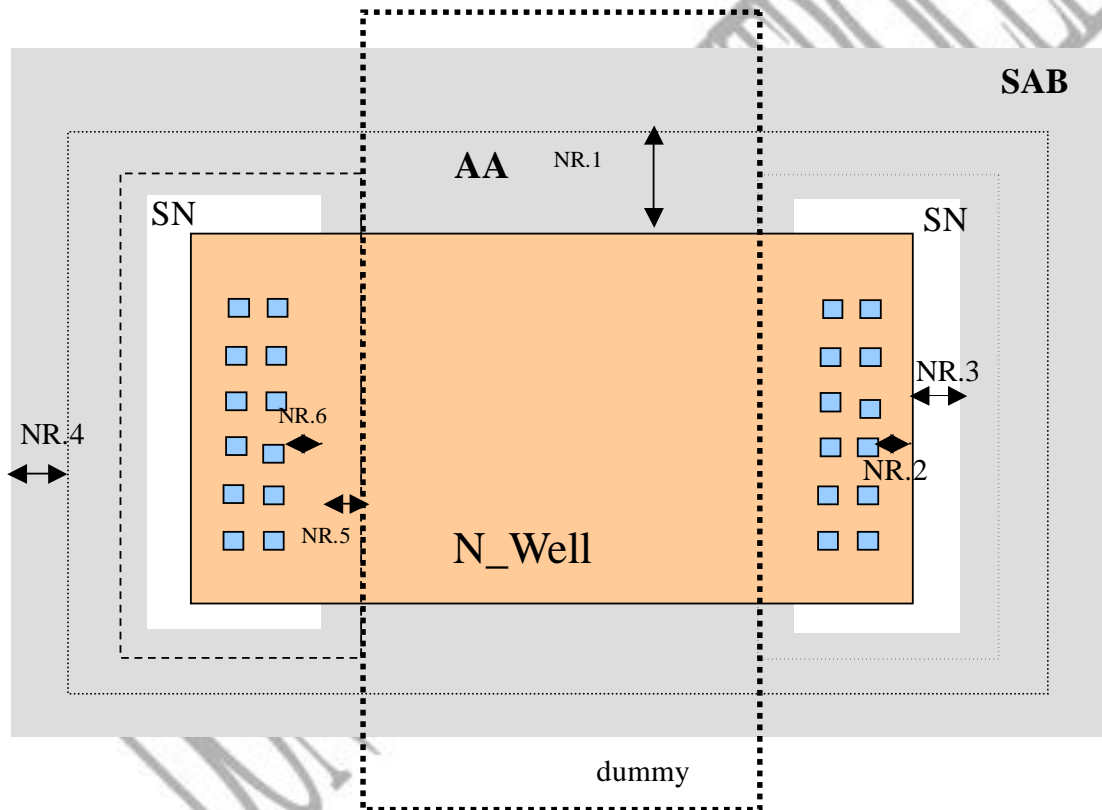Semiconductor Manufacturing International Corporation

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WIDTH

SPACE

ENCLOSURE

EXTENSION

OVERLAP

7.6   DESIGN RULE DESCRIPTIONS

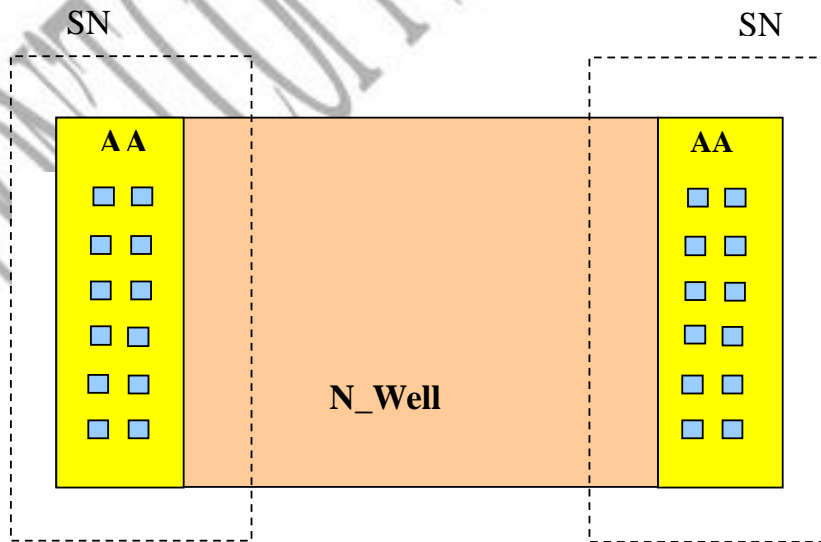## Semiconductor Manufacturing International Corporation

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a. All the design rules described here are for "Layout Drawn Layers".
b. Those design rules numbered with xxxx.xx comply to SMIC 0.18um Generic Logic Process layout Design Rules.
c. Those design rules numbered with xxxx.Exx are specific for SMIC 0.18um e-EEPROM process.

7.6.0   Design Geometry Rules

RULE NO.	DESCRIPTION
GRID	The design grid must be an integer multiple of 0.005μm.
OFFGRID	All edge boundaries must be snapped to the grid defined above.
ACUTE	All shapes must be orthogonal or on a 45° unless otherwise stated.

7.6.1   PSUB (18EE)

The (PSUB) layout layer is drawn to define PSUB tubes for HV N/ZMOS (5v/15.5v) and EEPROM arrays.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**PSUB**	
PSUB.E01	Minimum PSUB width	1.0
PSUB.E02	Minimum space for PSUB to PSUB	1.0

(PSUB)

7.6.2   DNW (18EE)

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The (DNW) layout layer is drawn to define NW tubes for 5/16v Quasi/Real-HVPMOS, and special 3.3v MV PMOS.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**DNW**	
DNW.E01	Minimum width of an DNW region	2.2
DNW.E02	Minimum space between DNW (different potential)	6.0
DNW.E03	Minimum space between DNW (same potential)	2 or 0
DNW.E04	Minimum space between DNW to NW	5.0
DNW.E05	Minimum space between DNW to PSUB	2.5
DNW.E06	DNW overlap of PSUB or TPW is forbidden	
DNW.E07	For DRC/LVS purpose, it's RECOMMENDED to draw RLHVP (#91) on DNW which will operate at >10v as Real-HVPMOS.	
DNW.E08	For DNW operating at >10v, a PW guarding MUST be added at DNW boundary, in which no 1) AA 2)GT is allowed. Any AA/GT on the PW MUST be put outside the PW guard-ring. Min. PW guard ring width	1.20

(DNW)

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7.6.3 TPW (18EE)

The (TPW) layout layer is drawn to define MV-PW tubes for special 3.3v MV NMOS.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**TPW**	
TPW.E01	Minimum width of an TPW region	1.0
TPW.E02	Minimum space between TPW	1.0
TPW.E03	Minimum space between TPW to NW	0.78
TPW.E04	Minimum space between TPW to DNW	
	TPW.E04a DNW Vop>10v, Real-HVPMOS	1.20
	TPW.E04b DNW Vop<10v, 3.3v or 5v devices	0.78
TPW.E05	Minimum space between TPW to PSUB	0 or 1.0
TPW.E06	TPW overlap of PSUB or DNW or NW is forbidden	

(TPW)

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7.6.4 NW

The (NW) layout layer is drawn to define NW tubes for 1.8v core LVPMOS.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**NW**	
NW.01	Minimum width of an NW region	0.86
NW.02a	Minimum space between two NW regions (equi-potential wells) Merge if space is less than 0.6μm	0.60
NW.02b	Minimum space between two NW (different potential wells)	1.40
NW.03	Minimum width of a hot NW region, which is not connect to Vdd. Put NW resistor within AA region to minimize the influence of process variation on NW resistance	2.10
NW.E01	Minimum space between NW to DNW	5.0
NW.E02	Minimum space between NW to PSUB	1.5
NW.E03	NW overlap of DNW is forbidden	
NW.E04	NW overlap of PSUB is forbidden	
NW.E05	NW overlap of TPW is forbidden	
NW.E06	PW (for DRC/LVS) region is defined by " Not { (NW) or (DNW) or (PSUB) or (TPW) or (PWI)} "	

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(NW)

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Notices: N-Well resistor usage
The mean value and deviation of N-well resistor depend on the layout and dimension. If the designer requires tight control of Rsh deviation, the features of having NW within AA (refer to Fig. 1) is recommended. If the design is not sensitive to the deviation, Fig. 2 will be another option.

Fig 1 NW within AA
- Add SAB to prevent salicide formed in the NW resistance region.
- Dummy layer is needed to avoid N+/P+ implanting into NW resistance region.

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RULE NO.	DESCRIPTION	LAYOUT RULE (Unit in μm)
NR.01	Minimum extension of AA to NW	1.00
NR.02	Minimum extension of salicide NW to CT	0.30
NR.03	Minimum space from SAB to related NW	0.30
NR.04	Minimum space from SAB to related AA	0.22
NR.05	Minimum overlap of SAB to SN inside NW	0.40
NR.06	Minimum space from SAB to CT in SAB hole	0.30
NR.07	Minimum NW space	1.40
NR.08	LDD, SN and SP implant inside NW resistance region is not allowed	

Fig 2 NW under STI
- Rs_NW is varied with STI thickness under normal process variation

Note: Minimum NW resistor space is 1.40um (NR.7), otherwise the space less than 1.40um will cause decreased & un-stale resistance due to poor NW-NW isolation.

Notice:
1. Hot NW: NW not connected to the most positive power supply (VDD).
2. Cold NW: NW connected to the most positive power supply (VDD).
3. To distinguish hot NW and cold NW in DRC, a VDD text label is needed to tag on cold NW net, using the metal layer on the top level. For example:

Two NW connected to VDD with M1, with text "VDD" using M1.

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7.6.5   AA

The (AA) layout layer is drawn to define drawn to define the Active Area regions.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**AA**	
	Below design rules apply to AA outside DNW, PSUB and TPW. That is, inside NW or PW.	
AA.01	Minimum width of an active region for interconnect (N+/P+)	0.22
AA.02	Minimum width of an active region to define the width of NMOS/PMOS	0.22
AA.03	Minimum space between N+ AA and N+ AA or P+ AA and P+ AA (both regions are either inside or outside NW)	0.28
AA.04	Minimum enclosure from NW edge to an N-well pick-up	0.12
AA.05	Minimum space between N-Well edge and an N+AA region which is inside an NW	0.43
AA.06	Minimum space between N-Well edge and a P+AA region which is inside an NW	0.43
AA.07	Minimum space between N-Well edge and a P+AA region (for PW pick-up) outside an NW	0.12
AA.08	Minimum space between poly edge and edge of a butted diffusion AA region	0.32
AA.09	Minimum space between N+AA and P+ AA for butted diffusion	0.00
AA.10	Minimum area of a butted diffusion AA is $0.176\mu m^2$. At least one segment (AA.10) of the consecutive SN/SP edge of butted diffusion AA should be longer than $0.42\mu m$.	0.42
AA.11	Minimum area of a stand-along AA region	0.20
AA.12	For the situation where N-well and P-well pick-ups are put head-to-head across the well boundary, the space between N-pick-up and P-pick-up should be $0.36\mu m$ in order to meet the implant layout rules.	

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Below design rules apply to AA inside DNW or PSUB or TPW
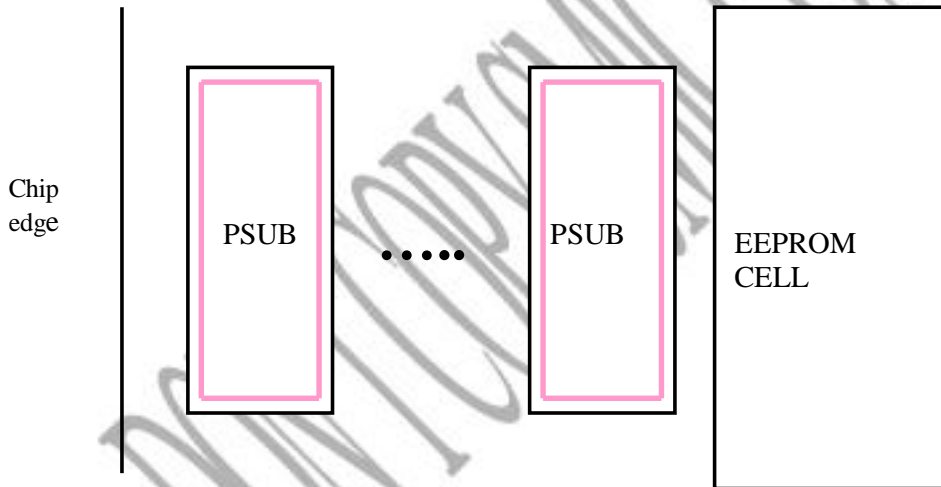
AA.E01	Minimum AA width for		
	AA.E01a	interconnect (N+ or P+)	0.6
	AA.E01b	TIM resistor	0.6
	AA.E01c	5v/15.5v HVN/ZMOS, 5v Quasi-HVPMOS	0.6
	AA.E01d	3.3v MV N/PMOS	0.6
	AA.E01e	16v Real-HVPMOS	1.62
AA.E02	Minimum space between two N+AA space (both inside PSUB)		
	AA.E02a	5v HVN/ZMOS	0.9
	AA.E02b	15.5v HVN/ZMOS	1.05
AA.E03	Minimum space between N+AA to (P+AA pick-up), both inside PSUB		
	AA.E3a	<=6v N+AA	0.50
	AA.E3b	> 6v N+AA	1.0
	AA.E3c.	Butted Diffusion	0
AA.E04	Minimum enclosure from PSUB edge to (N+AA inside PSUB)		2.8
AA.E05	Minimum enclosure from PSUB edge to (P+AA pick-up inside PSUB)		1.0
AA.E06	Minimum space between PSUB edge to (N+AA outside PSUB, NW, DNW)		0.5
AA.E07	Minimum space between PSUB edge to (P+AA outside PSUB, NW, DNW)		0.4
AA.E08	Minimum space between two P+AA, both inside DNW		
	AA.E08a	3.3v MV PMOS	0.4
	AA.E08b	5v Quasi-HVPMOS, or <=10v voltage difference	0.5
	AA.E08c	16v Real-HVPMOS, or >10v voltage difference	0.8
AA.E09	Minimum space between P+AA to (N+AA pick-up), both inside DNW		
	AA.E09a	Non-Butted	1.5

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	AA.E09b Butted	0
AA.E10	Minimum enclosure from DNW edge to (P+AA inside DNW)	
	AA.E10a 3.3v MV PMOS, 5v Quasi-HVPMOS	0.80
	AA.E10b 16v Real-HVPMOS	3.30[*]
AA.E11	Minimum enclosure from DNW edge to (N+AA pick-up inside DNW)	1.2
AA.E12	Minimum space between DNW edge to (N+AA outside PSUB, NW, DNW)	1.2
AA.E13	Minimum space between DNW edge to (P+AA outside PSUB, NW, DNW)	1.18
AA.E14	Minimum space between two N+AA space (both inside TPW)	0.4
AA.E15	Minimum space between N+AA to (P+AA pick-up), both inside TPW	
	AA.E15a Non-Butted	0.4
	AA.E15b Butted	0
AA.E16	Minimum enclosure from TPW edge to (N+AA inside TPW)	0.8
AA.E17	Minimum enclosure from TPW edge to (P+AA pick-up inside TPW)	0.4
AA.E18	Cross-over of AA to PSUB is NOT allowed. AA must be fully inside, or outside PSUB	
AA.E19	Cross-over of AA to DNW is NOT allowed. AA must be fully inside, or outside DNW	
AA.E20	Cross-over of AA to TPW is NOT allowed. AA must be fully inside, or outside TPW	

Notice : For 16v Real_HVPMOS, it should be surrounded by N+AA as guarding for the rule AA.E10b of P+ inside DNW to DNW

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(AA)

Butted diffusion

(AA) outside DNW,PSUB,TPW

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(AA)

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Some suggestion guidelines for decoder Well/Tube arrangement

7.6.5.1 All HV MOS devices are suggested to use pickup AA guard ring to acquire good isolation and reliability.

N+ pickup guard ring

P+ pickup guard ring

DNW

PSUB

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7.6.5.2 HVNW , MVNW , LVNW arrangement (suggested)

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7.6.5.3　HV device well arrangement example(suggested)

1. .DNW in the middle of two PSUB

2. DNW and PSUB are neighbor　for each other

3. A p+ pick up is suggested to added between DNW and PSUB

PSUB　DNW　PSUB　DNW

Chip edge

PSUB　• • • • •　PSUB　EEPROM CELL

4. The WELL near the Chip edge or EE Cell edge had better be　PSUB

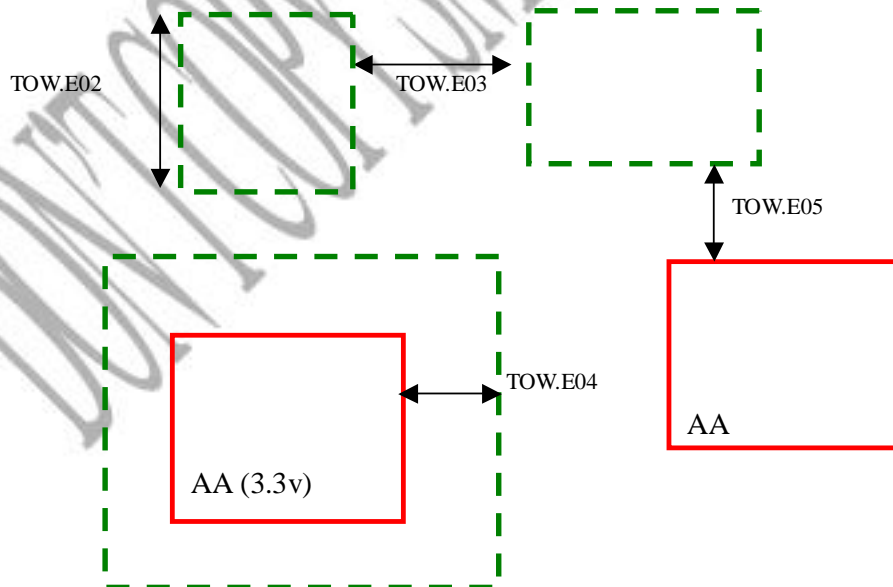![SMIC logo] Semiconductor Manufacturing International Corporation

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7.6.6 TIM (18EE)

The (TIM) layout layer is drawn to define EEPROM cell float-gate transistor length, and NCODE MaskROM N- depletion CODE implant.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**TIM**	
	Below design rules apply to TIM outside EEArrays[Note1]	
TIM.E01	Minimum TIM width	0.45
TIM.E02	Minimum TIM to TIM space	0.45
TIM.E03	Minimum TIM enclosure related AA	0.3
TIM.E04	Minimum TIM space to unrelated AA	0.3
	Below deign rules apply to TIM for NCODE ROM N- depletion Code implant	
TIM.E05	Minimum TIM to TIM space	merge if <0.45
TIM.E06	Minimum TIM extension AA (NCODE)	0.10
TIM.E07	Minimum TIM extension related GP (NCODE)	0.12
TIM.E08	Minimum TIM space to unrelated GP (NCODE)	0.25
TIM.E09	Minimum TIM space to unrelated AA (NCODE)	0.20
Note.1	TIM inside EEPROM bitcell is blocked from DRC with DRC auxiliary layer RP93 and described in details on 7.7 "DRC AUXILIARY LAYERS"	

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(TIM)

NCODE CELL

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7.6.7 HVPF (18EE)

The (HVPF) layout layer is drawn to block AA inside PSUB from HV-N channel stop (Field) implant.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**HVPF**	
	Below design rules apply to HVPF outside EEArrays[Note1]	
PF.E01	HVPF is only drawn inside PSUB	
PF.E02	AAs overlap of HVPF is regarded as the same potential. Any two AAs with different potential must be covered by HVPF SEPARATELY. Any HVPF-HVPF overlap or spacing< PF.E07 is NOT allowed.	
PF.E03	All N+AA must be covered by HVPF separately.	
PF.E06	Minimum/Maximum HVPF enclosure of AA inside PSUB	
	PF.E06a 5v HVN/ZMOS	=0.150
	PF.E06b 15.5v HVN/ZMOS	=0.225
PF.E07	Minimum HVPF to HVPF space	0.60
PF.E08	Minimum HVPF width	0.60
PF.E09	Inside EEArray, N+AA for VSS is allowed NOT covered by HVPF.	
Note.1	HVPF inside EEPROM bitcell is blocked from DRC with DRC auxiliary layer RP93 and described in details on 7.7 "DRC AUXILIARY LAYERS"	

(HVPF)

HVPF inside PSUB

7.6.8   VTNH (18EE)

The (VTNH) layout layer is drawn to define VT adjust implant for HVNMOS and EEPROM Array.

RULE NO.   DESCRIPTION   LAYOUT RULE

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Layer   **VTNH**

Below design rules apply to VTNH outside EEArrays[Note1]

VTN.E01   Minimum VTNH width   0.45

VTN.E02   Minimum VTNH to VTNH space.   0.45

VTN.E03   Minimum VTNH enclosure to related AA   0.30

VTN.E04   Minimum VTNH space to unrelated AA   0.30

VTN.E05   Minimum VTNH extension related P1 (GT) on AA   0.30

VTN.E06   Minimum VTNH space to unrelated P1 (GT) on AA   0.30

Note.1   VTNH inside EEPROM bitcell is blocked from DRC with DRC auxiliary layer RP93 and described in details on 7.7 "DRC AUXILIARY LAYERS"

(VTNH)

7.6.9 TOW (18EE)

The (TOW) layout layer is drawn to define EEPROM tunnel window opens and special 3.3v MVN/PMOS.

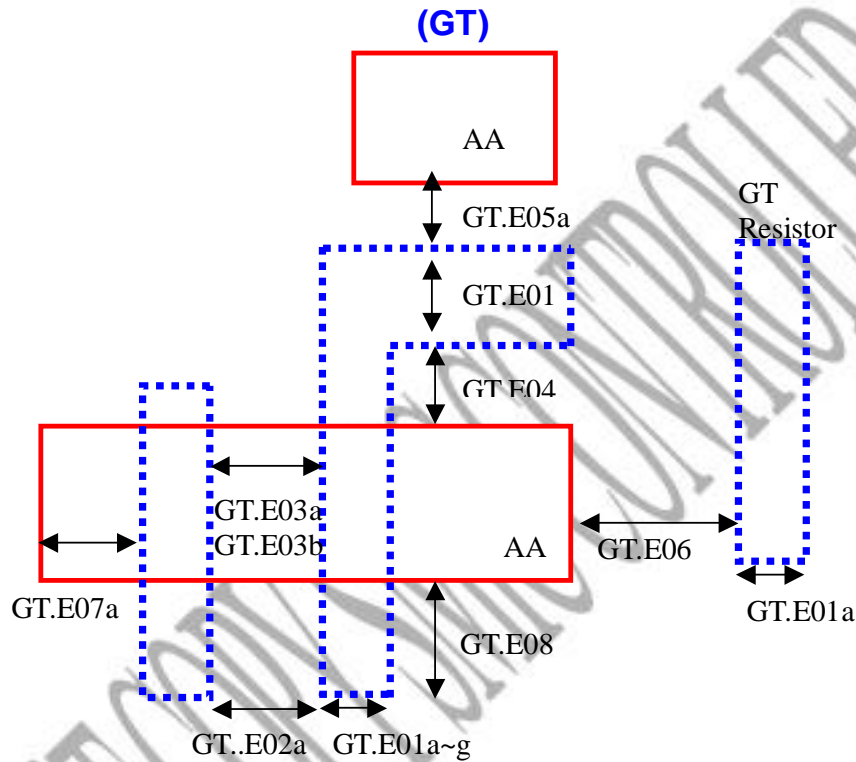**Semiconductor Manufacturing International Corporation**

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RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**TOW**	
	Below design rules apply to TOW outside EEArrays[Note1] , that is, special 3.3v MV N/PMOS.	
TOW.E01	TOW MUST cover AA of special 3.3v MV N/PMOS	
TOW.E02	Minimum TOW width	0.50
TOW.E03	Minimum TOW-to-TOW space.	Merge if <0.60
TOW.E04	Minimum TOW enclosure of related AA	0.30
TOW.E05	Minimum TOW space to un-related AA	0.30

Note.1   TOW inside EEPROM bitcell is blocked from DRC with DRC auxiliary layer RP93 and described in details on 7.7 "DRC AUXILIARY LAYERS"

(TOW)

7.6.10 Poly1-GT (18EE)

The Poly1-(GT) layout layer is drawn to define Poly1 Gate of HVN/ZMOS, HVPMOS (Real/Quasi),

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3.3v MV N/PMOS, PiP capacitor bottom-plate and EEPROM cell Select-Gate and Float-Gate.

RULE NO.	DESCRIPTION		LAYOUT RULE
Layer	**GT**		
	Below design rules apply to GT outside EEArrays[Note1]		
GT.E01	Minimum width of GT		
	GT.E01a	Interconnect/Resistor purpose	0.60
	GT.E01b	15.5v HVNMOS (inside PSUB)	1.7
	GT.E01c	15.5v HVZMOS (inside PSUB)	2.1
	GT.E01d	16v Real HV PMOS (inside DNW)	1.0
	GT.E01e	5v HV NMOS (inside PSUB)	1.4
	GT.E01f	5v HVZMOS (inside PSUB)	1.8
	GT.E01g	5v Quasi-HV PMOS (inside DNW)	1.0
	GT.E01h	3.3v MV NMOS (inside TPW)	0.60
	GT.E01i	3.3v MV PMOS (inside DNW)	0.80
GT.E02a	Minimum space of GT to GT on FOX		0.40
GT.E02b	For 16v Real-HVPMOS, GT cross over AAs of different potential is NOT allowed. (field isolation) [Note.2]		
GT.E03	Minimum space of GT to GT on AA		
	GT.E03a	outside DNW	0.40
	GT.E03b	inside DNW, not 16v Real-HVPMOS	0.40
	GT.E03c	inside DNW, Real-HVPMOS (with CT between)	1.92
	GT.E03d	inside DNW, Real-HVPMOS (without CT between)	1.54
GT.E04	Minimum space of GT on FOX to related AA edge.		0.20
GT.E05	Minimum space of GT on FOX to un-related AA edge		
	GT.E05a	Except 16v Real-HVPMOS	0.20
	GT.E05b	16v Real-HVPMOS	0.45

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GT.E06	Minimum space of GT on FOX to un-related AA edge (Resistor purpose)	0.45
GT.E07	Minimum space of GT on AA to related AA edge.	
	GT.E07a Except 16v Real-HVPMOS	0.40
	GT.E07b 16v Real-HVPMOS (with CT between)	1.77
	GT.E07c 16v Real-HVPMOS (without CT between.)	1.39
GT.E08	Minimum extension of GT to related AA edge (end-cap)	0.35

Note.1   GT inside EEPROM bitcell is blocked from DRC with DRC auxiliary layer RP93 and described in details on 7.7 "DRC AUXILIARY LAYERS"

Note.2   Interconnect at 16v HV level inside DNW should be routed in metal whenever possible

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(GT)

AA

GT.E05a

GT.E01

GT.E04

GT Resistor

GT.E03a
GT.E03b

AA

GT.E06

GT.E07a

GT.E01a

GT.E08

GT..E02a

GT.E01a~g

GT.E02

Vpp=16v

Note.2

GT.E07

GT.E07

GT.E03

GT.E03

GT.E02b

Real-HVP

Real-HVP

GT.E05b

Real-HVP

W

different potential

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7.6.11 ONO (18EE)

The (ONO) layout layer is drawn to define the regions that remain ONO dielectric layer after ONO etch. (ONO) must cover all GT and AA of 5v/16v HVN/ZMOS, HVPMOS (Real/Quasi), 3.3v special MV N/PMOS and EEPROM arrays. (ONO) covering entire (PSUB), (DNW), and (TPW) is recommended.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**ONO**	
ONO.E01	Minimum width of ONO	0.60
ONO.E02	Minimum space between ONO and ONO	0.60
ONO.E03	Minimum ONO enclosure of AA	0.60
ONO.E04	Minimum space for ONO to unrelated AA.	0.60
ONO.E05	Minimum ONO enclosure of P1 (GT).	0.60
ONO.E06	Minimum ONO enclosure P2 (CG)	0.60
ONO.E07	Minimum space for ONO to P2 (GP) outside ONO.	0.60
ONO.E08	All Poly1 (GT) must be inside ONO.	
ONO.E09	All Poly2 (CG) must be inside ONO, cross-over is forbidden	
ONO.E10	All Poly2 (GP) must be outside ONO, cross-over is forbidden	
ONO.E11	All AAs must be either inside or outside ONO, cross-over is forbidden.	

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(ONO)

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7.6.12 CG (18EE)

The Poly2-(CG) layout layer is drawn to define EEPROM cell Control-Gate and PIP capacitor top -plate.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**CG**	
	Below design rules apply to Poly2-(CG) outside EEArrays[Note1]	
CG.E01	CG outside ONO is not allowed	
CG.E02	Minimum width of CG	0.50
CG.E03	Minimum width of CG for Resistor purpose	0.70
CG.E04	Minimum space of CG to CG	
	CG.E04a on AA	0.40
	CG.E04b on FOX	0.40
CG.E05	Minimum space of POLY2 (CG) to POLY1 (GT)	
	CG.E05a Non-overlap case.	0.30
	CG.E05b Overlap, CG to GT space when CG inside GT (PiP)	0.35
	CG.E05c Overlap, CG to GT space when GT inside CG.	0.35
	CG.E05d Outside EEArrays, overlap of CG and GT must be cover by SAB	
CG.E06	Minimum space of POLY2 (CG) on FOX to related AA	0.20
CG.E07	Minimum space of POLY2 (CG) on FOX to unrelated AA	0.20
CG.E08	Minimum space of POLY2 (CG) on AA to related AA edge.	0.40
CG.E09	Minimum extension of POLY2 (CG) to AA (end-cap)	0.40
CG.E10	SP overlap of POLY2 (CG) Resistor is not allowed	
CG.E11	POLY2 (CG) resistor length is defined as POLY2 (CG) length crossed by SAB	
CG.E12	POLY1 (GT)/ONO/POLY2 (CG) Capacitor is allowed	

Note.1   CG inside EEPROM bitcell is blocked from DRC with DRC
auxiliary layer RP93 and described in details on 7.7 "DRC
AUXILIARY LAYERS"

(CG)

7.6.13 GP

The (GP) layout layer is drawn to define Poly2 Gate-Poly of 1.8v N/PMOS.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**GP**	
GP.01	Minimum width of a GP region for interconnects.	0.18
GP.02	Minimum width of a GP region for channel length of 1.8V PMOS / NMOS.	0.18
GP.03	Minimum space between two GP regions on AA with no contact.	0.25
GP.04	Minimum space between two GP regions on field oxide area.	0.25
GP.05	Extension beyond diffusion to form poly end cap	0.22
GP.06	Minimum extension from AA region to GP	0.32
GP.07	Minimum space between field interconnect poly and AA	0.10
GP.10a	Maximum length of salicide poly on STI between two contacts when poly width <=0.24um	50
GP.10b	Maximum length of salicide poly on STI between one contact and poly line end when poly width <=0.24um	50
GP.11a	90° bends on active area are not allowed	
GP.11b	GP must enter AA region perpendicularly.	
GP.13	Minimum space between two GP's with CT on active area.	0.375
GP.14	Minimum channel length of 1.8v device poly gate on AA with 45-degree	0.21
GP.E01	GP (Poly2) must be outside ONO, ONO overlap of GP is forbidden.	

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Note: Poly2-(GP) resistor design rule. (recommendation)

    a. The resistor width is larger than 2.0µm and Nsq>=5

    b. The separation from SAB to contact on poly must be equal to 0.22µm

    c. The space from an un-related SAB to a resistor poly must be >= 0.3µm

    d. The minimum separation between resistors with un-related implant region is 0.26µm

    e. The contact to pick-up poly resistor should be a single column

    f. Can not use dog-bone at the end of poly resistor for contact pick-up.

    g. PLL, NLL, are NOT allowed to overlap N+ or P+ GP resistor.

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7.6.14 DDD (18EE)

The (DDD) layout layer is drawn to define 3.3v MV NMOS, 5v/15.5v HVN/ZMOS, EEArray NLDD implant regions.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**DDD**	
	Below design rules apply to DDD outside EEArrays[Note1]	
DDD.E01	Minimum width of DDD	0.50
DDD.E02	Minimum space for DDD to DDD (merged if <0.5um)	0.50
DDD.E03	Minimum enclosure of DDD to related AA[Note2]	0.50
DDD.E04	Minimum space of DDD to unrelated AA.	0.30
DDD.E05	DDD inside DNW or NW is forbidden	
DDD.E06	AA must be either fully inside DDD, or outside DDD.	

Note.1 DDD inside EEPROM bitcell is blocked from DRC with DRC auxiliary layer RP93 and described in details on 7.7 "DRC AUXILIARY LAYERS"

Note.2 For butted diffusion regions, the DDD is allowed to cover the P+AA. But in mask-layer generation, it will use logic operation to block the P+AA from DDD implant.

(DDD)

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7.6.15 NLL

The (NLL) layout layer is drawn to define 1.8v NMOS NLDD implant regions.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**NLL**	
NLL.1	Minimum width of an NLL region	0.44
NLL.2	Minimum space between two NLL regions. Merge if the space is less than 0.44μm	0.44
NLL.3	Minimum space between an NLL region and a P+ AA region	0.26
NLL.4	Minimum space between an NLL region and a P+ pick-up AA region	0.10
NLL.5	Minimum overlay from an NLL edge to an AA	0.23
NLL.6	Minimum enclosure of an NLL region over SN active region	0.18
NLL.8	Minimum enclosure of an NLL region to an N-channel poly gate	0.32
NLL.9	Minimum area of an NLL region	0.40
NLL.10	Separation from an NLL to a butted edge of a butted diffusion P+ AA (inside P-Well)	0.00
NLL.12	Minimum enclosure of an NLL region over N-channel along the direction of poly gate	0.35
NLL.13	Minimum NLL area for a N-channel poly gate must follow NLL.8 and NLL.12	
NLL.14	NLL implant is NOT allowed in non-salicide AA/GP resistor region.	
NLL.E01	NLL inside DNW or PSUB or TPW is forbidden.	

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7.6.16 PLL

The (PLL) layout layer is drawn to define 1.8v PMOS PLDD implant regions.

RULE NO.   DESCRIPTION   LAYOUT RULE

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	Layer	**PLL**	
PLL.1		Minimum width of a PLL region	0.44
PLL.2		Minimum space between two PLL regions. Merge if the space is less than 0.44μm	0.44
PLL.3		Minimum space from a PLL region to an N+ AA region. (inside Pwell)	0.26
PLL.4		Minimum space from a PLL region to an N+ pick-up AA region.	0.10
PLL.5		Minimum enclosure from a PLL edge to an AA	0.23
PLL.6		Minimum enclosure of a PLL region beyond a SP active region	0.18
PLL.8		Minimum enclosure of a PLL region to a P-channel poly gate	0.32
PLL.9		Minimum area of a PLL region	0.40
PLL.10		Separation from a PLL to a butted edge of a butted diffusion N+ AA (inside N-Well)	0.00
PLL.12		Minimum enclosure of a PLL region of P-channel along the direction of poly gate	0.35
PLL.13		Minimum PLL area for a P-channel poly gate must follow PLL.8 and PLL.12	
PLL.E01		PLL inside DNW or PSUB or TPW is forbidden.	

Note: Diagram refers to 7.6.14 NLL and change N+ AA to P+AA, P+AA to N+AA, PW to NW and NW to PW, NLL to PLL and NLH to PLH

7.6.17 SN
The (SN) layout layer is drawn to define N+ S/D implant regions.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**SN**	
SN.E01	To be compatible to 0.18LG's mask-layer logic operation rules, SN must be fully inside DNW or PSUB or TPW, or fully outside DNW	

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or PSUB or TPW. Partial-overlap of SN to DNW or PSUB or TPW is NOT allowed.

SN.E02	Minimum space of SN to DNW or PSUB or TPW	0.30
SN.E03	Poly2(CG) must be fully inside SN, cross-over of SN to Poly2(CG) is NOT allowed.	
SN.E04	Minimum enclosure of SN to Poly2(CG)	0.26
SN.E05	SN overlap of Poly1-(GT) inside NW is forbidden	
SN.E06	Minimum space of SN to non-SN Poly1(GT)	
	SN.E06a From an SN edge butted well pickup to a P-Channel P1(GT) 3.3v MV, 5v Quasi-HVPMOS (Show on SN layout). <0.3um extension of gate in the direction of GT	0.32
	SN.E06b From an SN edge butted well pickup to a P-Channel P1(GT) Real-HVPMOS (Show on SN layout). <0.3um extension of gate in the direction of GT	1.20
	SN.E06c From an SN edge to a P1(GT) > = 0.3um extension of gate in the direction of GT	0.26
SN.E07	Poly1(GT) for Resistor purpose must be covered by SN	

Below design rules also apply to SN inside PSUB, DNW, TPW

SN.1	Minimum width of an SN region	0.44
SN.2	Minimum space between two SN regions. Merge if space is less than 0.44µm	0.44
SN.3	Minimum space between a SN region and a P+ AA region. (inside N-well)	0.26
SN.4	Minimum space between a SN region and a P+ pick-up AA region. if the distance between P+AA and NW >=0.43um.	0.10
SN.5	Minimum space between a SN region and a non-butted edge of P-well pick-up P+AA region if the distance between P+AA and N-well <0.43µm	0.18
SN.6	Minimum space from a SN edge to a P-channel Poly gate.	0.32
SN.7	Minimum enclosure of a SN edge to an N-channel Poly gate.	0.32
SN.8	Minimum overlap from a SN edge to an AA	0.23

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SN.9	Minimum enclosure of a SN region beyond a SN active region	0.18
SN.10	Minimum enclosure of a SN region beyond an N+ pick-up AA region if the distance between N+AA and P-Well >=0.43µm	0.02
SN.11	Minimum enclosure of a SN region beyond an N+ pick-up AA region if the distance between N+AA and P-Well < 0.43µm	0.18

    a. To obey this rule and SN.3 simultaneously, the minimum space between N+ pick-up AA and SP active AA should be increased to 0.44µm

    b. To obey this rule and SN.5 simultaneously, the minimum space between N+ pick-up AA and SP active AA should be increased to 0.36µm

SN.12	Separation from a SN region to butted edge of a butted diffusion SP AA (inside P-well)	0.00
SN.13	Minimum extension of a SN region along the edge of a butted diffusion N+AA/P+AA	0.00
SN.14	Minimum area of a SN region	0.40
SN.15	Minimum extension of a SN region beyond a poly as a resistor. SAB poly without SN or SP implant is NOT allowed.	0.18
SN.16	Minimum space from a SN edge to a P-channel Poly gate along the direction of poly gate.	0.35
SN.17	Minimum enclosure of a SN edge to a N-channel Poly gate along the direction of poly gate.	0.35
SN.18	SN is not allowed to overlap with SP	
SN.19	It is prohibited that SN being generated by the reverse tone of SP, since this operation might violate SN.3 and SN.4	
SN.20	Minimum SN area for a N-channel poly gate must follow SN.7 and SN.17	

(SN)

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7.6.18 SP

The (SP) layout layer is drawn to define P+ S/D implant regions.

RULE NO.	DESCRIPTION		LAYOUT RULE
Layer	**SP**		
SP.E01	To be compatible to 0.18LG's mask-layer logic operation rules, SP must be fully inside DNW or PSUB or TPW, or fully outside DNW or PSUB or TPW. Partial-overlap of SP to DNW or PSUB or TPW is NOT allowed.		
SP.E02	Minimum space of SP to DNW or PSUB or TPW		0.30
SP.E03	SP can NOT cover Poly2(CG), cross-over of SP to Poly2(CG) is NOT allowed.		
SP.E04	Minimum space of SP to Poly2(CG)		0.26
SP.E05	SP overlap of Poly1(GT) inside PW is forbidden		
SP.E06	Minimum space of SP to non-SP Poly1(GT)		
	SP.E06a	From an SP edge butted well pickup to a N-Channel P1(GT) HVN/ZMOS, <0.3um extension of gate in the direction of GT	0.32
	SP.E06b	From an SP edge to a P1(GT) > = 0.3um extension of gate in the direction of GT	0.26
SP.E07	Poly1(GT) for Resistor purpose can NOT be covered, or cross-over by SP		
	SP.E08 ~ SP.E12 apply to Real-HVPMOS only		
SP.E08	SP must be drawn inside Real-HVPMOS AA, cross-over of SP to AA is NOT allowed.		
SP.E09	Minimum SP width inside Real-HVPMOS Active Area		
	SP.E09a	with CT	0.82
	SP.E09b	without CT	0.44
SP.E10	Min/Max space of SP inside AA to Poly1(GT) gate edge.		= 0.55
SP.E11	Min/Max space of SP inside AA to AA edge		= 0.40
SP.E12	Minimum Space of SP outside AA to Real-HVPMOS AA edge.		0.26
	Below design rules also apply to SP inside PSUB, DNW, TPW.		
SP.1	Minimum width of a SP region		0.44

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SP.2	Minimum space between two SP regions. Merge if the space is less than 0.44μm	0.44
SP.3	Minimum space between a SP region and a N+ AA region (inside P-well)	0.26
SP.4	Minimum space between a SP region and a non-butted edge of N+ pick-up AA region if the distance between N+AA and PW >=0.43um.	0.10
SP.5	Minimum space between a SP region and a non-butted edge of N-well pick-up N+AA region if the distance between N+AA and P-well <0.43μm	0.18
SP.6	Minimum space from a SP edge to N-channel Poly gate.	0.32
SP.7	Minimum enclosure of a SP edge to P-channel Poly gate.	0.32
SP.8	Minimum overlap from a SP edge to an AA	0.23
SP.9	Minimum enclosure of a SP region beyond a SP active region	0.18
SP.10	Minimum enclosure of a SP region beyond a P-Well pick-up P+AA region if the distance between P+AA and N-Well >=0.43μm	0.02
SP.11	Minimum enclosure of a SP region beyond a P-Well pick-up P+AA region if the distance between P+AA and N-Well < 0.43μm	0.18
	c. To obey this rule and SP.3 simultaneously, P+ pick-up AA to SN active AA minimum spacing must be increased to 0.44μm	
	d. To obey this rule and SP.5 simultaneously, P+ pick-up AA to SN pick-up AA minimum spacing must be increased to 0.36μm	
SP.12	Separation from a SP region to butted edge of a butted diffusion SN AA (inside N-well)	0.00
SP.13	Minimum extension of a SP region along the edge of a butted diffusion P+AA/N+AA	0.00
SP.14	Minimum area of a SP region	0.40
SP.15	Minimum extension of a SP region beyond a poly as a resistor. SAB poly without SN or SP implant is NOT allowed.	0.18
SP.16	Minimum space from a SP edge to N-channel Poly gate along the direction of poly gate	0.35
SP.17	Minimum enclosure of a SP edge to P-channel Poly gate along the direction of poly gate	0.35

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SP.18   SP is not allowed to overlap with SN

SP.19   It is prohibited that SP is generated by the reverse tone of SN, since
             this operation might violated SP.3 and SP.4

SP.20   Minimum SP area for a P-channel poly gate must follow SP.7 and
             SP.17

Note: Diagram refers to 7.6.16 and replaces SP as SN, P+AA as N+AA, N-Well as P-Well.

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7.6.19 SAB
The (SAB) layout layer is drawn to define regions to be blocked from salicidation.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**SAB[Note1,2]**	
SAB.1	Minimum width	0.43
SAB.2	Minimum space	0.43
SAB.3	Minimum space to unrelated diffusion	0.22
SAB.4	Minimum space to contact	0.22
SAB.5	Minimum space to GT/CG/GP on diffusion	0.45
SAB.6	Minimum extension over related diffusion	0.22
SAB.7	Minimum extension of diffusion over related SAB	0.22
SAB.8	Minimum extension over related GT/CG/GP on field oxide	0.22
SAB.9	Minimum space of SAB to unrelated GT/CG/GP on field oxide	0.30
SAB.10	Minimum area of SAB	2.00
SAB.11	Below CTs in SAB area is forbidden	
	SAB.11a inside NW or PW	
	SAB.11b inside P+AA	
SAB.E01 ~ SAB.E07 apply to Real-HVPMOS only		
SAB.E01	SAB must cover Real-HVPMOS AA, only S/D contact regions are allowed to open SAB. (SAB Opening)	
SAB.E02	SAB Opening must be drawn inside SP in Real-HVPMOS AA, cross-over of SAB Opening to SP is NOT allowed.	
SAB.E03	Minimum SAB Opening width inside Real-HVPMOS AA	merge if < 0.52
SAB.E04	Minimum enclosure of SP to SAB Opening boundary (inside GT or AA)	0.15
SAB.E05	Minimum enclosure of SAB to Real-HVPMOS AA	0.25
SAB.E06	Minimum enclosure of SAB to Real-HVPMOS Poly1(GT)	0.25
SAB.E07	Minimum space of SAB opening on Poly1(GT) to Poly1(GT) boundary	0.20

Note.2　　　Follow poly resistor guideline, if poly resistor is used.

Note.3　　　For I/O and ESD, pls follow "0.18um EEPROM ESD/LatchUp
Device Layout Guide Line " (TD-EE18-DR-2005)
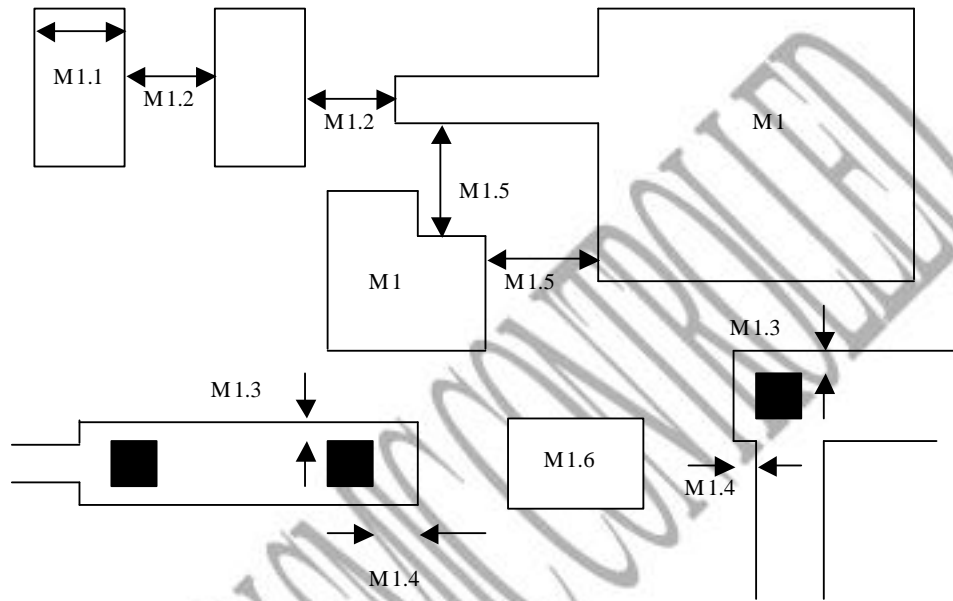
(SAB)

(SAB)

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7.6.20 CT

The (CT) layout layer is drawn to define contact hole opening.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**CT**	
	Below design rules apply to CT outside EEArrays[Note1]	
CT.01	Minimum/maximum contact size	0.22
CT.02	Minimum space between two contacts	0.25
CT.03	Minimum space between two contacts in a contact array with row and column numbers are both greater than 3.	0.28
CT.04	Minimum space between a poly (GT/CG/GP) CT and a diffusion region	
	CT.04a CT on Poly2-GP to AA	0.20
	CT.04b CT on Poly1-GT/Poly2-CG to AA	0.40
CT.05	Minimum space between a poly gate (GT/CG/GP) to a diffusion CT	
	CT.05a Diffusion CT to Poly2-GP on AA	0.16
	CT 05b Diffusion CT to Poly1-GT on AA (5v)	0.19
	CT.05c Diffusion CT to Poly1-GT on AA(15.5v)	0.26
	CT.05d Diffusion CT to Poly2-CG on AA	0.22
CT.06	Minimum diffusion enclosure for a diffusion contact	
	CT.06a outside (PSUB or DNW)	0.10
	CT.06b inside DNW or PSUB	0.15
CT.07	Minimum poly enclosure for a Poly1(GT)/Poly2(GP)/Poly2(CG) contact	
	CT.07a Poly2-GP CT	0.10
	CT.07b Poly1-GT/Poly2-CG CT	0.20
CT.08	Minimum enclosure of a SP region beyond an AA contact region	0.12
CT.09	Minimum enclosure of a SN region beyond an AA contact region	0.12
CT.10	Poly (GT/CG/GP) CT on AA region is forbidden	

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CT.11   AA contact located on SN/SP boundary is NOT allowed

CT.12   Non-Salicide CT is ONLY allowed in PSUB, and the CT must be covered by SN.

CT.E01~E04 apply to Real-HVPMOS only

CT.E01   Minimum space of CT to SAB Opening of Real-HVPMOS, either on AA or Poly1(GT)   0.15

CT.E02   Minimum space of CT to SP Opening of Real-HVPMOS, either on AA or Poly1(GT)   0.30

CT.E03   Minimum space of CT on AA to Poly1(GT) of Real-HVPMOS   0.85

CT.E04   Minimum space of CT on AA to AA edge of Real-HVPMOS   0.70

Note.1   CT inside EEPROM bitcell is blocked from DRC with DRC auxiliary layer RP93 and described in details on 7.7 "DRC AUXILIARY LAYERS"

(CT)

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According to: SMIC Document Control Procedure; Attachment No.: QR-QUSM-02-2001-023; Rev.:1   2008-06-27

(CT)

7.6.21 Metal-1

The (M1) layout layer is drawn to define Metal-1, first metal layer.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**M1**	
M1.1	Minimum width of M1 region	0.23
M1.2	Minimum space between two M1 regions	0.23

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M1.3	Minimum enclosure of M1 region over CT region	0.005
M1.4	Minimum enclosure of M1 line end region beyond CT region. (For CT at 90 degree corner, one side of metal enclosure must be considered as line end region)	0.06
M1.5	Minimum space between Ml lines with one or both metal line width and length are greater than 10µm; the minimum space must be maintained between a metal line and a small piece of metal (<10µm) that is connected to the wide metal within 1.0µm range from the wide metal	0.60
M1.6	Minimum area of M1 region	0.20
M1.7	Minimum density of M1 area Density is calculated as [total metal layout area]/[chip area] Dummy pattern is required for those with M1 density less than 30%.	30%
M1.8	For dummy metal pattern, please check SMIC dummy rule.	

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M1.1

M1.2

M1.2

M1

M1.5

M1

M1.5

M1.3

M1.3

M1.6

M1.4

M1.4

Example of Dummy Pattern

M1.8

5 µm

2 µm

2 µm

2 µm

2 µm

7.6.22 Via-1

The (V1) layout layer is drawn to define Via-1, the first Via layer.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**V1**	
V1.1	Minimum/maximum size of a V1	0.26
V1.2	Minimum space between two V1	0.26
V1.3	Minimum metal 1 enclosure for a V1	0.01
V1.4	If Metal 1 line end beyond V1	0.06
	For V1 located at the 90 degree corner, one side of metal extension must be treated as end-of-line and the other side follows V1.3	
V1.5	Stacked Via's and contacts are allowed	

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7.6.23 Metal n

The (Mn) layout layer is drawn to define the Metal-2 of 2P3M process.
The (Mn) layout layer is drawn to define the _Metal-2,3_ of _2P4M_ process.
The (Mn) layout layer is drawn to define the _Metal-2,3,4_ of _2P5M_ process.
The (Mn) layout layer is drawn to define the _Metal-2,3,4,5_ of _2P6M_ process.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**Mn**	
Mn.1	Minimum width of an Mn region	0.28
Mn.2	Minimum space between two Mn regions	0.28
Mn.3	Minimum extension of Mn region beyond Vn-1 region	0.01
Mn.4	Minimum extension of Mn line end region beyond Vn-1 region.	0.06
	For Vn-1 located at 90 degree corner, one side of metal extension must be treated as end-of-line, the other side follows Mn.3.	
Mn.5	Minimum space between metal lines with one or both metal line width and length are greater than 10µm; the minimum space must be maintained between a metal line and a small piece of metal (<10µm) that is connected to the wide metal within 1.0µm range from the wide metal	0.60
Mn.6	Minimum area of a Mn region	0.20
Mn.7	Minimum density of Mn area	30%
	Density is calculated as [total metal layout area]/[chip area]	
	Dummy pattern is required for those with Mn density less than 30%.	
Mn.8	As to metal dummy pattern, please check SMIC Dummy Rules.	

* Refers to 7.12 for MIM design rule

7.6.24 Via-n

The (Vn) layout layer is drawn to define the Via-1 of 2P3M Process.
The (Vn) layout layer is drawn to define the _Via-2_ of _2P4M_ Process.
The (Vn) layout layer is drawn to define the _Via-2,3_ of _2P5M_ Process.
The (Vn) layout layer is drawn to define the _Via-2,3,4_ of _2P6M_ Process.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**Vn**	
	Vn can be located at any region	
Vn.1	Minimum/maximum size of a Vn	0.26
Vn.2	Minimum space between two Vn	0.26
Vn.3	Minimum Mn enclosure for a Vn	0.01
Vn.4	Minimum enclosure of Mn over Vn along metal line direction	0.06
	For Vn located at the 90 degree corner, one side of metal extension must be treated as end-of-line and the other side follows Vn.3	
Vn.5	Vn can be fully or partially stacked on Vn-1, any stacked structure such as stacked Vn/Vn-1/…/V1/CT	

7.6.25 Top_Via(VT)

The Top_Via(V2) layout layer is drawn to define Via-2, the last Via of 2P3M Process.
The Top_Via(V3) layout layer is drawn to define _Via-3_, the last Via of _2P4M_ Process.
The Top_Via (V4) layout layer is drawn to define _Via-4_, the last Via of _2P5M_ Process.
The Top_Via (V5) layout layer is drawn to define _Via-5_, the last Via of _2P6M_ Process.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**Top_Via**	
VT.1	Minimum/maximum size of a VT	0.36
VT.2	Minimum space between two VT	0.35
VT.3	Minimum Mn-1 enclosure for a VT (Mn is top Metal)	0.01

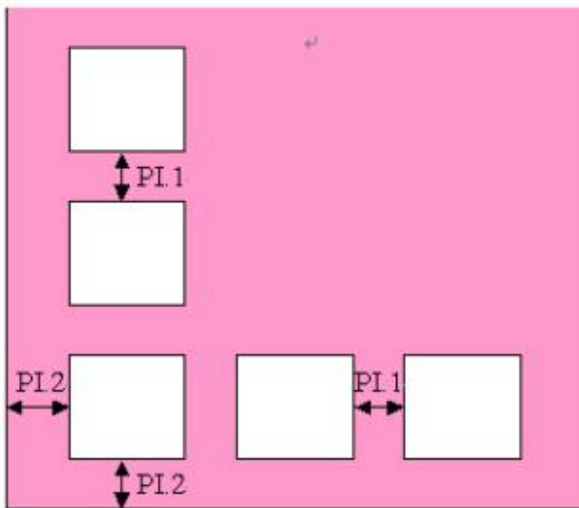## Semiconductor Manufacturing International Corporation

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VT.4   Minimum enclosure of Mn-1 over VT along metal line direction   0.06

For Mn-1 located at the 90 degree corner, one side of metal extension must be treated as end-of-line and the other side follows VT.3   (Mn is top Metal)

VT.5   VT can be fully or partially stacked on VT/Vn-2/Vn-3, any stacked structure such as stacked VT/Vn-2/Vn-3/…/V1/CT

(n=4 if 2P4M process adopted)

(n=5 if 2P5M process adopted)

(n=6 if 2P6M process adopted)

7.6.26 Top Metal-TM

The (TM) layout layer is drawn to define the last Metal layer, which is M3 for 2P3M process.
The (TM) layout layer is drawn to define the last Metal layer, which is *M4* for *2P4M* process.
The (TM) layout layer is drawn to define the last Metal layer, which is *M5* for *2P5M* process.
The (TM) layout layer is drawn to define the last Metal layer, which is *M6* for *2P6M* process.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**TM – Top Metal**	
TM.1	Minimum width of a top metal region	0.44
TM.2	Minimum space between two top metal regions	0.46
TM.3	Minimum extension of TM region over VT	0.09
TM.4	Minimum space between top metal lines with one or both metal line width and length are greater than 10µm; this also includes all metals attached to these areas or extending out for a distance of 1.0µm or less	0.60
TM.5	Minimum area of an TM region	0.56
TM.6	Minimum density of metal n area	30%
	Density is calculated as [total metal layout area]/[chip area]	
	Dummy pattern is required for those with TM density less than 30%.	
TM.7	As to TM dummy pattern, please check SMIC Dummy Rules.	

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7.6.27 Polyimide

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**PI - Polyimide**	
PI.1	Minimum space between two polyimide open area	15
PI.2	Minimum space between polyimide open area to chip edge	15

Notice :
Generally PI is LOTA generated layer in SMIC, if it is drawn by customer, pls kindly follow the rule.

Polyimide

7.6.28 LAYOUT SUGGESTION FOR CIRCUIT YIELD OPTIMIZATION

Front-end concerns
    A. AA: add dummy patterns for isolated small structures or open areas around AA.
    B. Poly: dummy Poly pattern density rule
        B1 : GT pattern density had better be in 15% - 55%.
        GT pattern density calculation : GT/Chip
        B2 : GP pattern density should be in 35% - 85%.
        GP pattern density calculation : [(ONO sd 0.25) + GP]/Chip
        B3 : CG pattern density revise to 10% - 80%.
        Notice :
        If CG pattern density can not meet the spec, pls try to enlarge or scale the ONO area
        CG pattern density can be adjusted by ONO enlarge or scale
        CG pattern density calculation : (1 - (((((ONO su 0.25) su 0.25) sd 0.3) - CG)/chip))*100%
        If pattern density is not meet the requirement, dummy pattern is suggested follow the 7.6.28
    C. Follow the antenna rules to ensure gate oxide reliability.
    D. For the leakage concern, avoid 90 degree bent poly designs, which should be replaced by 45 degree bent poly on AA with shortest length.
    E. Avoid island pattern designs for implantation layers.

Back-end concerns
    B. Add dog-bone or wider line end designs for metal lines.
    C. Use redundant contacts or Via's if possible.
    D. Avoid small metal island structures for stacked Via as possible.
    E. Follow the antenna rules to ensure gate oxide reliability.

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7.6.29 Dummy Pattern Layout Suggestion

Dummy pattern layout guide line for customer, customer should add dummy pattern by themselves if dummy pattern is necessary.
Pls kindly and carefully check the DRC after the dummy pattern added for the chip.

7.6.29.1 Dummy Metal Rule

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	**Dummy Metal Pattern**	Unit : (um)
DM.01	Dummy metal line width	2
DM.02	Dummy metal line length	5
DM.03	Dummy metal space	2
DM.04	Displacement of adjacent dummy lines	2
DM.05	Space of dummy metal and the dummy metal block layer	2
DM.06	Space of dummy metal and the real metal	2
DM.07	Space between dummy metal and chip edge	2
DM.08	Space between dummy and MOS edge (Poly * AA) Poly means GT/GP/CG	2
DM.09	Define GDSII 121 (DUMBM) as block layer for metal	
DM.10	No metal dummy layer is allowed under DUMBM	
DM.11	The dummy pattern of adjacent layer Mn and M_{n+1} need 90° rotate	
DM.12	Only whole dummy metal pattern is allowed, chopped pattern is not suggested	
DM.13	No dummy metal is allowed on CSD layer, space of dummy metal to CSD	2
DM.14	No dummy layer is allowed on BITCEL, space of dummy metal to BITCEL	2

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7.7 DRC/LVS AUXILIARY LAYERS

User is RECOMMENDED to use following auxiliary layers for DRC/LVS purpose.

	Tech	Drawn Layer Name	Drawn Layer GDS Num	Description
1	18EE	RESDMY	(90)	Dummy Layer For DRC/LVS purpose: Define resistors other than covered by RESNW, RESAA, RESP1 CAD layers.
2	18EE	RLHVP	(91)	Dummy Layer for DRC/LVS purpose: Define Real-HVPMOS
3	18EE	5VHVNZ	(92)	Dummy Layer for DRC/LVS purpose: Define 5V HVN/ZMOS
4	18EE	BITCEL	(93)	Dummy Layer for DRC/LVS purpose: Define EEArray BitCell
5		RESNW	(95)	Dummy Layer For DRC/LVS purpose: Define NW resistors.
6		RESP1	(96)	Dummy Layer for DRC/LVS purpose: Define non-Salicide Poly2-(GP) resistors.
7		RESAA	(97)	Dummy Layer for DRC/LVS purpose: Define non-Salicide Diffusion resistors.
8		CAPBP	(137)	Dummy Layer for DRC/LVS purpose: Capacitor Bottom Plate.
9		DMPNP	(134)	Dummy Layer for DRC/LVS purpose: Define 3.3v/1.8v BJT Device.
10		ESDIO	(133)	Dummy Layer for IO region DRC/LVS purpose: Define ESD/IO Device
11		HRP	(39)	Dummy Layer for HRP DRC/LVS purpose: Define High Resistor Poly Device
12		HRPDMY	(210)	Dummy Layer for HRP DRC/LVS purpose: Define High Resistor Poly Device
13		DSTR	(138)	Define diode for LVS purpose
14		OPCBA	(100)	Blocking layer for DRC/LVS operation on AA
15		OPCBP	(101)	Blocking layer for DRC/LVS operation on GP
16		OPCBM	(102)	Blocking layer for DRC/LVS operation on M1
17		MIMDMY	(88;1)	Define the dummy MiM

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7.7.1   RESDMY   (GDS#90)

RESDMY   (GDS#90): DRC/LVS Auxiliary Layer for Resistor

a) To define Resistor other than covered by Res_P1, Res_AA, Res_NW. (e.g. TIM resistor)

b) User is RECOMMENDED to draw RESDMY to prevent possible False DRC/LVS errors on Resistors.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	RESDMY. **(GDS#90)**	
DRC.RE1	Those design rules specifically described for Resistor are checked with DRC auxiliary layer, RESDMY.	
DRC.RE2	The portions of NW/AA/GT/CG(Poly2) overlapped with RESDMY is defined as Resistor.	
DRC.RE3	RESDMY must entirely cover NW/AA/GT/CG/GP for resistor purpose.	
DRC.RE4	TIM resistor: AA.E01b is applied to " (AA) AND (TIM), which is inside RESDMY ".	
DRC.RE5	Inside RESDMY, except specifically described, other DRC items follow general design rules.	

7.7.2   RLHVP   (GDS#91)

RLHVP   (GDS#91): DRC/LVS Auxiliary Layer for Real-HVPMOS

a) To define Real-HVPMOS region to discern between Quasi/Real-HVPMOS.

b) User is RECOMMENDED to draw RLHVP to prevent possible False DRC errors on Real-HVPMOS.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	RLHVP **(GDS#91)**	
DRC.HP1	Those design rules specifically described for Real-HVPMOS are checked with DRC auxiliary layer, RLHVP.	
DRC.HP2	RLHVP must entirely cover AA/GT/SP/SAB/CT of Real-HVPMOS.	
DRC.HP3	AA/GT/SP/SAB/CT inside RLHVP are checked with Real-HVPMOS Design Rules.	
DRC.HP4	Inside RLHVP, except specifically described, other DRC items follow general design rules.	

7.7.3 5VHVNZ (GDS#92)

5VHVNZ (GDS#92): DRC/LVS Auxiliary Layer for 5v HVN/ZMOS

a) To define 5v HVN/ZMOS to discern between 15.5v HVN/ZMOS.

b) User is RECOMMENDED to draw 5VHVNZ to prevent possible False DRC errors on 5v HVN/ZMOS.

RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	5VHVNZ **(GDS#92)**	
DRC.MN1	Those design rules specifically described for 5v HVN/ZMOS are checked with DRC auxiliary layer, 5VHVNZ	
DRC.MN2	5VHVNZ must entirely cover AA/HVPF/GT for 5v application.	
DRC.MN3	Inside 5VHVNZ, except specifically described, other DRC items follow general design rules.	

7.7.4 BITCEL (GDS#93)

BITCEL (GDS#93): DRC/LVS Auxiliary Layer for EEArray BitCell

a) To define EEArray BitCell for DRC.

b) User is RECOMMENDED to draw BITCEL to prevent possible False DRC errors on EEArray BitCell.

7.7.5 RESNW, RESP1, RESAA (GDS#95//96/97)

The usage of RESNW, RESP1, RESAA follows same guideline for SMIC 0.18um generic logic process.

7.7.6 CAPBP (GDS#137)

CAPBP (GDS#137): DRC/LVS Auxiliary Layer for PIP

a) To define PIP for DRC.

b) User is RECOMMENDED to draw CAPBP to prevent possible False DRC errors on PIP.

c) Rule ONLY check from AA to CT

7.7.7 DMPNP (GDS#134)

DMPNP (GDS#134): DRC/LVS Auxiliary Layer for PIP

a) To define 1.8/3.3V PNP for DRC&LVS

b) User is RECOMMENDED to draw DMPNP to prevent possible False DRC errors on PNP.

c) Rule ONLY check from AA to SAB

7.7.8 HRP,HRPDMY (GDS#39/ GDS#210)

HRP,HRPDMY (**GDS#39/ GDS#210**): DRC/LVS Auxiliary Layer for HRP

Pls refer to layout example 7.12.2 **HRP DESIGN RULES**

7.7.9   FUSE (GDS#209)

FUSE (**GDS#209**): Define fuse window

Pls refer to layout example **7.8   METAL FUSE/ALIGNMENT MARK FOR LASER REPAIR AND STRESS RELIEF**

7.7.10   EXCLU (GDS#132)

EXCLU (GDS#209): Define un-DRC area

        a.) Define un-DRC area

        b.) If seal ring drawn by customer, pls add this layer in seal ring for un-DRC purpose

        c.) Since seal-ring is un-DRC area, pls kindly make sure it is fully meet the design rule if it is drawn by customer

7.7.11   OPCBA (GDS#100)/ OPCBP (GDS#101)/ OPCBM (GDS#102)

OPCBA (GDS#100)/ OPCBP (GDS#101)/ OPCBM (GDS#102) : Define SRAM OPC block layer

        a.) Define SRAM area for SRAM model OPC on AA/GP/M1

        b.) These three layers are auto generated by library

7.7.12   MIMDMY(GDS# 88;1)

MIMDMY(GDS# 88;1) : Define dummy MiM patteren

Used to distinguish MiM and dummy MiM

7.7.13   INST(GDS#60)

INST(GDS#60) : DRC/LVS Auxiliary Layer for EEArray BitCell

  a) To define EEArray BitCell for DRC with BITCEL(GDS#93).

  b) User is RECOMMENDED to draw INST to fully cover all EEArray Region.

  c) These rules are based on SMIC provided EEPROM array layout to generate _ONLY_ for DRC, and CTM must compare their own layout with SMIC array example before tape out.

  From AA to CT(FEOL DRC check), only rules listed here are checked, BEOL follow standard rule

  Region covered by (BITCEL and INST)

RULE NO.		DESCRIPTION	LAYOUT RULE
Layer	Layer	EEPROM Cell Special Rule apply to EEPROM Cell	Unit (um)
EE.01	AAE_1	Minimum AA width	0.3
EE.02	AAE_2	Minimum space between two N+AA space (both inside PSUB)	0.28

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EE.03	TIM.3	Minimum TIM enclosure related AA	Not necessary
EE.04	PF_6b	Minimum HVPF enclosure AA in PSUB	0.3
EE.05	GTE.1c	Minimum width of GT 15.5V HZNMOS (inside PSUB)	1.4 (where cover [INST-BITCEL])
EE.06	GTE_8	Minimum extension of GT to related AA edge (end-cap)	0.14 (Byte-SG)
EE.07	CG.2	Minimum width of CG	No issue, runset to cover
EE.08	CG.6_7	Minimum space of POLY2(CG) on FOX to AA	0.05 (Byte-SG)
EE.09	CG_9	Minimum extension of CG to AA (end cap)	0.25 (Byte-SG)
EE.10	DDD.3	Minimum enclosure of DDD to related AA	0
EE.11	DDD.4	Minimum space of DDD to unrelated AA	0.3
EE.12	DDD.6	AA must be either fully inside DDD,or outside DDD	Not Necessary
EE.13	SAB_8	Minimum extension of SAB over related poly on field oxide is 0.22um	0
EE.14	SAB_9	Minimum space of SAB to unrelated poly on field oxide is	0.1 (Byte-SG)
EE.15	CT_1	Mininmum/Maximum contact size is 0.22um	0.32 (min.)(where cover [INST*SAB])
EE.16	CT_4b	Minimum space between GT/CG contact to AA is 0.40um	0.175 (Byte-SG)
EE.17	CT_5c	Minimum space between diffusion contact to GT_poly on AA(15.5V) is 0.26um	0.2 (Byte-SG area, mini 0.2,but Drain side must be 0.26
EE.18	CT_6b	Minimum enclosure of an AA region beyond an AA CT region is 0.15um (intside PSUB or DNW)	0.04 (BL CT)
EE.19	CT_10	CT on gate region is forbidden	Not necessary
EE.20	RES_1	Min. TIM extension GT for TIM resistor is 0.30	Use INST layer, exclude Cell array check
EE.21	RES_2	GT must be drawn for TIM resistor	Use INST layer, exclude Cell array check
EE.22		ONO/PSUB/SN/ space is not allowed in INST	
EE.23	AA.E5	Minimum enclosure from PSUB edge to (P+AA pick-up inside PSUB)	0.6
EE.24	AA.E4	Minimum enclosure from PSUB edge to (N+AA inside PSUB)	2.5
EE.25	SN.E4	Minimum enclosure of SN to Poly2(CG)	0
EE.26	SN.7	Minimum enclosure of a SN edge to an N-channel Poly gate.	0
EE.27	SN.9	Minimum enclosure of a SN region beyond a SN active region	0
EE.28	SAB.5	Minimum space to GT/CG/GP on diffusion	0.4
EE.29	sab.6	Minimum extension over related diffusion	0
EE30	AA.E3	Minimum space between N+AA to (P+AA pick-up), both inside PSUB	0.30

Not necessary : means cell do not check this rule

7.7.14 CLPDMY(GDS#87)

CLPDMY(GDS#87) : DRC/LVS Auxiliary Layer for SMIC provided the clamp diode

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The rules list here is special for clamp diode, which do not same as periphery design rule

RULE NO.		DESCRIPTION	LAYOUT RULE
Layer	Layer	Clamp diode layout rule	Unit (um)
CLP.01	NWE_2	Minimum space NW to PSUB	0
CLP.02	SP_1	Minimum width of a SP region	0.43
CLP.05	CT_6a	Minimum enclosure of an AA region beyond an AA CT region is 0.10um (outside PSUB or DNW)	0.09
CLP.06		Convention_BAD_IMP	Not necessary
CLP.07		Minimum space of CT to GT	0.55
CLP.08		Minimum AA space	0.50
CLP.09		Minimum DNW to PSUB	2.80
CLP.10		Minimum DNW enclosure N+AA	2.00
CLP.11		Minimum NW enclosure N+AA	1.02
CLP.12		ONO must cover all CLPDMY region	

7.8   METAL FUSE/ALIGNMENT MARK FOR LASER REPAIR AND STRESS RELIEF

7.8.1   Metal Fuse Rules

RULE NO.	DESCRIPTION	LAYOUT GUIDELINE (Unit in μm)
Fuse.1	Width of metal fuse	0.80
Fuse.2	Minimum space of metal fuse	4.00
Fuse.3	Minimum length of metal fuse	4.00
Fuse.4	Maximum length of metal fuse	10
Fuse.5	Minimum extension from GT to CT	0.30
Fuse.6	Minimum extension from M1 to CT	0.30
Fuse.7	Minimum extension from M1 to MT-1 to CT/V1~V3 (stacked via)	0.30
Fuse.8	Min. separation from fuse edge to p-well edge (p-type substrate are used)	8.00
Fuse.9	Min. separation from fuse to fuse window	3.50

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Fuse.10	Min. separation from fuse window to protection ring	1.50
Fuse.11	Width of V1~Vx-1 in protection ring	0.26
	Width of Vx-1 in protection ring	0.36
Fuse.12	Minimum extension from M1~Mx to V1~Vx-1 in protection ring	0.40
Fuse.13	Minimum width of fuse window	5.00
Fuse.14	Minimum length of fuse window	20
Fuse.15	Minimum width of polymide opening	30
Fuse.16	Min. extension from polymide window to passivation window	12
Fuse.17	Min. separation between Via's inside protection ring	0.00
Fuse.18	Min. separation from metal island to protection ring	1.00

- **In 2PxM process, MT-1 is required to be used as fuse.**
  For Example:
  In 2P6M process, M5 is required to be used as fuse.
  In 2P5M process, M4 is required to be used as fuse.
  In 2P4M process, M3 is required to be used as fuse.
  In 2P3M process, M2 is required to be used as fuse.
  In 2P2M process, M1 is required to be used as fuse.
- **Metal fuse has to be connected to GP through stacked Via/contact.**
- **Alignment Mark should be located at each corner of the chip.**
- **Alignment Mark should follow the Alignment Mark Rule for laser repairing.**

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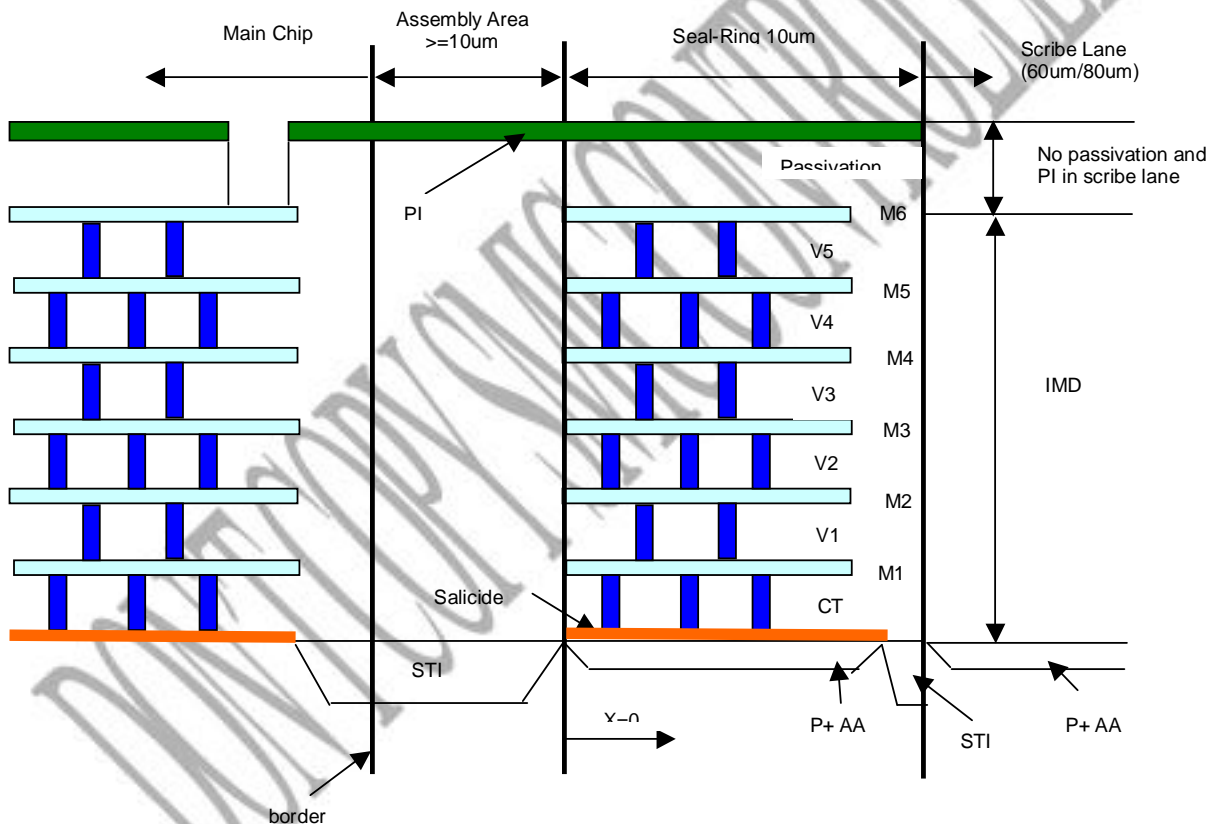# Semiconductor Manufacturing International Corporation

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Fuse (Metal) Window Cross Section

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7.8.2 Alignment Mark for Laser Repairing

L mark should be on each corner of a chip

L mark should be the top metal layer and with passivation open above the target

L mark should be surrounded by protection ring

L mark and its protection ring can replace corner dummy pads to serve as stress-relieve structure, i.e., alignment marks do not occupy extra die area.

RULE NO.	DESCRIPTION	LAYOUT GUIDELINE (Unit in μm)
Mark.1	Minimum width of mark	10
Mark.2	Minimum length of mark	40
Mark.3	Min. separation from a mark to the protection opening	30
Mark.4	Min. separation from passivation opening to protection ring	1.50
Mark.5	Min. and max. width of V1/V2/V3/V4 in protection ring	0.36
Mark.6	Min. extension from M1/M2/M3/M4/M5 to V1/V2/V3/V4	0.40

7.8.3 Metal Slot Suggestion rule

This rule just suggestion rule for CTM to use .

RULE NO	DESCRIPTION	RULE (μm)
	The slot rules are applied to avoid thermal stress induce reliability issue.	
	All metal layers suggest to follow this rule.	
	The metal slot must be placed for wide metal lines. The wide metal is defined as being >= 35μm wide. Only bonding pad areas are excluded.	
SL.1a	Maximum width of an open slot	5
SL.1b	Minimum width of an open slot	2
SL.2	Minimum length of an open slot	20
SL.3a	Suggested maximum space between any two parallel open slots	35
SL.3b	Suggested minimum space between any two parallel open slots	10

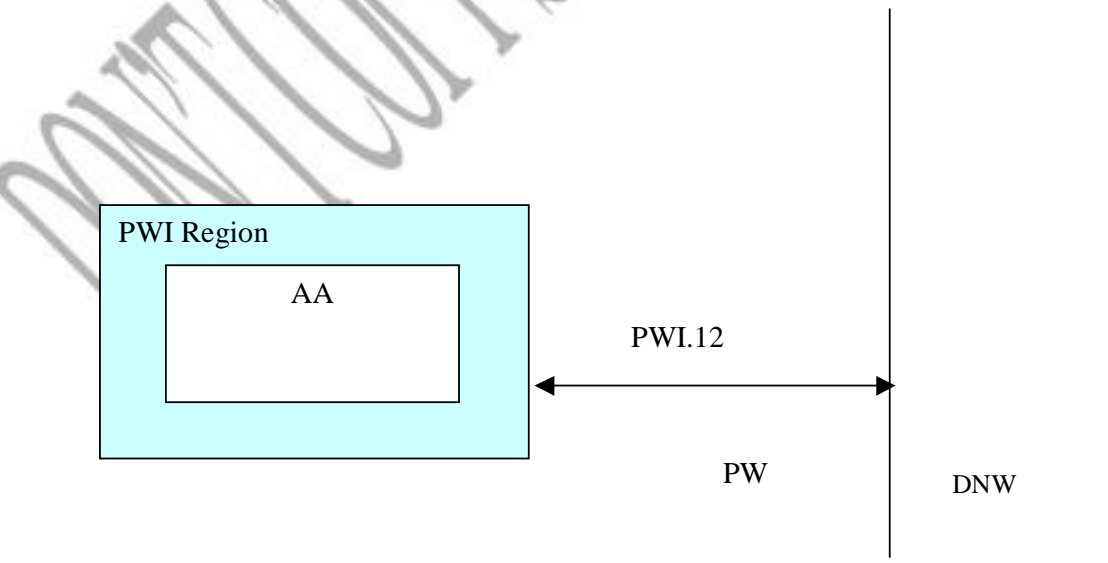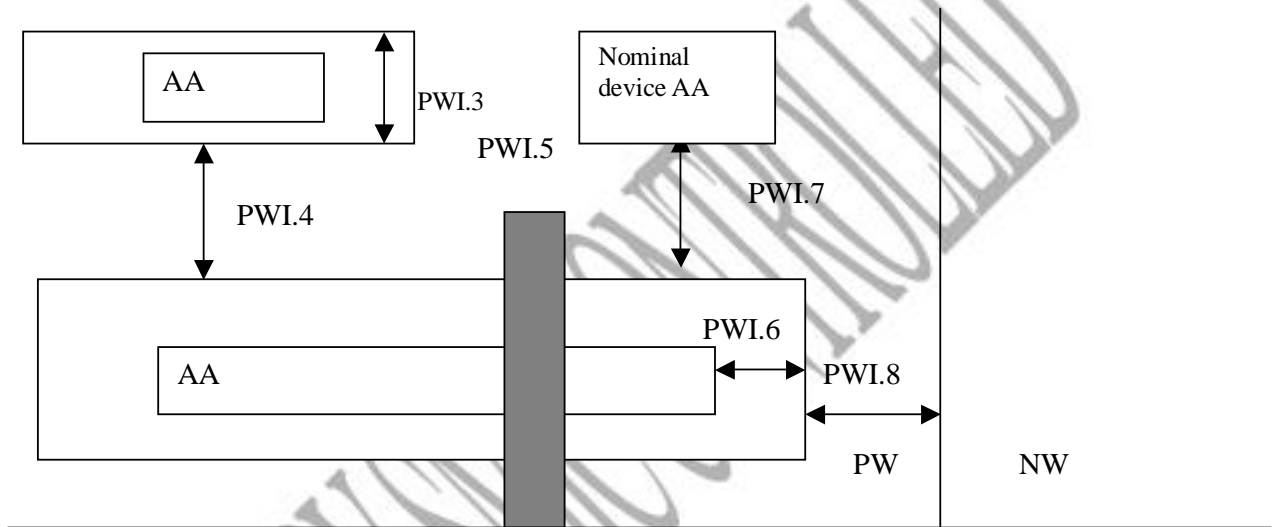# Semiconductor Manufacturing International Corporation

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SL.4a	Suggested maximum space between any two open slots in a coaxial line	35
SL.4b	Suggested minimum space between any two open slots in a coaxial line	10
SL.5a	Suggested maximum clearance between any open slot to the metal edge	35
SL.5b	Suggested minimum clearance between any open slot to the metal edge	10
SL.6	The length of the slot should be parallel to the current flow direction	
SL.7	Minimum clearance between two slots in neighbor layers (for example: M1 slot and M2 slot, M2 slot and M3 slot)	2
SL.8	The starting position of the parallel slots should be staggered	

7.9 ANTENNA/SCRIBE LINE SEAL GUARD RING/ BOND PAD OPENING RULES
Refer to
TD-LO18-DR-2004   0.18 micro LOGIC 1.8/3.3V Antenna Ratio / Scribe Line and Guard Ring Guideline
/ Bond Pad Opening Design Guide Rule
Note: Seal Ring Layout for 0.18um e-EEPROM related mask layer,
   a. DNW(292)/TIM (394)/PFLD(391)/VTNH(396)/TOW(320)/CG(330)/DDD(316)/PLL(113)
       => All Dark
   b. GT(130)/ONO(321)/GP(331) ==>All Clear
   c. Others follow same as those of 0.18um Generic Logic Process.
   d. If seal ring drawn by customer, pls add layer EXCLU for un-DRC purpose in this area
   e.   Customer can also draw the seal-ring by themselves, here will explain how to draw the it .
Notice:
   Customer has two option on seal-ring/scribe lane layout, one is request SMIC/Maskshop help do the

them, the other is do the them by CTM.

Here is the description for customer do the seal-ring layout and scribe lane

    a) If customer's pattern is different from the SMIC standard rule, seal-ring must be drawn by customer themselves.

    b) If customer draw the seal-ring/scribe lane by themselves, the pattern will be treated as main chip for mask manufacture.

Customer how to draw the seal-ring/Scribe lane :

Notice :

1. 0.18um EEPROM provide two kind of scribe lane, one is 60um, the other is 80um, pls kindle select it based on CTM requirement! And inform SMIC before tape out.
2. Only the layers list here are necessary!

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N.O	layer name	GDS	Assemble Isolation	Seal Ring			Scribe lane
				Start X=0	End	Size	
1	AA	10	N/A	0	9.2	9.2	60/80
2	SP	43	N/A	0	9.3	9.3	60/80
3	SAB	48	N/A	N/A	N/A	N/A	60/80
4	CT	50	N/A	1.30	1.56	0.26	N/A
4	CT	50	N/A	3.06	3.32	0.26	N/A
4	CT	50	N/A	4.82	5.08	0.26	N/A
5	M1	61	N/A	0	6	6	N/A
6	V1	70	N/A	2.02	2.38	0.36	N/A
6	V1	70	N/A	3.81	4.17	0.36	N/A
7	M2	62	N/A	0	6	6	N/A
8	V2	71	N/A	1.23	1.59	0.36	N/A
8	V2	71	N/A	3.02	3.38	0.36	N/A
8	V2	71	N/A	4.81	5.17	0.36	N/A
9	M3	63	N/A	0	6	6	N/A
10	V3	72	N/A	2.02	2.38	0.36	N/A
10	V3	72	N/A	3.81	4.17	0.36	N/A
11	M4	64	N/A	0	6	6	N/A
12	V4	73	N/A	1.23	1.59	0.36	N/A
12	V4	73	N/A	3.02	3.38	0.36	N/A
12	V4	73	N/A	4.81	5.17	0.36	N/A
13	M5	65	N/A	0	6	6	N/A
14	V6	74	N/A	2.02	2.38	0.36	N/A
14	V6	74	N/A	3.81	4.17	0.36	N/A
15	M6	66	N/A	0	6	6	N/A
16	PA	80	N/A	N/A	N/A	N/A	60/80
17	PI	82	N/A	N/A	N/A	N/A	60/80

3. N/A means it is not drawn!
4. Space between seal ring and scribe lane is for AR mask logic operation concern in AA layer
5. CT is not suggested for slit type in seal ring, only Via is allowed for slit type
6. If slit type seal ring is necessary, customer MUST draw seal ring.
7. Scribe lane drawing layer size is same as scribe lane size

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7.10 ESD/LATCH-UP PREVENTION LAYOUT GUIDELINES

Refer to

TD-EE18-DR-2005   0.18um e-EEPROM 2P4M(5M/6M) Salicide 1.8v/3.3v/5.0v/15.5v ESD/Latch Up Layout Guide Line

7.11 CURRENT DENSITY RULES

Refer to

TD-LO18-DR-2006   0.18um LOGIC 1P6M Salicide 1.8/3.3V Current Density Design Rules

7.12 Option Layer Drawing Rule

7.12.1 1.8v Native device design rule --- PWI

This dummy layer is used for mask making, for 1.8v native NMOS only. If using 1.8v native NMOS in circuit, PW is generated by reverse tone of NW+DNW+PWI+PSUB+TPW for DRC
(But mask generate, PW is reverse tone of (NW+DNW+PWI+PSUB))

Notice :

1. 1.8V Native device is an optional choice , and it may be different from 0.18 generic Logic. CTM should make careful evaluation before using Native Device.
2. 3.3V native device is not allowed.

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RULE NO.	DESCRIPTION	LAYOUT RULE (Unit in um)
		1.8V
PWI.1	PWI inside or cross over a N-WELL is not allowed	
PWI.2	PWI MUST be surrounded by PW	
PWI.3	Minimum dimension of PWI region	0.84
PWI.4	Minimum space between 2 PWI region	0.84
PWI.5	Minimum GP as gate dimension of 1.8V native device	0.50
PWI.6	Minimum and Maximum PWI enclosure beyond SN (N+) AA region	0.26
PWI.7	Minimum space from a PWI region to a normal AA region.	0.52
PWI.8	Minimum space from a PWI region to N-well edge	1.62
PWI.9	Bent gate poly is not allowed to put in PWI region	
PWI.10	P+ region is not allowed to put in PWI region	
PWI.11	Only one AA region is allowed to put in PWI region	
PWI.12	Minimum space from a PWI region to DNW edge	4.0
PWI.13	GT is not allowed in PWI	
PWI.14	NLL/SN MUST be drawn for Native device	

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7.12.2 HRP DESIGN RULES

This layer is used to define high resistance poly region.

RULE NO.	DESCRIPTION	LAYOUT GUIDELINE (Unit in μm)
HRP.1	It is strongly suggest that resistor square number > 5 for precision Rs	
HRP.2	Minimum extension from HRP region beyond a PO resistor region	0.26
HRP.3	Minimum clearance from HRP region to GT/GP of NMOS	0.32
HRP.4	Minimum clearance from HRP region to GT/GP of PMOS	0.32
HRP.5	Minimum and maximum P+ implant for pickup overlap with SAB	0.30
HRP.6	Minimum extension from SAB region beyond a PO resistor region	0.22
HRP.7	Minimum width of Poly region for high resistance poly resistor	2.00
HRP.8	Dummy layer "HRPDMY" is needed for DRC for high resistance Poly region	
HRP.9	For contact rule, please follow Logic baseline rule	
HRP.10	It is not allowed to receive SN , and all LDD implant in the HRP region.	
HRP.11	HRP only drawn in NW or PW	

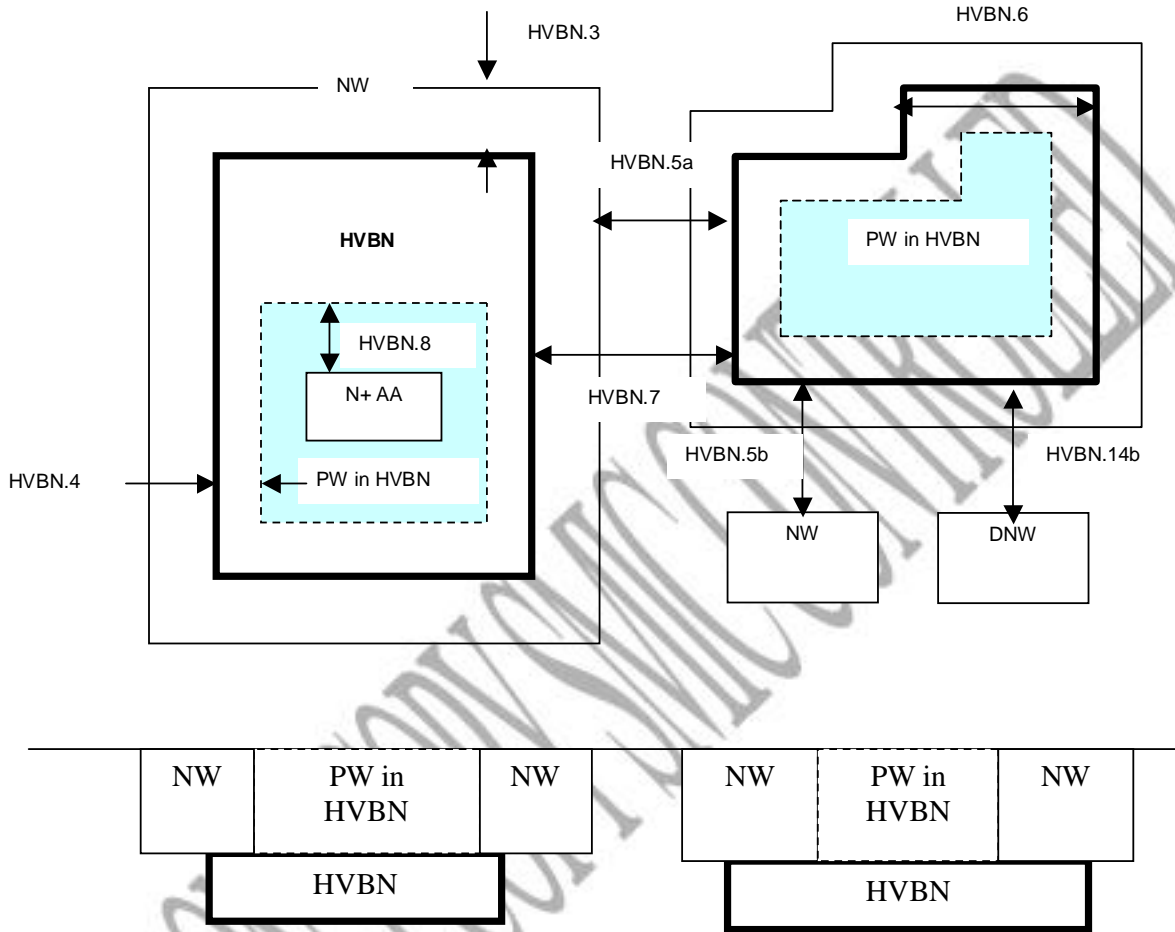**Semiconductor Manufacturing International Corporation**

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7.12.3 MIM DESIGN RULES

The MiM modules of 0.18um EEPROM process adopt TM-1/MIM/TV/TM layers. The MiM Structure is placed within top metal and previous 1 metal.

The (TM) layout layer is drawn to define the last Metal layer, which is M3 for 2P3M process.
The (TM) layout layer is drawn to define the last Metal layer, which is _M4_ for _2P4M_ process.
The (TM) layout layer is drawn to define the last Metal layer, which is _M5_ for _2P5M_ process.
The (TM) layout layer is drawn to define the last Metal layer, which is _M6_ for _2P6M_ process.

RULE NO.	DESCRIPTION	LAYOUT GUIDELINE (Unit in μm)
MiM.1	Minimum width of MiM region as top plate	4.00
MiM.2	Minimum space between two MiM regions as top plate.	1.20
MiM.3	Minimum extension of MiM region beyond a Via which connect to this MiM	0.50
MiM.4	Minimum extension of bottom plate (Mn-1) region on a MiM region	0.50
MiM.5	MiM region cross bottom plate (Mn-1) Metal region is not allowed	
MiM.6	Maximum dimension of a MiM region as capacitor top metal If capacitor lager than 30*30,please use combination of smaller capacitor	30.0
MiM.7	Maximum dimension of a bottom metal (Mn-1) region in capacitor If capacitor lager than 35*35,please use combination of smaller capacitor	35.0
MiM.8	Minimum density of MiM pattern. Dummy MiM pattern suggested 2X 5μm with line space 1.5μm is required if density less than 3% Notice:	3%
MiM.9	1. Active devices under MiM are not preferred. However, when active devices (AA, CT, Via, metal layers) are used under MiM, it should follow the guideline: a) MiM/Mn-1 as bottom plate and tie to fixed voltage. (i.e. GND or Vcc or Vss…) b) Designer must re-run circuit simulation with the extra parasitic	

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capacitance from Mn-1/ lower Mn layers. Make sure the AC performance is acceptable.

MiM.10	Minimum extension of capacitor bottom metal beyond Via connect to Mn	0.20
MiM.11	Minimum clearance of a top Via to MiM region	0.50
MiM.12	Minimum space between two Via on MiM	2.00
MiM.13	Minimum space between two Via on bottom metal (Mn-1)	1.00
MiM.14	Minimum width of dummy MiM region	0.60
MiM.15	Minimum space of dummy MiM to MiM region	0.80
MiM.16	Minimum space of dummy Mn-1 to Mn-1	0.80
MiM.17	Minimum space of MIM capacitor bottom(metal) Mn-1 with VIA to below all metal layers	2.00
MIM.18	The MIM structure is placed within top metal and next 1 metal	

ESD2 DESIGN RULES ： MiM(Capacitor Top plate)

： Capacitor bottom plate or Dummy

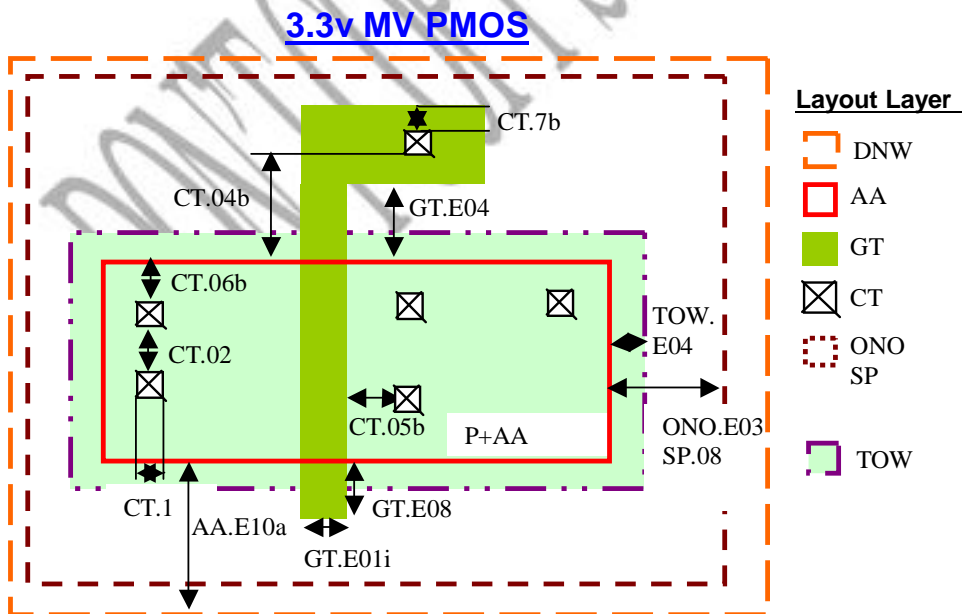# Semiconductor Manufacturing International Corporation

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ESD2 is only for customer self-define ESD implant, if customer need do the ESD implant based their own design, pls use this layer to define the ESD region.

Notice : If customer define ESD condition by themselves, pls inform SMIC related information for process run.

RULE NO.	DESCRIPTION	LAYOUT GUIDELINE (Unit in μm)
ESD2.1	Minimum width of ESD2 region	0.44
ESD2.2	Minimum space between two ESD2 regions.	0.44

7.12.5   ESD3 DESIGN RULES

ESD3 is only to SMIC/Design Service for some special I/O design.

RULE NO.	DESCRIPTION	LAYOUT GUIDELINE (Unit in μm)
ESD3.1	Minimum width of ESD3 region	0.44
ESD3.2	Minimum space between two ESD3 regions.	0.44

7.12.6   HVBN DESIGN RULES

HVBN function is same as 0.18um MM DNW which is used to isolate the PW of 1.8v NMOS from the substrate.

Only 1.8v Vcc is allowed to force on the NW, which is connected to the HVBN.

RULE NO.	DESCRIPTION	LAYOUT GUIDELINE (Unit in μm)
HVBN.1	HVBN must be surrounded by NW	
HVBN.2	It's not allowed to use HVBN layer as resistor	
HVBN.3	Minimum extension of NW beyond HVBN	1.50
HVBN.4	Minimum overlap of NW onto HVBN	2.00

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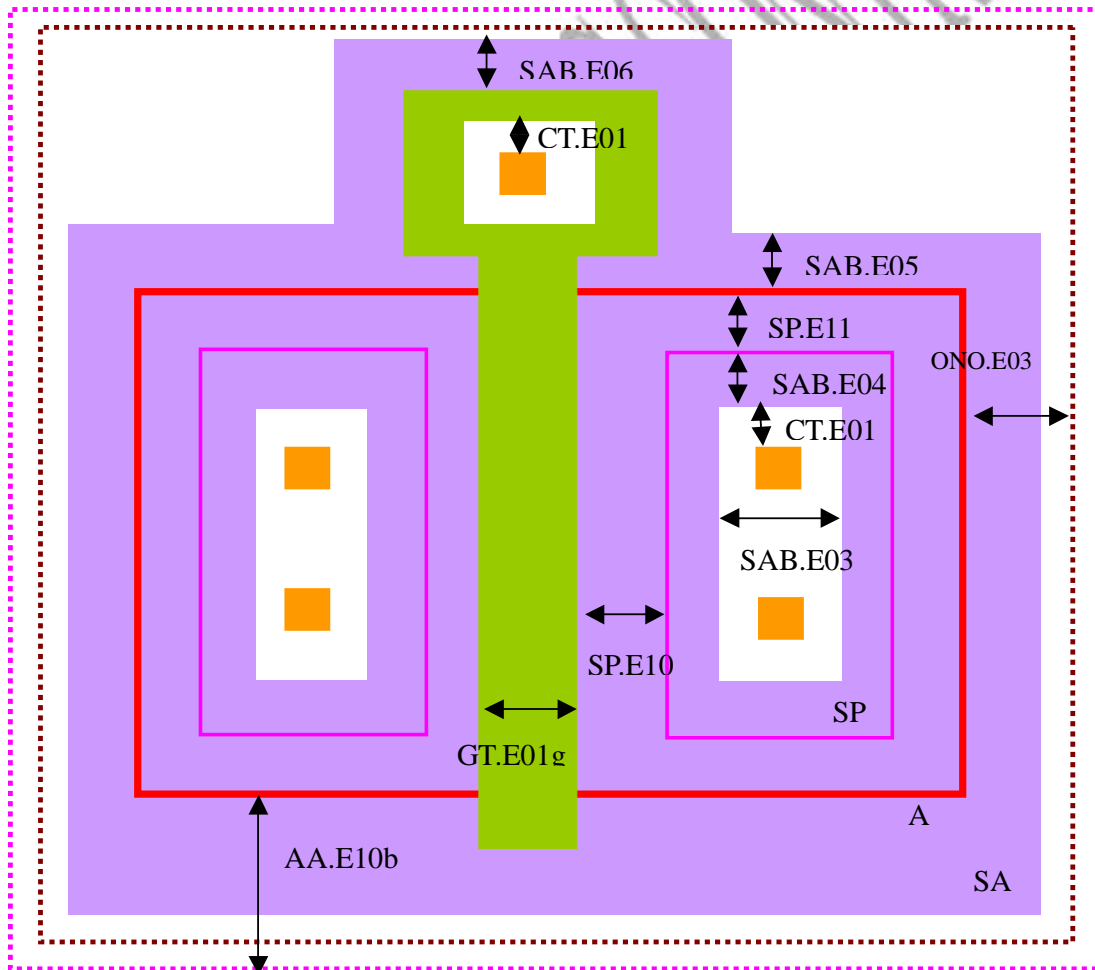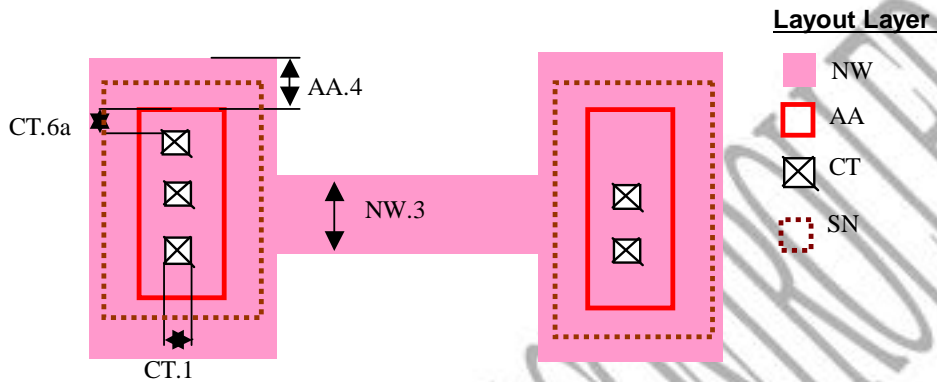| HVBN.5a	Minimum clearance from HVBN to NW, which is connected to un-related HVBN	3.00
HVBN.5b	Minimum clearance from HVBN to NW, which is not connected to any HVBN	5.00
HVBN.6	Minimum width of a HVBN region	3.00
HVBN.7	Minimum space between 2 HVBN regions	5.00
HVBN.8	Minimum clearance from NW edge to a N+ AA region is outside a NW when HVBN is implemented	0.50
HVBN.9	Recommend to keep NW connected to HVBN be in reverse bias for lower leakage application	
HVBN.10	It's not allowed to use NW connect to HVBN as resistor	
HVBN.11	TPW must be fully outside of HVBN	
HVBN.12	PWI must be fully outside of HVBN	
HVBN.13	Psub must be fully outside of HVBN	
HVBN.14a	DNW must be fully outside of HVBN	
HVBN.14b	Minimum space of DNW to HVBN which is connected with NW	8

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Cross Section for NW, PW within HVBN, and HVBN

where

PW in HVBN:

NW:

HVBN:

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7.13 Device Layout Examples
   SMIC provide device layout examples for user's reference.
   1. User is RECOMMENDED to follow the guideline to design devices.
   2. The design rules otherwise stated follow those previously listed.
   3. User is RECOMMENDED to inform SMIC first if other special device design is adopted
7.13.1 Transistors
   7.13.1.1   1.8v NMOS

1.8v-NMOS

7.13.1.2   1.8v PMOS

1.8v-PMOS

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7.13.1.3   3.3v special MV NMOS

3.3v MV NMOS

7.13.1.4   3.3v special MV PMOS

3.3v MV PMOS

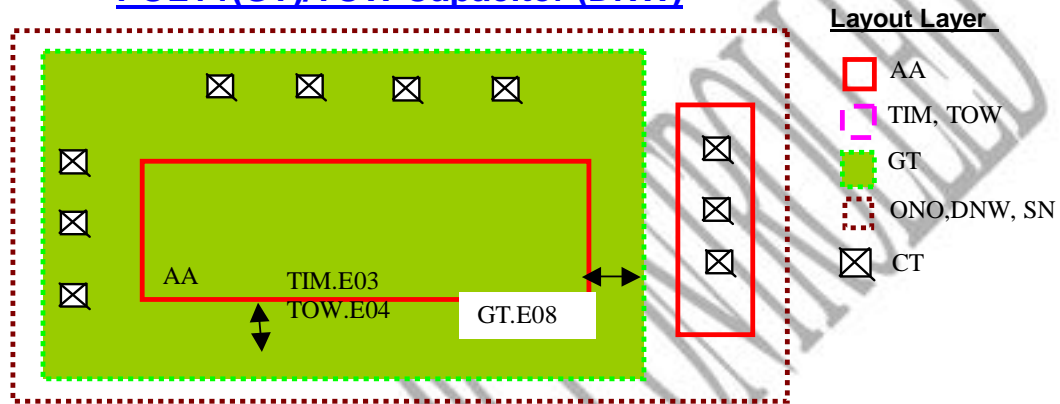Semiconductor Manufacturing International Corporation

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7.13.1.5   5v/15.5v HV NMOS, D/S DDD

5v/15.5v HVNMOS

7.13.1.6   5v/15.5v HV ZMOS, D/S DDD

5v/15.5v HVZMOS

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7.13.1.7   5v Quasi-HVPMOS

5v Quasi-HVPMOS

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7.13.1.8   16v Real-HVPMOS

Layout Layer

- DNW
- AA
- GT
- ONO
- SP
- SAB
- CT

16v Real-HVPMOS

7.13.2 Resistors

7.13.2.1 NW Resistor (under STI)

NW Resistor (STI)

7.13.2.2 TIM Resistor

TIM Resistor

RULE NO.	DESCRIPTION	LAYOUT RULE
RES.1	Minimum TIM extension GT for TIM resistor	0.3
RES.2	GT must be drawn for TIM resistor	
RES.3	TIM resistor GT gate and low-voltage terminals are tied together to minimize gate modulated resistance variation.	

TIM Resistor (inside PSUB)

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7.13.3 Capacitors

7.13.3.1   Buried N+ POLY1 (GT) /TOW Capacitor

Buried N+
POLY1(GT)/TOW Capacitor (DNW)

Layout Layer

- AA
- TIM, TOW
- GT
- ONO,DNW, SN
- CT

AA   TIM.E03   TOW.E04   GT.E08

Notice:
   Buried N+ POLY1(GT)/TOW Capacitor(DNW) is an optional device
   PLS kindly take care of isolatin if this device used

7.13.3.2   POLY2 (CG) /ONO/POLY1(GT), P-i-P Capacitor

PIP ONO Capacitor

RULE NO.	DESCRIPTION	LAYOUT RULE
	PIP.01 – PIP.08 extra rule for PIP (w/i SAB & Partial SAB)	
PIP.01	Minimum CG width for PIP ONO capacitor	5
PIP.02	Minimum space of CT to Poly2(CG) or Poly1(GT) edge	0.35
PIP.03	Minimum enclosure of Poly1(GT) to Poly2(CG)	0.35
PIP.04	Minimum CG extension GT	0.35
PIP.05	Maximum CG width for PIP ONO capacitor	40

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PIP.06	Space of CT to CT for PIP	0.40
PIP.07	CT on CG which stack on GT is forbidden	
PIP.08	If GT, CG of PIP must be fully covered by SAB	
	Minimum and Maximum of CT (w/i SAB)width	0.36
	PIP.09 – PIP11 extra rule only for PIP (Partial SAB) needed	
PIP.09	Minimum and Maximum of CT width	0.22
PIP.10	Space of CT to SAB	0.22
PIP.11	Width of SAB enclosure GT or CG	0.25

POLY2(CG)/ONO/POLY1(GT) Capacitor

Layout Layer

GT

CG

CT

Notice : PIP.07 CT on CG which stack on GT is forbidden

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POLY2(CG)/ONO/POLY1(GT) Capacitor(w/i SAB)

Layout Layer

- GT
- CG
- ONO, SN
- CT
- SAB

PIP.06

PIP.04

SP

SP.E06b

POLY2(CG)/ONO/POLY1(GT) Capacitor(Partial SAB)

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7.13.3.3　　Stack Psub/POLY2 (CG) /ONO/POLY1(GT), Stack_P-i-P Capacitor

RULE NO.	DESCRIPTION	LAYOUT RULE
	Below extra rule is used for Stack PIP TOW & Stack PIP HVGOX capacitor	
SPIP.01	Min/Max CT w/o SAB block	0.22
SPIP.02	SAB extention/enlosure CG	0.40
SPIP.03	CT on CG to GT under CG	0.40
SPIP.04	AA enclosure TOW	0.30
SPIP.05	CT to CT	0.40
SPIP.06	GT enclosure TOW	0.30
SPIP.07	CG overlap GT	0.35
SPIP.08	GT extension related AA	0.35
Suggestion	Max GT length under CG	5.00

Notice : Stack_PIP is a new device, is operation voltage had better be lower than 3.3v

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Stack _PIP　TOW Capacitor

Layout Layer

- ONO/SN/HVPF/Psub
- TIM
- CG
- CT
- AA
- GT
- TOW
- SAB

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Stack_PIP   HVGOX Capacitor

Layout Layer

- ONO/SN/HVPF/Psub
- TIM
- CG
- CT
- AA
- GT
- SAB

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Doc. No.: TD-EE18-DR-2002	Doc. No.:	0.18um e-EEPROM 2P3M (4M/5M/6M) Salicide 1.8V/3.3V/5.0V/15.5V Process Layout Design Rule	Doc.Rev: 11T	Tech Dev Rev: 0.9	Page No.: 131/135

7.13.4 BJT

7.13.4.1 1.8v- vertical BJT

Notice : BJT layout GDS in 0.18um EEPROM 2P4M Salicide 1.8/3.3/5/15.5V SPICE Model (Version 1.3) (TD-EE18-SP-2001)
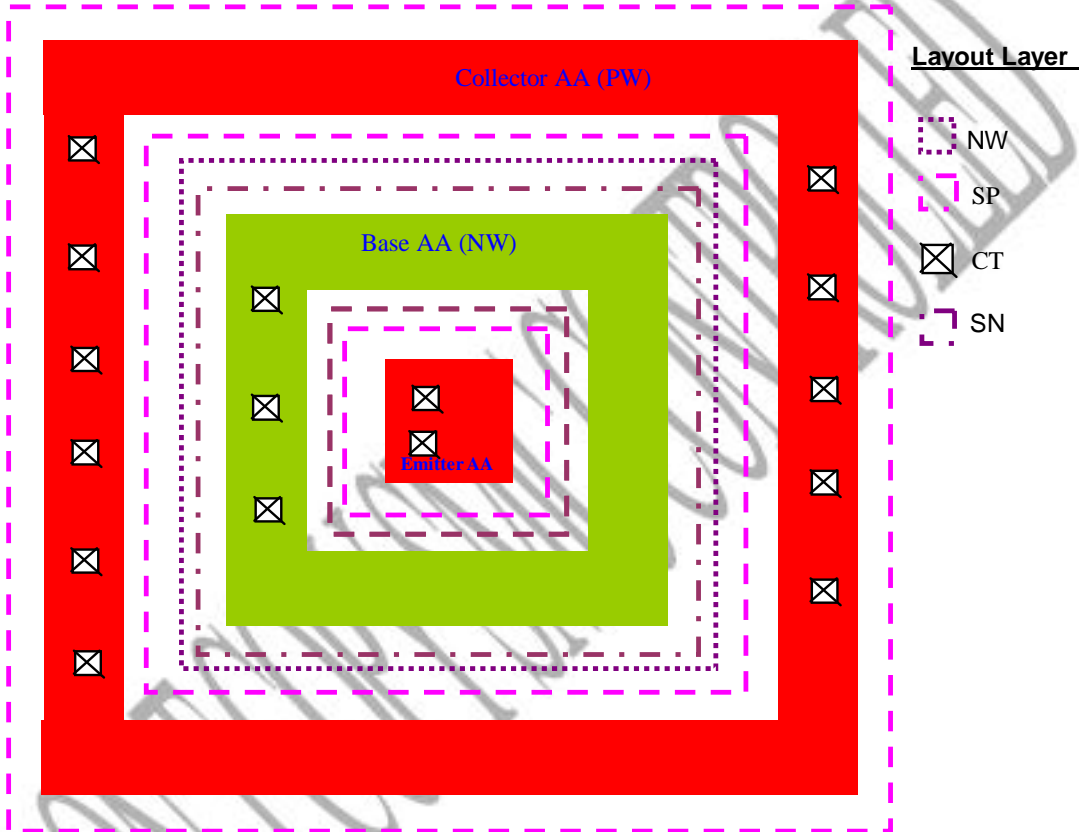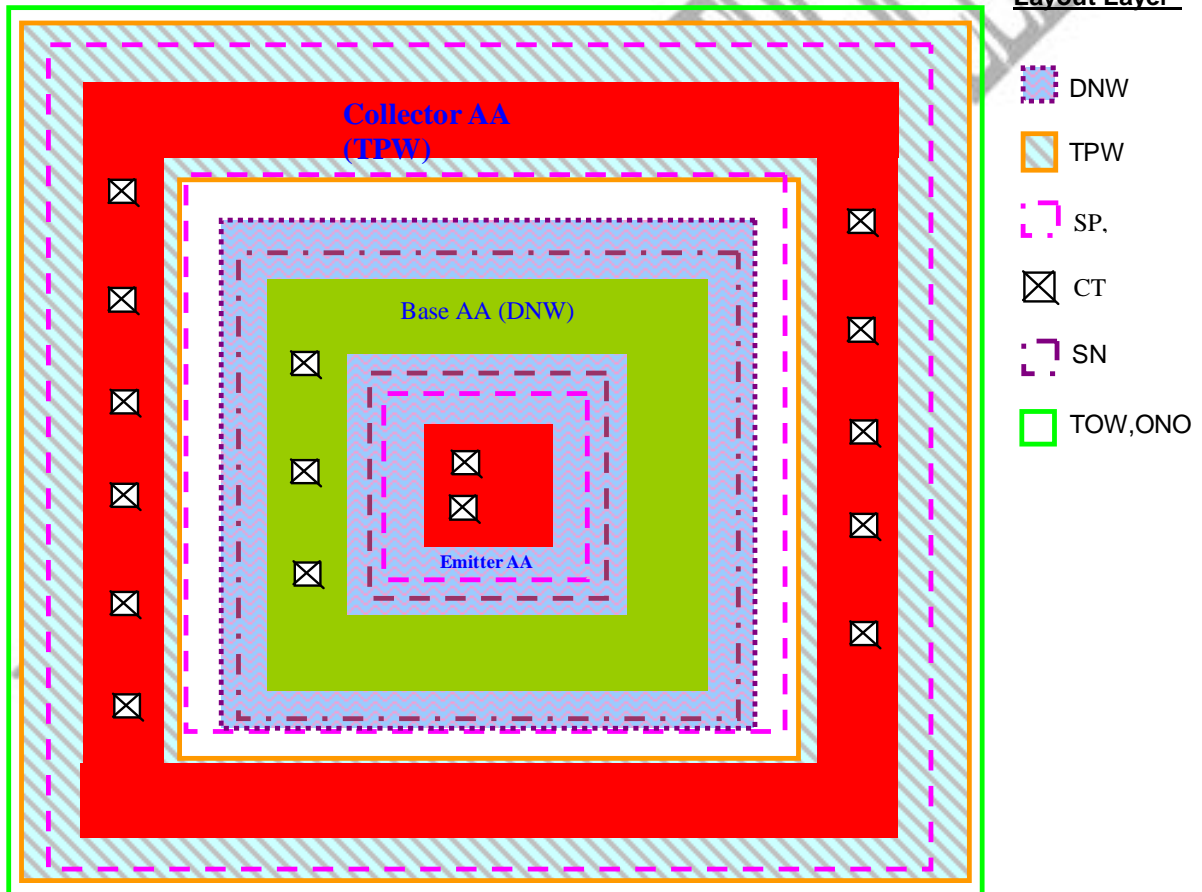
v-BJT

RULE NO.	DESCRIPTION	LAYOUT RULE
BJT18.01	Emitter AA width must be for v-BJT emitter	2.0/5.0/10.0
BJT18.02	Emitter AA must in NW	
BJT18.03	Collector AA width	2.0
BJT18.04	Base AA width	1.5
BJT18.06	SP enclosure emitter AA	0.35
BJT18.07	SP for emitter AA to base AA	0.65
BJT18.08	SN enclosure base AA	0.35
BJT18.09	SN for base AA to emitter AA	0.65
BJT18.10	SP enclosure collector AA	0.4
BJT18.11	SP for collector AA to base AA	1.1
BJT18.12	NW to collector AA	1.0
BJT18.13	NW enclosure base AA	0.5

Notice : All BJT rule is fixed value, pls follow it.

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v-BJT (P+/NW/PW)

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Doc. No.: TD-EE18-DR-2002	Doc. No.:	0.18um e-EEPROM 2P3M (4M/5M/6M) Salicide 1.8V/3.3V/5.0V/15.5V Process Layout Design Rule	Doc.Rev: 11T	Tech Dev Rev: 0.9	Page No.: 133/135

7.13.4.2   3.3v- vertical BJT

Notice : BJT layout GDS in 0.18um EEPROM 2P4M Salicide 1.8/3.3/5/15.5V SPICE Model (Version 1.3) (TD-EE18-SP-2001)

v-BJT

RULE NO.	DESCRIPTION	LAYOUT RULE
BJT33.01	Emitter AA width must be for v-BJT emitter	2.0/5.0/10.0
BJT33.02	Emitter AA must in DNW	
BJT33.03	Collector AA width	1.03
BJT33.04	Base AA width	1.5
BJT33.05	Collector AA to base AA	1.5
BJT33.06	Base AA to emitter AA	1.0
BJT33.07	DNW enclosure base AA	0.5
BJT33.08	DNW to collector AA	1.0
BJT33.09	TPW enclosure collector AA	1.0
BJT33.10	TPW to base AA	0.5
BJT33.11	SN enclosure AA	0.2
BJT33.12	SP enclosure AA	0.2

Notice : All BJT rule is fixed value, pls follow it.

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v-BJT (P+/DNW/TPW)

Layout Layer

- DNW
- TPW
- SP,
- CT
- SN
- TOW,ONO

Collector AA (TPW)

Base AA (DNW)

Emitter AA

7.13.5 1.8v Native device --- PWI

Native Device(1.8V NMOS)
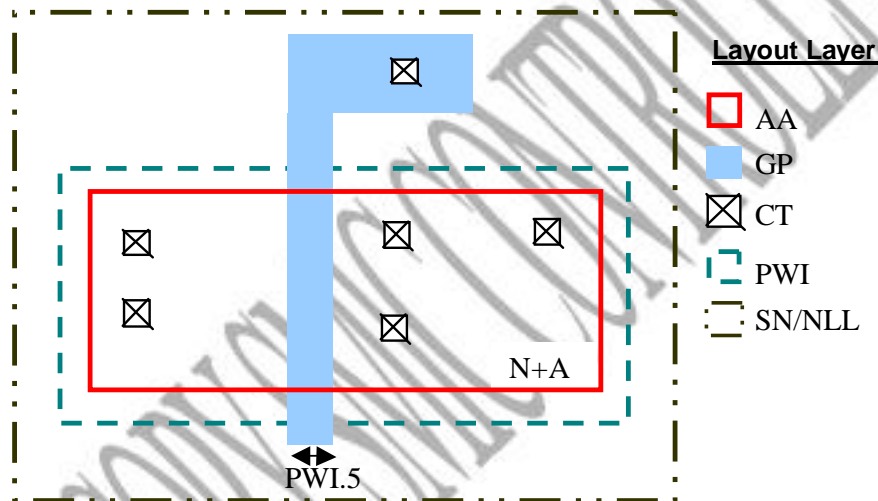
7.13.6 SRAM

SMIC library provide two type SRAM : Poly-Cross and Metal-Cross, Metal-Cross type SRAM is suggested, especially when customer adopt 2.88um^2 size EECell.
(SMIC provide two type EECell, one cell size is 3.96um^2, the other one is 2.88um^2)

Notice: If CTM have concern on two type SRAM meaning, pls contact with SMIC Design service department.

8.   Attachments:

8.1   Examples of device layout mentioned above
GDSII files:
SMIC_18EE_1.8vRealHV_DeviceExamples_V3p0.gds

8.2   Layer mapping file
ASCII file:
SMIC_18EE_MAP_V3p0.map