Voltage Scaling on 8 × 8 Wallace Tree Multiplier

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Abstract – The aim of this project is to implement a Wallace Tree multiplier, and improve its performance by voltage scaling. A baseline multiplier has been implemented with 3:2 compressors and RCA(Ripple Carry Adder). For scaling voltage purpose, further optimized multiplier with pipelining and CSA(Carry Selection Adder). In order to explore Cadence tools, while gaining better circuit performance, all the blocks are fully customized. Results for scaling voltage could be seen in part 8.

Keywords – Wallace Tree, Voltage Scaling, Pipelining

1 – Introduction

Multiplier, as a function unit in most modern CPU, significantly increases the critical path in naive 1-stage CPU. Even in 5-stage pipelining, with multiplier residing in EX stage, the long delay of multiplier could cause unbalanced pipelining, and, worst case, will choke the pipeline.

However, from circuit aspect, a lower operation voltage is expected, which could save a great amount of energy. This may accentuate the long delay problem of a multiplier, for propagation delay of a circuit will increase as operation voltage decreases.

CRISTA[1] is a novel method in voltage scaling, without hurting the circuit performance. This is done by isolating the critical paths, with a small predictor to detect input vectors. For critical paths, the pipeline is stalled for 1 cycle, allowing 2-cycle operation on a small set of inputs. The predictor, in this report, is implemented with CSA.

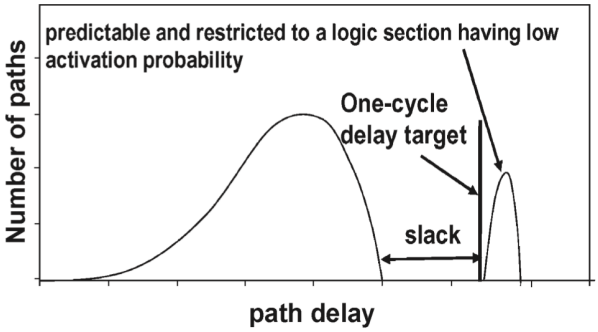

Fig.1 – Path delay distribution required for CRISTA[1]

2 – Wallace Tree Architecture

Fig.2 shows the top level architecture for a general Wallace Tree Multiplier. The multiplier first takes 2 sets of 8-bit inputs (A[7:0] & B[7:0]), and generates 64 partial products. Then, the compression tree, as well as RCA, adds up the partial products, and outputs the final 16-bit result (S[15:0]).

In Fig.2, the Registers consist of D Flip Flops, while Partial Product Generator consists of AND gates. Compression Tree and RCA are implemented with Full Adders.

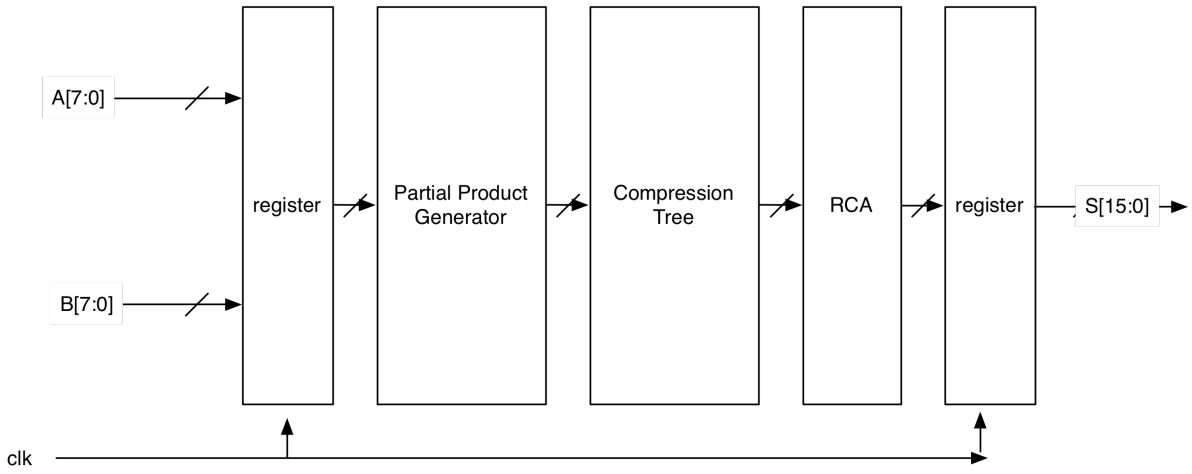

Fig.2 – Wallace Tree multiplier, top view architecture

3 – TSMC180 Testing & Sizing

Before proceeding to layout, it's necessary to test the technology and decide the size of the standard inverter. At one aspect, a large Wp:Wn is desired, to get a similar rise time and fall time. Yet, a large Wp:Wn ratio would affect trip point, thus decrease noise margin. Moreover, it would significantly waste area.

From testing standard inverter driving 4X inverter, it showed that Wp:Wn=3.3 would yield the same rise time and fall time, which is, taking Lamda into consideration, (Wp, Wn) = (855nm, 270nm). Yet, from engineering point of view, (Wp, Wn)=(540nm, 270nm) is enough to achieve a fair performance.

4 – Elementary Block Design

a, Mirror Adder

The Mirror Adder has symmetric PMOS and NMOS chains, which could reduce diffusion capacitance. Also, mirror adder could be optimized for carry calculation, in both sizing and placing close to output. Since carry out is driving 3 pairs of gates, carry calculation part should be 3 times standard sizing of an inverter. As in Fig.3.

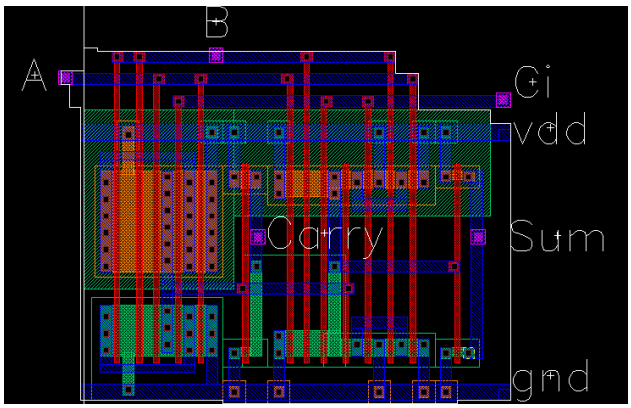

Fig.3 – Mirror adder layout

b, Positive Edge Triggered D-FF

Master-Slave edge triggered D Flip Flop is consist of 4 transmission gates. With the complementary property, signal D could be transmitted to Q, without losing much. Based on simulation, standard sizing is enough to have a reasonable output. As in Fig. 4.

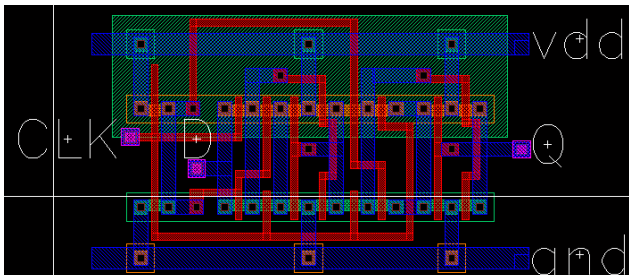

Fig.4 – D Flip Flop layout

5 – Functionality Verification

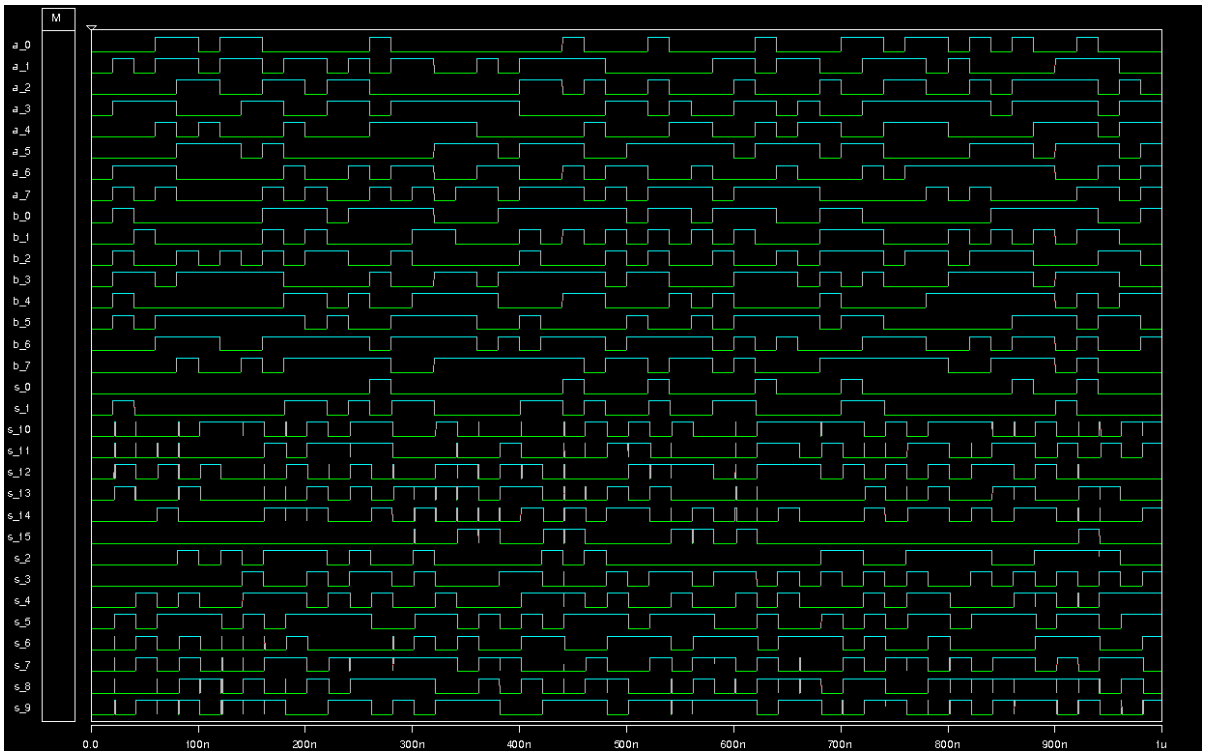

Fig.5 – Waveform for functionality verification
(Top down: A_0->A_7, B_0->B_7, S_1*->S_2->…->S_9, T/2=10ns)

6 – Voltage Scaliing

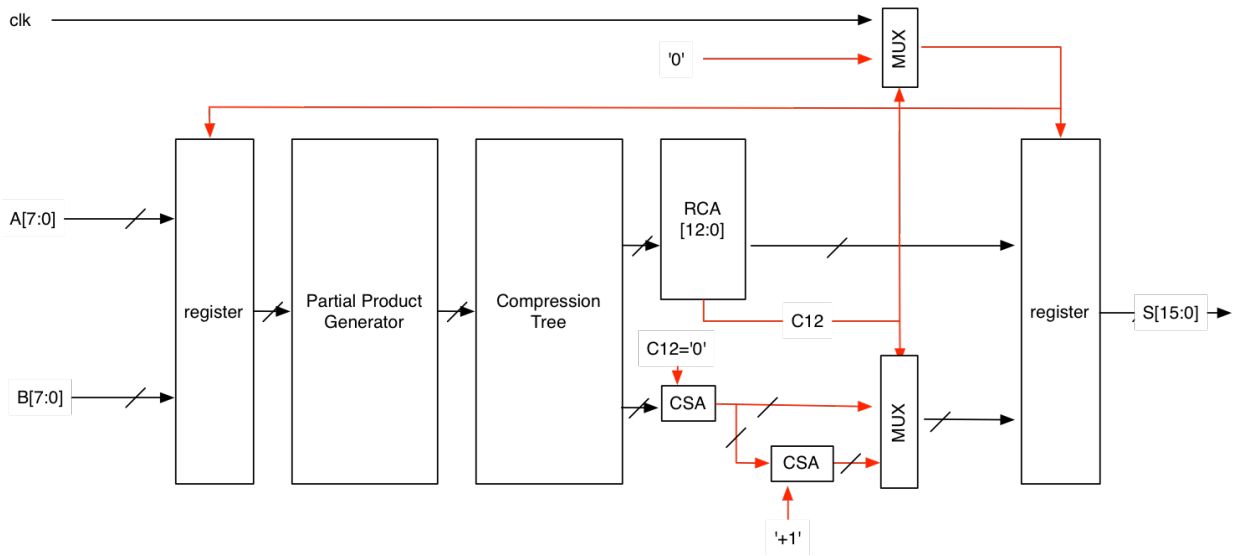

Fig.6 – Architecture for Wallace Tree multiplier with CSA

The top view architecture for Wallace Tree multiplier, with CSA being predictor, is as Fig.6. Once the 12th carry-in is '1', which means the carry needs more time to propagate, the clock signal is disabled for 1-cycle. In this way, the critical path is extended to 2-cycle operation. Also, it is obvious that the probability for 12th carry-in to be '1' is fairly smaller than the lower carry-ins to be '1'. The physical layout is as Fig.7. The elements in the red circle indicate the CSA.

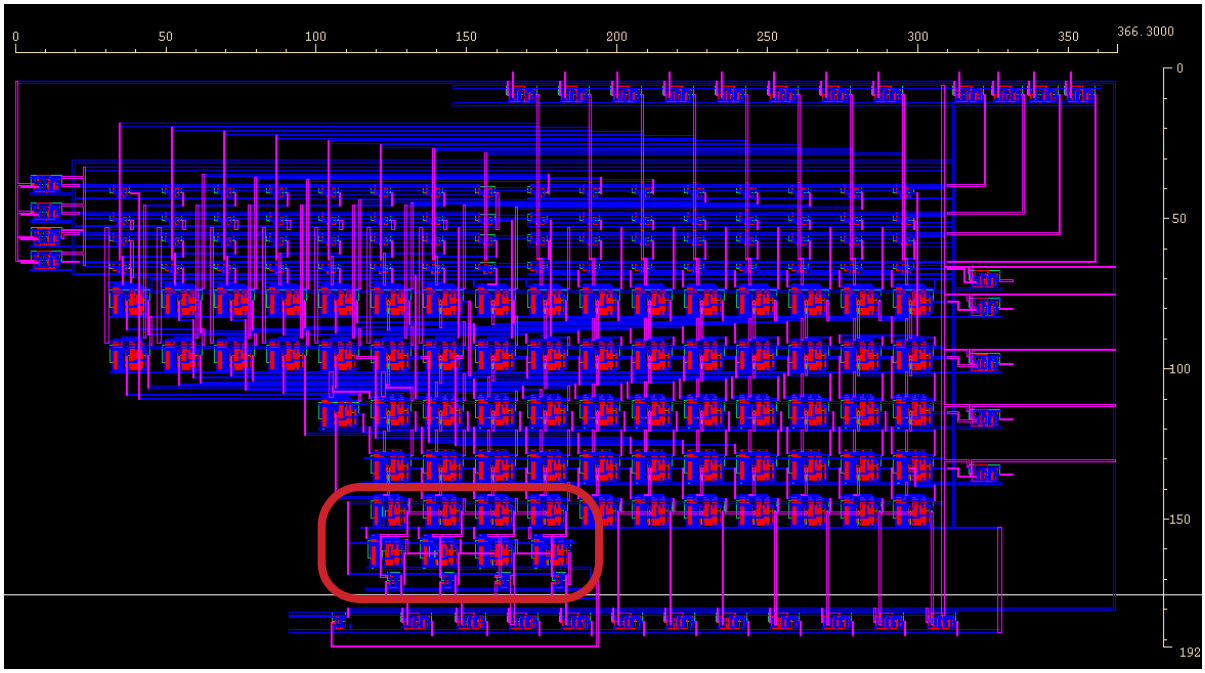

Fig.7 – Layout for Wallace Tree multiplier with CSA

7 – Library Parameters (extracted)

	AREA(um^2)	Propagation Delay(ns)
AND	7.0200*5.1750	0.08
D-FF	10.7550*6.6150	0.14
FA	14.5800*11.4300	0.1
MUX	6.3900*6.3450	0.0295
Wallace Tree Logic	293.5800*147.4650	—
Top View	366.3000* 191.6550	—

Table 1 – Library parameters for extracted module

8 – Average Block Power (uW)
(white cells have correct outputs)

T/2	1.8V	1.6V	1.4V	1.2V	1.0V	0.8V
10ns	567.680593	422.759080	287.932771	193.450077	132.2995177	5.472986
5ns	1071.397585	801.269362	543.870471	73.417674	14.374521	5.877144
1ns	1848.915762	474.667701	91.748834			
0.75ns	2361.836201	506.599569				
0.6ns	2599.614430 (glitch)					
0.5ns	2442.004098 (failure in upper 4 bits)					

Table 2 – Voltage scaling results

9 – Possible Optimizations

Further optimizations could be done, with more time:

a, pin buffer
Pin buffer could decrease capacitance, which could result a decrease in total delay.

b, power(ground) well
Since long power line has voltage drop, a power well may be a better solution on a large system. A power well may have 4 VDD pins in each side of the chip.

c, clock tree
Clock tree could reduce clock skew, introduced by long interconnect wires.

10 – Development Directory

Logic design and layout:
559mg27/cadence/project
Netlist and simulation:
559mg27/cadence/nanosim

11 – Reference

[1] Swaroop Ghosh et.al -CRISTA: IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol. 26, No. 11, November 2007

[2] S. Ghosh and K. Roy, "Exploring high-speed low-power hybrid arithmetic units at scaled supply and adaptive clock-stretching," in ASP- DAC '08: Proceedings ofthe Asia and South Pacific Design Automation Conference, pp. 635–640, IEEEComputer Society Press, 2008

[3] Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, "Digital Integrated Circuits, A Design Perspective, 2nd Edition"