a) selected signal assignment statement

library IEEE;

use IEEE.std\_logic\_1164.all;

entity mux is

port(I0,I1,I2,I3,C,D: in std\_logic;

F: out std\_logic);

end mux;

architecture behavior of mux is

singal q: std\_logic;

begin

q<= C&D;

with q select

F <= I0 after 10ns when "00";

I1 after 10ns when "01";

I2 after 10ns when "10";

I3 after 10ns when "11";

end behavior;

b) Conditional

library IEEE;

use IEEE.std\_logic\_1164.all;

entity mux4 is

port(I0,I1,I2,I3,C,D: in std\_logic;

F: out std\_logic);

end mux4;

architecture behavior of mux41v3 is

signal q: in std\_logic\_vector;

q<=c&d;

begin

x <= I0 when (q="00") else

I1 when (q="01") else

I2 when (q="10") else

I3;

end behavior;

c) Case and process

library IEEE;

use IEEE.std\_logic\_1164.all;

entity mux4 is

port(I0,I1,I2,I3,C,D: in std\_logic;

F: out std\_logic);

end mux4;

architecture behavior of mux41v3 is

begin

process(C,D)

begin

case CD is

when "00" =>

F <= I0;

when "01" =>

F <= I1;

when "10" =>

F <= I2;

when "11" =>

F <= I3;

end case;

end process;

end behavior;

Problem 2

a) library ieee;

use ieee.std\_logic\_1164.all;

entity 74194 is

port (clrb : in std\_logic; clk : in std\_logic;

s1, s0 : in std\_logic; SDR, SDL : in std\_logic;

D : in std\_logic\_vector(3 downto 0);

Q : out std\_logic\_vector(3 downto 0));

end 74194;

architecture behavior of 74194 is

signal temp : std\_logic\_vector(3 downto 0);

begin

process(clrb, clk)

begin

if (clrb = '0') then

temp <= "0000";

elsif (clk'event and clk = '1') then

if (s1 = '1' and s0 = '1') then

temp <= D;

elsif (s1 = '1' and s0 = '0') then

temp <= SDR & temp(3 downto 1);

elsif (s1 = '0' and s1 = '1') then

temp <= temp(2 downto 0) & SDL;

end if;

end if;

end process;

end behavior;

b) library ieee;

use ieee.std\_logic\_1164.all;

entity shift8 is

port (CLRb : in std\_logic; clk : in std\_logic;

s1, s0 : in std\_logic; RSD, LSD : in std\_logic;

X : in std\_logic\_vector(7 downto 0);

Y : out std\_logic\_vector(7 downto 0));

end shift8;

architecture behavior of shift8 is

component 74194 is

port (clrb : in std\_logic; clk : in std\_logic;

s1, s0 : in std\_logic; SDR, SDL : in std\_logic;

D : in std\_logic\_vector(3 downto 0);

Q : out std\_logic\_vector(3 downto 0));

end component;

signal T0, T1 : std\_logic\_vector(3 downto 0);

begin

U1 : 74194 port map(CLRB, CLK, s1, s0, RSD, T0(3), X(7 downto 4), T1);

U2 : 74194 port map(CLRb, clk, s1, s0,

T1(0), LSD, X(3 downto 0), T0);

Y(7 downto 4) <= T1;

Y(3 downto 0) <= T0;

end behavior;

