## ECE 4250/ 7250: VHDL and Programmable Logic Devices Laboratory

**Lab # 1**

**Lab Title: Design Simulation using MODELSIM**

**Group# 8**

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**Teaching Assistant Use Only:**

**Points Earned Reasons for Deduction**

**Pre-lab:**

**Post Lab report**:

**Demonstration:**

**Final Lab Grade:**

**Comments to students:**

# Objective

To familiarize with the process of simulation and verification of VHDL code using Model sim

# Lab Work

### **VHDL code for Full Subtractor**

library IEEE; --including library

use IEEE.std\_logic\_1164.all;

entity Fs is --Defining Entity

port(A,B,Bi: in std\_logic; -- I/O ports

D,Bo: out std\_logic);

end Fs;

Architecture model of Fs is --Architecture

begin

D <= A xor B xor Bi after 10 ns;

Bo <= (not A and B) or (B and Bi) or (not A and Bi);

end model;

### **VHDL code for 6 bit Subtractor**

library IEEE; --including library

use IEEE.std\_logic\_1164.all;

entity sub6 is --entity

port(A,B: in std\_logic\_vector(5 downto 0); --I/O ports

Bi:in std\_logic;

D:out std\_logic\_vector(5 downto 0);

Bo:out std\_logic);

end sub6;

Architecture Full of sub6 is -- Architecture

component Fs -- Components

port(A,B,Bi: in std\_logic;

S,Bo: out std\_logic);

end component;

signal C: std\_logic\_vector(5 downto 1); --Internal signals

begin

FS1: Fs port map (A(0),B(0),Bi,D(0),C(1)); --Instances of Full subtrator

FS2: Fs port map (A(1),B(1),C(1),D(1),C(2));

FS3: Fs port map (A(2),B(2),C(2),D(2),C(3));

FS4: Fs port map (A(3),B(3),C(3),D(3),C(4));

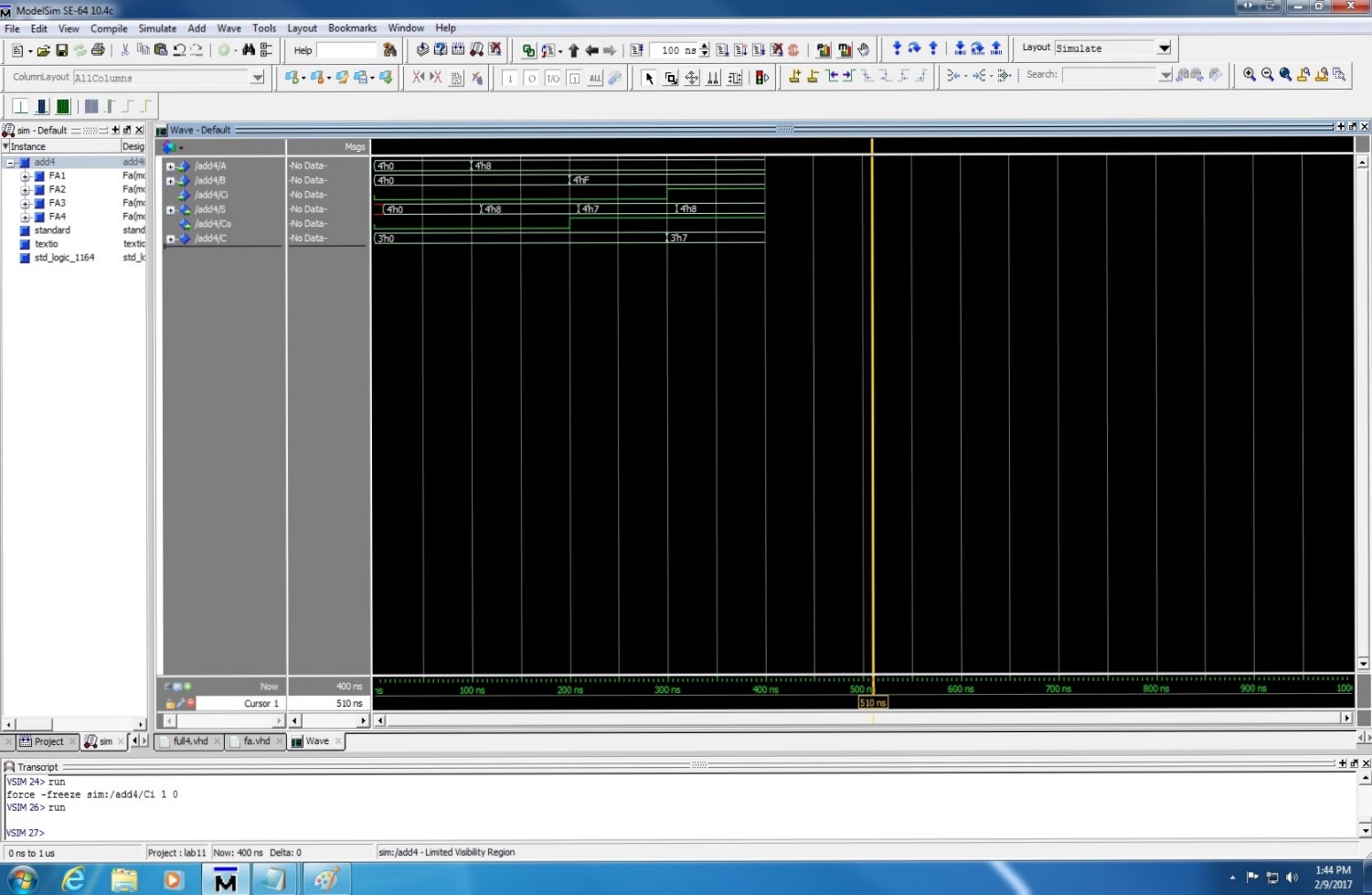
FS5: Fs port map (A(4),B(4),C(4),D(4),C(5));

FS6: Fs port map (A(5),B(5),C(5),D(5),BO);

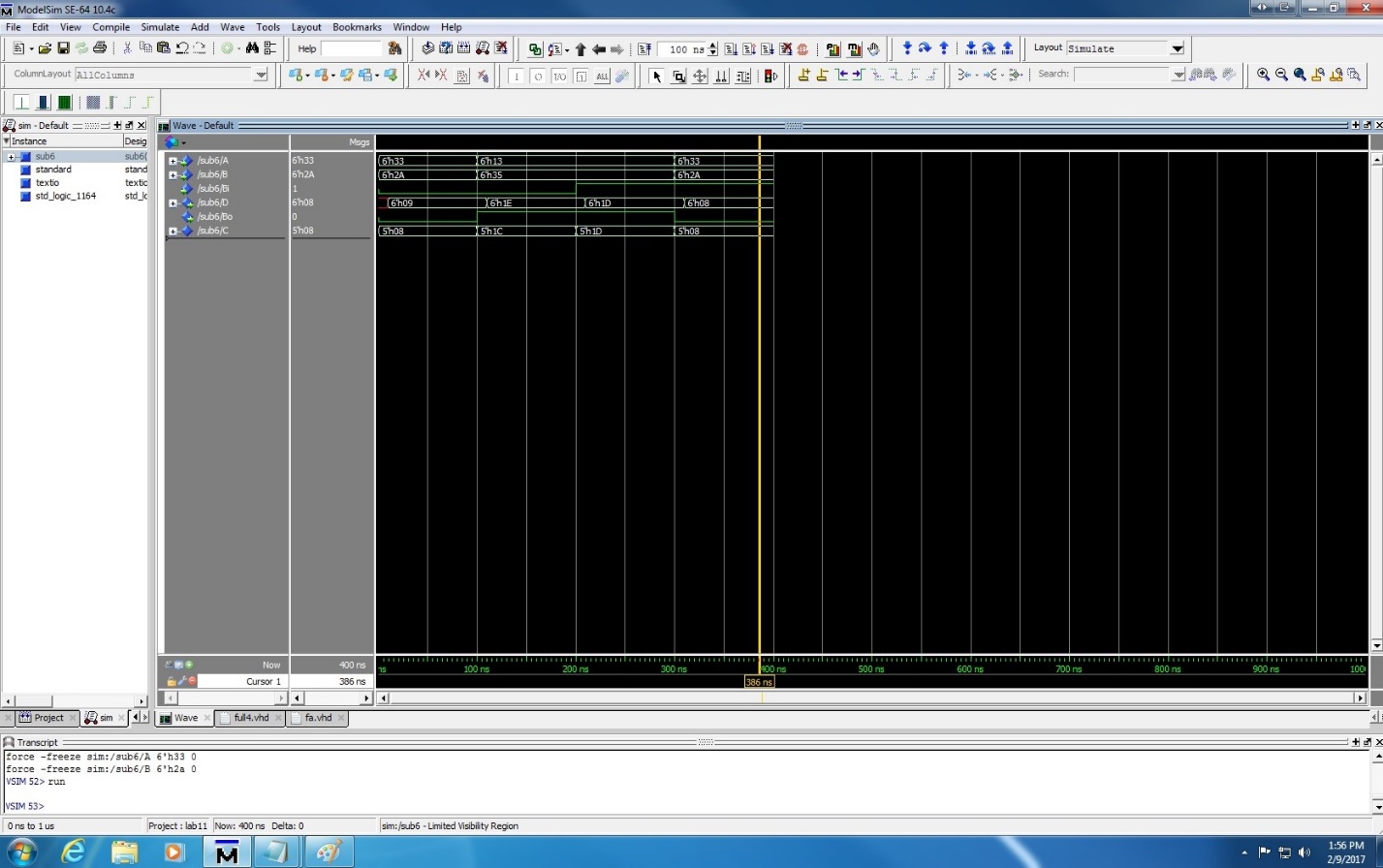
end Full;

**Screenshots**

**4 bit Full adder**



**6 bit Subtractor**



**Answers**

**3.** **Briefly describe about the function and the syntax of port-map statements? For example, in our Adder4.vhd, why does the order have to be port map (A(0),B(0),Ci, C(1),S(0))?**

1. The ports in a component declaration must usually match the ports in the entity declaration one-for-one. The component declaration defines the names, order, mode and types of the ports to be used when the component isinstanced in the architecture body.

Instancing a component implies making a local copy of the corresponding design entity - a component is declared once within any architecture, but may be instanced any number of times

Syntax

Component\_name port map(I/O ports);

The statement mentioned above matches the ports of an instance of full adder.

**5. What is the difference between entity, architecture and component? How are they used in this project?**

1. An entity is a real interface to a design unit which can have multiple architectures. An entity defines how stuff gets in and out, while the architecture defines how the design unit operates

A component is an ideal or "virtual" design unit.

# Conclusion

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We had learnt how to use Model Sim and to simulate VHDL programs