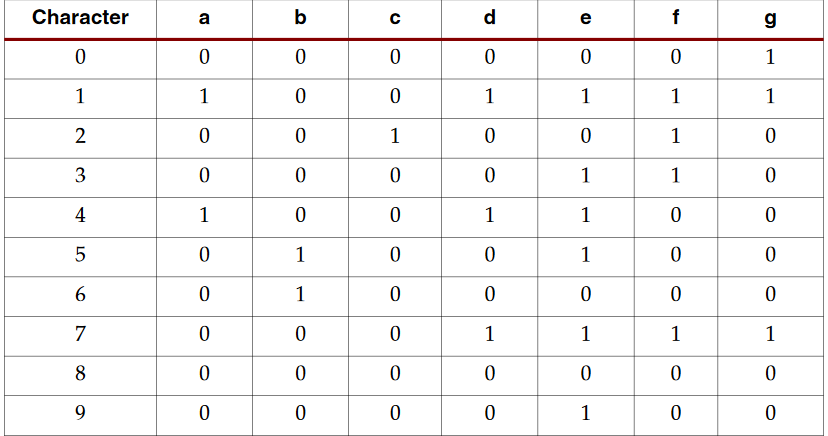
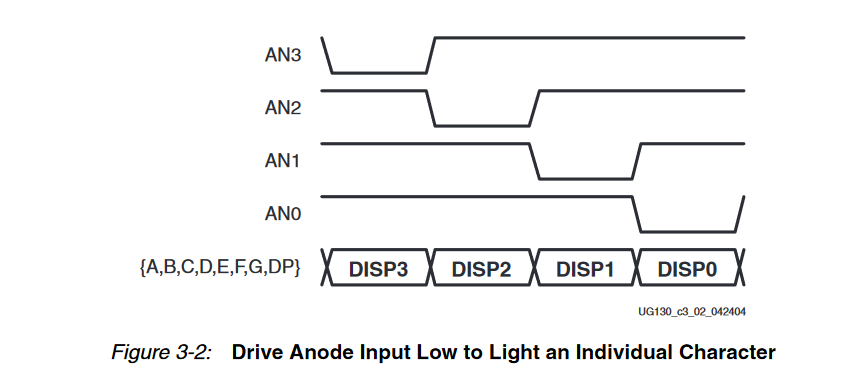
Prelab3:

1. i. 4 bits programmed like this ： 

Scanning technique:



Advantage: The scanning technique reduces the required I/O down to 12 pins.

Disadvantage: the FPGA logic must continuously scan data out to the displays

1. ucf: Co is wrong. It should not be T9. It should be clock.