## ECE 4250/ 7250: VHDL and Programmable Logic Devices Laboratory

**Lab # 6**

**Lab Title: Simulation the Design Using Test Bench**

**Group# 8**

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**Teaching Assistant Use Only:**

**Points Earned Reasons for Deduction**

**Pre-lab:**

**Post Lab report**:

**Demonstration:**

**Final Lab Grade:**

**Comments to students:**

# Objective

To learn the VHDL modeling of a State Machine. We take the traffic light controller as the example and simulate our design using ModelSim and Xilinx Project Navigator.

# Lab Work

### **VMBehave.vhd**

library IEEE;

use IEEE.std\_logic\_1164.all;

entity traffic\_light is

PORT (clk, PB: in std\_logic;

Ga, Ya, Ra, WALK, NOWALK: out std\_logic);

END traffic\_light;

architecture behave of traffic\_light is

signal clk1: std\_logic;

signal state,n\_state: integer range 0 to 18;

signal counter : integer range 0 to 3;

signal pb\_i: std\_logic ;

signal rst: std\_logic := '1' ;

component GenClock is

Generic(t\_p : integer range 1 to 4 );

Port (clk: in std\_logic;

Clock: out std\_logic);

End component;

begin

c1: GenClock generic map(2) port map (clk,clk1);

process(clk1)

begin

if(clk1 = '1' and clk1'event) then

case state is

when 14 to 17 => state <= n\_state;

when others => if (counter = 3) then state <= n\_state; counter <= 0;

else counter <= counter +1;

end if;

end case;

end if;

end process;

process(clk,rst)

begin

if(clk = '1' and clk'event) then

if(PB = '1' and rst ='1') then

pb\_i <= '1';

elsif(PB = '0' and PB = '1' and rst = '0') then

pb\_i <= '0';

else pb\_i <= pb\_i ;

end if;

end if;

end process;

process(state,pb\_i)

begin

Ga<='0';

Ya<= '0';

Ra<='0';

WALK <= '0';

NOWALK <= '0';

case state is

when 0 to 7 => Ga <= '1'; NOWALK <='1'; n\_state <= state+1;

when 8 => if(pb\_i = '1' ) then Ya <= PB;NOWALK <= '1'; n\_state <= state+1; rst <= '0';

else Ga <= '1'; n\_state <= 8; NOWALK <='1' ;

end if;

when 9 to 13 => Ra <= '1'; WALK <= '1'; n\_state <= state+1;

when 14 => Ra<= '1'; WALK <= '1'; n\_state <= state+1;

when 15 => Ra<= '1'; WALK <= '0'; n\_state <= state+1;

when 16 => Ra<= '1'; WALK <= '1'; n\_state <= state+1;

when 17 => Ra<= '1'; WALK <= '0'; n\_state <= state +1;

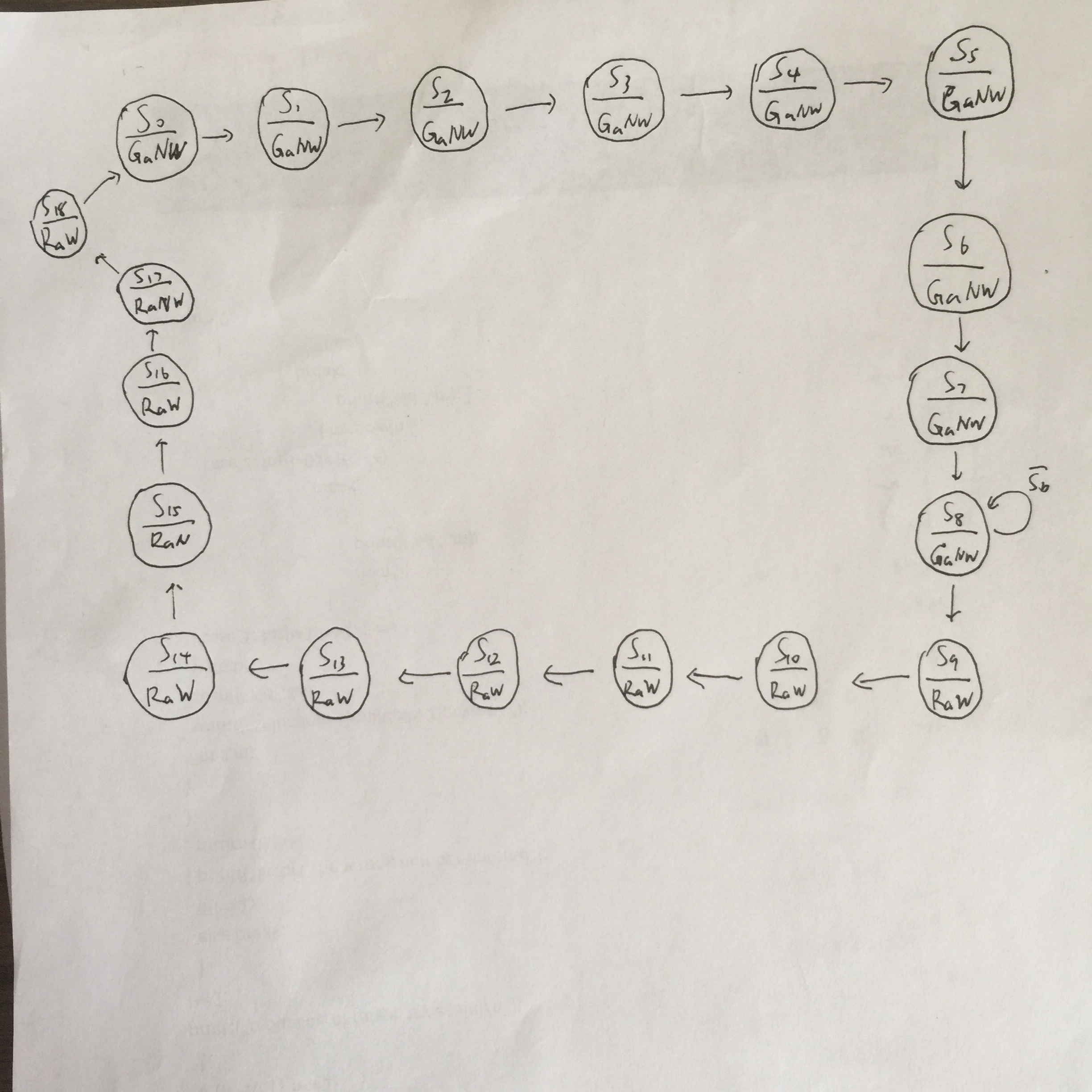
when 18 => Ra<= '1'; WALK <= '1'; n\_state <= 0;

end case;

end process;

end behave;

**State Transition Diagram**



# Conclusion

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We had learnt modeling a VHDL state machine by designing a traffic light controller. We simulate traffic light successfully by using Modelsim and Xilinx Project Navigator.