Zheng Zhao

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Education

University of Texas at Austin (UT Austin), Austin, TX, U.S. *Sep '15 - May '20 (Expected)*
Ph.D., Electrical and Computer Engineering, **GPA:** 4.0/4.0
Advisor: David Z. Pan

Shanghai Jiao Tong University (SJTU), Shanghai, China *Sep '12 - May '15*
M.S., Electrical and Computer Engineering, **GPA:** 3.9/4.0

Tongji University, Shanghai, China *Sep '08 - Jul '12*
B.S., Electrical and Computer Engineering, **GPA:** 4.8/5.0

Professional Experience

Cadence Design Systems, Inc., Austin TX. U.S. *May '19 - Aug '19*
Software Intern: C++ buffer insertion engine runtime and result improvement
- Improved 40%-60% runtime on commercial benchmarks with speed-up techniques including library caching & pruning, memory pool, data structure and program flow refactoring
- Developed Python quality-of-result (QoR) analyzer for algorithmic guidance

Nvidia Corporation, Austin TX. U.S. *May '16 - Aug '16*
Research Intern: highlevel synthesis (HLS) for design space exploration
- Studied C++ writing style for highlevel synthesis QoR
- Implemented ALU units using C++ template metaprogramming
- Tested and debugged commercial HLS software, verified on ALU and commercial benchmarks

Research Experience

Logic Synthesis for Emerging Technologies, UT Austin & SJTU *Sep '15 - Present*
- Developed C++ optical logic synthesizer and achieved 27× power efficiency by binary decision diagram transformation and polynomial programming approximation based on Gurobi Solver [Zhao+, ASPDAC '18]
- Improved utility by 30% by hypergraph partitioning based on hMETIS hypergraph package and min-cost max-flow modeling based on LEMON graph library [Zhao+, DATE '19]
- Developed C logic synthesizer for SET array and stochastic computing [Zhao+, ICCAD '15; DATE '16]

Hardware-software Co-design of Optical Neural Network, UT Austin *Sep '18 - Present*
- Designed and implemented slimmed optical neuromorphic computing architecture based on TensorFlow
- Reduced 40% utility and enhanced robustness [Zhao+, ASPDAC '19; Arm Invited Talk '19]

Complete list of 20+ publications can be found in my Google Scholar profile.

Computer Skills

Languages: C/C++, Python (TensorFlow, PyTorch), Bash, Verilog, LaTeX
Tools: Boost C++ Libraries; LEMON graph library; Hypergraph partitioning package (hMETIS); Gurobi Solver; Eigen C++ library

Courses

Taken: Algorithm Analysis and Theory, Advanced Algorithms, Engineering Programming Language Methods of Applied Mathematics, Engineering Optimization, Database, Microprocessor Principle
TA-ed: Introduction to Computing Systems (Prof. Yale Patt), Programming and Data Structures, Introduction to Embedded Systems

Selected Awards

Cadence Women in Technology Scholarship, Cadence Design Systems, Inc. *2019*
UT Austin Graduate Student Fellowship, University of Texas at Austin *2015-2019*
Best Paper Award, Hardware Oriented Security and Trust (HOST) *2017*
Richard Newton Young Student Fellow Award, Design Automation Conference (DAC) *2016*
National Scholarship, Ministry of Education, P. R. China *2009-2011*