

开关电源电磁兼容分析和设计技术

EMC Analysis and Design Technology of a Switched Mode Power Supply



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08, 16, 2018

本资料相应课程可在电子研习社APP上观看，更多精品好课推荐

陈为 - 功率变换器磁元件高频化的挑战与对策

- 磁元件高频化带来的理论和实际问题
- 磁芯的高频损耗及特性
- 绕组的高频损耗分析及特性
- 磁性元件的优化设计
- 高频阵列化磁性元件

陈桥梁 - 功率半导体器件应用及电源设计

- 常用功率半导体器件的基本原理及特性对比分析
- 功率MOSFET的开关过程分析及EMI整改策略
- 功率MOSFET关键参数解读及选型原则
- 功率MOSFET在电源中的应用案例分析
- 基于几种典型电路仿真软件的电源设计

邵革良 - 精通反激电源变压器及电路设计

- 反激电源的类型与特点
- 精通反激电源设计的关键
- 反激电源变压器计算方法
- 反激电源变压器计算实例讲解
- 反激电源变压器的绕线制作技巧

徐强华 - 电子产品的电磁兼容设计

- 电磁兼容基础
- 电子产品的电磁兼容性设计
- 电磁兼容测试技术
- 用户现场的EMC问题
- 常见问题及解决方法

傅强 - 电子电路基础知识讲座

- 电子电路设计基础知识
- 晶体管电路设计
- 运放应用基础
- 电力MOSFET开关
- 电源管理

李义 - 开关电源EMC设计实用技术

- 开关电源电磁兼容特性
- 开关电源EMC接地信号分析
- 线制非隔离系统设计考虑
- 两线制隔离系统设计考虑
- E接地系统设计考虑

陈为 - LLC电路磁元件分析及设计技术

- LLC电路的基本工作原理
- LLC电路磁元件的特点
- LLC电路磁元件损耗分析与绕组设计
- LLC电路磁元件的磁集成技术
- LLC电路磁元件的电磁干扰特性

黄敏超 - 电磁兼容理论设计与整改实践

- 电磁兼容基本概念
- EMI 电磁干扰法规、理论与整改篇
- EMS 电磁抗干扰法规、理论与整改篇
- EMC设计与整改的展望



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内容

第1节：开关电源电磁兼容设计的挑战

第2节：开关电源电磁干扰发射测试

第3节：开关电源传导干扰形成机理及模型

第4节：传导干扰的抑制设计

EMI滤波器设计

无Y电容变压器设计

其它新型抑制方法

第5节：总结和讨论



和军平

哈尔滨工业大学（深圳）
副教授

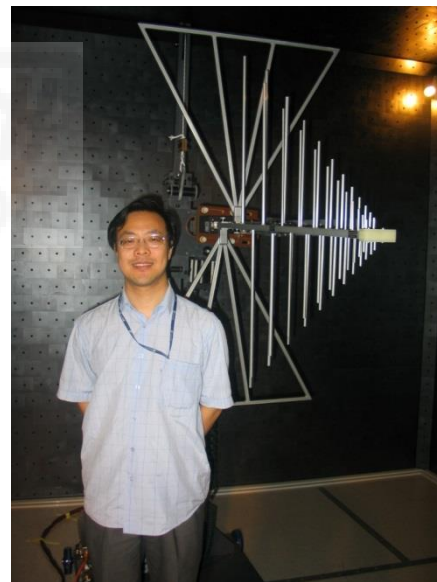
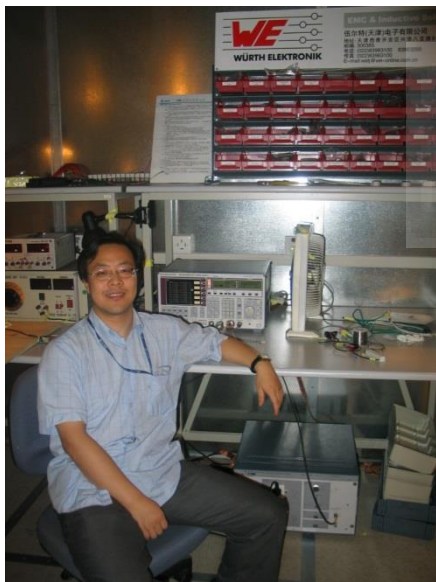
教育经历：

2003年—2005年 博士后（电气工程），清华大学、台达DPEC
1999年—2003年 获博士学位（电气工程），清华大学

研究方向：

电力电子电磁兼容，电力电子技术

- 1) 国家自然科学基金资助项目：2项
- 2) 深圳市科技计划：3项
- 3) 企业EMC课题项目：10多项
- 4) IEEE-EMC、ECCE, PESC, 电机工程学报发表论文80多篇、国内外专利7项



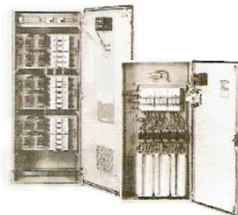
第1节：开关电源的电磁兼容设计挑战

开关变换技术功能灵活、效率高、体积小，在国民经济中应用广泛！

新能源逆变发电



电力系统交/直流输调电：



电力传动：电力机车、电动车

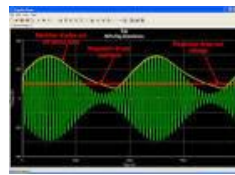
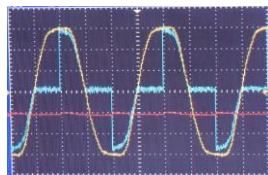


开关电源：UPS、A2D、D2D

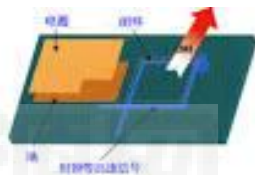


开关变换也不可避免地产生负面效应

电能质量问题：谐波、电压波动、电压暂降等



干扰负载及邻近设备：高速信号线、电机轴电流



降低自身稳定可靠性和抗扰性：模/数控制电路



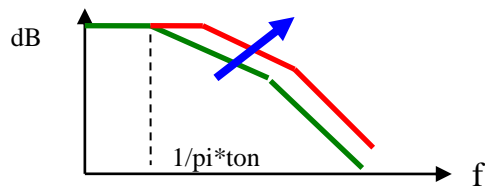
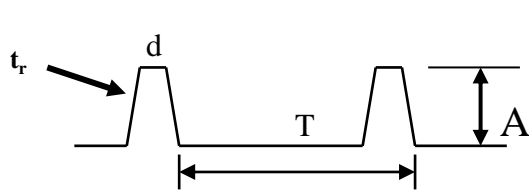
形成无线电干扰：辐射超标



危害电磁环境：家居、汽车内、新能源电场



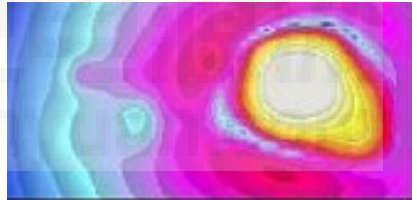
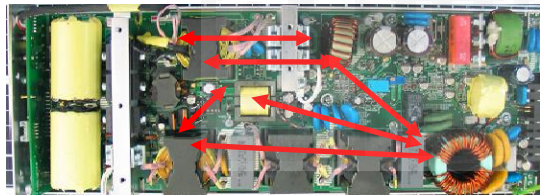
更高的工作频率、更高的V, i, dv/dt 、 di/dt , 更强高频频谱!



10MHz/1MMz

更强的 EMI 源

更小的体积, 更强的电磁耦合, 更加复杂电磁干扰形成和传播!



更多互联/串并联开关电子设备, 电磁干扰时空随机分布更复杂!



更大的挑战!

开关电源电磁兼容

电源对外界不产生电磁干扰（EMI）
能承受一定的外界的电磁干扰（EMS）

电子产品电磁兼容认证：FCC（美），CCC（中国），CE（欧洲）

电磁
兼容
认证
测试

电磁干扰发射测试（EMI）

低频：电能质量
中频：传导发射
射频：辐射发射

.....

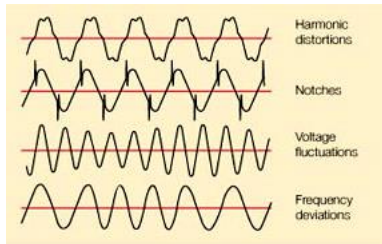
抗电磁干扰能力测试（EMS）

时域测试：雷击、静电
频域测试：射频干扰

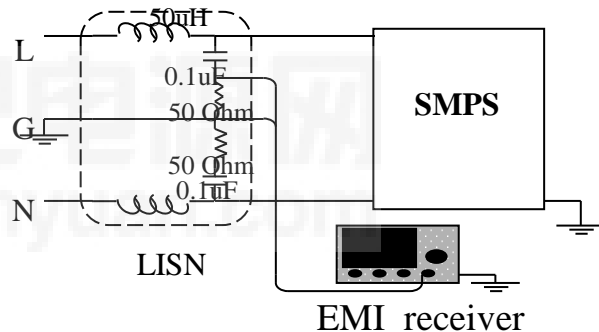
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干扰的频率范围分为低频、传导频段、辐射频段

谐波 (Low frequency, 50Hz及其谐波)



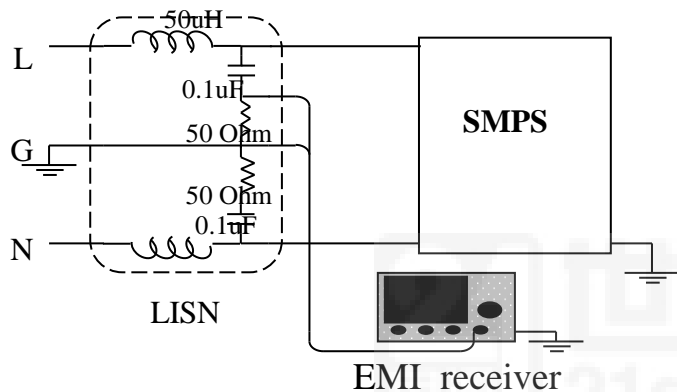
传导 (middle frequency, 9k-30MHz)



感应和辐射 (Middle-Radiated frequency)



测试原理和布局



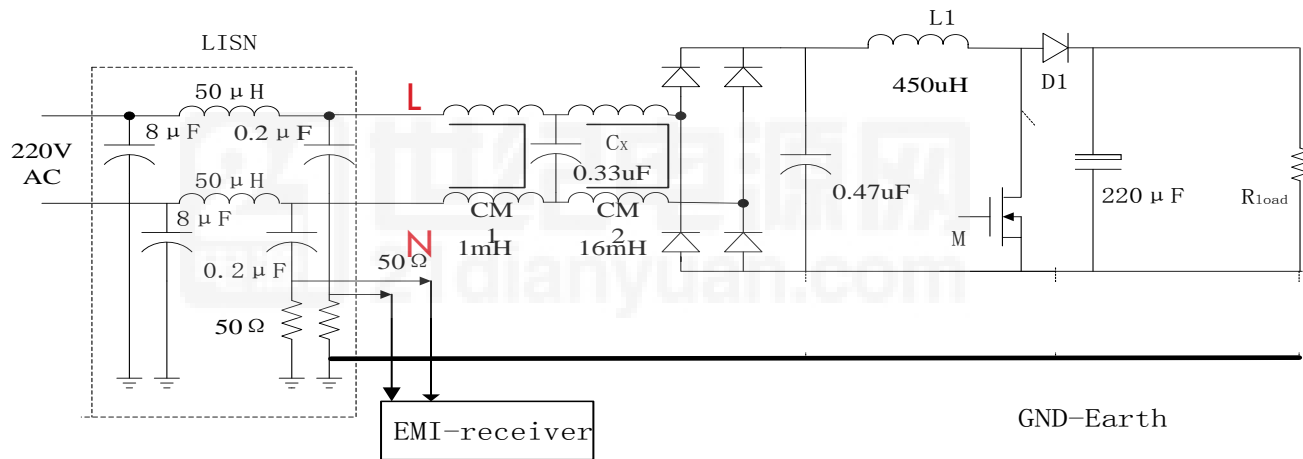
电视机电源传导噪声测试实景



主要设备

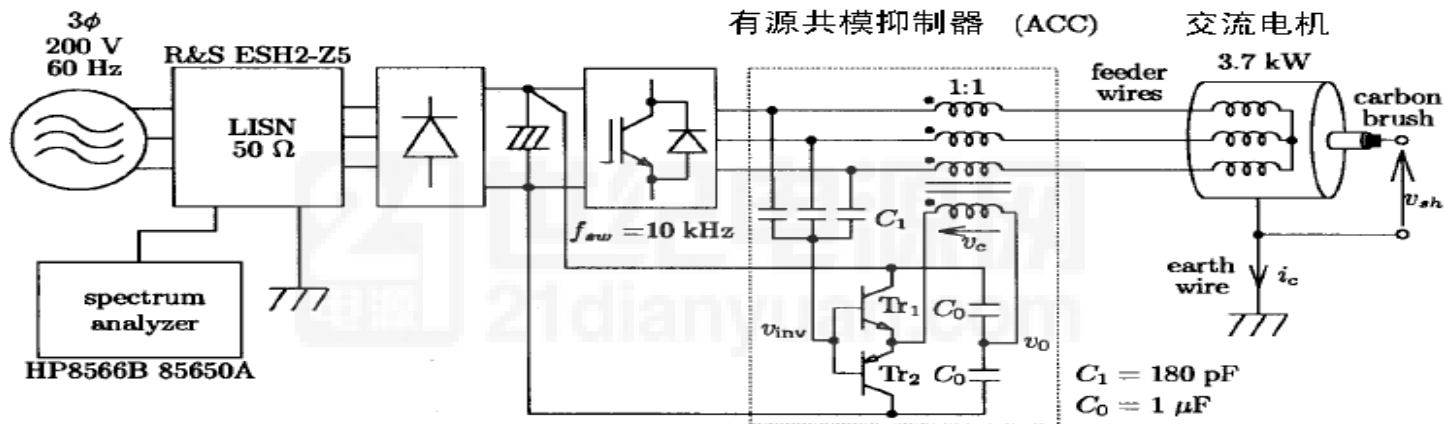
- LISN: 线路阻抗稳定网络
- EUT: 被测设备
- GND: 金属地平面
- EMI receiver: 电磁噪声接收机

单相：L, N line



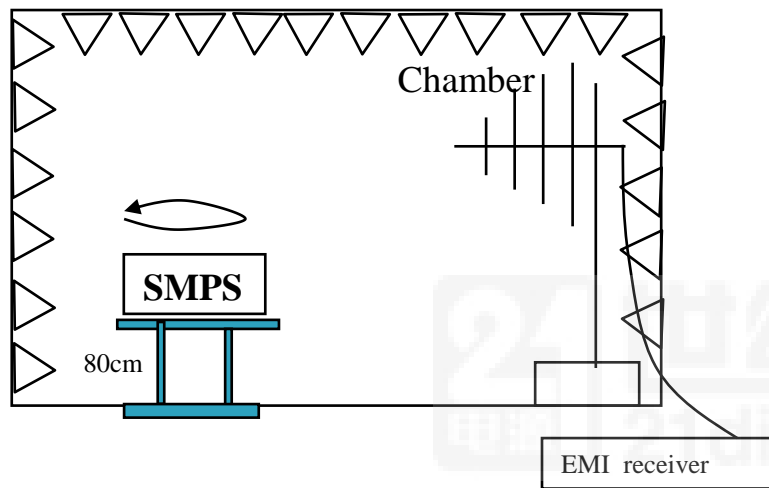
EMI接收机测量上述线上的射频干扰量值，均要小于限值

三相：L1, L2, L3,



EMI接收机测量上述线上的射频干扰量值，均要小于限值

测试原理和布局



主要设备

Antenna: 宽带天线

EUT: 被测设备

Chamber: 电波暗室

Turntable: 转台

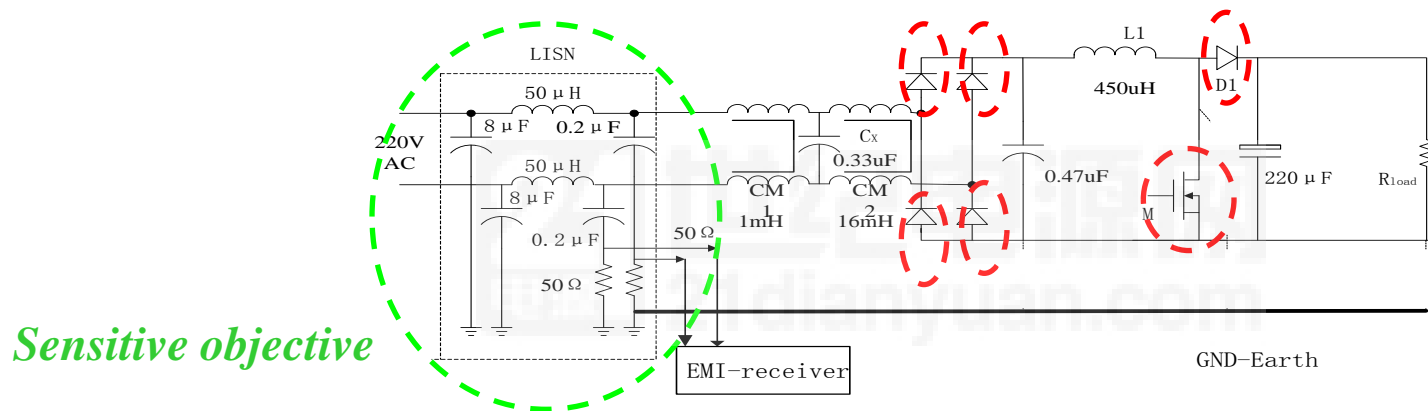
EMI receiver: 电磁噪声接收机

3m法辐射测试实景



Three factors of EMI! EMI source, coupling paths, sensitive objective

EMI source

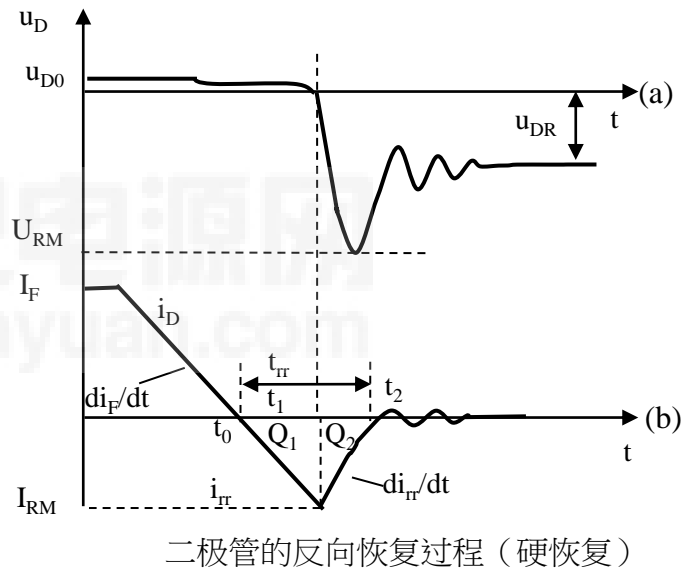
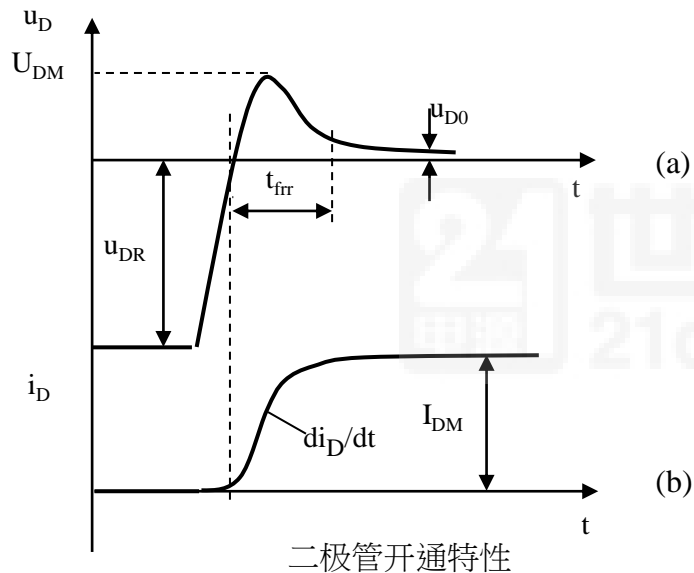


There are lots of different opinions. Mosfet, Diode, transformer, AC loop etc
Strictly speaking,

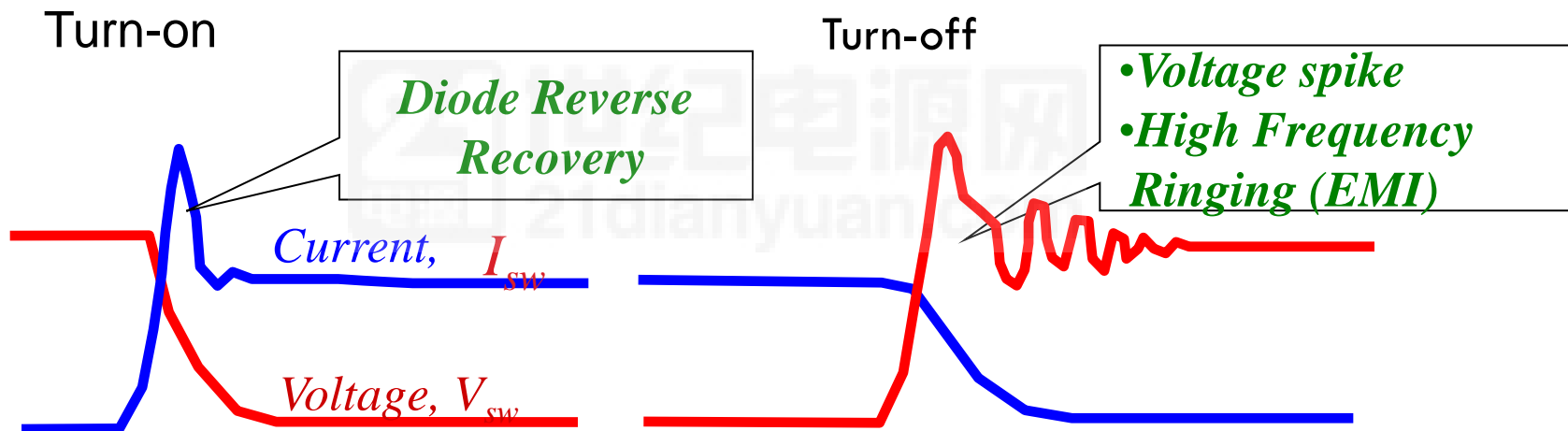
***Only Nonlinear switching devices are true EMI sources for EMI emission!
Others are coupling paths!***

Only for Radiation emission or simply analysis, others transformer and AC loop can be treated as EMI source!

A: Diode turn-on and turn-off



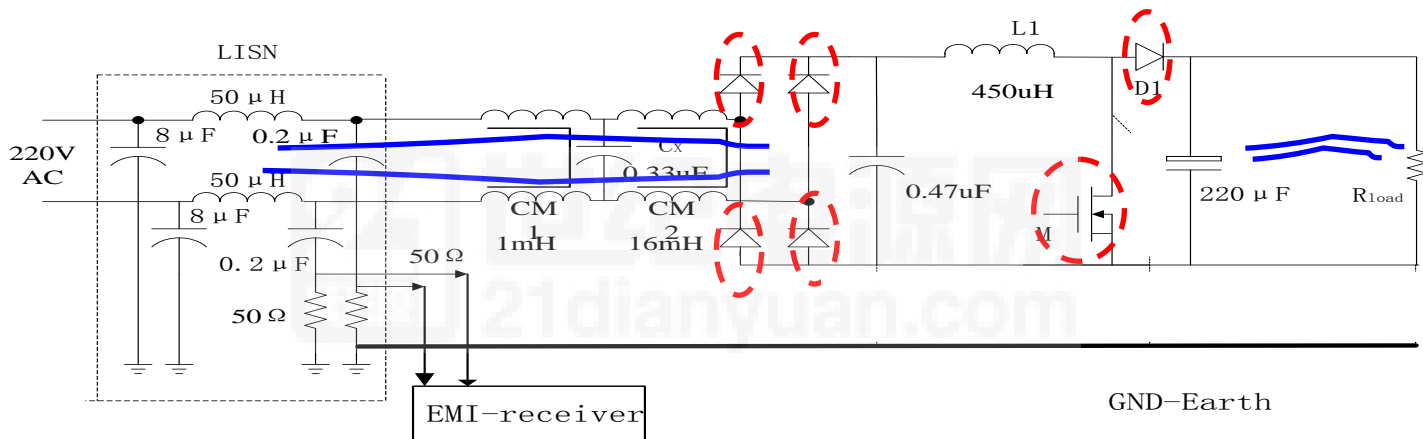
B: Transistor turn-on and turn-off



How about coupling paths! The difficult factors!

Basic EMI coupling mechanism

A: Along metal Lead

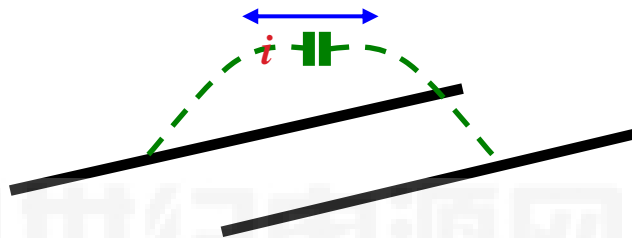


B: space Induct effect

B1: Capacitive coupling effect:

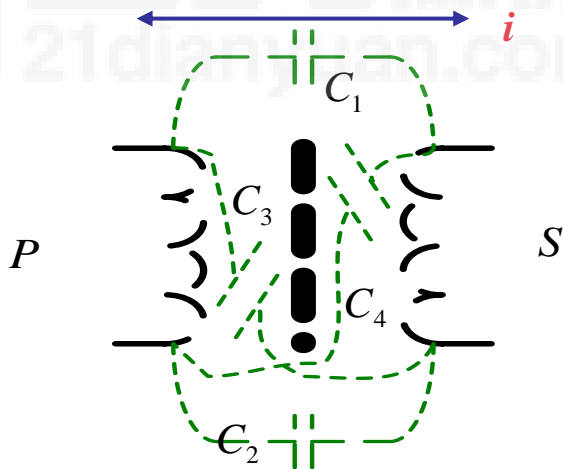
There is a coupling capacitor between every-two conductors!

Trace



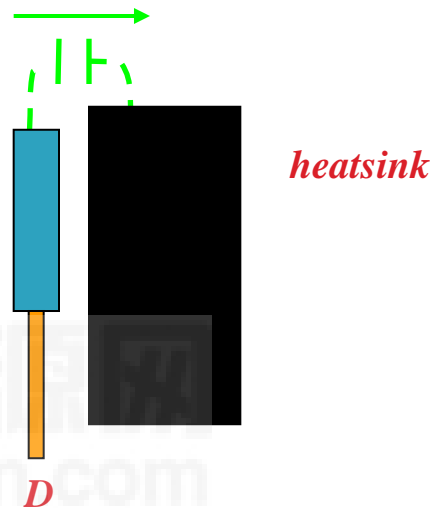
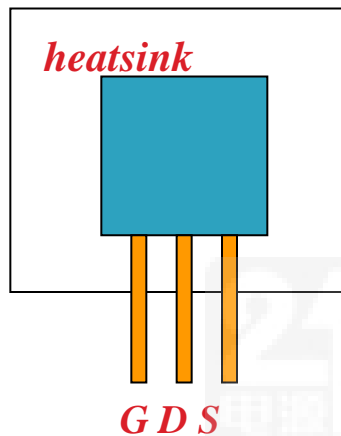
$$C_{12} = k \frac{S_1 S_2}{D}$$

Transformer

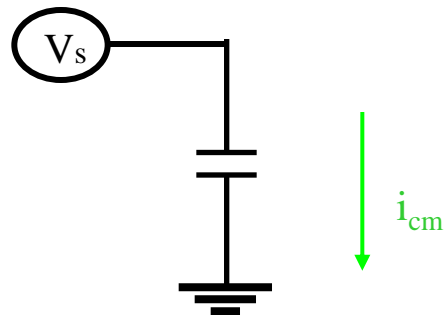
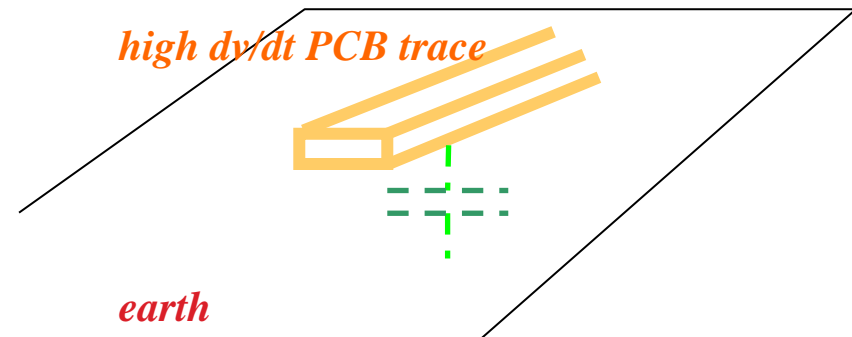


B1: Capacitive coupling effect:

Capacitor between drain to heatsink



Capacitor between high dv/dt trace or metal to earth

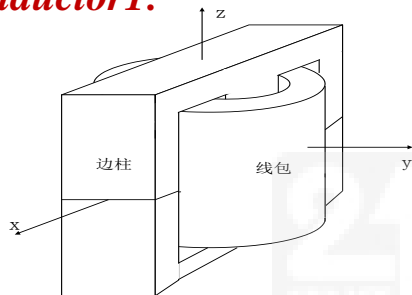


B2: Inductive coupling effect:

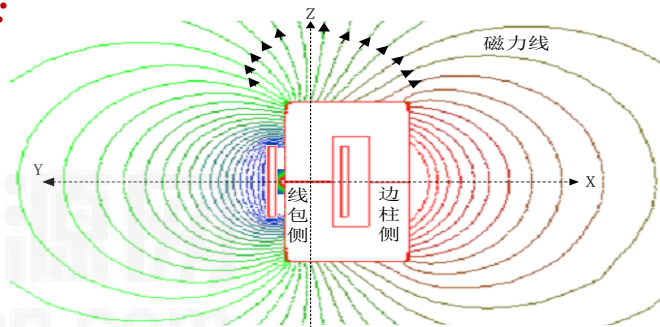
There is a coupling inductor between every-two loops!

Typical magnetic loops:

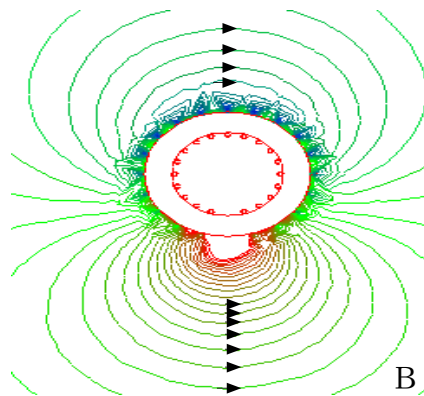
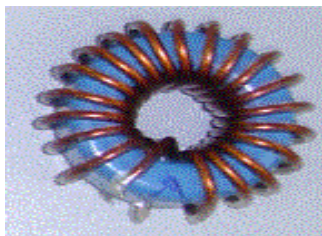
Inductor1:



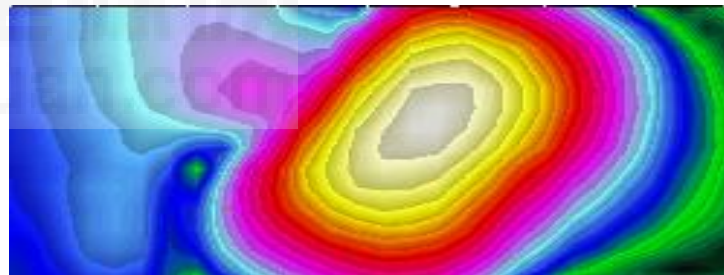
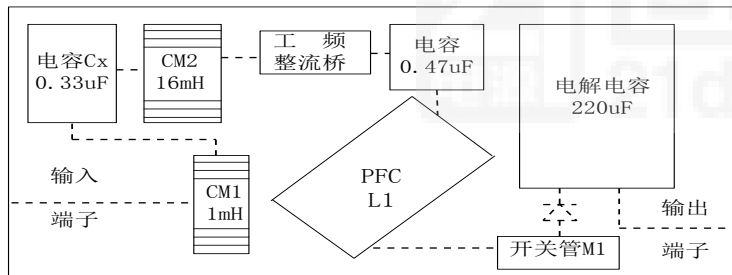
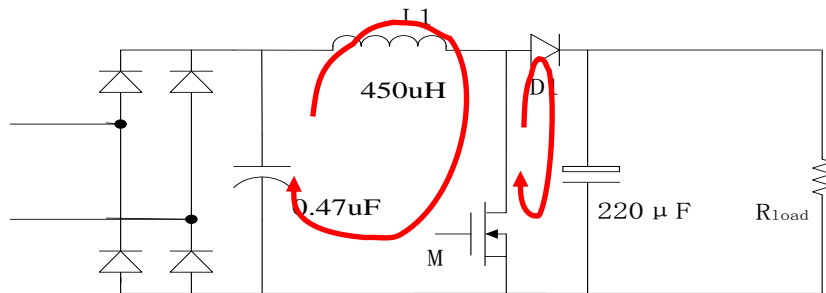
Transformer:



Inductor2:

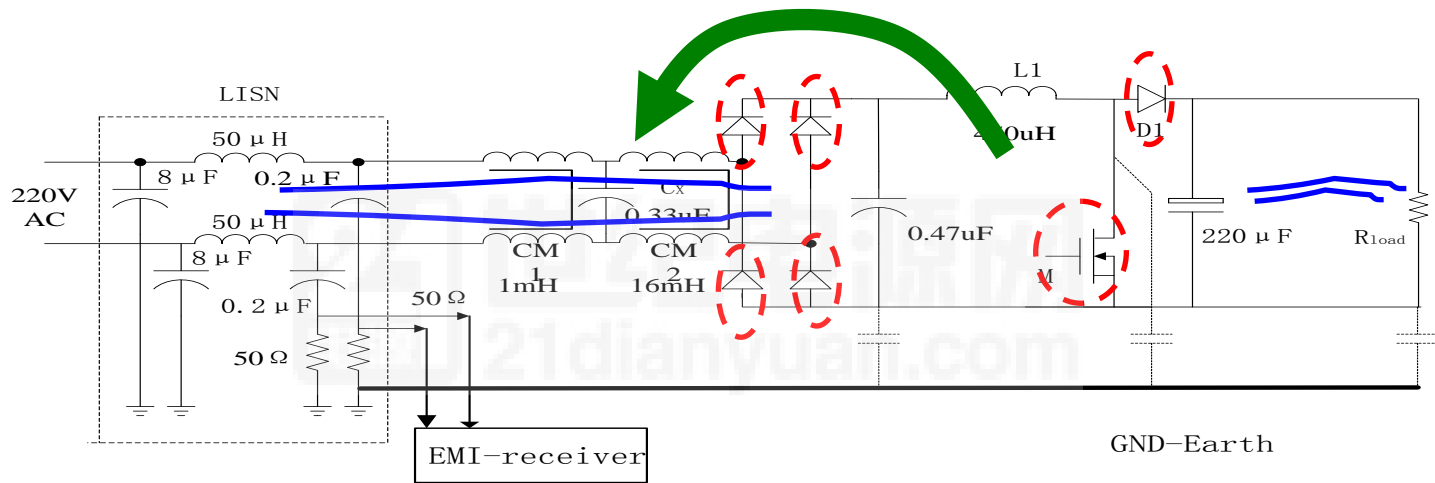


High frequency AC loops



Inductive coupling: produce EMI directly some time → sensitive circuit
complicit EMI coupling paths. → influence EMI filter performance.

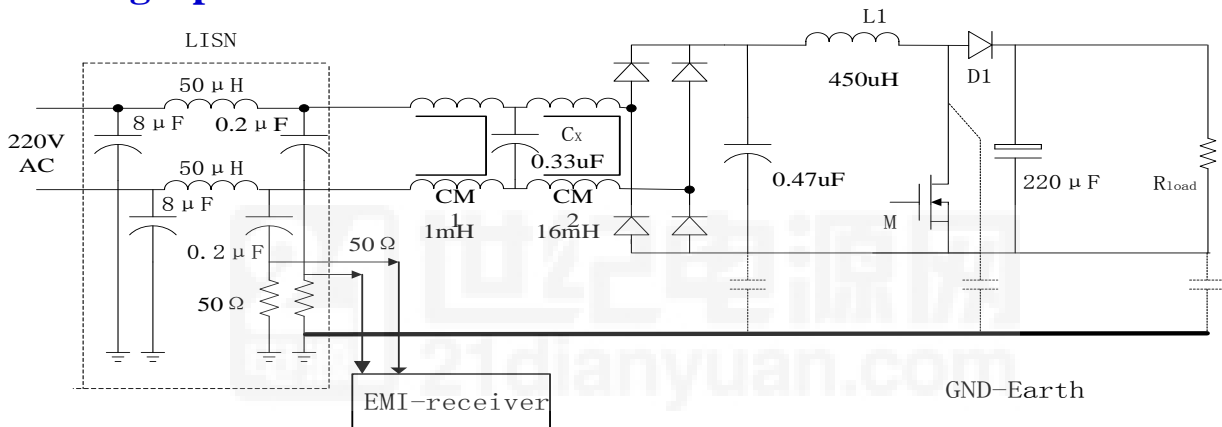
Total EMI coupling paths



3.2 开关电源电磁干扰的共模/差模分析

Why?

Example: Single phase



Emission on L line: V_L
Emission on N line: V_N

V_{cm} & V_{dm}

$$V_{CM} = (V_L + V_N) / 2$$

$$V_{DM} = (V_L - V_N)$$

$$V_L = V_{CM} + V_{DM} / 2$$

$$V_N = V_{CM} - V_{DM} / 2$$

So, V_L & V_N V_{cm} & V_{dm} are same!

因为差模回路和共模回路有不同的特点和性质，分开考虑，便于把握EMI形成、传播和抑制。

差模回路：voltage or current between L&N or among L1、L2、L3

Equivalent internal impedance is small! Paths is clear!

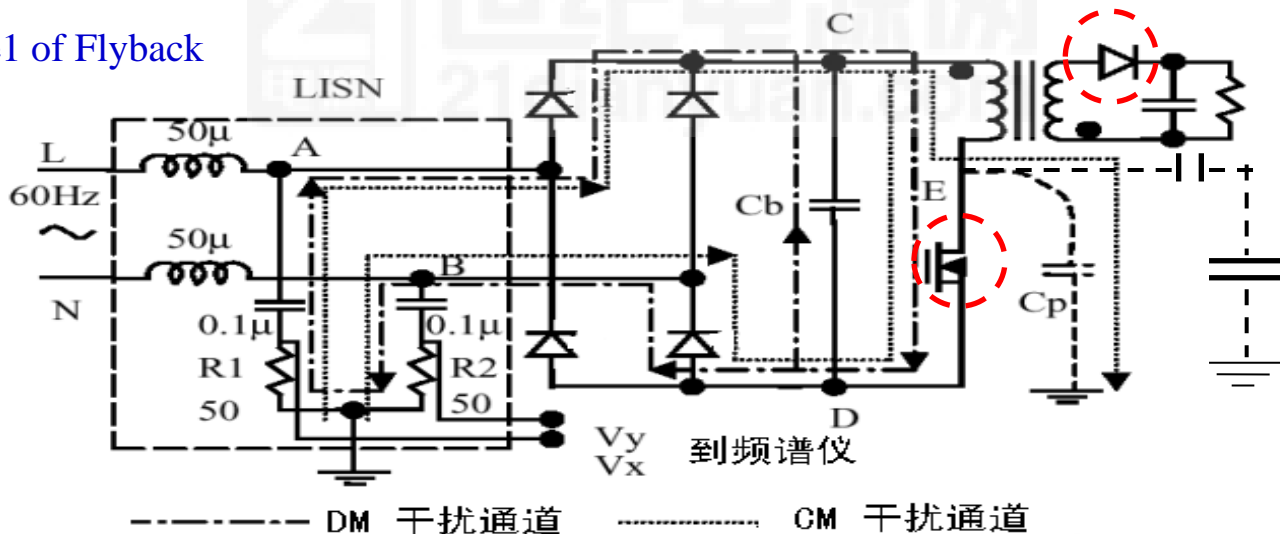
Through lines-load

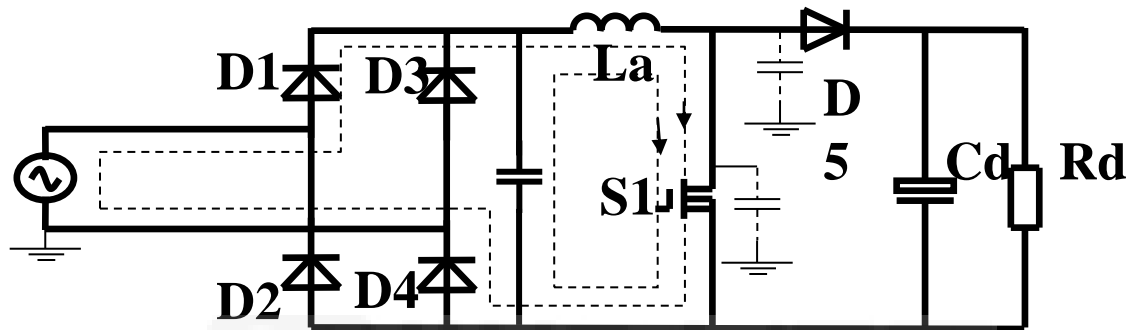
共模回路：voltage or current between lines and Earth

Equivalent internal impedance is large! Paths is unclear in most case!

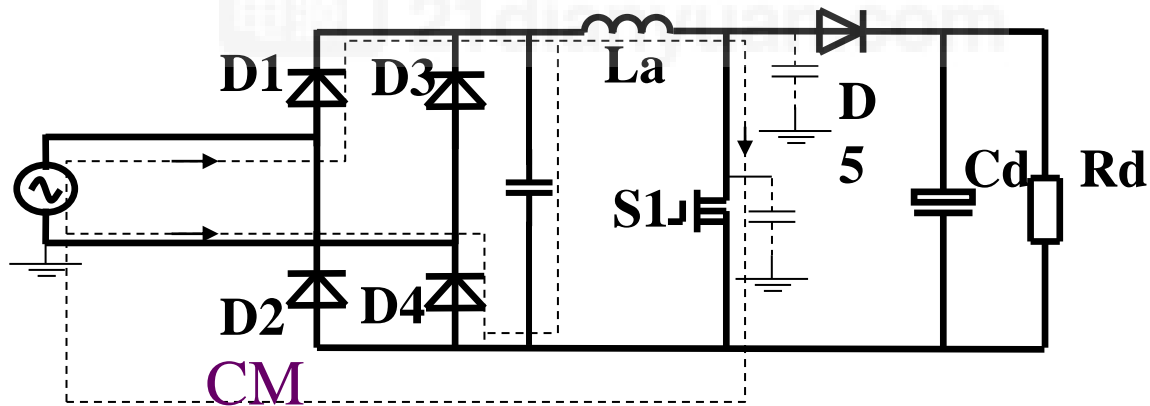
Through parasitic capacitor

Example1 of Flyback

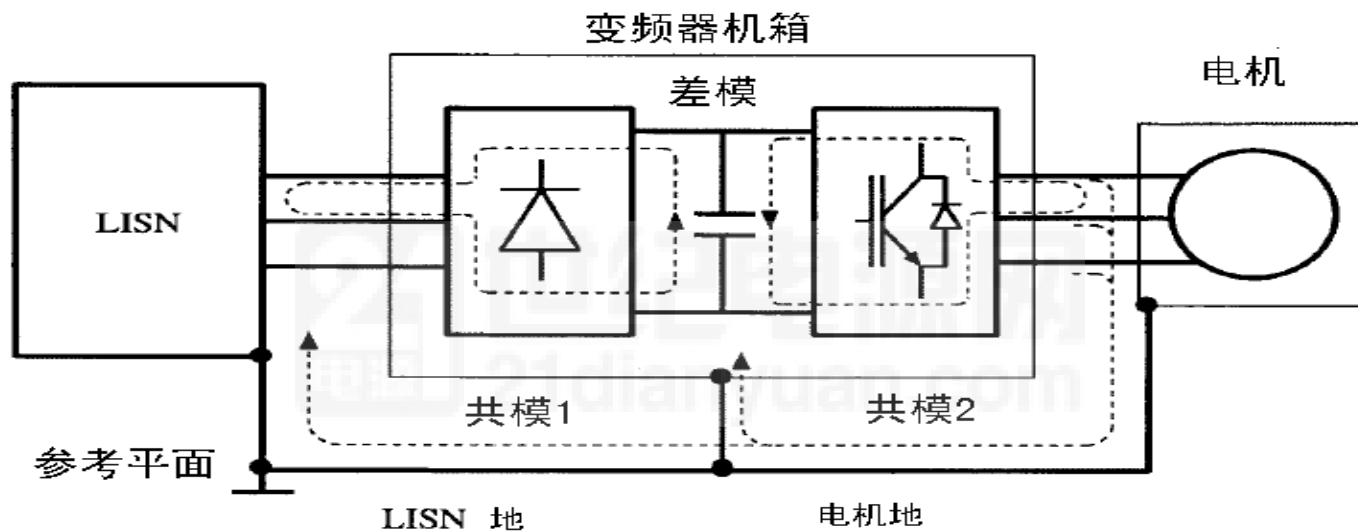




Noise Path of DM Noise without LISN



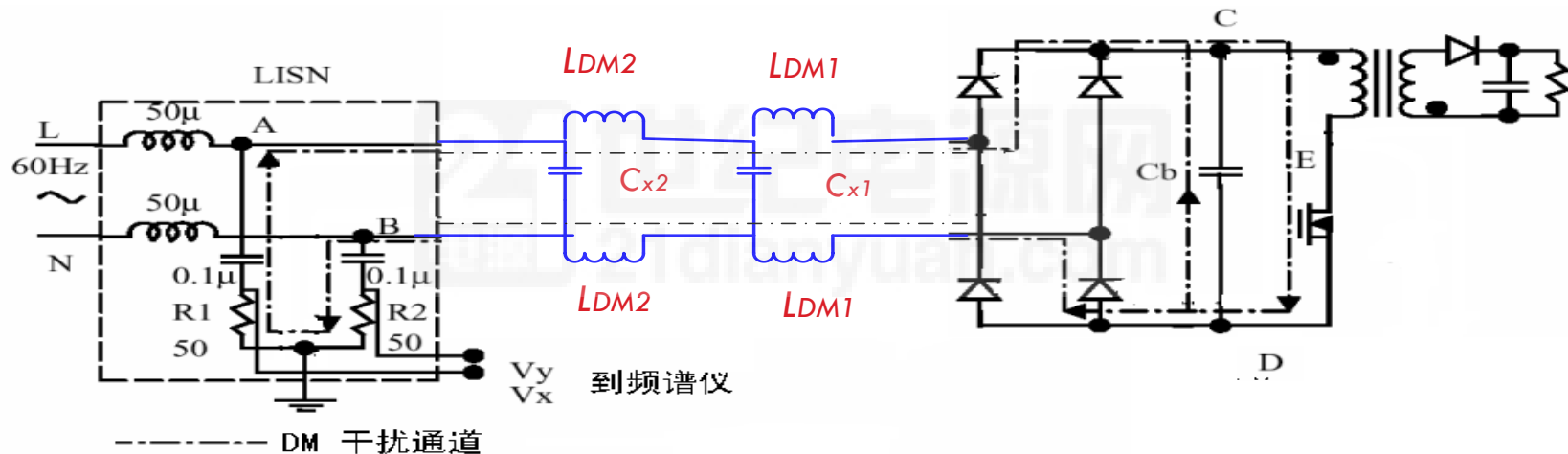
Noise Path of CM Noise without LISN



Usage of DM/CM Analysis:

It is very useful for EMI filter design and EMI debug!

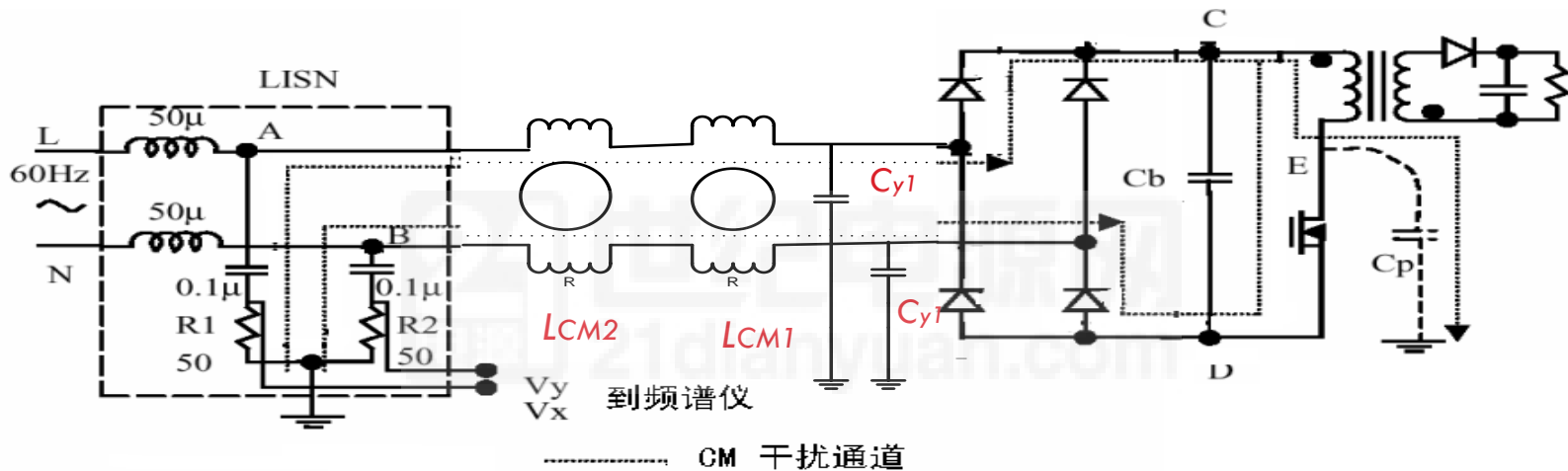
DM EMI filter to control DM emission! It has no influence on CM EMI.



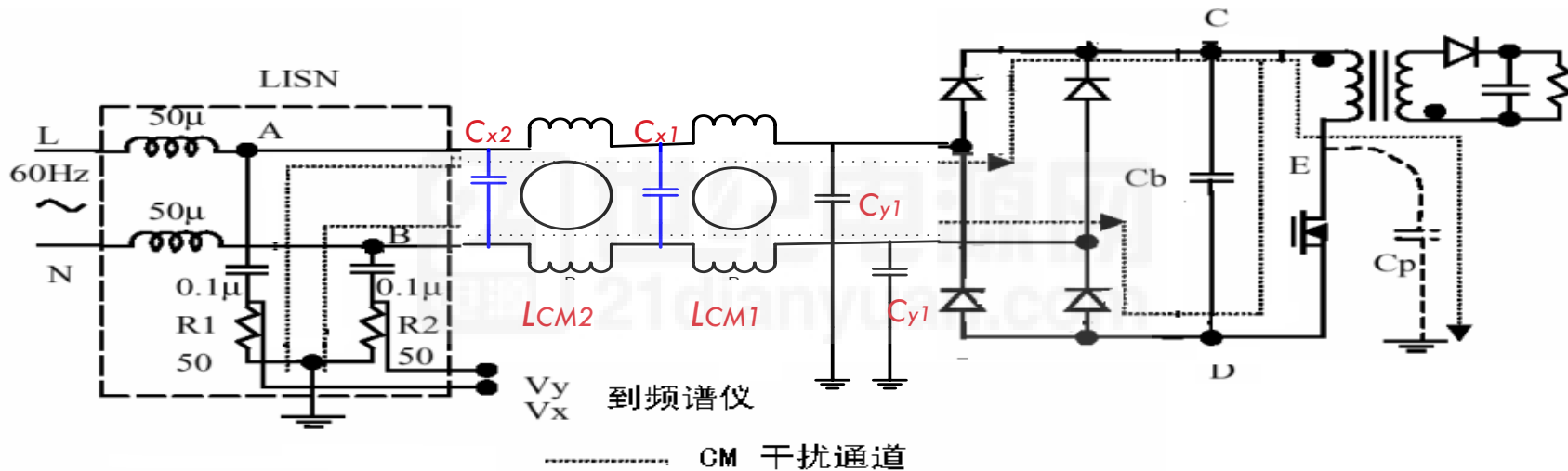
Generally, C_x is large several uF, L_{dm} is small!

CM EMI filter to control CM emission!

It has no influence on DM EMI.



CM filter+DM filter

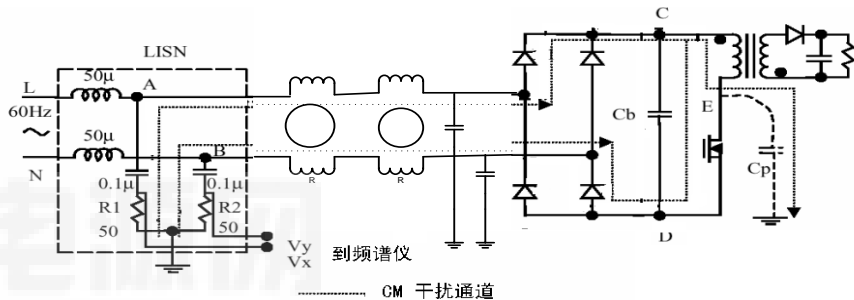
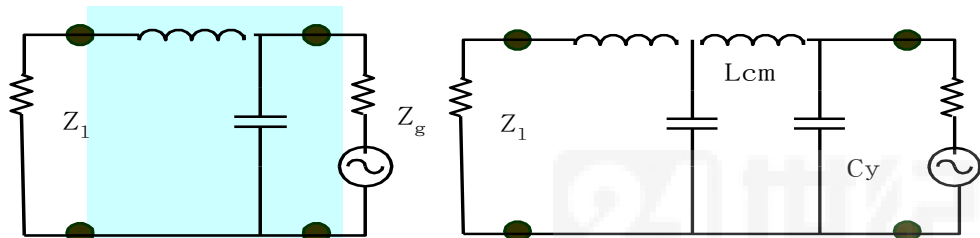


Caution: The leakage inductance of CM choke can be used as L_{DM}

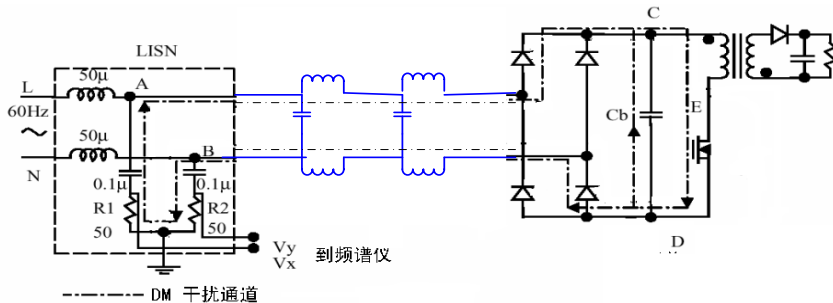
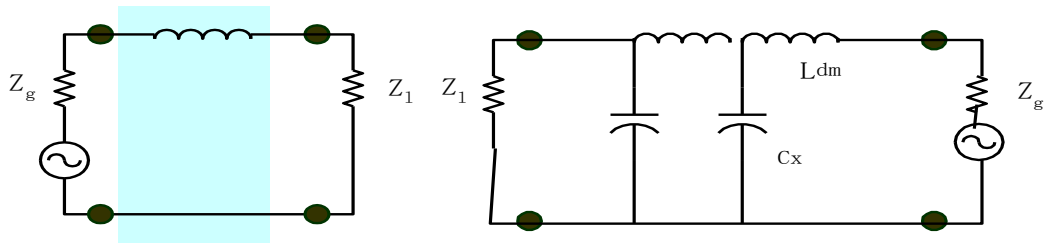
第4节 开关电源传导干扰的抑制设计

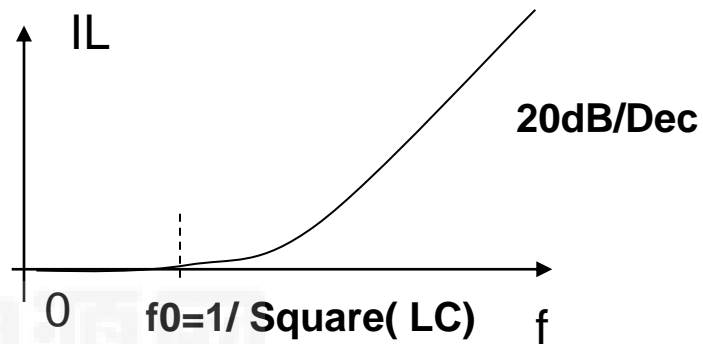
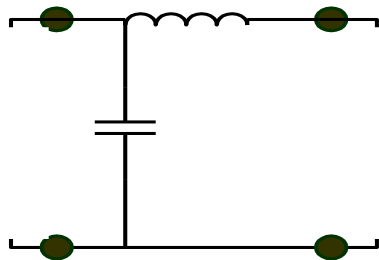
4.1 EMI 滤波器的参数设计

Multistage CM filter topology

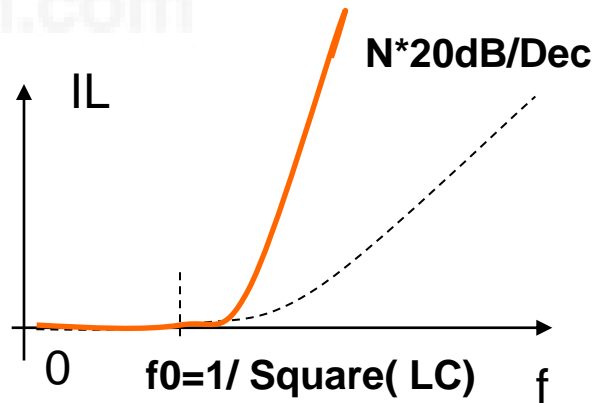
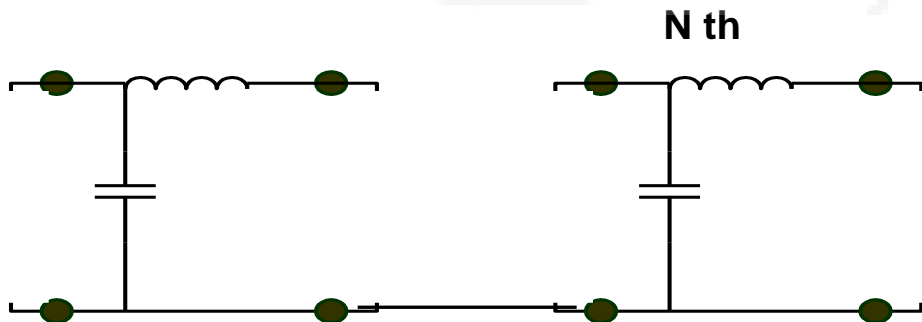


Multistage DM filter topology



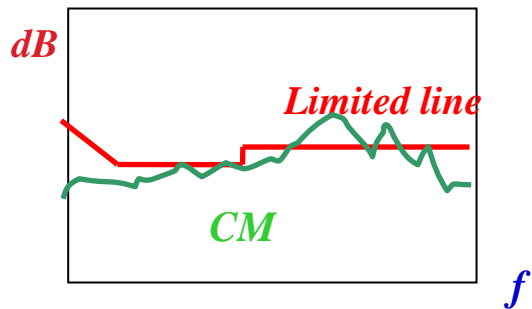
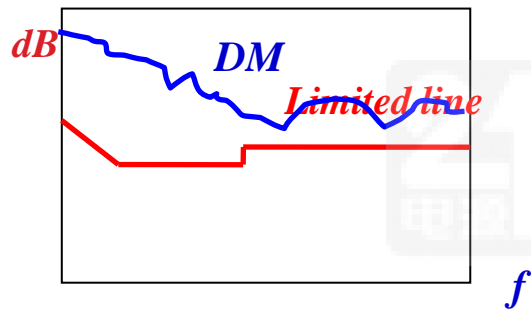


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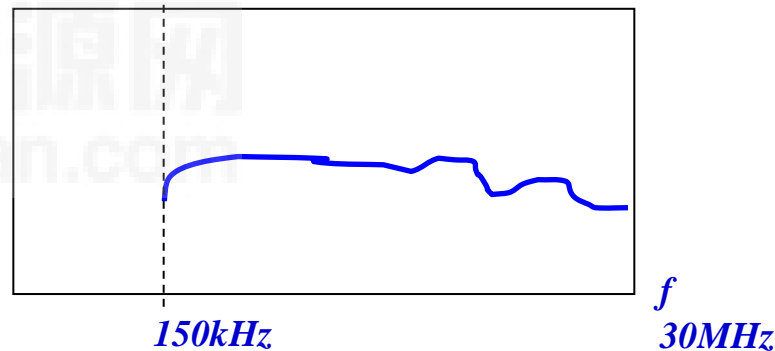


B: How to decide inductance, capacitance value of EMI filter ?

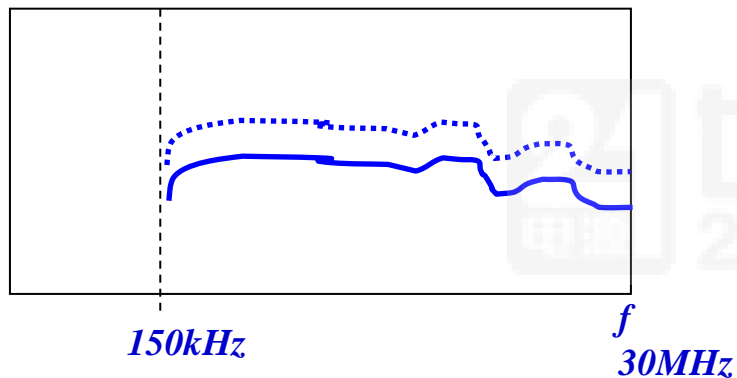
Step1: Separate CM/DM emission using
test or simulation results!



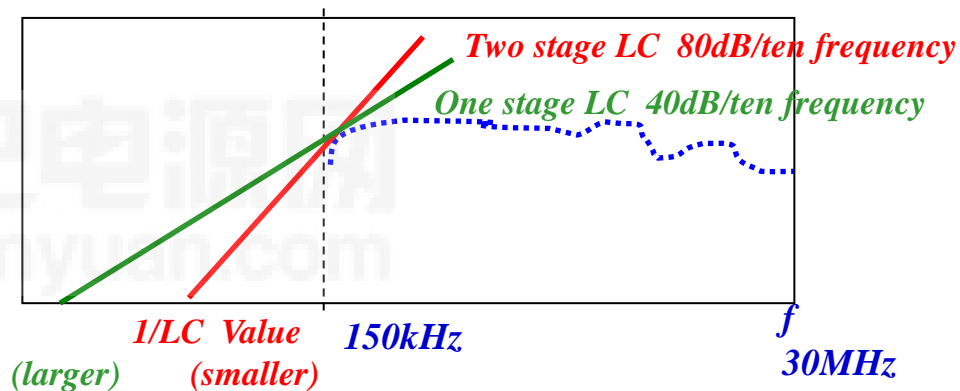
Step2: Using CM/DM emission decrease
limited line, the IL needed of filter are gotten.



**Step3: adding 10 dB margin for both
CM/DM IL needed**

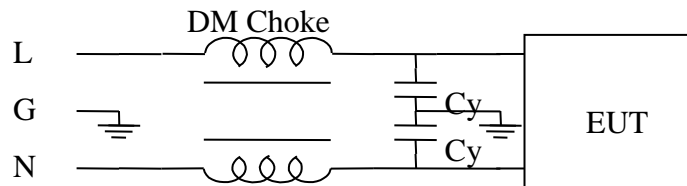


**Step4: According LC number, draw $N \times 40\text{dB}$ line
which is tangential to dot IL line.**

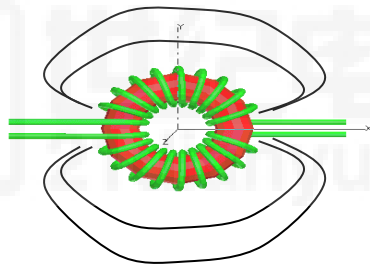


Step5: LC value, consider other factor, we can decide L and C.

For CM, the max C_y value is limited by leakage current, so $L_{cm}=f_0/C_y$. L_{cm} is called CM choke too.

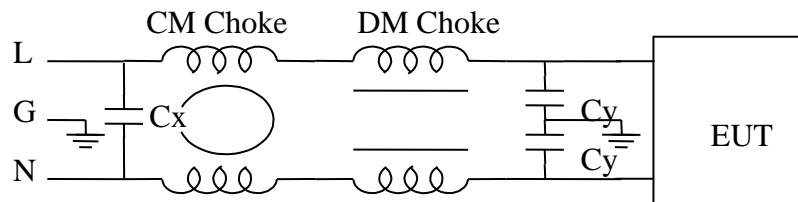


For DM, for C_x can be easy large enough, L_{dm} is select small. In most case L_{dm} can be replaced by the leakage inductor of CM choke.



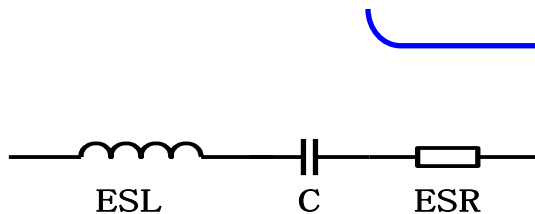
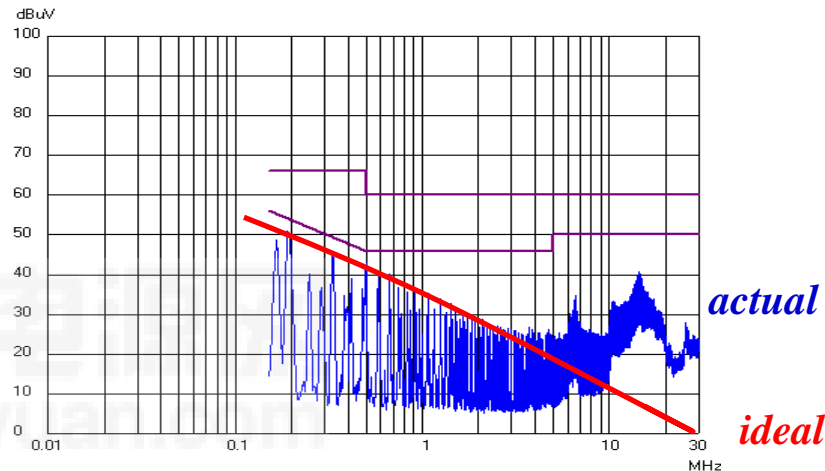
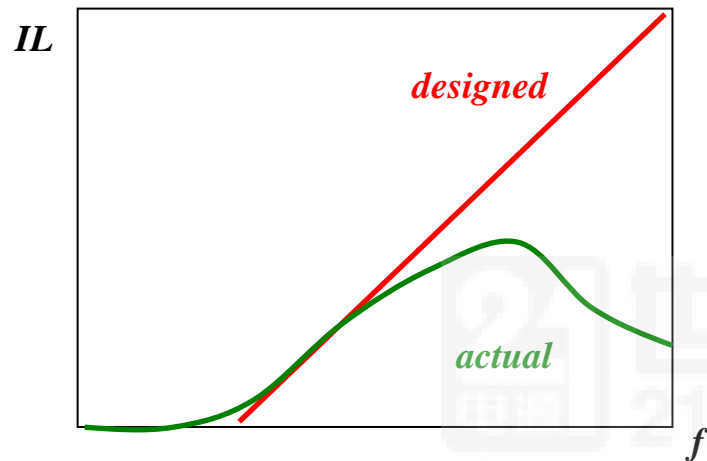
leakage inductor

Step6: finish design and test.

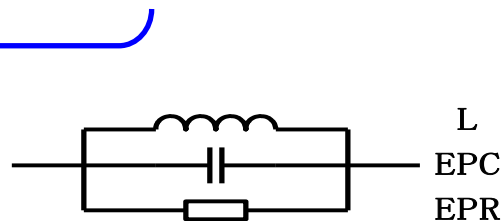


C: Actual problem after EMI filter inserted

1: HF IL are lower than expected.



Capacitor Model



Inductor Model

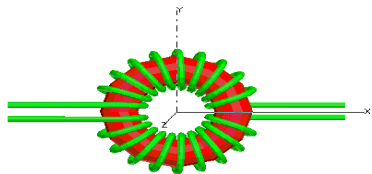
What to do?

Decrease parasitic as possible!

1: Using good HF capacitor or inductor! Small parasitic parameter!

对于电感:

铁氧体: 易饱和、导磁率高, 常用作共模扼流圈的磁芯



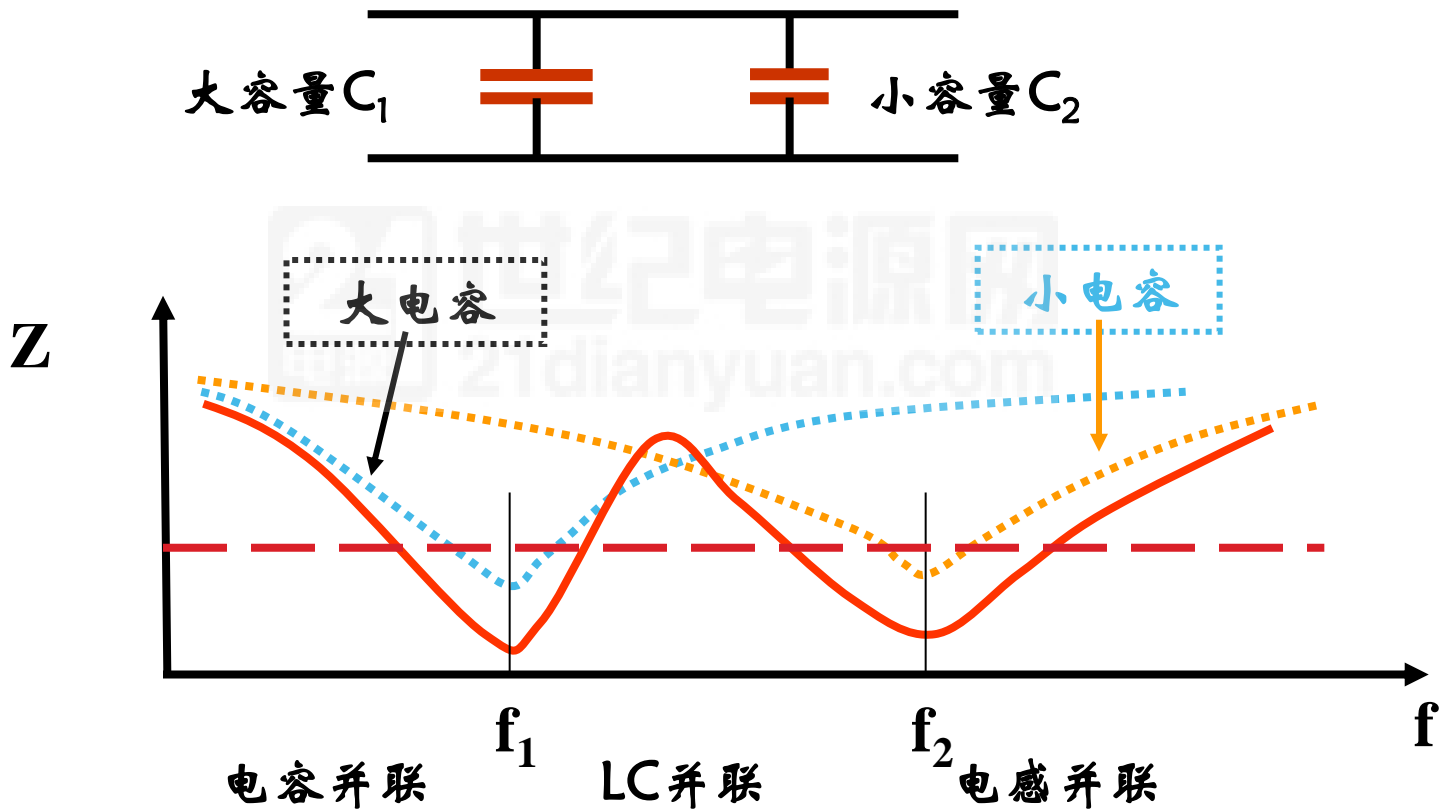
锰锌: $\mu_r = 500 \sim 10000$ for lower frequency CM choke

镍锌: $\mu_r = 10 \sim 100$ fit for HF CM choke

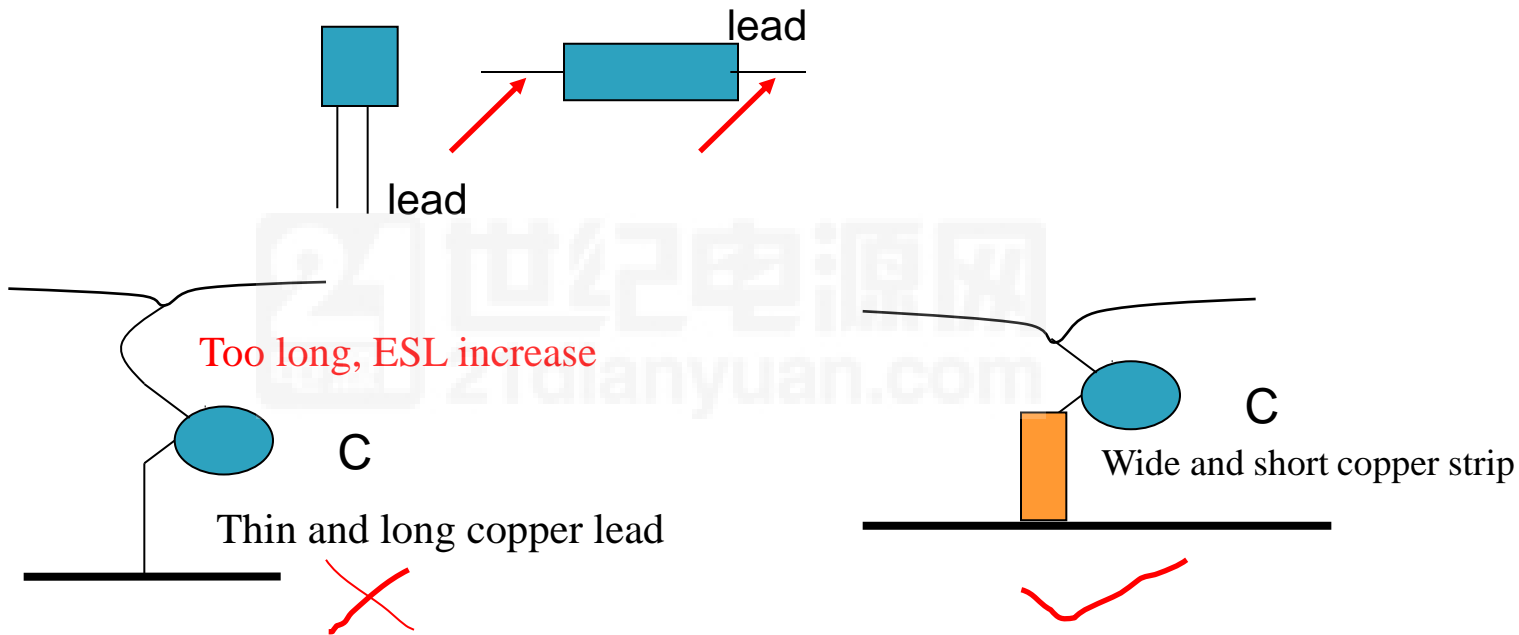
采用少匝, 交错绕制等方法减小线圈的EPC!

对于电容

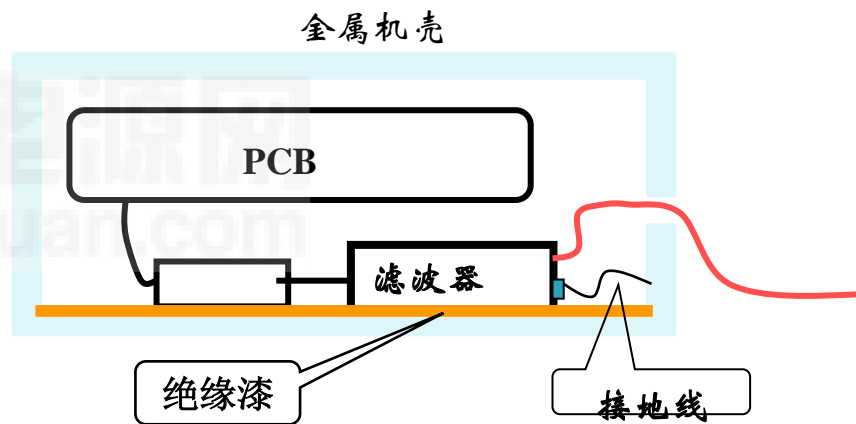
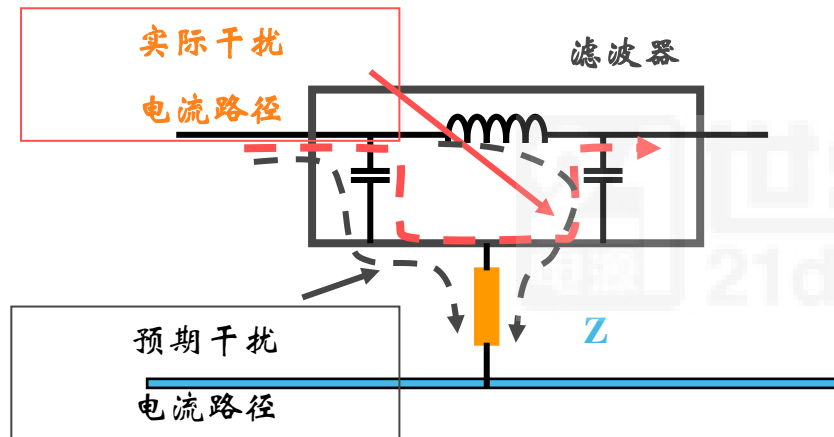
1: 采用高频性能好的小电容。



2: Decrease lead length of capacitor as shorter as possible. ESL!

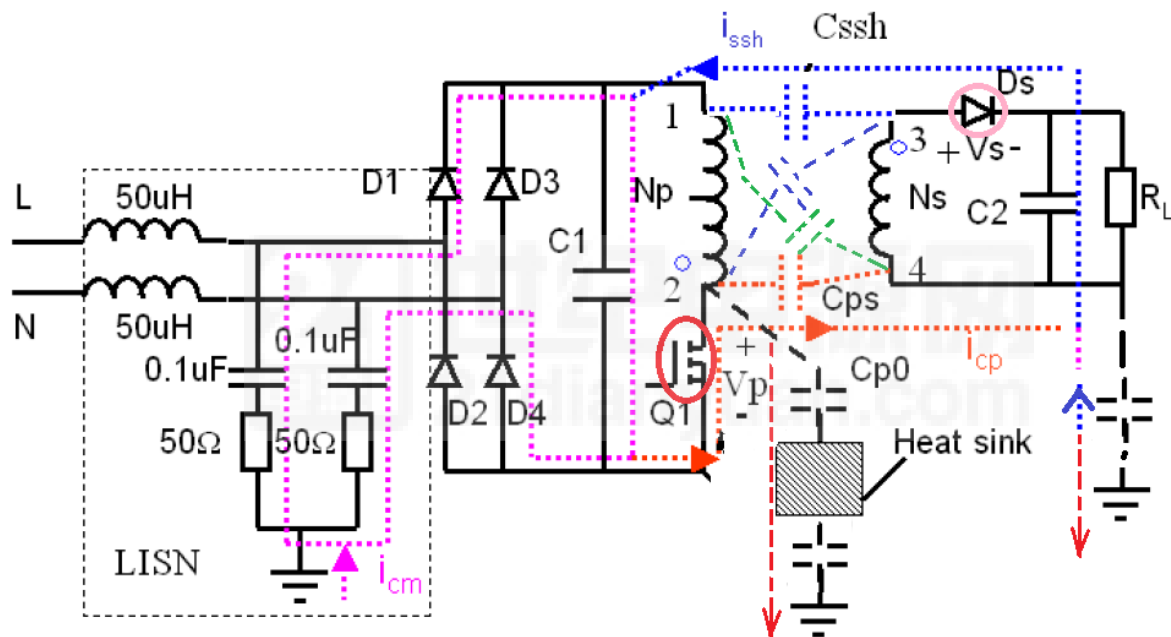


3: Carefully installment!

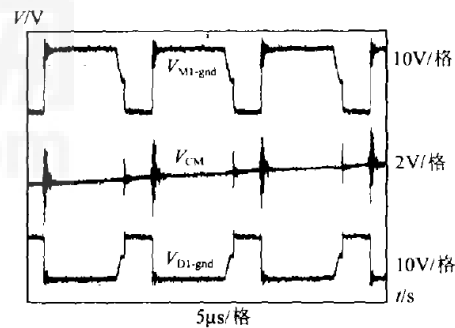
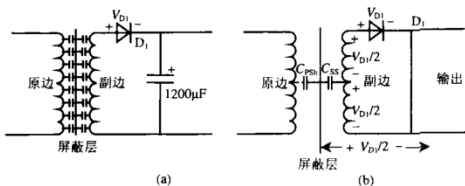


4.2 无Y电容开关电源设计

Flyback电源为例

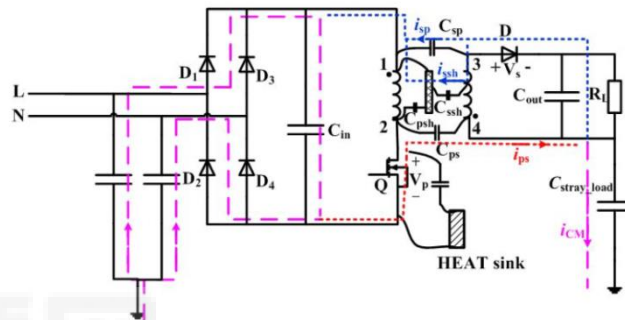
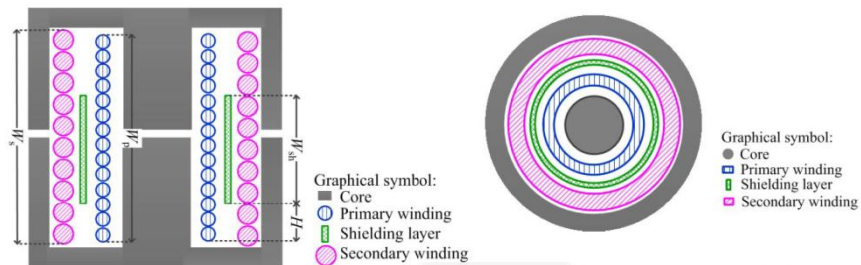


原始噪声通道 $V_p \gg V_d$



屏蔽后变压器简化模型

2: 变压器屏蔽层居中结构设计



2016, Henglin Chen

$$i_{ps} = f_{11}(H, W_{sh}, C_{ps0})$$

$$i_{ssh} = f_2(H, W_{sh})$$

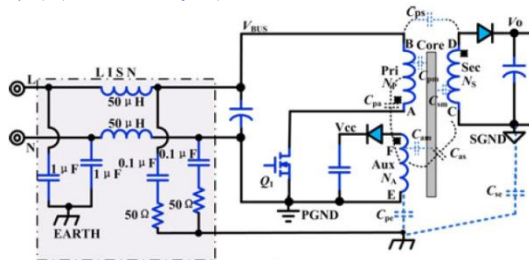
$$i_{sp} = f_3(H, W_{sh})$$

$$i_{CM} = i_{ps} - (i_{sp} + i_{ssh}) = 0$$

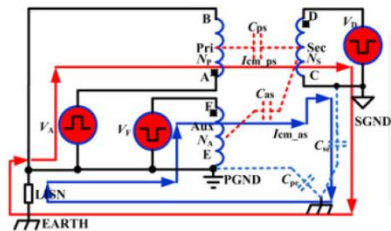
优点：低成本。低漏电流。

缺点：绕制工艺要控制

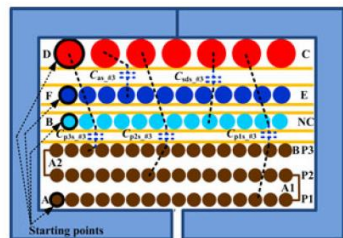
3: 类似具体工程设计



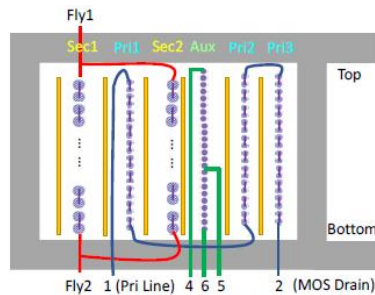
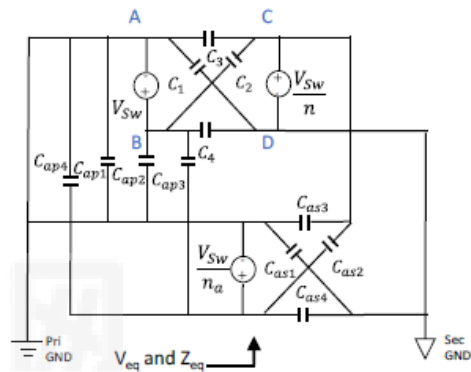
(a)



(b)



- Secondary
- Auxiliary
- Shielding
- Primary
- Tape
- *Clockwise winding



Modern modulation techniques

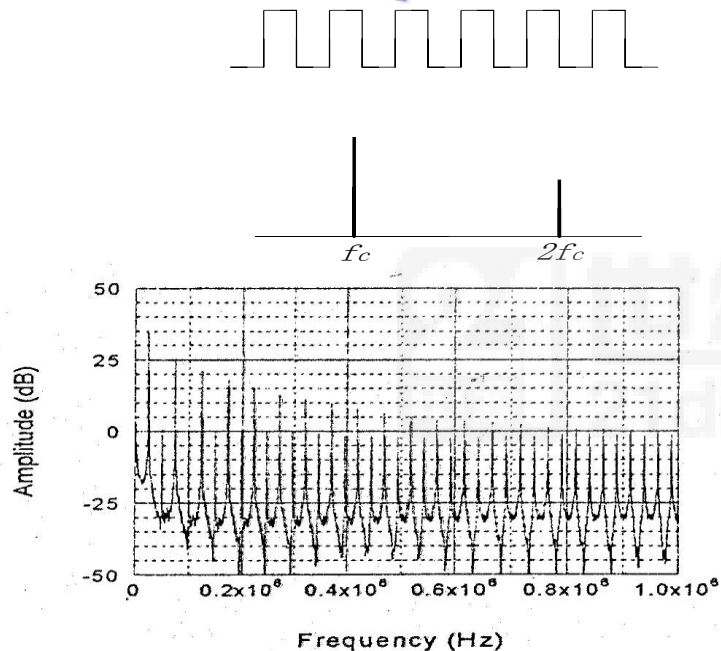


Fig 1a. Constant 25kHz PWM

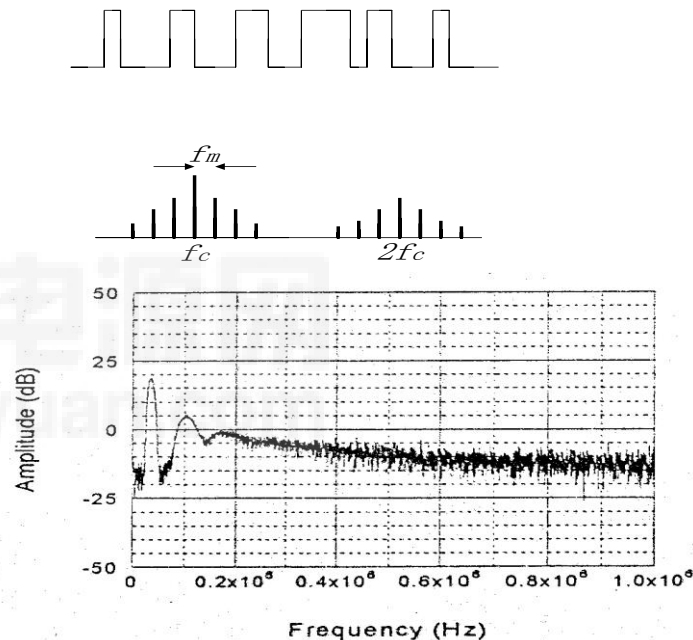


Fig 1c. $\Delta f = 20\text{kHz}$ (frequency varied from 25kHz to 45kHz), $n=256$.

Switching frequency modulation

— proposed by F. Lin et al , IEEE PESC'93

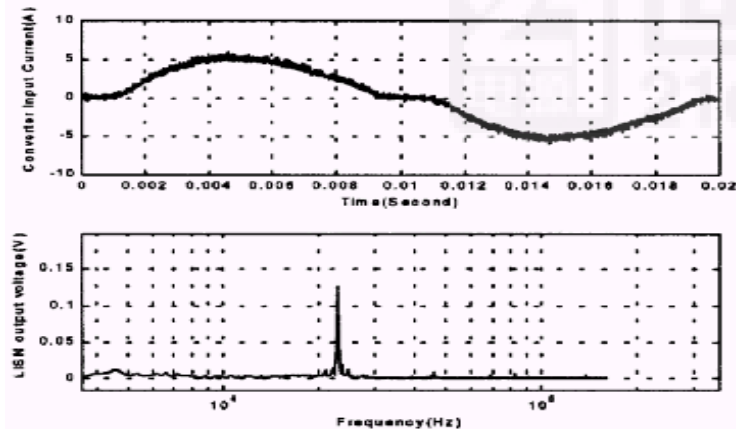
- **Random modulation**

_____ proposed by D.A. Stone et al, IEEE APEC'96

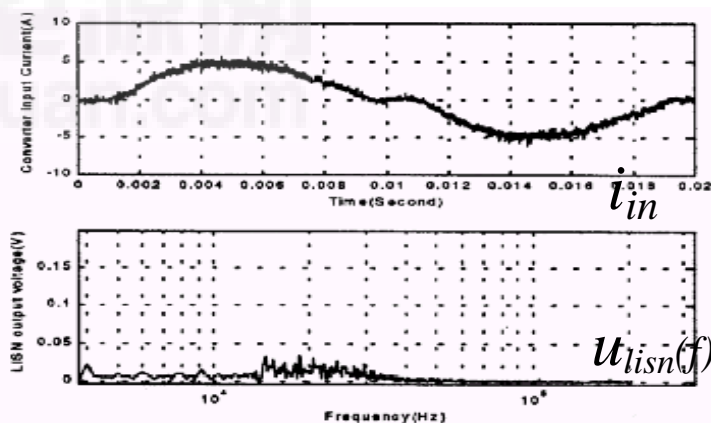
- **Sigma - Delta modulation**

_____ proposed by J. Paramesh et al, IEEE APEC'99

- **Comparison : PWM & RPWM**

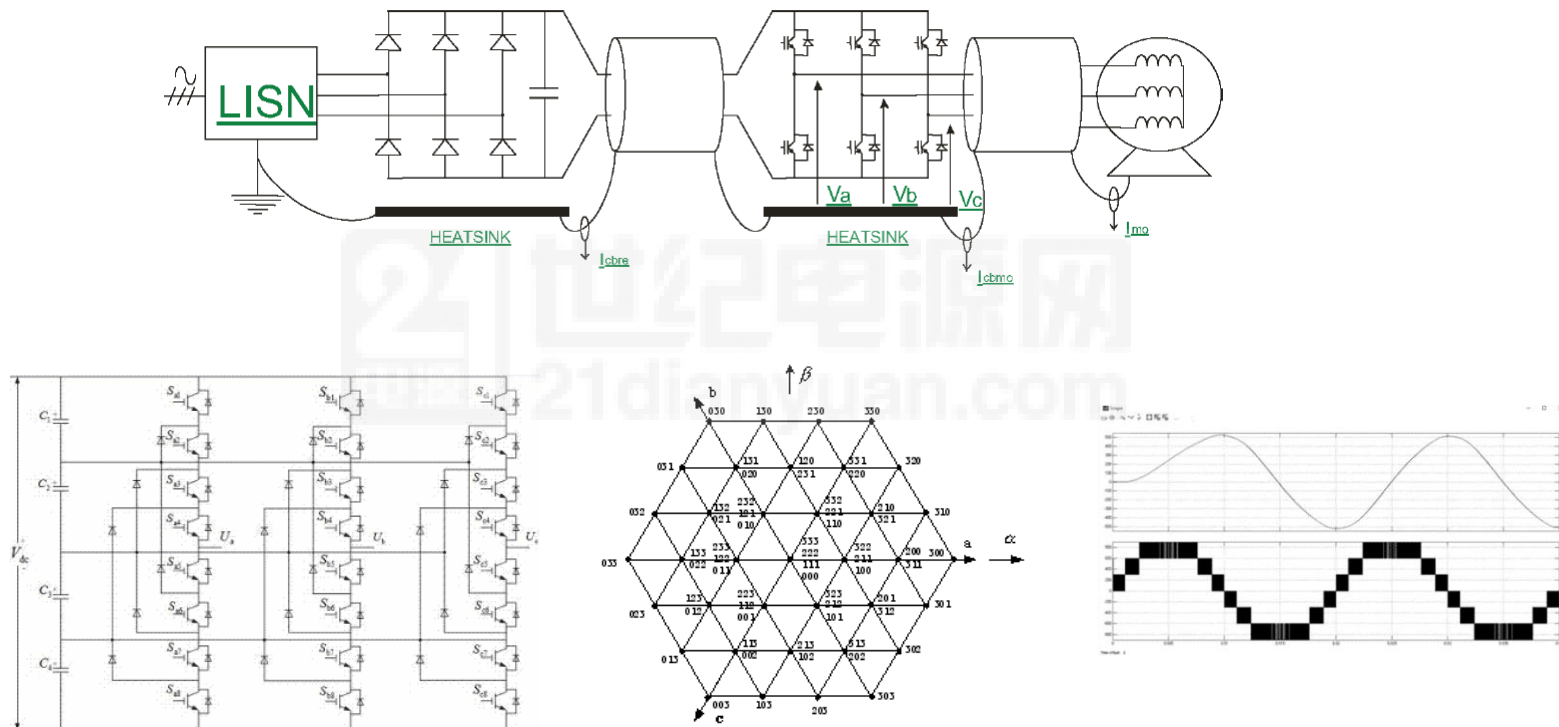


PWM, $f = 25 \text{ kHz}$



RPWM, $15 \text{ kHz} < f < 30 \text{ kHz}$

Jitter and PWM modulation fit for SMPS, inverter, multilevel converter



五：总结

- 1： 详细介绍了开关电源电磁干扰的产生原理、差/共模通道及几种典型电源的干扰模型；
- 2： 细致介绍了EMI滤波器设计、无Y电容电源设计、抖频调制等实用新型抑制和设计技术；
- 3： 介绍和探讨了开关电源EMC设计挑战和机遇。

问答和讨论环节

?



谢谢大家！



Thanks for your attention!