Research Letter

Ultrahigh Frequency Carbon Nanotube Transistor Based on a Single Nanotube

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***Abstract*—Single-walled carbon nanotube field-effect transistors (CNT FETs) are predicted to have intrinsic cutoff frequencies approaching the THz range. Here "intrinsic" means that the parasitic capacitance due to fringing fields is negligible compared to the gate-source capacitance required to modulate the conductance. In practice, although there are strategies proposed to mitigate this based on parallel arrays of CNT FETs, this parasitic capacitance dominates most geometries (even aligned arrays to date). In this work we show nanotube transistor performance with maximum stable gain above 1 GHz (even including the parasitics) by combining "on-chip" the electrical properties of 100 CNT FETs fabricated on one long nanotube. This also solves the problem of impedance matching by boosting the on current to a large (mA) value, and at the same time allows one to extract properties of each individual CNT FET, since they are identical in electrical characteristics as they are made out of the same CNT. This strategy opens the door to applications of carbon nanotube devices in the RF and microwave frequency range, a technologically relevant portion of the spectrum for both wired and wireless electronics, that has been (until now) incompatible with nanotube device technology.**

***Index Terms*—Nanotube, nanotechnology, RF.**

I. Introduction

IDEALLY, ONE would like to fabricate an individual carbon nanotube field-effect transistor (CNT FET) and measure its full S parameters (or equivalently Z, h, or ABCD matrix [11]) which relates the ac currents and voltages at each terminal of the device to one another, and then come up with an equivalent circuit model that could then be compared to theoretical models[1]–[10] and used as basis to construct more complex circuits out of more than one CNT FET. In practice, the high impedance and low on current of a single CNT FET makes this measurement very challenging, and to date only one group [12], [13] has partially measured the S matrix of an individual CNT FET, while other groups have measured the device nonlinear response (which is more feasible to measure) up to 50 GHz [14]–[17]. In this work, using one individual 100 μm long single walled carbon nanotube, 100 individual nanotube top gated field effect transistors are combined in a finger geometry to produce a single transistor with a cutoff frequency (after de-embedding parasitic capacitance of the finger structure) of 7.6 GHz; before de-emdedding the cutoff frequency is 0.2 GHz. The max stable gain value after de-embedding falls to unity at over 15 GHz (extrapolated), and before de-embedding falls to unity at 2 GHz (measured). A dc power of >1 mW and a transconductance (dc) over of over 1.5 mS is sustained by the combined device.

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II. Fabrication and DC Characterization

A. Fabrication

Individual single-walled carbon nanotubes were synthesized via chemical vapor deposition according to previously published recipes [18], [19] on oxidized high resitivity Si wafers with a 300–400 nm SiO_2 layer. Metal electrodes were formed on the SWNTs using electron-beam lithography and metal evaporation of 30-nm Pd/100 nm Au bylayer. The devices were not annealed. Evaporated silicon dioxide (thickness 10 nm) served as the insulator, and a Au top-gate was evaporated. Many devices were measured; here we present results from a typical device.

B. Device Design

The electrode geometry is indicated schematically in Fig. 1(A); an SEM image is shown in Fig. 1(B). The source–drain gap was 0.8 μm, and the gate length was 0.4 μm, so that part of the nanotube was not gated. A total of 100 gate fingers, 50 source fingers (sourcing current in both directions) and 50 drain fingers (sinking current in both directions), were connected electrically on-chip as indicated, for a combined total of 100 CNT FETs connected electrically in parallel. Since each CNT FET was fabricated with nominally the same geometry on the same nanotube, the electrical properties of each CNT FET are expected to be identical. The source/drain/gate electrodes were connected to industry standard coplanar waveguide structures (not shown) for compatibility with a commercial RF probe station.

C. DC Characterization

Fig. 2 shows the room temperature I–V characteristic of one of our devices. The inset shows the low-bias depletion curve. At

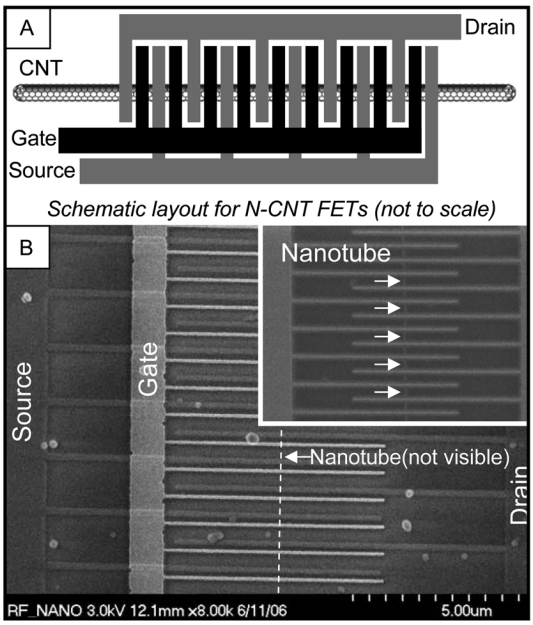

Fig. 1. **Multifinger nanotube RF device.** (A) Schematic indication of device geometry (not to scale). In total, there are 100 gate fingers in our design. (B) SEM image of a portion of a multifingered SWNT FET. Shown are 13 of the 100 gate fingers. The nanotube is visible in the inset before the dielectric is deposited; after dielectric and top-gate deposition the nanotube is not visible.

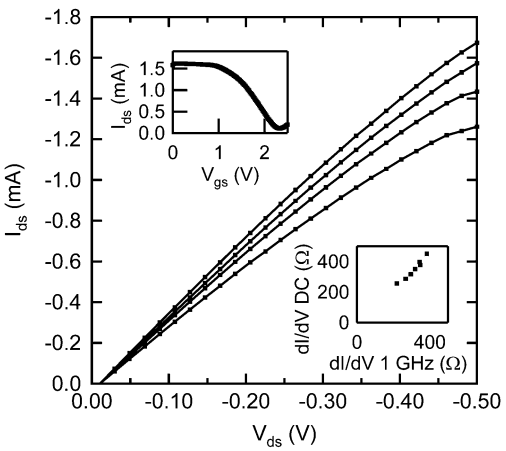

Fig. 2. **DC performance.** Current–voltage characteristic at $V_g = -1$ to $+0.5$ V in 0.5 V steps; upper left inset shows depletion curve at $V_{\rm ds} = 0.5$ V; lower right inset shows dc and 1 GHz $dI_{\rm ds}/dV_{\rm ds}$ under various bias conditions.

the gate and source–drain bias required to completely turn off the device or enter saturation, irreversible device damage occurs, which we believe is due to the low quality (evaporated) oxide; future devices with higher quality dielectric should allow higher bias voltages, since devices without the dielectric can sustain over 10 V on source–drain without damage. The devices display clear p-type behavior, with a transconductance of up to 1.5 mS, and dc power of over 1 mW. In addition, the bottom right inset shows the differential resistance at dc (from the measured I–V curves) versus the differential resistance from the measured microwave S parameters, described below. The agreement is very good: under a variety of bias conditions, the dynamical source–drain impedance is the same at 1 GHz as at dc. This is consistent with prior measurements of the same quantity on an individual nanotube FET [13].

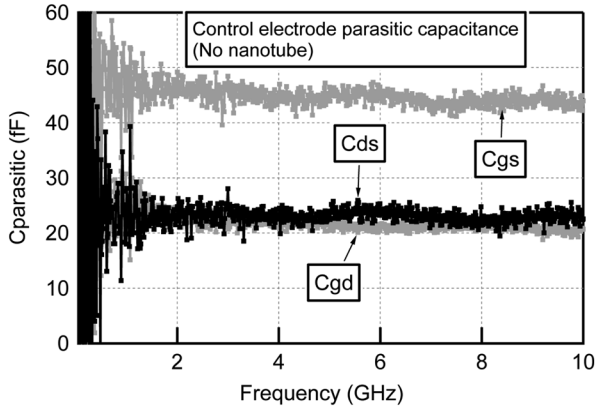

Fig. 3. **Parasitic capacitances.**. Measured electrode capacitances.

III. RF Characterization

A. Calibration

The microwave measurements were performed as follows: A commercially available microwave probe (suitable for calibration with a commercially available open/short/load calibration standard) allowed for transition from coax to lithographically fabricated on chip coplanar waveguide (CPW) electrodes. A microwave network analyzer is used to measure the full calibrated (complex) S parameters ($S_{11}, S_{12}, S_{21}, S_{22}$); the calibration procedure used a short/open/load/through (SOLT) cal on a commercial calibration standard. At the power levels used ($100\ \mu$W), the results are independent of the power used.

The calibration standard wafer does not have a finger geometry, so by measuring the S parameters of a control device with no nanotube, we are able to accurately determine the parasitic capacitance due to the finger electrodes; this is predominantly due to the fringing electric fields between the electrodes. From the measured S parameters on the control finger device, one can determine the Y matrix and then the capacitance (using the appropriate forms of the basic relationship $Y = i\omega C$), and hence one can easily determine the three important capacitances: $C_{\rm gs}$, $C_{\rm gd}$, $C_{\rm ds}$ (g, s, and d signifying gate, source, and drain, respectively). These are plotted in Fig. 3, which clearly shows a frequency independent capacitance, verifying the calibration and the model for the parasitics. The absolute values agree well with calculated capacitances based on the electrode geometry.

B. Cutoff Frequency

The common figure of merit for characterizing HF transistors is the cutoff frequency, defined as the frequency at which the current gain (H_{21}) falls to 0 dB. In our devices, because the parasitic capacitance is so large compared to the gate-source capacitance required to modulate the conductance, the cutoff frequency is limited by this parasitic. By measuring the entire device S parameters, we extract a cutoff frequency of 0.2 GHz, shown in Fig. 4.

Since we know the parasitic capacitances very well, these can be "subtracted off" to determine "intrinsic" device performance. Again, "intrinsic" means that the parasitic capacitance due to fringing fields is negligible compared to the gate-source capacitance required to modulate the conductance. In practice this de-embedding procedure is carried out by taking the measured

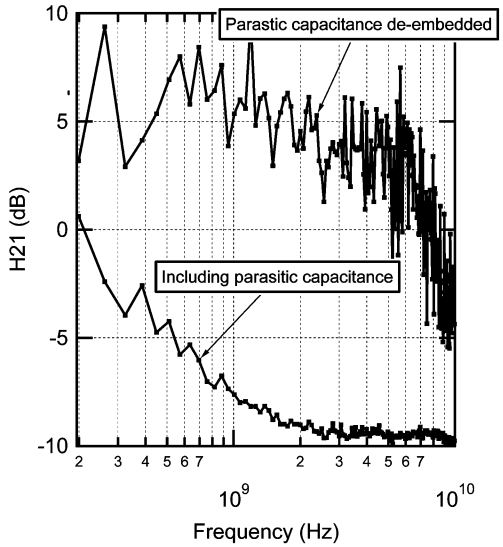

Fig. 4. **Determination of cutoff frequency.** Current gain H_{21} versus frequency before and after de-embedding the parasitic capacitance, at $V_{\rm ds} = 0.5$ V, $V_{\rm gate} = 2$ V. The gray dotted line shows extrapolation curve used to determine the frequency at which H_{21} drops to 0 dB.

Y matrix and subtracting the control (open) Y matrix of the fingers only (determined in a separate matrix), resulting in the "intrinsic" Y matrix: $Y_{\rm intrinsic} = Y_{\rm measured} - Y_{\rm control}$. Then, $Y_{\rm intrinsic}$ can by used to find the intrinsic (de-embedded) S, h, Z, and ABCD matrix [20]. After performing this procedure, we find the data shown in the upper curve in Fig. 4. The intrinsic capacitance is of order fF, whereas the parasitic capacitance is of order 50 fF, so that the de-embedded H_{21} data displays scatter on the order of a few dB. In order to determine the intrinsic cutoff frequency (the frequency at which the de-embedded current gain H_{21} drops to 0 dB), we used the extrapolation curve shown by grey dots in Fig. 4, formed by fitting a line to H_{21} (dB) versus frequency over the range covered by the grey dots. Using this procedure, we find a cutoff frequency of 7.6 GHz. This is one of the largest cutoff frequencies ever measured on nanotube FETs.

C. $f_{\rm max}$

A second common figure of merit is the frequency at which the maximum stable gain (defined as S_{21}/S_{12}) drops to 0 dB. In practice the conditions on stability and $f_{\rm MAX}$ depend on all four S parameters [11], so this is not always a direct measure of $f_{\rm MAX}$, the maximum frequency of oscillation. However, it is fairly straightforward to measure as one directly measures S_{12} and S_{21}, and so commonly use as a "poor man's" figure of merit. In Fig. 5, we plot the MSG before and after de-embedding the parasitic capacitances. The curve extrapolates to 15 GHz, which is one of the highest MSG ever reported for a nanotube device.

IV. Conclusion

We have clearly established that the de-embedded cutoff frequency may be useful for measuring ultimate device performance, but in a real circuit as soon as electrodes are attached they must be accounted for in any application, especially in

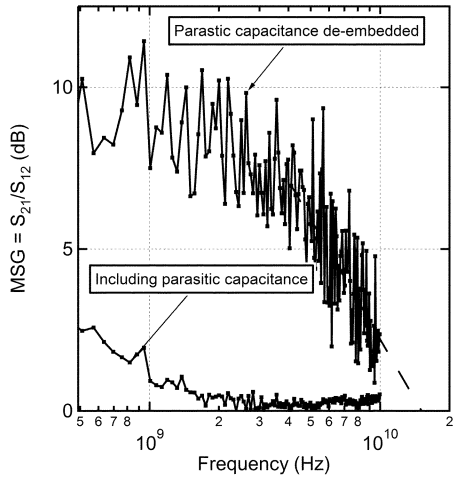

Fig. 5. **Determination of $f_{\rm MAX}$.** MSG before and after de-embedding the parasitic capacitances. The curve extrapolates to 15 GHz.

nanocircuits. In other words, the de-embedded device performance may be outstanding, but it is critical to quantify and characterize any contacting electrodes before devices can be used in any sort of a circuit.

The importance of parasitics on the cutoff frequency of nanotubes was first pointed out in [1], and subsequently, using more careful and varied analyses, in [3]–[5] and [21]. The present measurements, with de-embedded parasitics, clearly establish that transistor action persists all the way to 10 GHz in carbon nanotube transistors. Work to minimize the parasitics, as well as establish more sophisticated RF circuit models for the nanotube intrinsic performance, is currently under way, which will enable the application of nanotube devices in integrated circuits and, eventually, systems.

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