Spiking Neural Network Accelerator

Phase 2 Report

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Contents

1 Introduction

In this project, we are going to complete a spike neuron network (SNN) and a network on chip (NOC). In this report, we are going to include some sub-blocks of these systems.

In this project, we are using System Verilog to design. The protocol we use is 2-phase bundled data. The design mainly consists of several parts: NOC, 3 processing elements (PE), a memory unit and a sum unit. Each component has its own test-benches. Our main objective of this project is to search for some operations to improve the efficiency of our system.

The report will contain following parts:

- Overall architecture of our system
- Description of each component
- Verification and simulation results

2 Overall Architecture

In our design, we decide to use a tree topology for our NOC, which has 5 nodes for 3 PEs, one memory unit and one sum unit. This architecture is shown in Fig.1. In

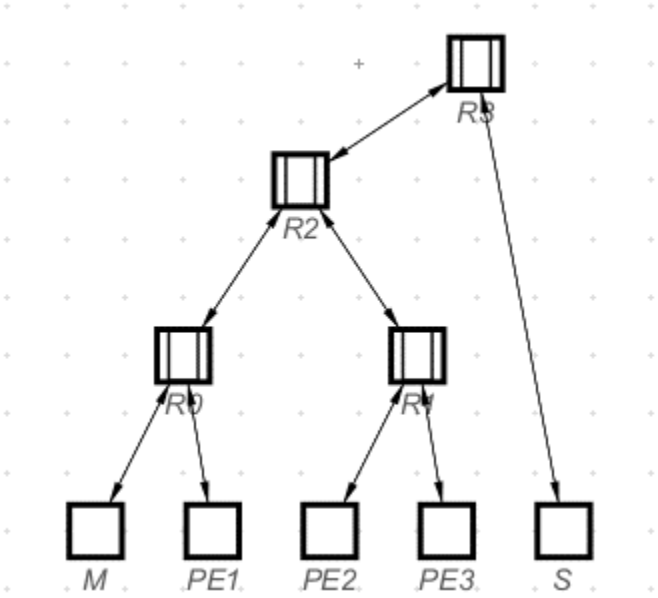


Figure 1: Architecture of our System

our design, we decide to use a fixed 32-bit packet of data to be transferred on our NOC. The detailed information of the packet is shown in Fig.2.

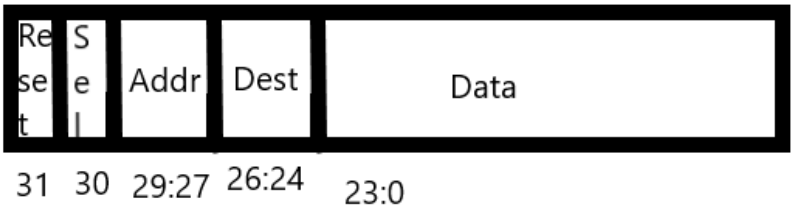
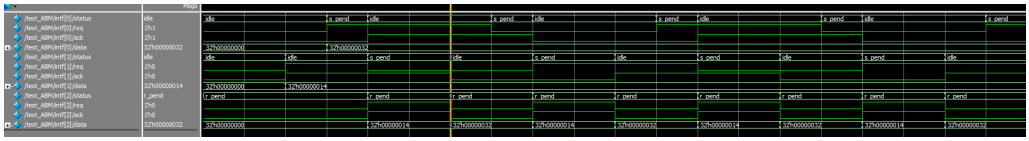


Figure 2: Packet Information

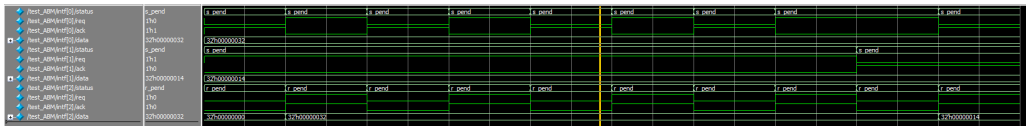
- [31]: One bit reset signal
- [30]: One bit select signal to tell the PE whether the data is from kernel of input feature map
- [29 : 27]: 3 bits of address to tell from which node the data is sent
- [26 : 24]: 3 bits of destination address to tell to which node the data is sent
- [23 : 20]: 24 bits of data

3 Arbitrated Merge Module

The arbitrated merge is the composition of arbiter and merge, which order the two inputs first and then send the winner to the output. This part would select the input channels and send the first arrived channel data to the output channel. To test this module, we have run several simulations, and the results are shown in Fig.3.



(a) One Channel Idle Case

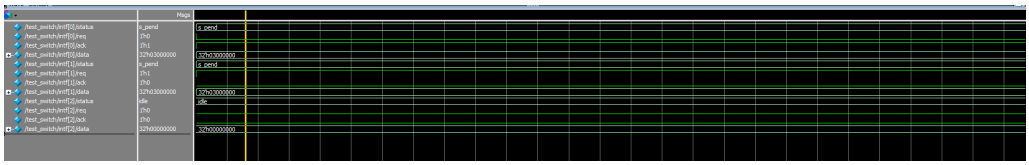


(b) No Channel Idle Case

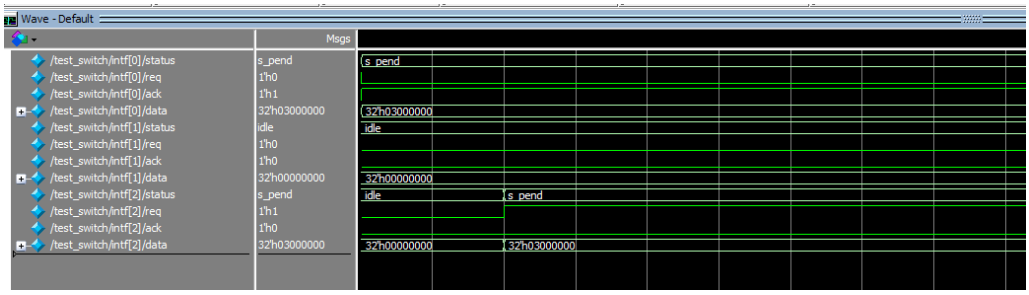
Figure 3: Simulation Results of Arbitrated Merge Module

4 Switch Module

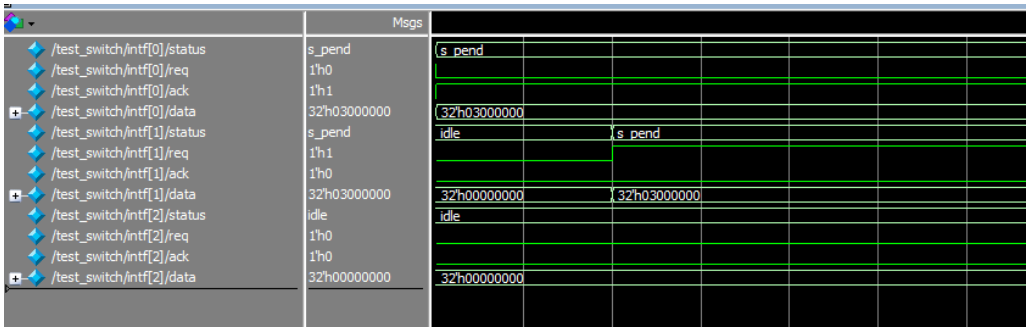
In router, switch part is used to decide if the input channels are parent or child. If the input come from a parent channel, the switch would base on the mask and address value to determine the output channel as the child1 or child2. If the input comes from the child channel, the switch is responsible to decide if the input should go to other child channel or the parent channel base on the dest & mask calculation. The switch outputs should connect to the arbitrated merge which are the router inside connection. We tested three cases of the switch module, and the results are shown in Fig.4. In all these three cases, dest = 011.



(a) Parent Side Input, Mask=000, Addr=000



(b) Parent Side Input, Mask=110, Addr=100



(c) Child Side Input, Mask=110, Addr=100

Figure 4: Simulation Results of Switch Module

5 Processing Element

5.1 Function Unit

The function unit stores one row of the kernel and three continuous elements in a row of input feature map. These data come from de-packetizer. It calculate the dot product of these two arrays, and output a partial sum to the packetizer. In our simulation, we take the kernel row to be [14 5 8] and the input spike is [1 0 1]. The simulation results is shown in Fig.5, and we get the correct partial sum, which is 22.

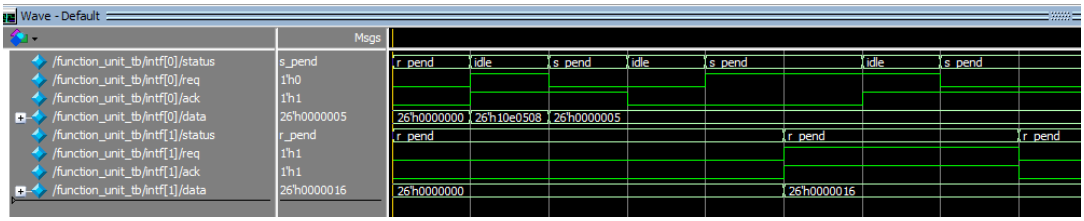


Figure 5: PE Function Unit Simulation Result

6 Work to be Completed

There are still some work uncompleted, which are list as follows:

- Router
- NOC
- Gate level module
- Packtizer and de-packtizer
- Integration of system