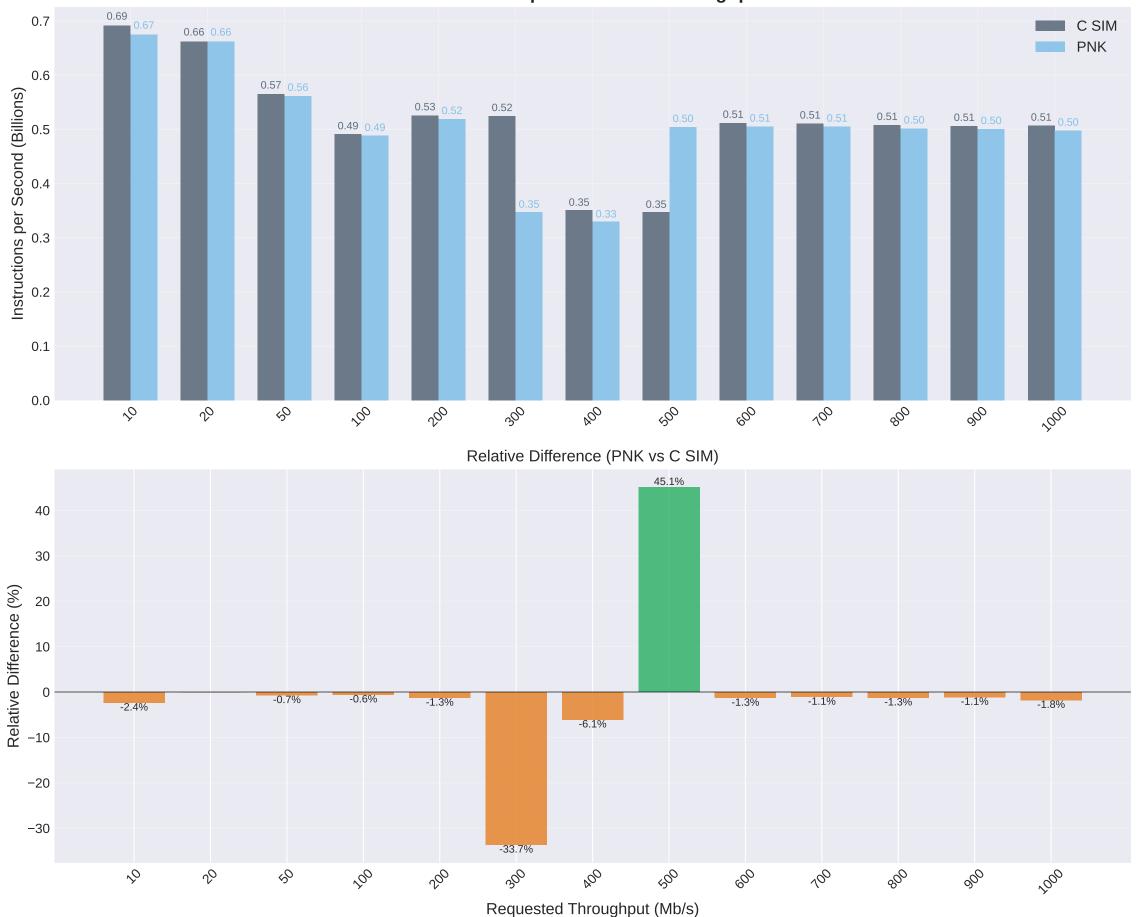
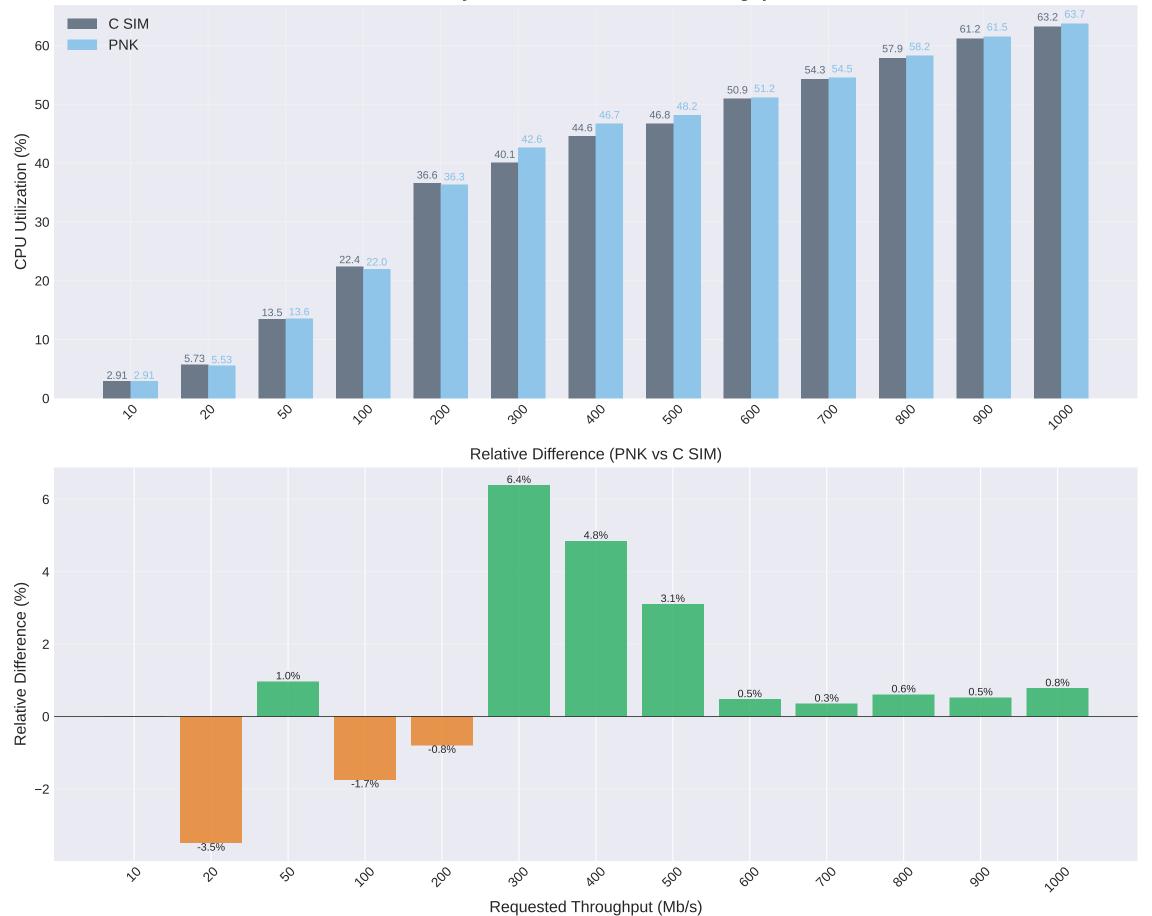
Instructions per Second vs Throughput

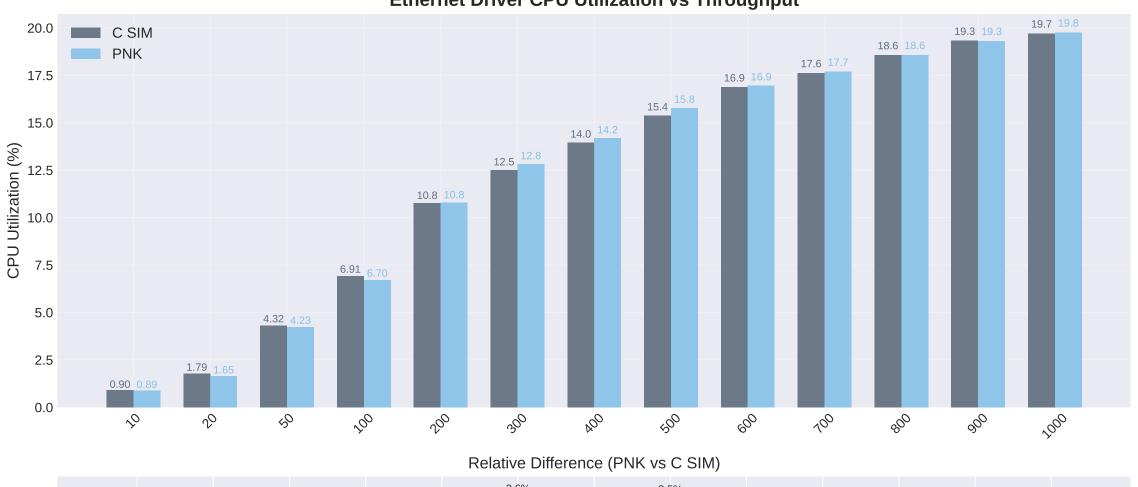


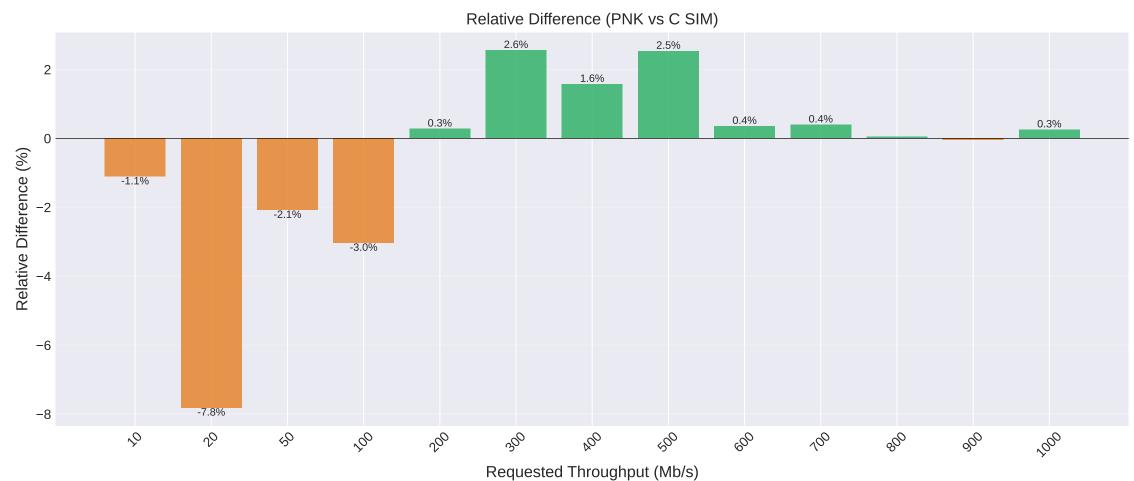
Received Throughput vs Requested with CPU Utilization Overlay 1000 C SIM Recv Throughput 957.3957.0 100 PNK Recv Throughput C SIM CPU Util 900.0900.0 PNK CPU Util 800.0800.0 800 80 700.0700.0 Received Throughput (Mb/s) 63.7% 61.5% 600.0600.0 600 CPU Utilization (%) 58.2% 54.5% 51.2% 500.0500.0 46.7% 400 300.0300.0 200.0200.0 200 20 100.0100.0 50.0 50.0 2.9% 20.0 20 0 900 200 go NOO 400 2000 700 600 100 900 20 20 50

Total System CPU Utilization vs Throughput

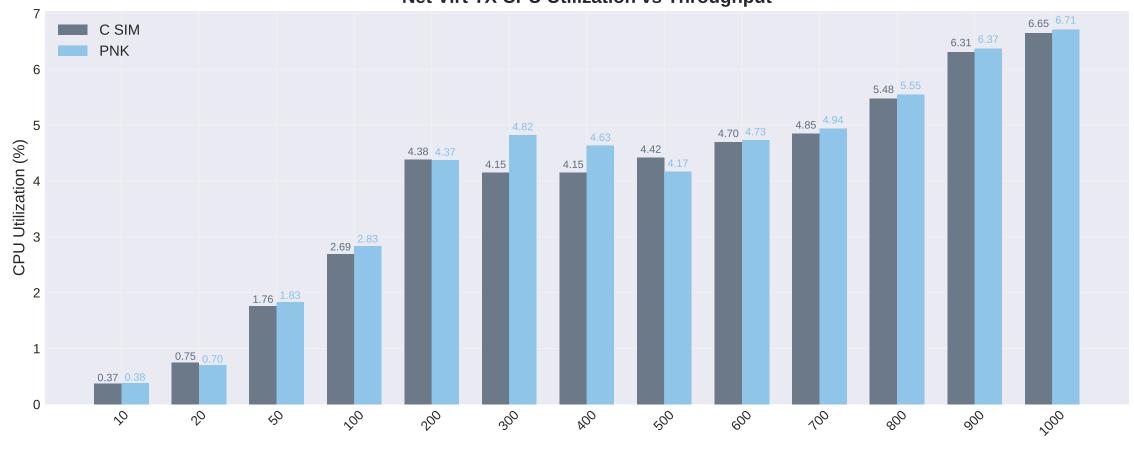


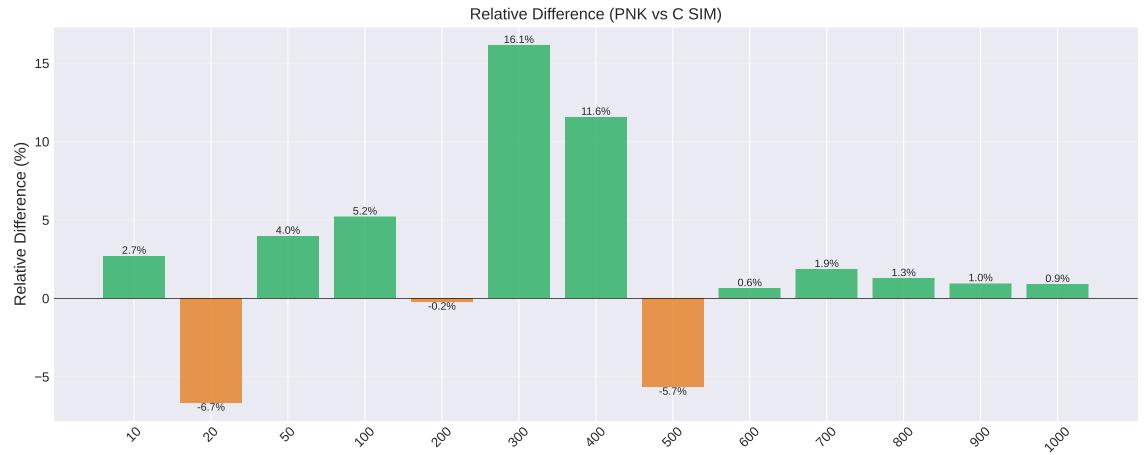
Ethernet Driver CPU Utilization vs Throughput



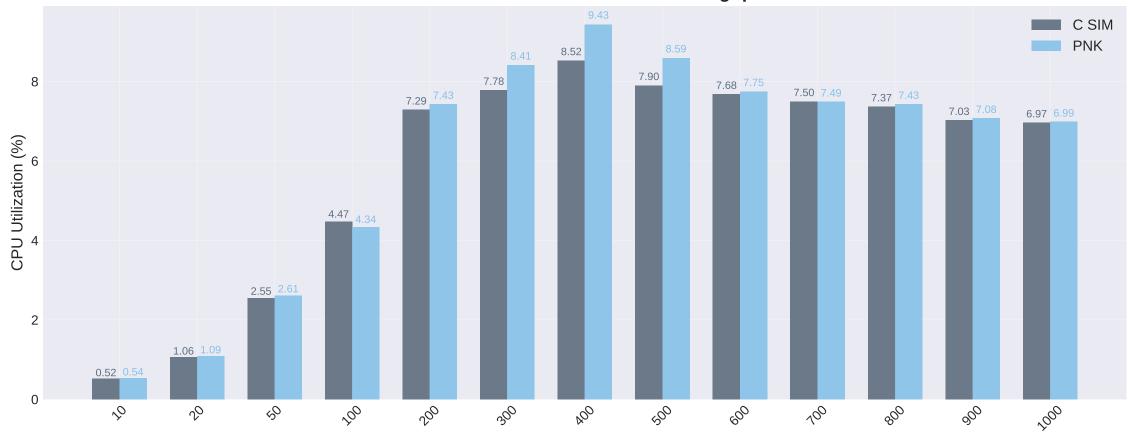


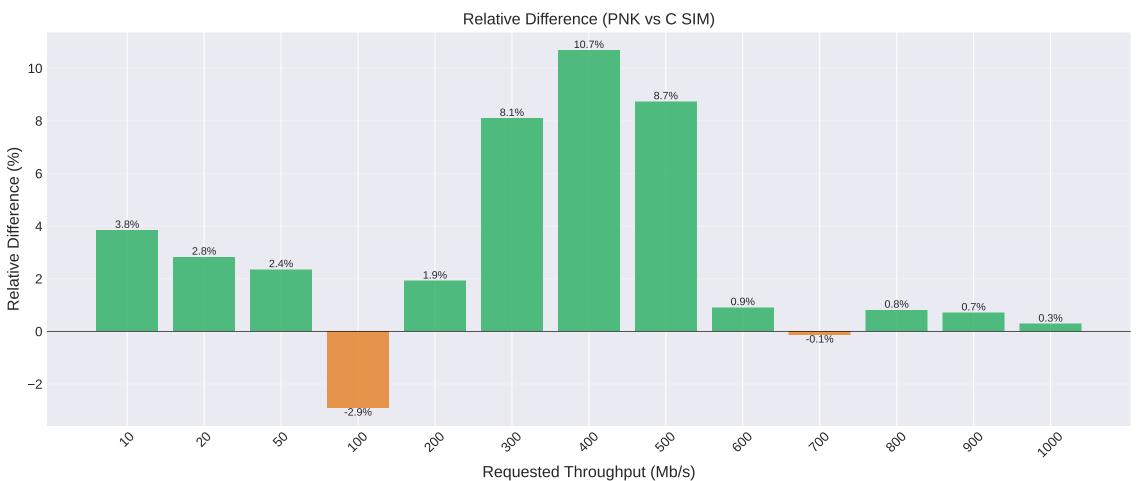




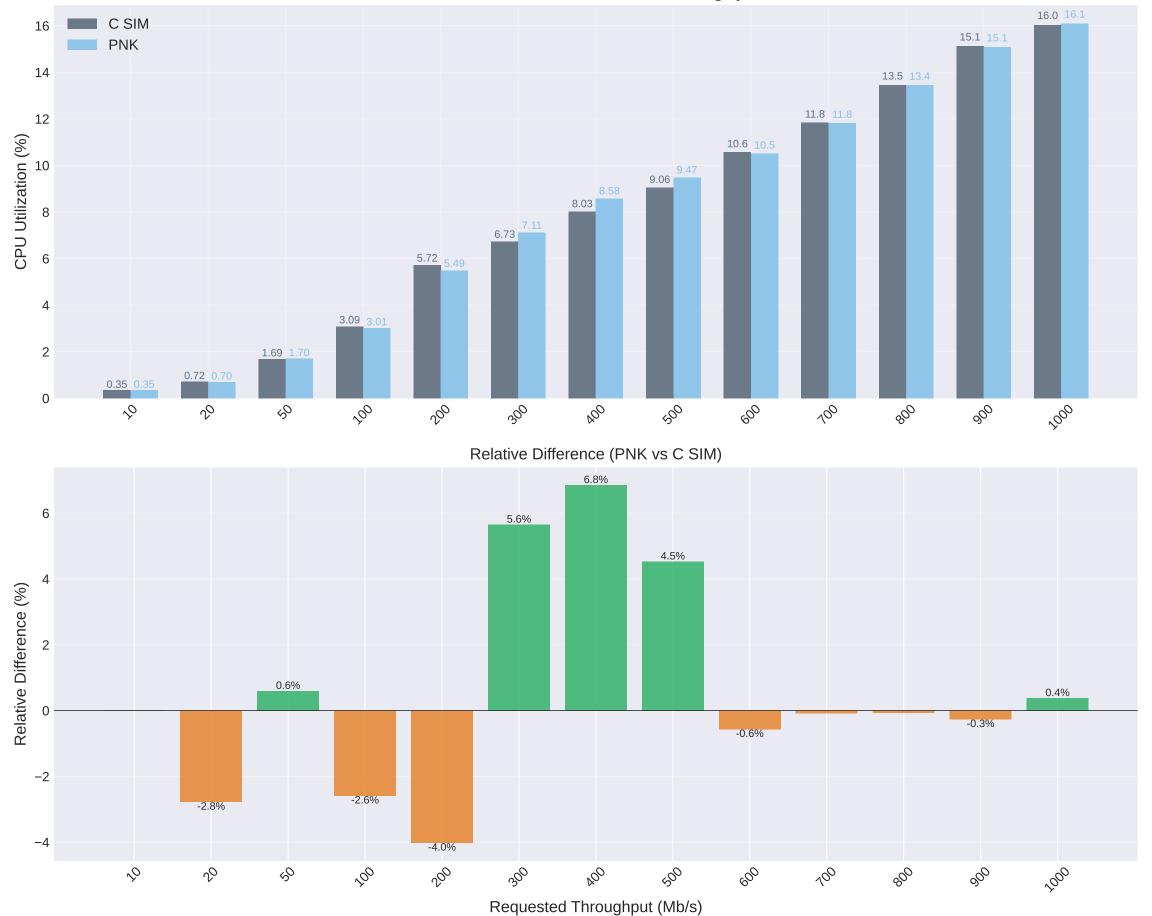


Net Virt RX CPU Utilization vs Throughput

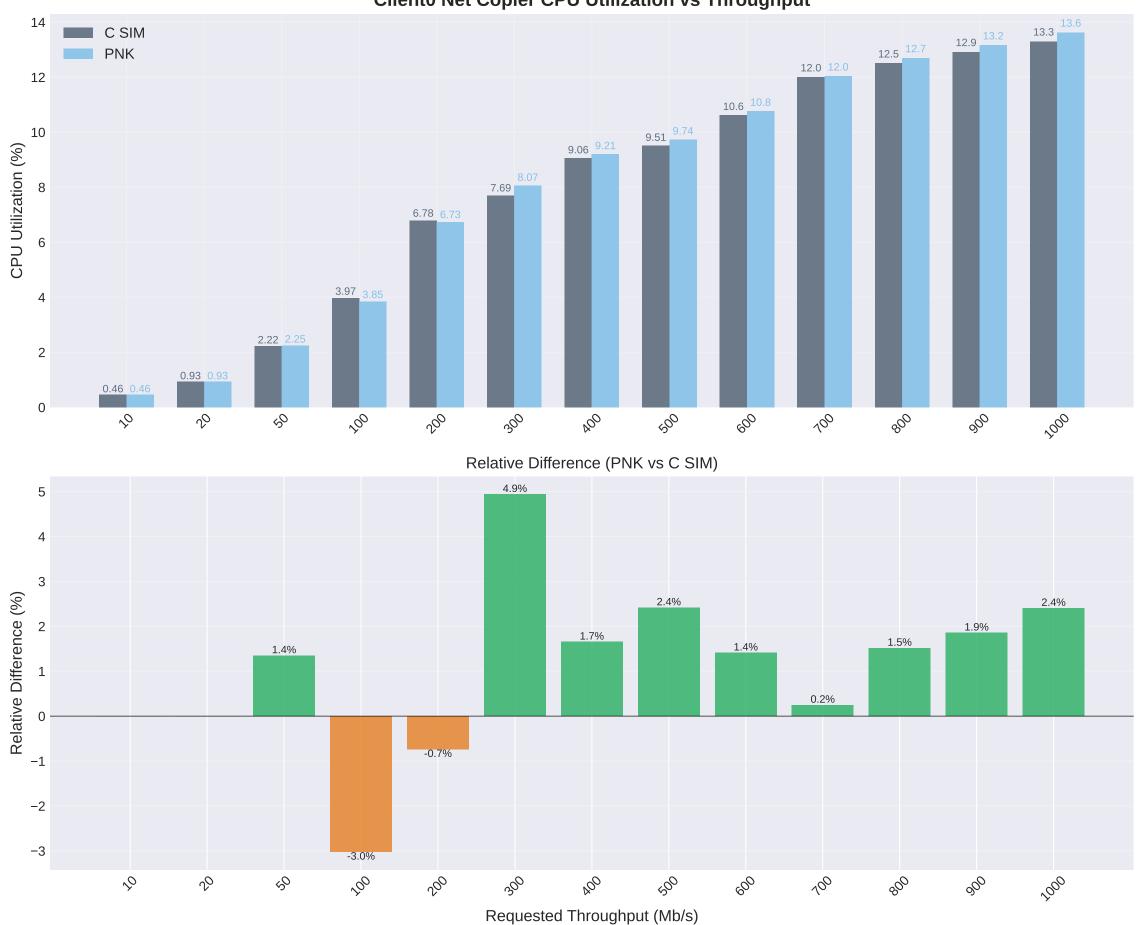




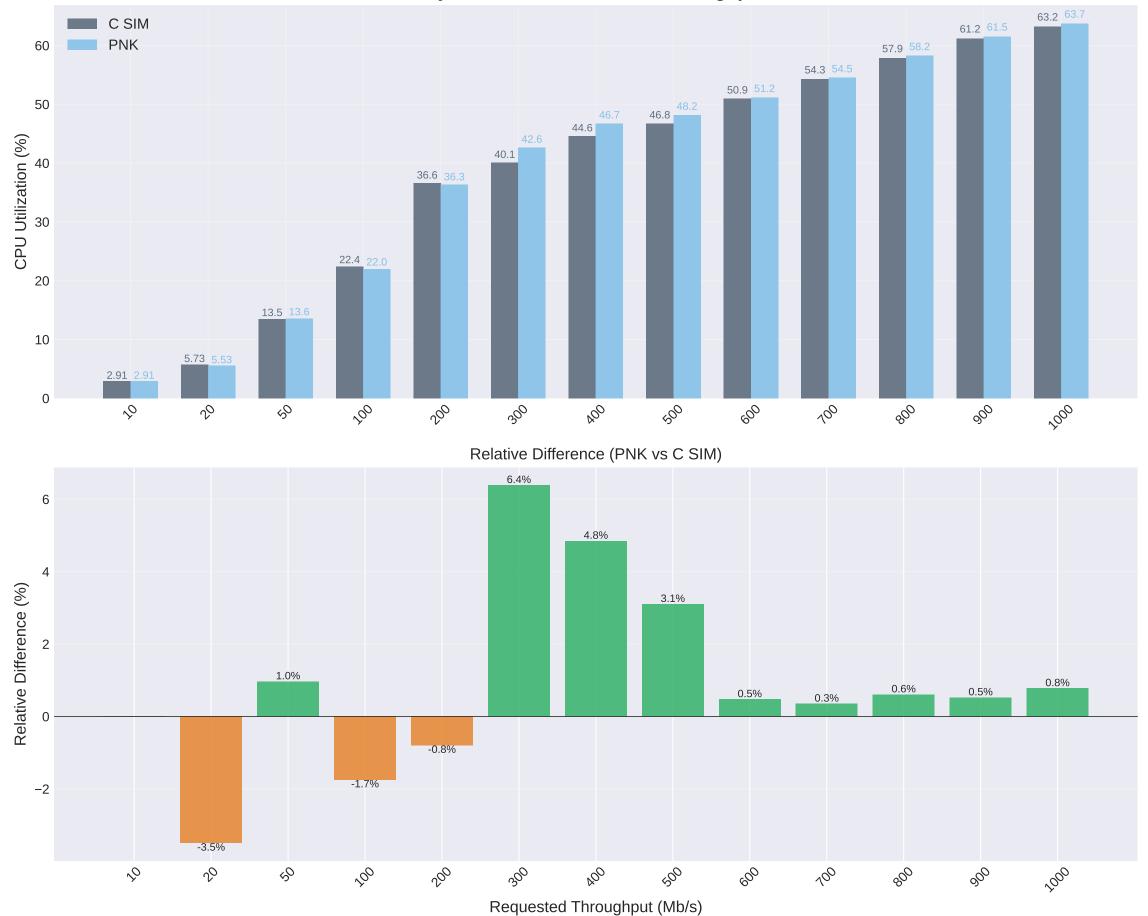
Client0 CPU Utilization vs Throughput

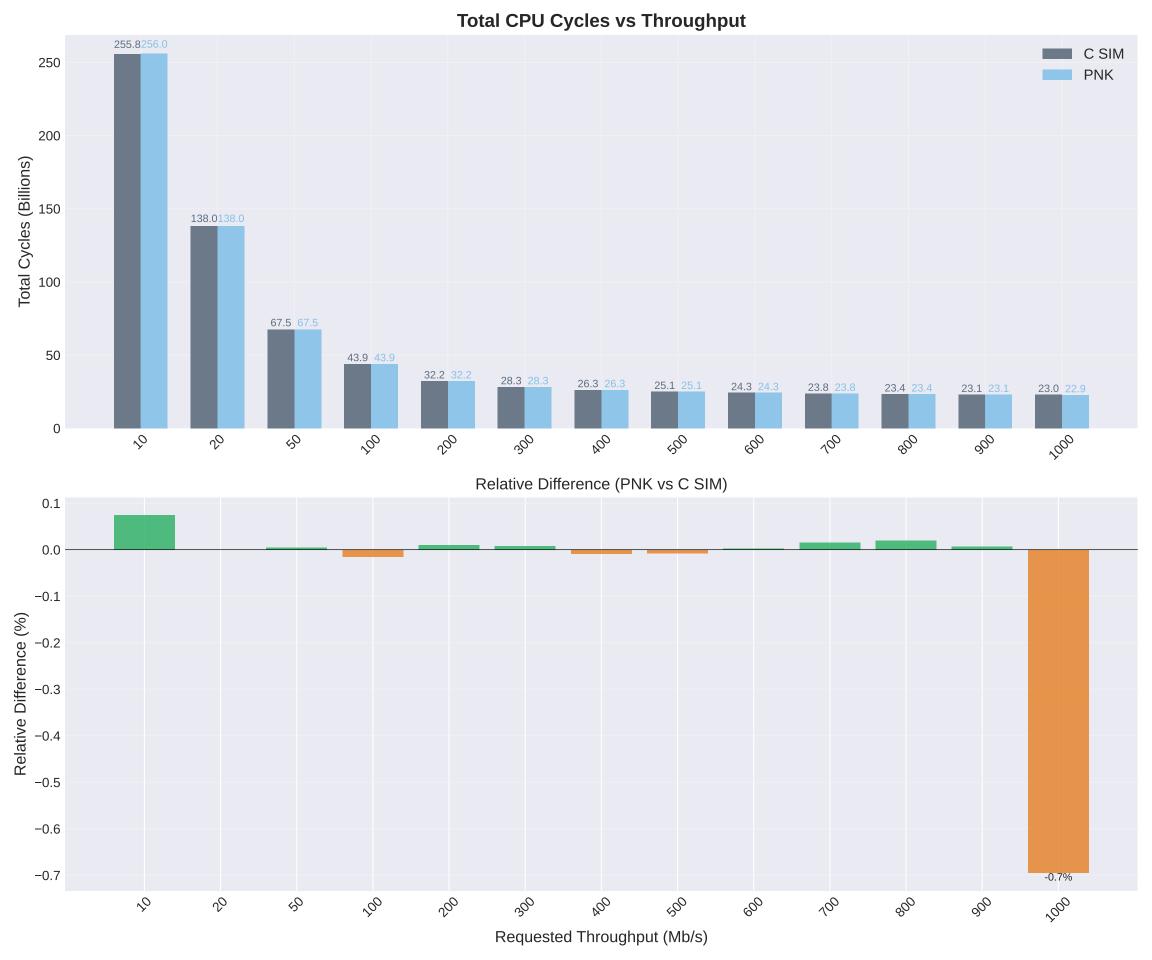


Client0 Net Copier CPU Utilization vs Throughput

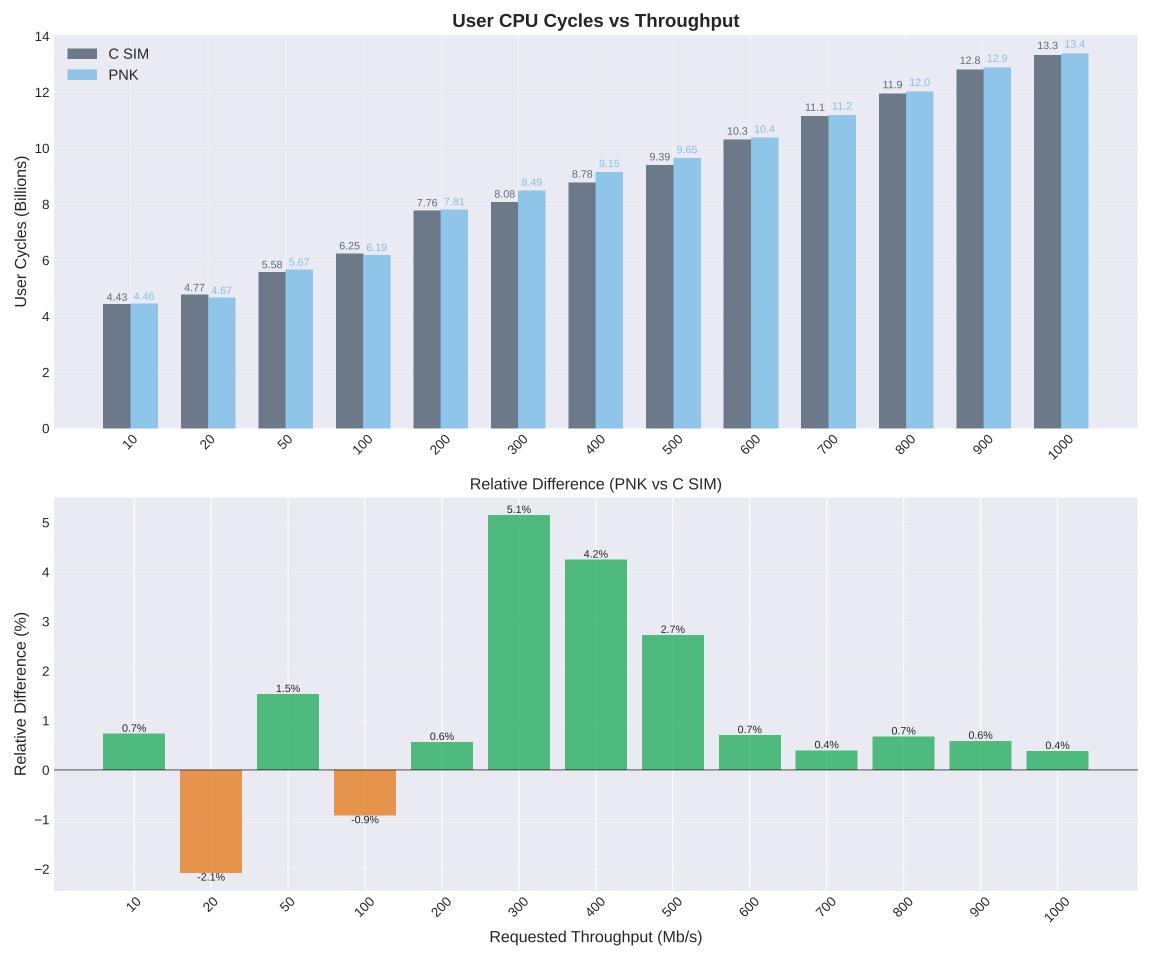


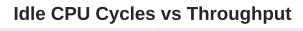
System CPU Utilization vs Throughput

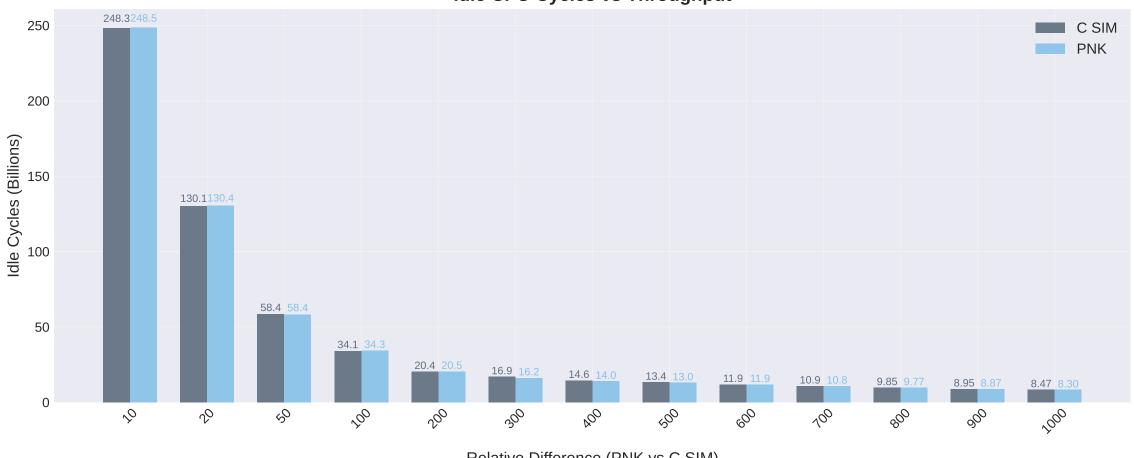


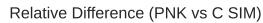


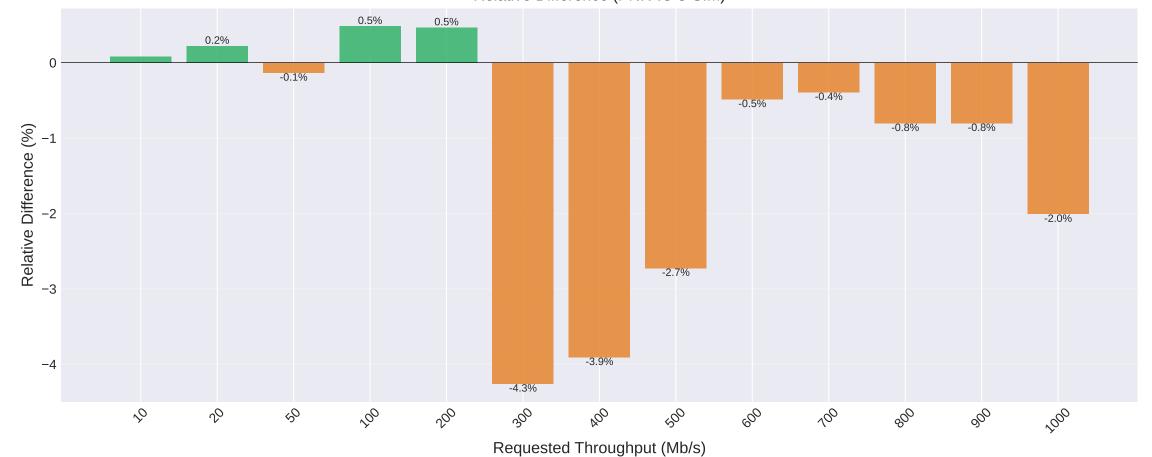
Kernel CPU Cycles vs Throughput C SIM 3.5 PNK 3.06 2.96 2.92 2.89 2.93 3.0 2.72 2.51 Kernel Cycles (Billions) 2.34 2.32 2.30 2.23 1.97 1.96 1.69 1.69 1.49 1.50 1.21 1.21 1.13 1.09 1.0 0.5 0.0 700 200 300 NOO 400 600 700 900 900 2000 30 20 60 Relative Difference (PNK vs C SIM) 8.8% 8.7% 8 6 4.9% Relative Difference (%) 0.2% -0.2% -0.7% -0.8% -1.0% -2 -2.2% -3.2% -4 -3.9% -5.0% \$0 20 60 200 200 300 NOO 400 100 900 Requested Throughput (Mb/s)



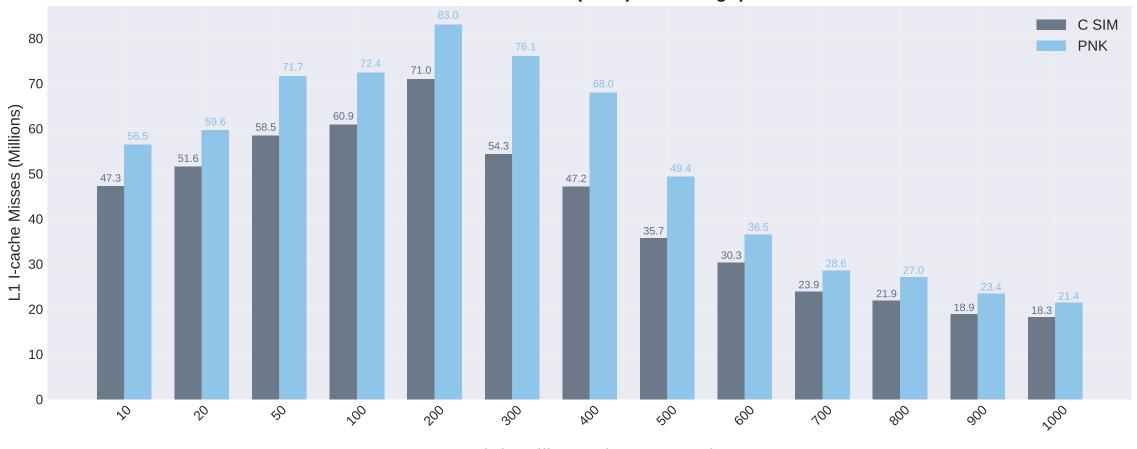


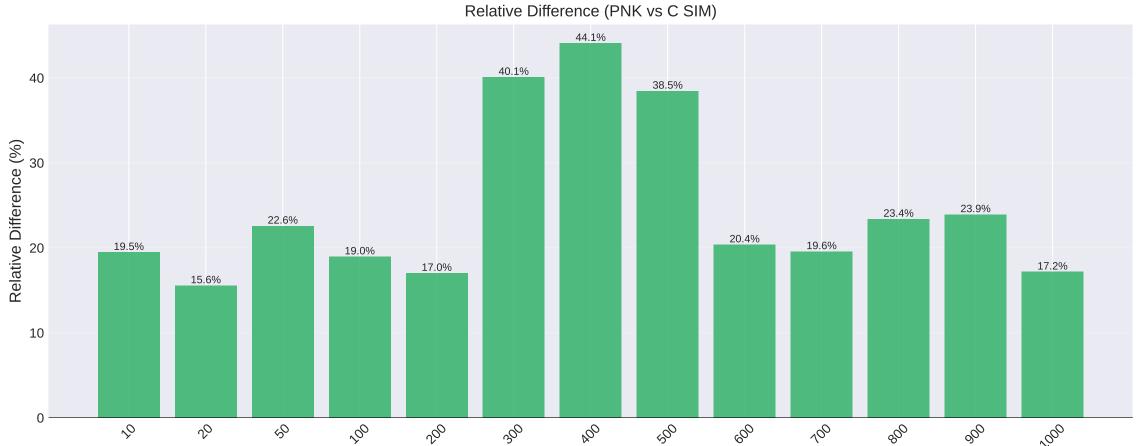






L1 I-cache Misses (Total) vs Throughput

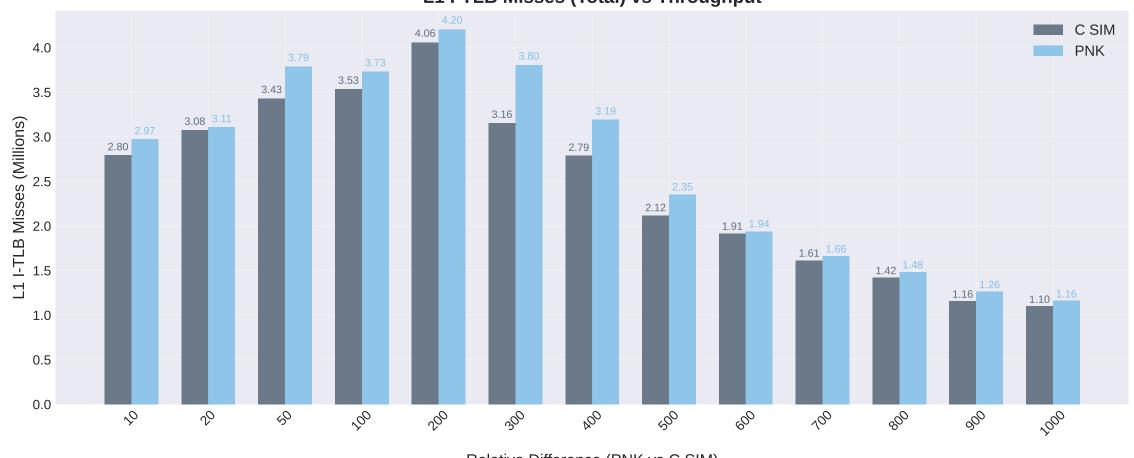


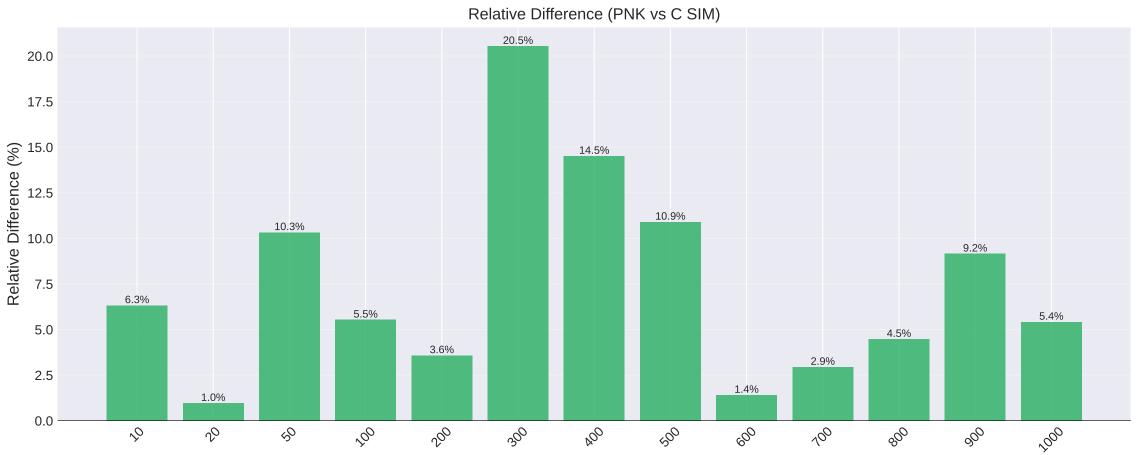


L1 D-cache Misses (Total) vs Throughput

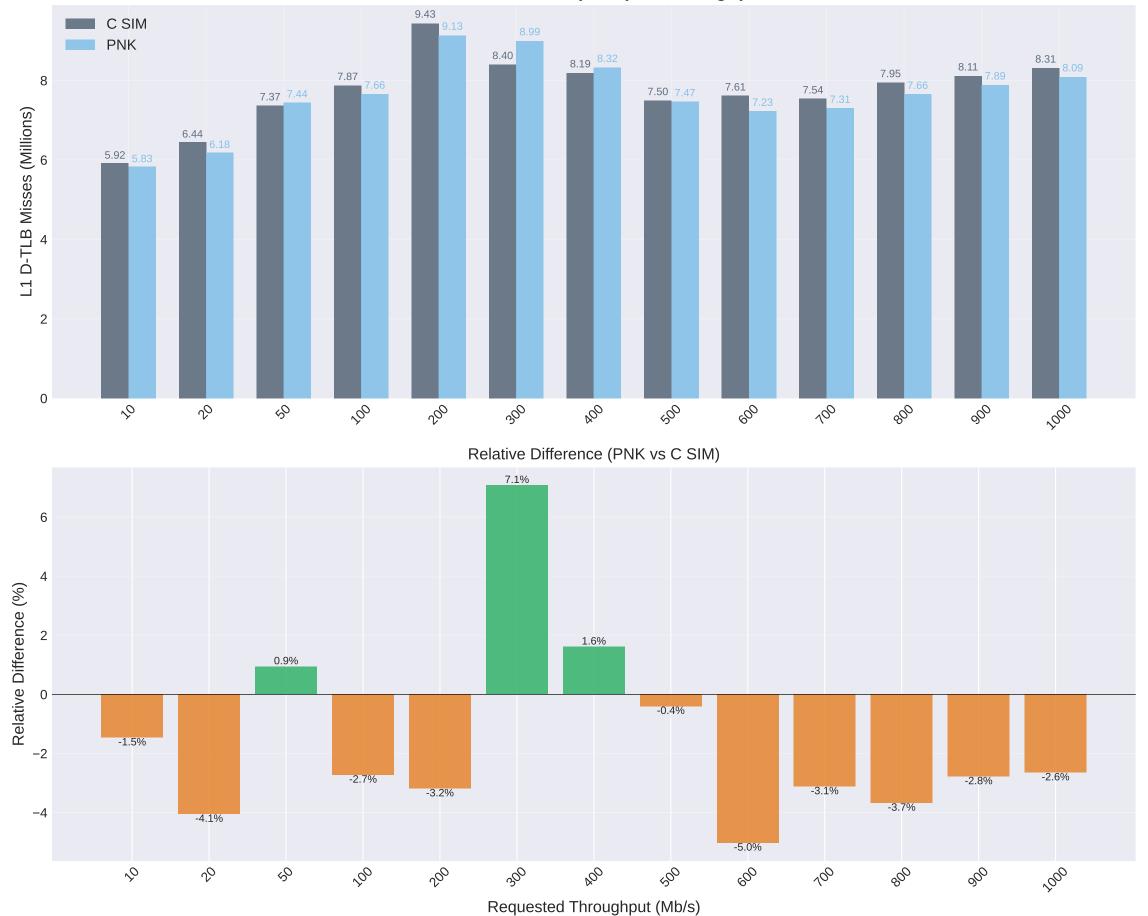


L1 I-TLB Misses (Total) vs Throughput

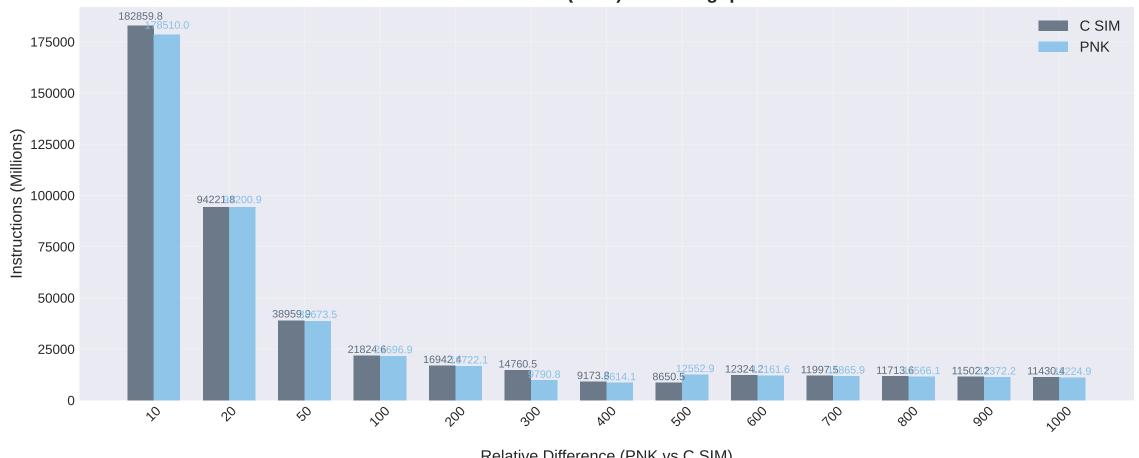


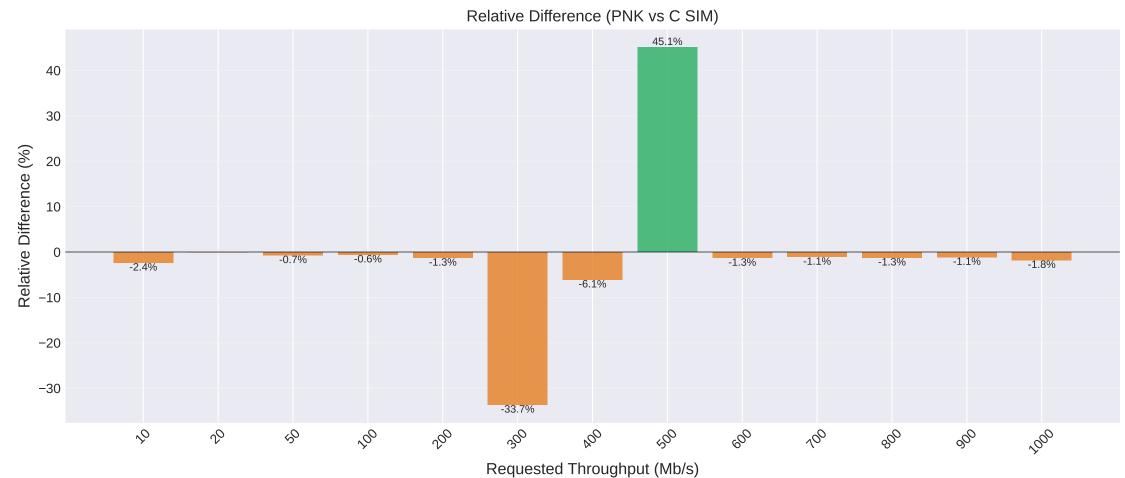


L1 D-TLB Misses (Total) vs Throughput

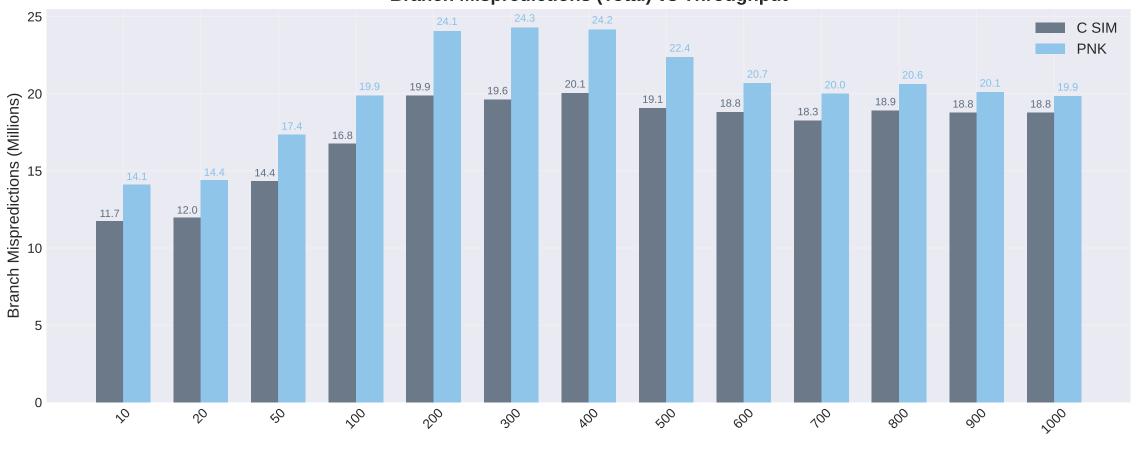


Instructions (Total) vs Throughput

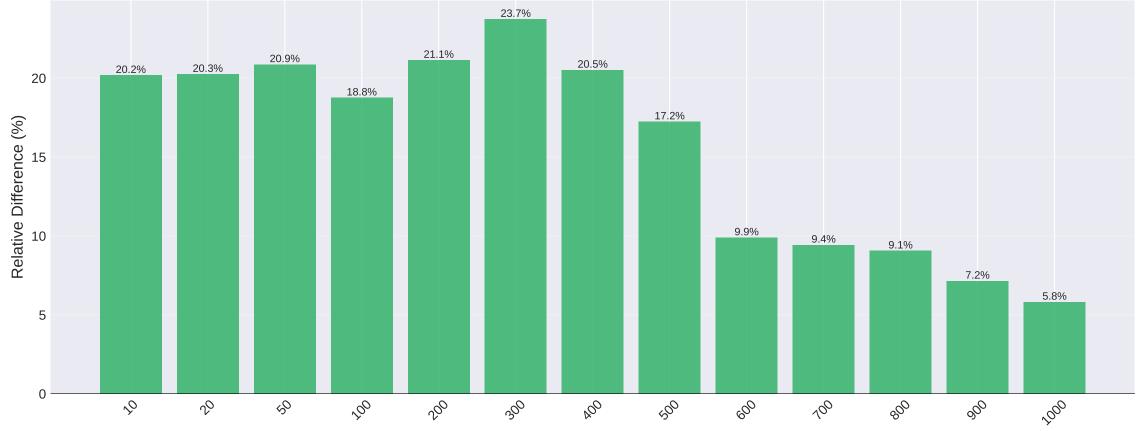




Branch Mispredictions (Total) vs Throughput

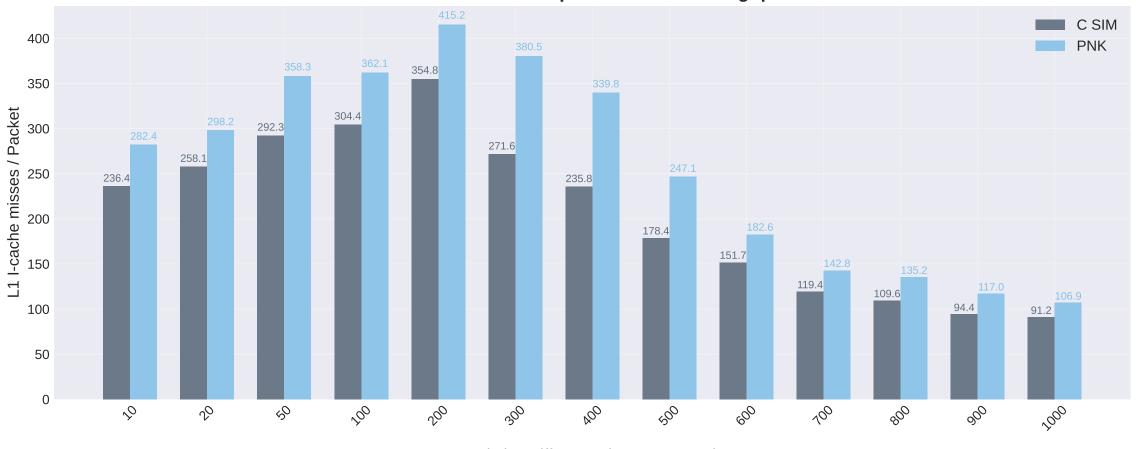


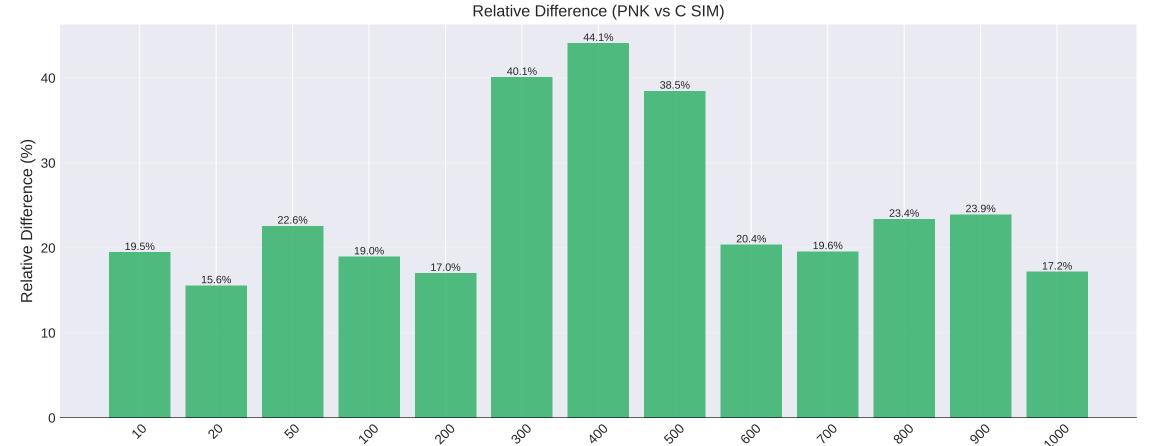




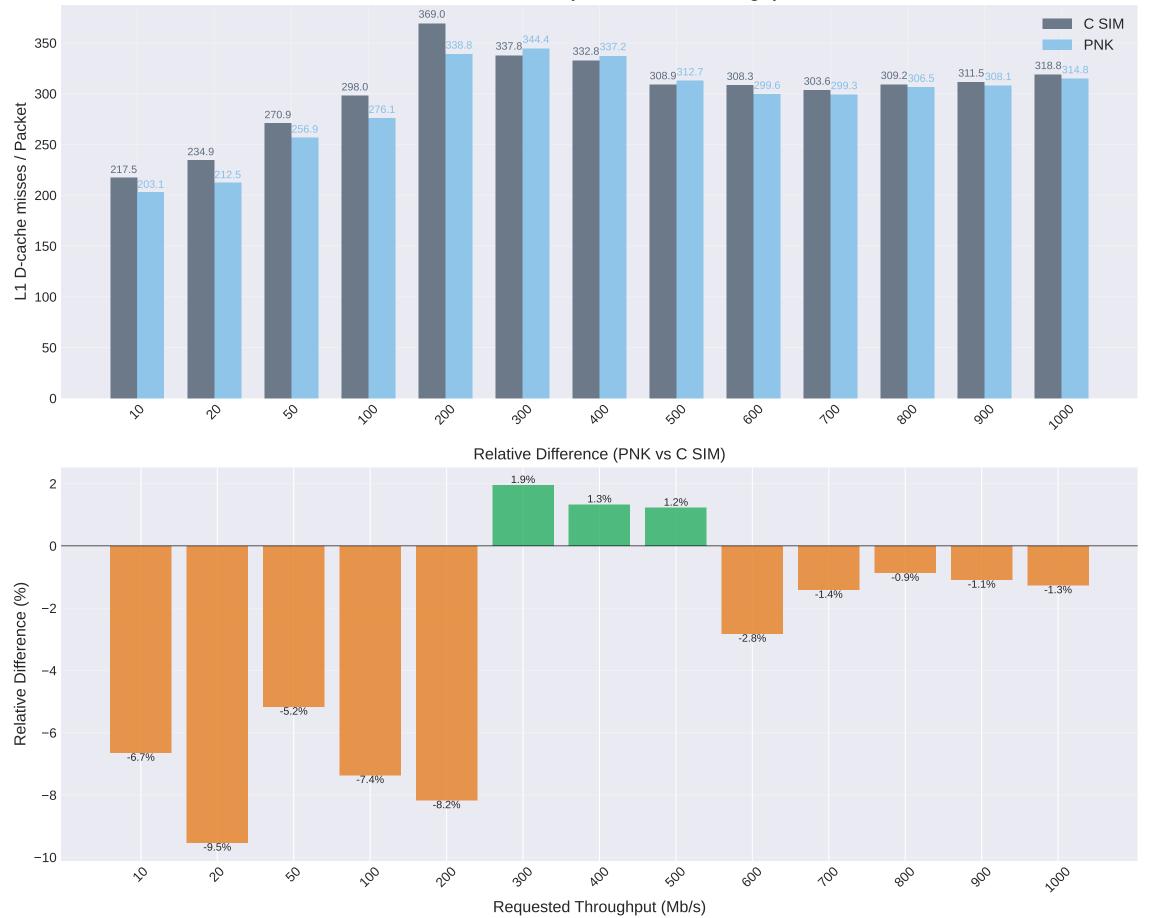
Requested Throughput (Mb/s)

L1 I-cache Misses per Packet vs Throughput

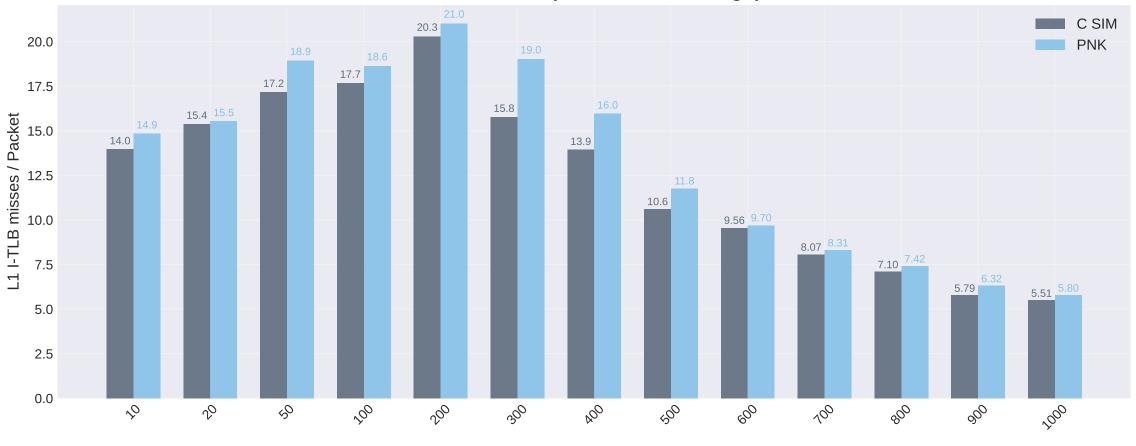


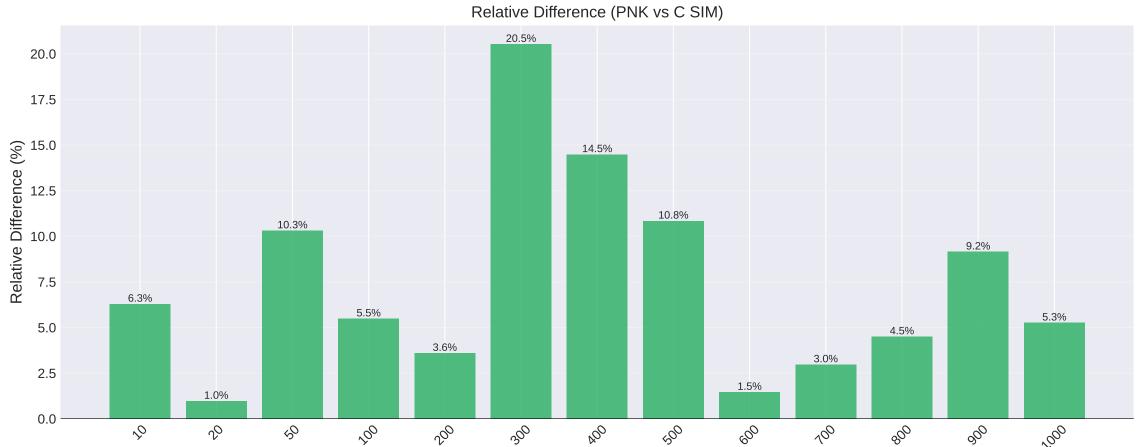


L1 D-cache Misses per Packet vs Throughput

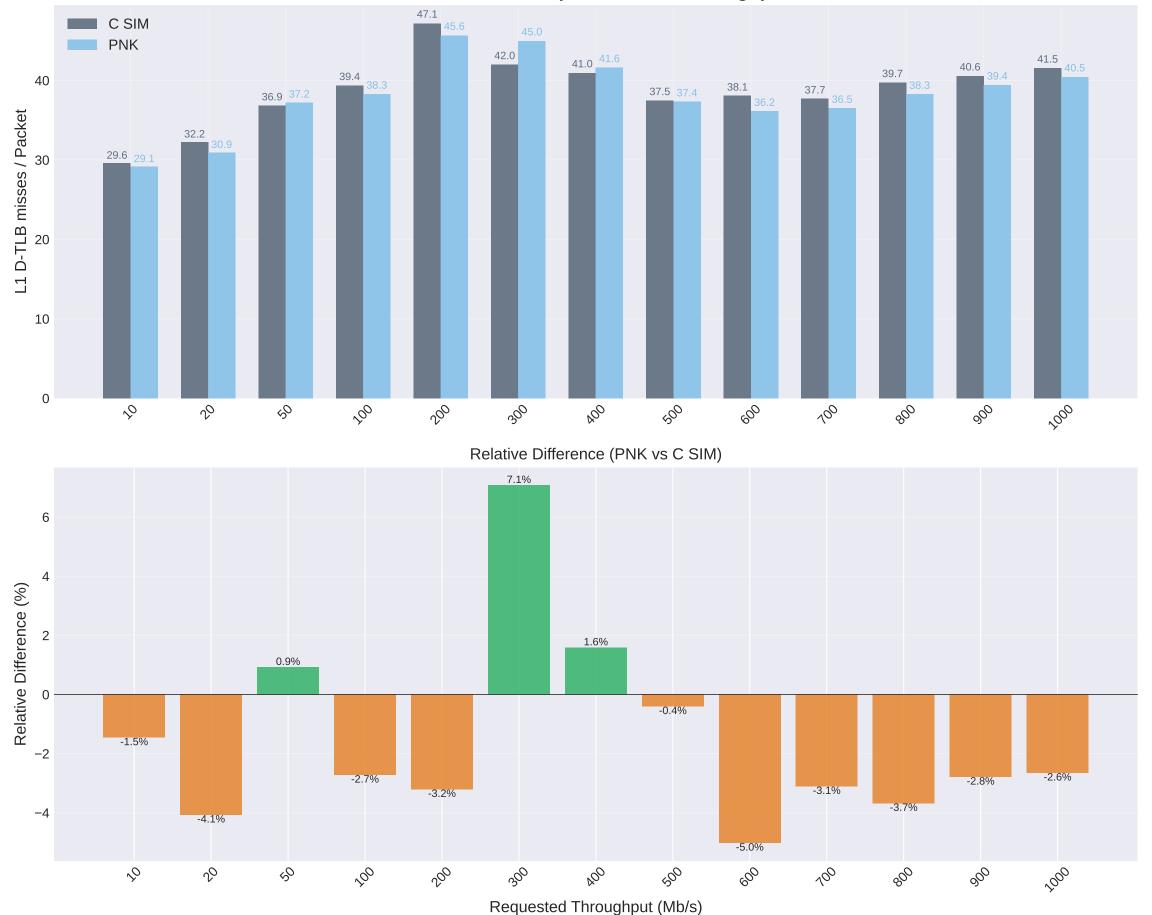


L1 I-TLB Misses per Packet vs Throughput

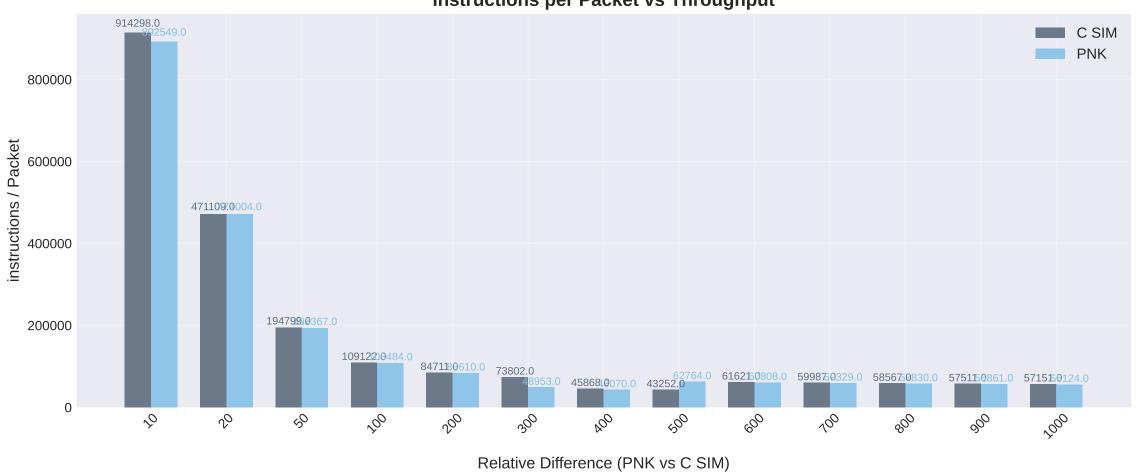


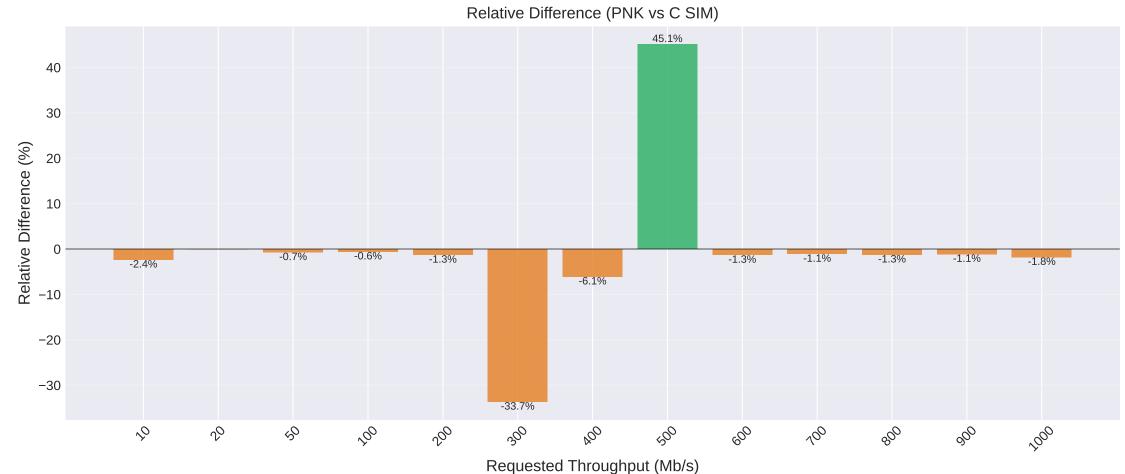


L1 D-TLB Misses per Packet vs Throughput

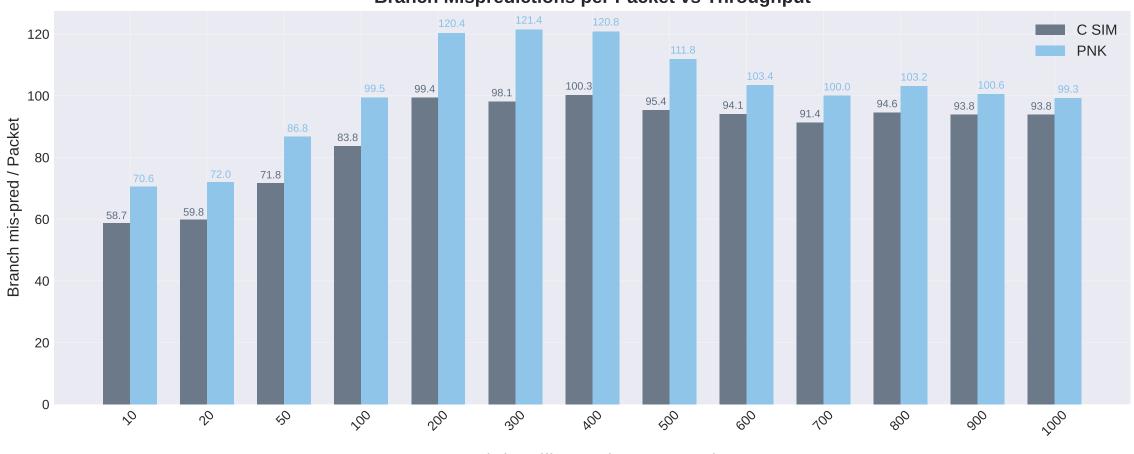


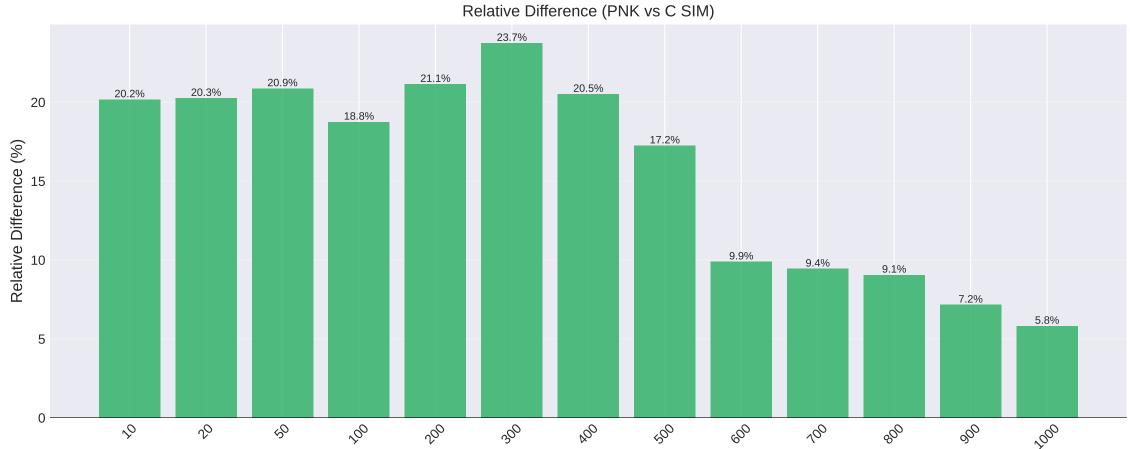
Instructions per Packet vs Throughput

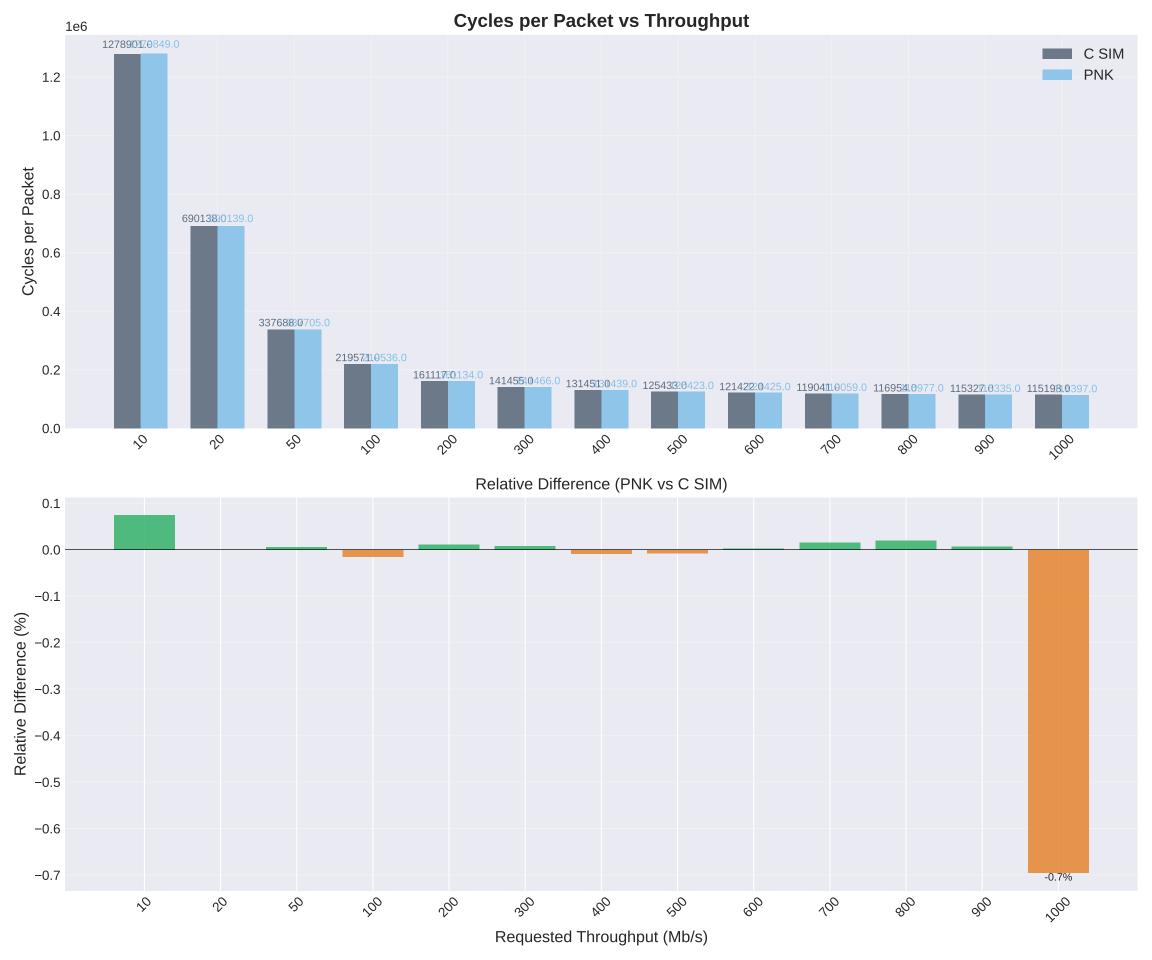




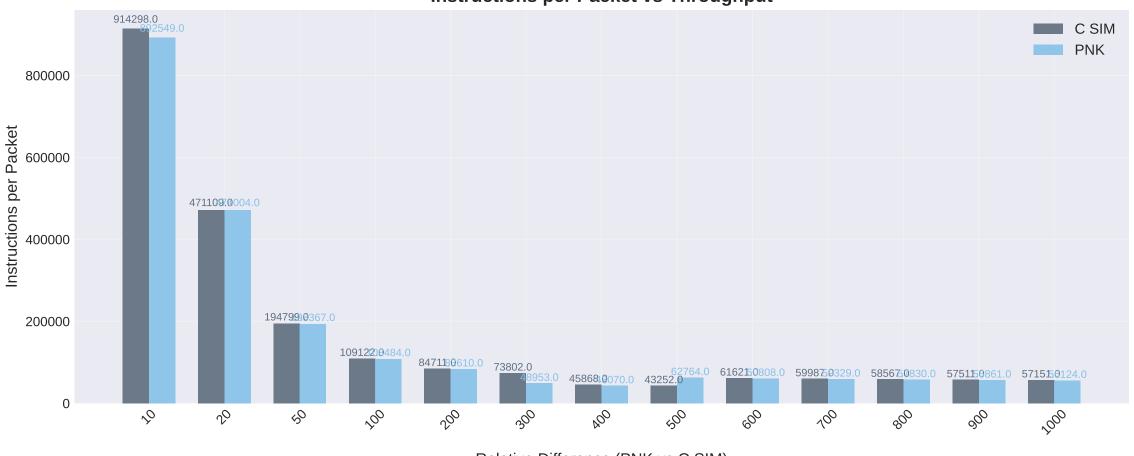
Branch Mispredictions per Packet vs Throughput

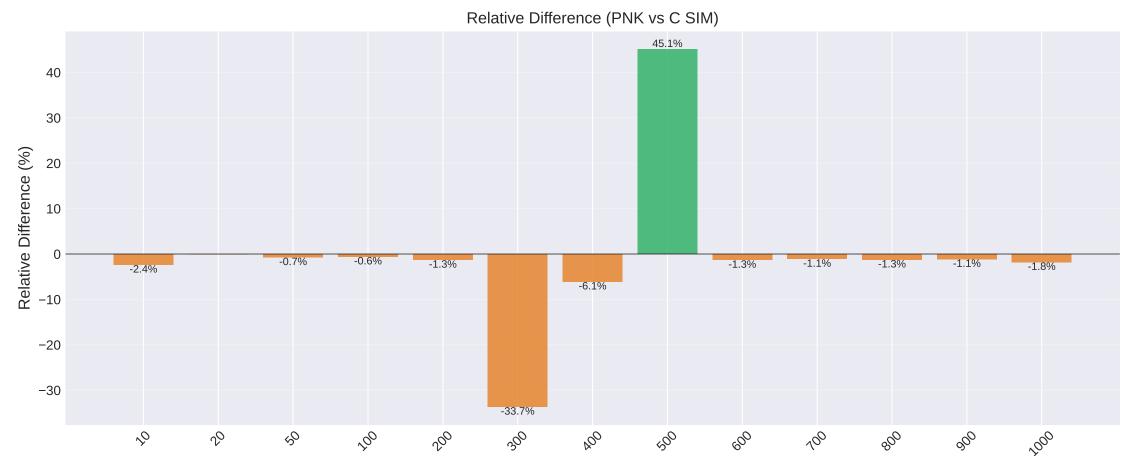




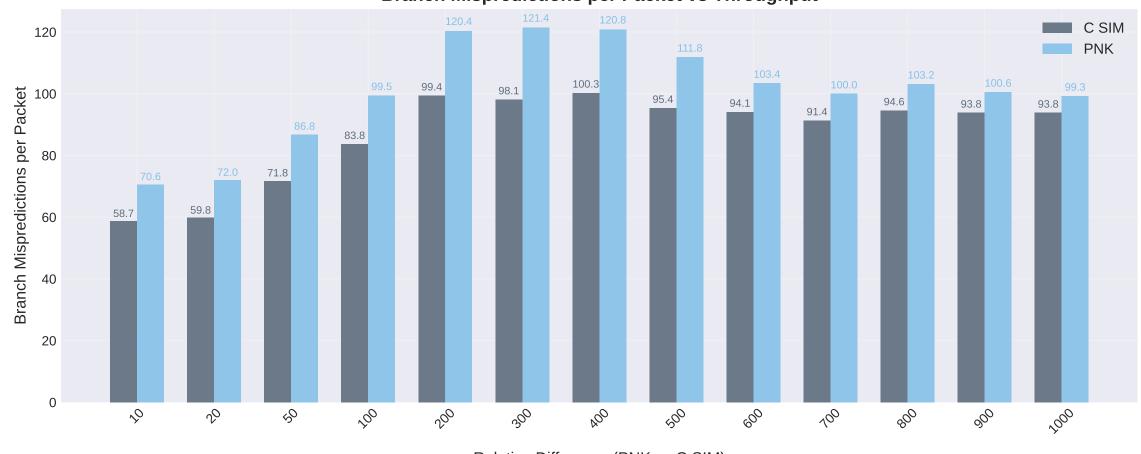


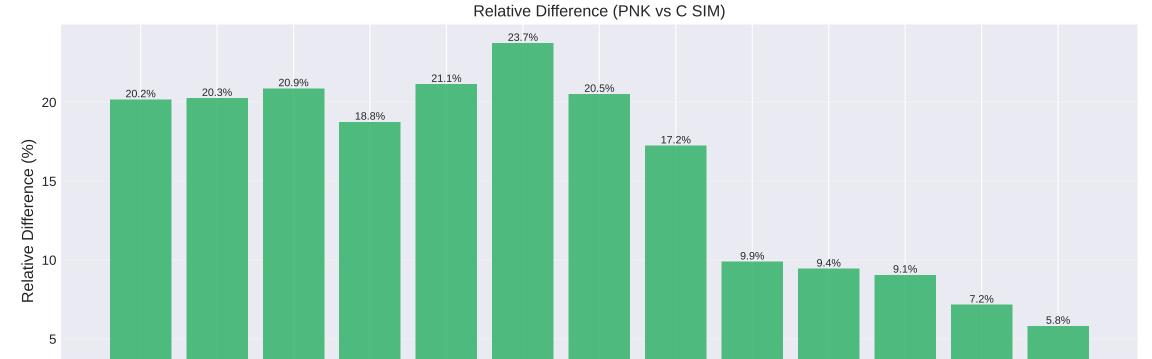
Instructions per Packet vs Throughput





Branch Mispredictions per Packet vs Throughput

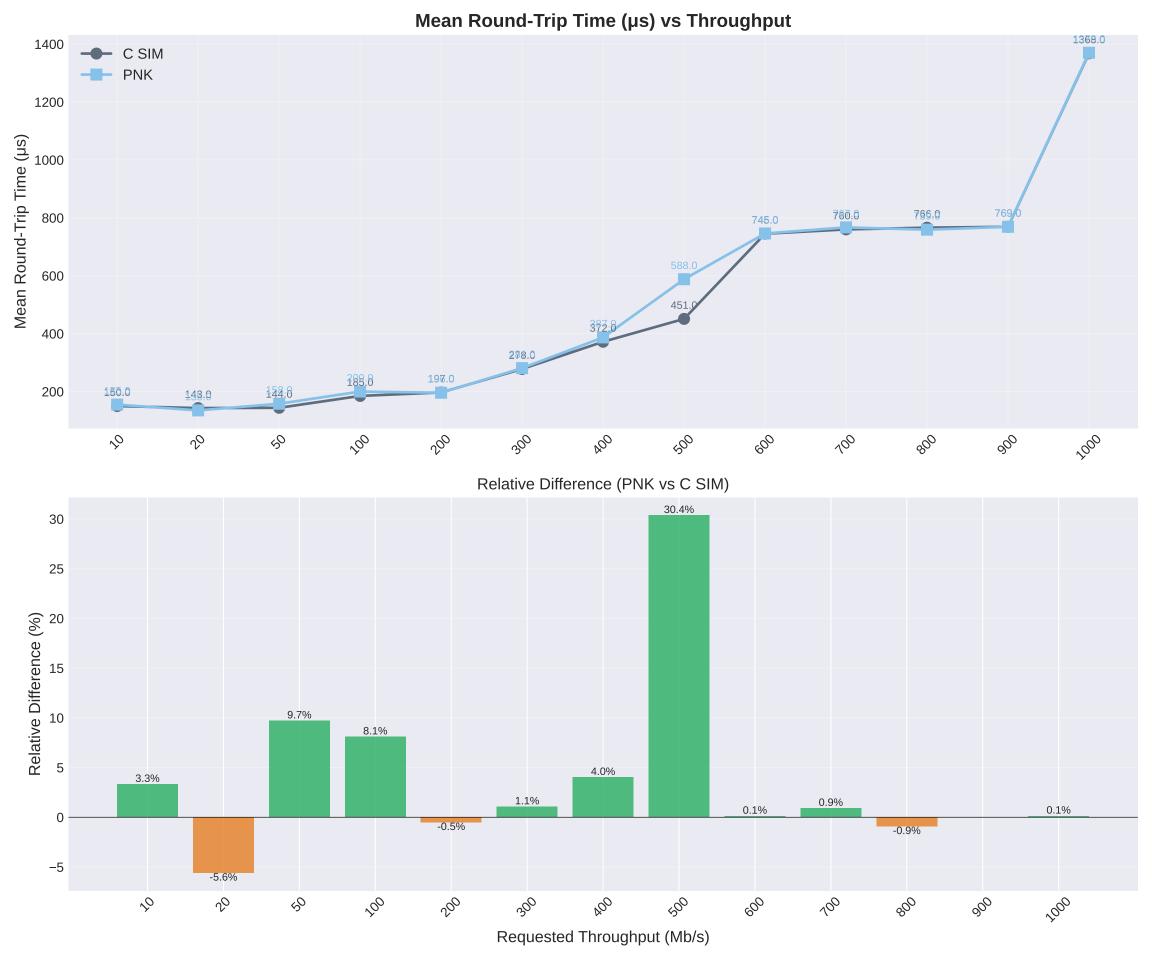




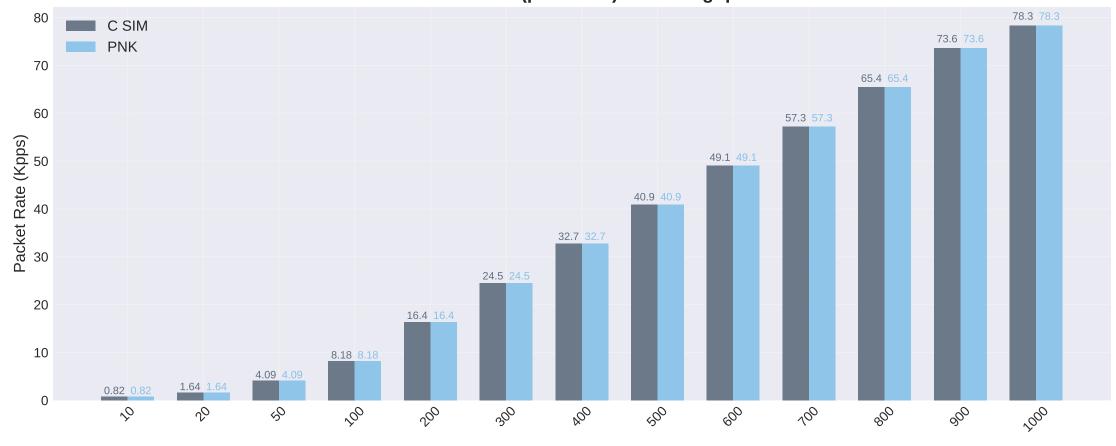
NOO

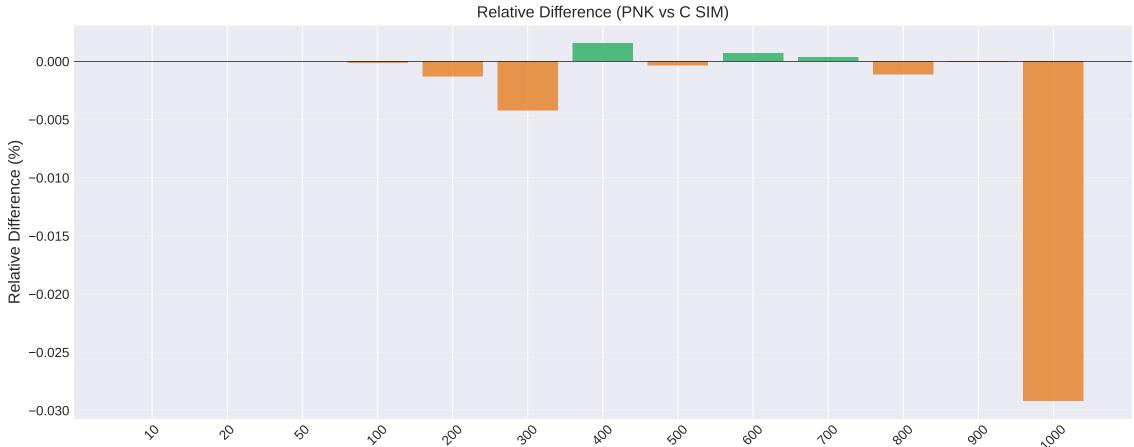
Requested Throughput (Mb/s)

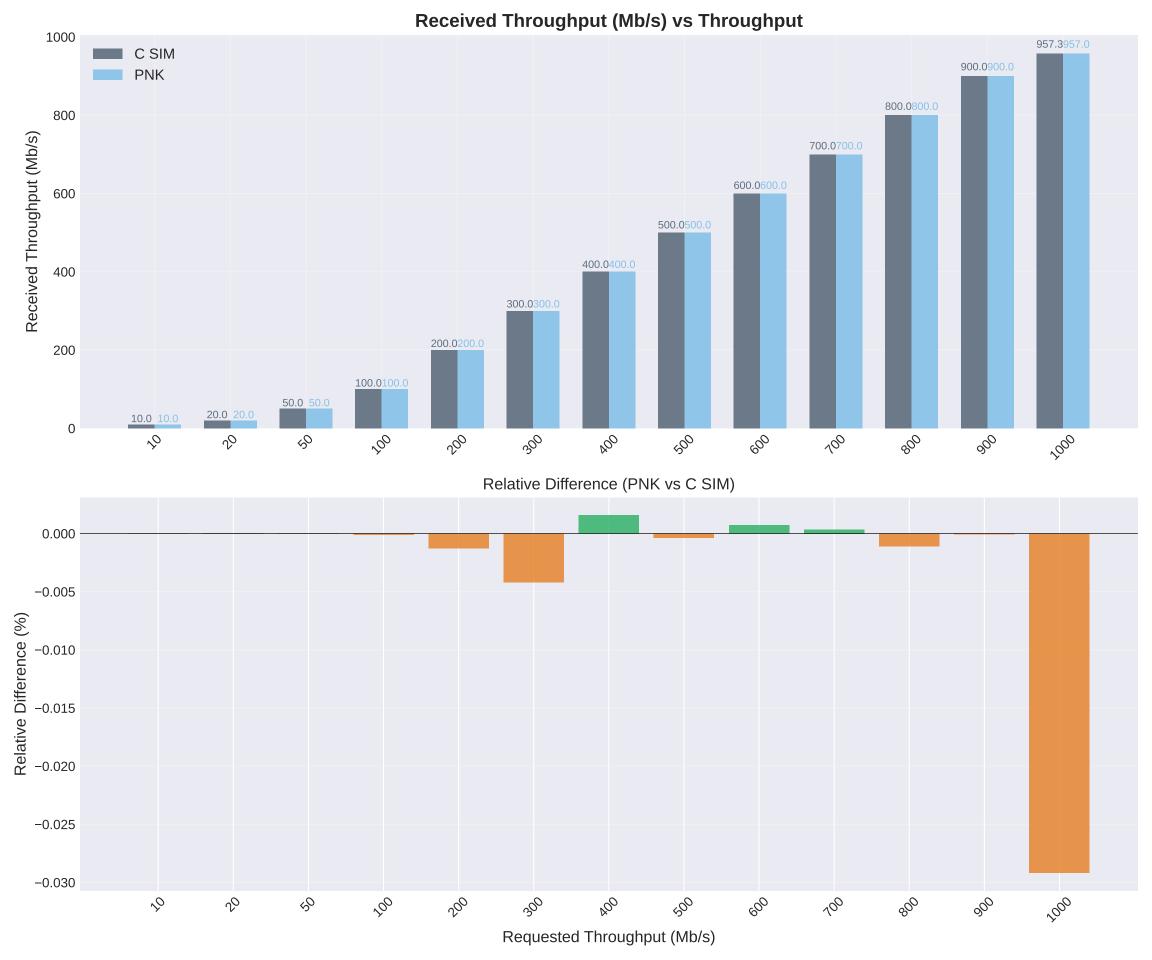
\$











Sent Throughput (Mb/s) vs Throughput 1000.0000.0 C SIM 1000 PNK 900.0900.0 800.0800.0 800 Sent Throughput (Mb/s) 700.0700.0 600.0600.0 600 500.0500.0 400.0400.0 400 300.0300.0 200.0200.0 200 100.0100.0 50.0 50.0 20.0 20.0 10.0 10.0 0 900 2000 \$ 200 200 300 NOO 400 600 700 900 20 50 Relative Difference (PNK vs C SIM) 0.0008 0.0006 Relative Difference (%)
0000.0
0000.0
0000.0
0000.0 -0.0004 -0.0006 30 20 200 200 300 NOO 400 600 100 900 50

Requested Throughput (Mb/s)