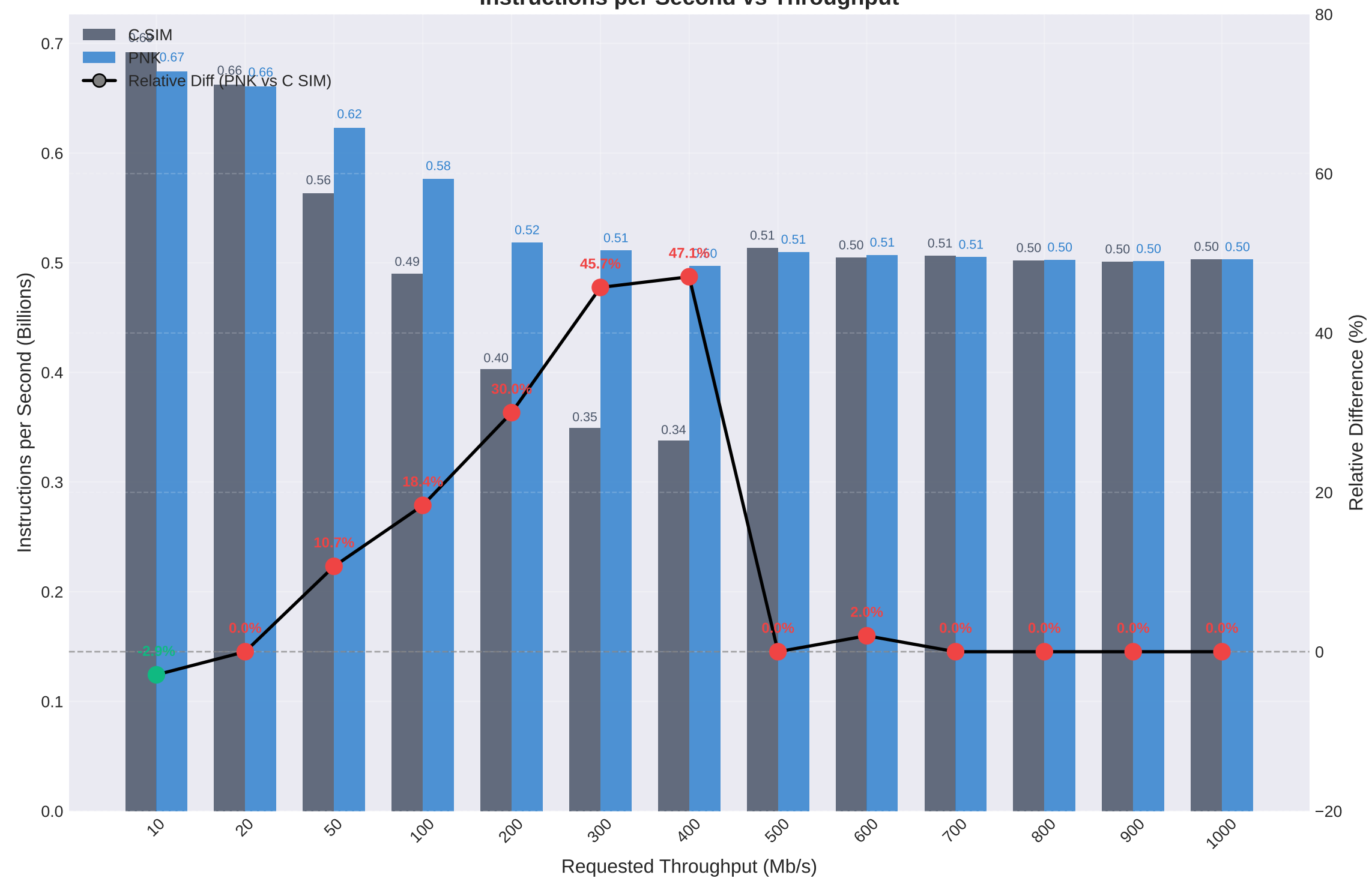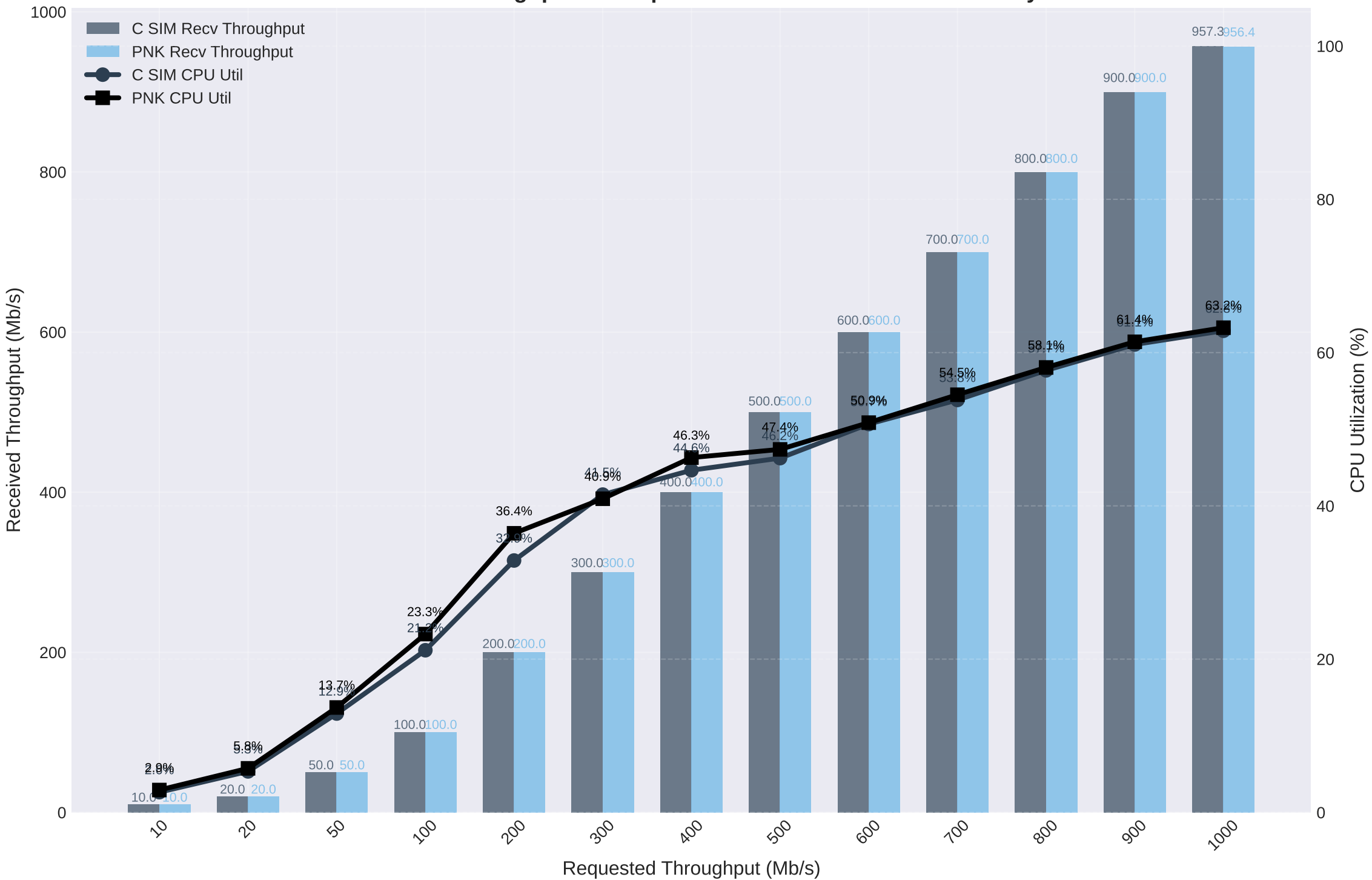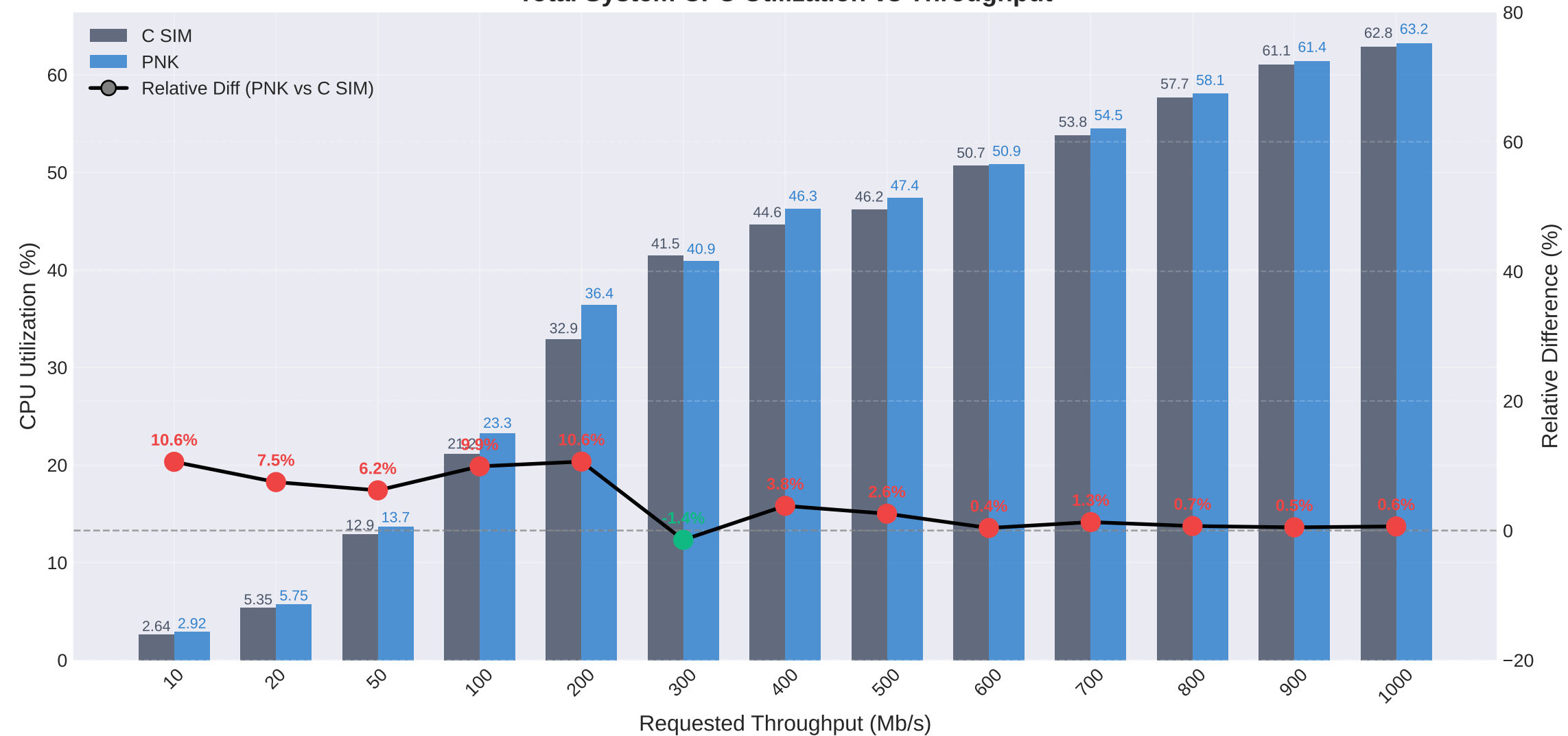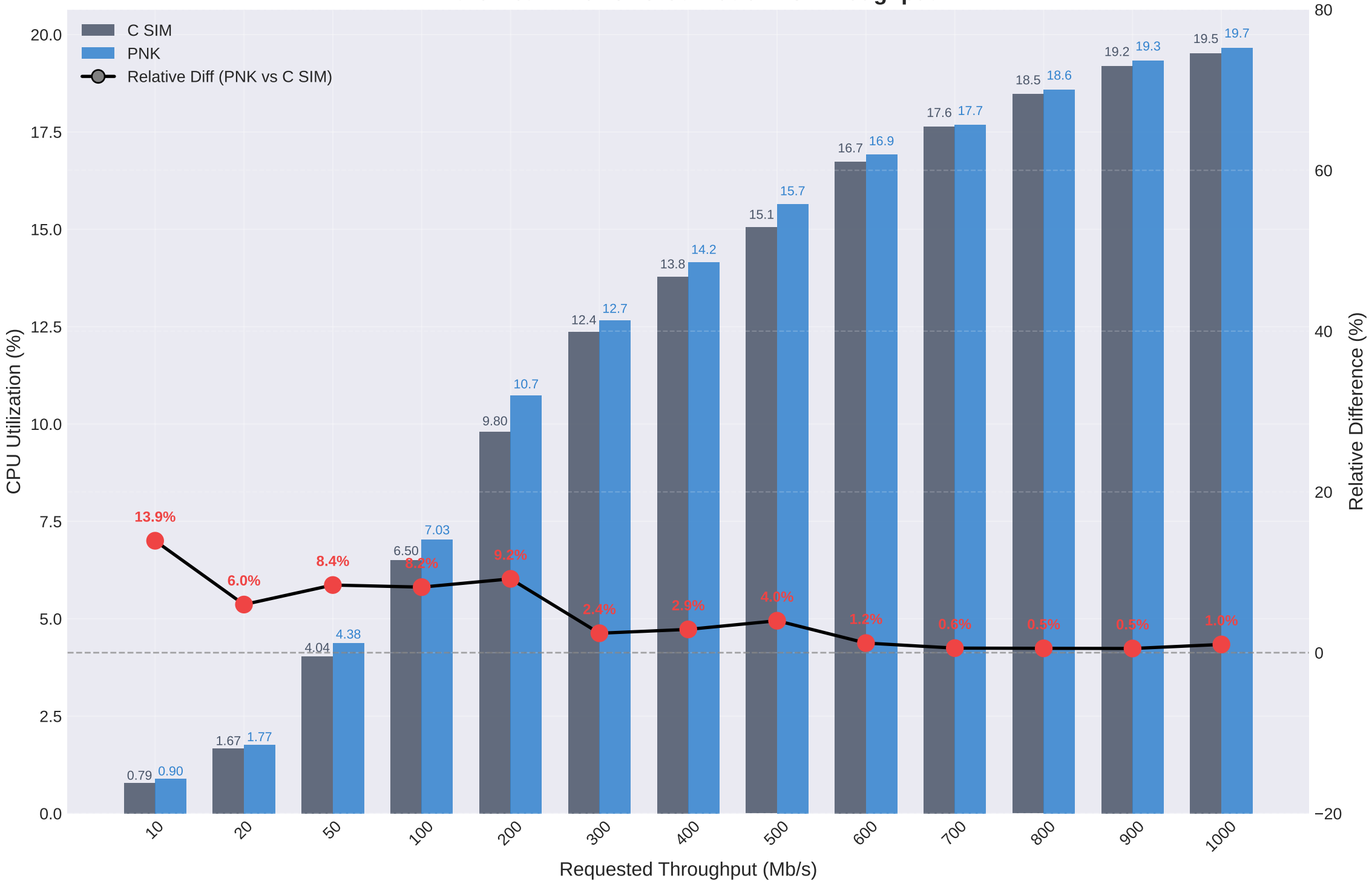Instructions per Second vs Throughput

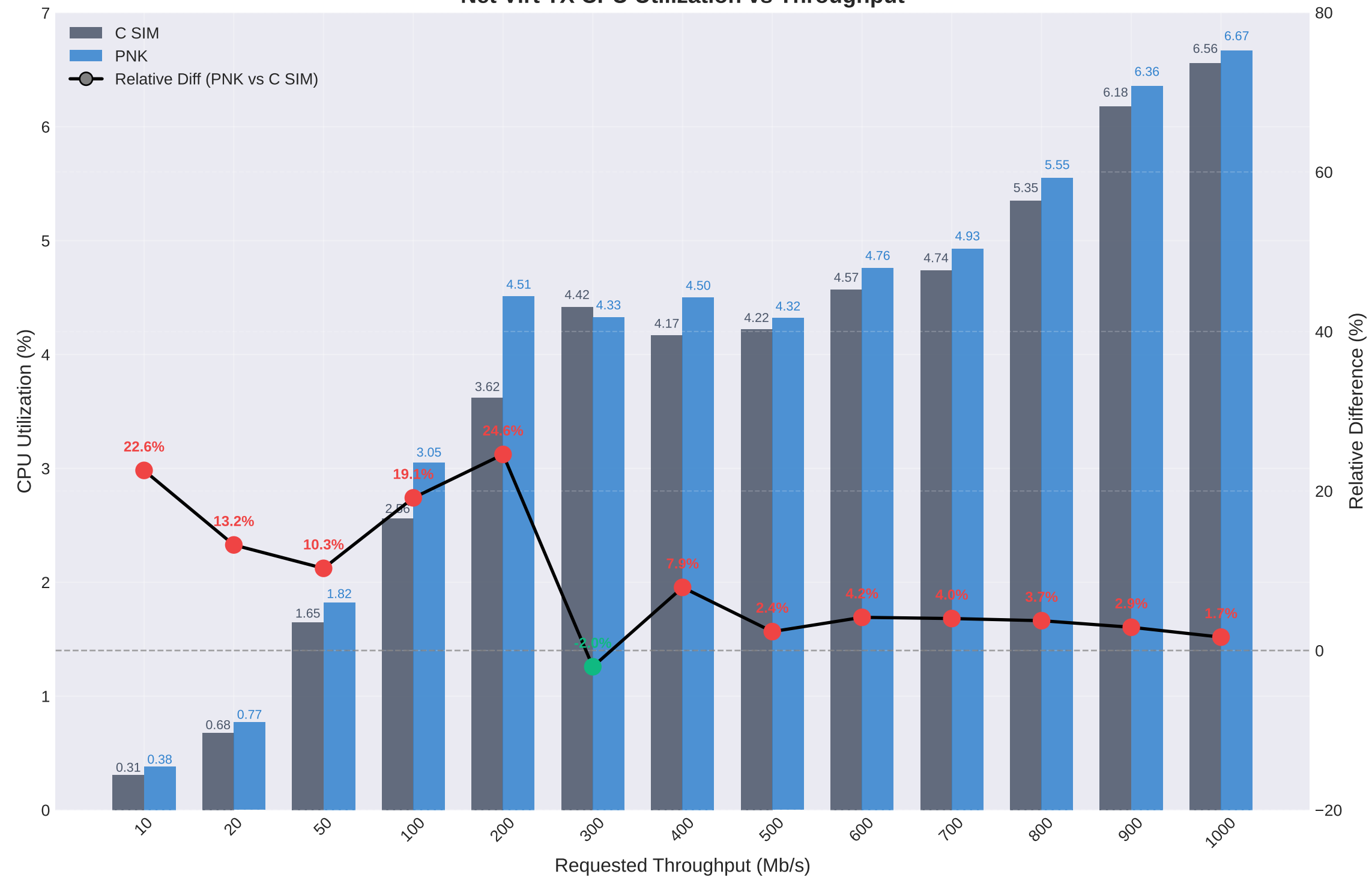Received Throughput vs Requested with CPU Utilization Overlay
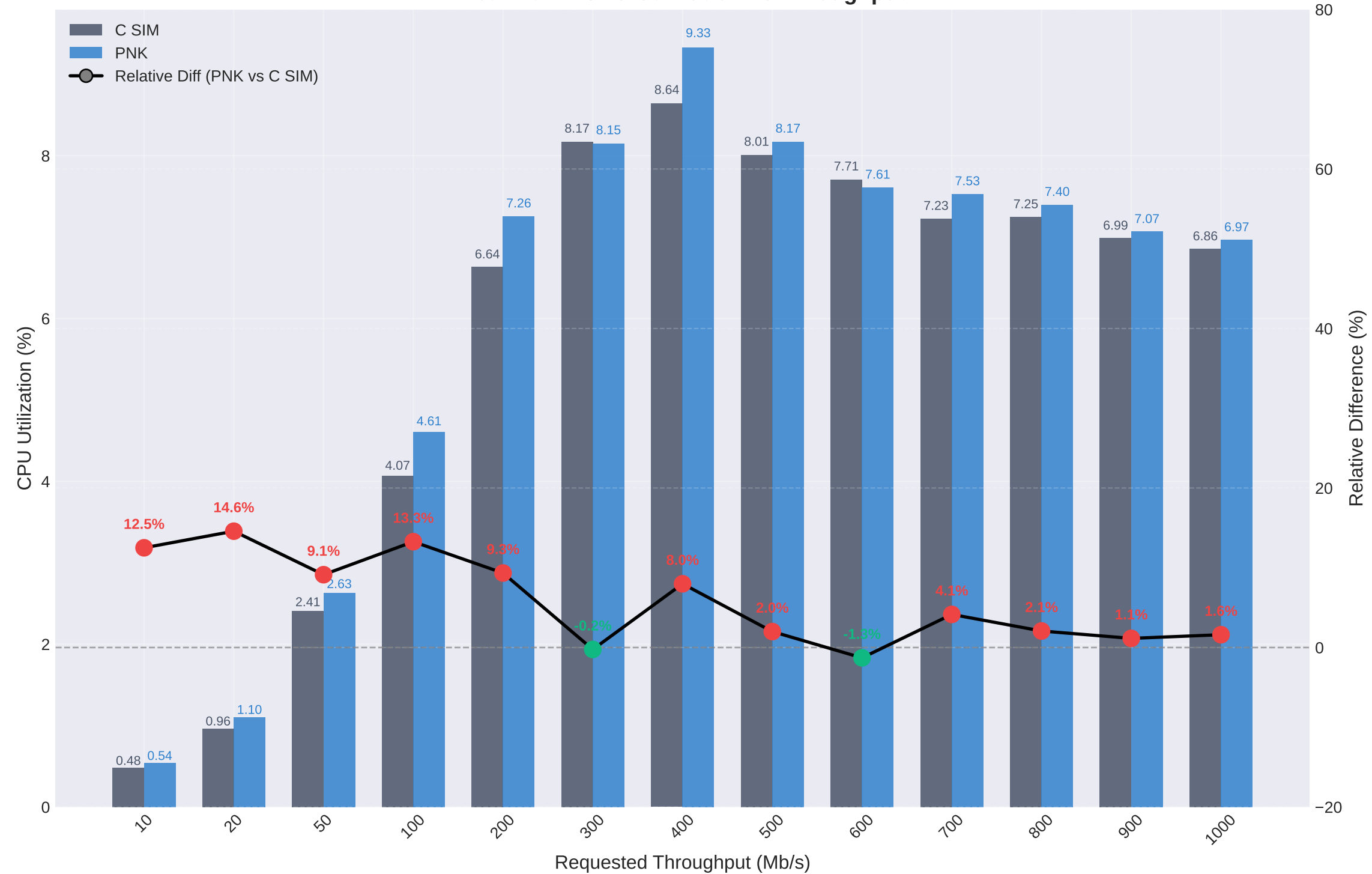
Total System CPU Utilization vs Throughput

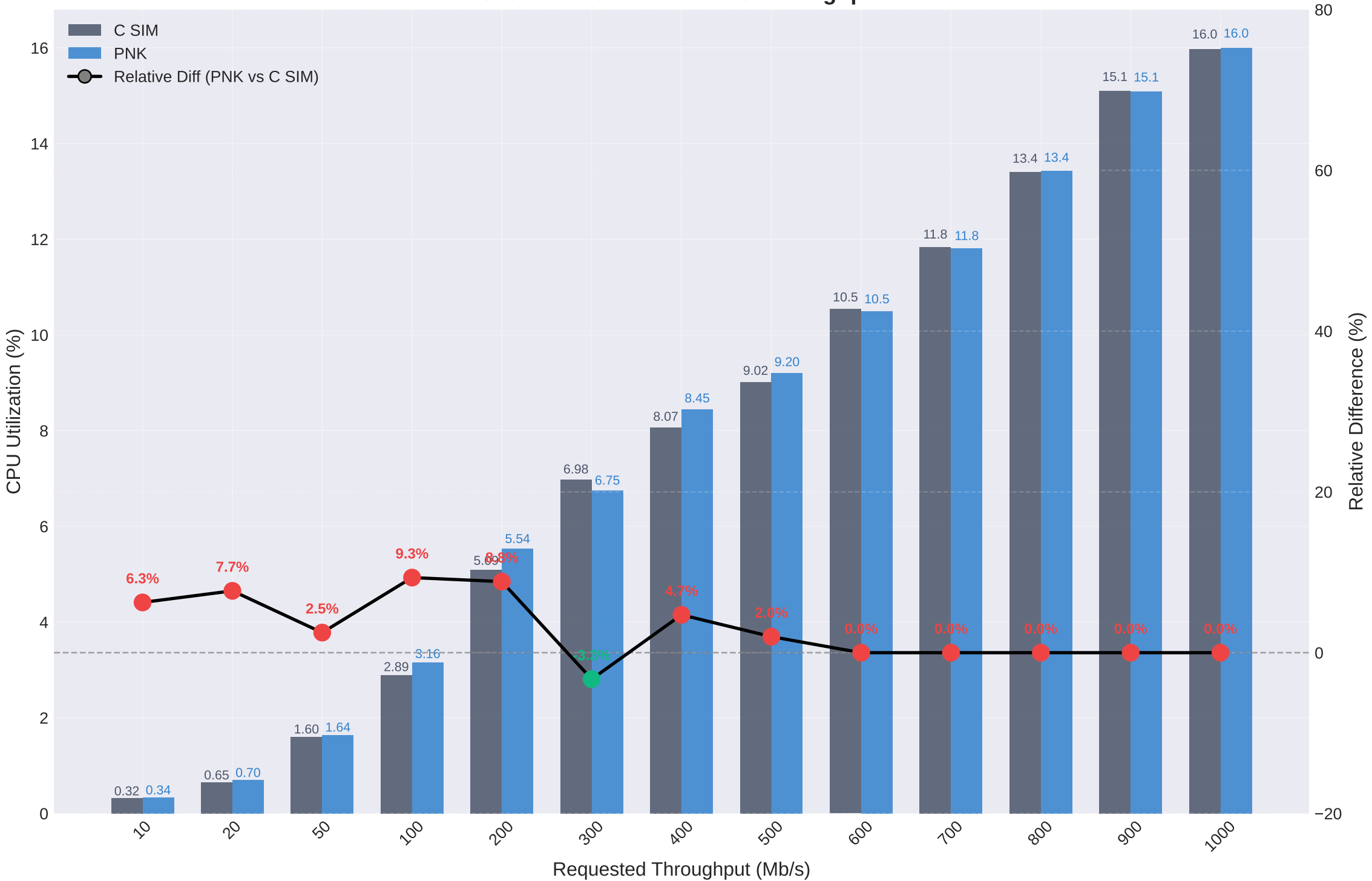Ethernet Driver CPU Utilization vs Throughput
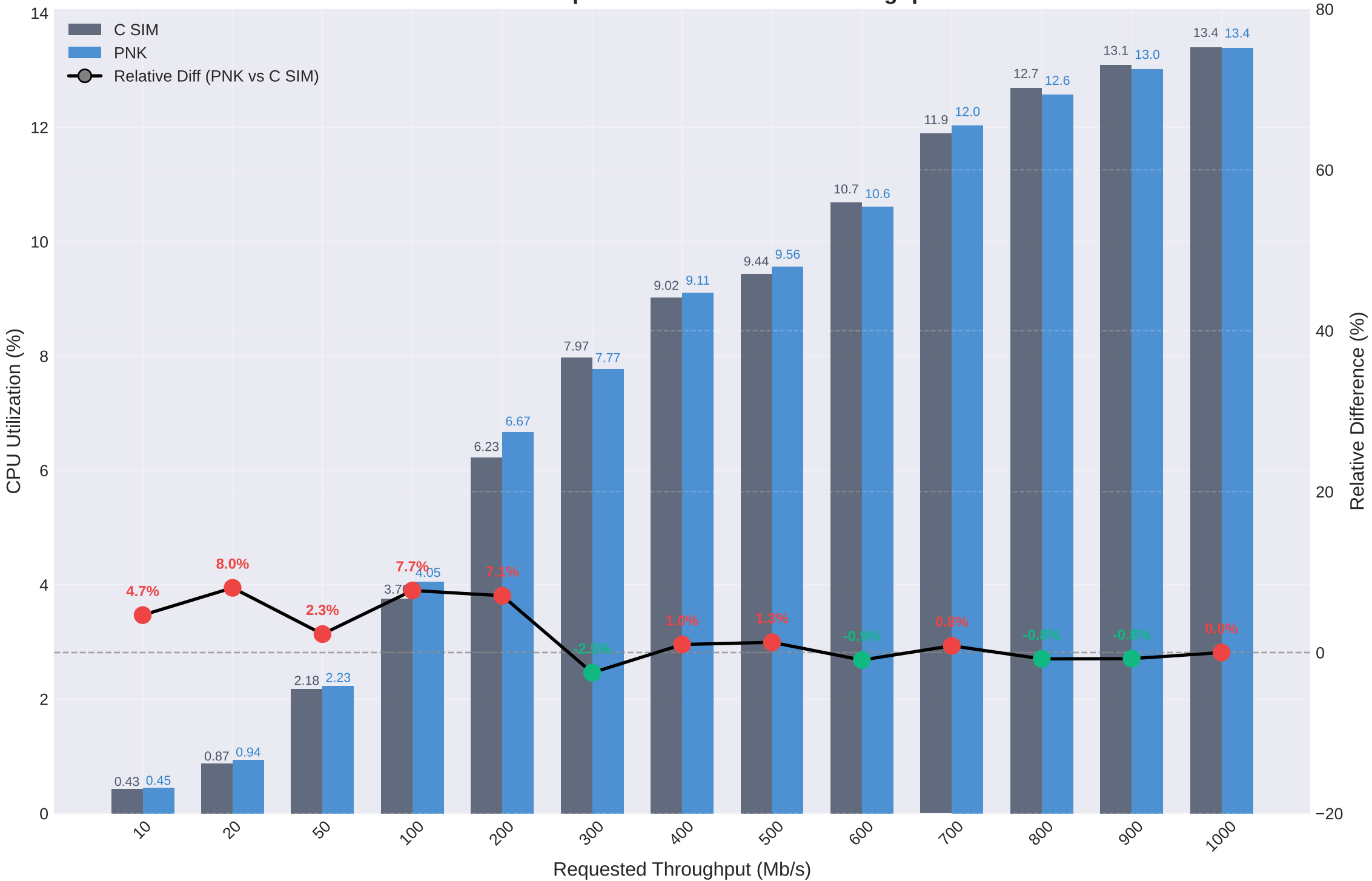
Net Virt TX CPU Utilization vs Throughput

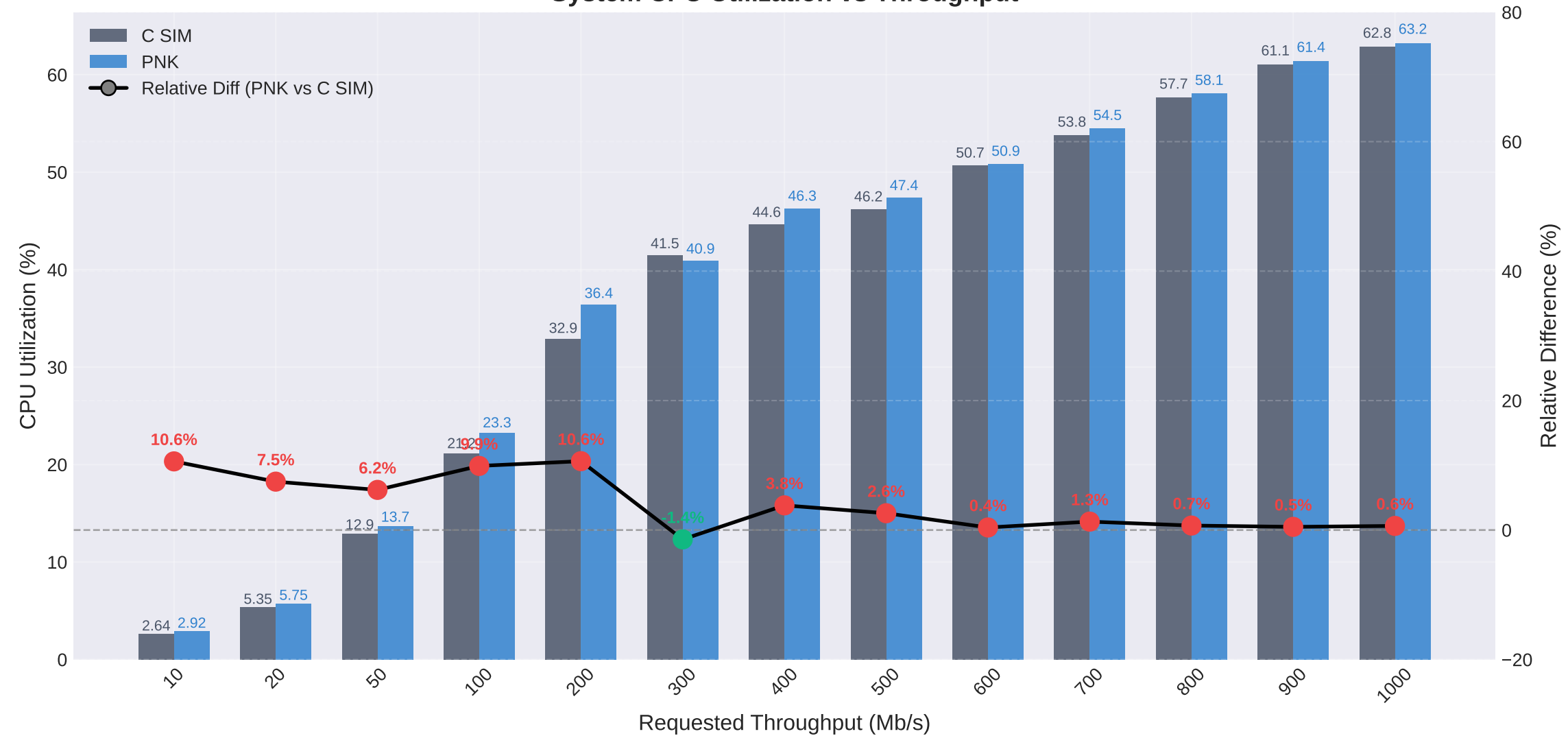Net Virt RX CPU Utilization vs Throughput

Client0 CPU Utilization vs Throughput

Client0 Net Copier CPU Utilization vs Throughput
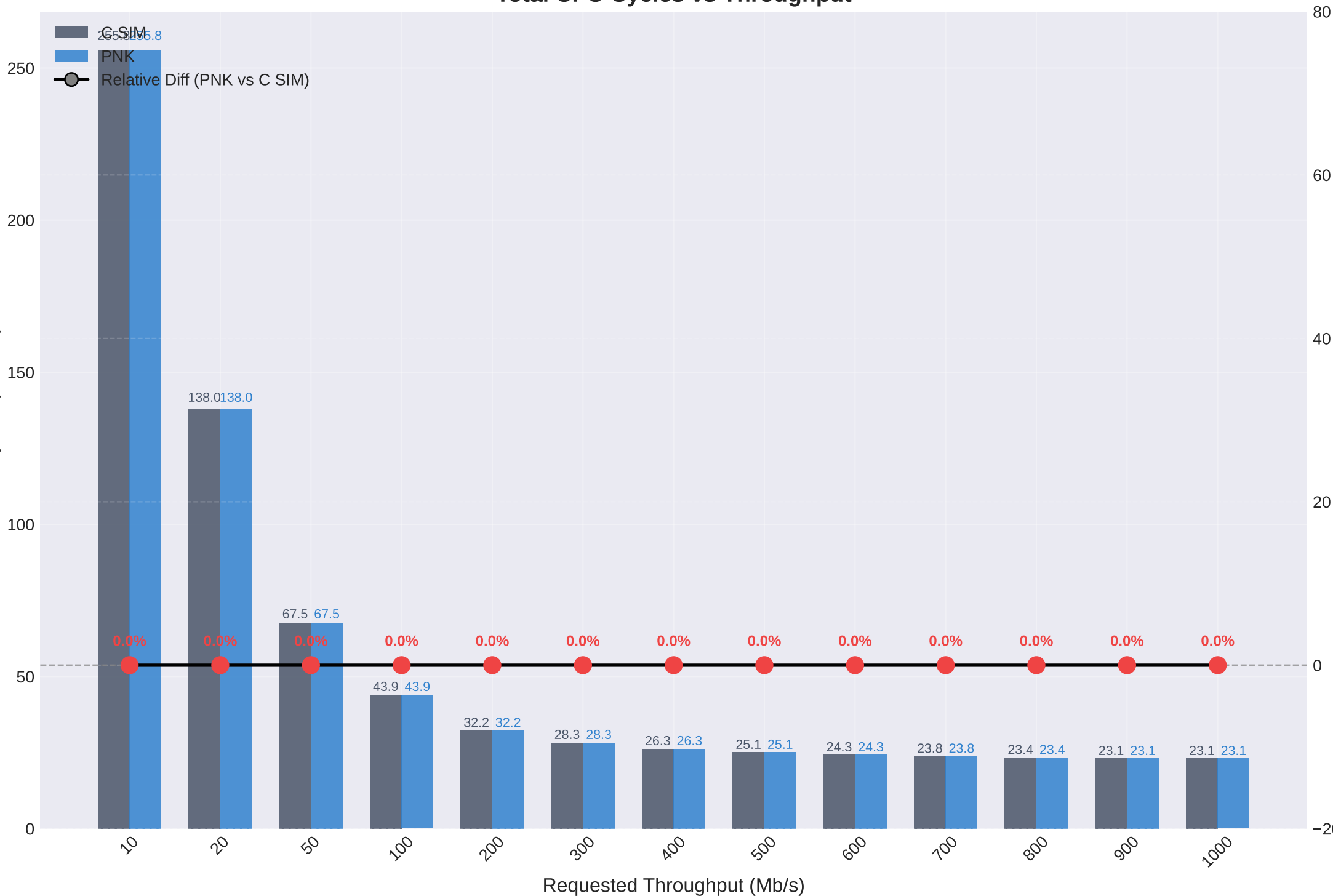
System CPU Utilization vs Throughput
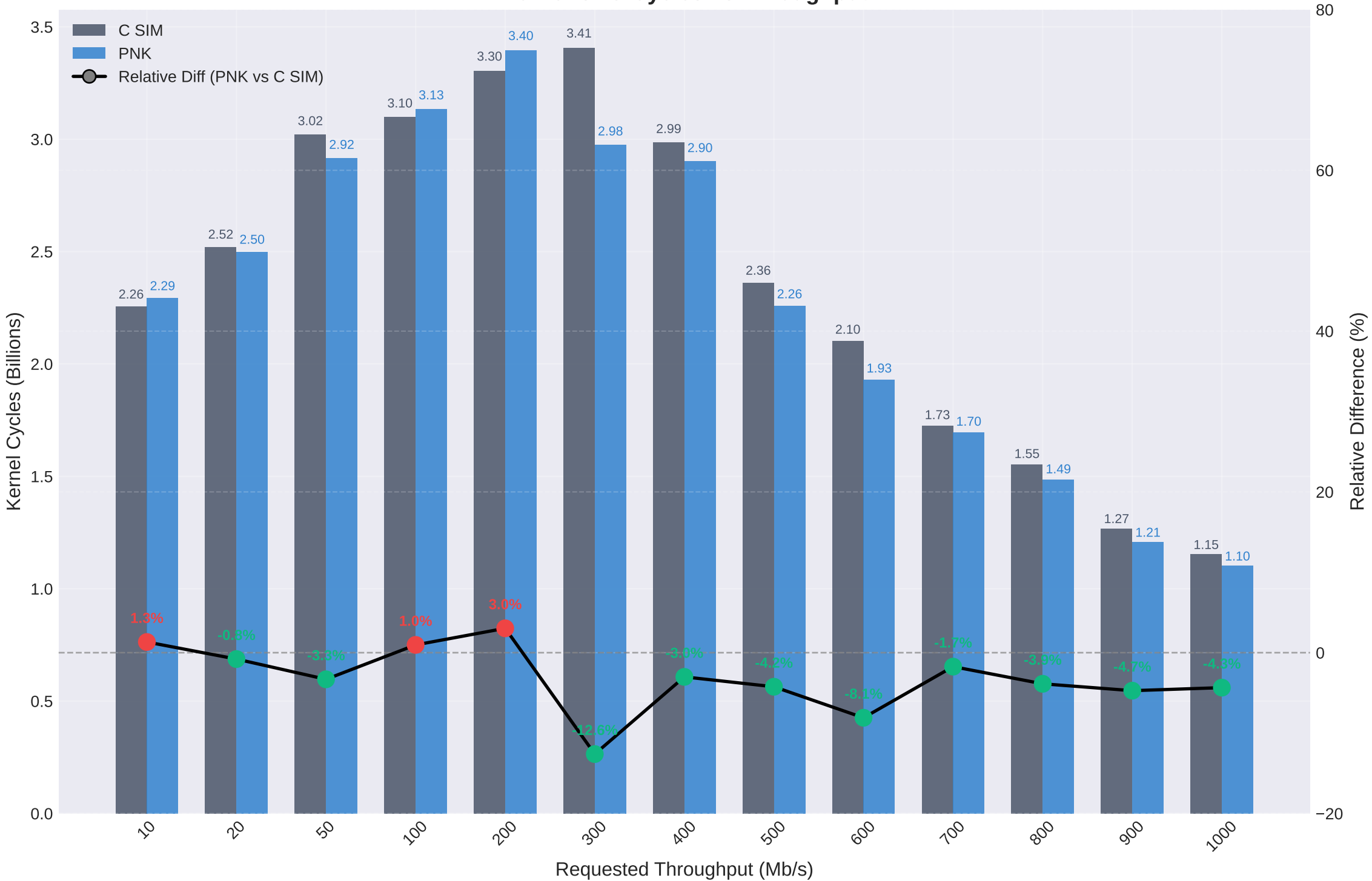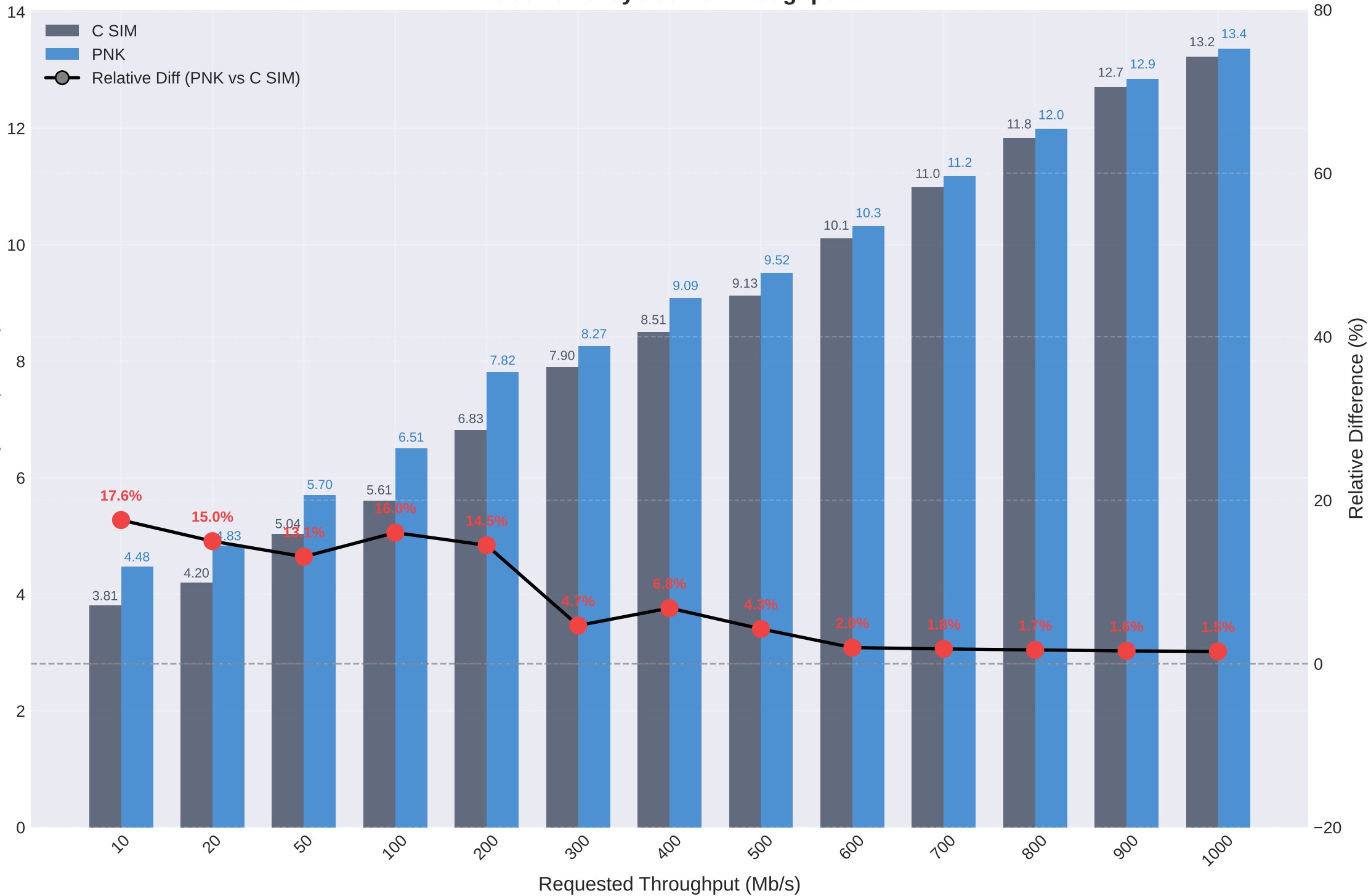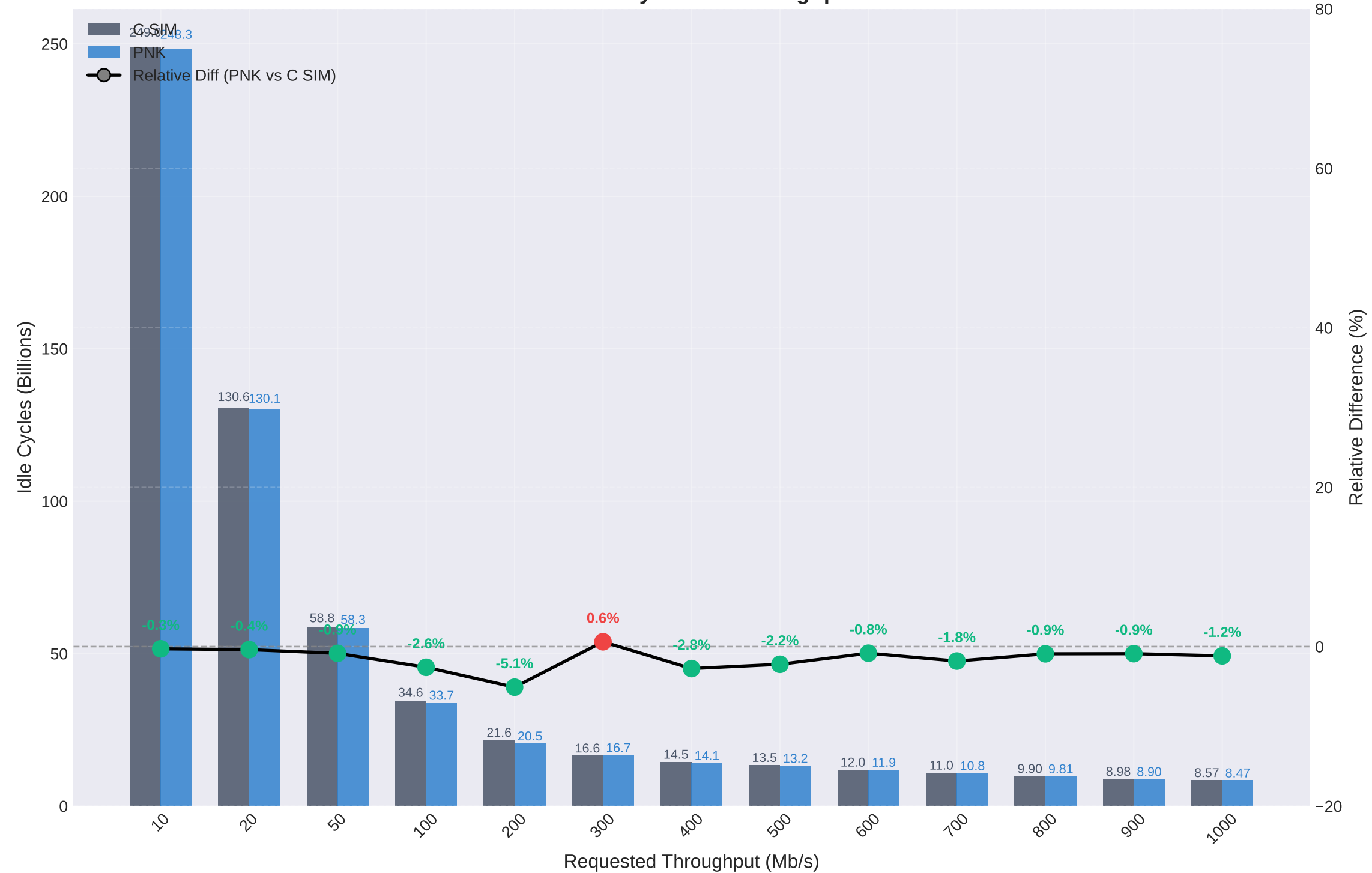
Total CPU Cycles vs Throughput

Kernel CPU Cycles vs Throughput

User CPU Cycles vs Throughput

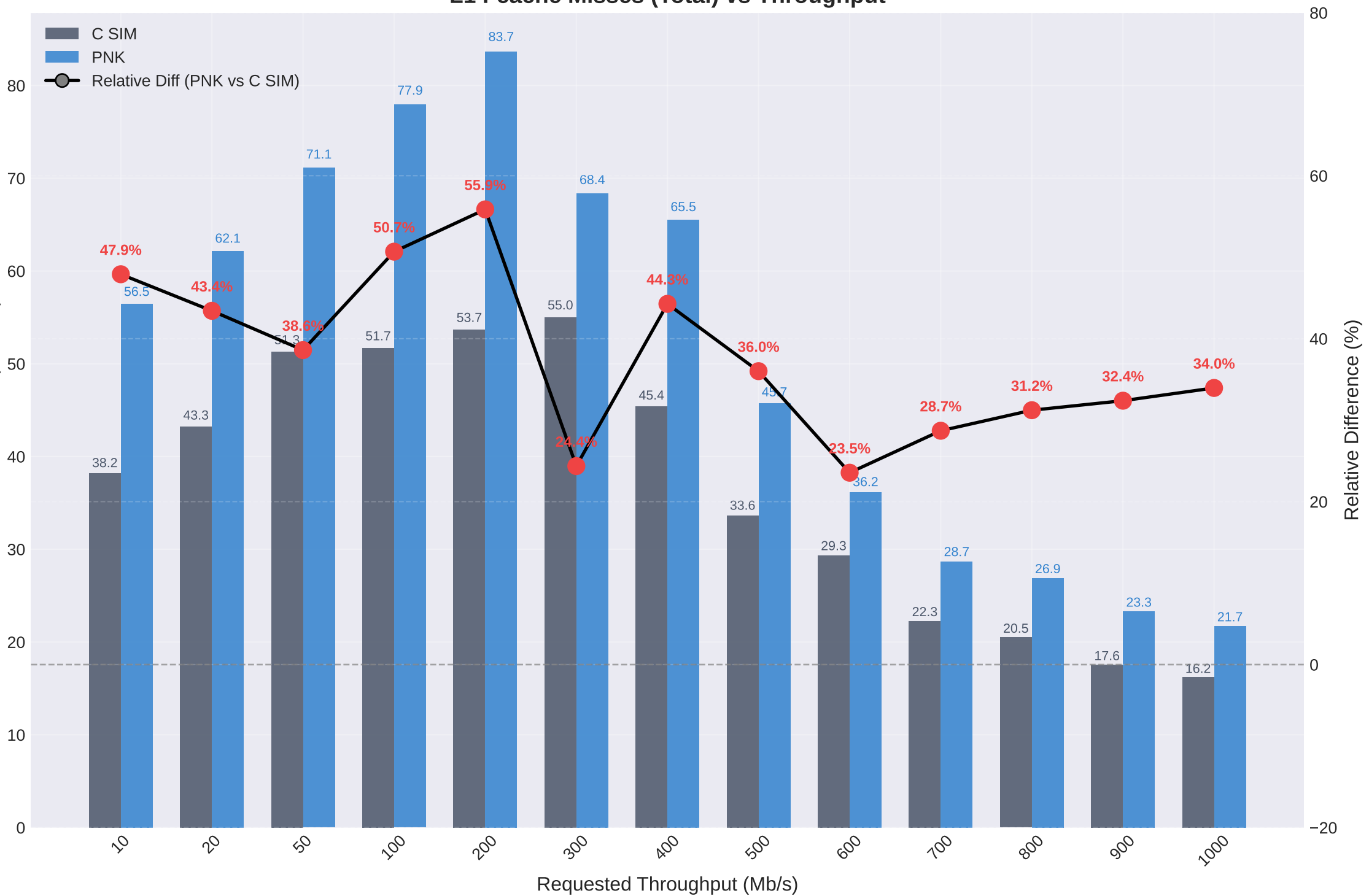Idle CPU Cycles vs Throughput

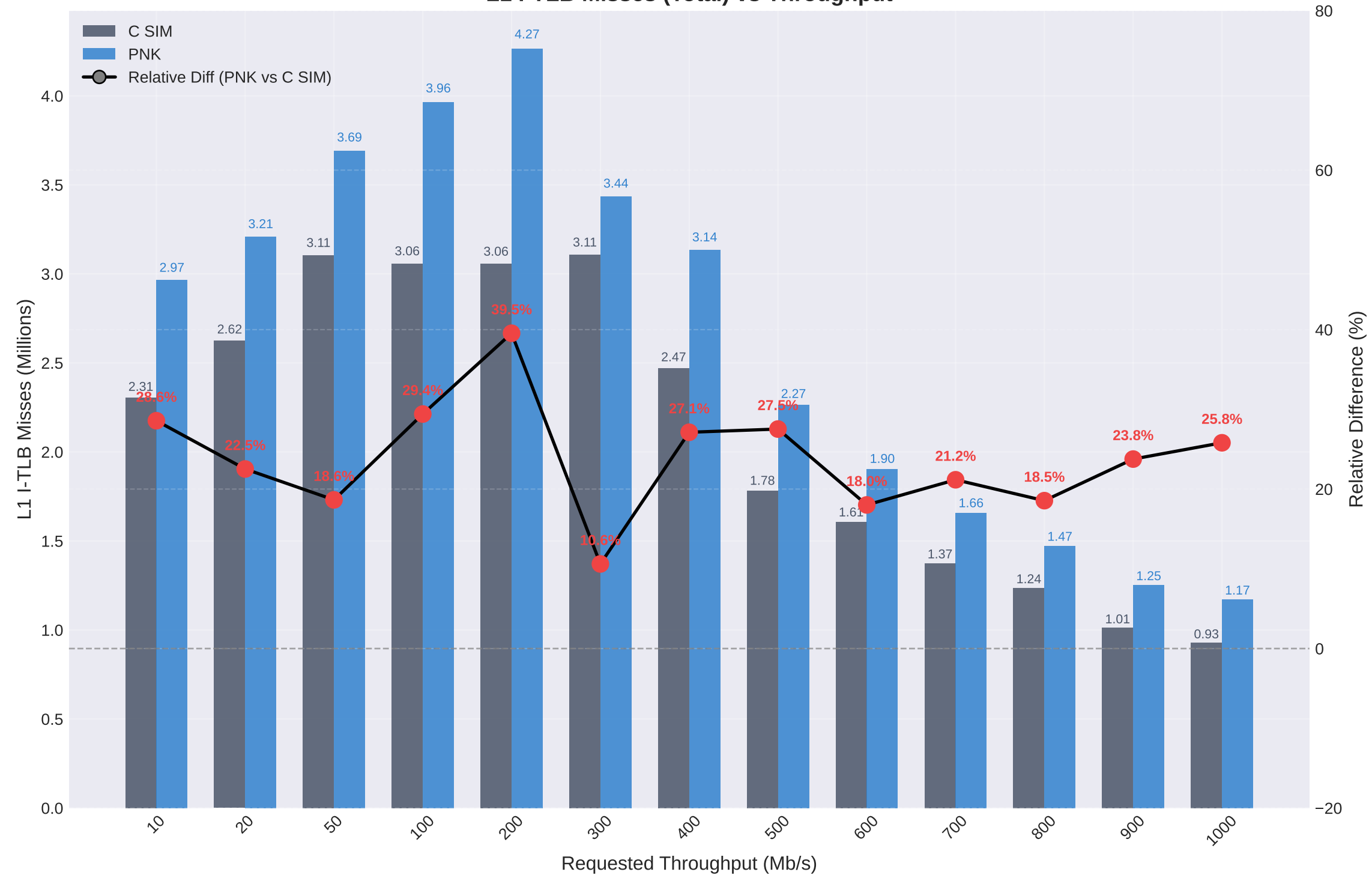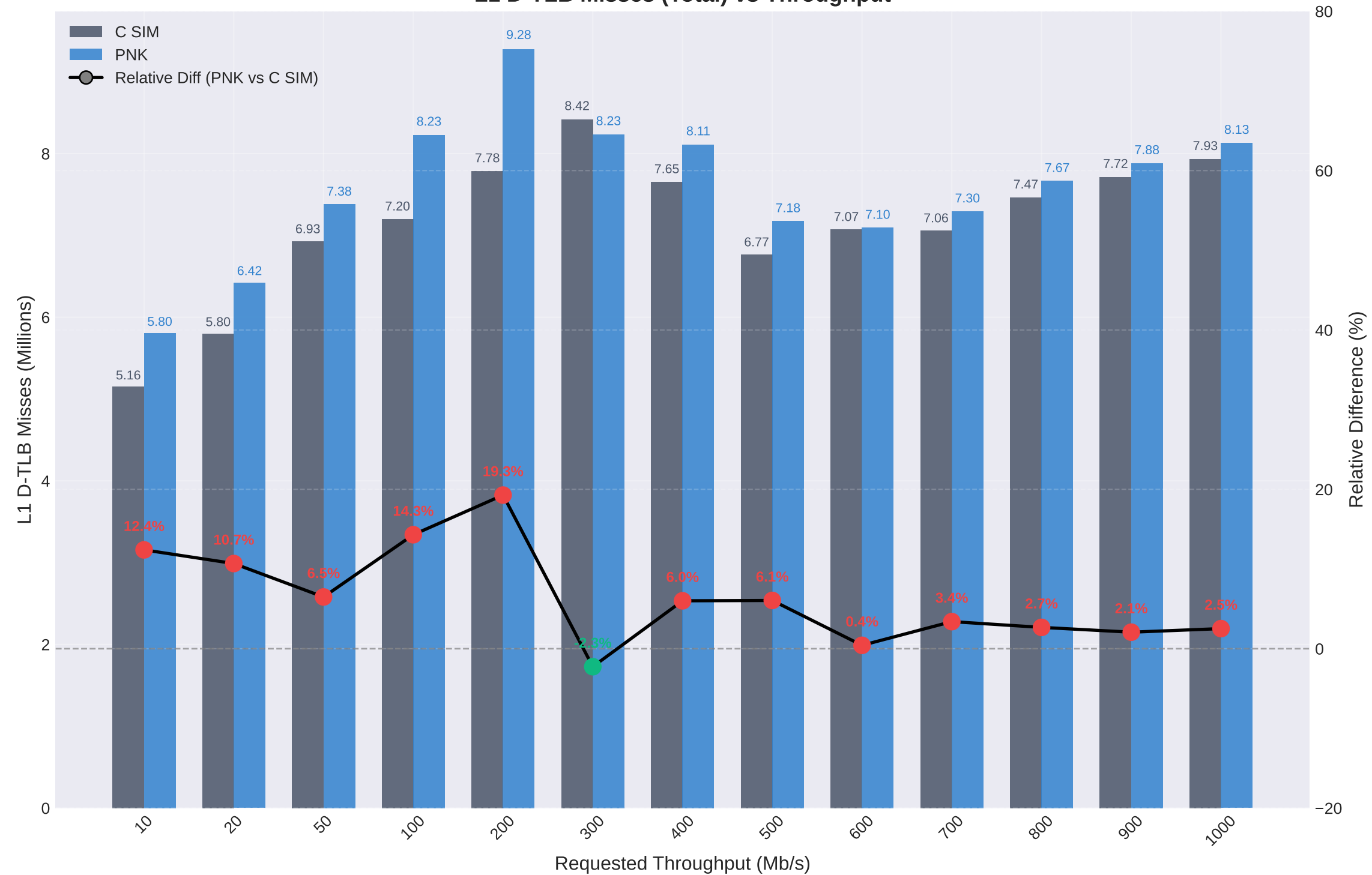**L1 I-cache Misses (Total) vs Throughput**

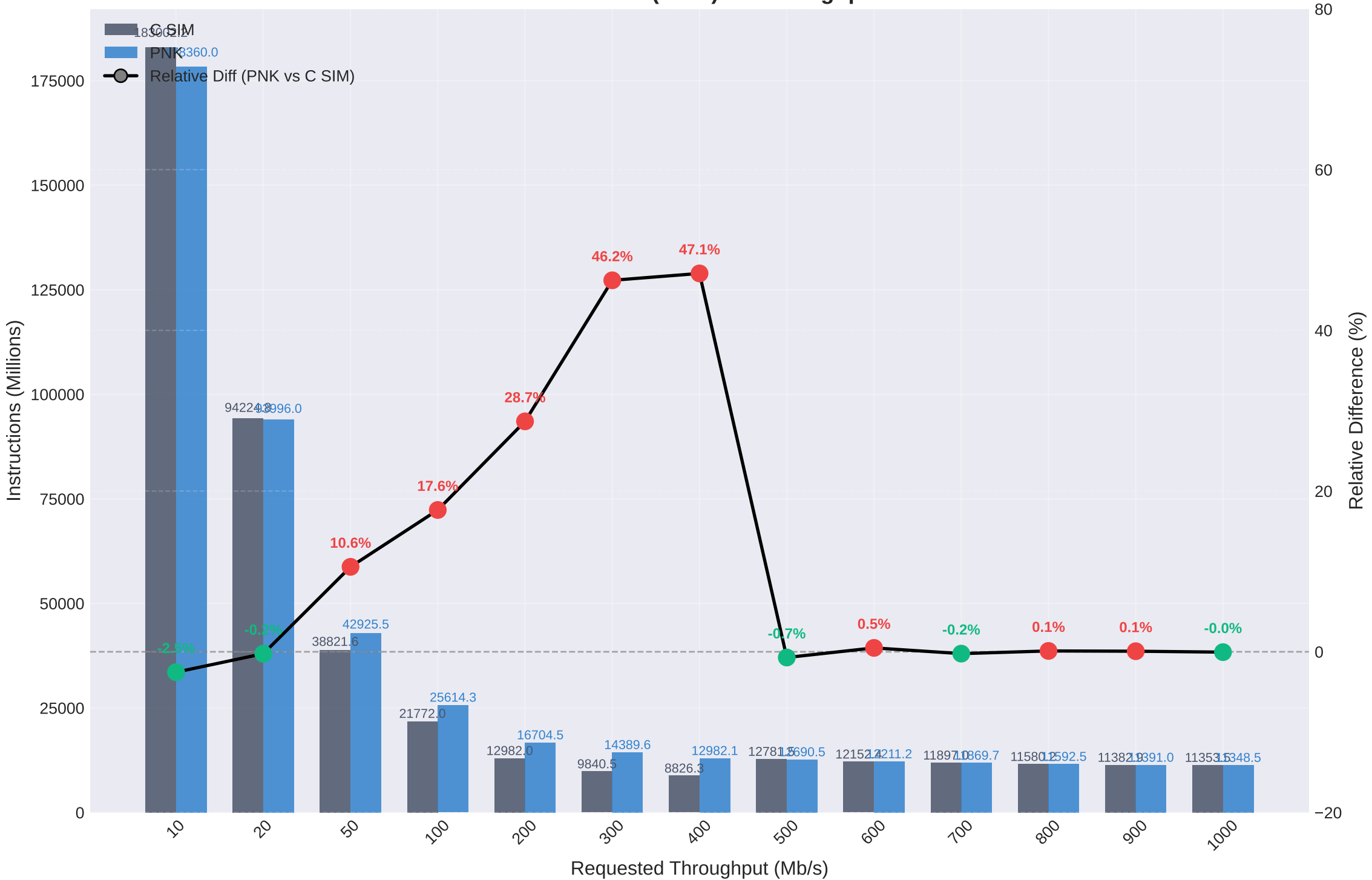**L1 D-cache Misses (Total) vs Throughput**
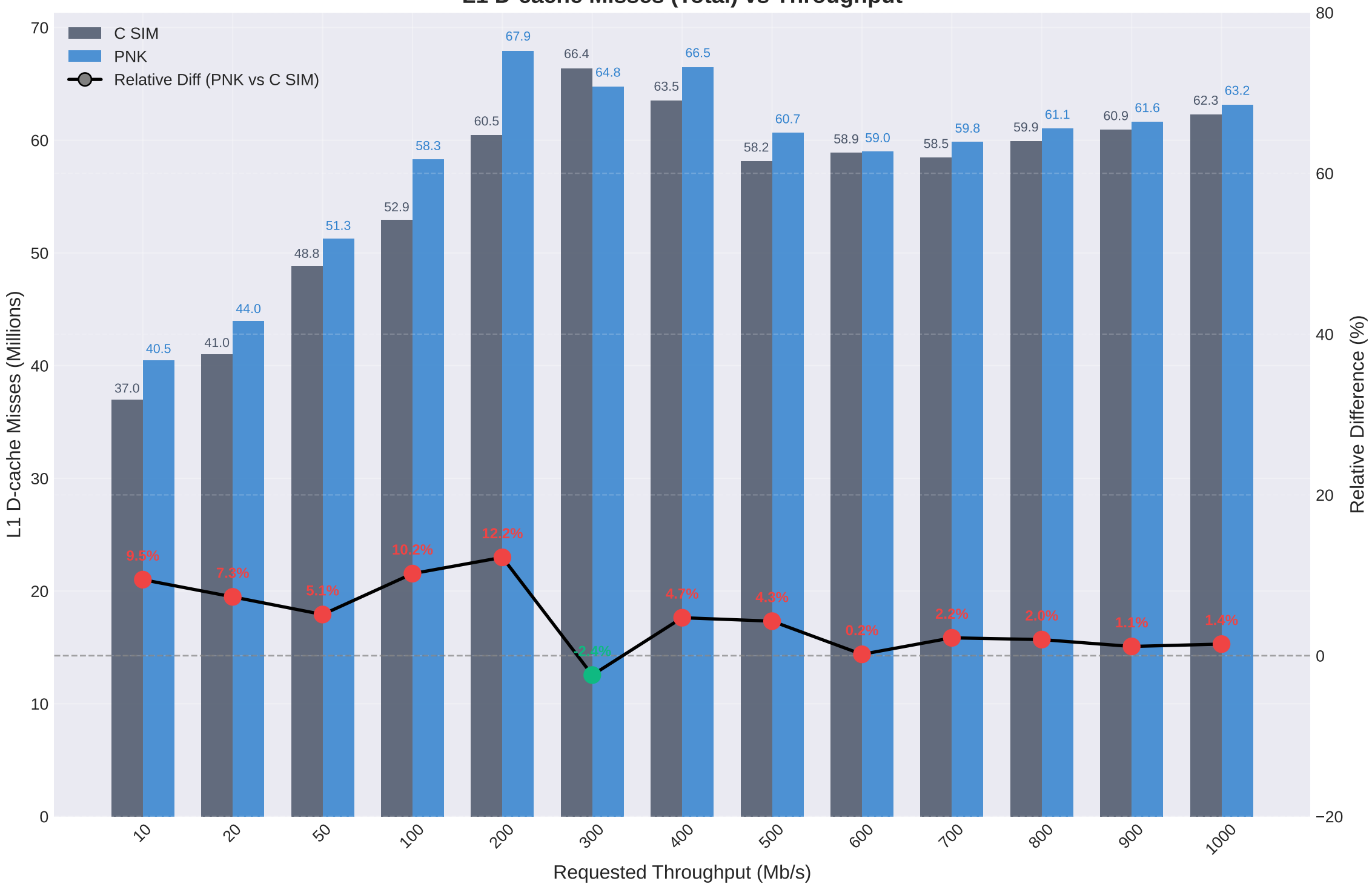
L1 I-TLB Misses (Total) vs Throughput

L1 D-TLB Misses (Total) vs Throughput
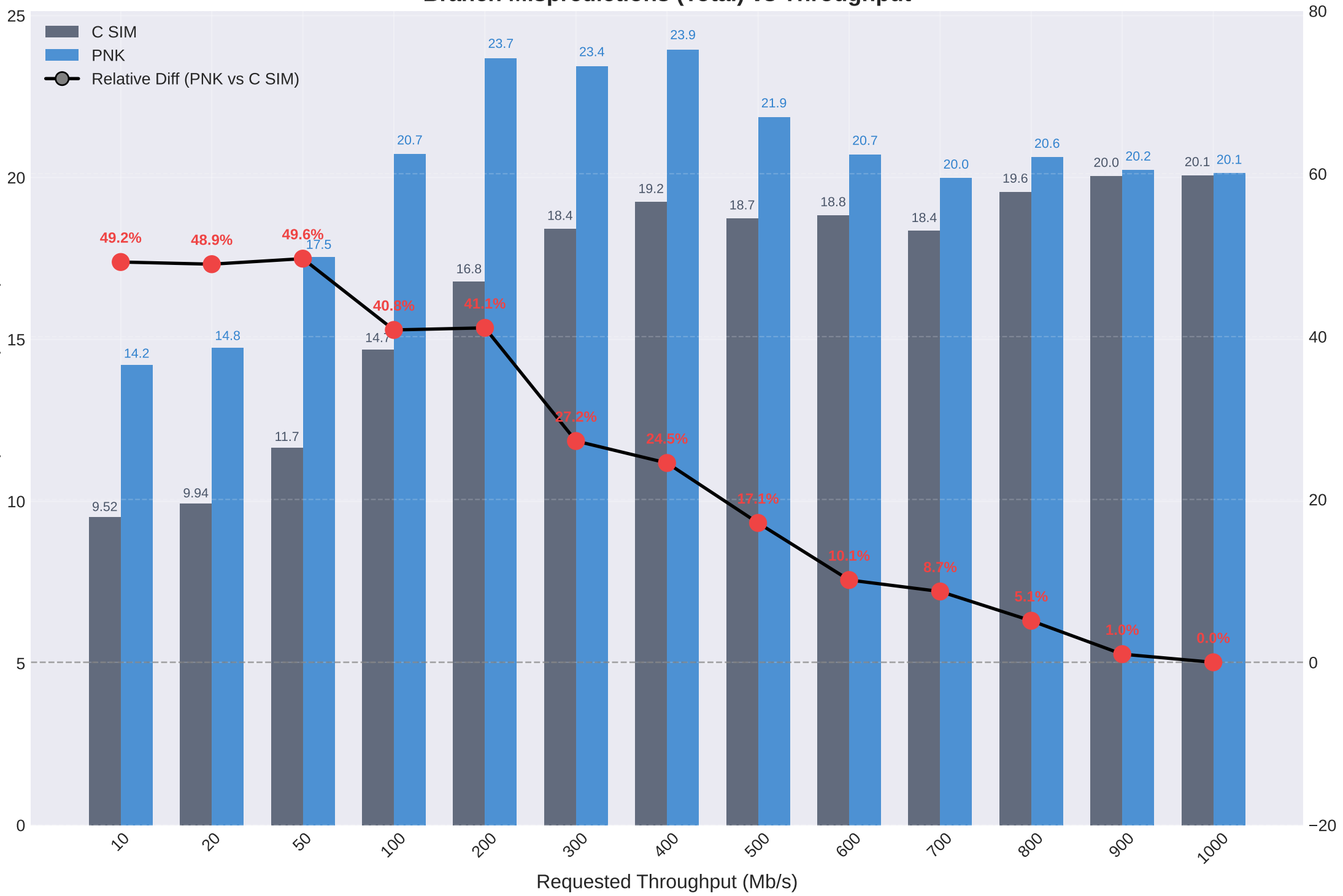
Instructions (Total) vs Throughput

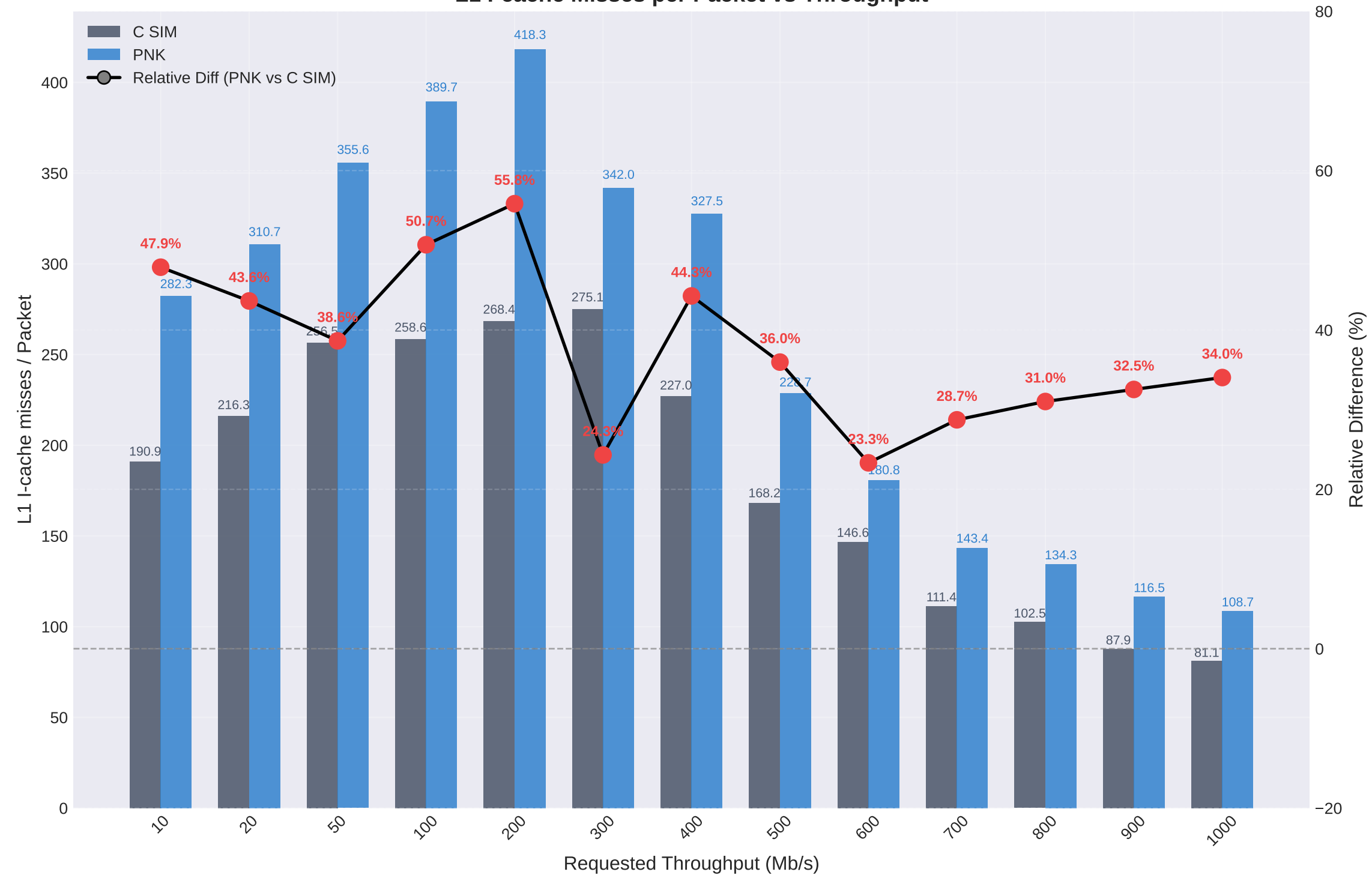Branch Mispredictions (Total) vs Throughput

L1 I-cache Misses per Packet vs Throughput

Legend:
- C SIM
- PNK
- Relative Diff (PNK vs C SIM)

X-axis: Requested Throughput (Mb/s)
Left Y-axis: L1 I-cache misses / Packet
Right Y-axis: Relative Difference (%)

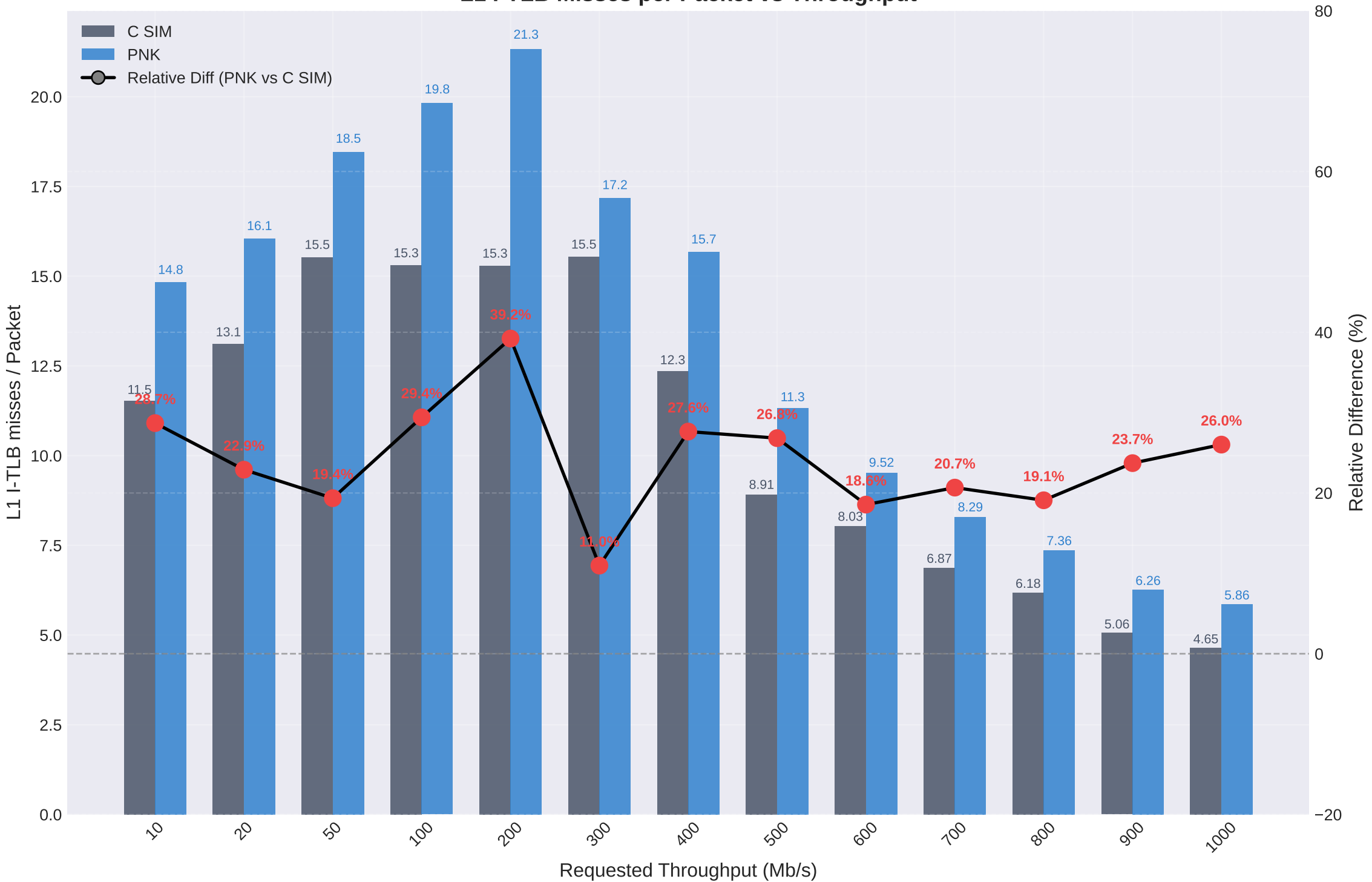| Throughput (Mb/s)	C SIM	PNK	Relative Diff
10	190.9	282.3	47.9%
20	216.3	310.7	43.6%
50	256.5	355.6	38.6%
100	258.6	389.7	50.7%
200	268.4	418.3	55.8%
300	275.1	342.0	24.3%
400	227.0	327.5	44.3%
500	168.2	228.7	36.0%
600	146.6	180.8	23.3%
700	111.4	143.4	28.7%
800	102.5	134.3	31.0%
900	87.9	116.5	32.5%
1000	81.1	108.7	34.0%

L1 D-cache Misses per Packet vs Throughput

L1 I-TLB Misses per Packet vs Throughput
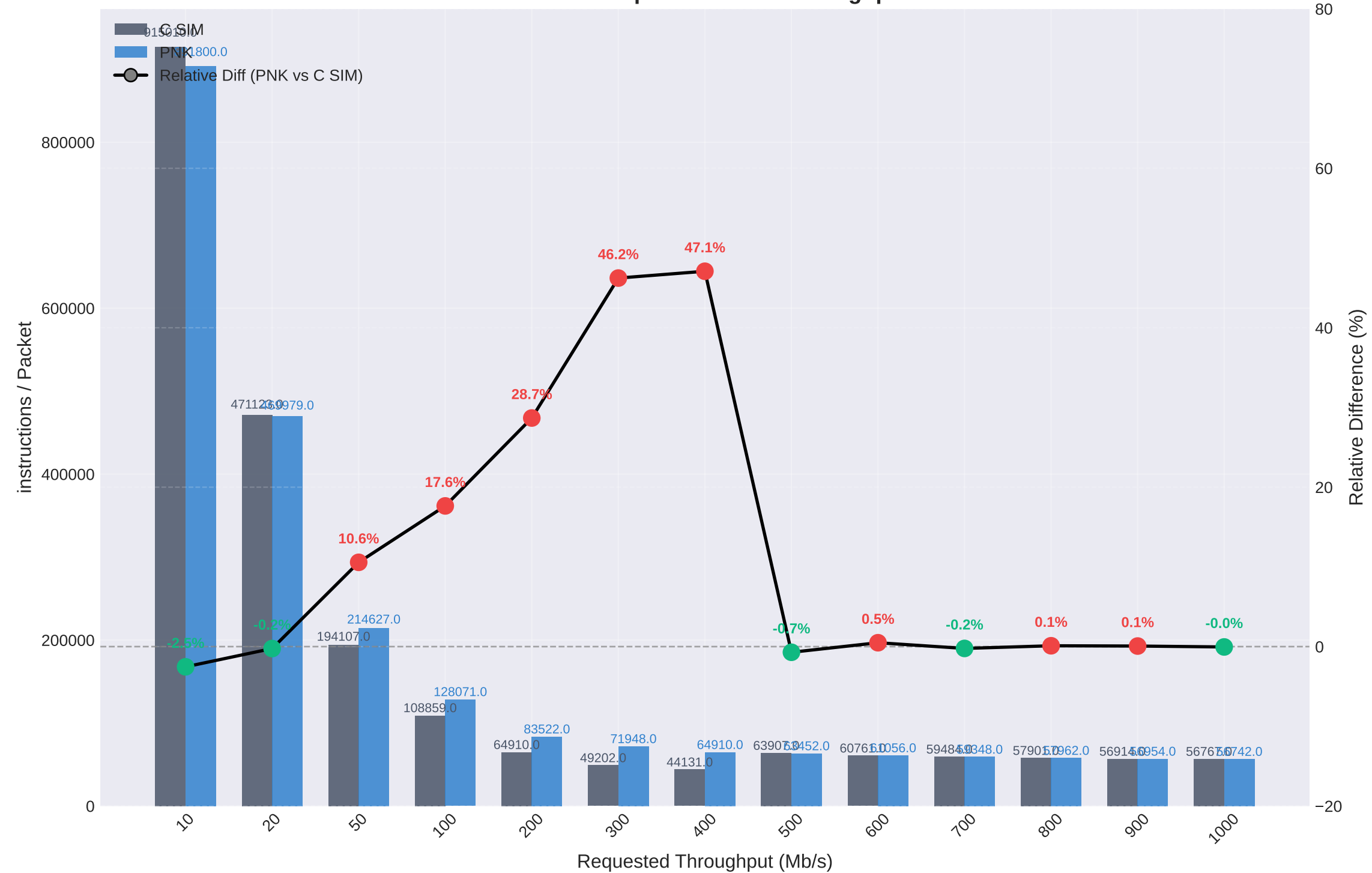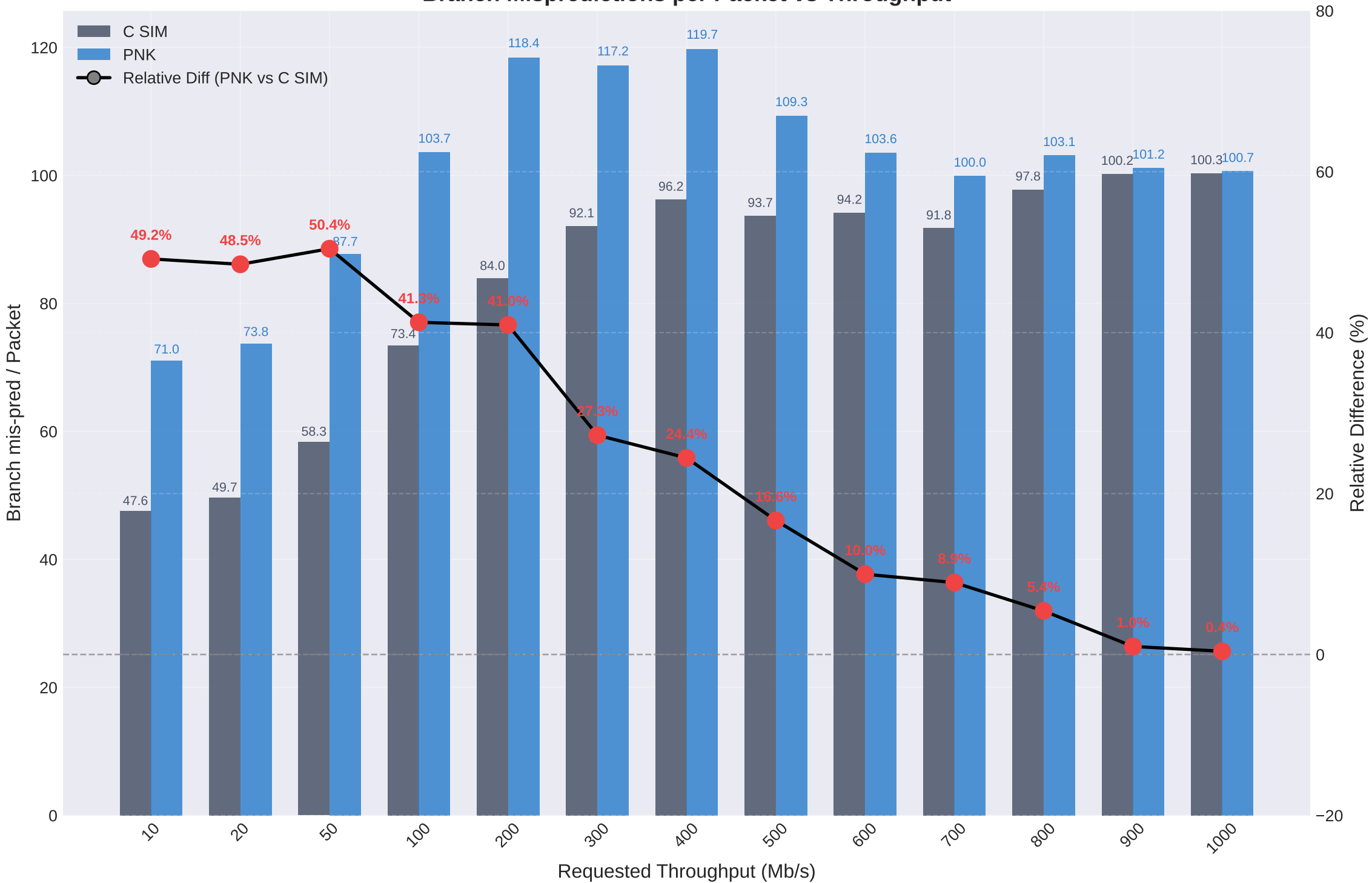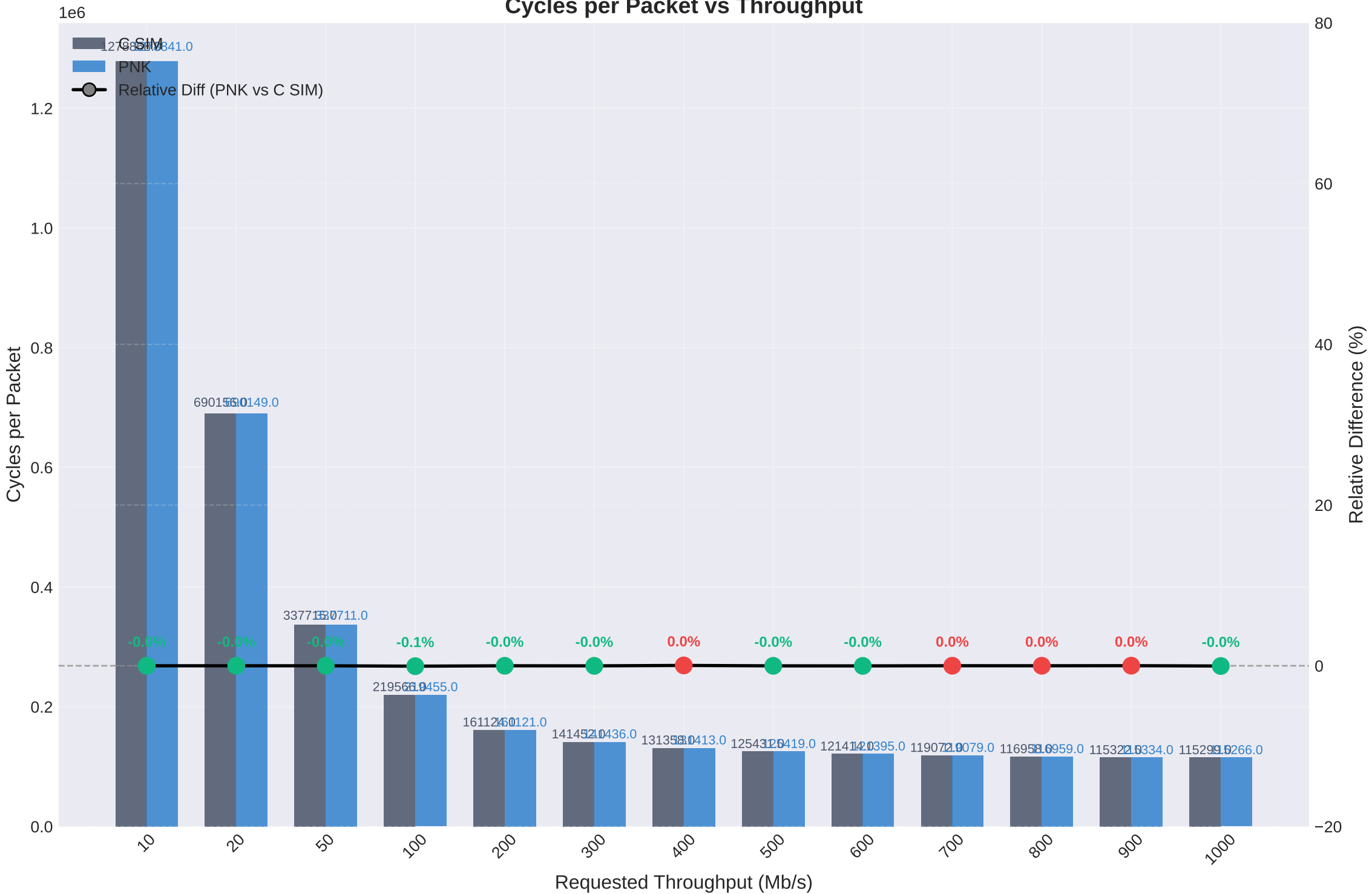
L1 D-TLB Misses per Packet vs Throughput
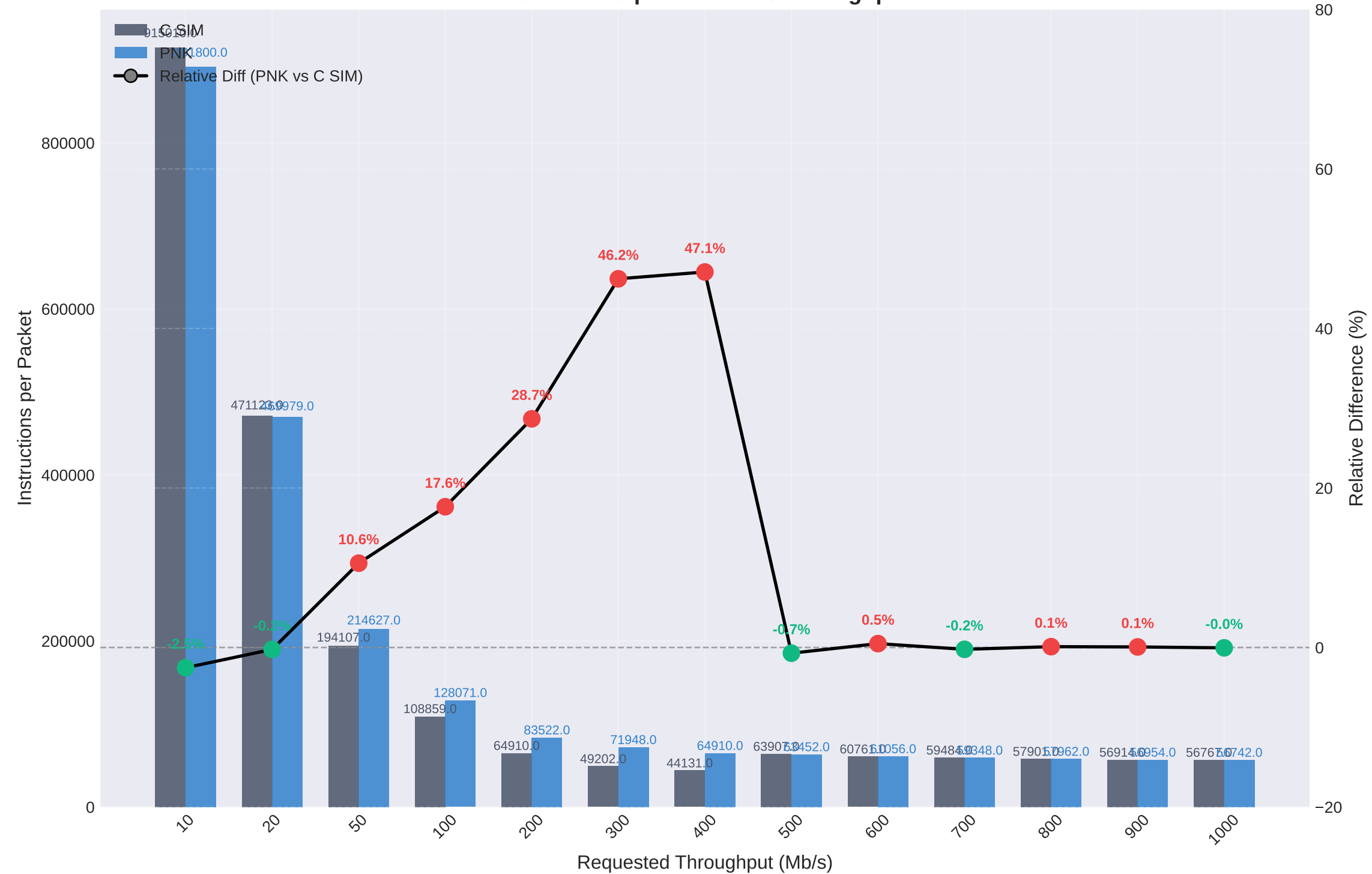
Instructions per Packet vs Throughput

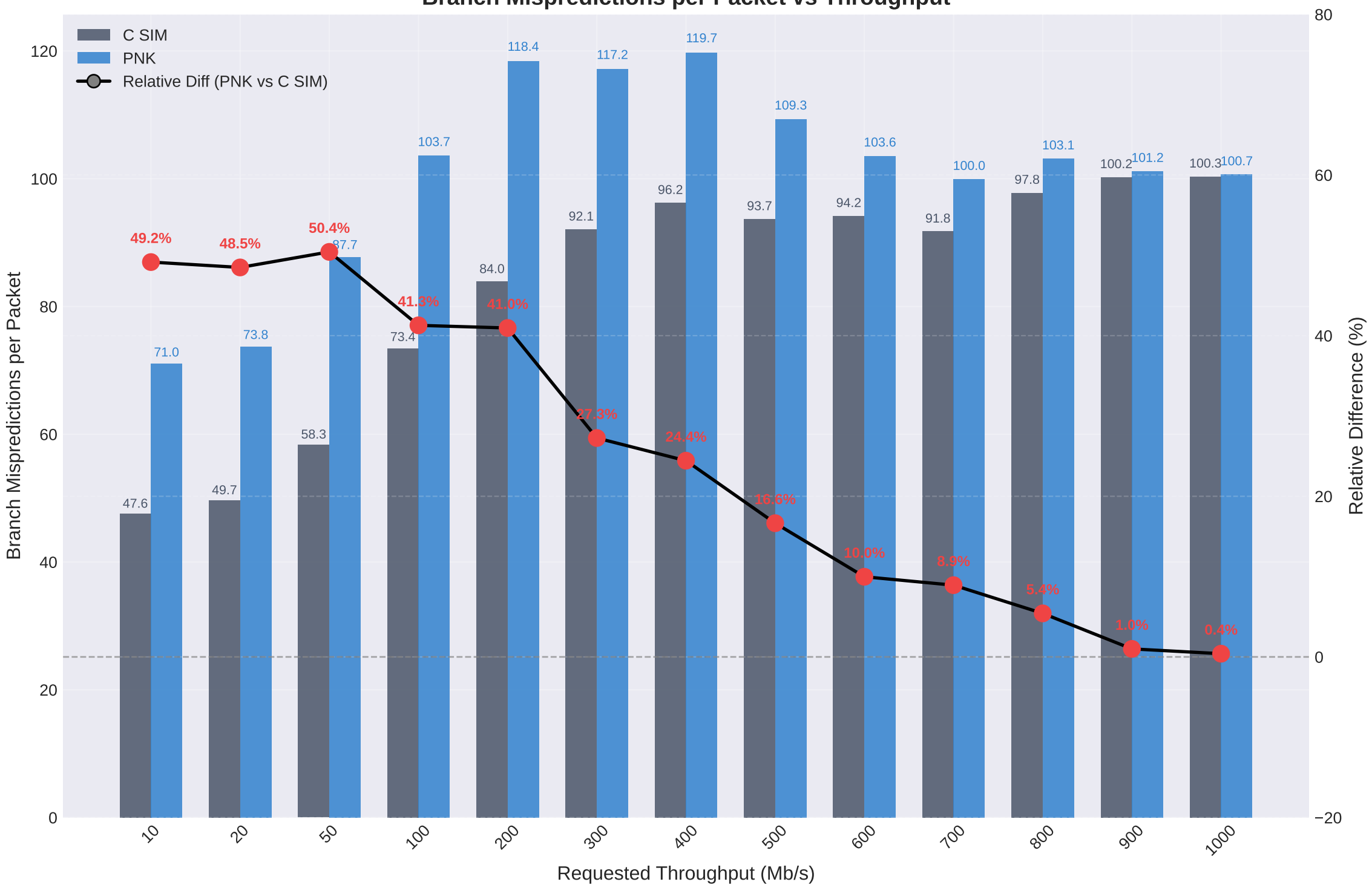Branch Mispredictions per Packet vs Throughput
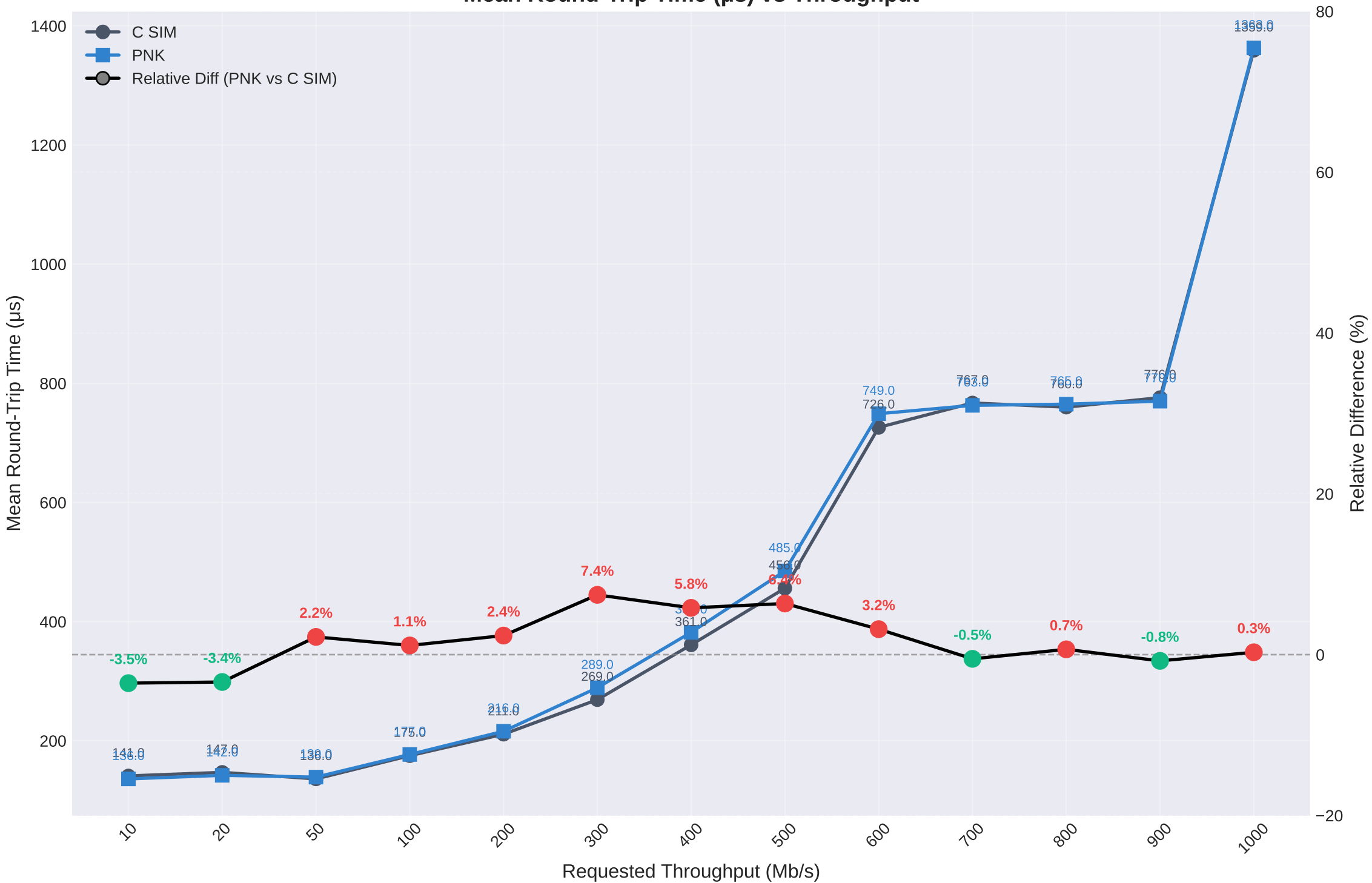
Cycles per Packet vs Throughput

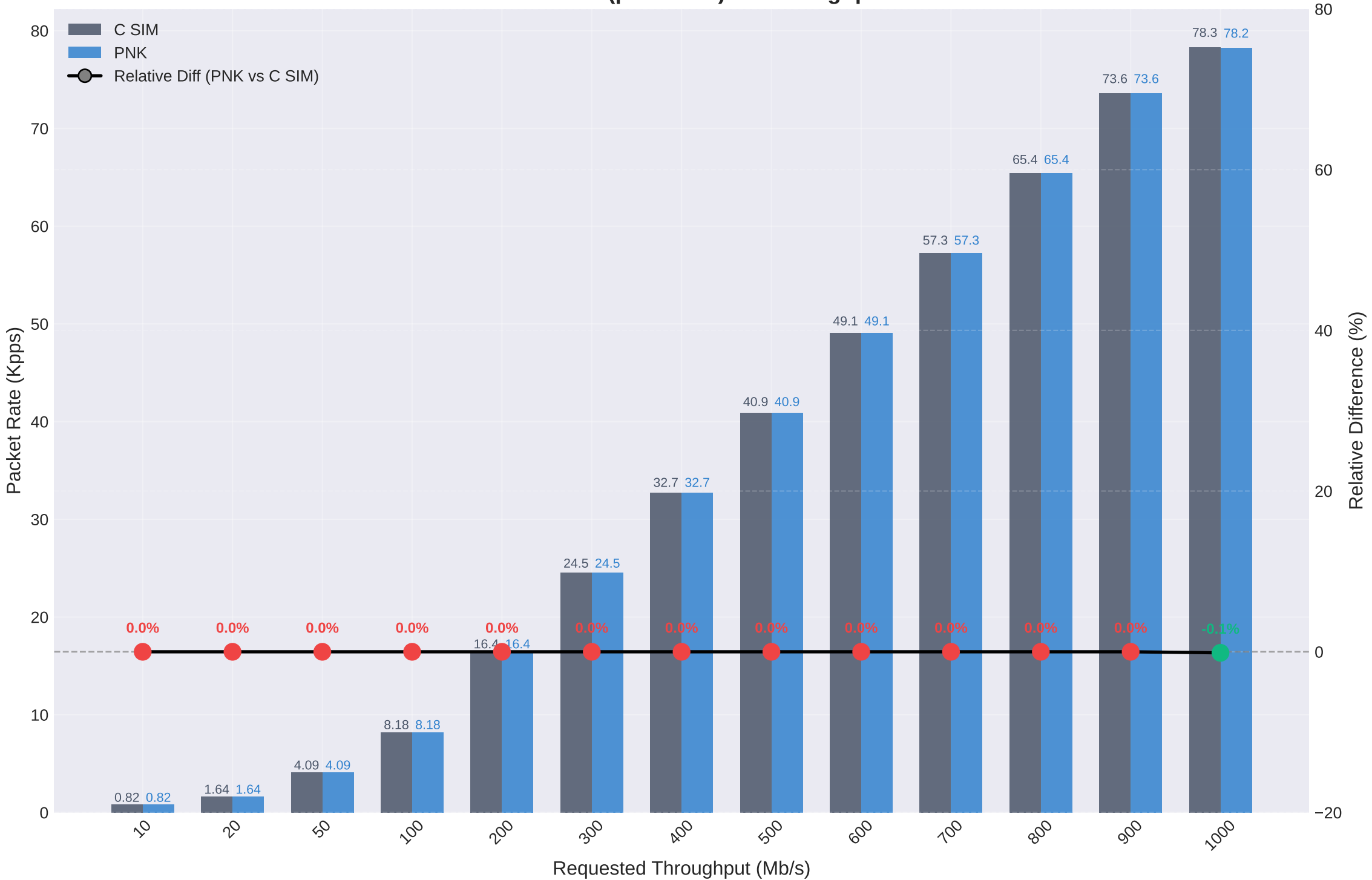Instructions per Packet vs Throughput

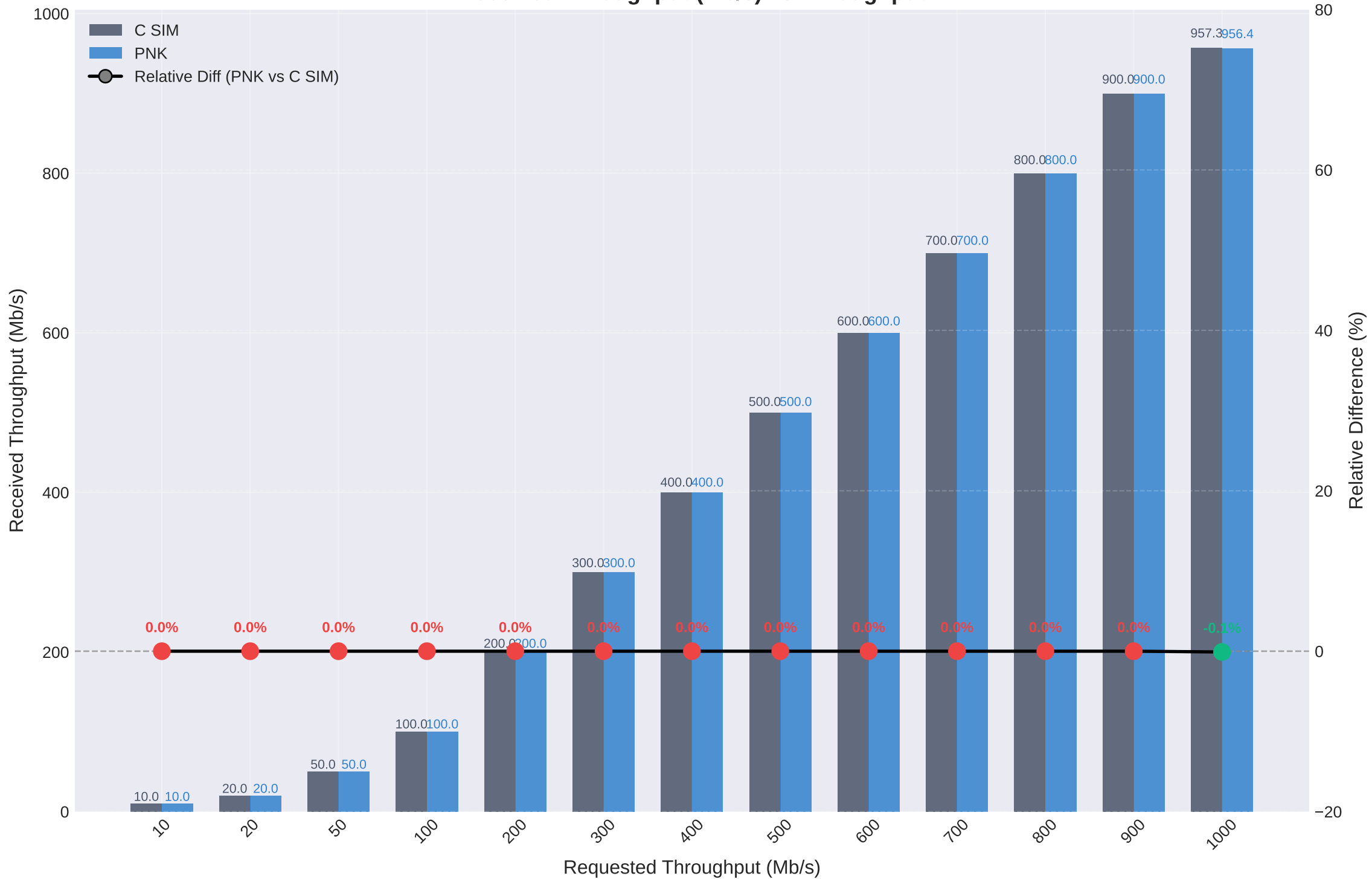Branch Mispredictions per Packet vs Throughput

Mean Round-Trip Time (µs) vs Throughput

Packet Rate (packets/s) vs Throughput

Received Throughput (Mb/s) vs Throughput

Sent Throughput (Mb/s) vs Throughput