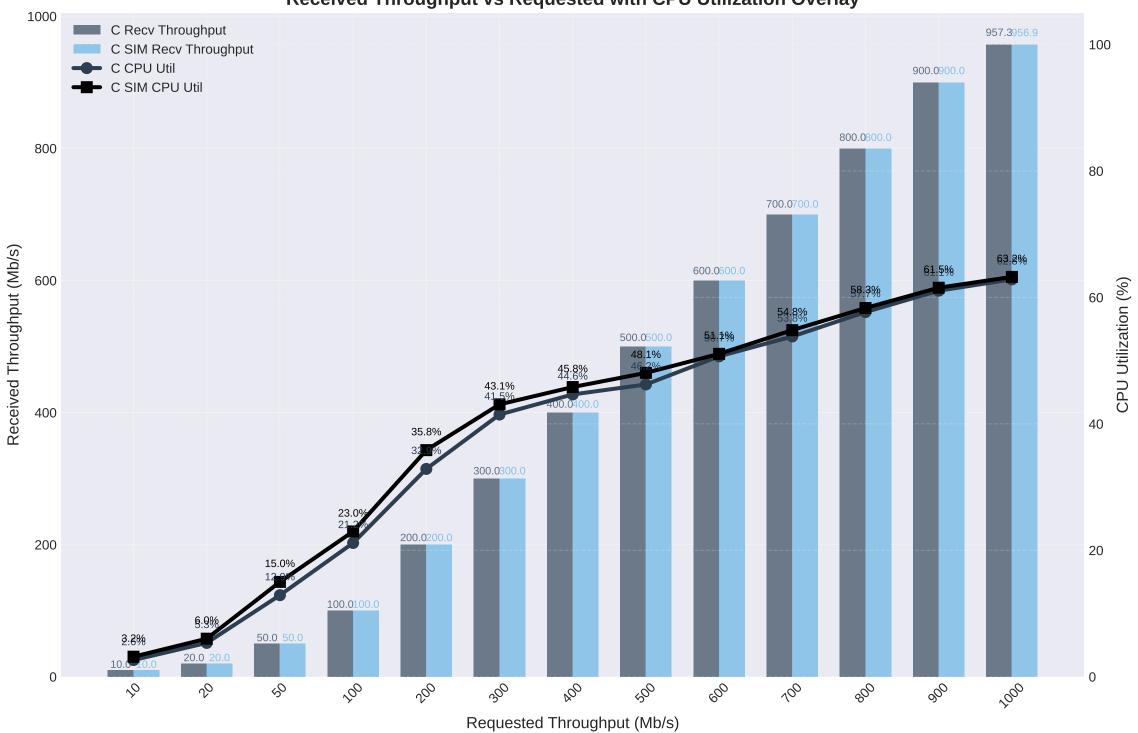
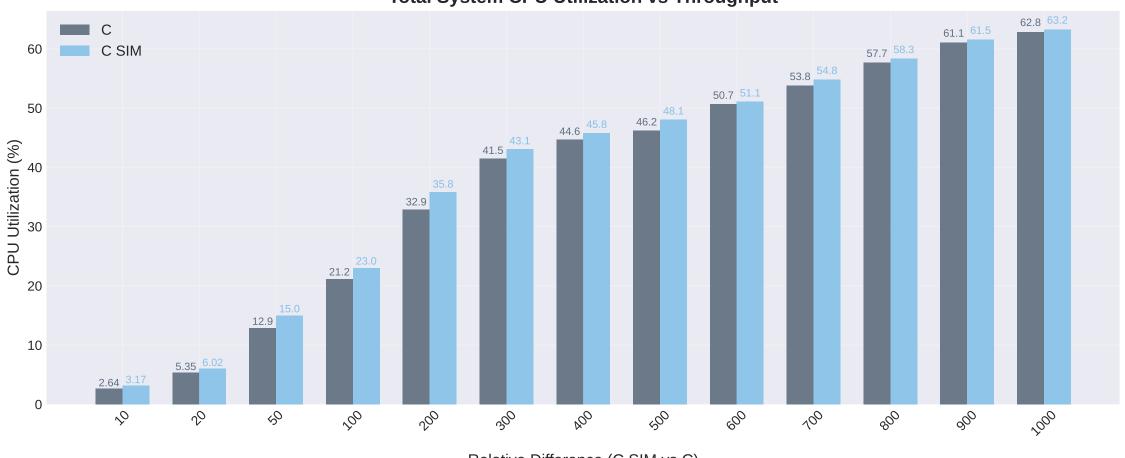
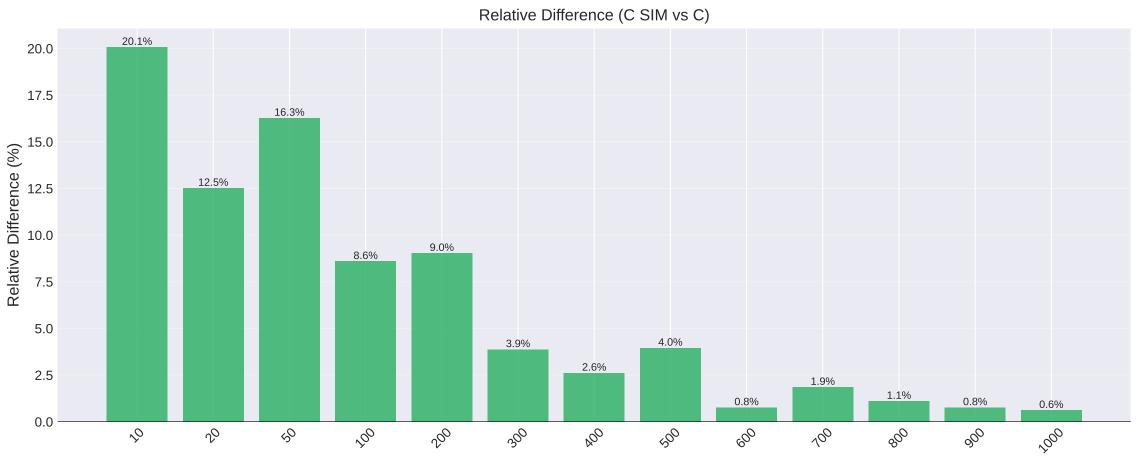
**Instructions per Second vs Throughput** 0.69 0.69 0.7 C 0.66 0.66 C SIM 0.6 0.56 Instructions per Second (Billions) 0.50 0.52 0.51 0.52 0.51 0.51 0.50 0.51 0.50 0.51 0.50 0.51 0.49 0.49 0.40 0.40 0.34 0.35 0.1 0.0 400 200 200 300 NOO 600 700 900 900 2000 30 20 60 Relative Difference (C SIM vs C) 46.7% 40 Relative Difference (%) 10.3% 10 3.3% 2.1% 1.3% 1.3% 1.3% 1.0% 0.5% 0.3% 0 -0.1% \$0 20 60 200 200 300 NOO 400 600 100 900 900

**Received Throughput vs Requested with CPU Utilization Overlay** 

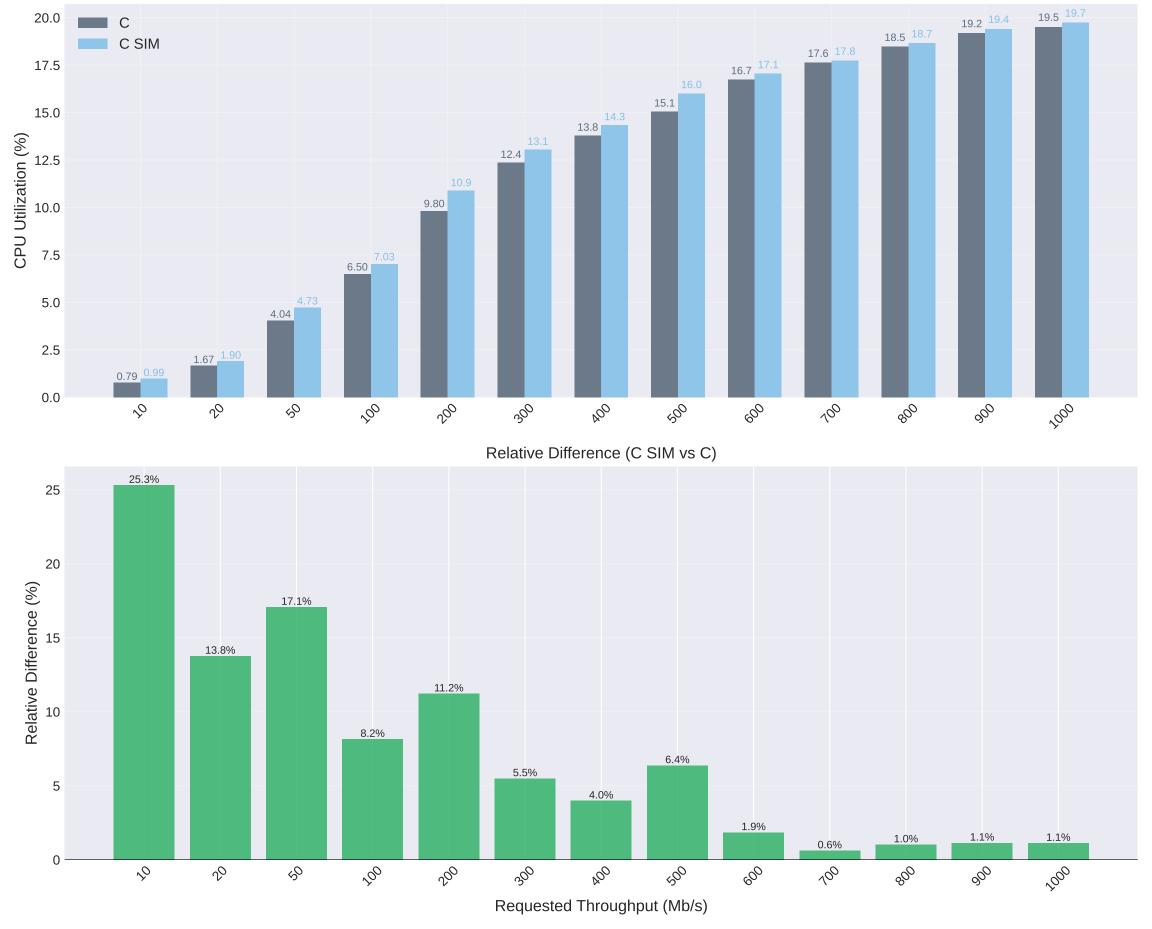


**Total System CPU Utilization vs Throughput** 



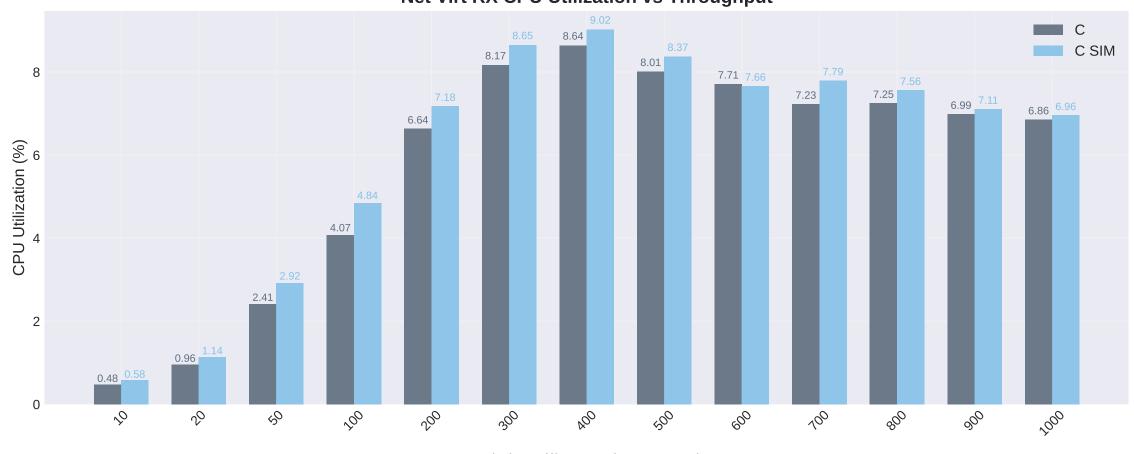


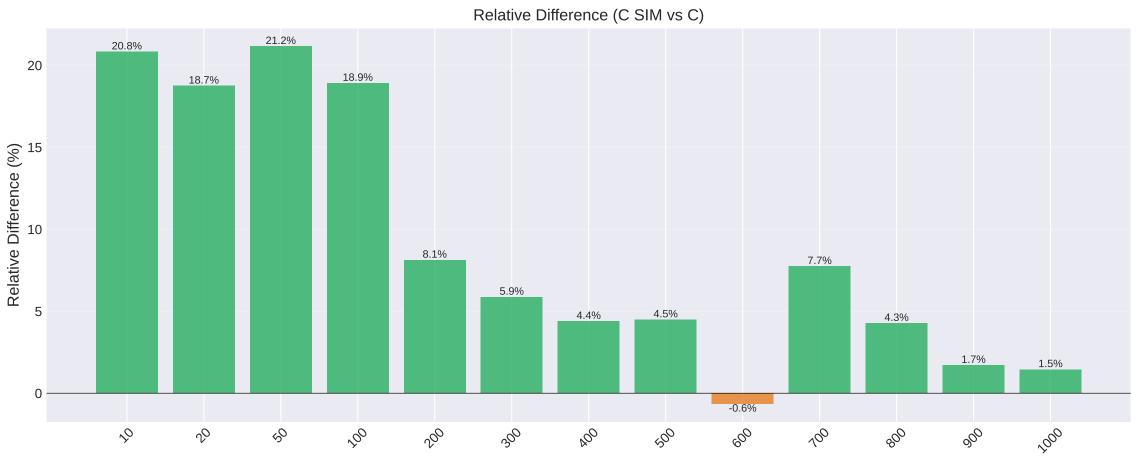
**Ethernet Driver CPU Utilization vs Throughput** 



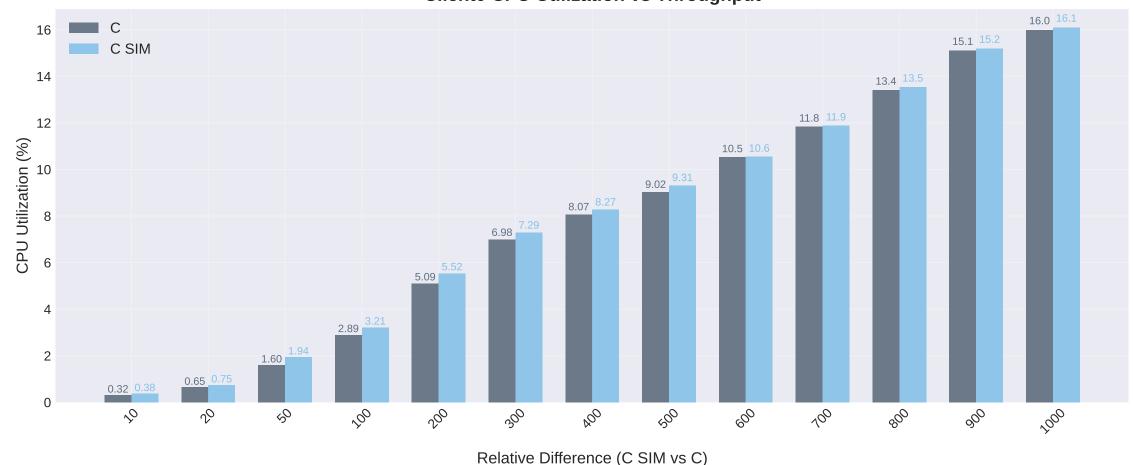


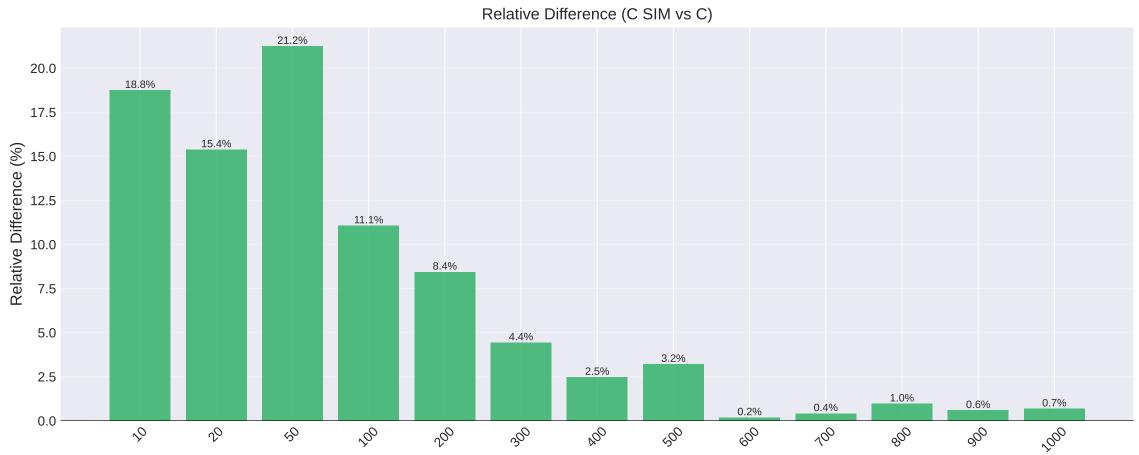
## **Net Virt RX CPU Utilization vs Throughput**

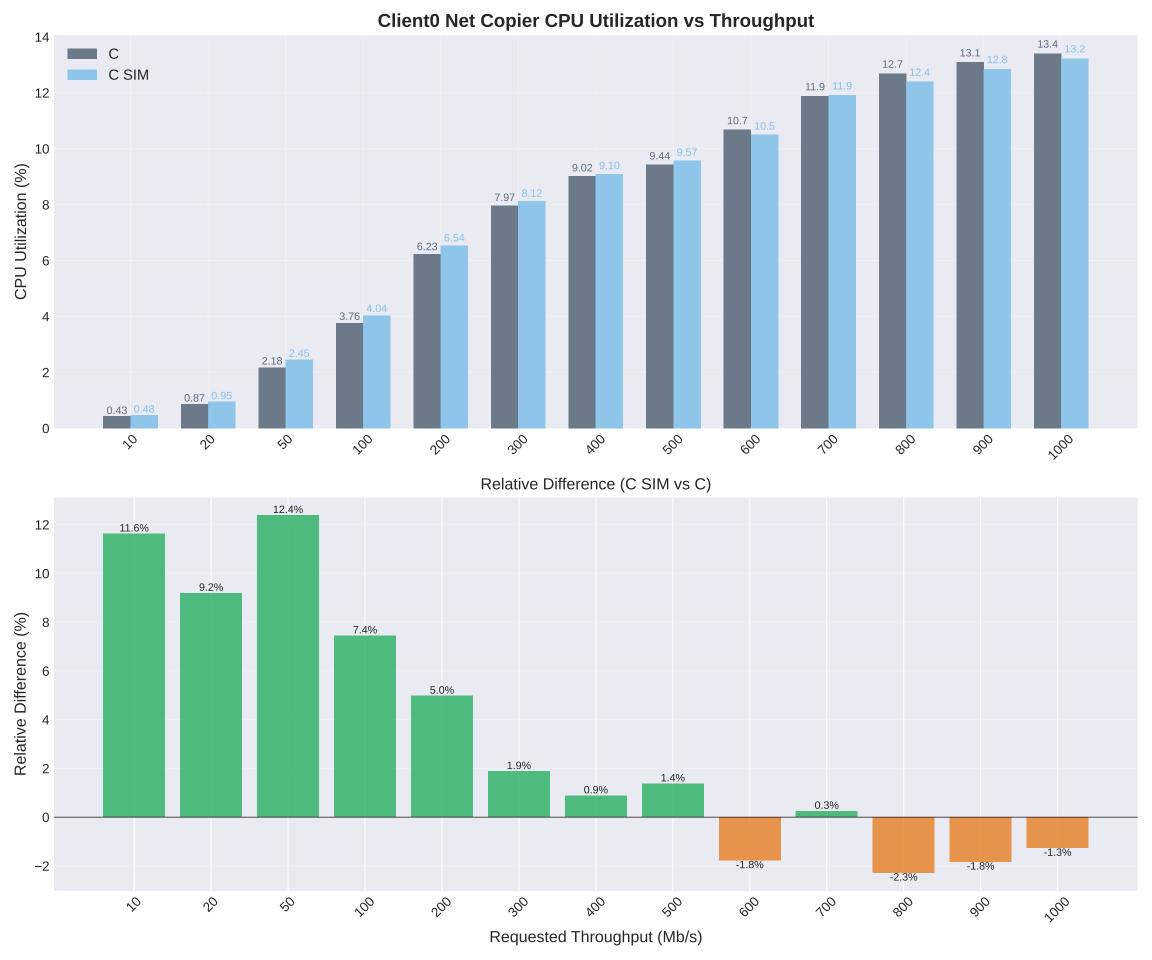




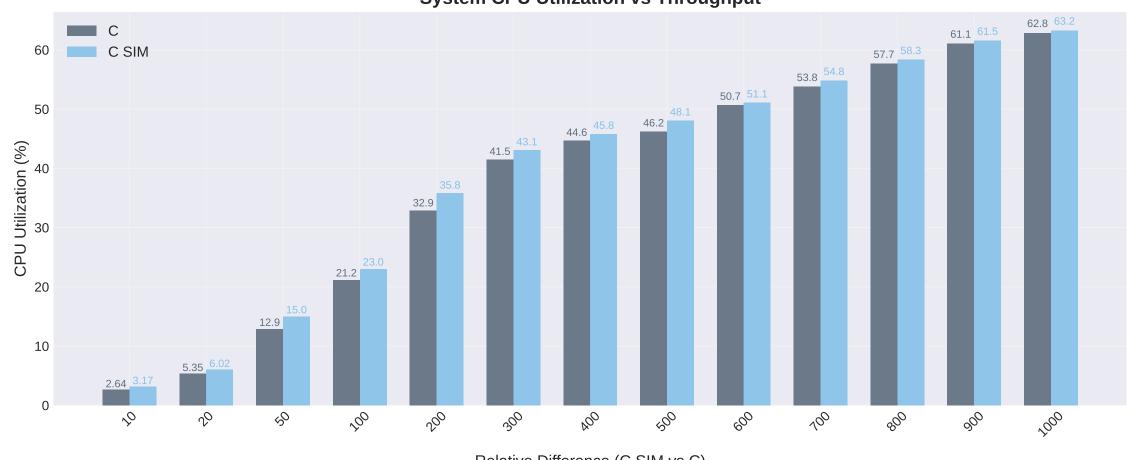
**Client0 CPU Utilization vs Throughput** 

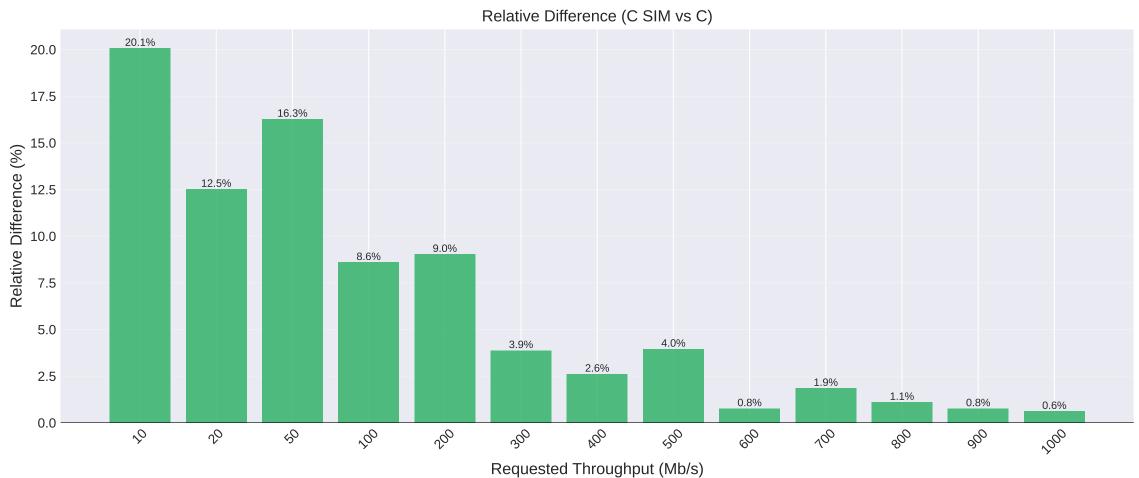


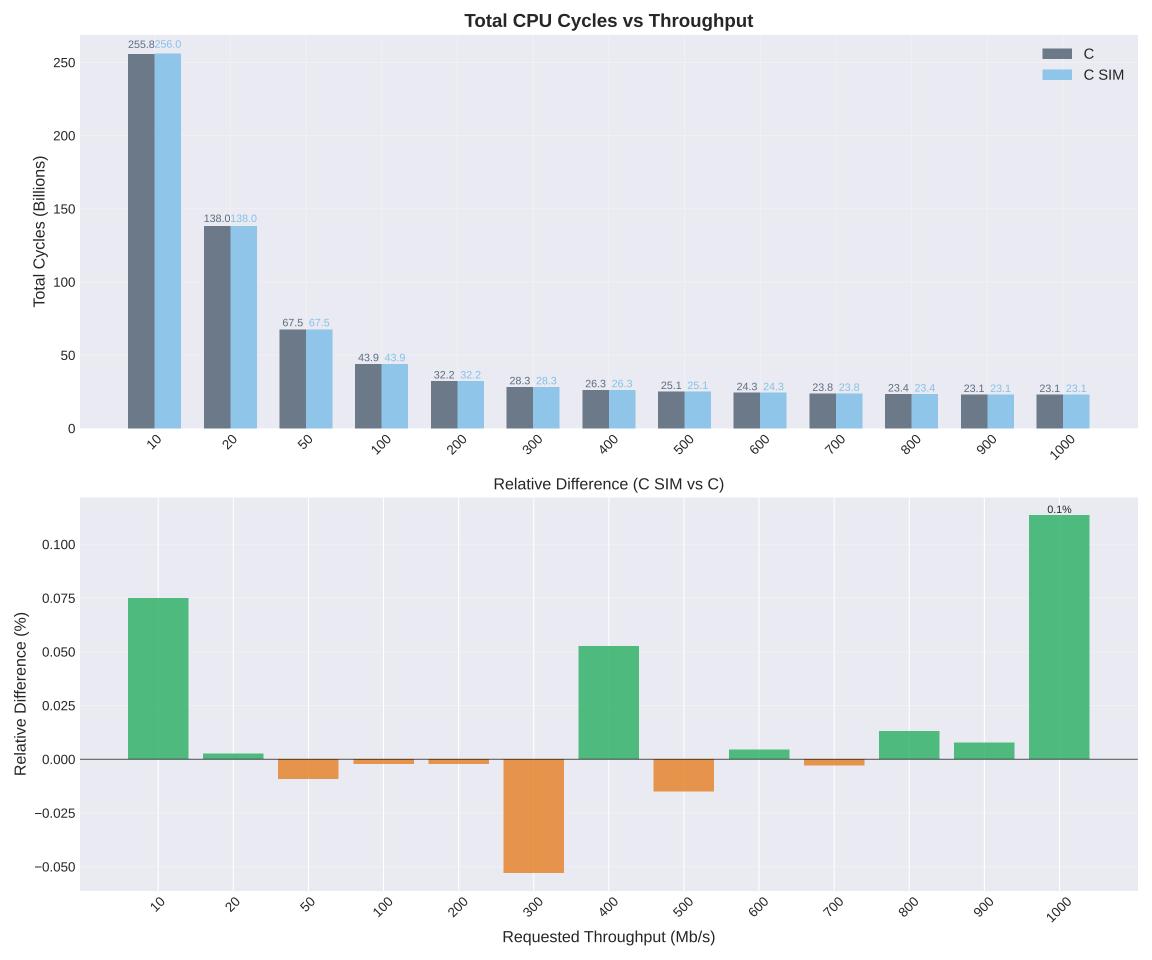




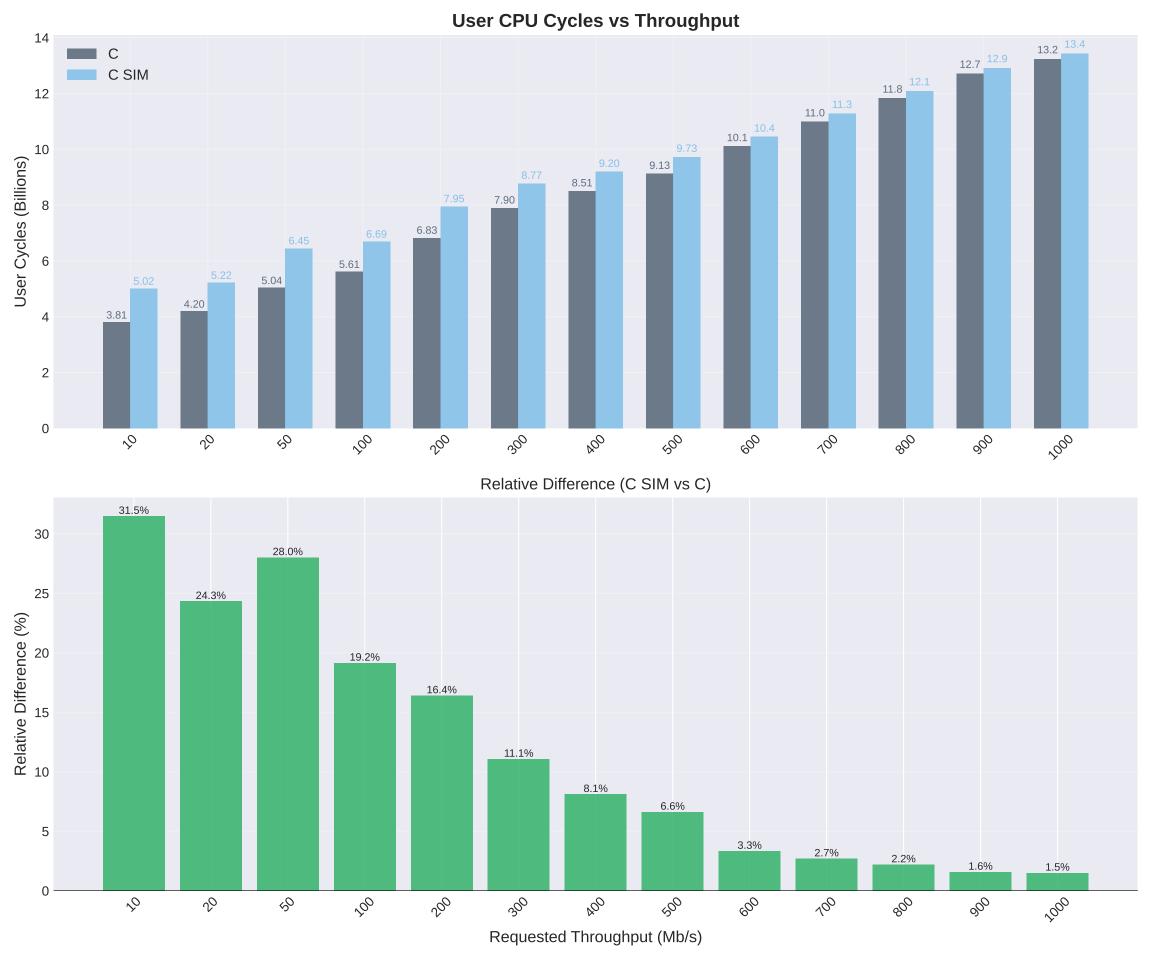
**System CPU Utilization vs Throughput** 





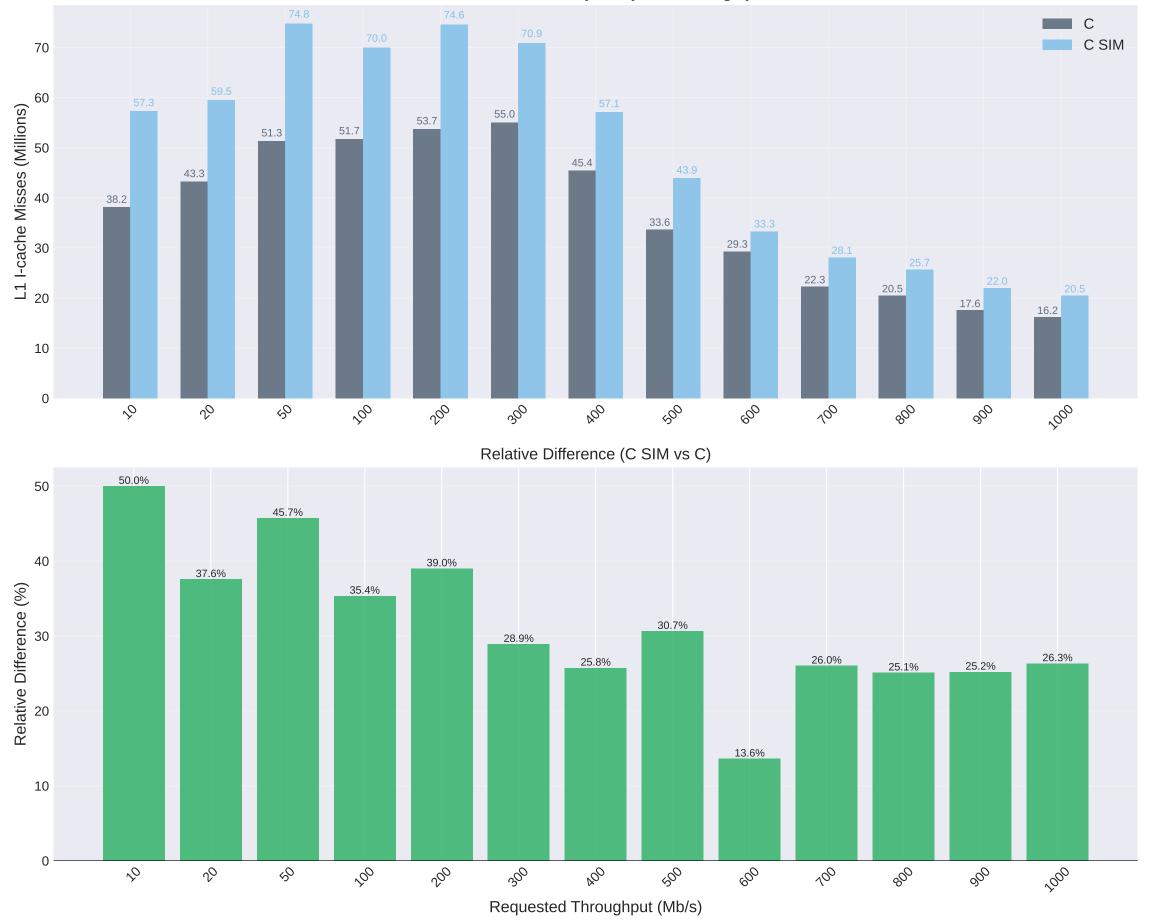


**Kernel CPU Cycles vs Throughput** 3.5 C 3.30 C SIM 3.02 3.10 3.06 2.99 3.0 2.52 2.46 Kernel Cycles (Billions) 1.5 1.0 2.38 2.36 2.26 2.10 1.73 1.55 1.27 0.5 0.0 100 200 300 NOO 400 100 7000 \$0 20 600 900 900 50 Relative Difference (C SIM vs C) 5.6% 5.0 2.4% 2.5 Relative Difference (%) 0.0 -2.5 -2.2% -3.6% -5.0 -5.0% -5.3% -6.0% -7.1% -7.5 -7.4% -8.0% -10.0 -10.2% -10.3% -11.6% -12.5 30 20 50 200 200 300 NOO 400 600 700 900 Requested Throughput (Mb/s)

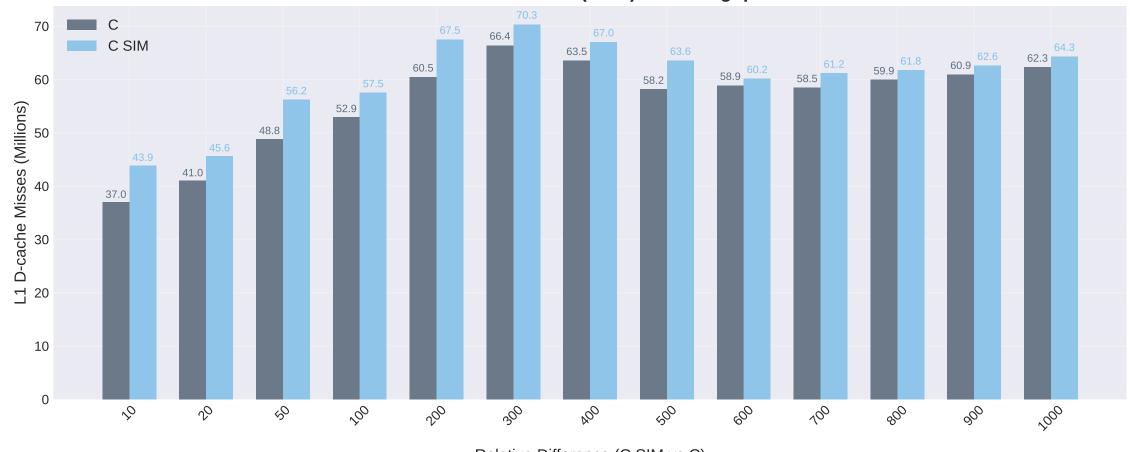


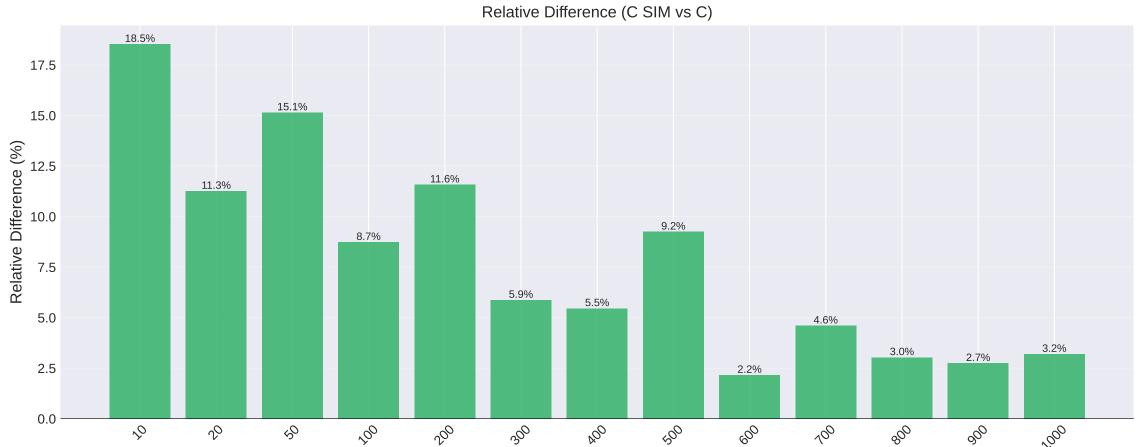
Idle CPU Cycles vs Throughput 249.0247.8 250 C C SIM 200 Idle Cycles (Billions) 130.6129.7 58.8 57.4 50 34.6 33.8 21.6 20.7 16.6 16.1 14.5 14.2 13.5 13.0 12.0 11.9 11.0 10.8 9.90 9.75 8.57 8.49 8.98 8.87 0 \$0 200 200 300 NOO 400 600 700 800 900 2000 20 60 Relative Difference (C SIM vs C) 0 -0.5% -0.7% -0.8% -1 -0.9% -1.2% Relative Difference (%)  $\overset{\ \, \sqcup}{\ \, }$ -1.5% -2.1% -2.2% -2.3% -2.4% -2.8% -3.4% -4 -4.4% 30 20 SO 200 200 300 NOO 400 600 100 900 Requested Throughput (Mb/s)

**L1** I-cache Misses (Total) vs Throughput

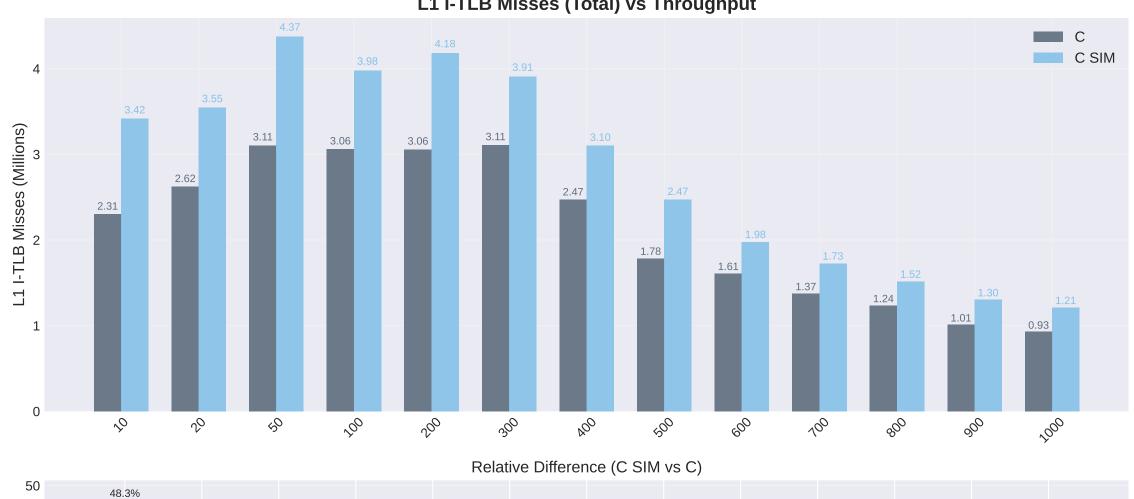


## L1 D-cache Misses (Total) vs Throughput



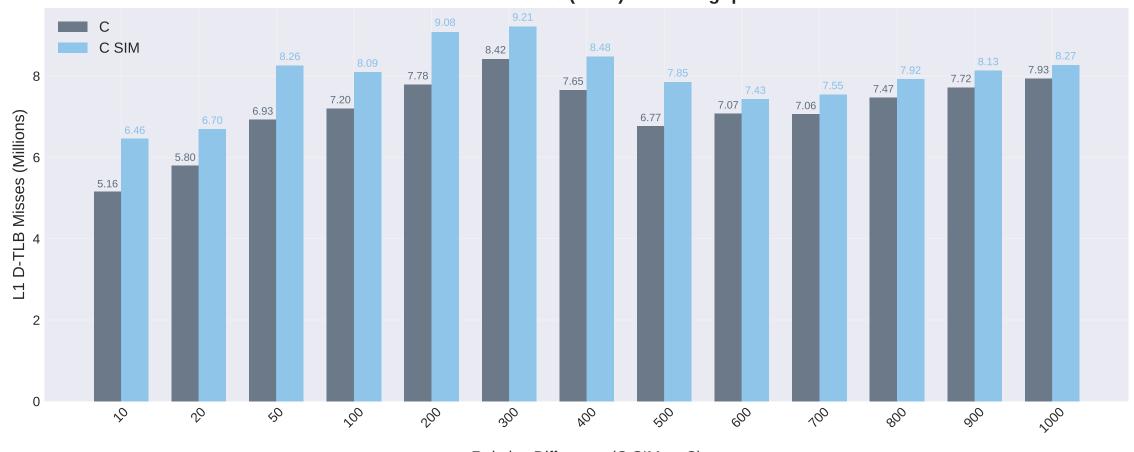


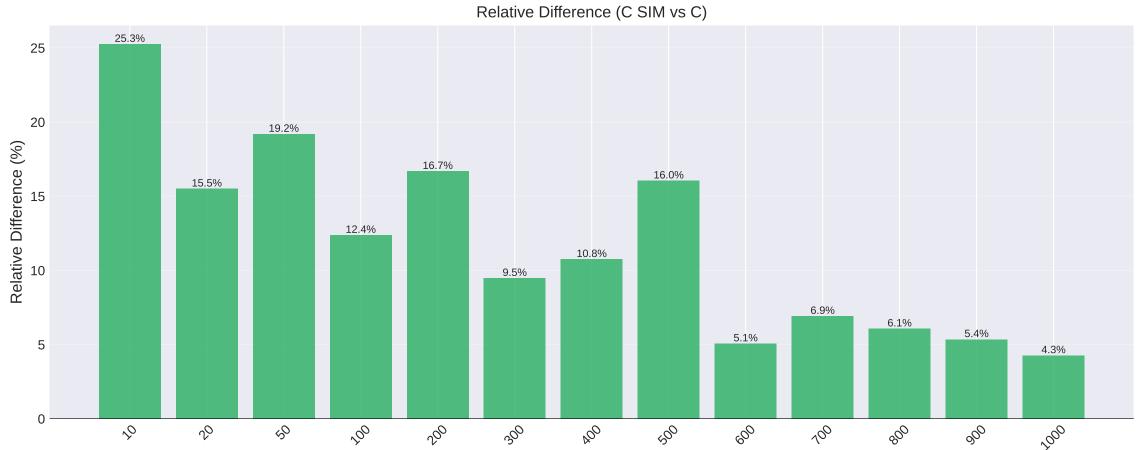
L1 I-TLB Misses (Total) vs Throughput



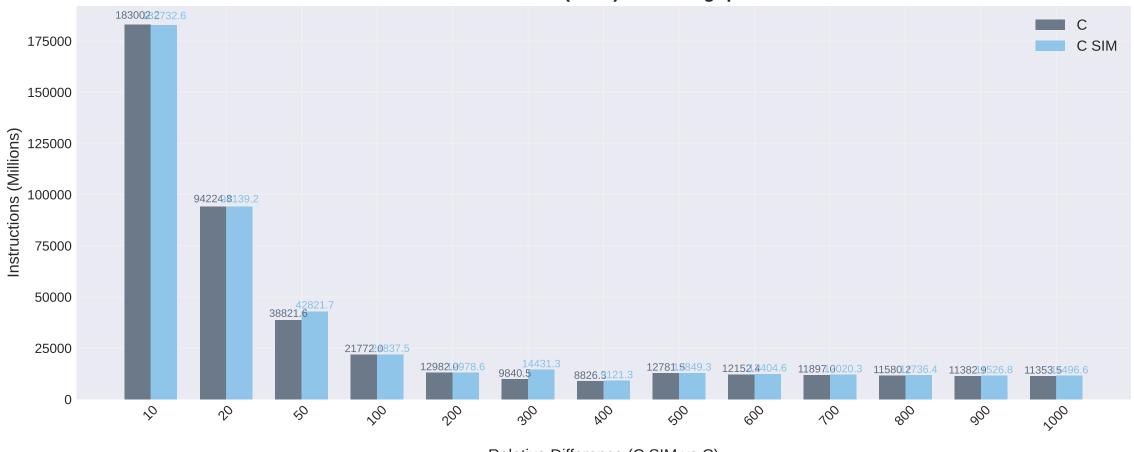


## L1 D-TLB Misses (Total) vs Throughput

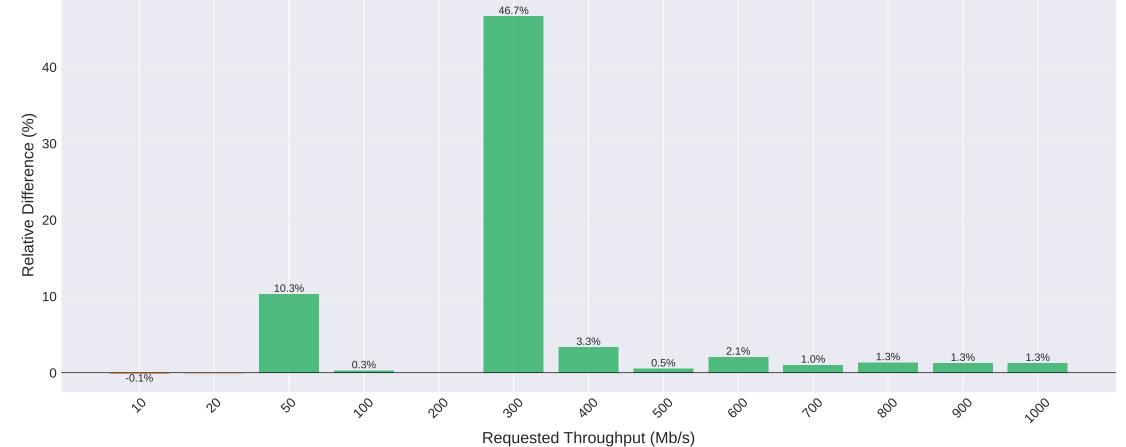




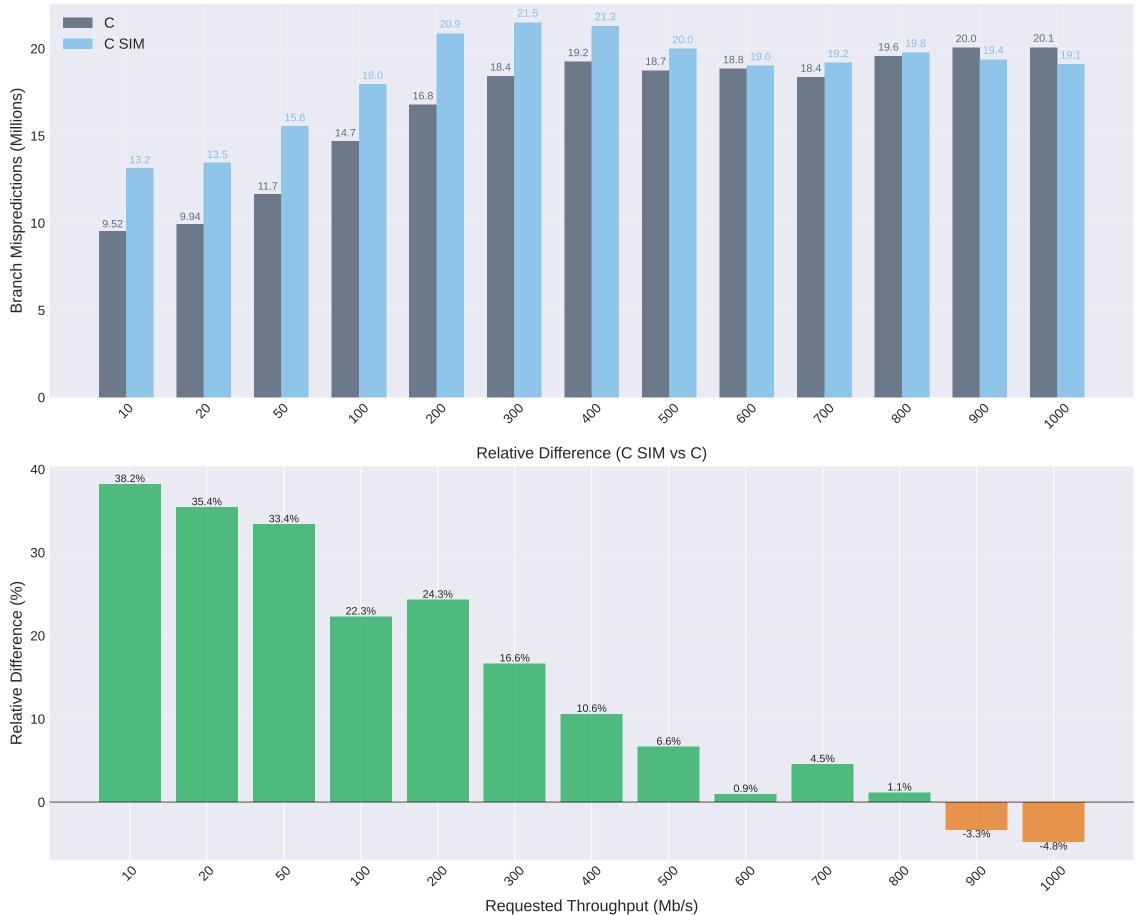




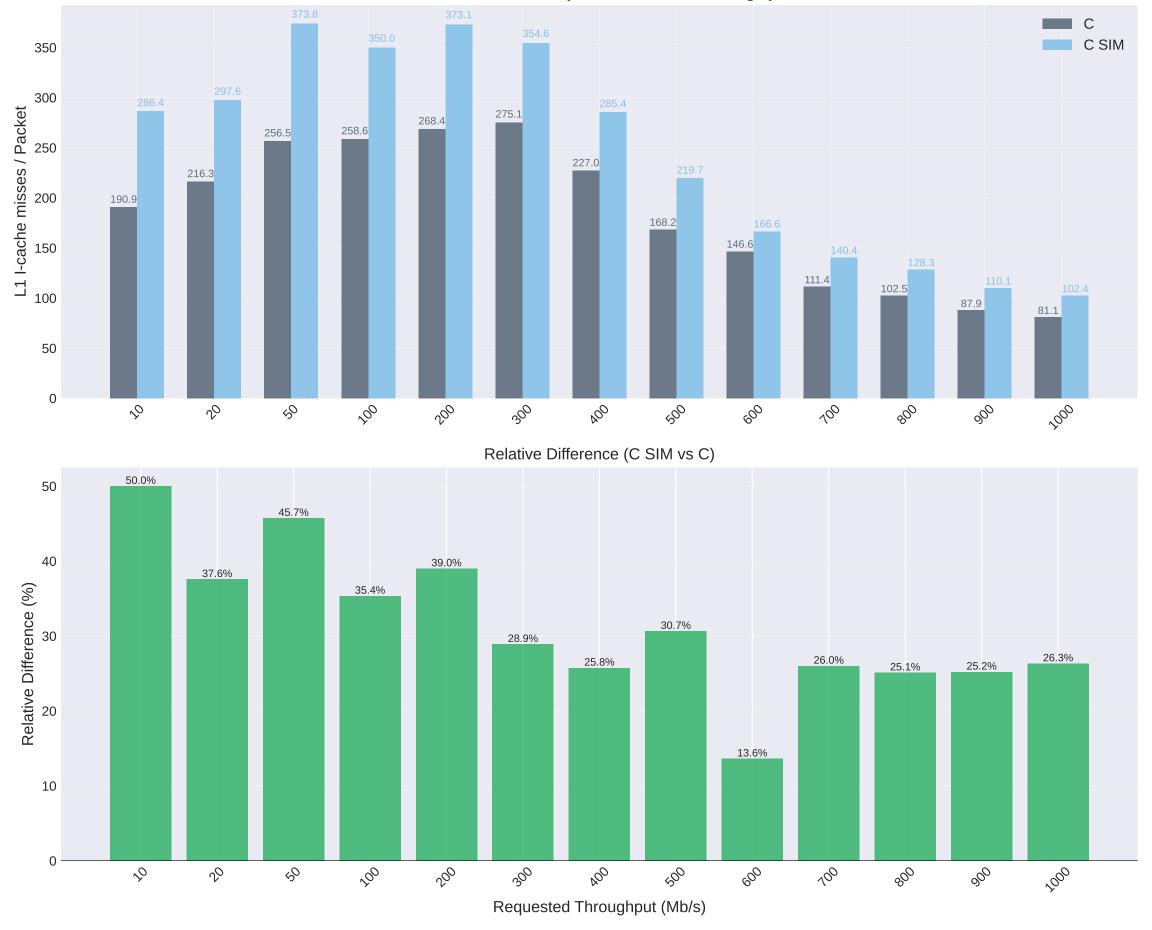




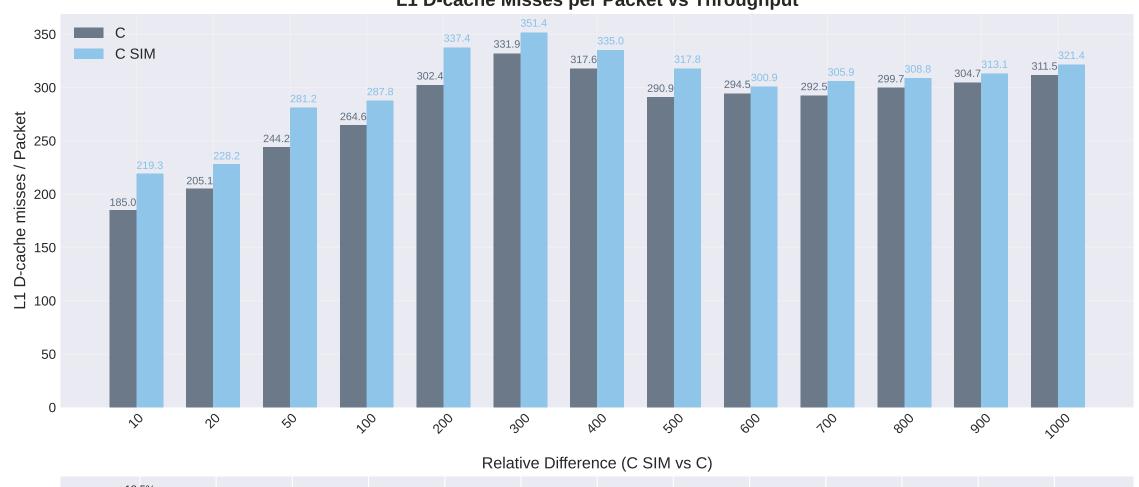
**Branch Mispredictions (Total) vs Throughput** 

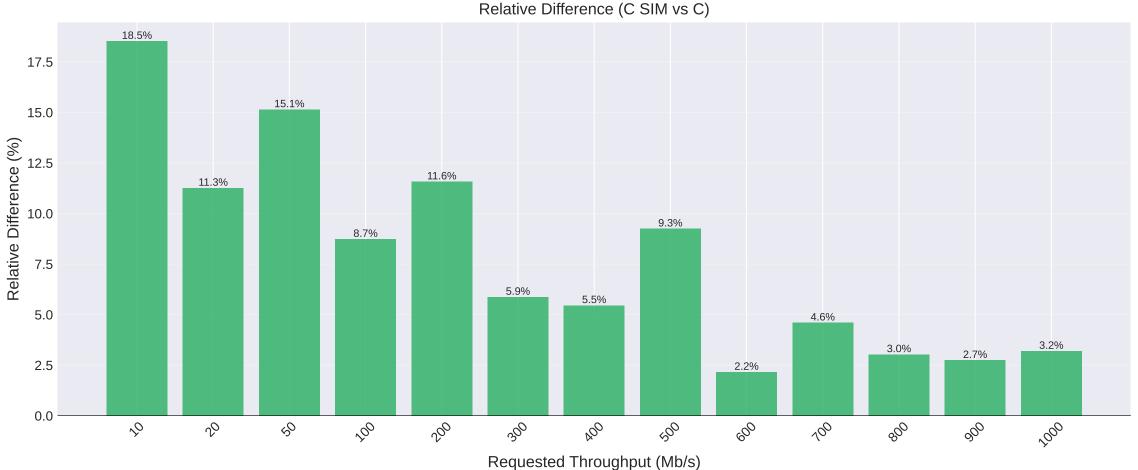


**L1** I-cache Misses per Packet vs Throughput

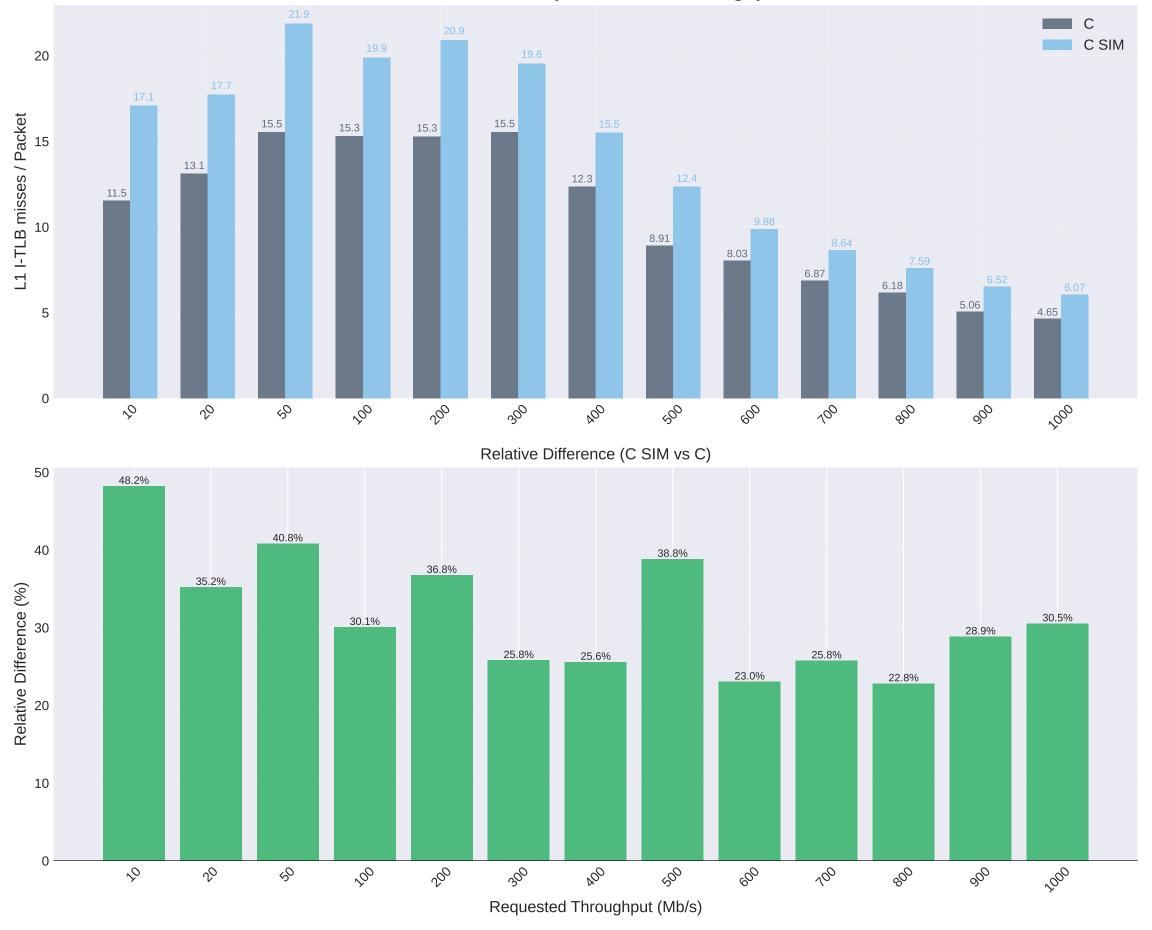


**L1** D-cache Misses per Packet vs Throughput

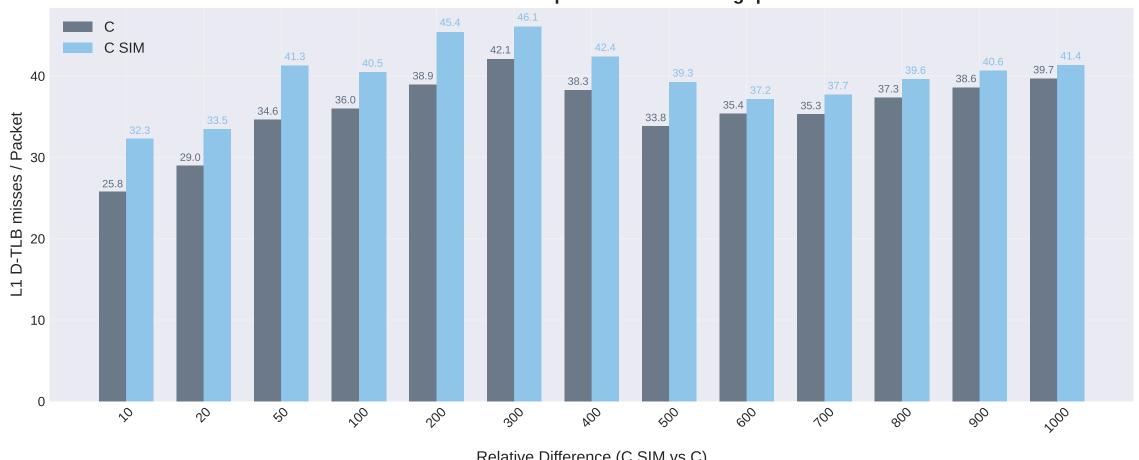


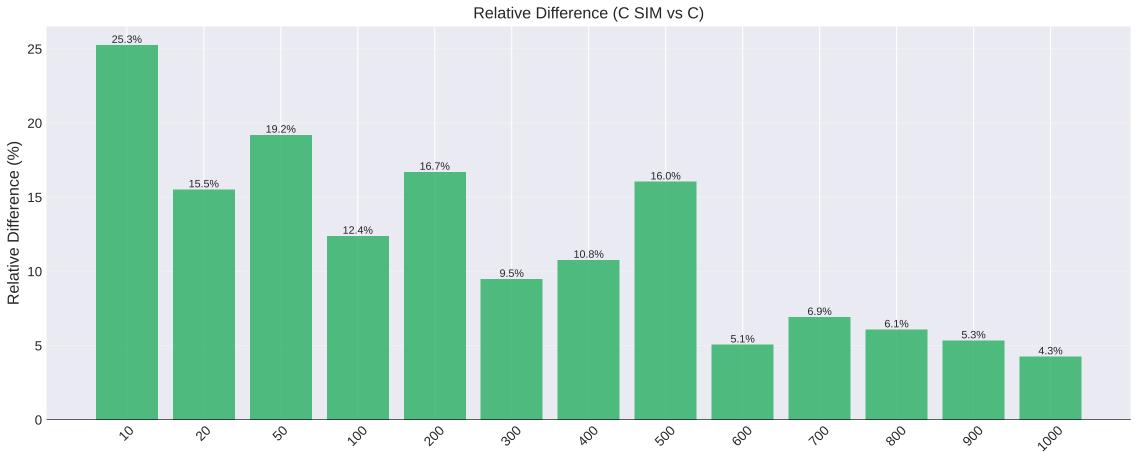


**L1 I-TLB Misses per Packet vs Throughput** 

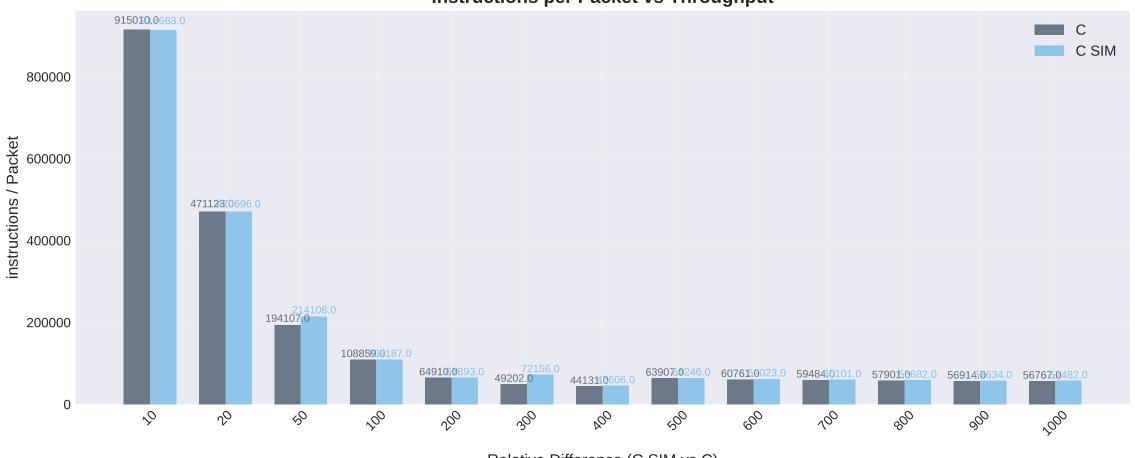


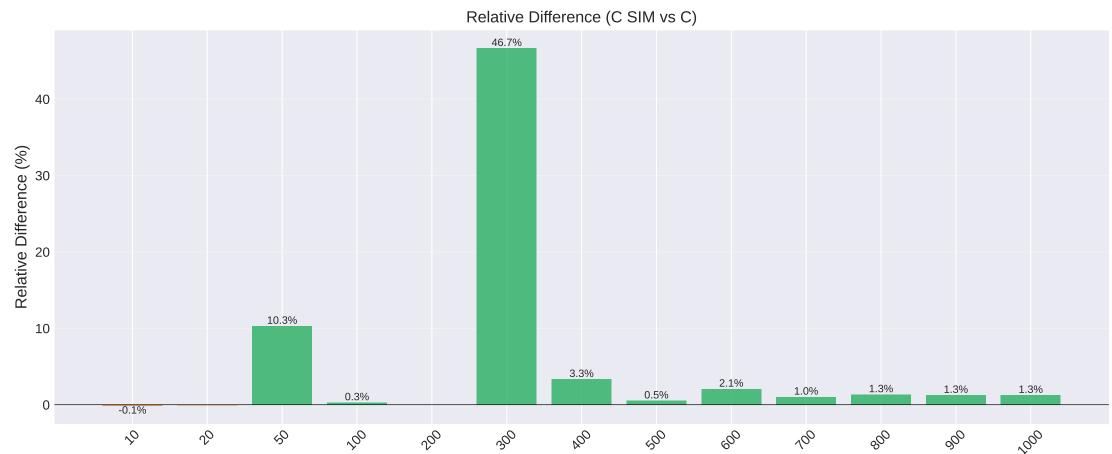
## **L1 D-TLB Misses per Packet vs Throughput**



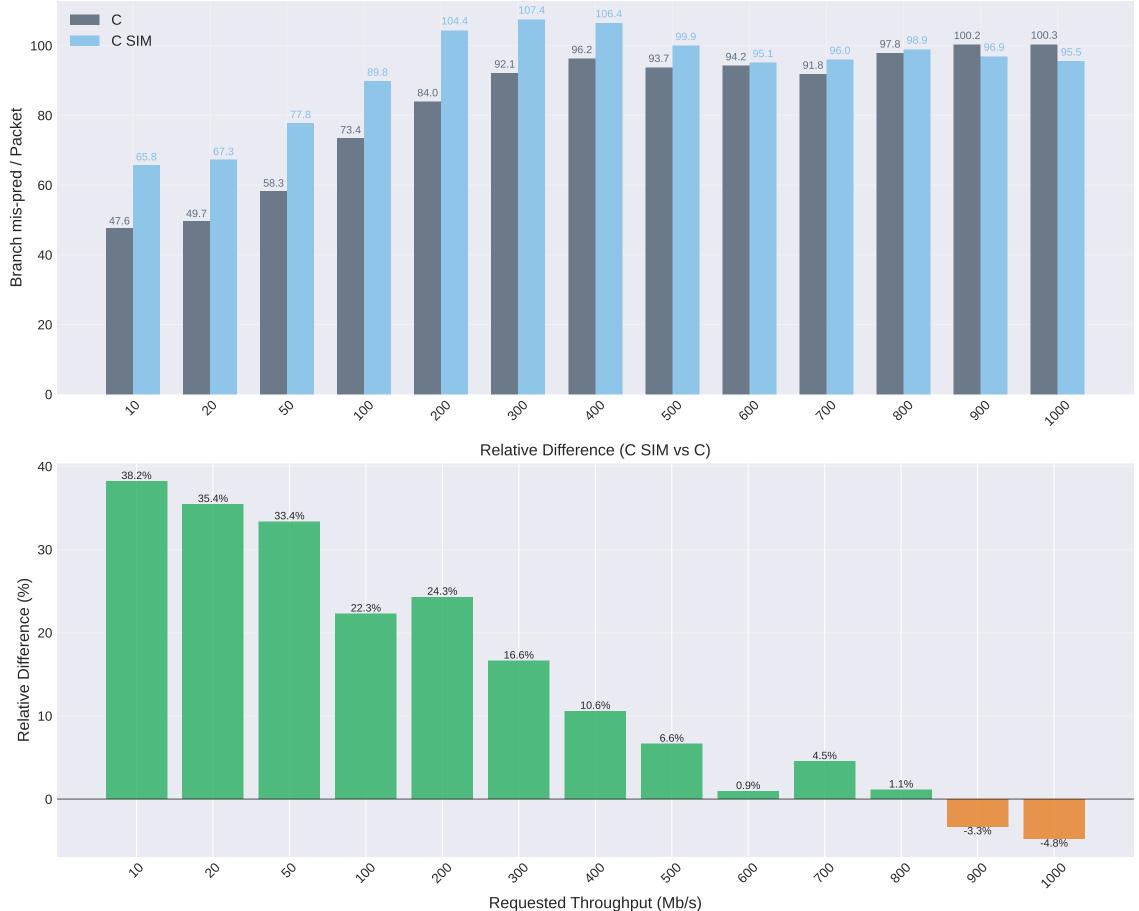


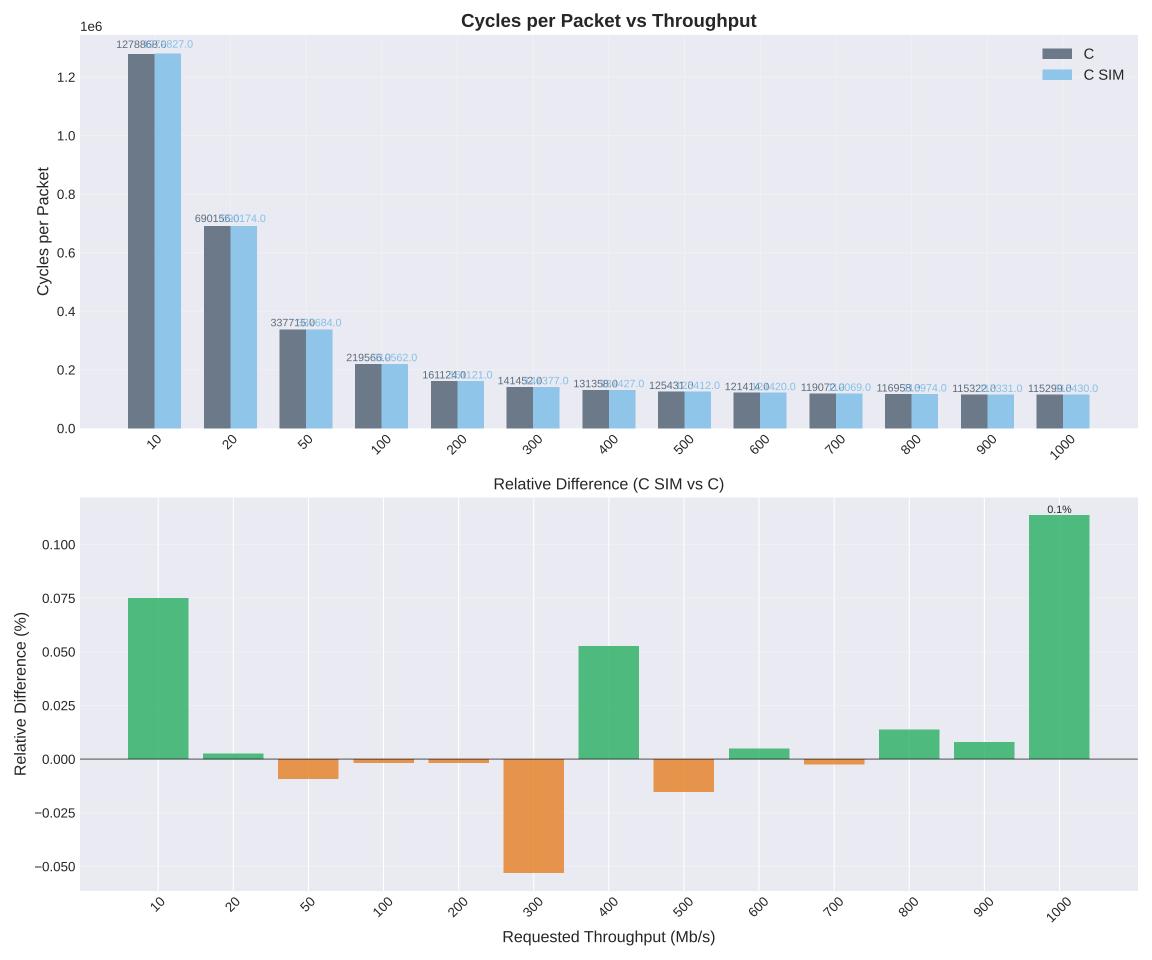




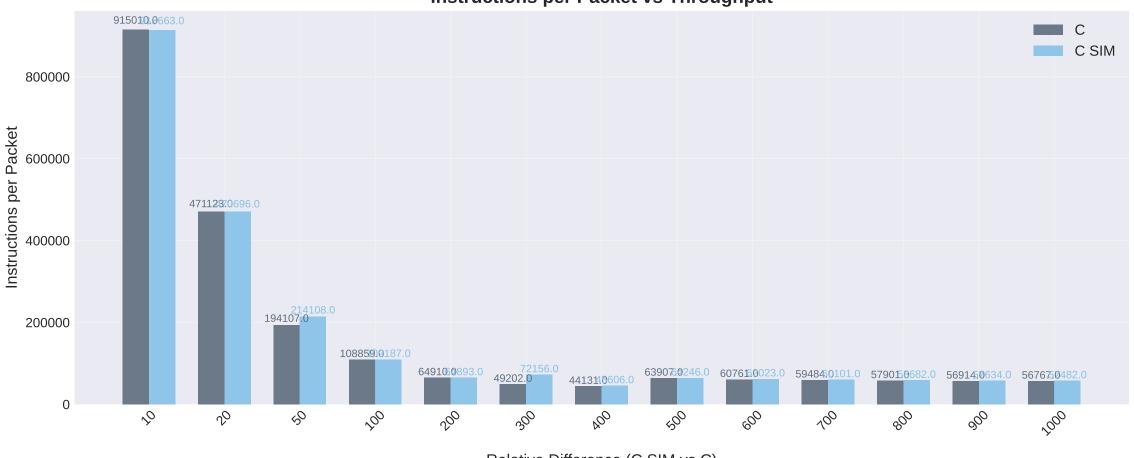


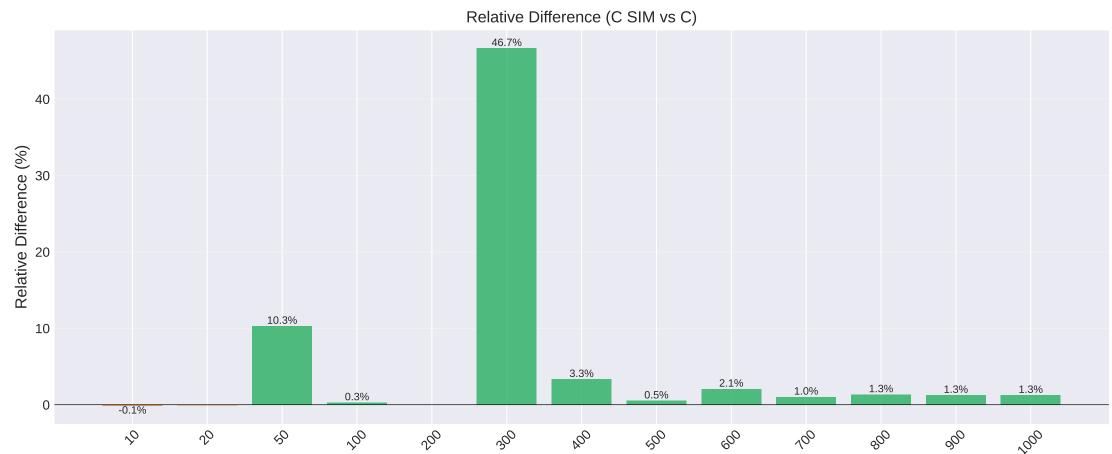
Branch Mispredictions per Packet vs Throughput



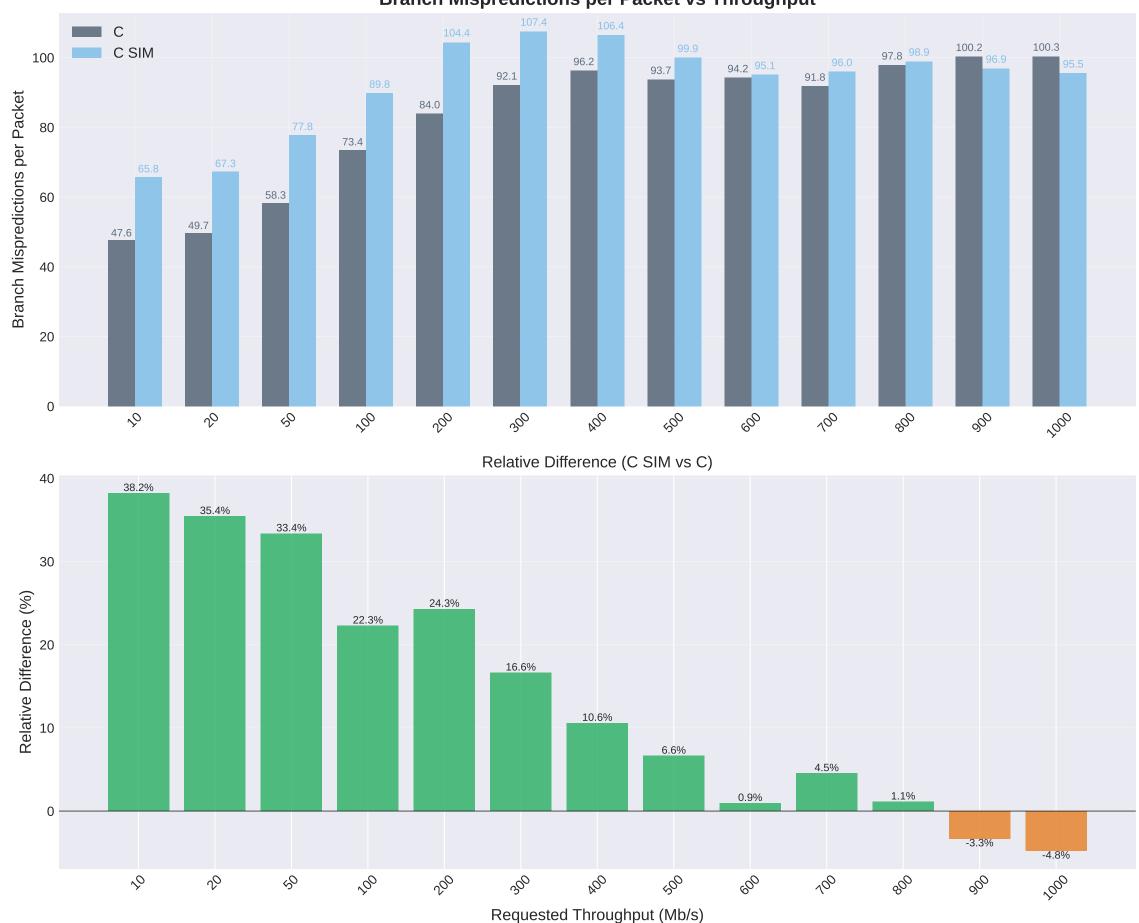




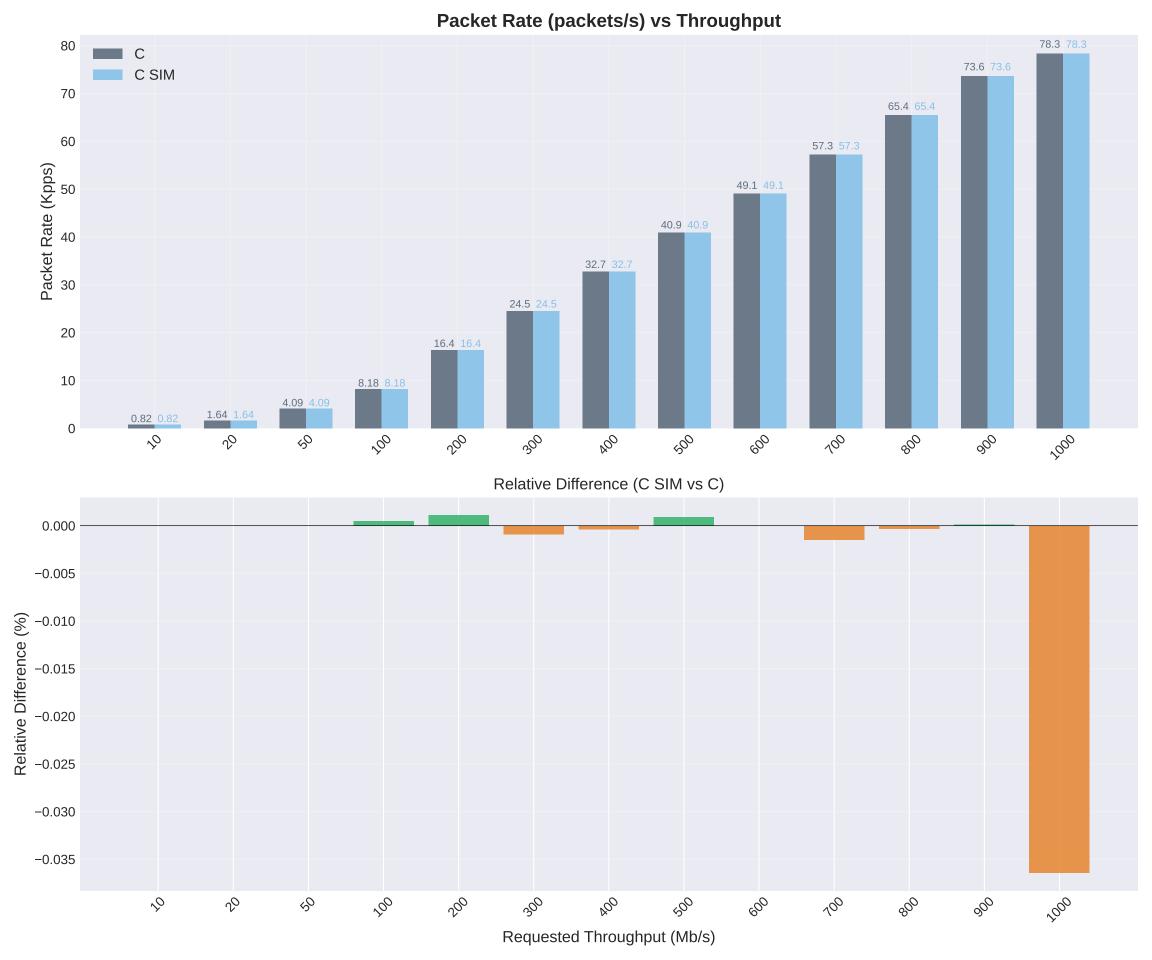


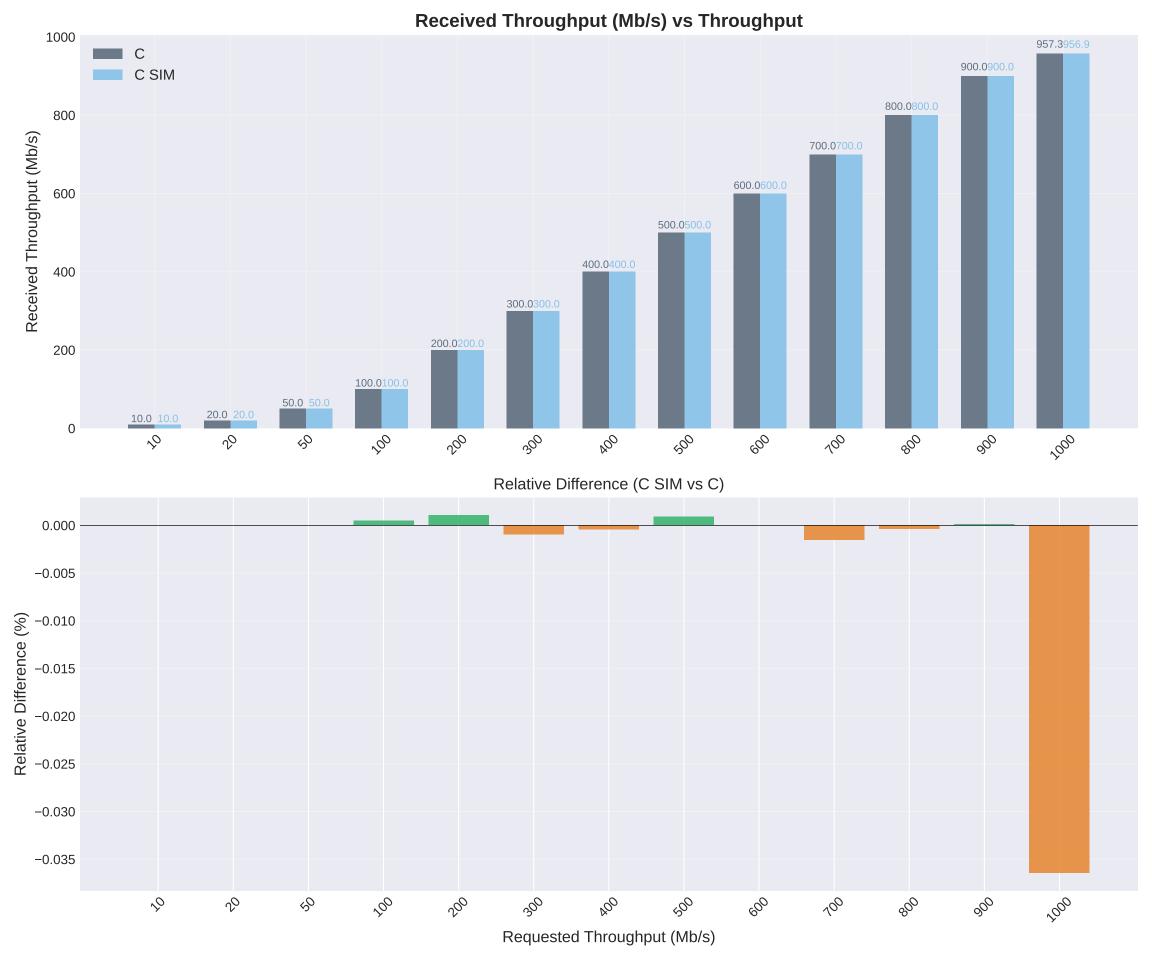


Branch Mispredictions per Packet vs Throughput









Sent Throughput (Mb/s) vs Throughput 1000.0000.0 С 1000 C SIM 900.0900.0 800.0800.0 800 Sent Throughput (Mb/s) 700.0700.0 600.0600.0 600 500.0500.0 400.0400.0 400 300.0300.0 200.0200.0 200 100.0100.0 50.0 50.0 20.0 20.0 10.0 10.0 0 2000 \$ 200 200 300 NOO 400 600 700 900 900 20 50 Relative Difference (C SIM vs C) 0.0008 0.0006 Relative Difference (%) 0.0004 0.0002 0.0000 -0.0002 -0.000430 20 SO 200 200 300 NOO 400 600 100 900 900 Requested Throughput (Mb/s)