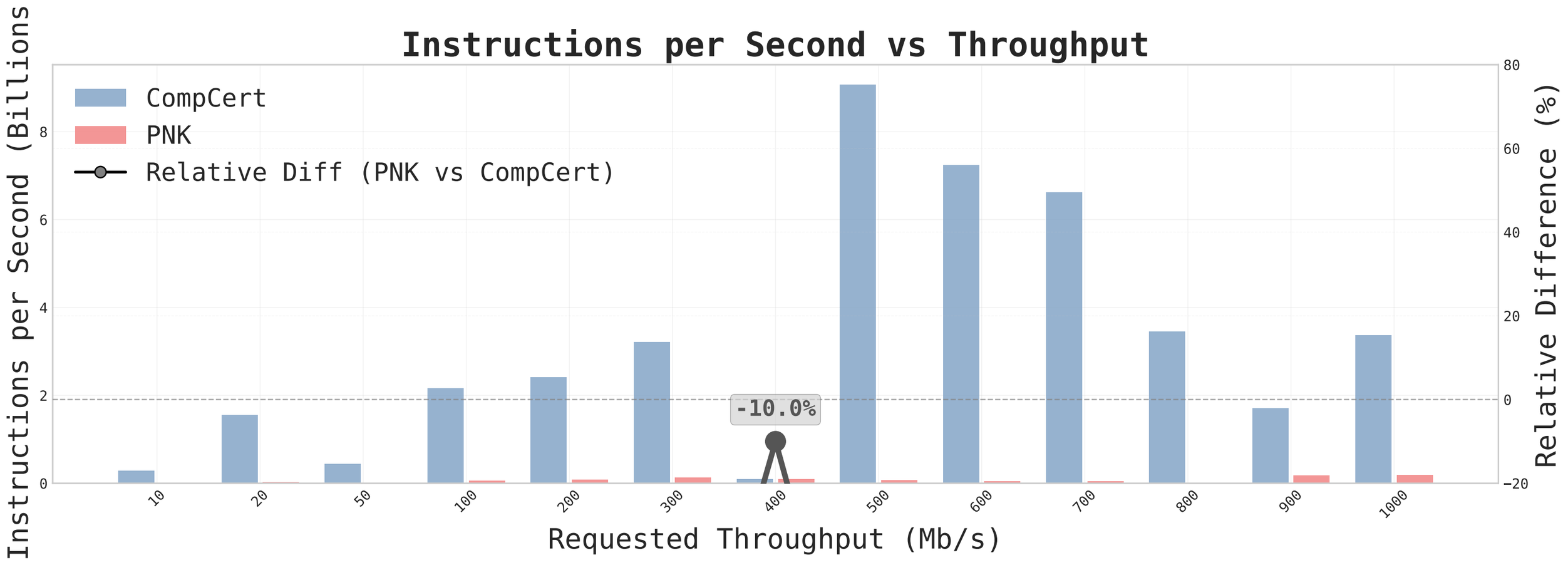
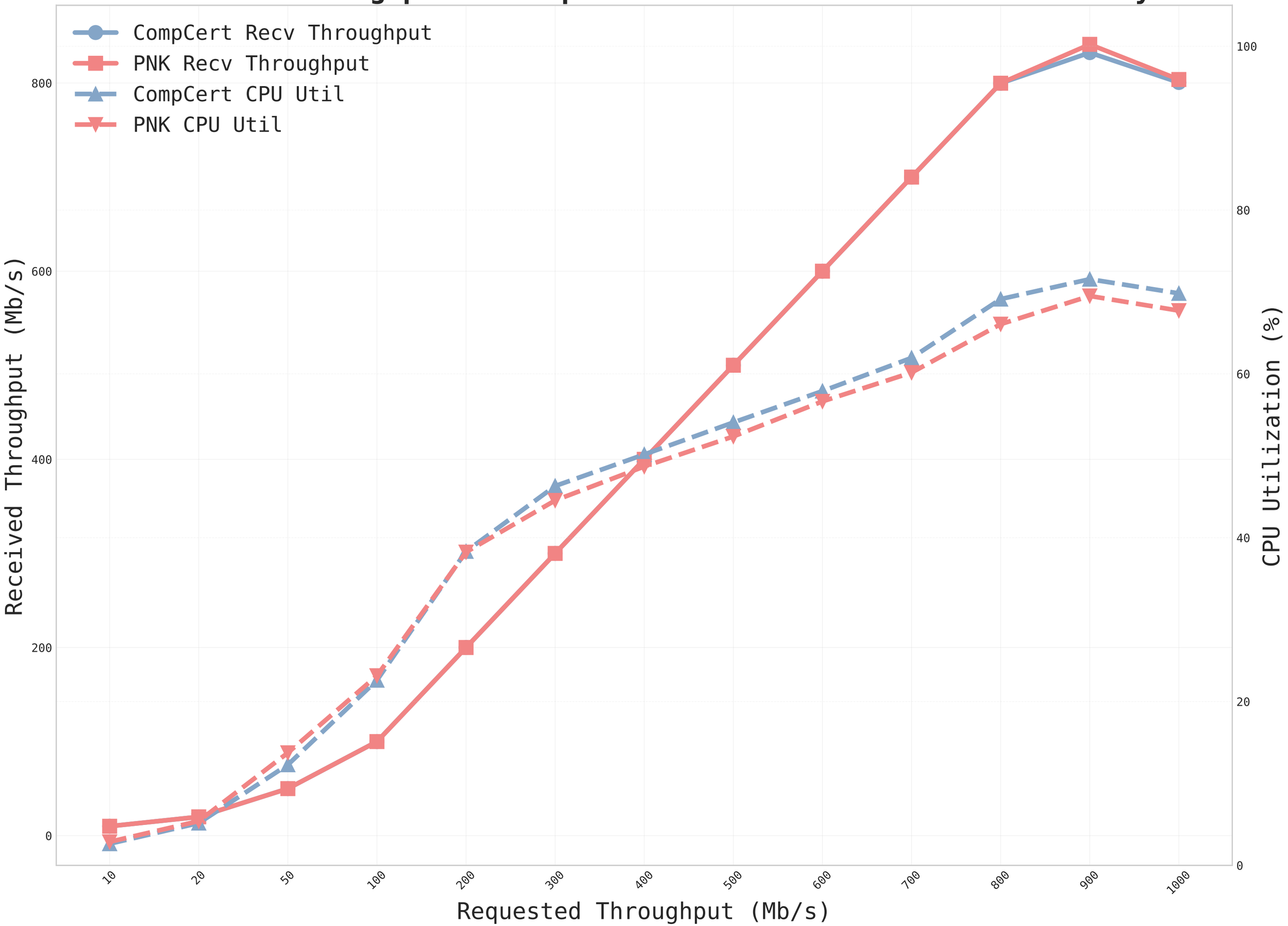
Instructions per Second vs Throughput



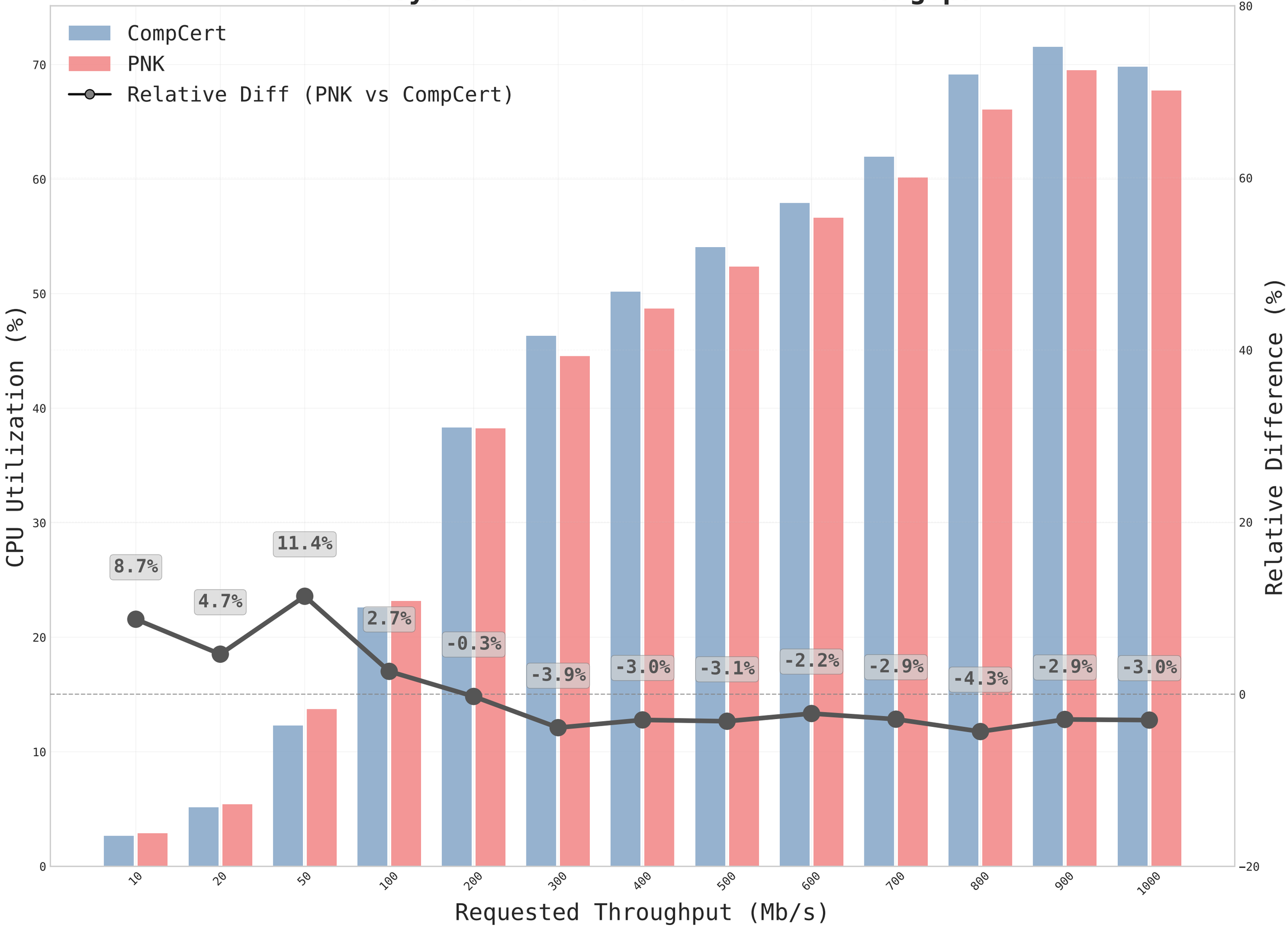
-100.0% -98.1% -97.7% -97.2% -96.7% -96.0%

-99.2% -99.3% -99.4% -99.7% -89.5% -94.4%

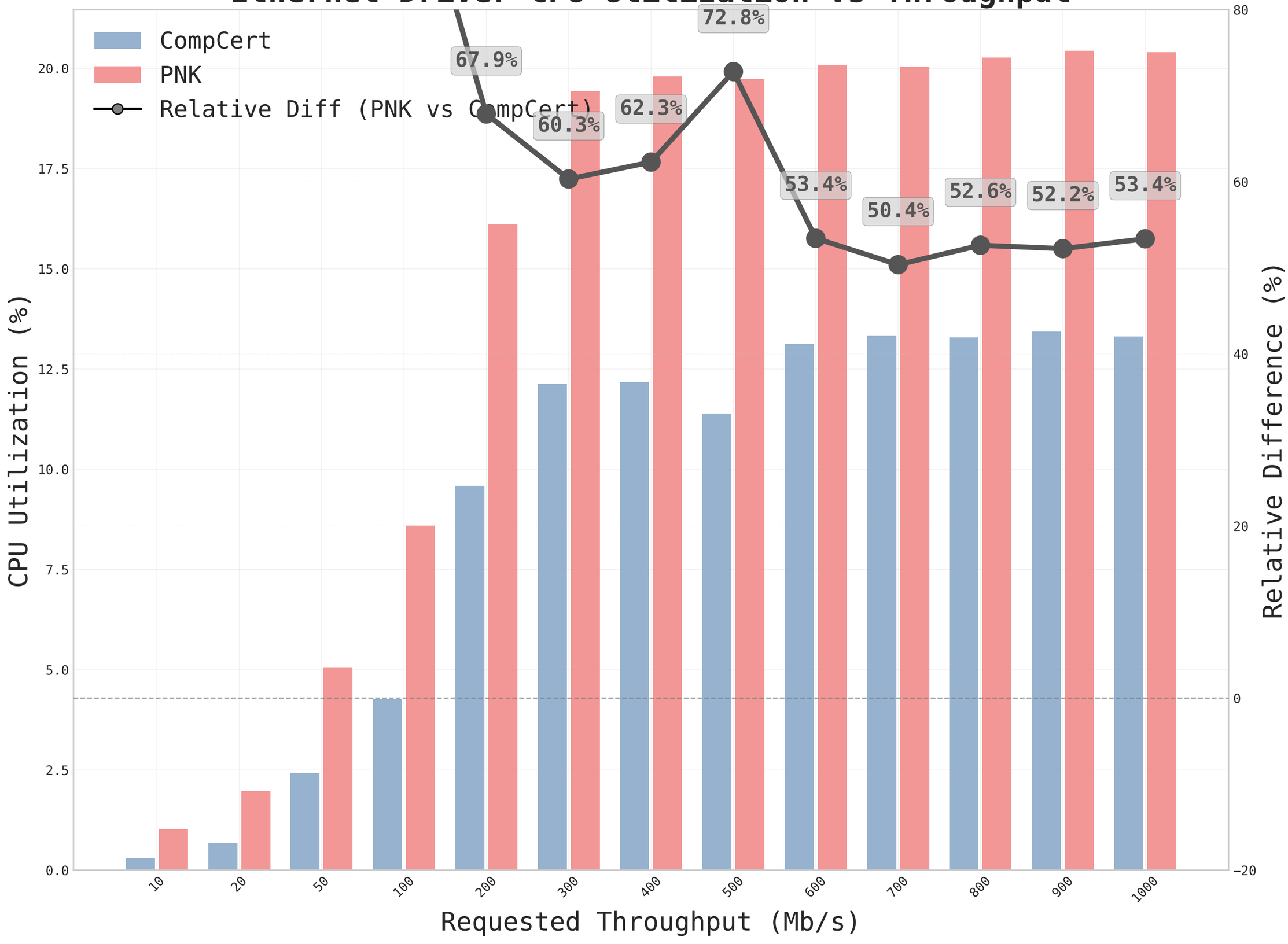
Received Throughput vs Requested with CPU Utilization Overlay



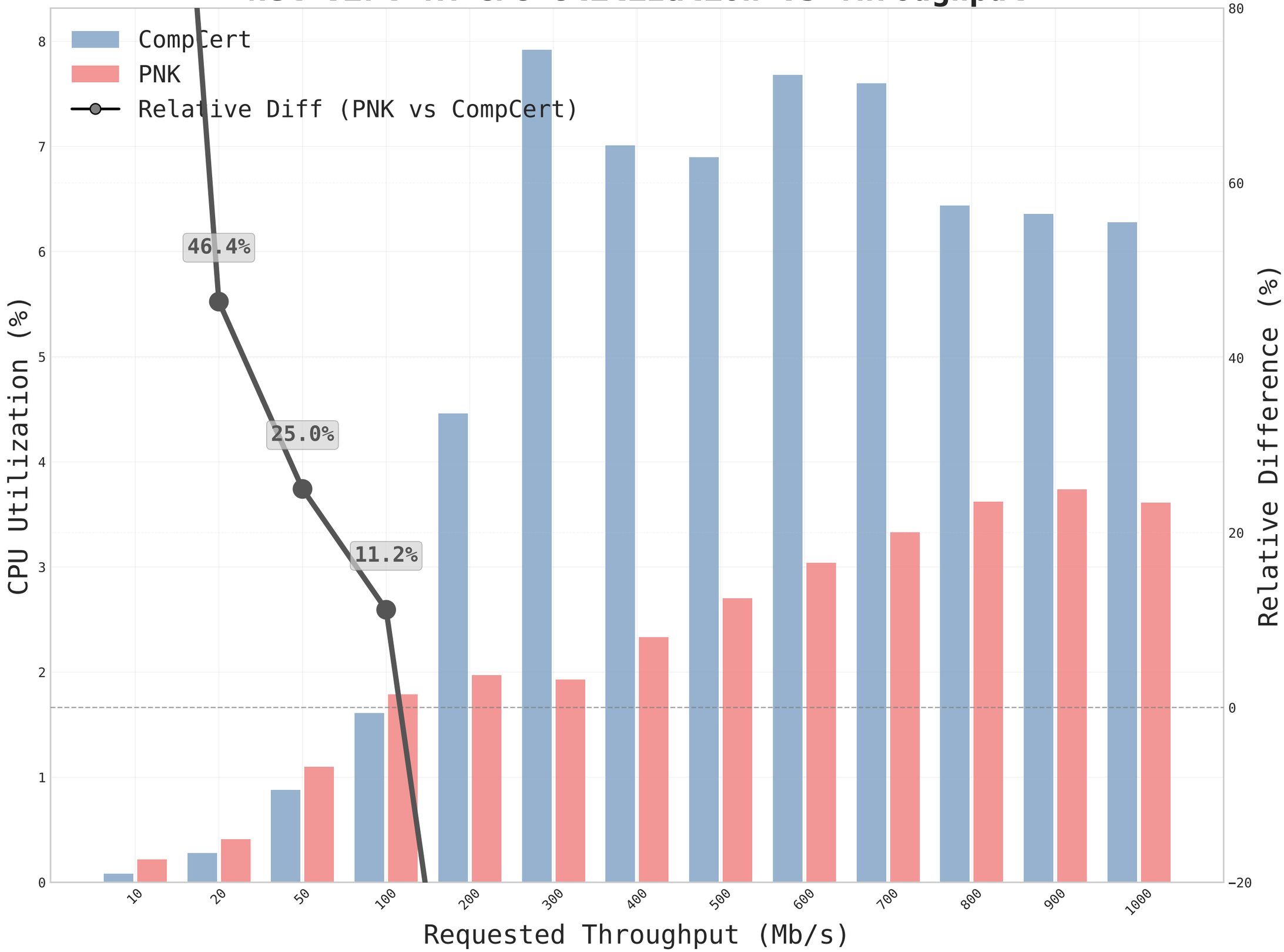
Total System CPU Utilization vs Throughput



Ethernet Driver CPU Utilization vs Throughput

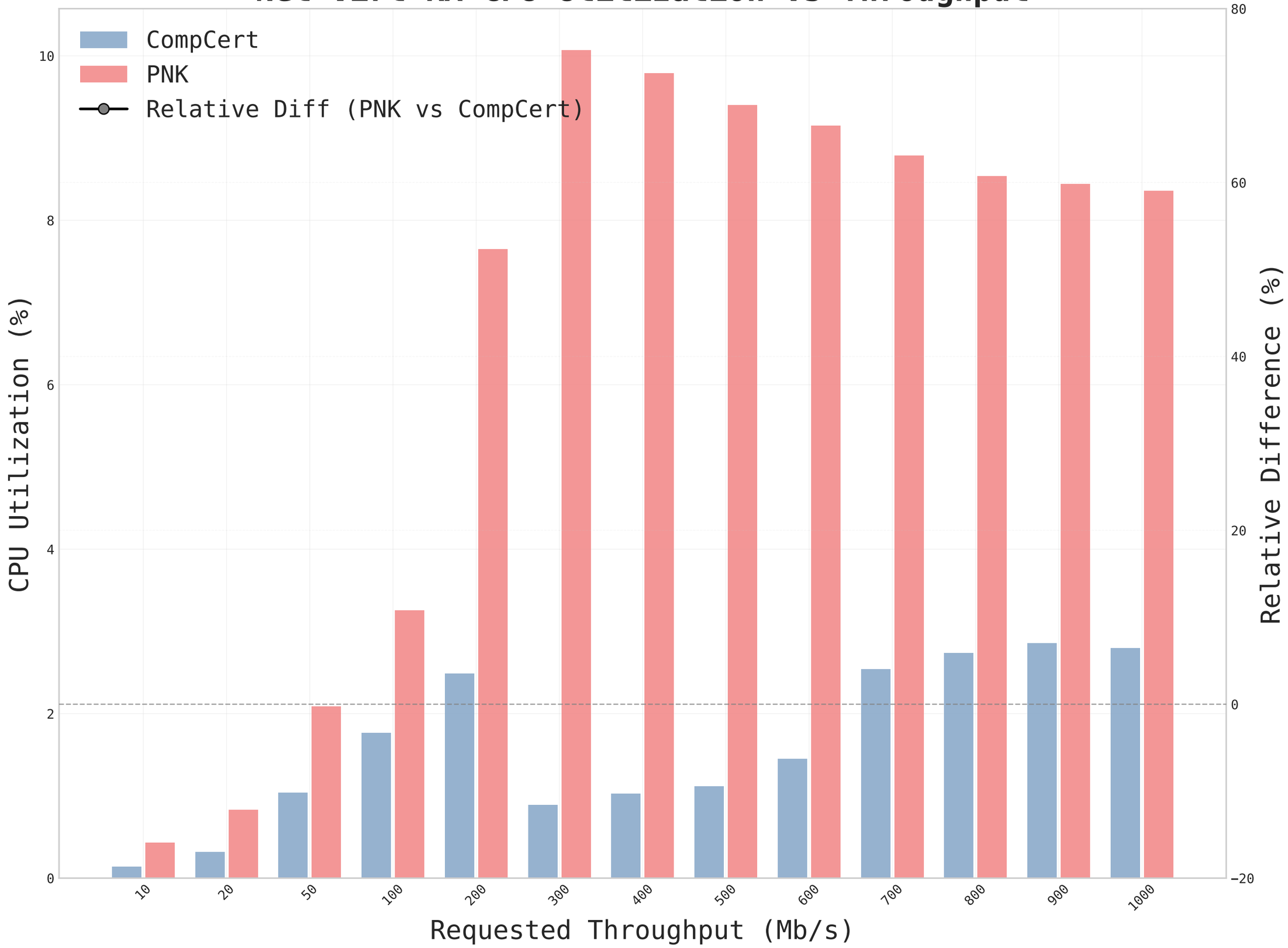


Net Virt TX CPU Utilization vs Throughput

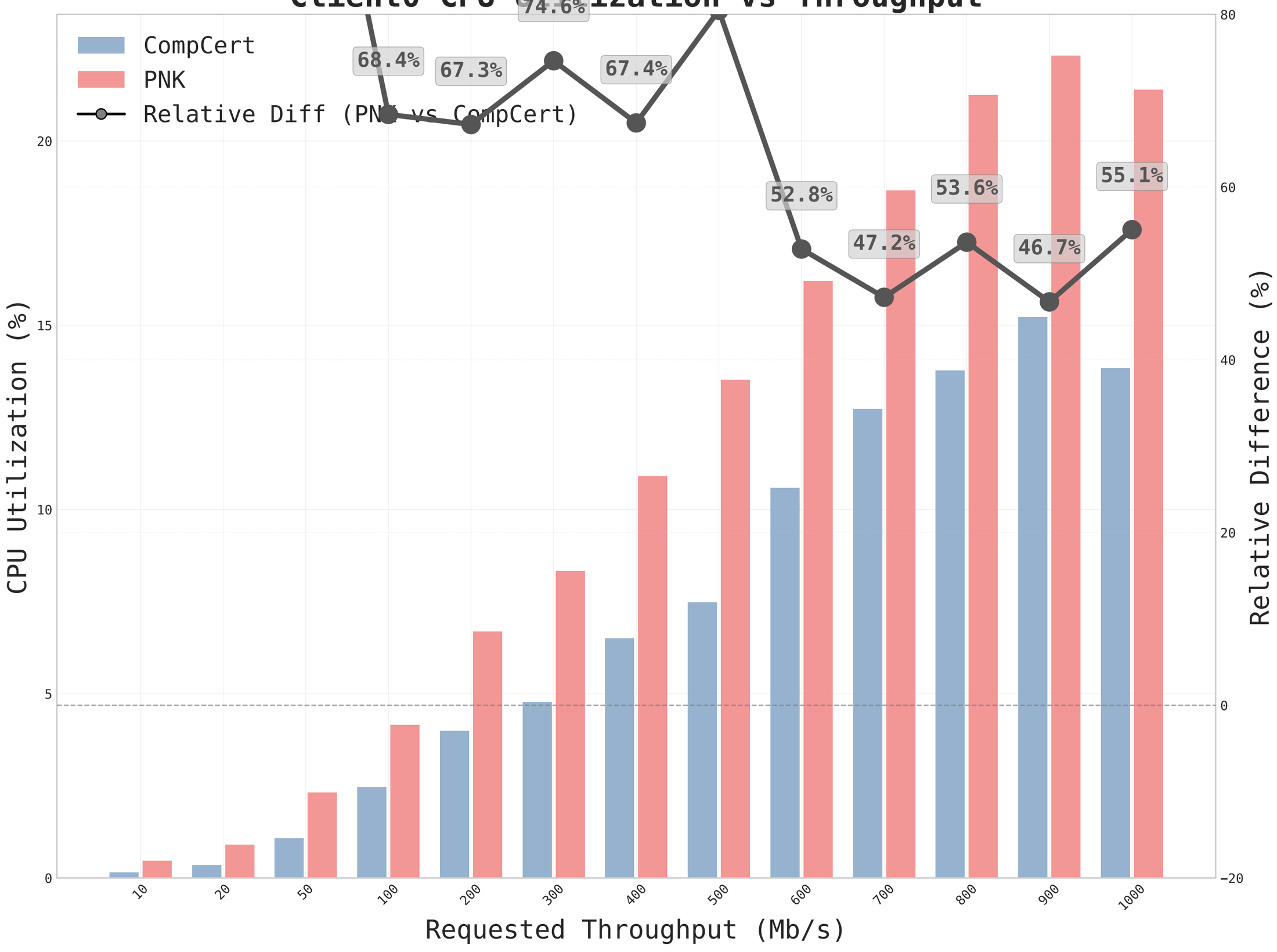


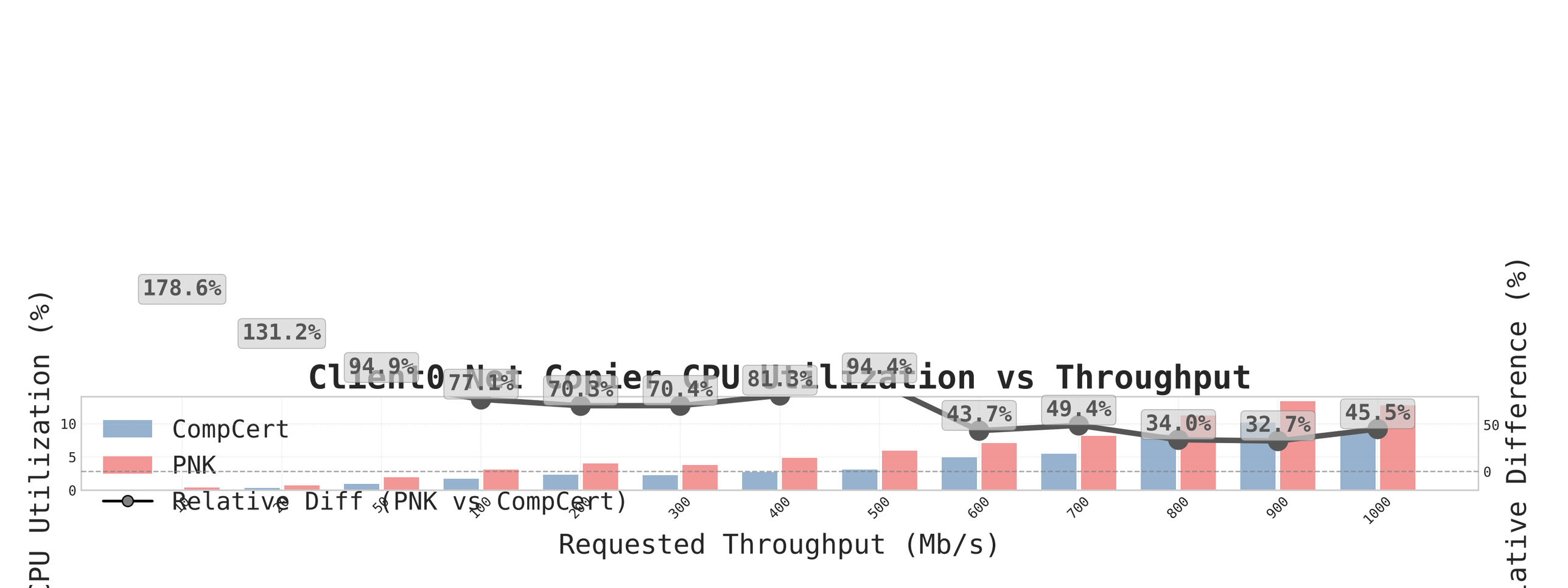
84.2%

Net Virt RX CPU Utilization vs Throughput

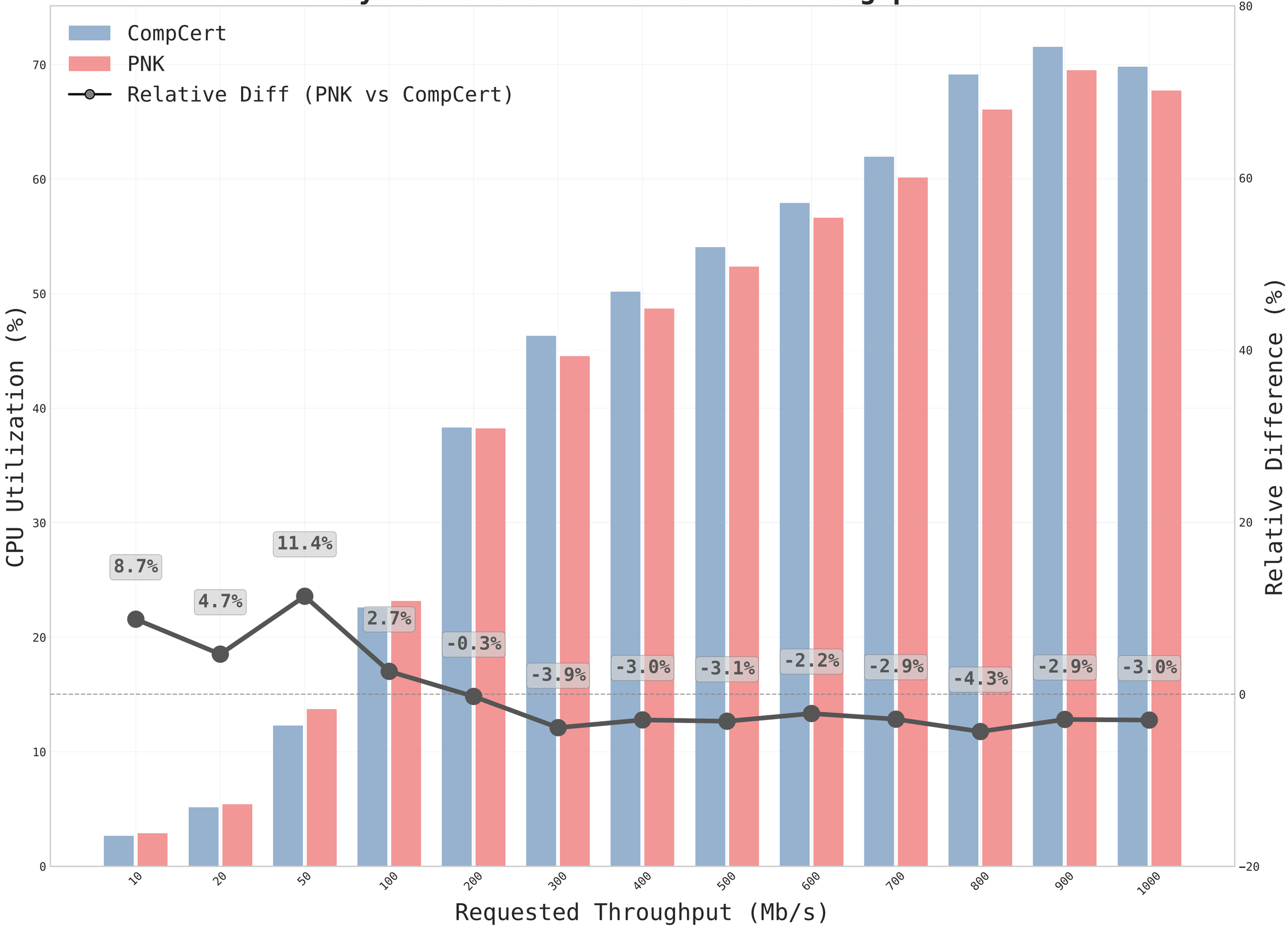


Client0 CPU Utilization vs Throughput

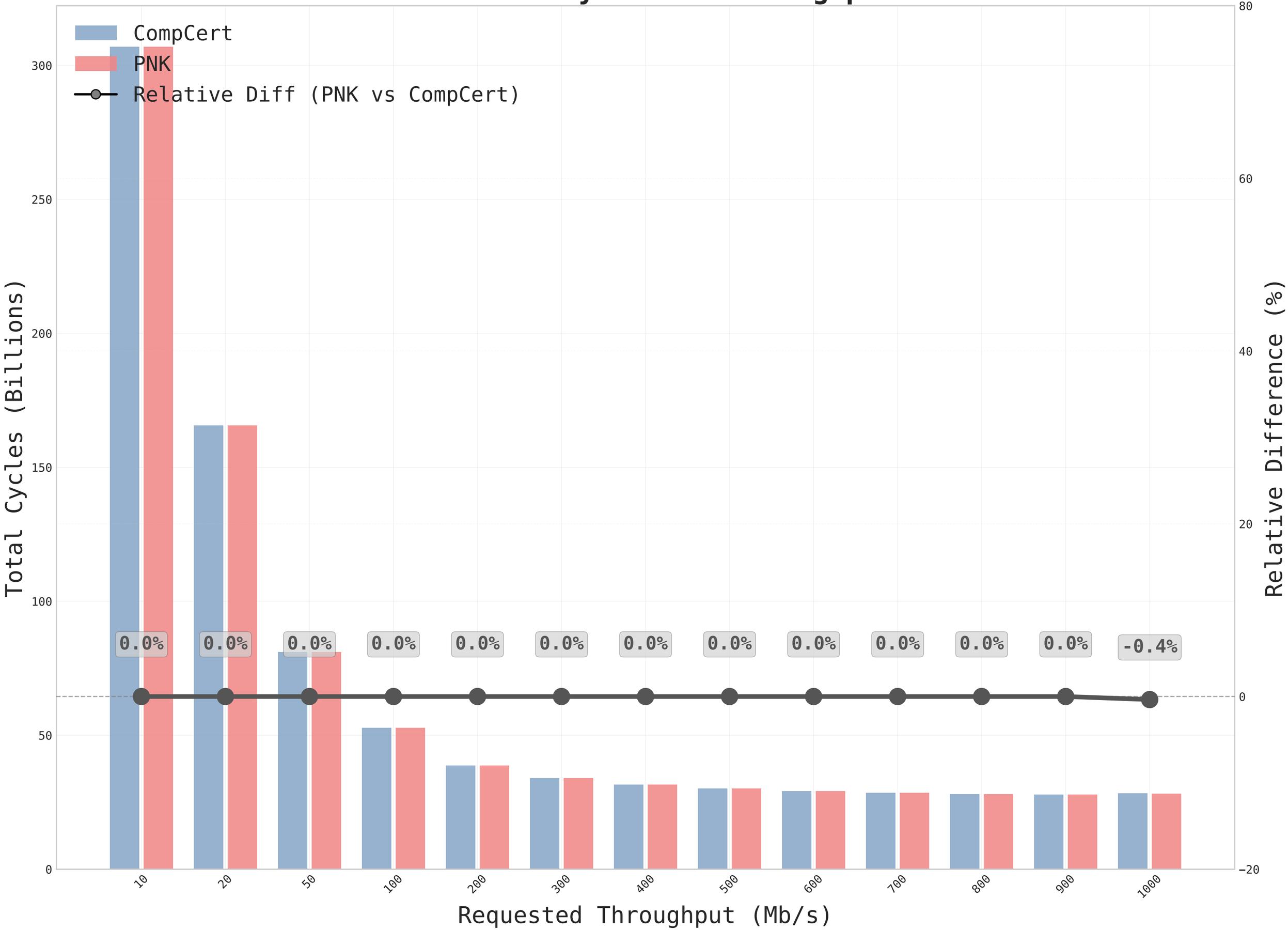


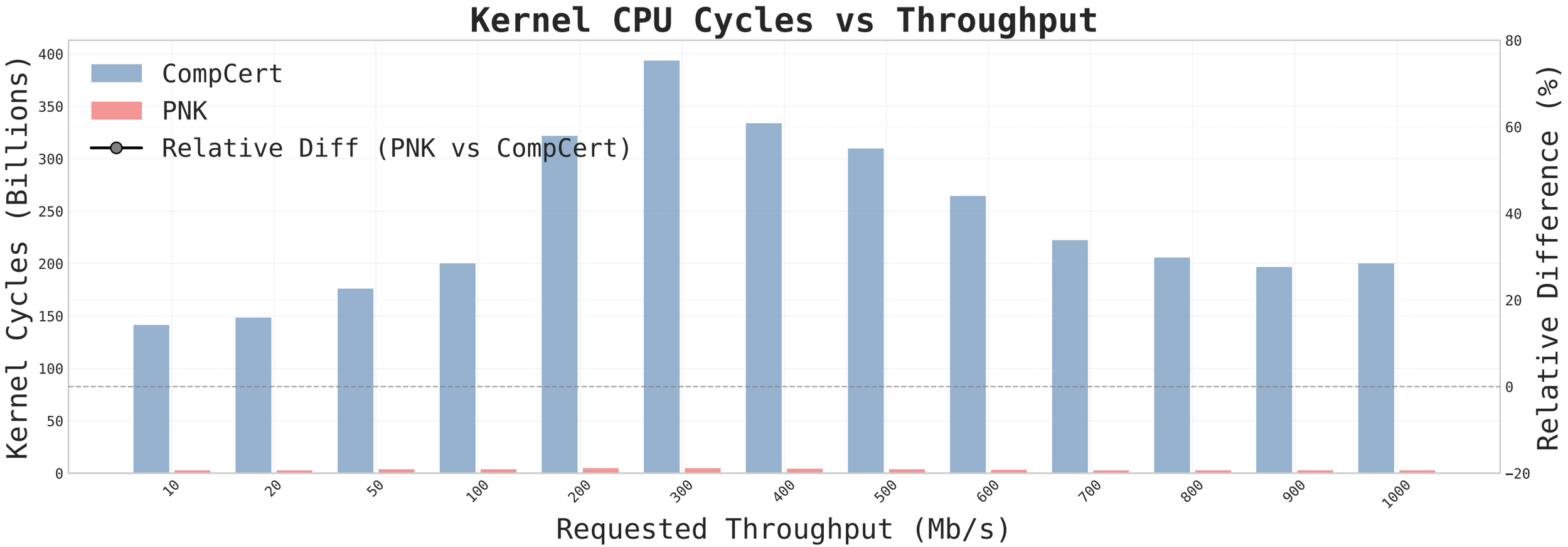

Client0 Net Copier CPU Utilization vs Throughput
CompCert
PNK
Relative Diff (PNK vs CompCert)
CPU Utilization (%)
Relative Difference (%)
Requested Throughput (Mb/s)
178.6%
131.2%
94.9%
77.1%
70.3%
70.4%
81.3%
94.4%
43.7%
49.4%
34.0%
32.7%
45.5%
10
5
0
50
0
1
2
5
10
20
50
100
200
300
400
500
600
700
800
900
1000

System CPU Utilization vs Throughput

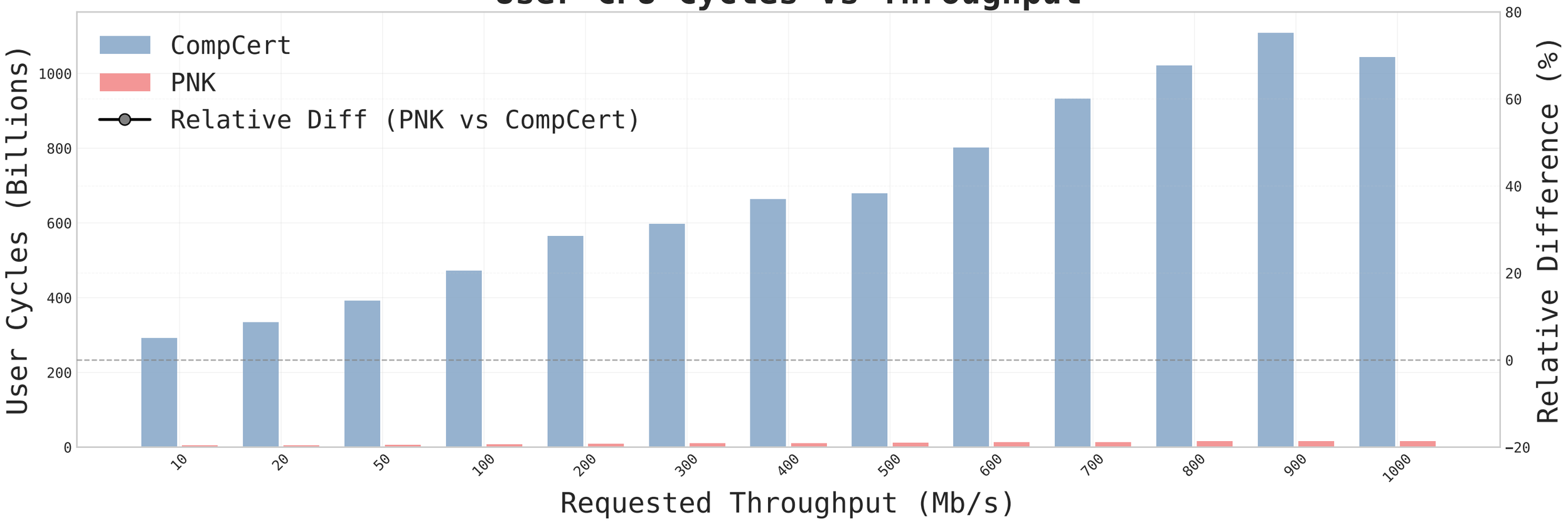


Total CPU Cycles vs Throughput



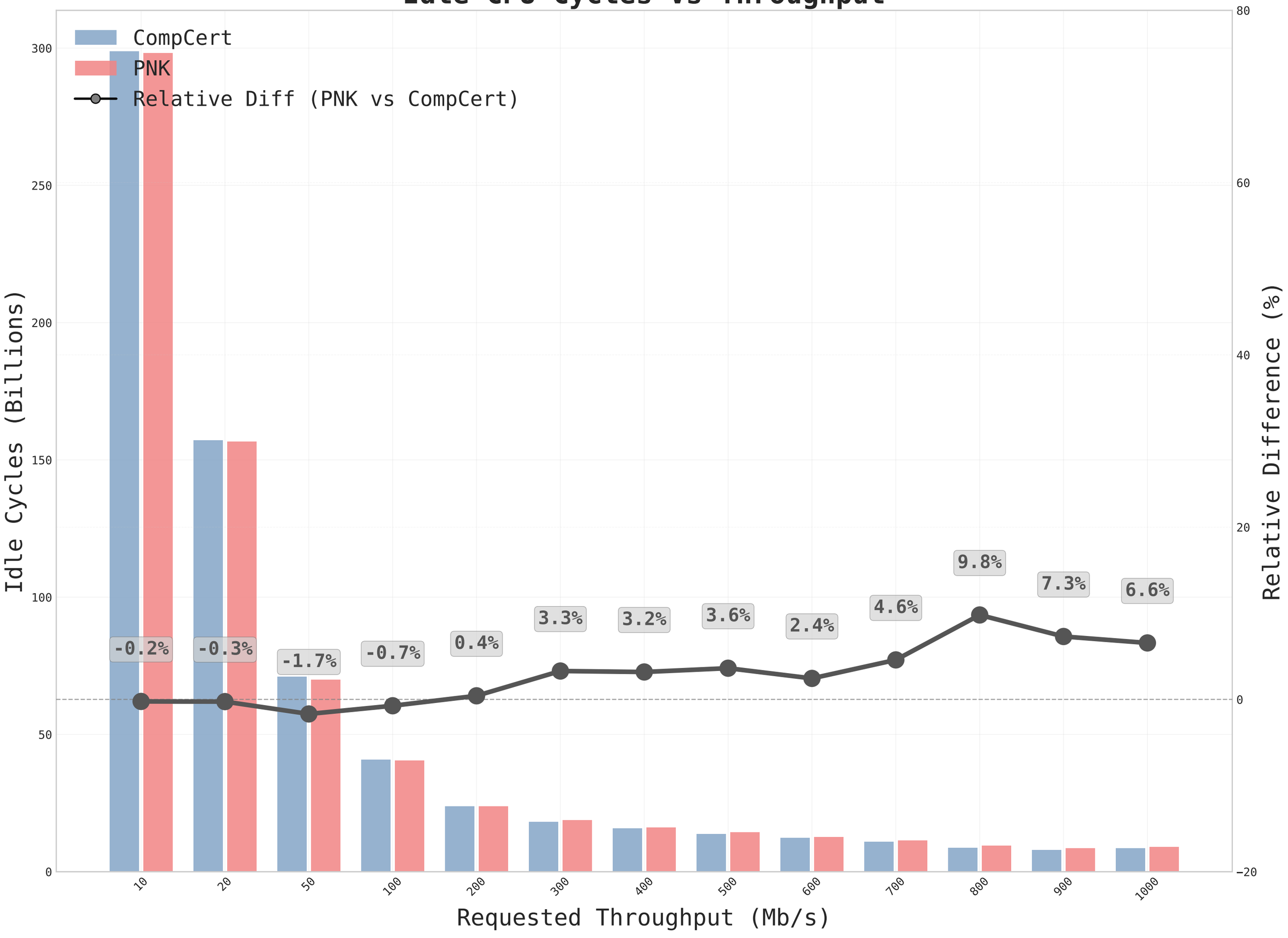


-98.1%	-98.1%	-98.0%	-98.2%	-98.5%	-98.7%	-98.7%	-98.8%	-98.7%	-98.7%	-98.7%	-98.7%	-98.7%

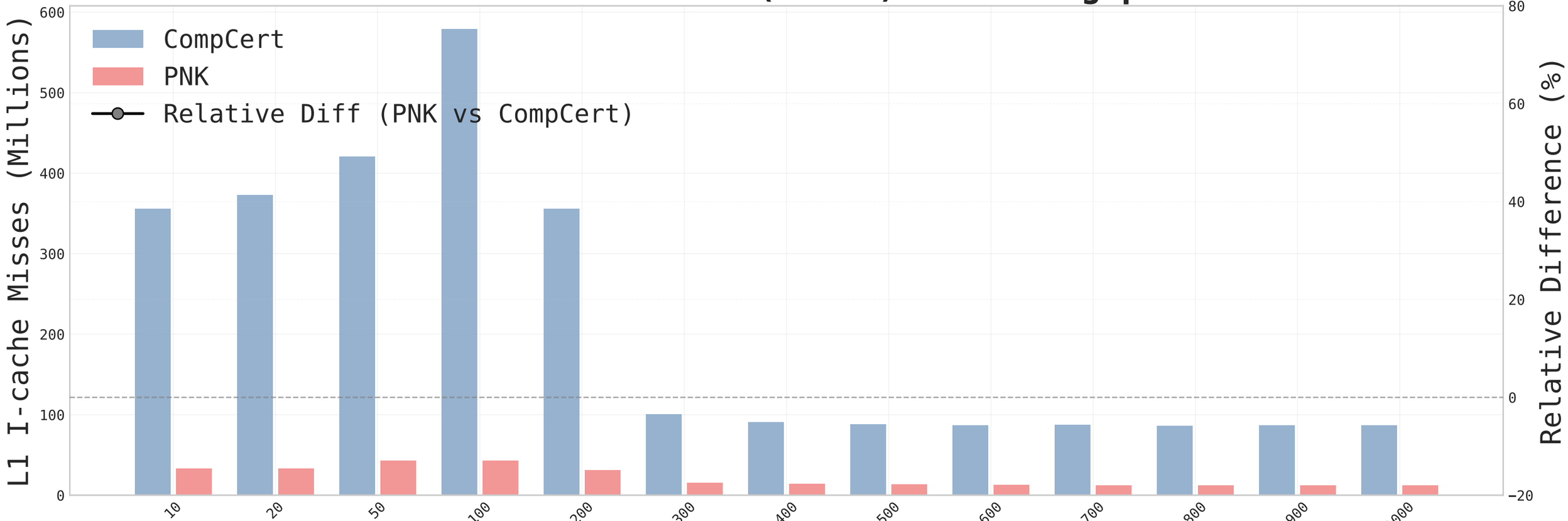


-98.2%	-98.4%	-98.3%	-98.4%	-98.4%	-98.3%	-98.4%	-98.3%	-98.4%	-98.5%	-98.5%	-98.5%	-98.4%

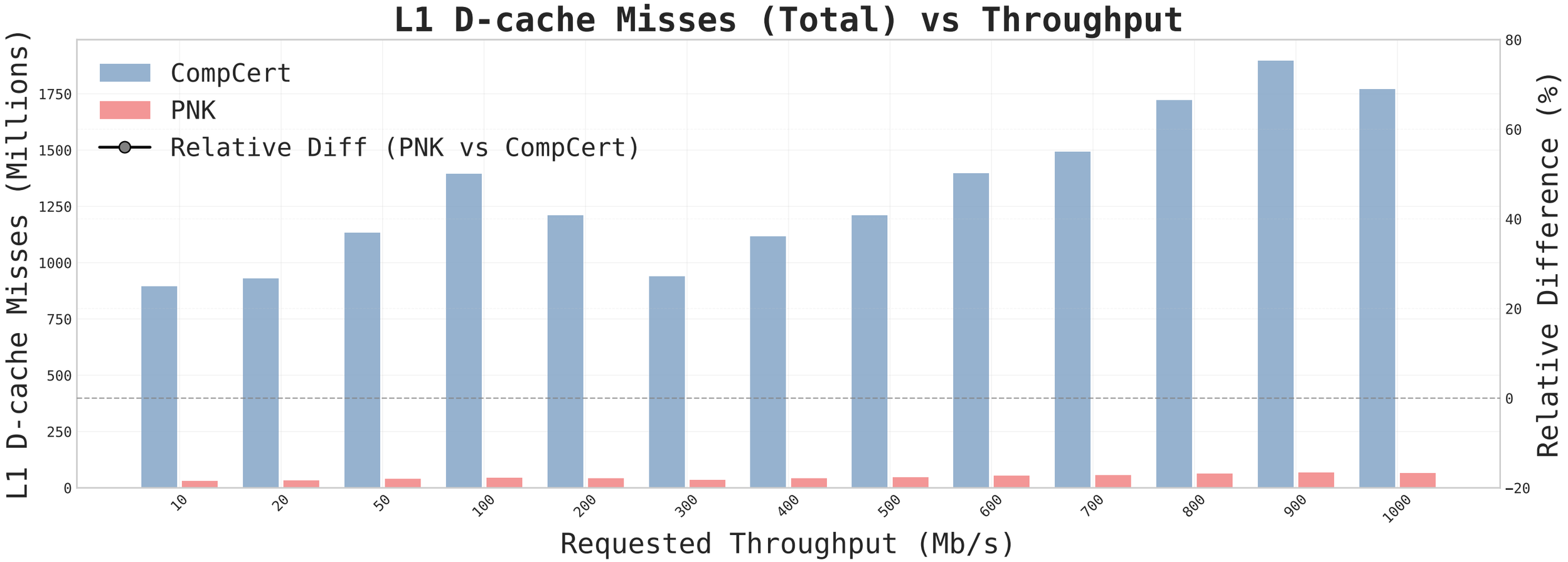
Idle CPU Cycles vs Throughput



L1 I-cache Misses (Total) vs Throughput

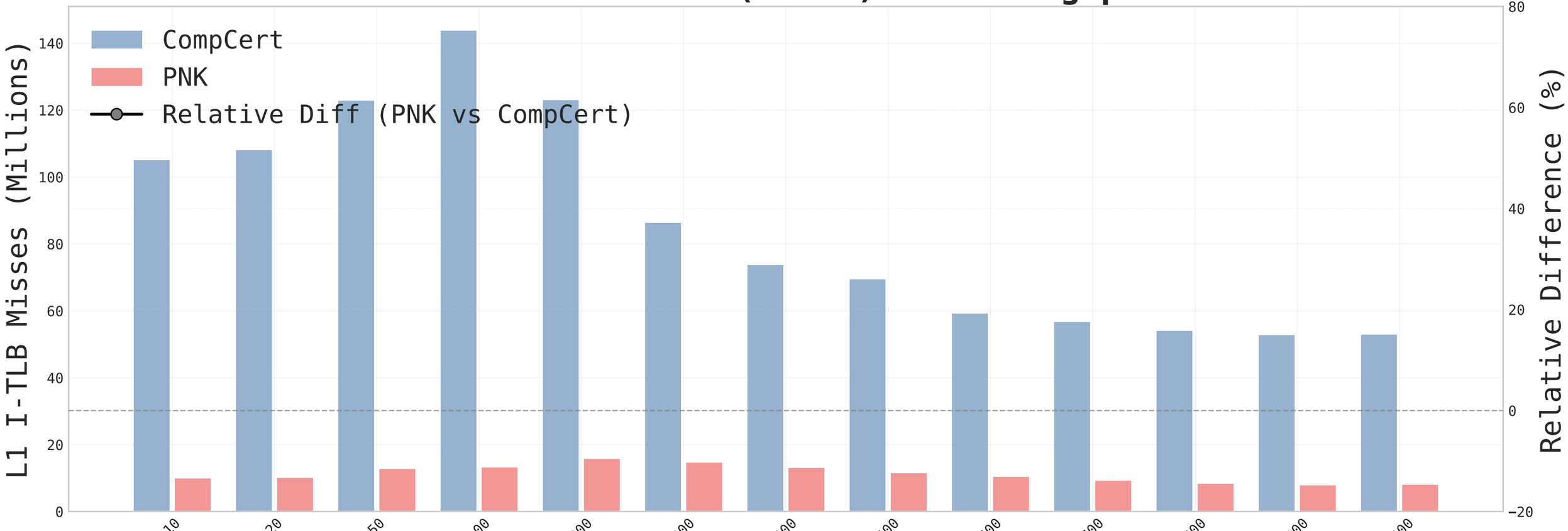


10	20	50	100	200	300	400	500	600	700	800	900	1000
-90.6%	-91.1%	-89.8%	-92.6%	-91.2%	-84.7%	-84.3%	-84.8%	-85.2%	-86.0%	-86.2%	-86.3%	-86.0%



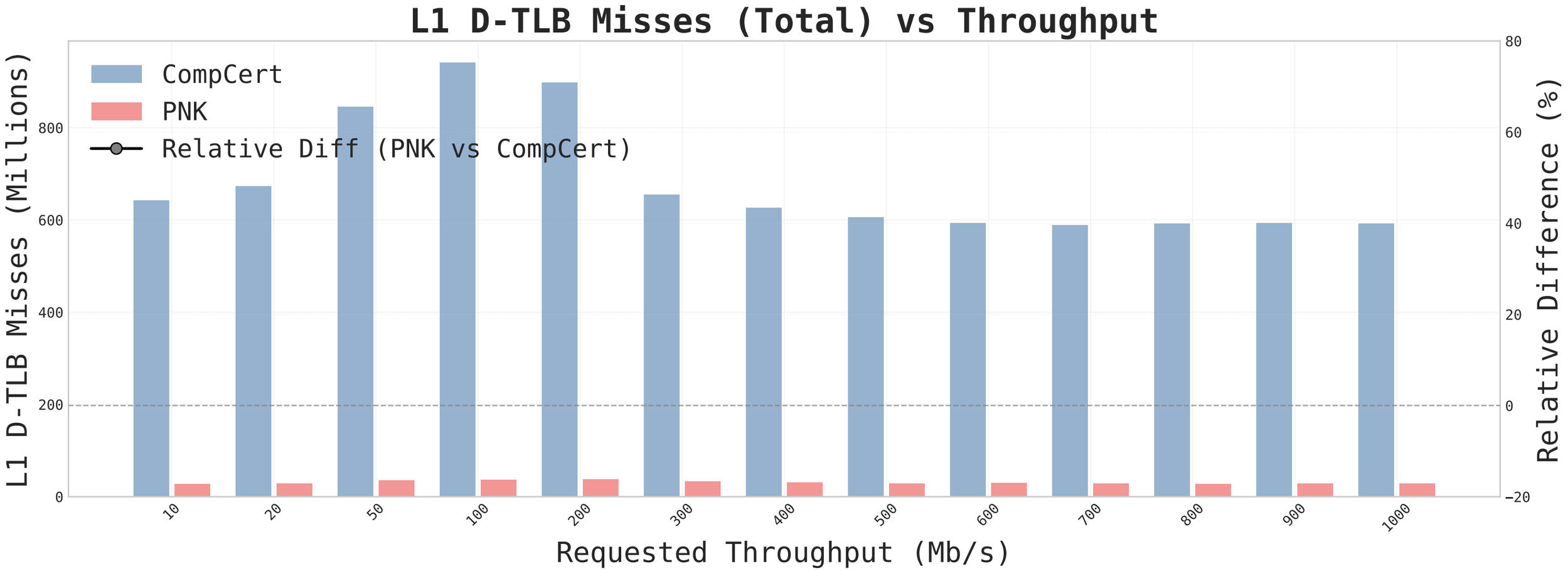
-96.5%	-96.6%	-96.5%	-96.9%	-96.6%	-96.2%	-96.3%	-96.1%	-96.2%	-96.2%	-96.3%	-96.5%	-96.3%

L1 I-TLB Misses (Total) vs Throughput



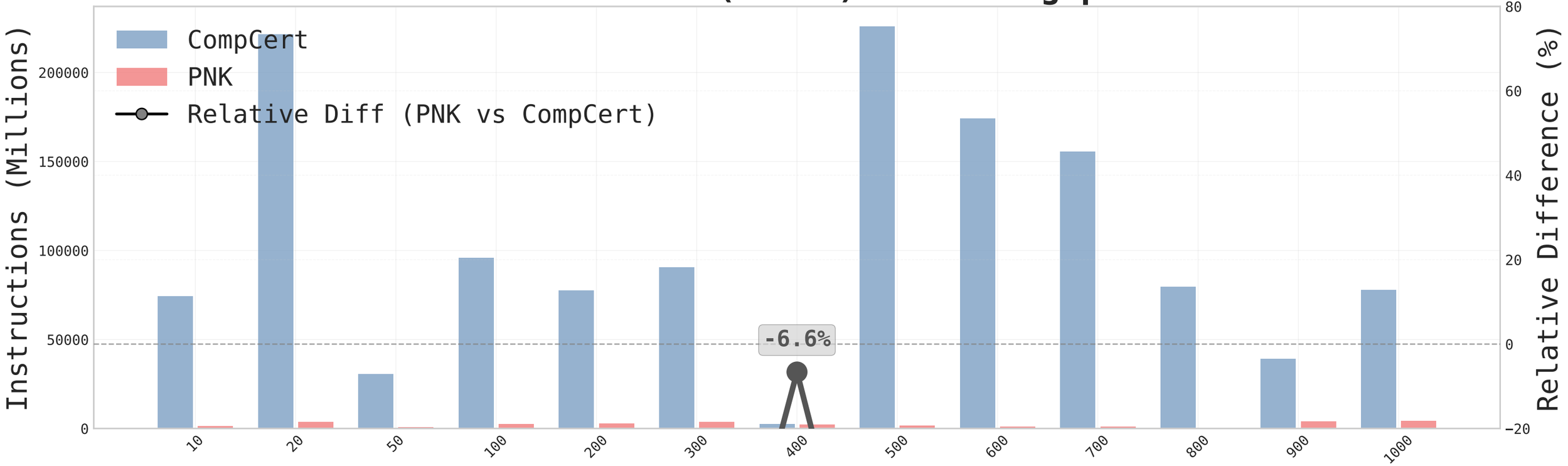
Requested Throughput (Mb/s)

10	20	50	100	200	300	400	500	600	700	800	900	1000
-90.6%	-90.8%	-89.7%	-90.9%	-87.3%	-83.1%	-82.5%	-83.6%	-82.6%	-83.8%	-84.7%	-85.4%	-85.1%

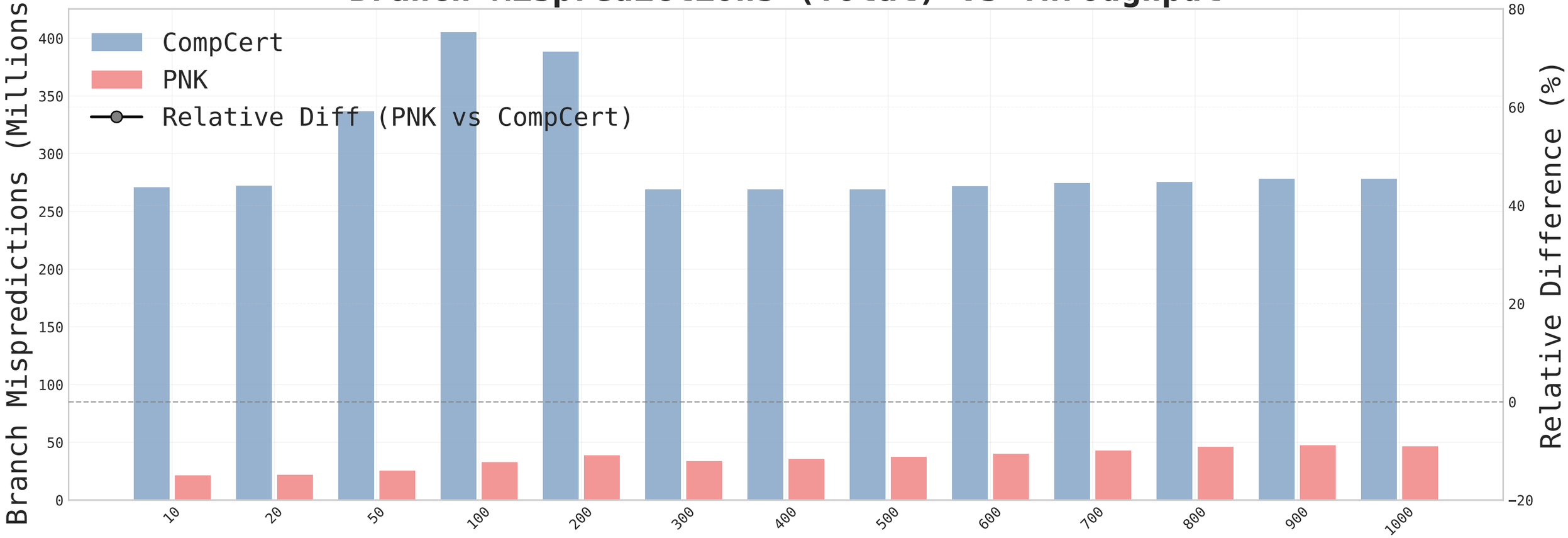


10	20	50	100	200	300	400	500	600	700	800	900	1000
-95.7%	-95.8%	-95.8%	-96.1%	-95.8%	-95.0%	-95.1%	-95.3%	-95.1%	-95.1%	-95.3%	-95.3%	-95.1%

Instructions (Total) vs Throughput

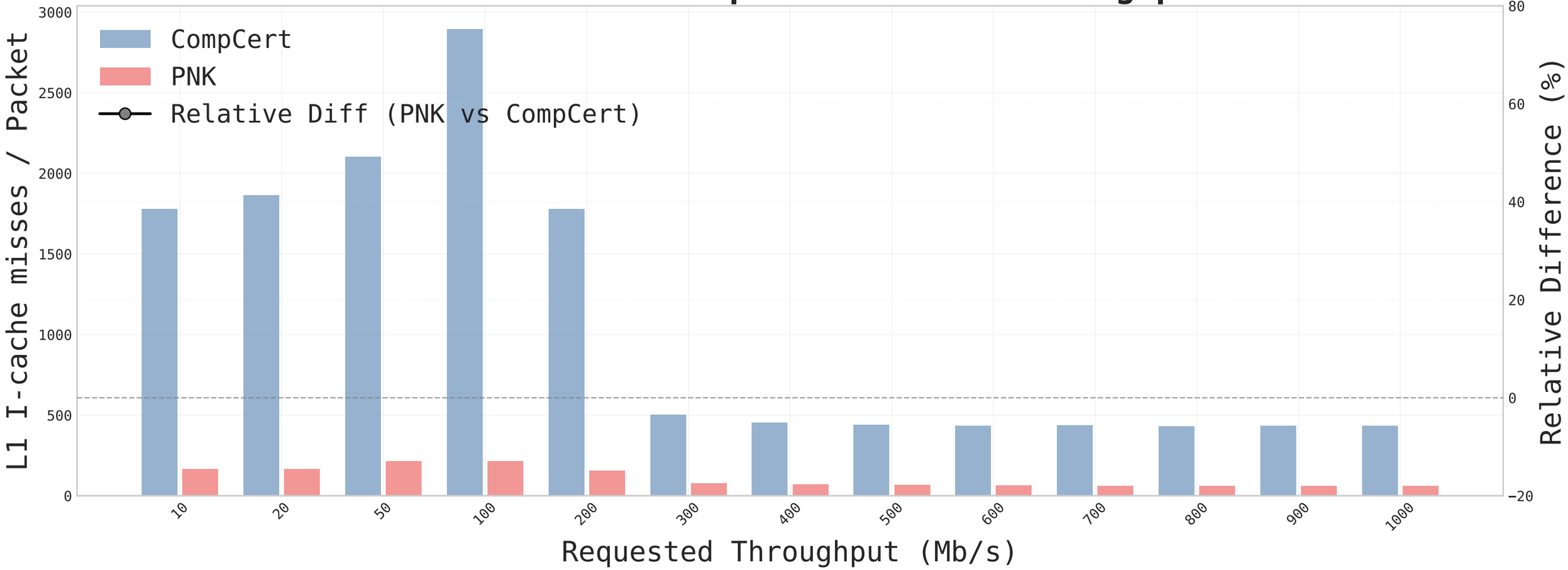


Branch Mispredictions (Total) vs Throughput

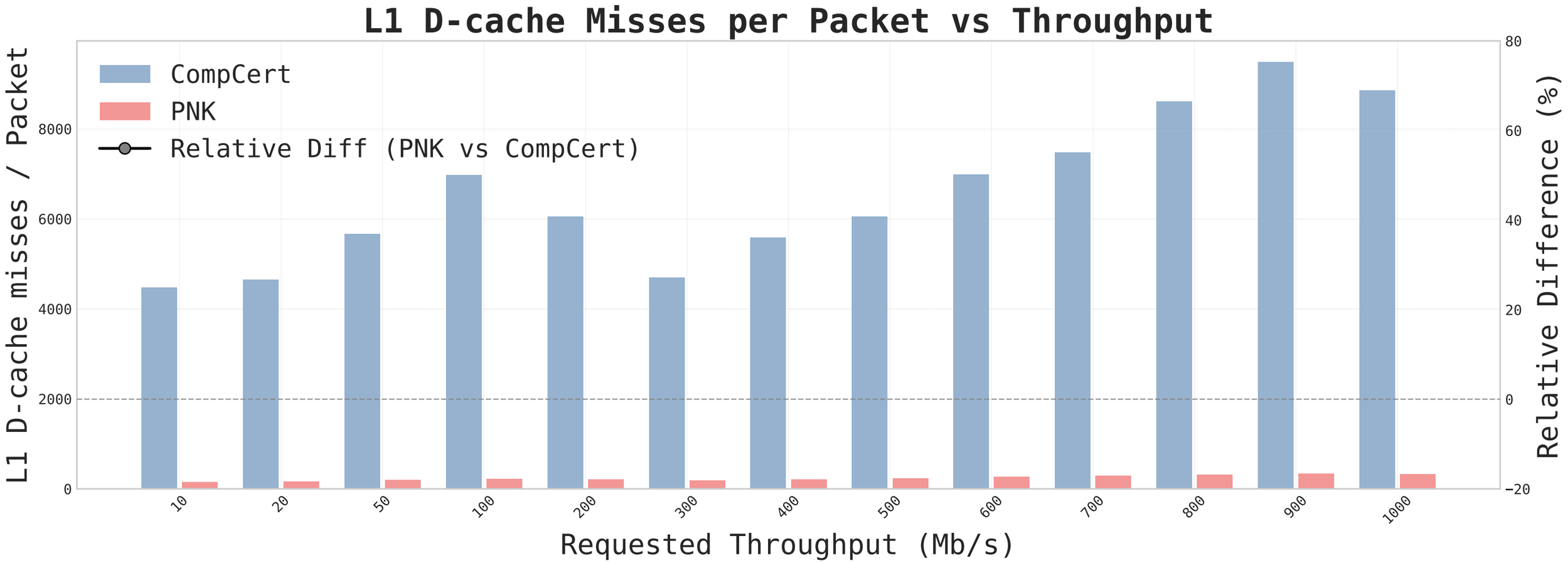


-92.2% -92.0% -92.5% -92.0% -90.0% -87.6% -86.9% -86.1% -85.3% -84.4% -83.4% -83.0% -83.2%

L1 I-cache Misses per Packet vs Throughput

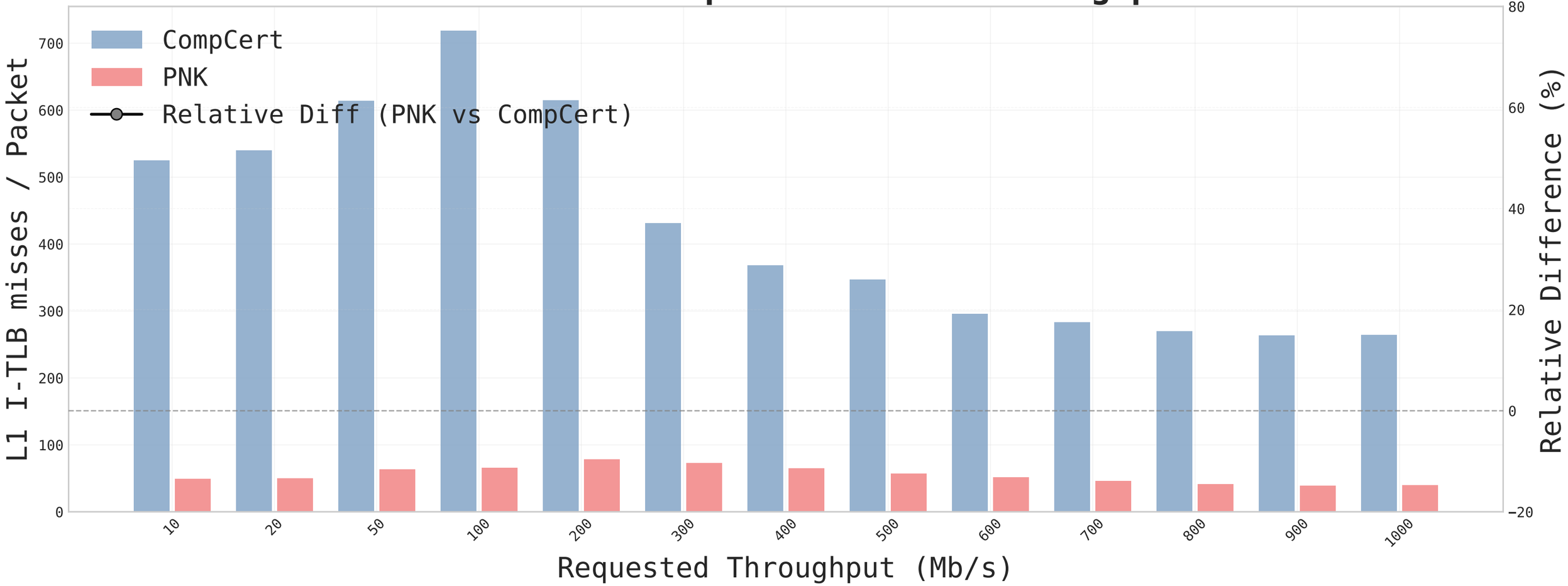


-90.6% -91.1% -89.8% -92.6% -91.2% -84.7% -84.3% -84.8% -85.2% -86.0% -86.2% -86.3% -86.0%

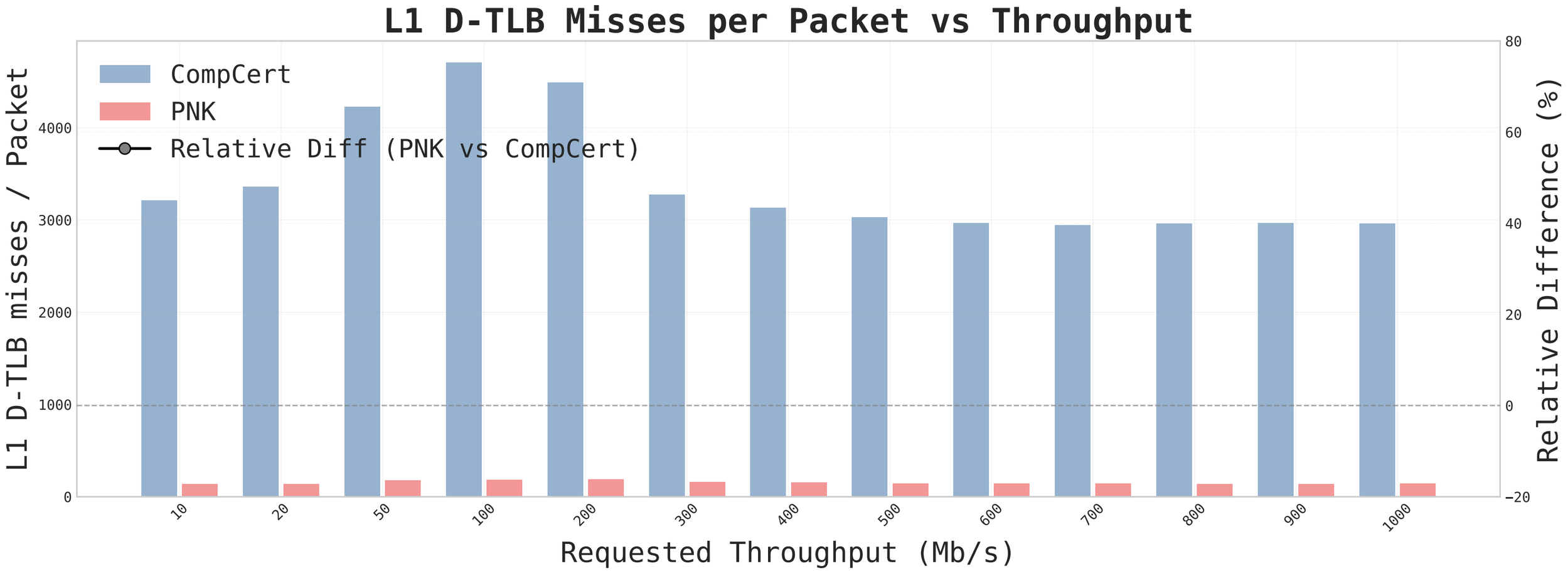


-96.5%	-96.6%	-96.5%	-96.9%	-96.6%	-96.2%	-96.3%	-96.1%	-96.2%	-96.2%	-96.3%	-96.5%	-96.3%

L1 I-TLB Misses per Packet vs Throughput

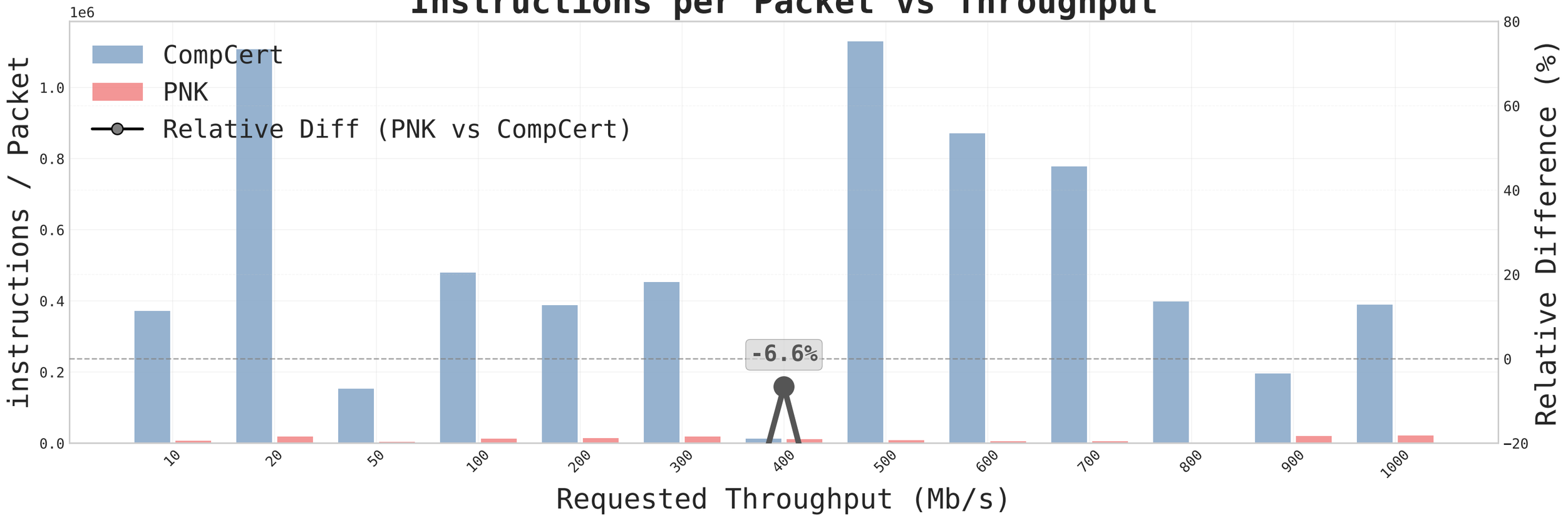


10	20	50	100	200	300	400	500	600	700	800	900	1000
-90.6%	-90.8%	-89.7%	-90.9%	-87.3%	-83.1%	-82.4%	-83.5%	-82.5%	-83.7%	-84.7%	-85.4%	-85.1%



10	20	50	100	200	300	400	500	600	700	800	900	1000
-95.7%	-95.8%	-95.8%	-96.1%	-95.8%	-95.0%	-95.1%	-95.3%	-95.1%	-95.1%	-95.3%	-95.3%	-95.1%

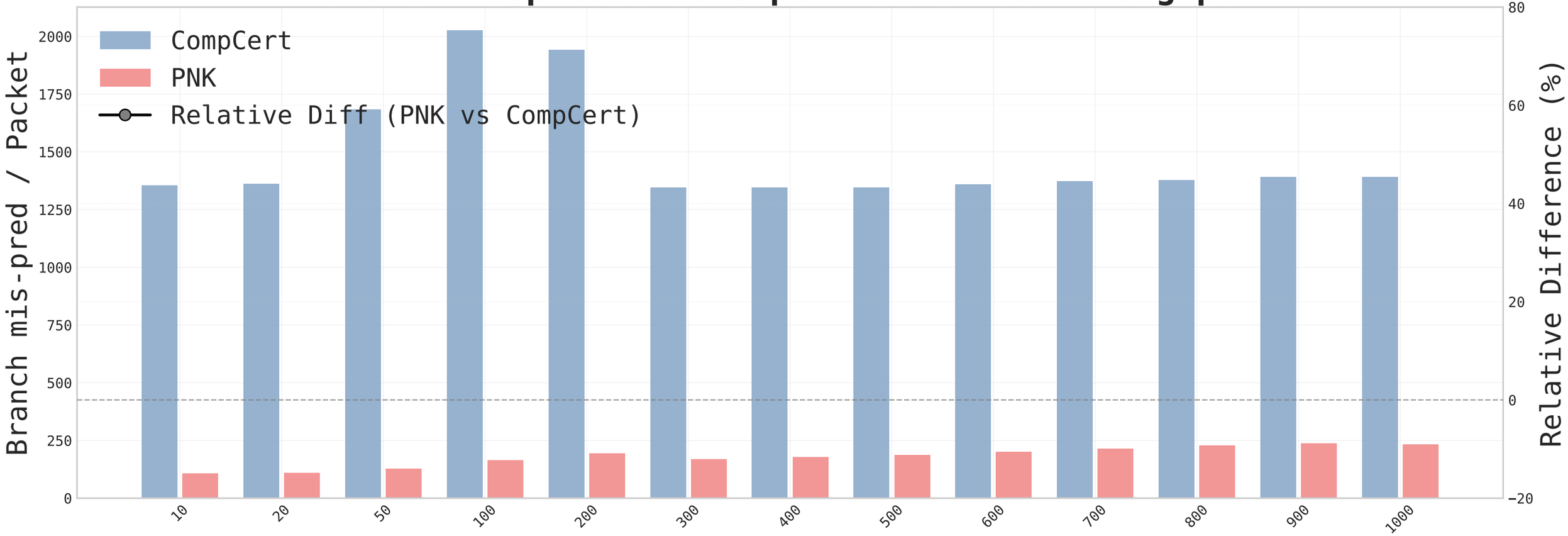
Instructions per Packet vs Throughput



-98.3% -98.3% -97.9% -97.4% -96.5% -95.9%

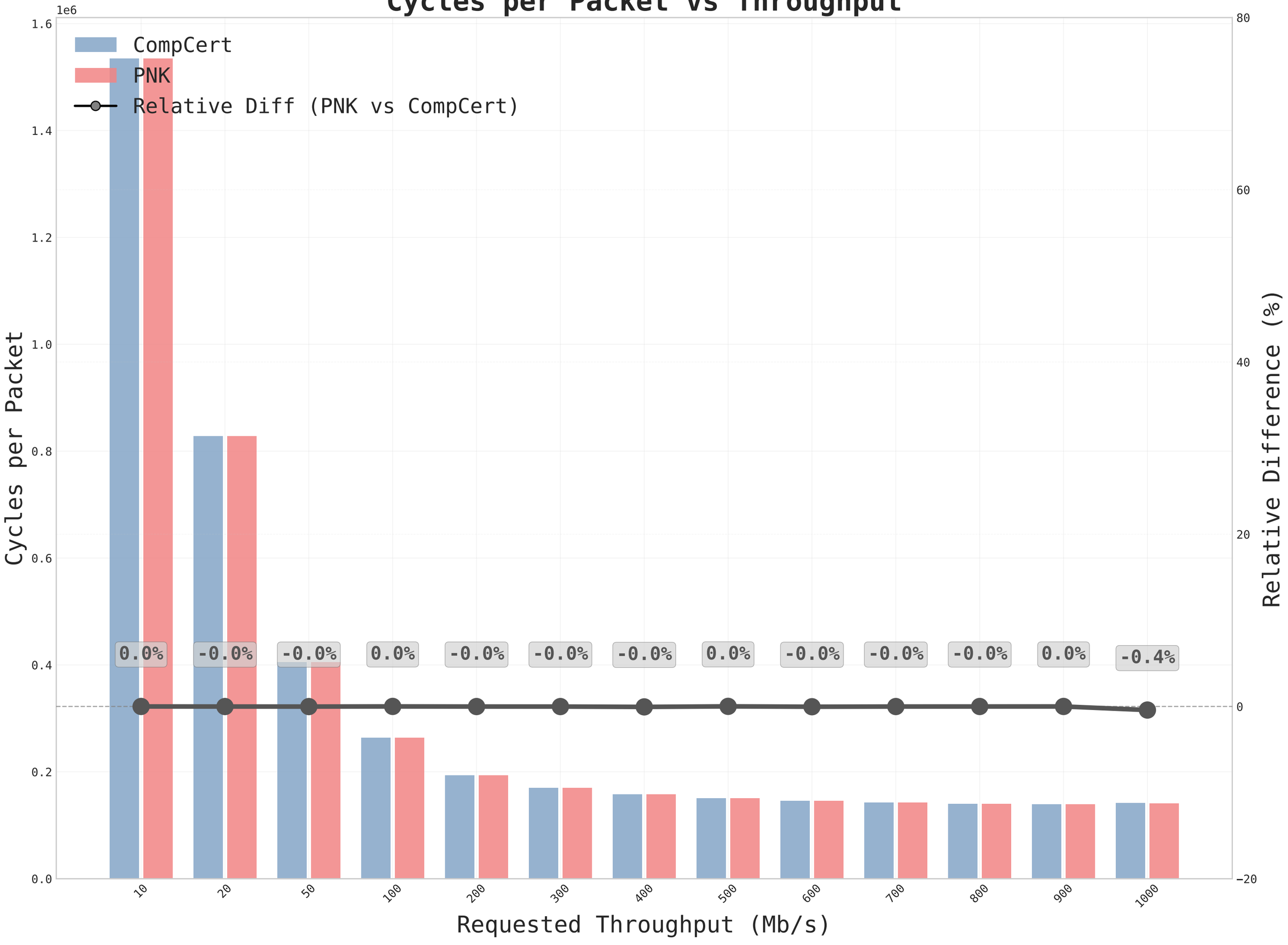
-99.3% -99.4% -99.4% -99.7% -89.6% -94.5%

Branch Mispredictions per Packet vs Throughput

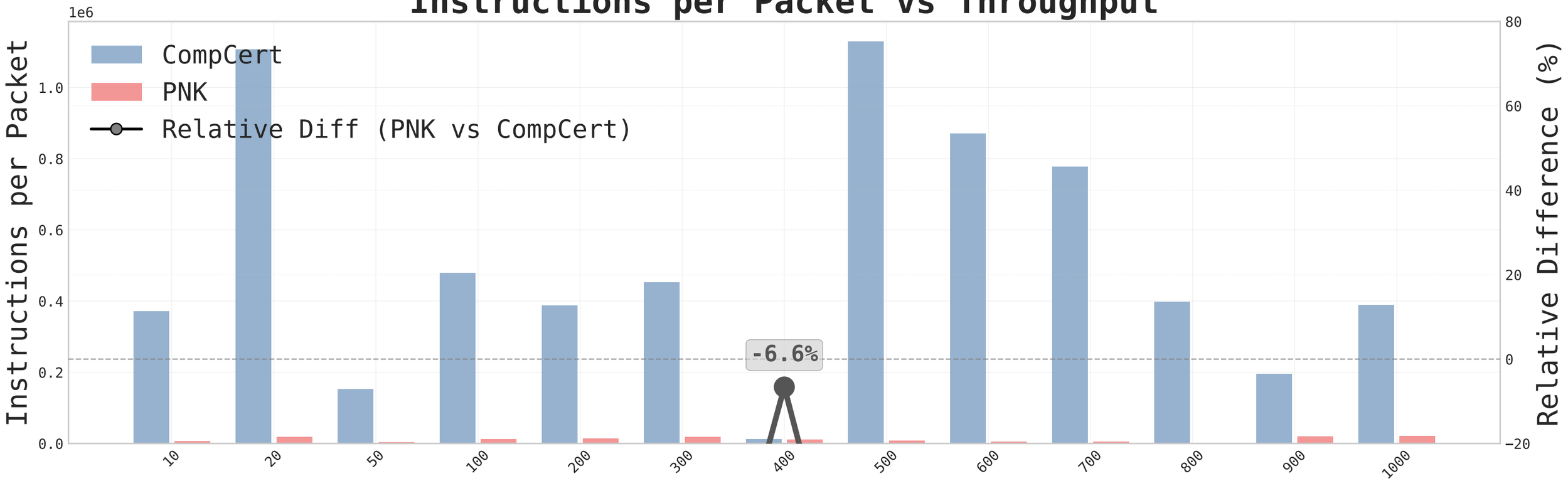


-92.2% -91.9% -92.5% -92.0% -90.0% -87.6% -86.9% -86.1% -85.3% -84.4% -83.4% -83.0% -83.2%

Cycles per Packet vs Throughput



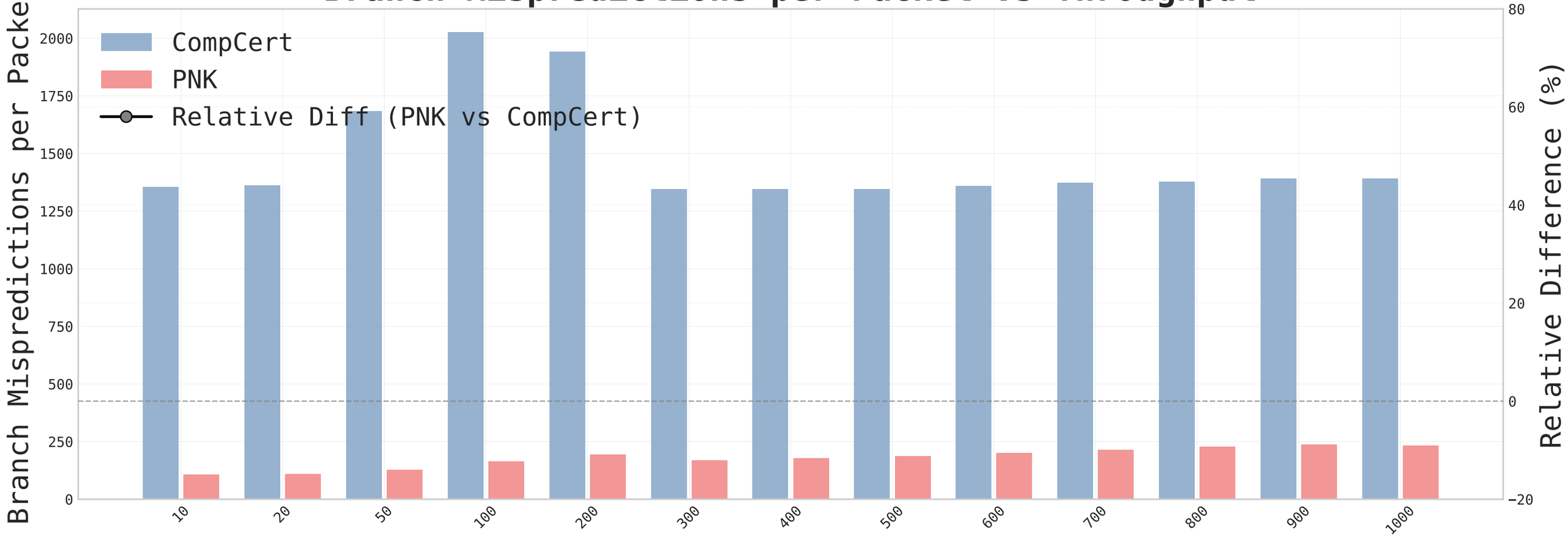
Instructions per Packet vs Throughput



-98.3% -98.3% -97.9% -97.4% -96.5% -95.9%

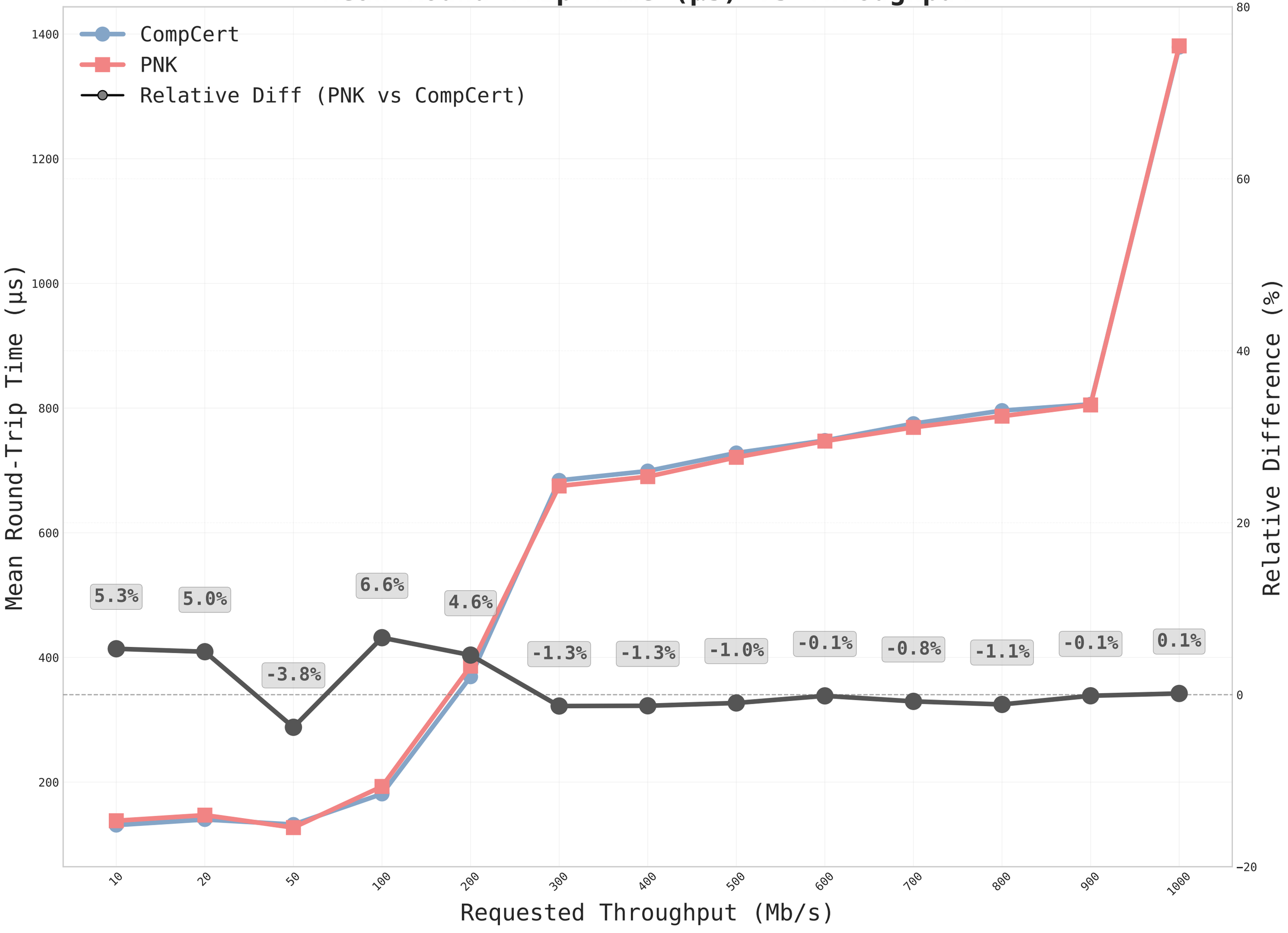
-99.3% -99.4% -99.4% -99.7% -89.6% -94.5%

Branch Mispredictions per Packet vs Throughput

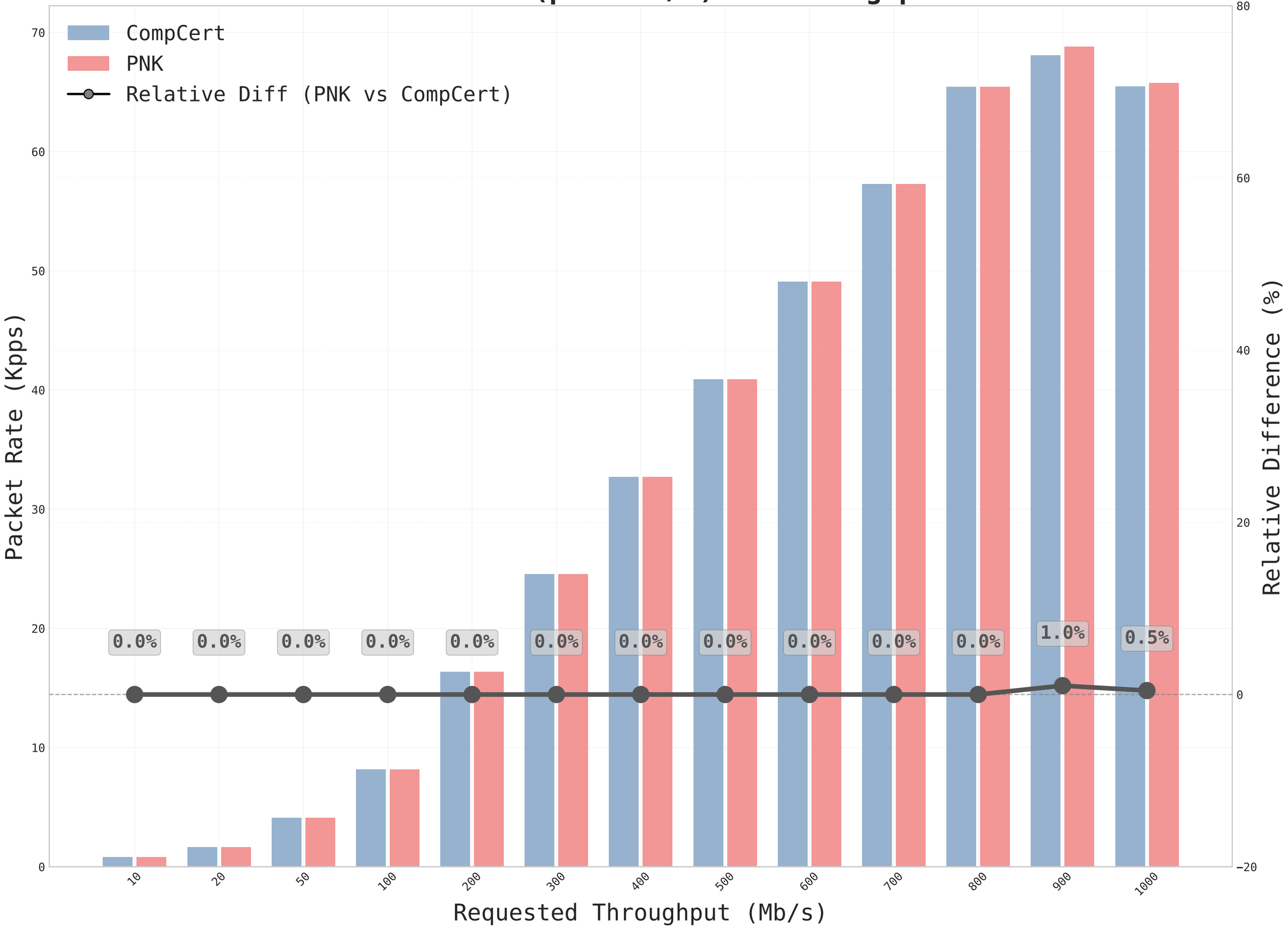


-92.2% -91.9% -92.5% -92.0% -90.0% -87.6% -86.9% -86.1% -85.3% -84.4% -83.4% -83.0% -83.2%

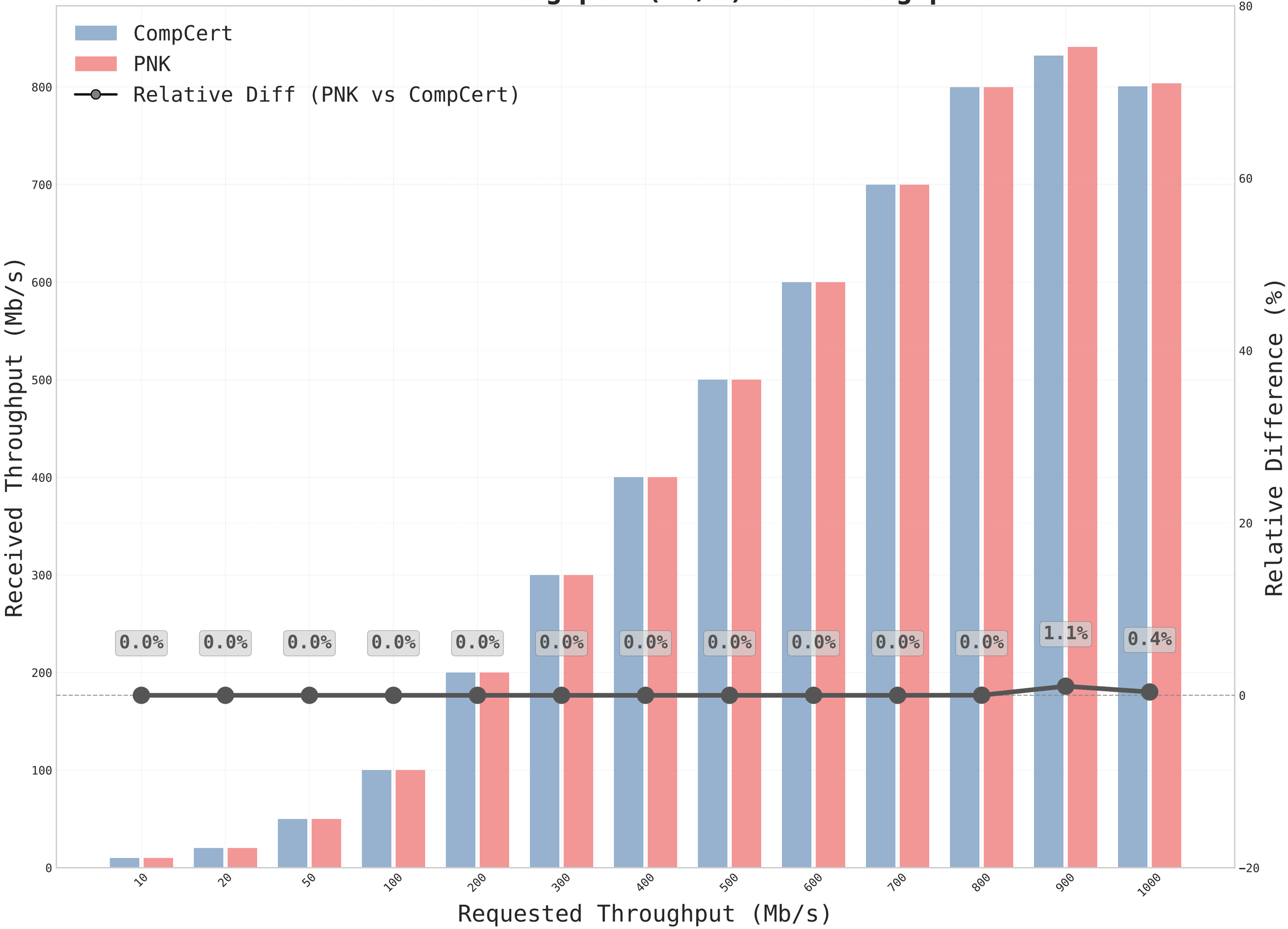
Mean Round-Trip Time (µs) vs Throughput



Packet Rate (packets/s) vs Throughput



Received Throughput (Mb/s) vs Throughput



Sent Throughput (Mb/s) vs Throughput