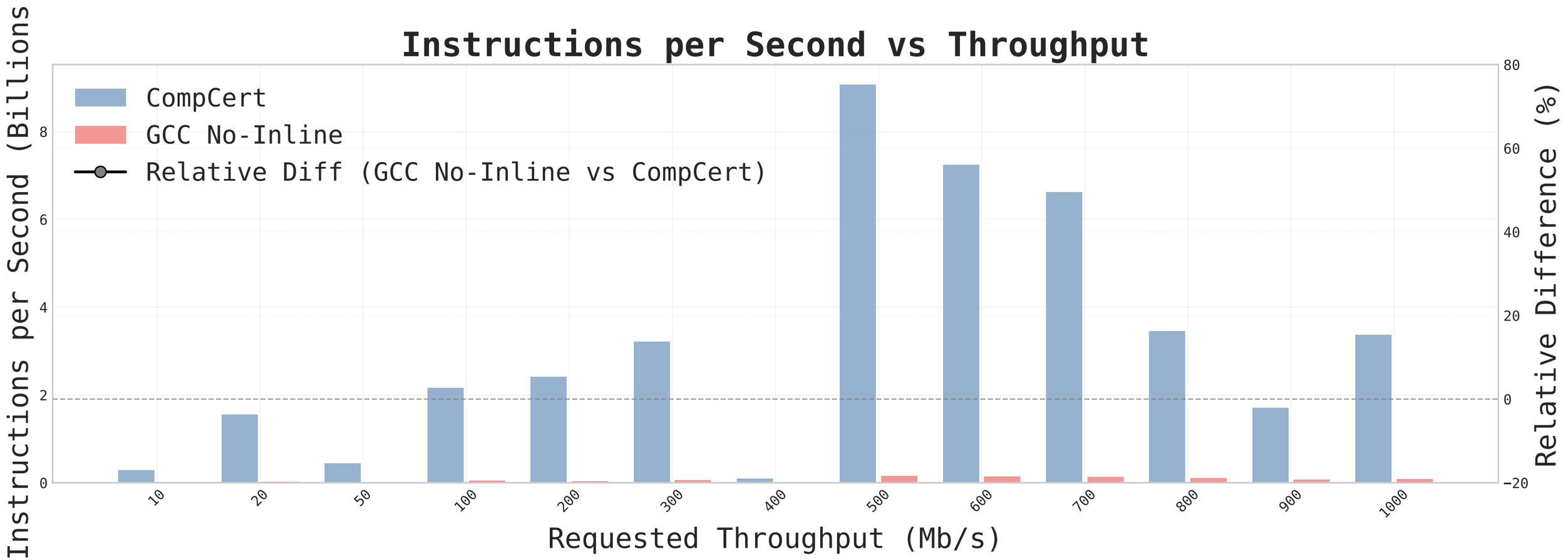
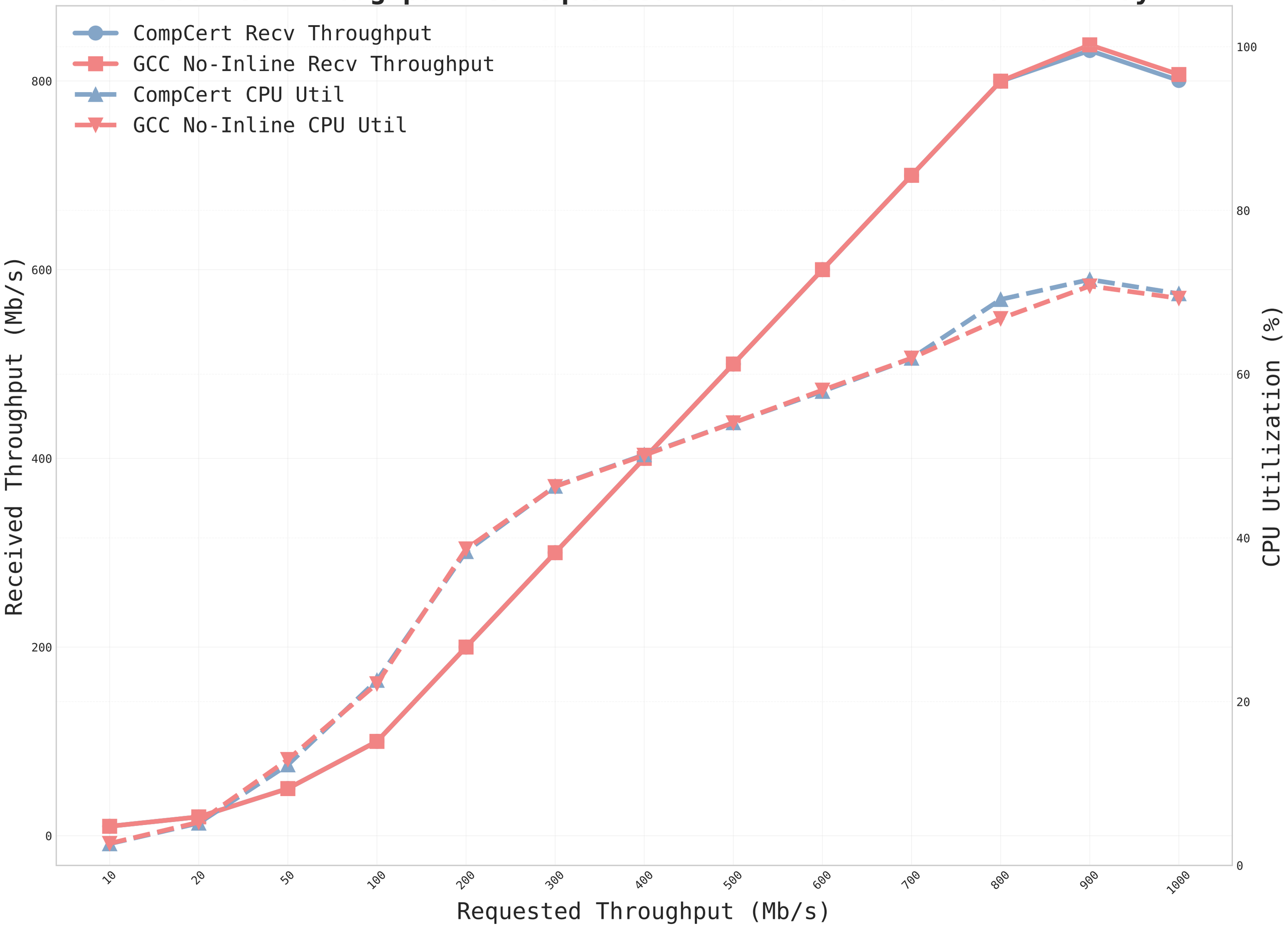
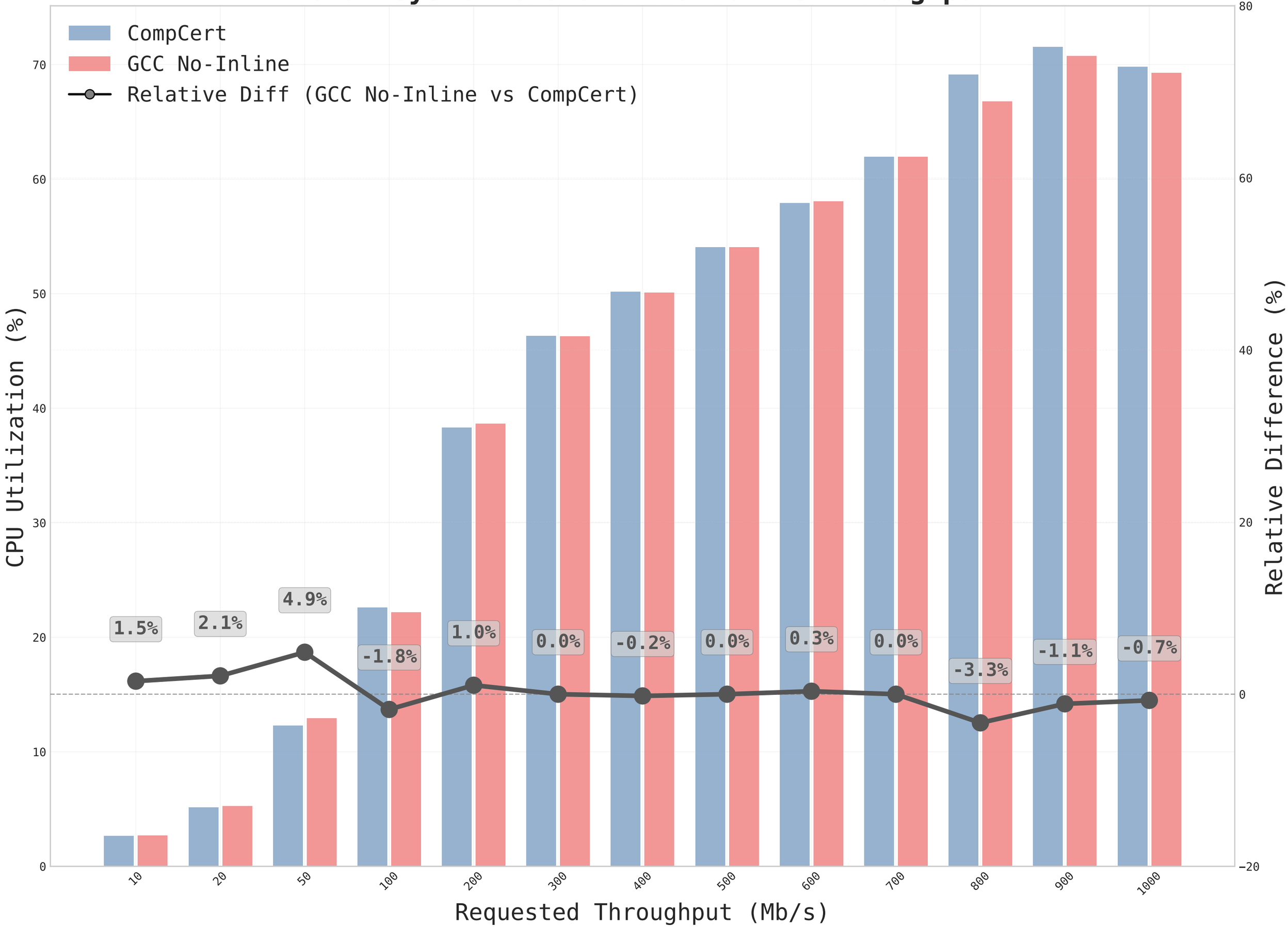


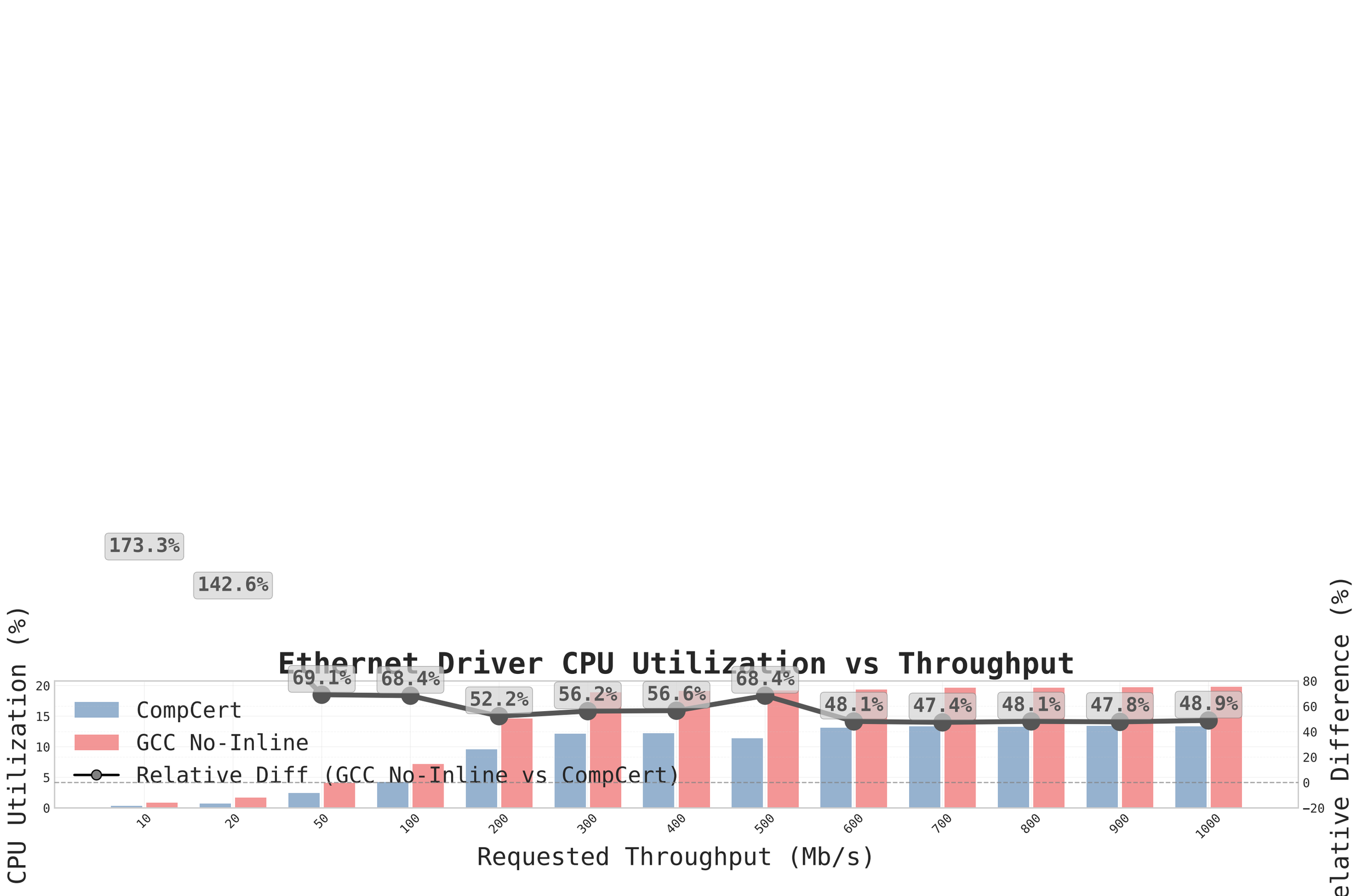
-100.0% -98.7% -100.0% -98.1% -98.3% -98.1% -90.0% -98.3% -98.2% -98.2% -97.1% -95.9% -97.6%

Received Throughput vs Requested with CPU Utilization Overlay

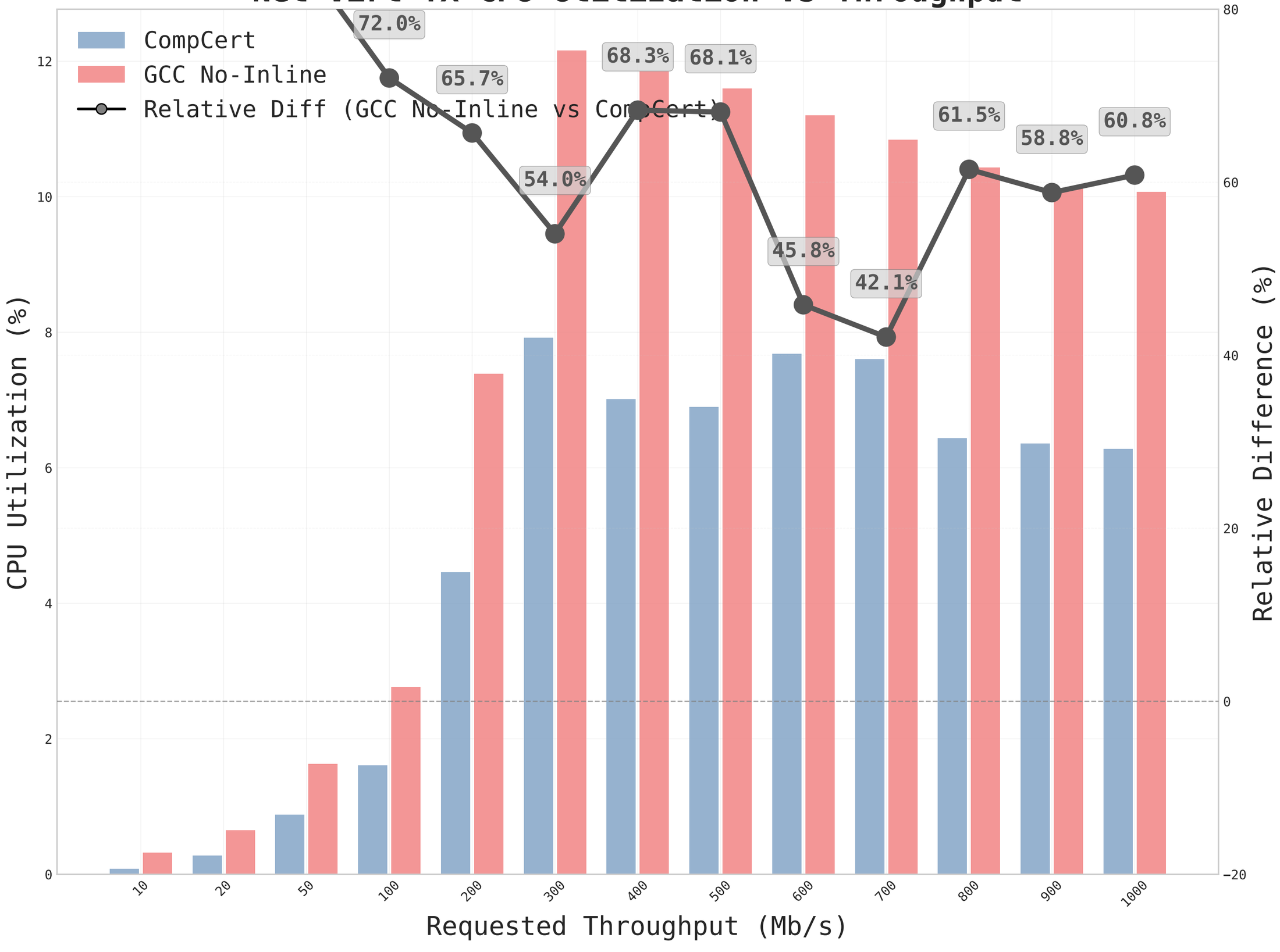


Total System CPU Utilization vs Throughput

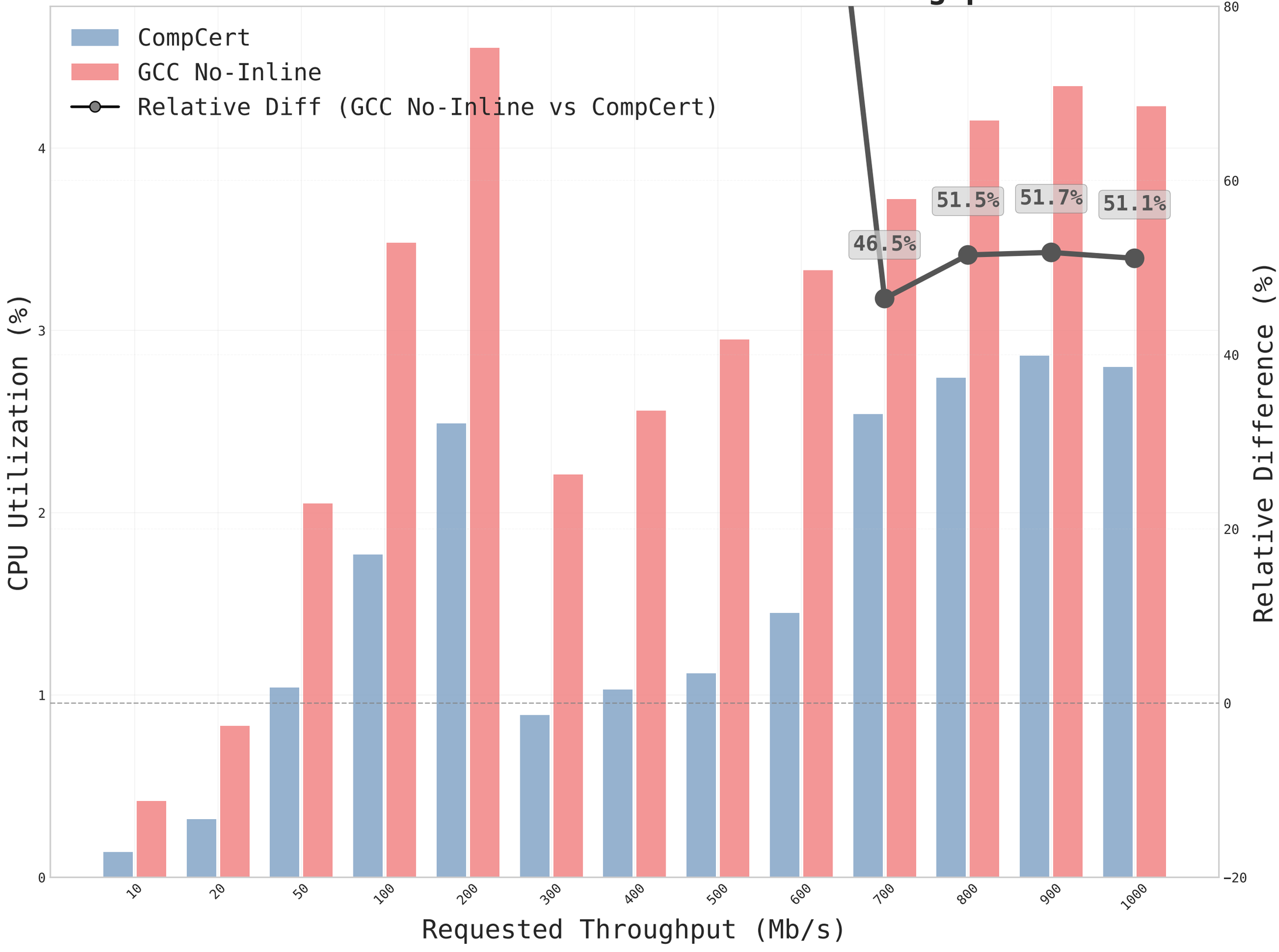



Ethernet Driver CPU Utilization vs Throughput
CompCert
GCC No-Inline
Relative Diff (GCC No-Inline vs CompCert)
CPU Utilization (%)
Relative Difference (%)
Requested Throughput (Mb/s)
173.3%
142.6%
69.1%
68.4%
52.2%
56.2%
56.6%
68.4%
48.1%
47.4%
48.1%
47.8%
48.9%
0
5
10
15
20
-20
0
20
40
60
80
10
20
50
100
200
300
400
500
600
700
800
900
1000

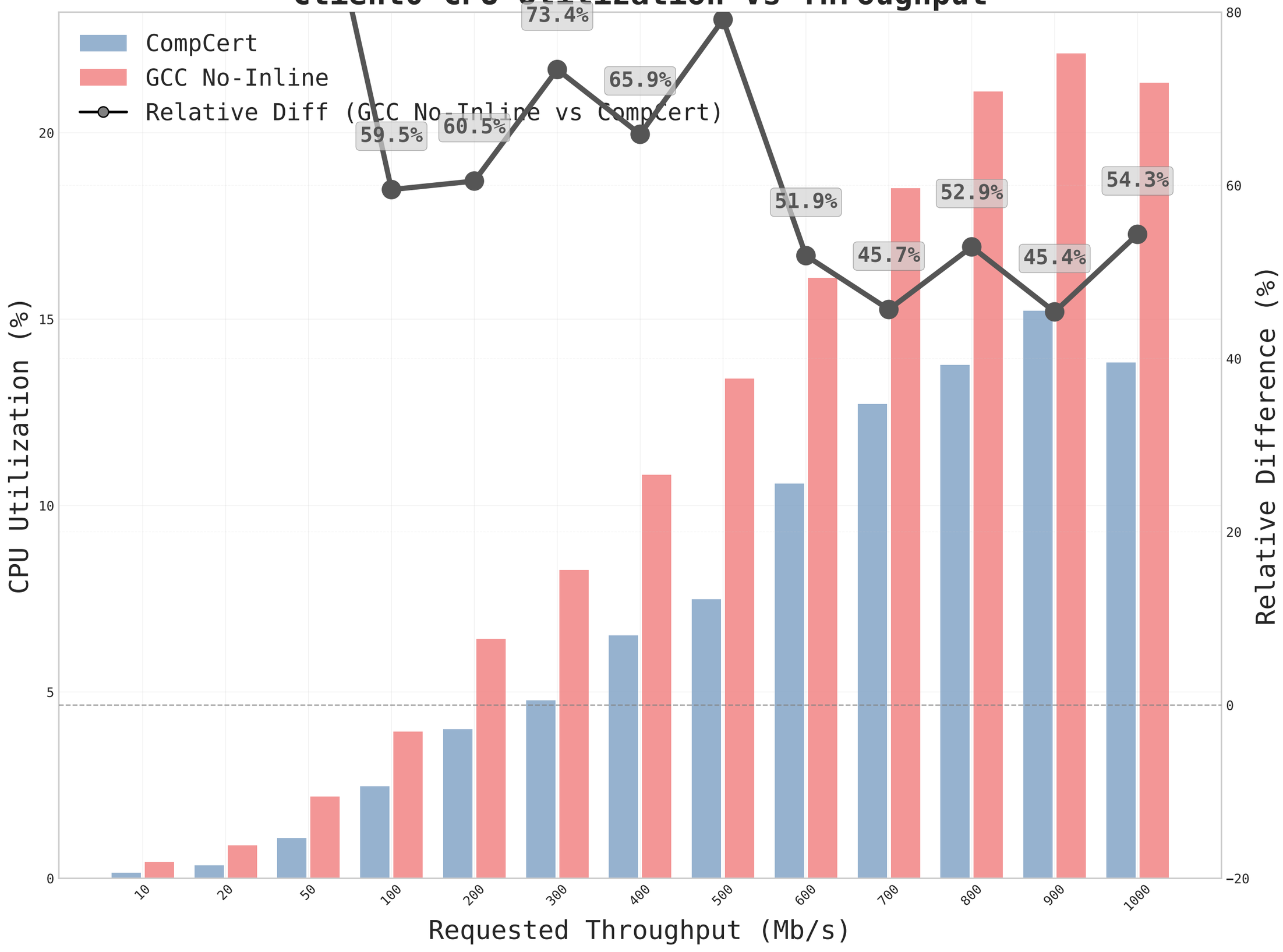
Net Virt TX CPU Utilization vs Throughput

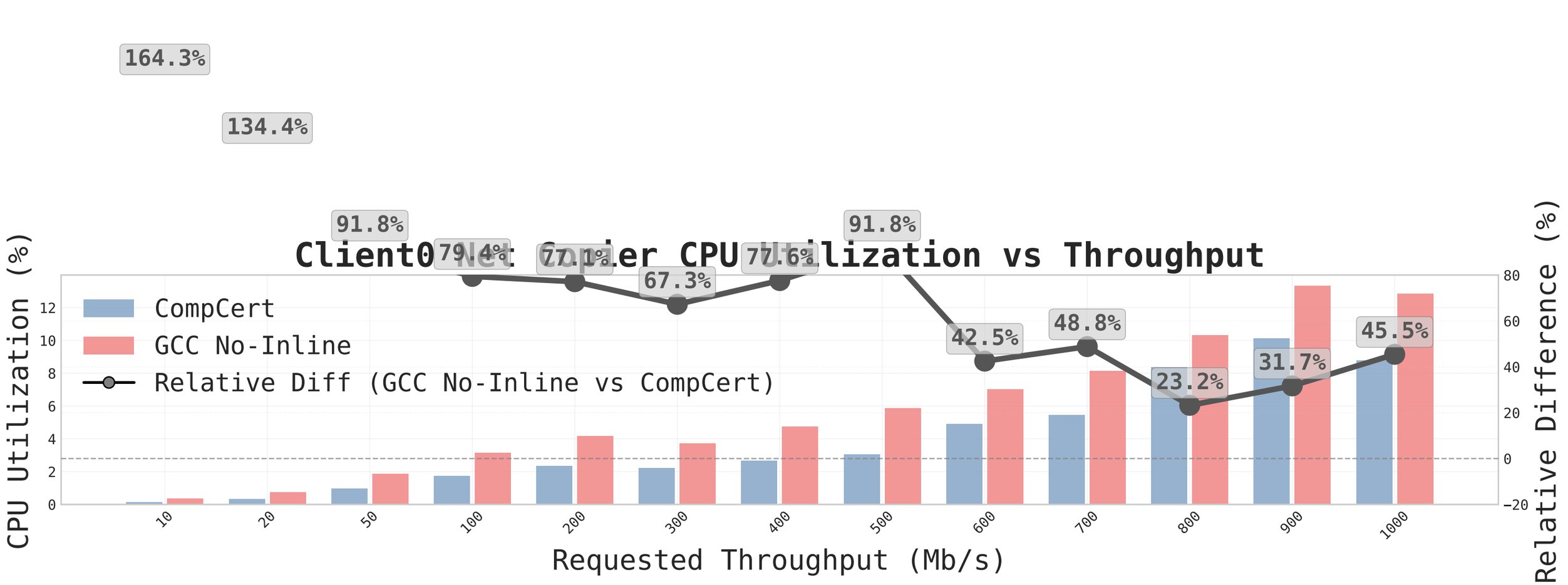


Net Virt RX CPU Utilization vs Throughput

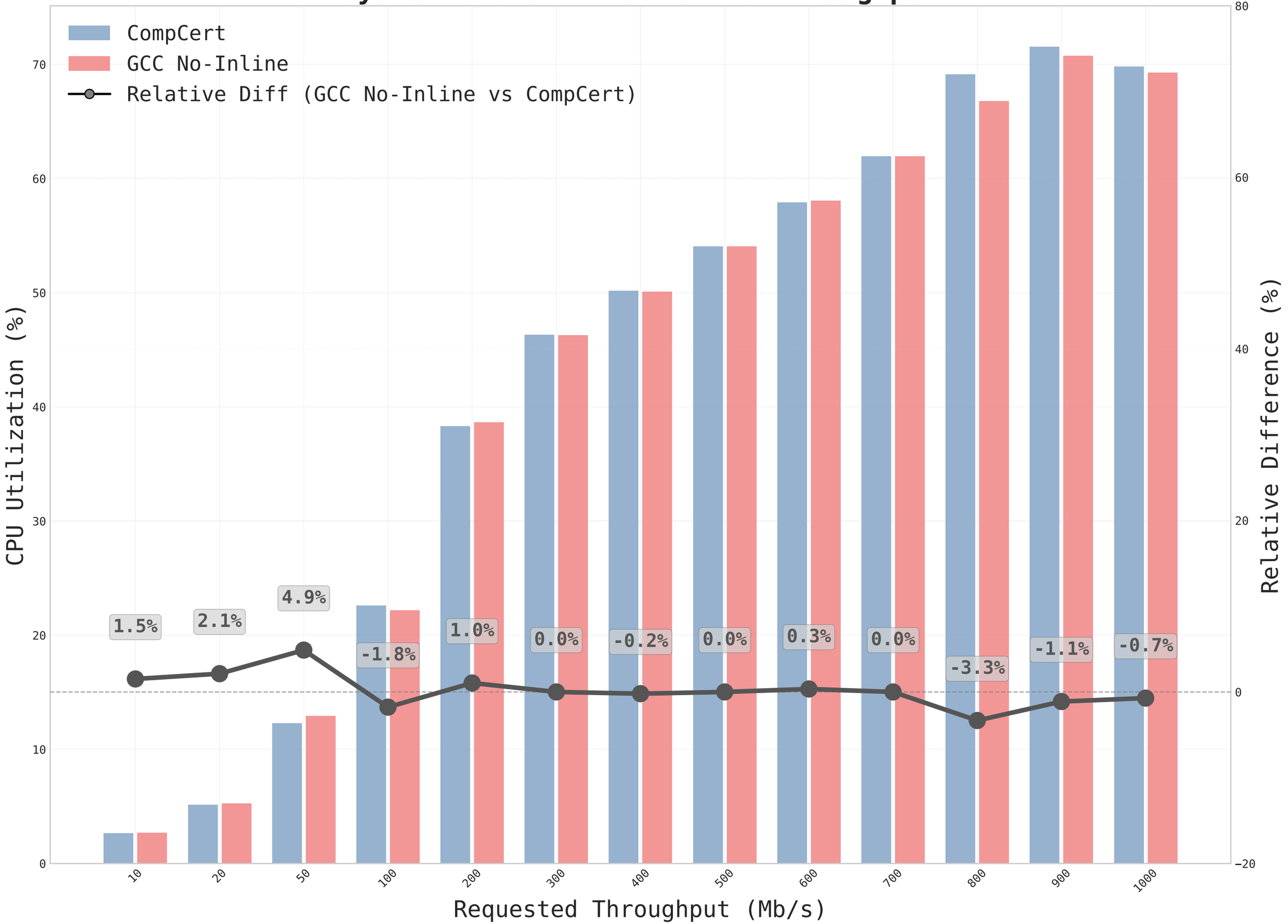


Client0 CPU Utilization vs Throughput

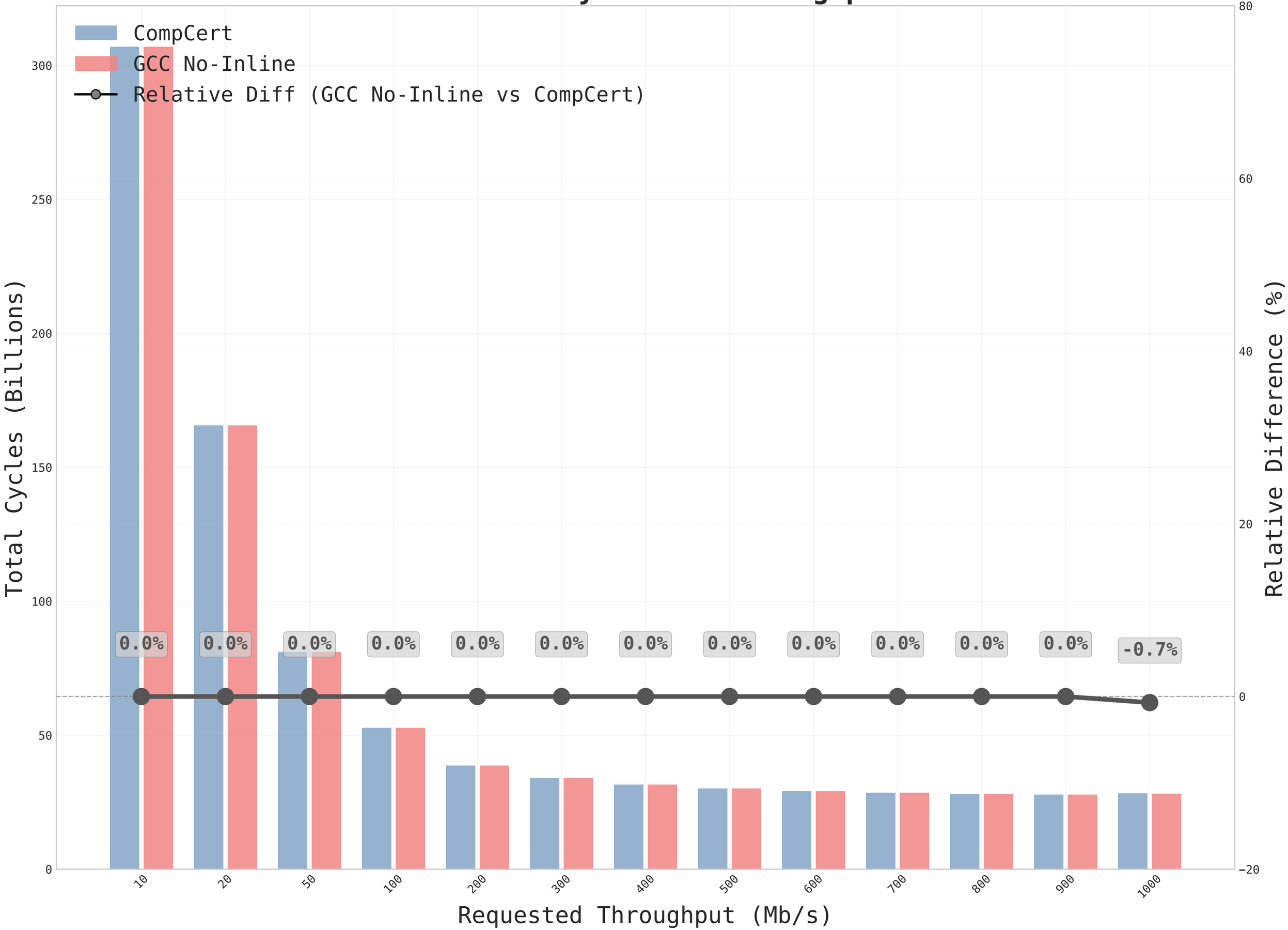


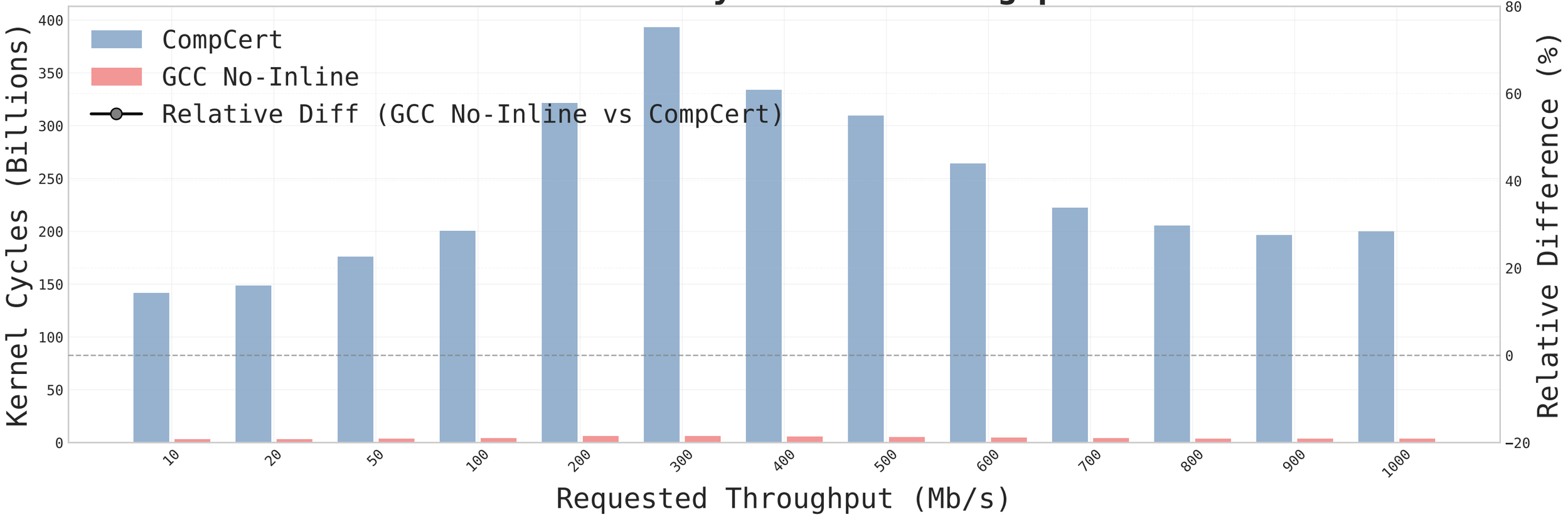

164.3%
134.4%
91.8%
79.4%
77.1%
67.3%
77.6%
91.8%
42.5%
48.8%
23.2%
31.7%
45.5%
Client0 Net Compiler CPU Utilization vs Throughput
CompCert
GCC No-Inline
Relative Diff (GCC No-Inline vs CompCert)
CPU Utilization (%)
Relative Difference (%)
Requested Throughput (Mb/s)
0
2
4
6
8
10
12
-20
0
20
40
60
80
10
20
50
100
200
300
400
500
600
700
800
900
1000

System CPU Utilization vs Throughput

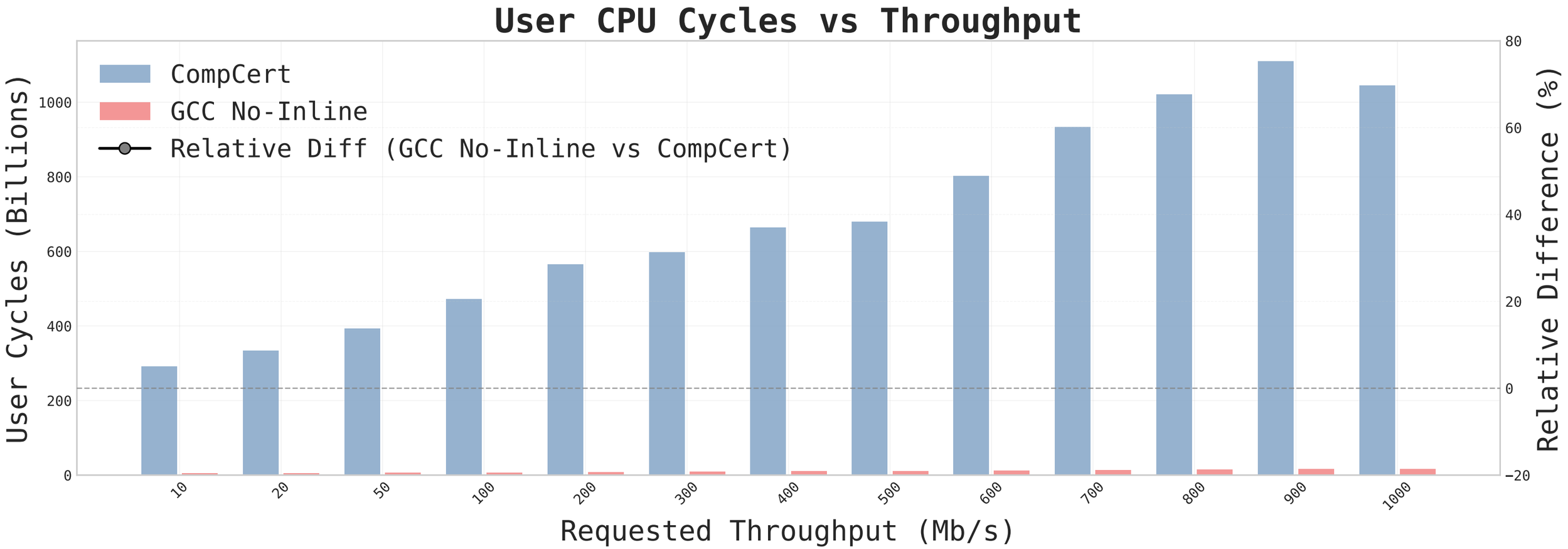


Total CPU Cycles vs Throughput



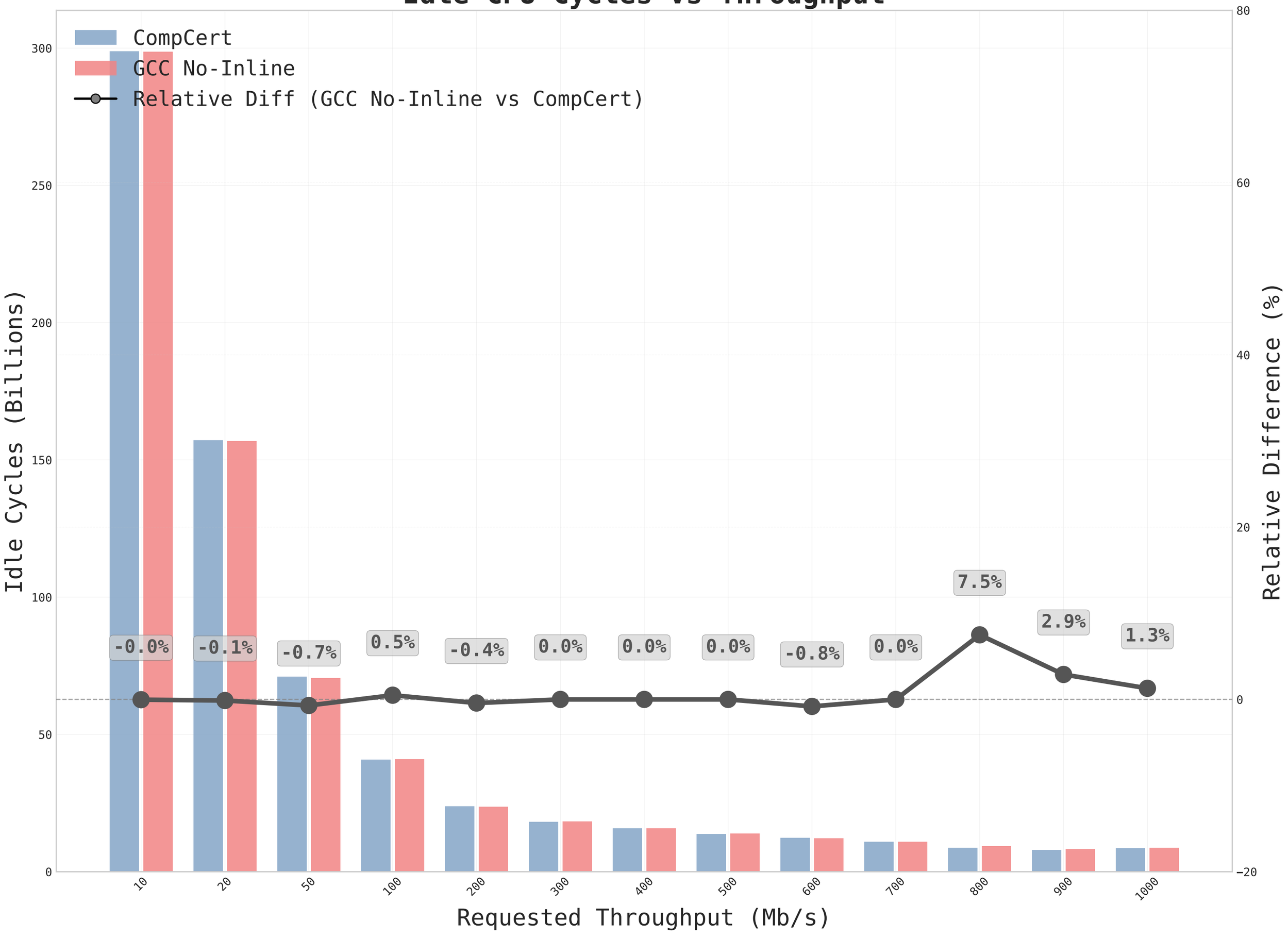


10	20	50	100	200	300	400	500	600	700	800	900	1000
-97.9%	-97.8%	-97.7%	-97.9%	-98.1%	-98.4%	-98.3%	-98.4%	-98.3%	-98.1%	-98.2%	-98.2%	-98.2%

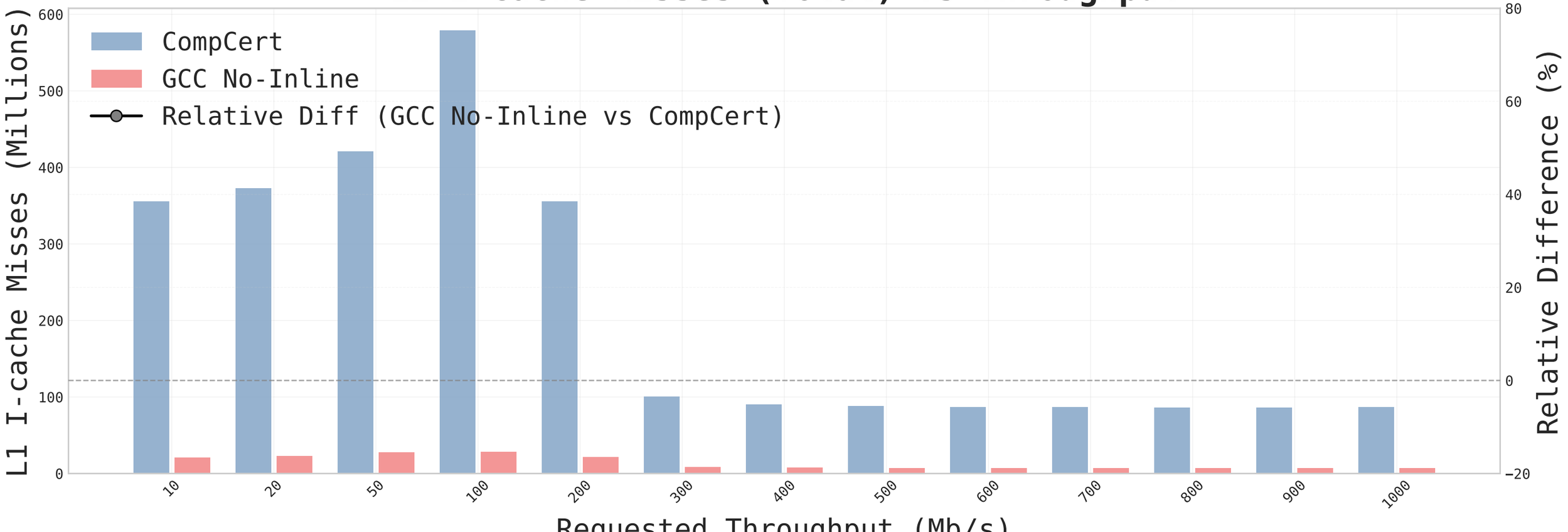


-98.5%	-98.6%	-98.6%	-98.6%	-98.5%	-98.5%	-98.5%	-98.4%	-98.5%	-98.6%	-98.6%	-98.6%	-98.5%

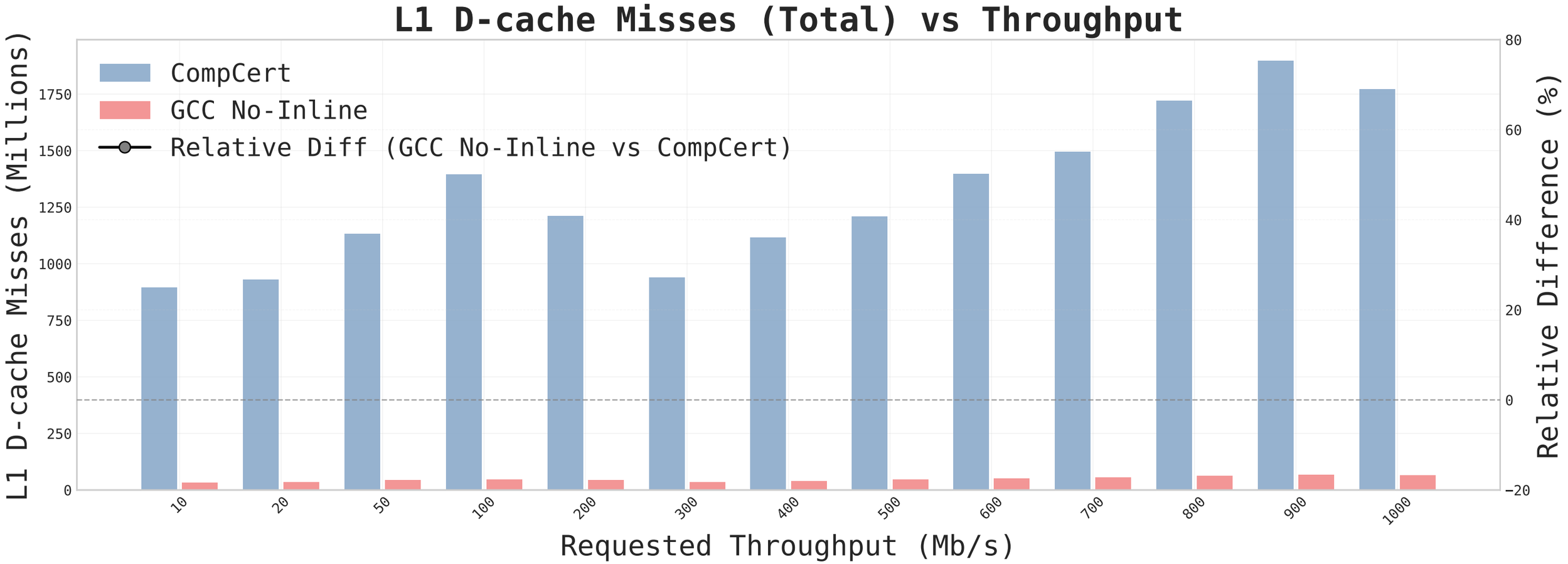
Idle CPU Cycles vs Throughput



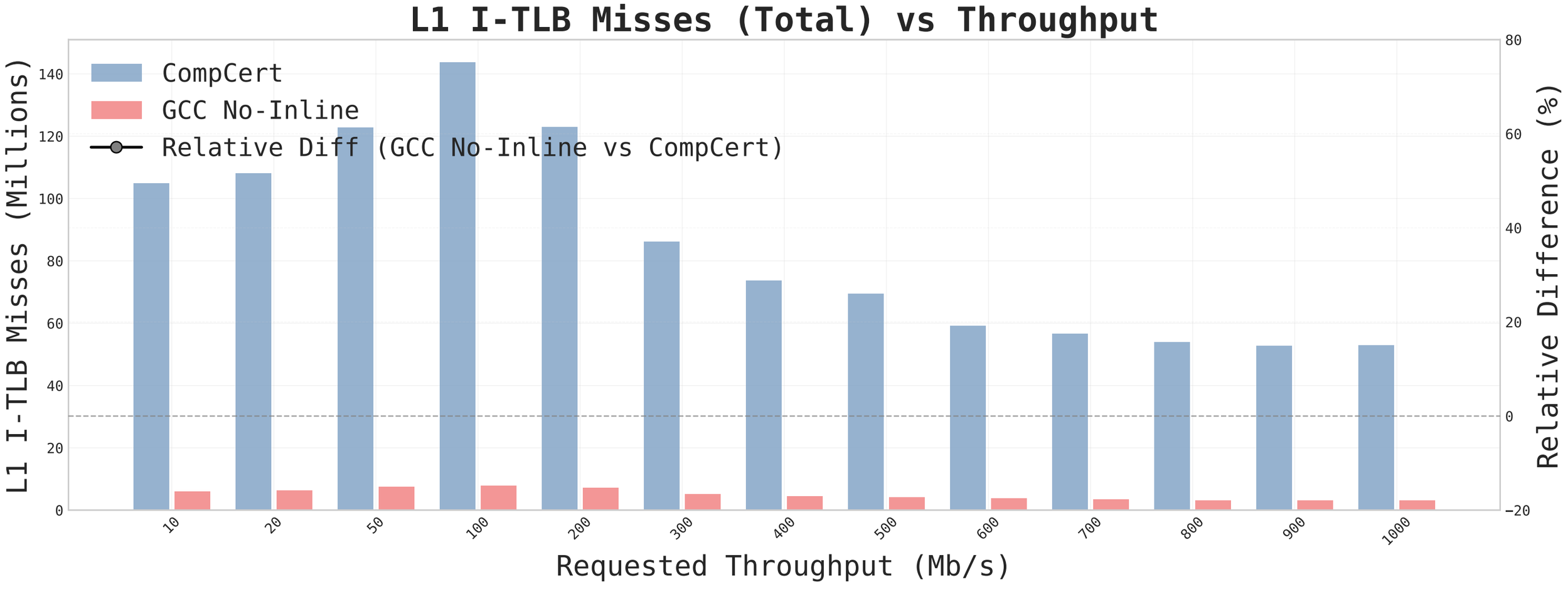
L1 I-cache Misses (Total) vs Throughput



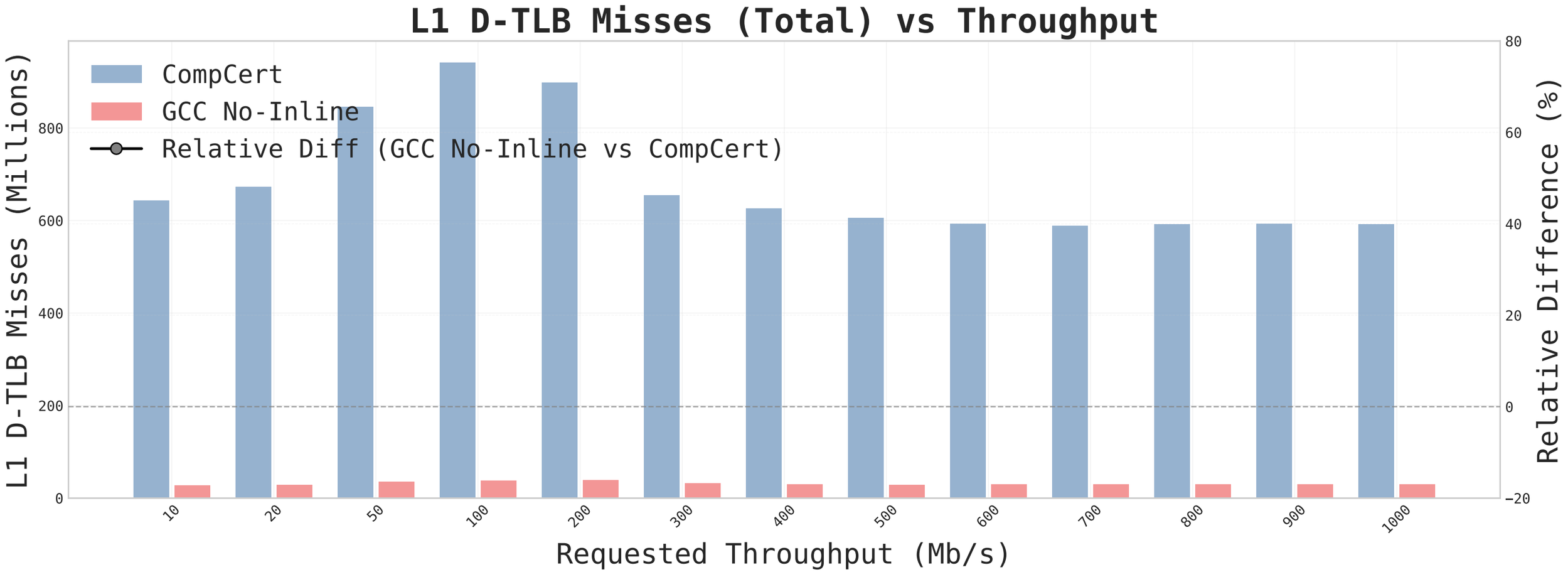
10	20	50	100	200	300	400	500	600	700	800	900	1000
-94.0%	-93.9%	-93.4%	-95.1%	-94.0%	-91.9%	-91.5%	-91.7%	-91.8%	-92.0%	-92.0%	-91.9%	-91.8%



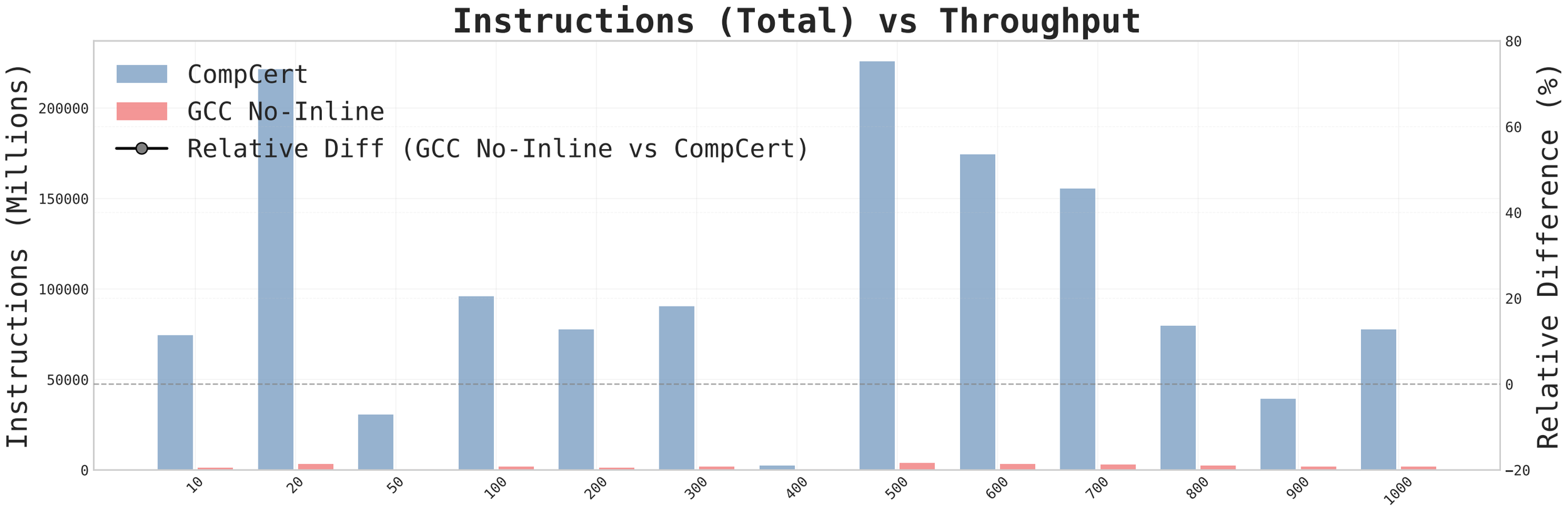
-96.4%	-96.3%	-96.2%	-96.7%	-96.4%	-96.4%	-96.5%	-96.3%	-96.3%	-96.3%	-96.5%	-96.5%	-96.4%



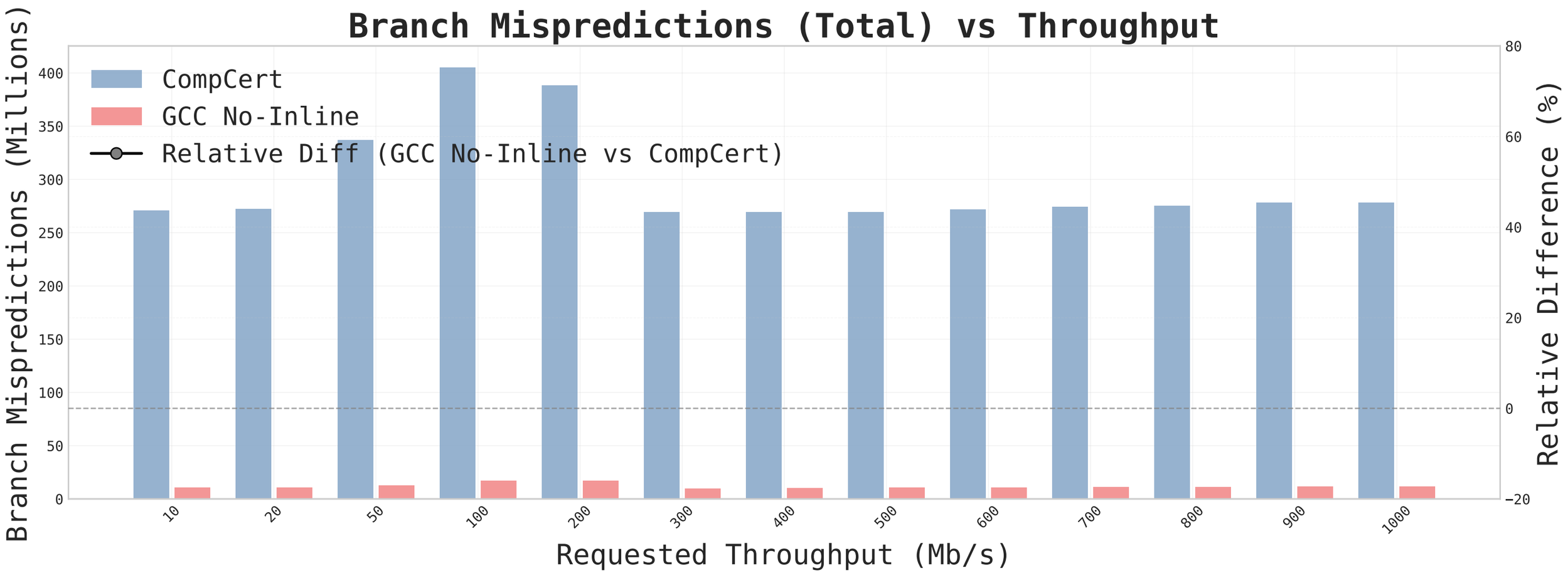
10	20	50	100	200	300	400	500	600	700	800	900	1000
-94.3%	-94.1%	-93.8%	-94.5%	-94.1%	-94.1%	-93.9%	-94.1%	-93.7%	-93.9%	-94.1%	-94.2%	-94.1%



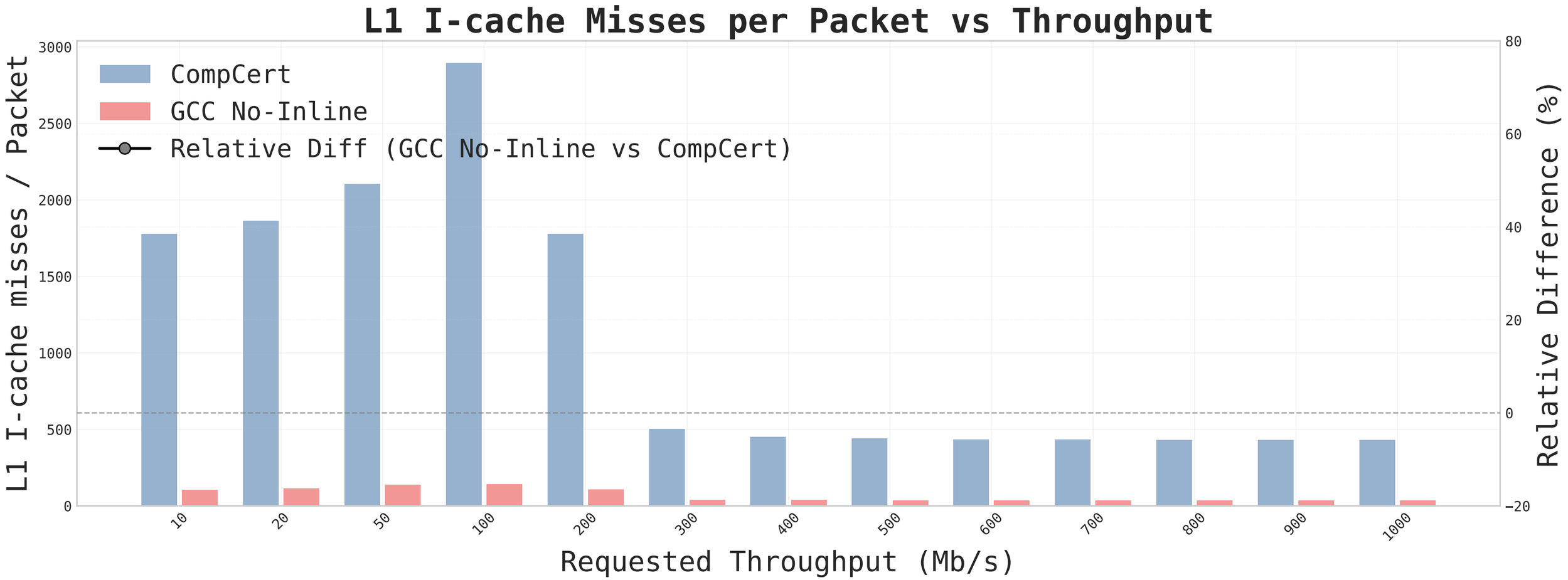
-95.8%	-95.6%	-95.8%	-96.0%	-95.6%	-95.1%	-95.2%	-95.2%	-94.9%	-95.0%	-95.0%	-94.9%	-94.9%



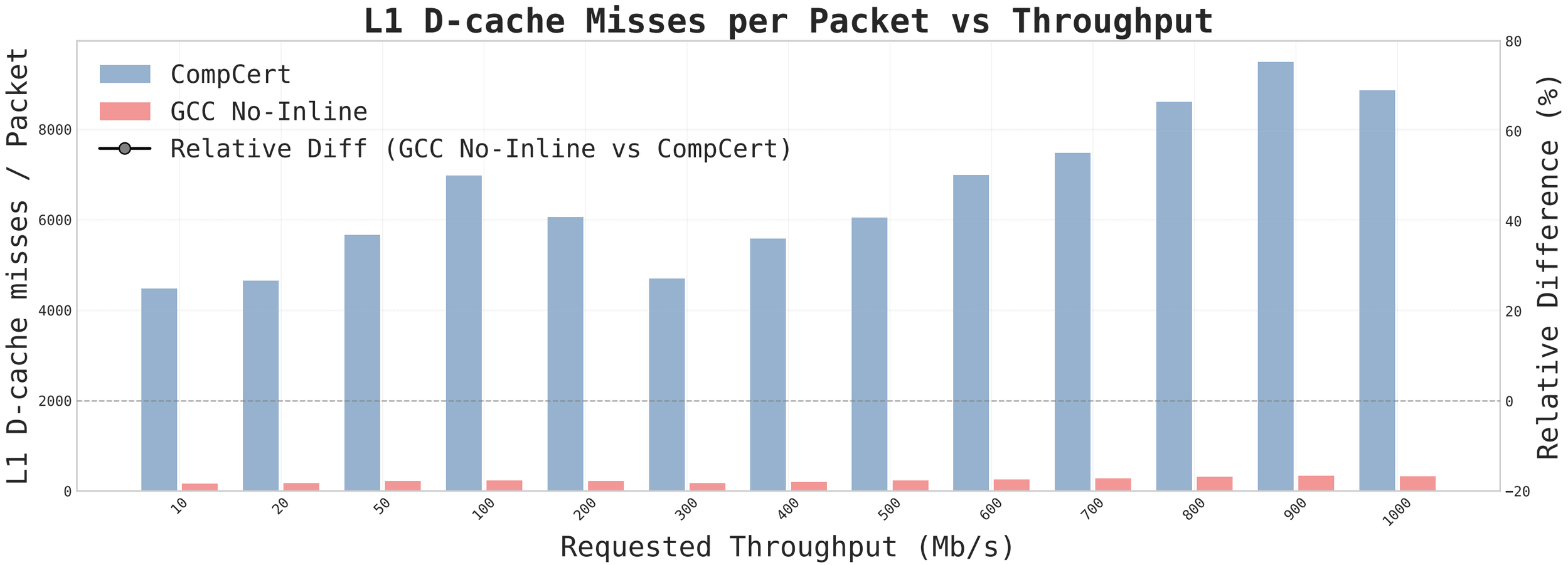
-98.5% -98.5% -98.9% -98.0% -98.4% -98.1% -86.3% -98.3% -98.1% -98.2% -97.1% -95.7% -97.6%



10	20	50	100	200	300	400	500	600	700	800	900	1000
-96.0%	-96.0%	-96.3%	-95.8%	-95.6%	-96.3%	-96.2%	-96.1%	-96.1%	-96.0%	-95.9%	-95.8%	-95.8%

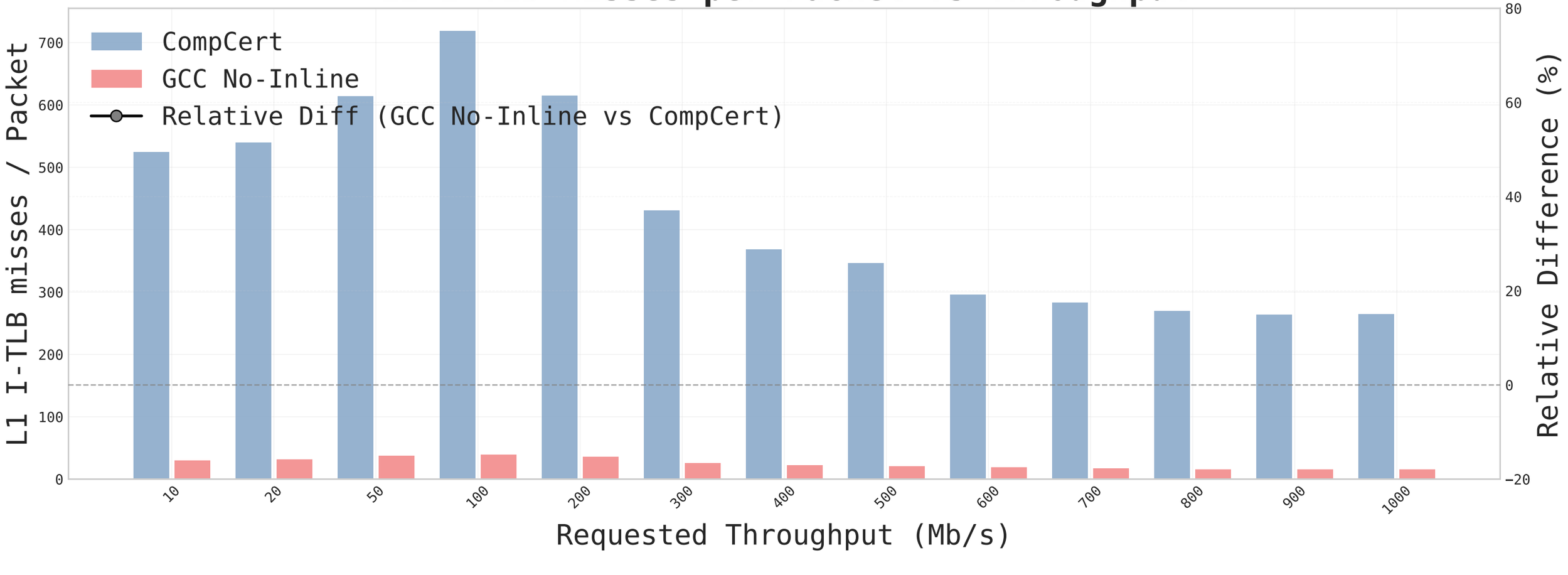


10	20	50	100	200	300	400	500	600	700	800	900	1000
-94.0%	-93.8%	-93.4%	-95.1%	-94.0%	-91.9%	-91.5%	-91.7%	-91.8%	-92.0%	-92.0%	-91.9%	-91.8%

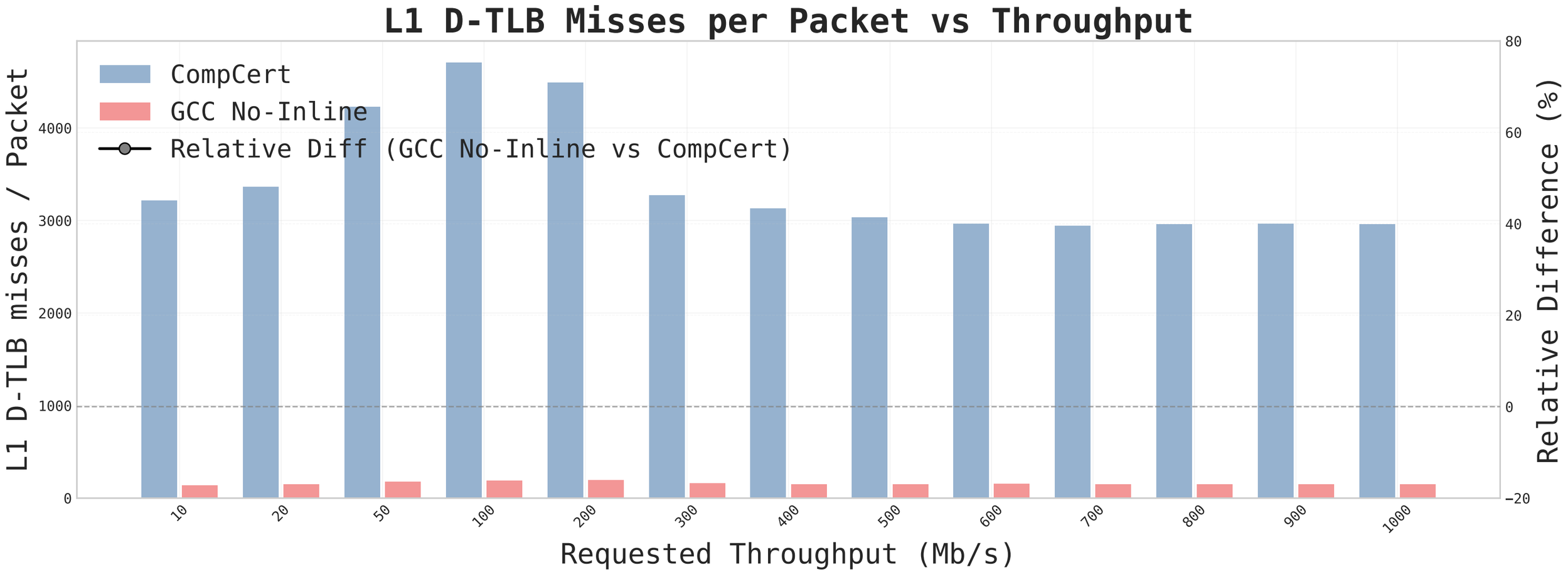


-96.4%	-96.3%	-96.3%	-96.7%	-96.4%	-96.4%	-96.5%	-96.3%	-96.3%	-96.3%	-96.5%	-96.5%	-96.4%

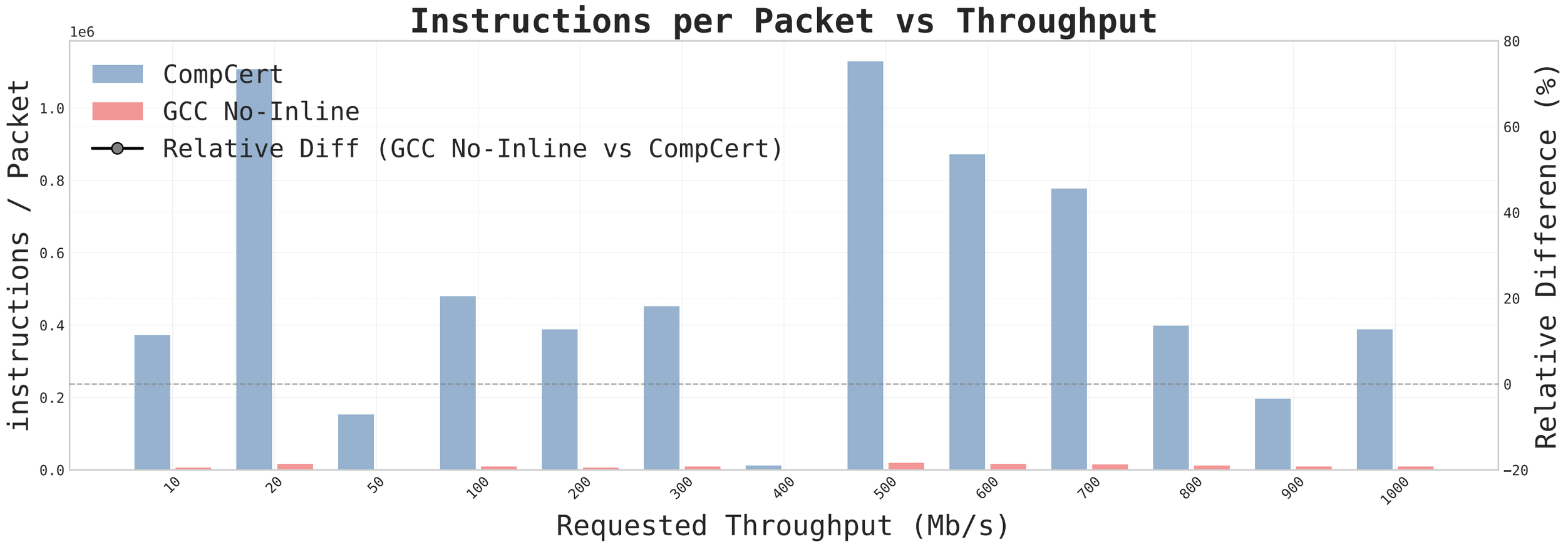
L1 I-TLB Misses per Packet vs Throughput



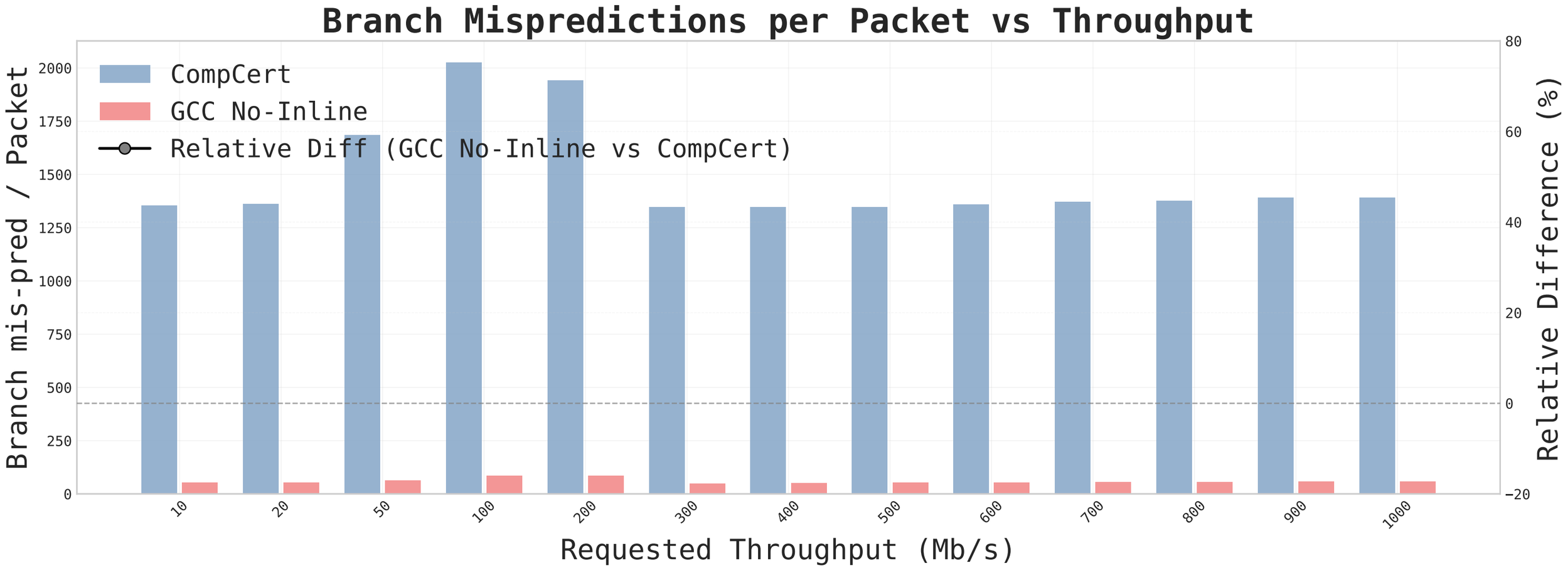
10	20	50	100	200	300	400	500	600	700	800	900	1000
-94.3%	-94.1%	-93.8%	-94.5%	-94.1%	-94.1%	-93.9%	-94.1%	-93.7%	-93.9%	-94.1%	-94.2%	-94.1%



10	20	50	100	200	300	400	500	600	700	800	900	1000
-95.8%	-95.6%	-95.8%	-96.0%	-95.6%	-95.1%	-95.2%	-95.2%	-94.9%	-95.0%	-95.0%	-94.9%	-94.9%

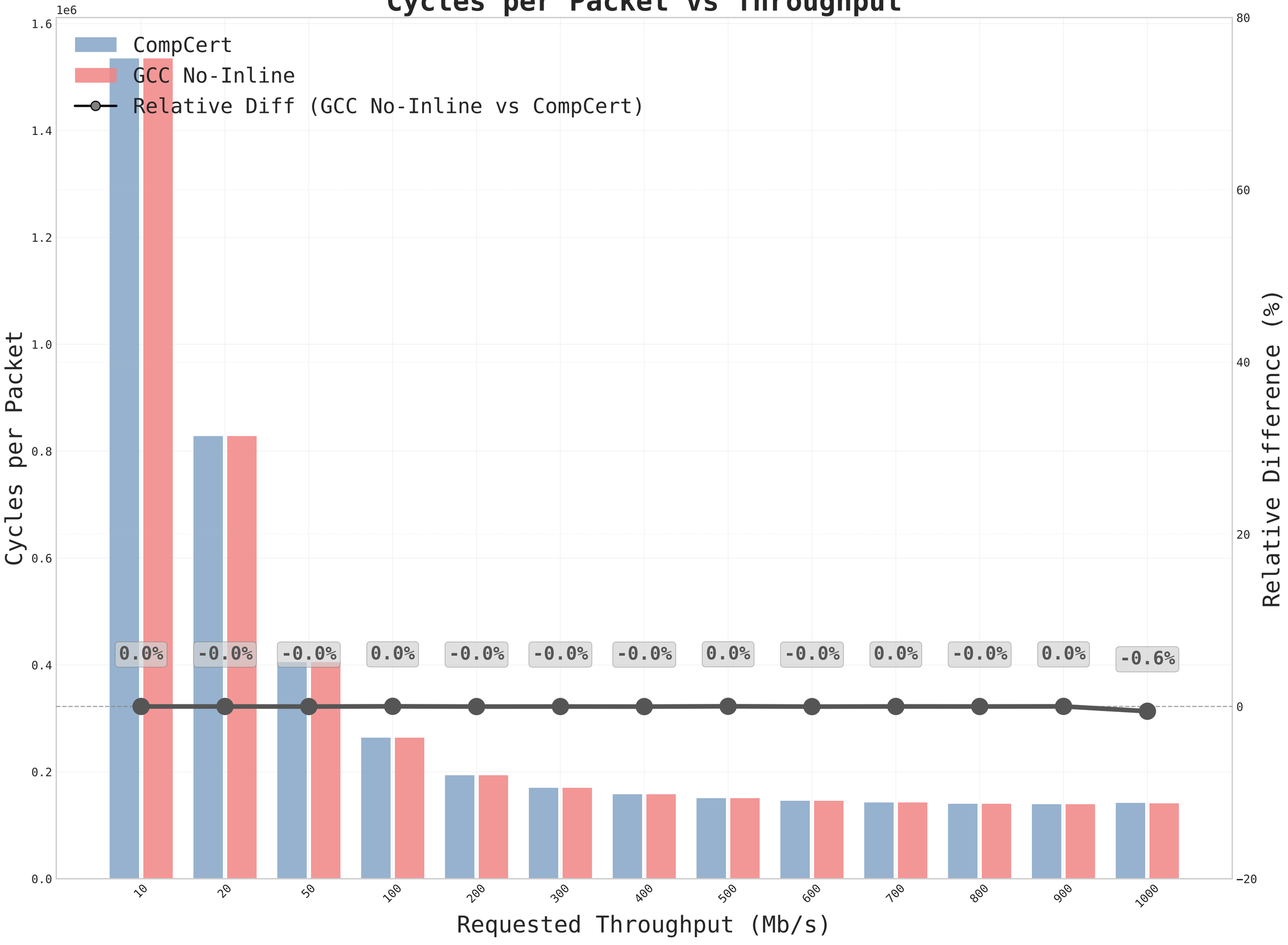


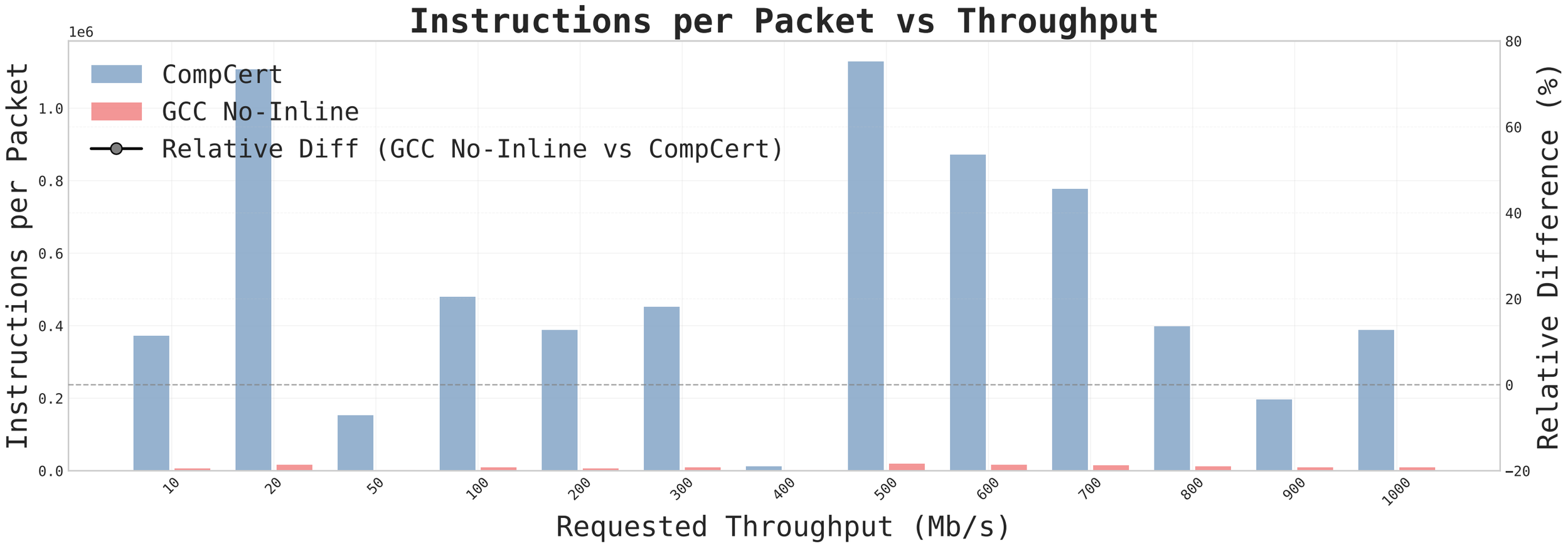
10	20	50	100	200	300	400	500	600	700	800	900	1000
-98.5%	-98.5%	-98.9%	-98.0%	-98.4%	-98.1%	-86.3%	-98.3%	-98.1%	-98.2%	-97.1%	-95.7%	-97.6%



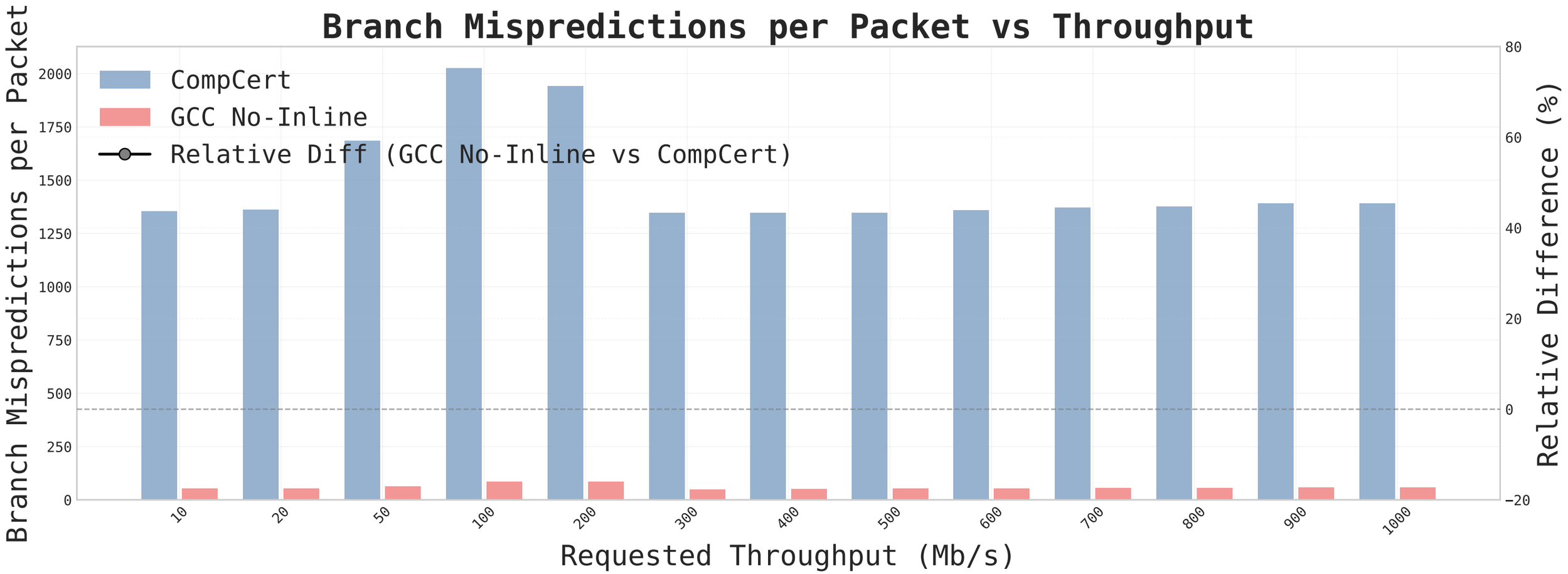
10	20	50	100	200	300	400	500	600	700	800	900	1000
-96.1%	-96.0%	-96.3%	-95.8%	-95.6%	-96.4%	-96.2%	-96.1%	-96.1%	-96.0%	-95.9%	-95.8%	-95.7%

Cycles per Packet vs Throughput



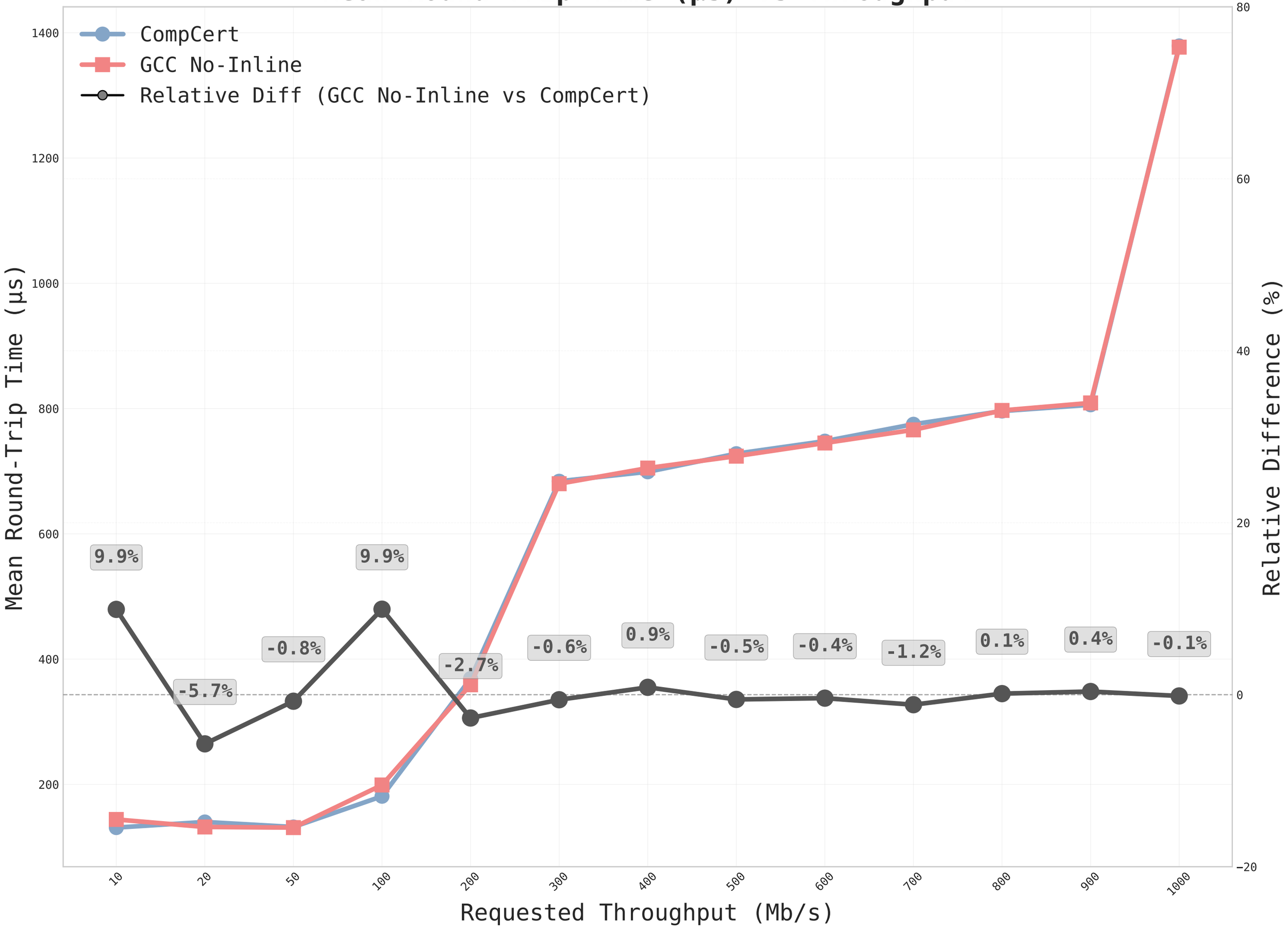


10	20	50	100	200	300	400	500	600	700	800	900	1000
-98.5%	-98.5%	-98.9%	-98.0%	-98.4%	-98.1%	-86.3%	-98.3%	-98.1%	-98.2%	-97.1%	-95.7%	-97.6%

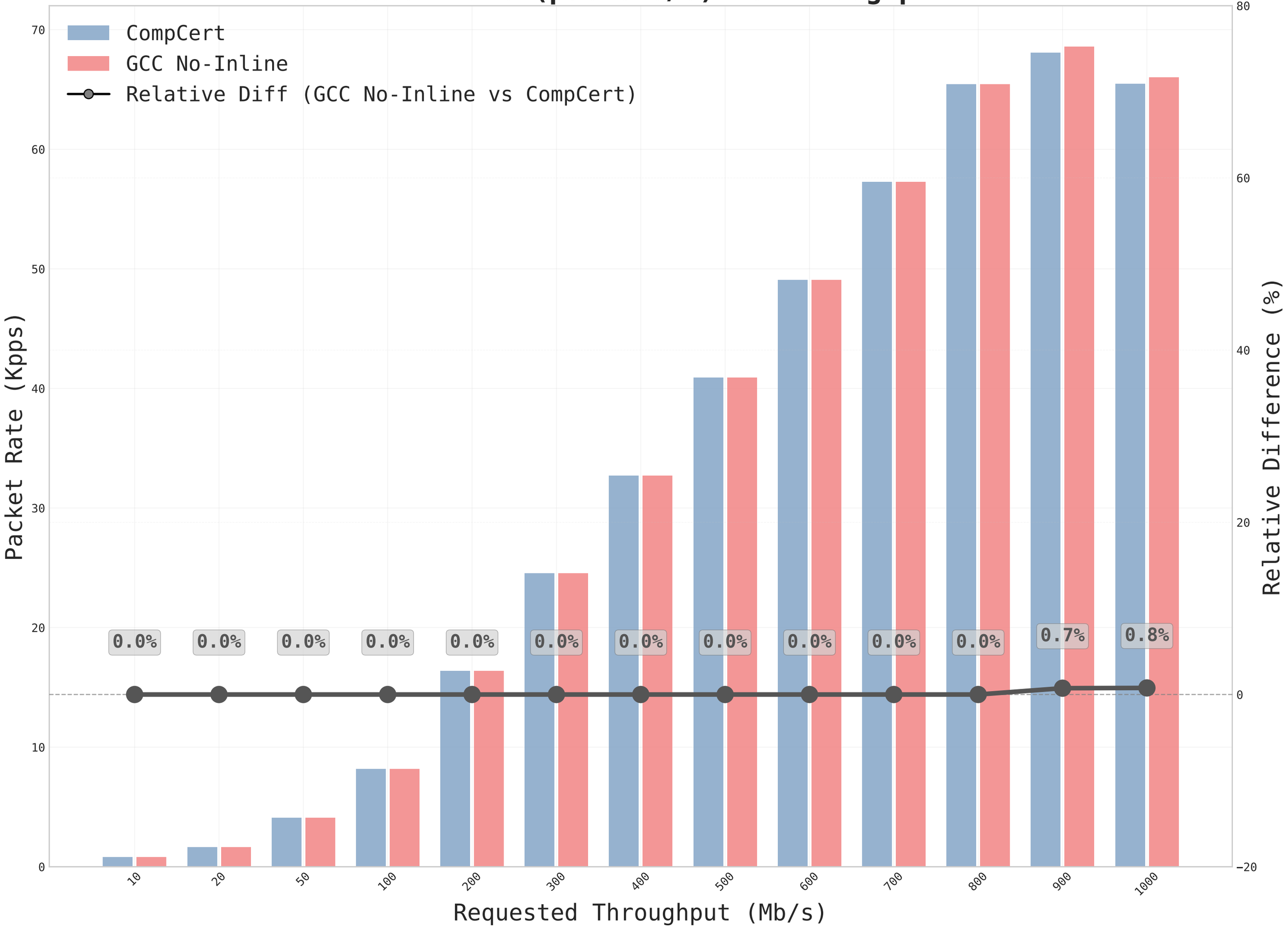


-96.1%	-96.0%	-96.3%	-95.8%	-95.6%	-96.4%	-96.2%	-96.1%	-96.1%	-96.0%	-95.9%	-95.8%	-95.7%

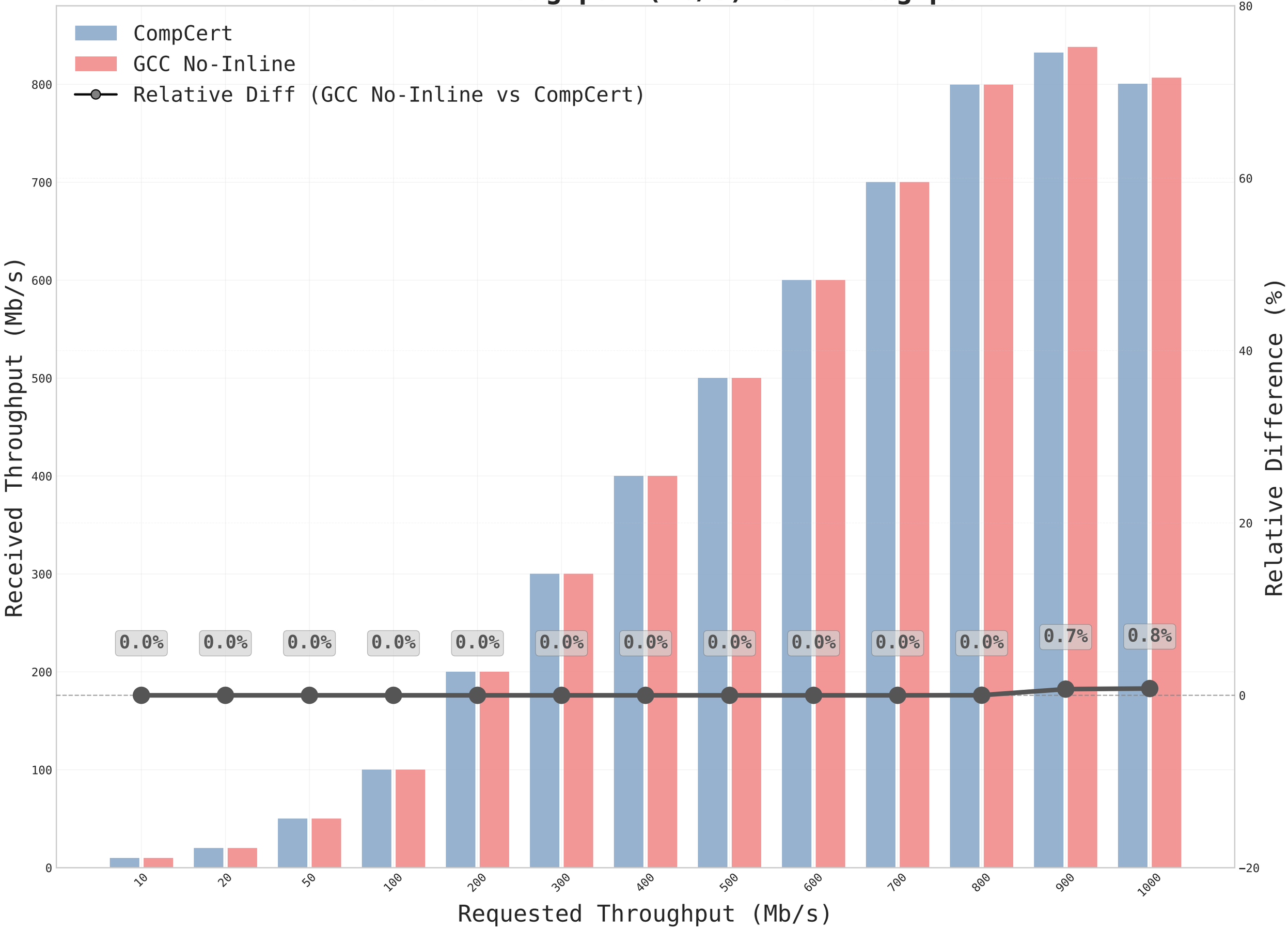
Mean Round-Trip Time (µs) vs Throughput



Packet Rate (packets/s) vs Throughput



Received Throughput (Mb/s) vs Throughput



Sent Throughput (Mb/s) vs Throughput