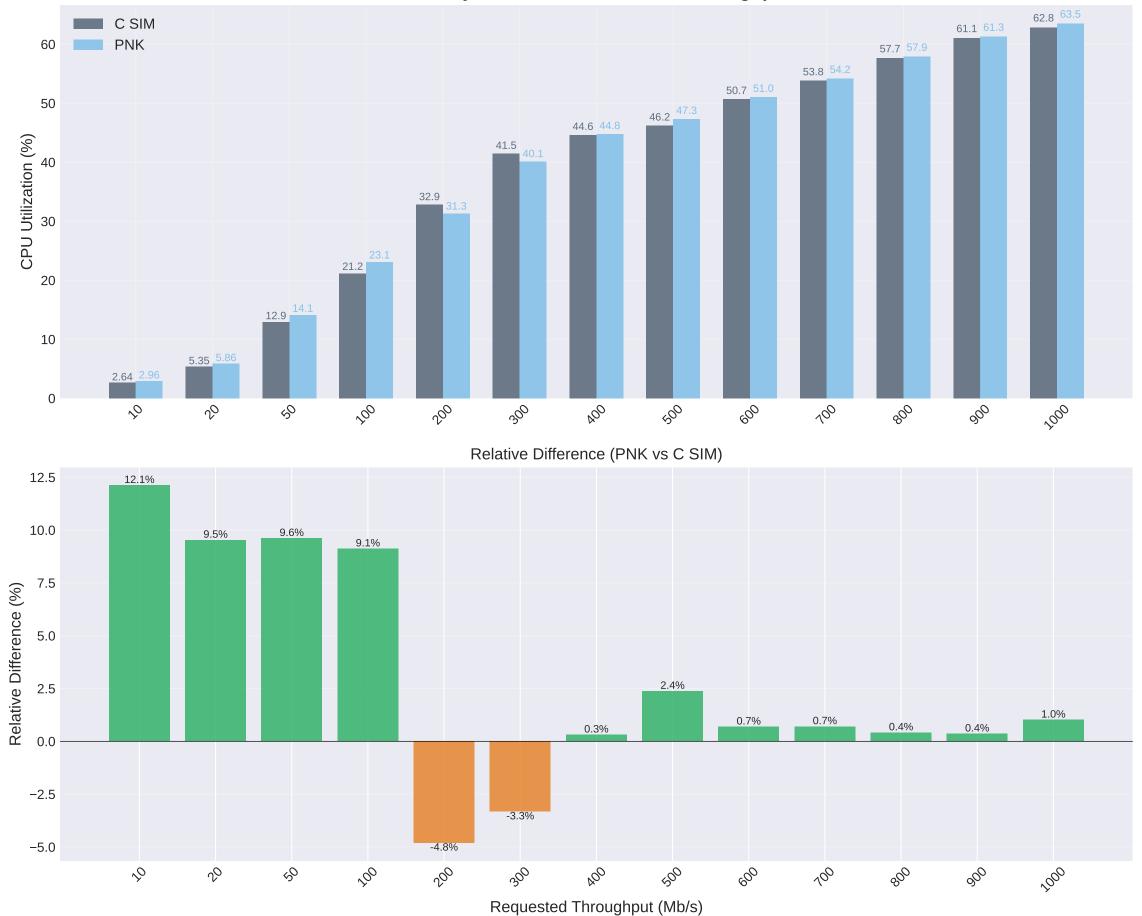


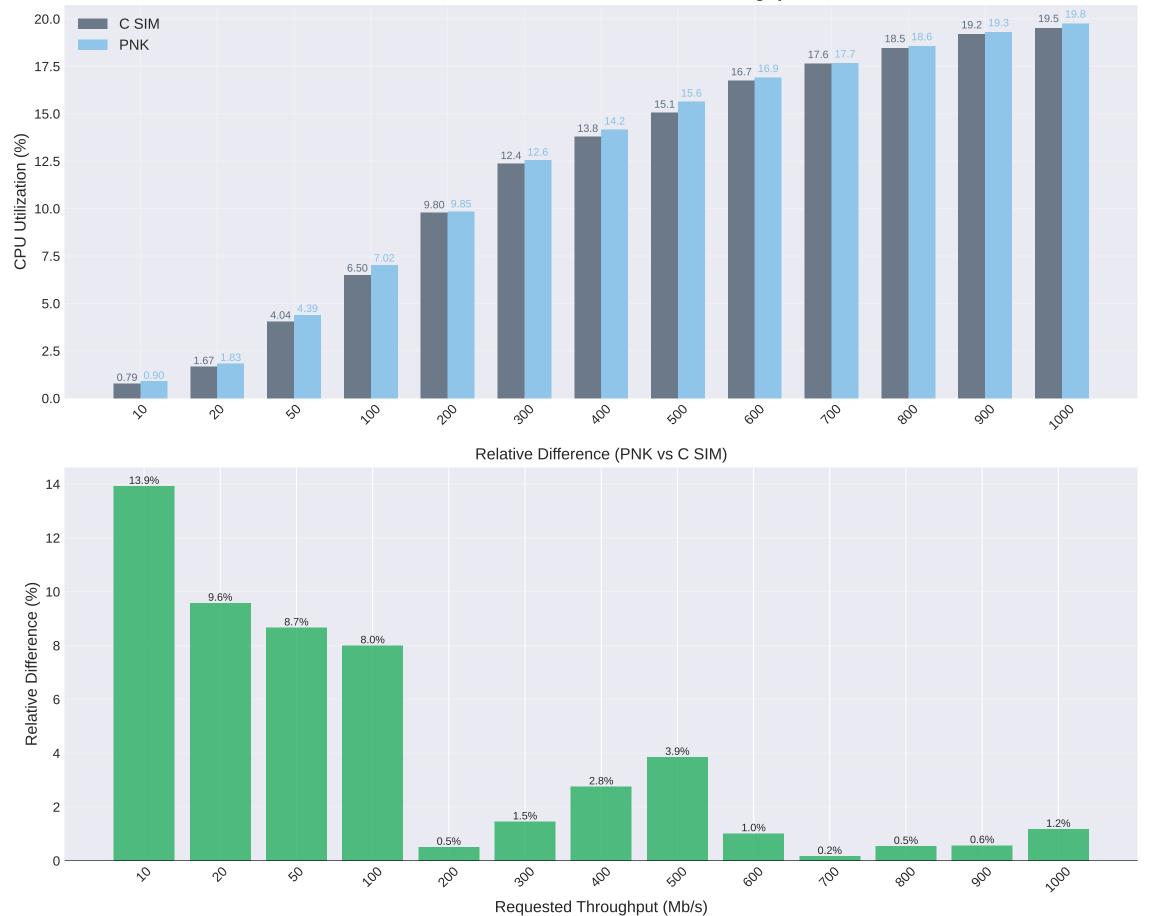
**Received Throughput vs Requested with CPU Utilization Overlay** 1000 C SIM Recv Throughput 957.3957.0 100 PNK Recv Throughput C SIM CPU Util 900.0900.0 PNK CPU Util 800.0800.0 800 80 700.0700.0 Received Throughput (Mb/s) 63.5% 61.3% 600.0600.0 600 CPU Utilization (%) 57.9% 54.2% 51.9% 500.0500.0 44.8% 400 300.0300.0 200.0200.0 200 20 100.0100.0 50.0 50.0 0 900 200 go NOO 400 2000 700 600 100 900 30 20 50

Requested Throughput (Mb/s)

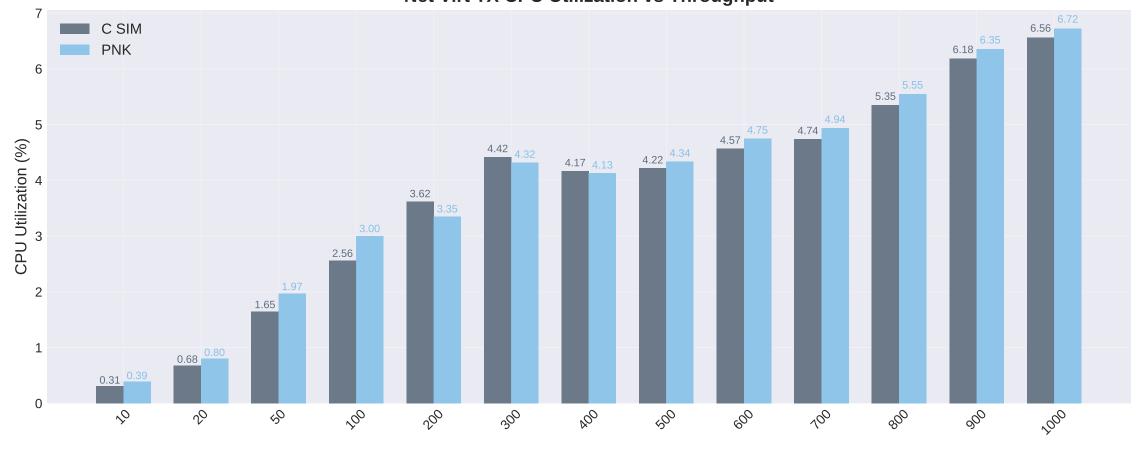
**Total System CPU Utilization vs Throughput** 

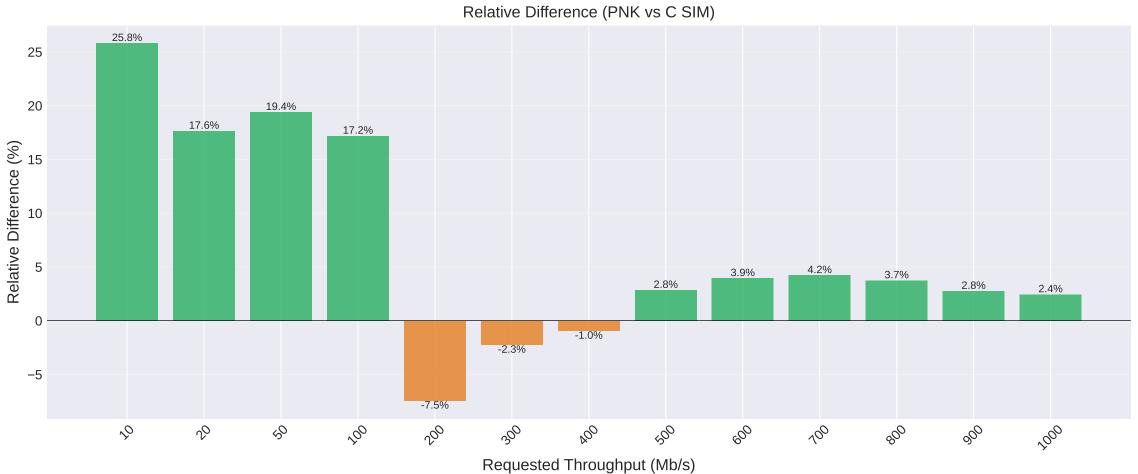


**Ethernet Driver CPU Utilization vs Throughput** 

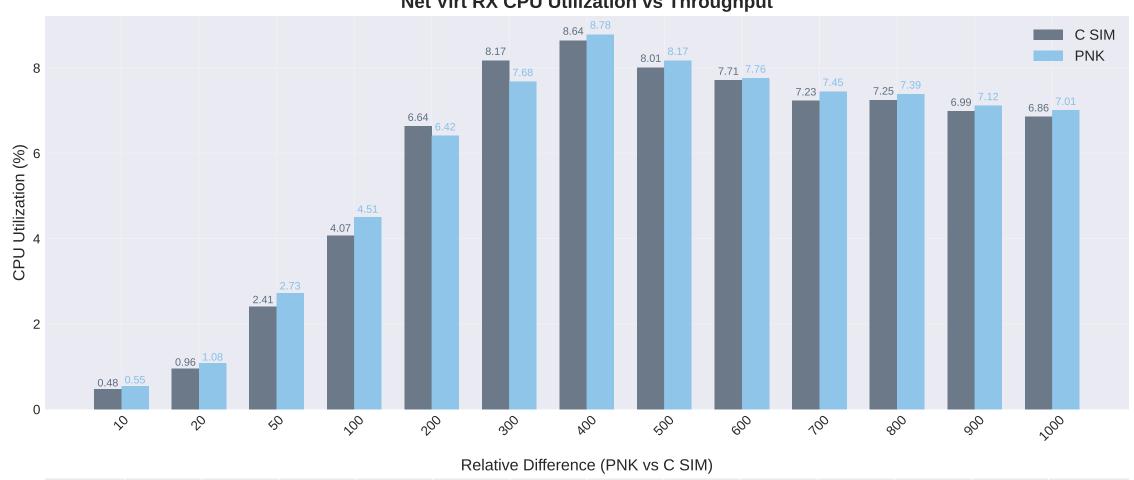


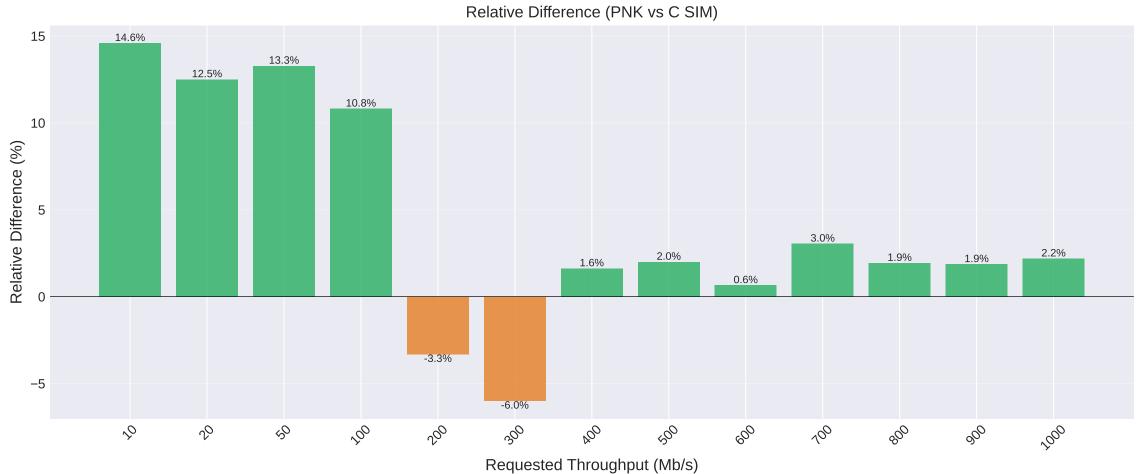




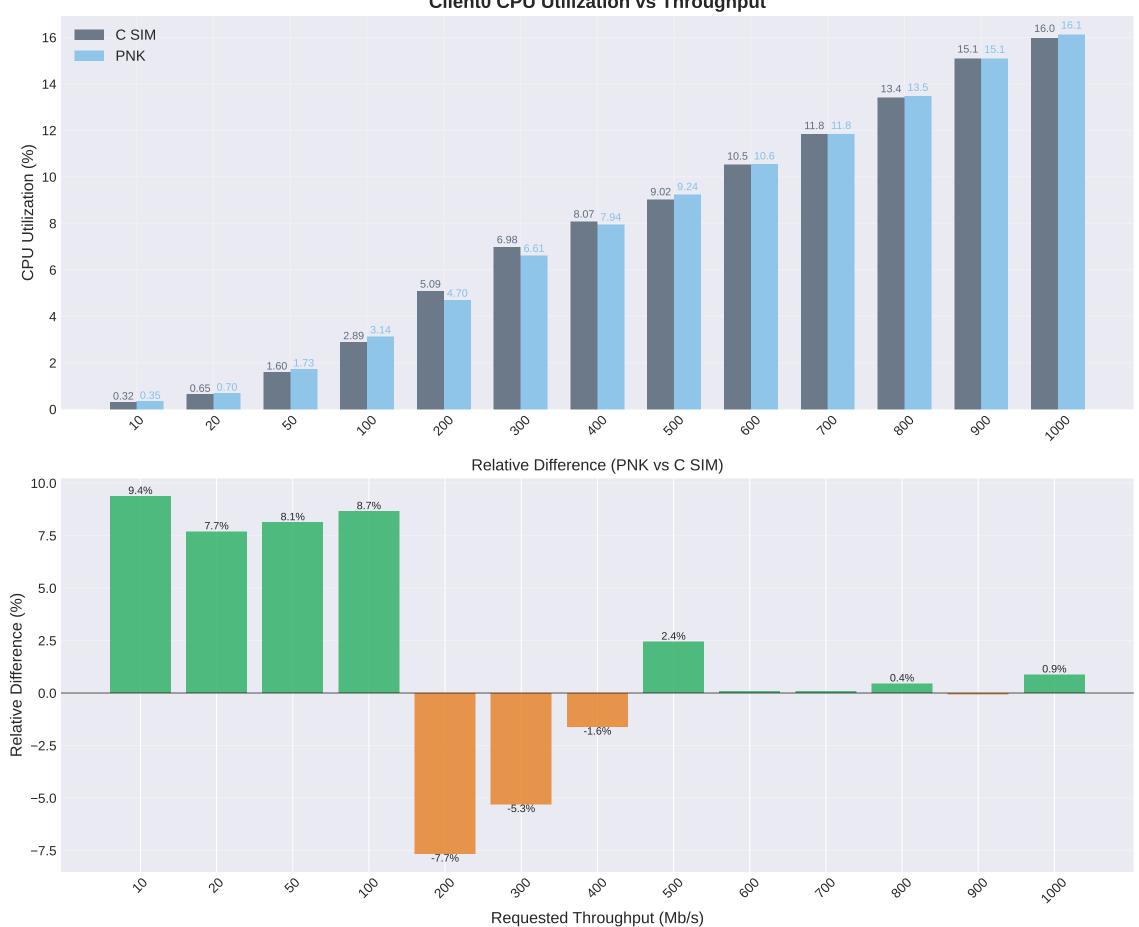


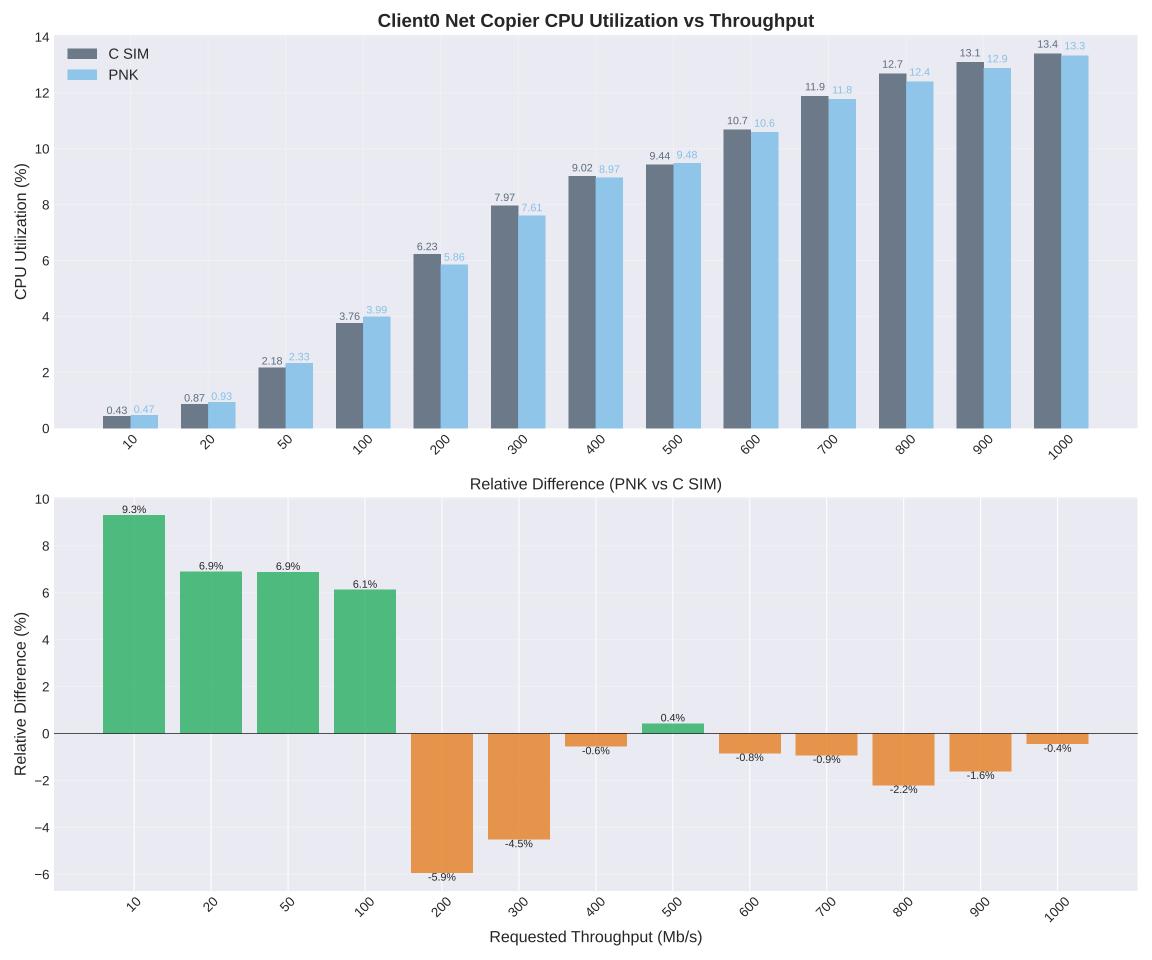
**Net Virt RX CPU Utilization vs Throughput** 



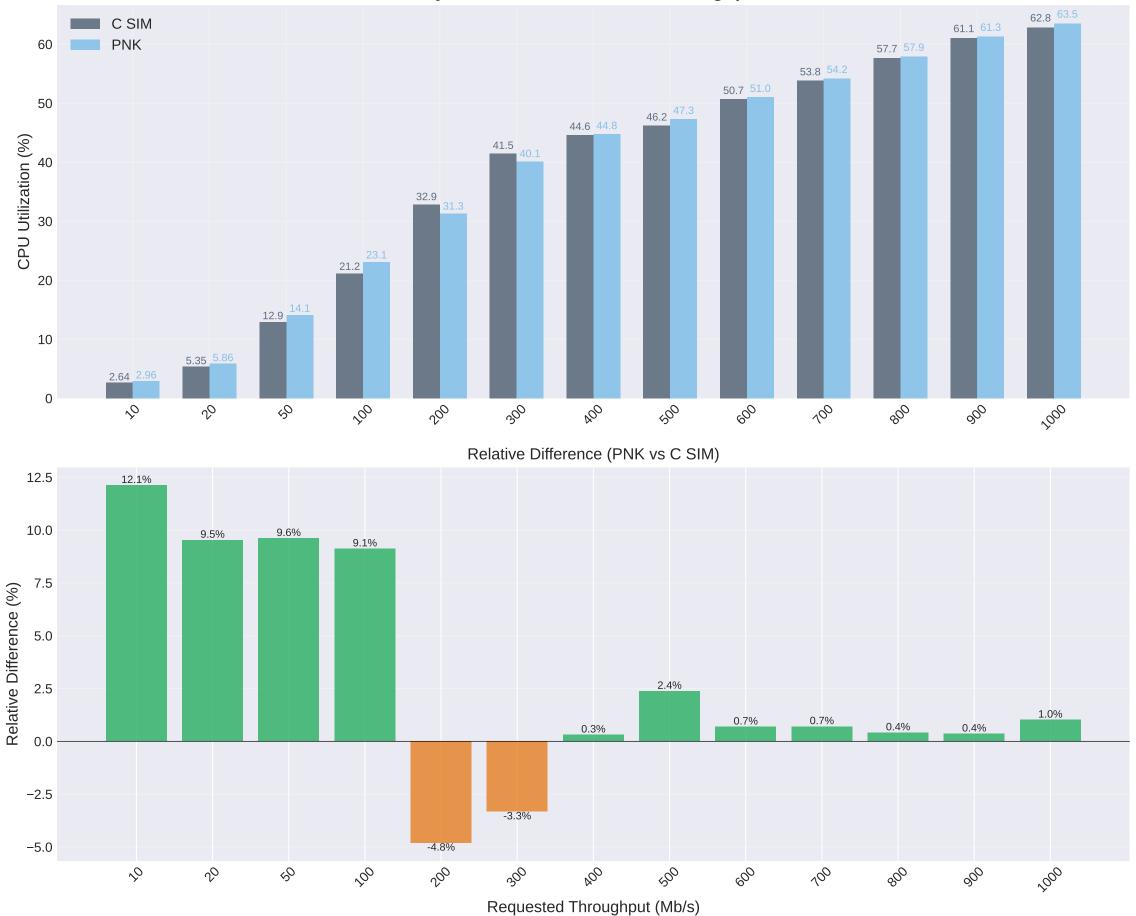


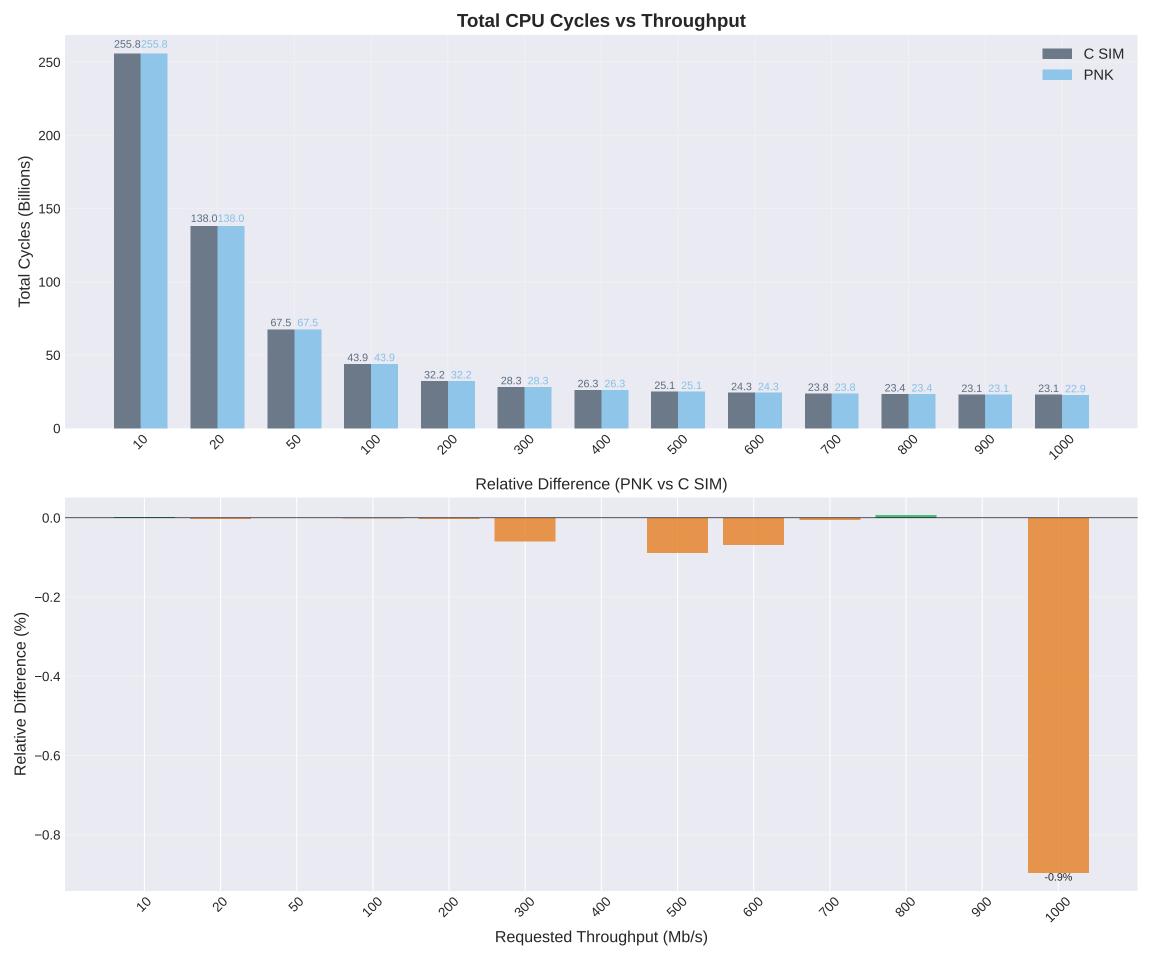
**Client0 CPU Utilization vs Throughput** 





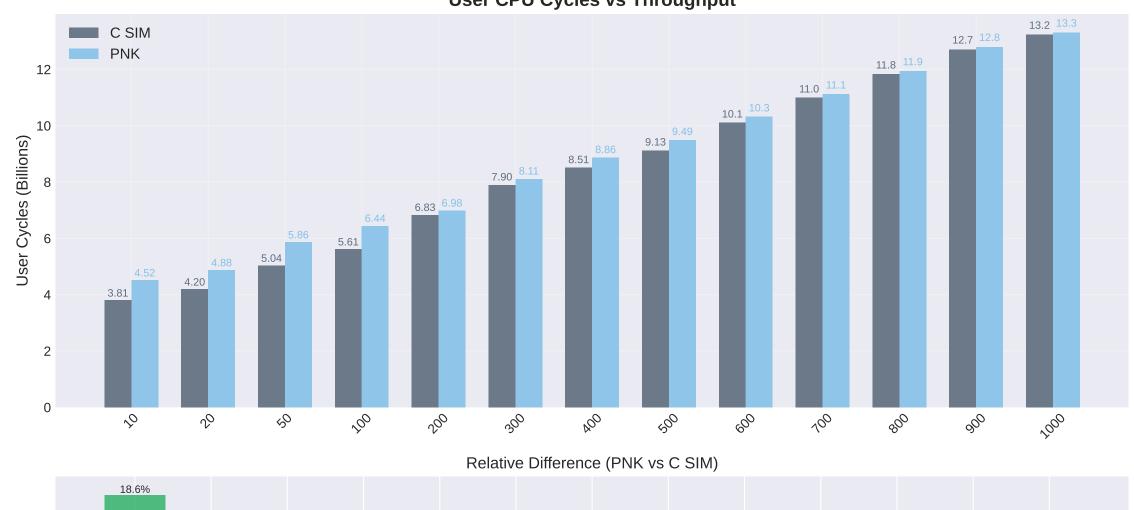
**System CPU Utilization vs Throughput** 

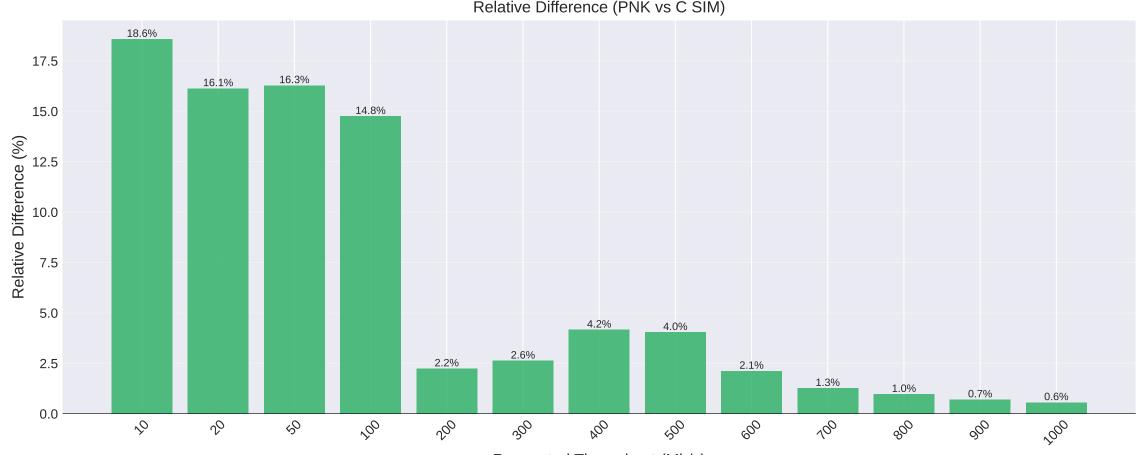




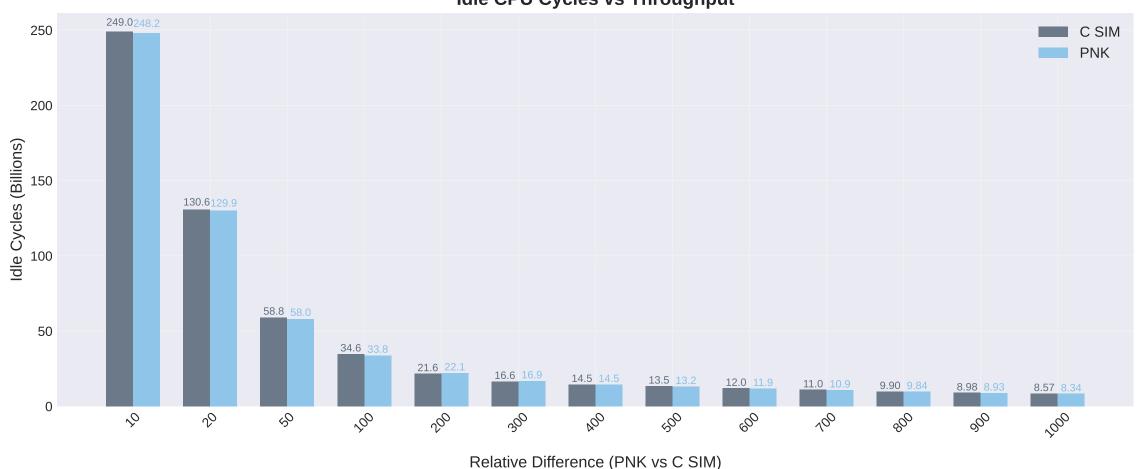
**Kernel CPU Cycles vs Throughput** 3.5 C SIM 3.30 PNK 3.02 3.07 3.10 3.09 2.99 3.0 2.76 2.52 2.55 Kernel Cycles (Billions) 1.5 1.0 2.36 2.26 2.10 1.73 1.55 1.27 1.15 0.5 0.0 200 200 300 400 400 600 700 800 900 2000 \$0 20 60 Relative Difference (PNK vs C SIM) 4.9% 5 1.5% 1.2% 0 -0.2% Relative Difference (%) -3.0% -3.3% -3.8% -4.0% -5.0% -6.6% -9.1% -15 -15.6% -16.4% 30 SO 200 200 300 NOO 500 600 100 900 20 Requested Throughput (Mb/s)

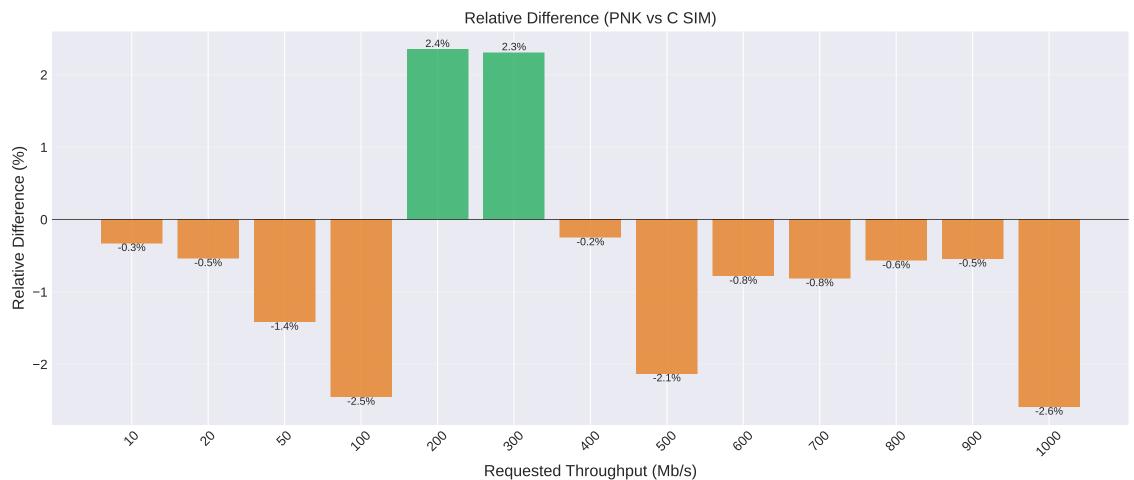
**User CPU Cycles vs Throughput** 



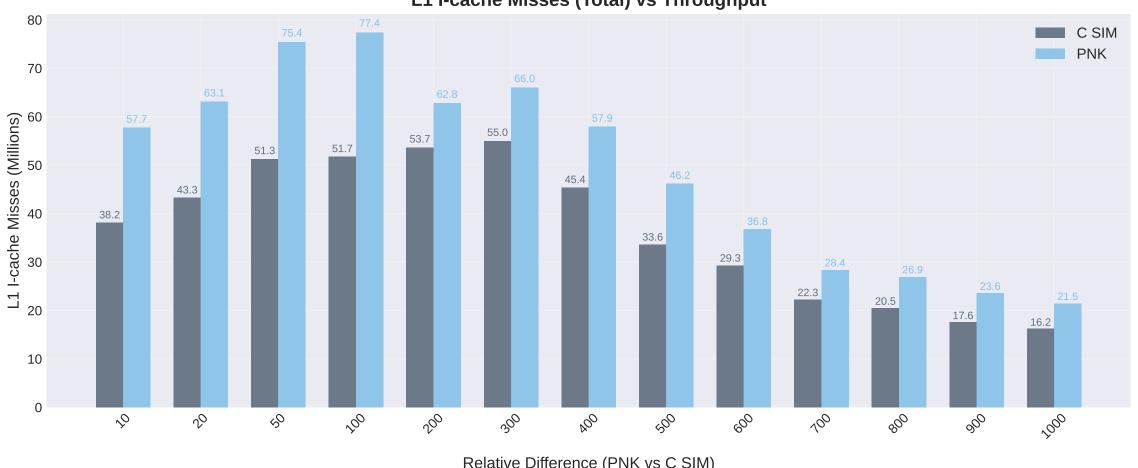


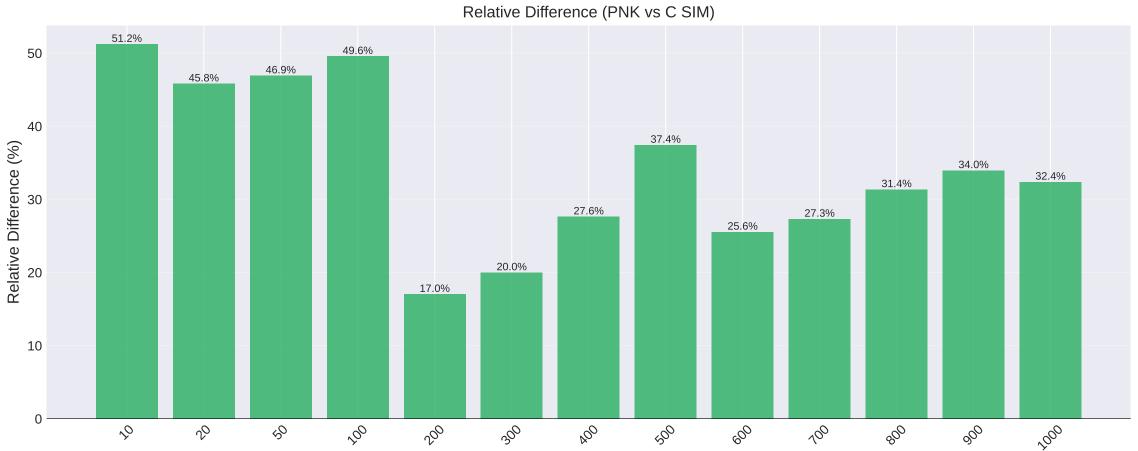
Idle CPU Cycles vs Throughput



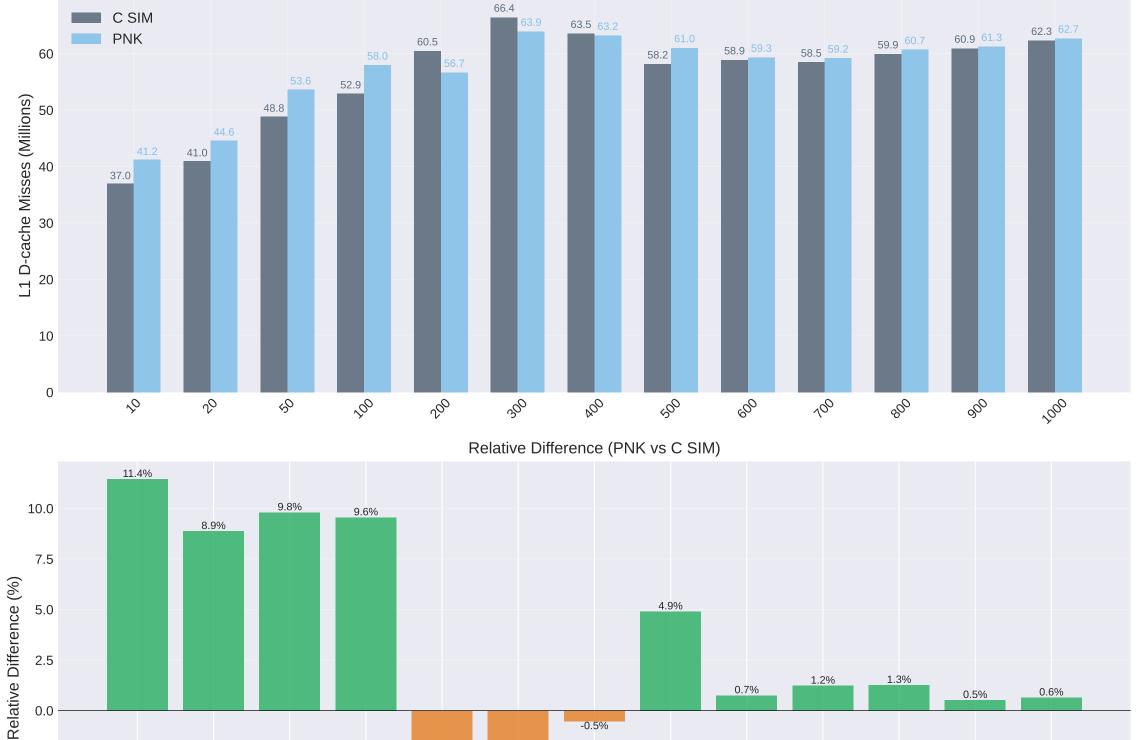


L1 I-cache Misses (Total) vs Throughput



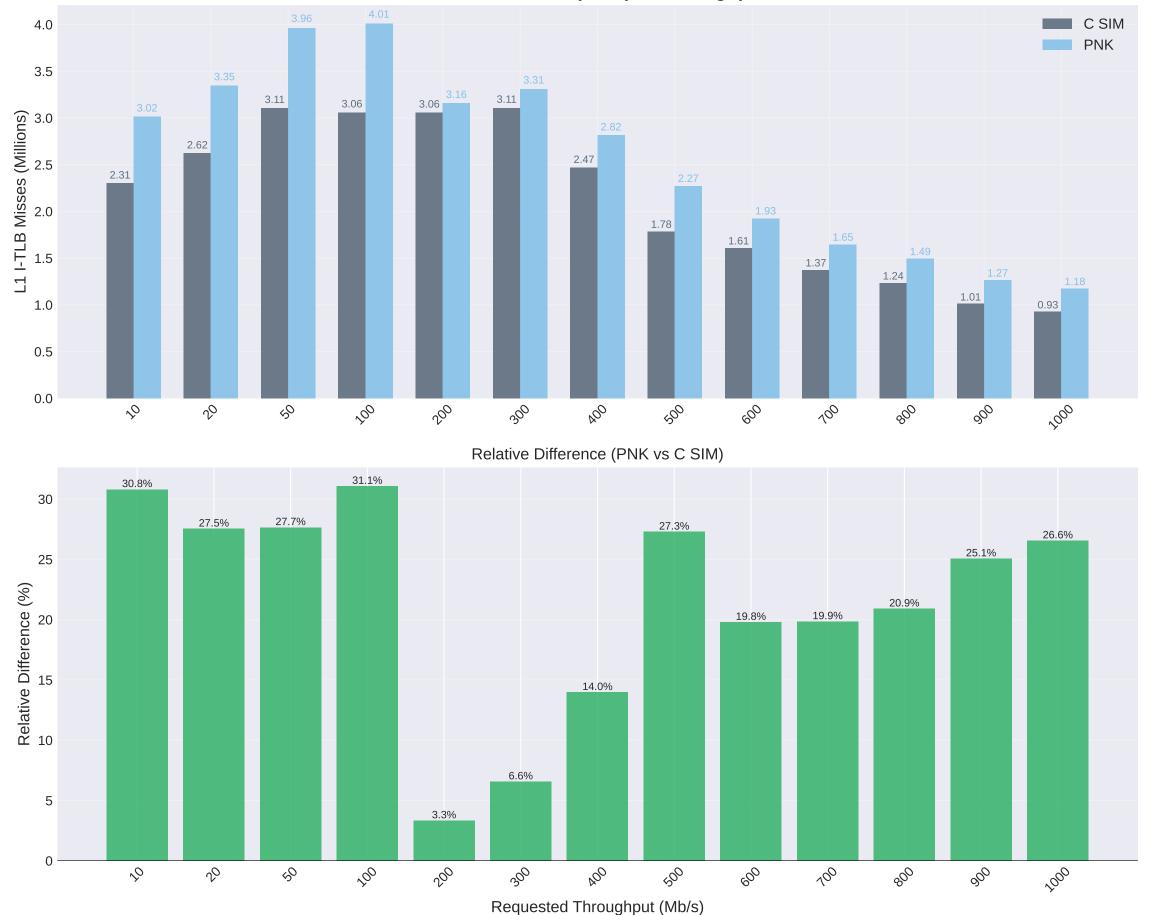


L1 D-cache Misses (Total) vs Throughput

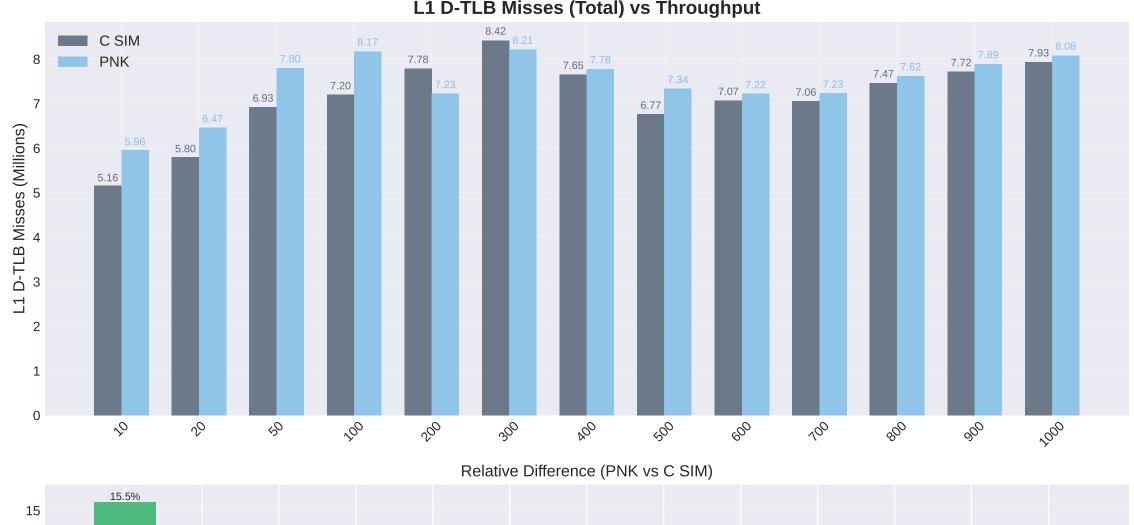


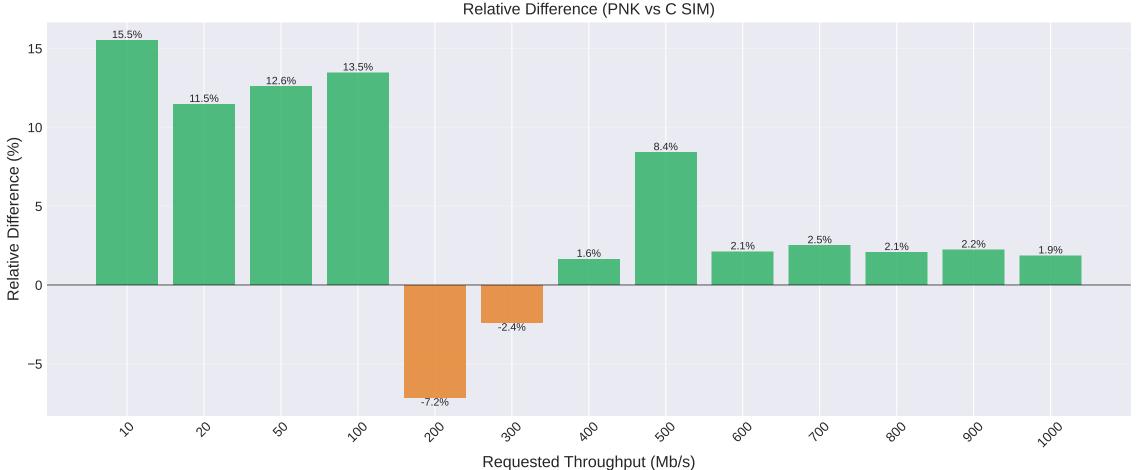
0.0 -0.5% -2.5 -3.7% -5.0 -6.2% 30 20 SO 200 200 300 NOO 500 600 100 900 900 Requested Throughput (Mb/s)

L1 I-TLB Misses (Total) vs Throughput

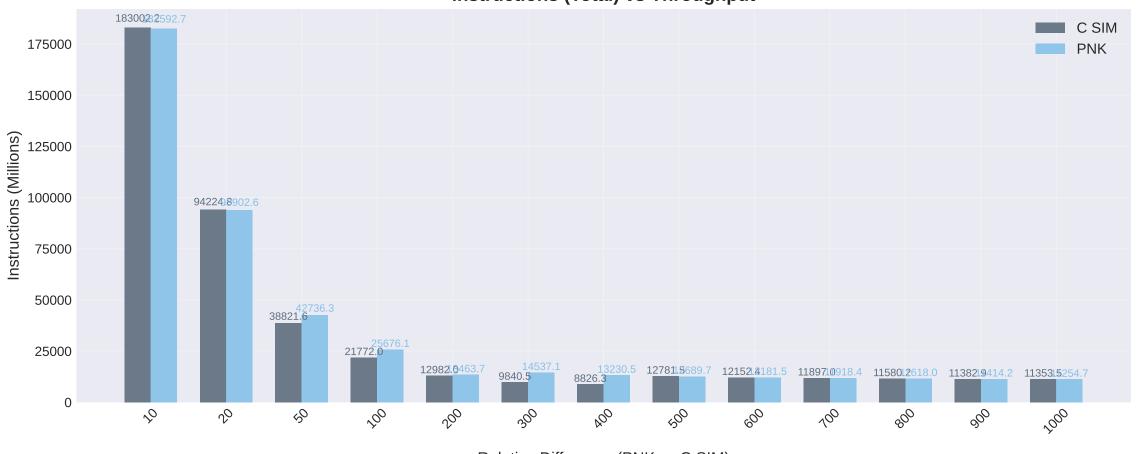


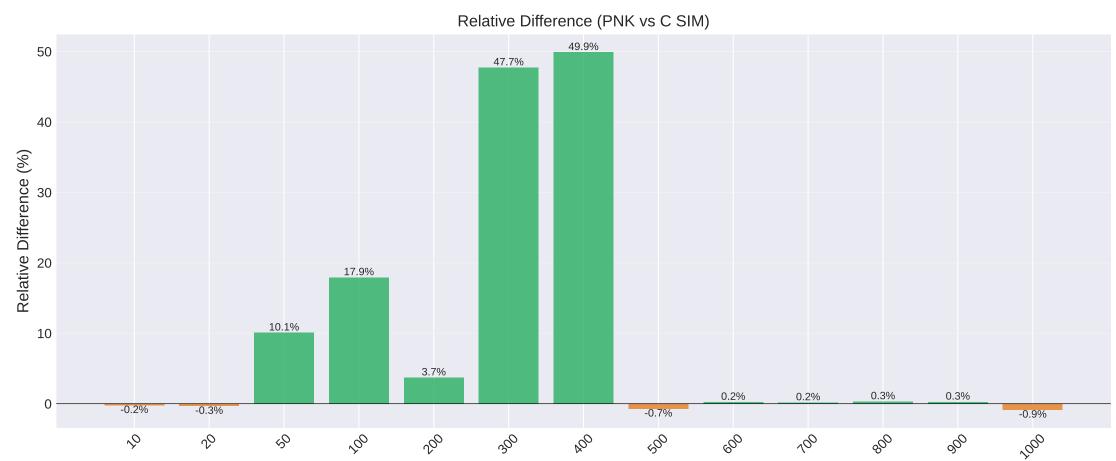
L1 D-TLB Misses (Total) vs Throughput



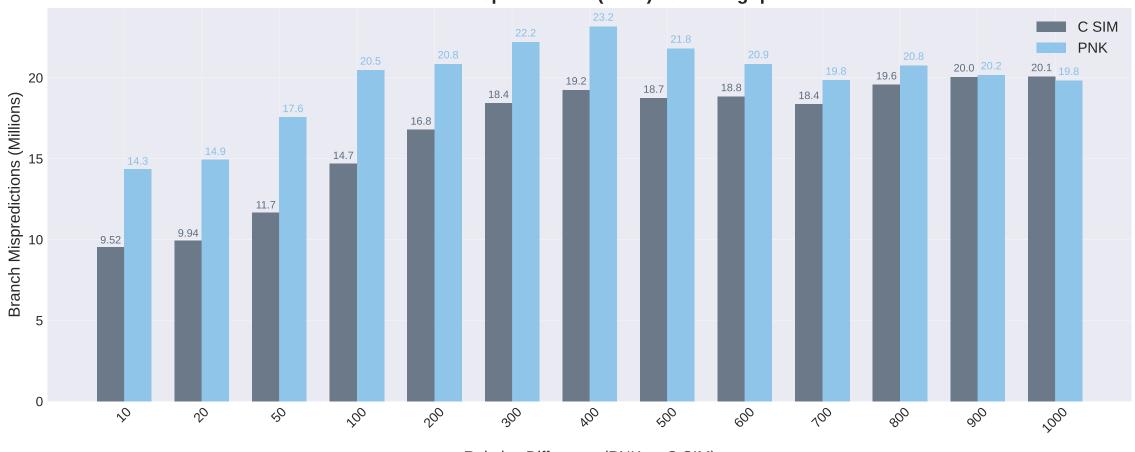


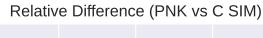


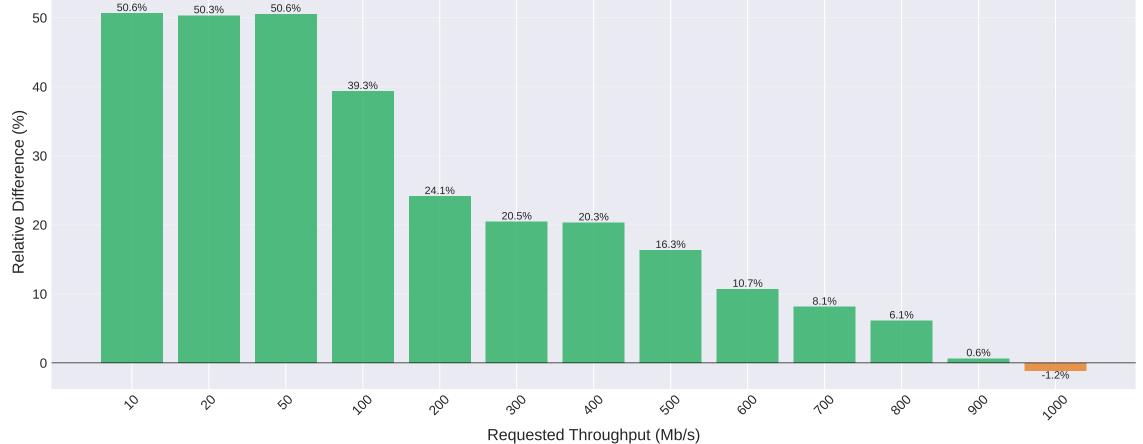




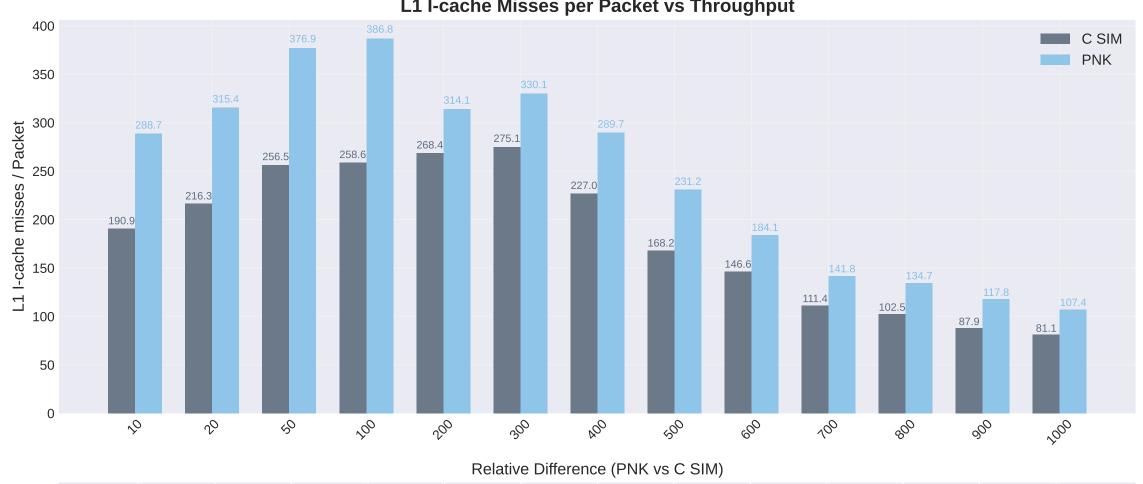
## **Branch Mispredictions (Total) vs Throughput**

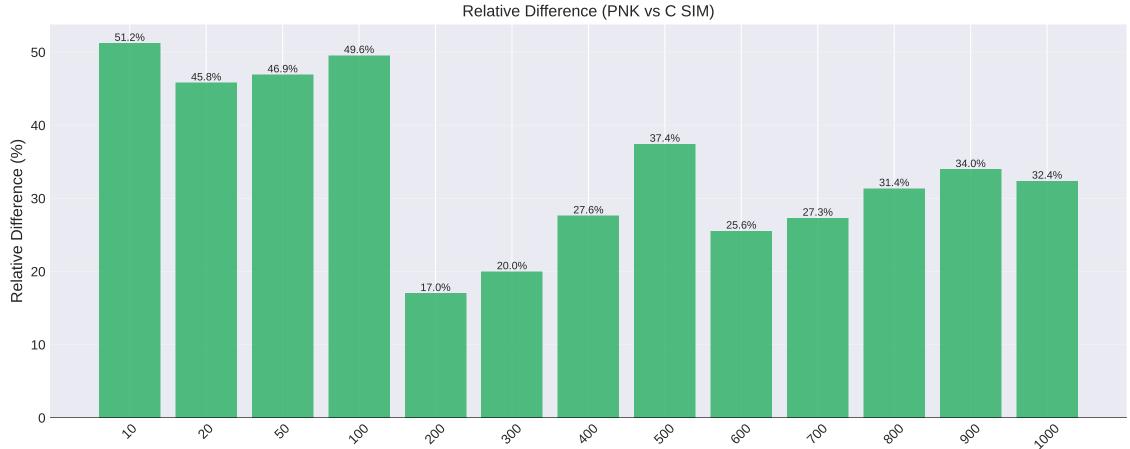


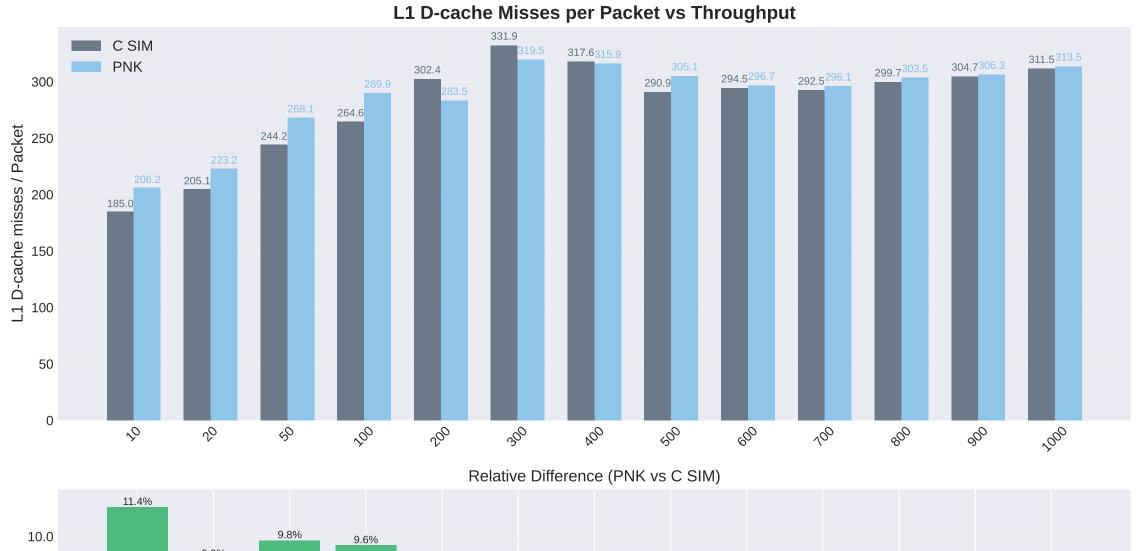


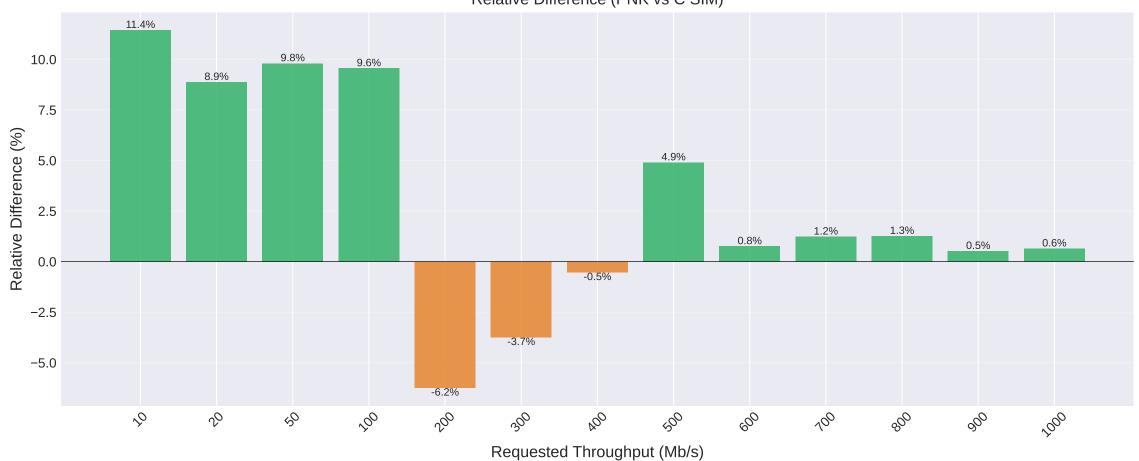


**L1** I-cache Misses per Packet vs Throughput

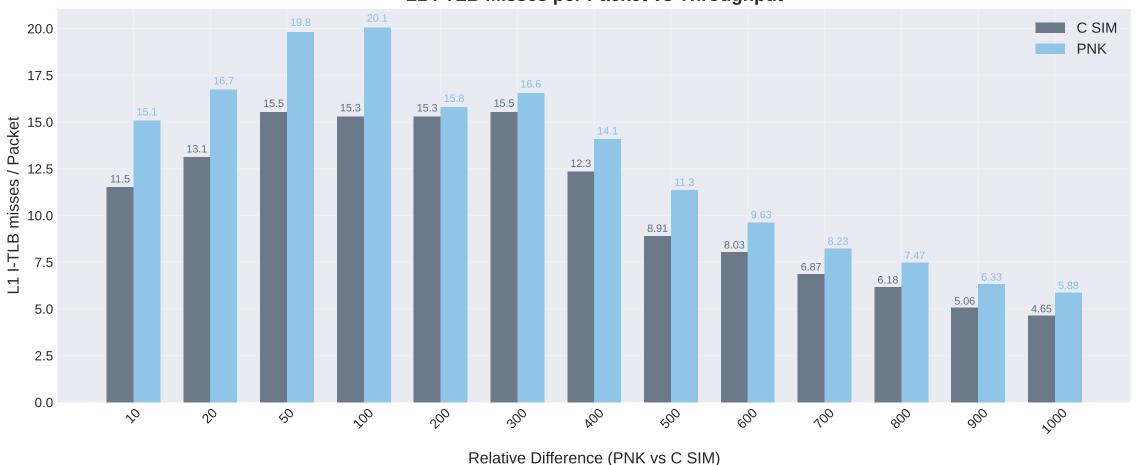


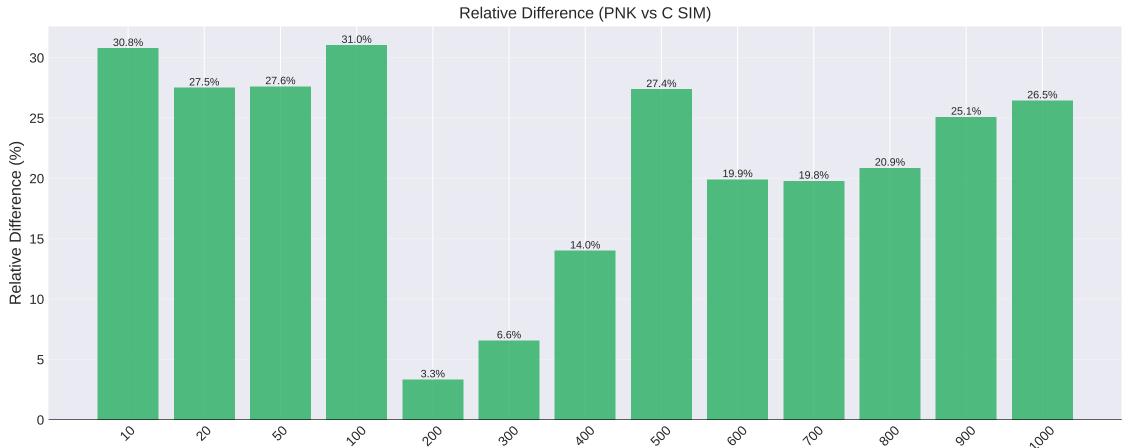




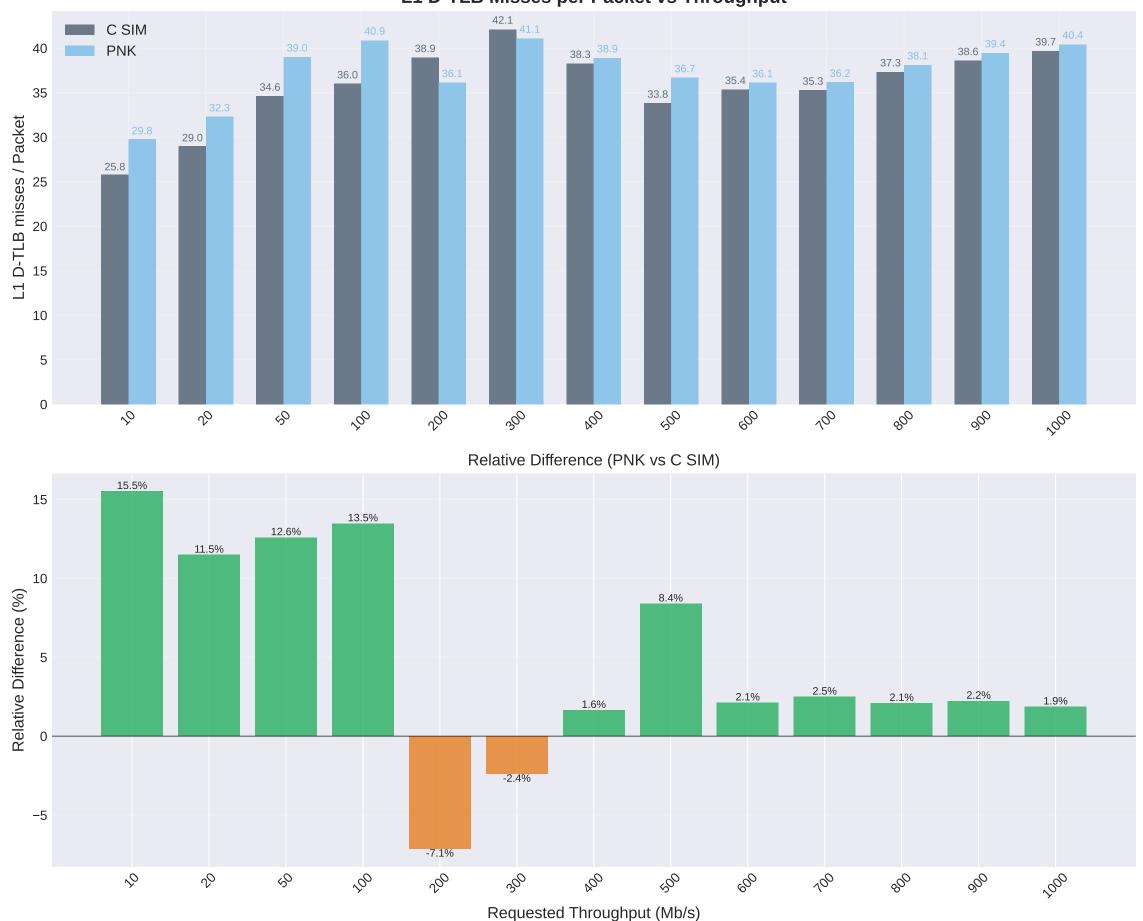


**L1 I-TLB Misses per Packet vs Throughput** 

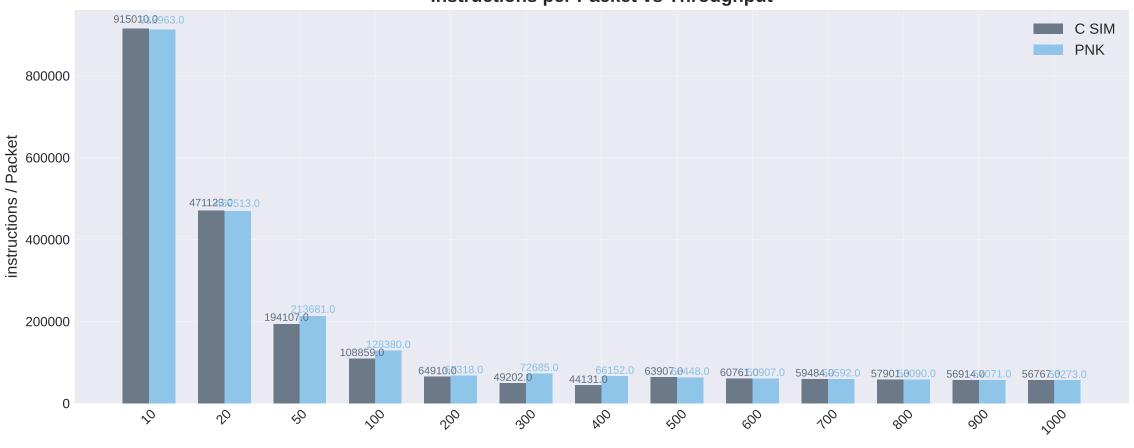


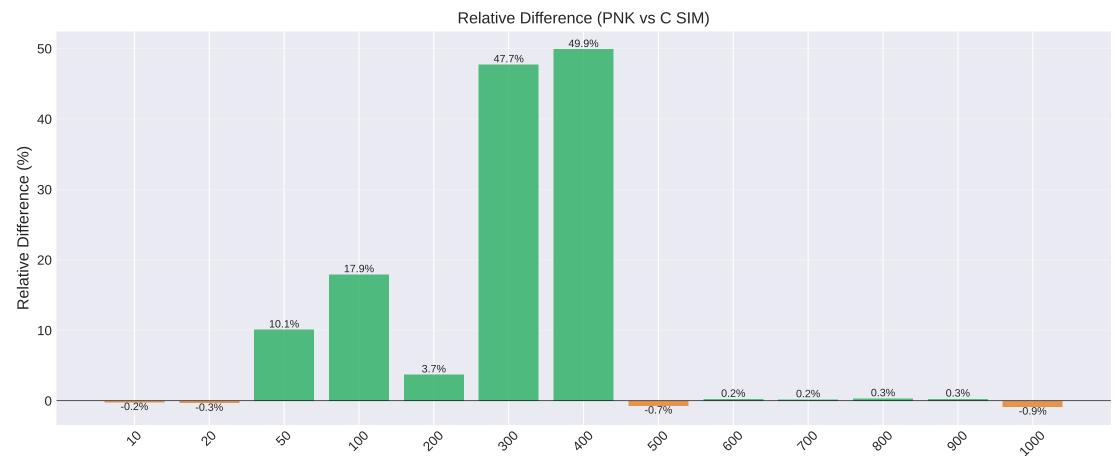


**L1 D-TLB Misses per Packet vs Throughput** 

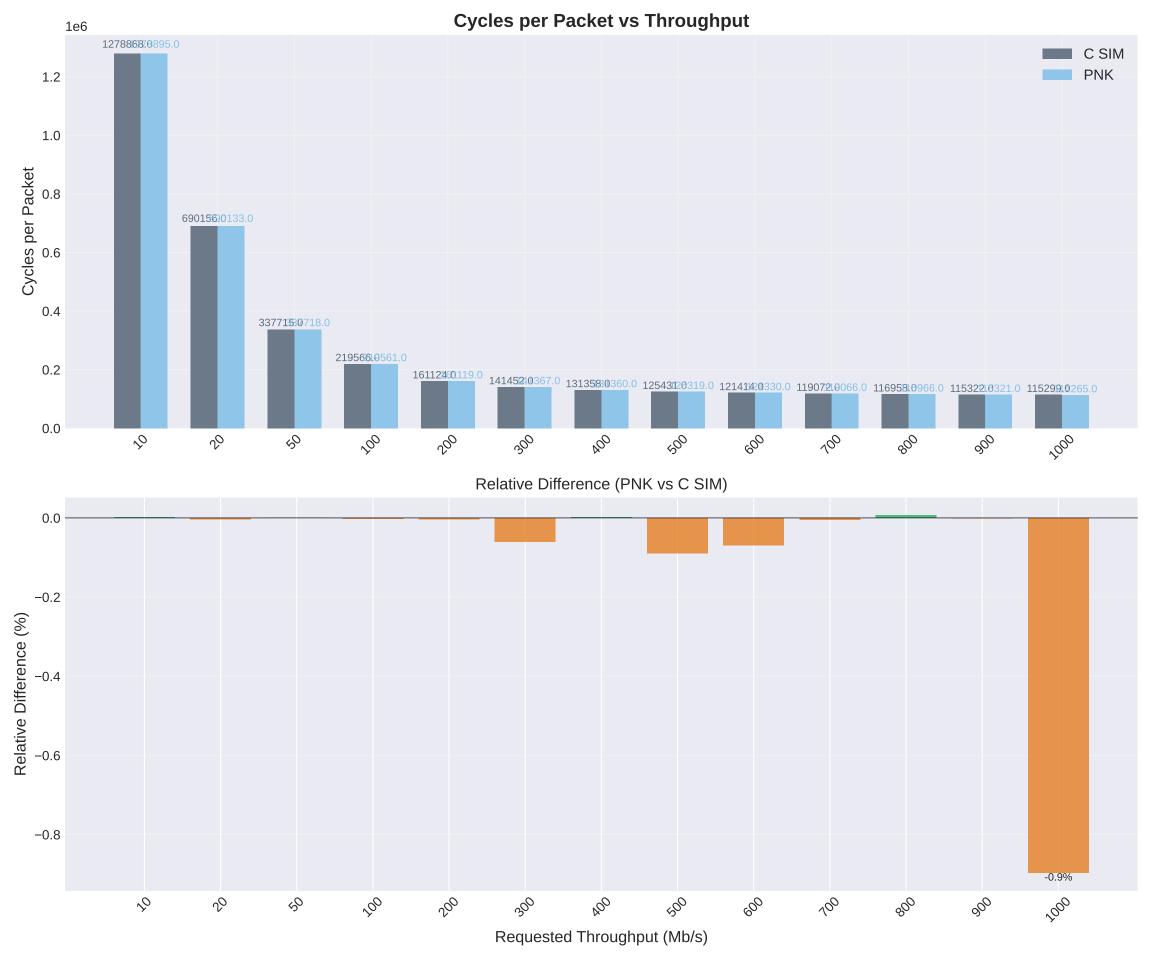


## Instructions per Packet vs Throughput

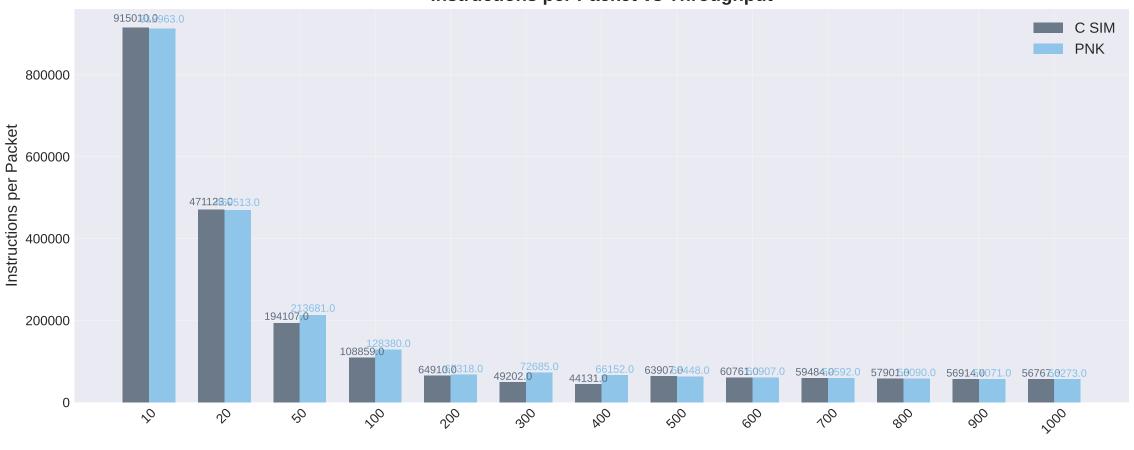


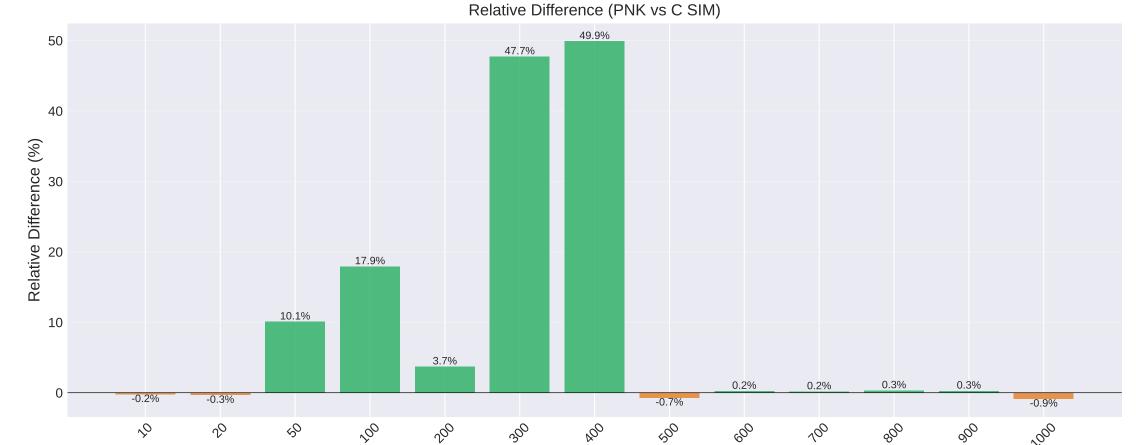


**Branch Mispredictions per Packet vs Throughput** 120 C SIM PNK 100.3 99.2 100.2100.9 99.2 97.8 100 96.2 94.2 93.7 92.1 91.8 87.8 Branch mis-pred / Packet 84.0 80 74.7 73.4 58.3 60 49.7 47.6 40 20 0 200 200 300 NOO 500 600 700 800 900 2000 20 20 50 Relative Difference (PNK vs C SIM) 50.7% 50.4% 50.5% 50 39.4% 40 Relative Difference (%) 24.1% 20.5% 20.3% 16.3% 10.7% 10 8.1% 6.1% 0.6% 0 -1.2% 30 20 SO 200 200 300 NOO 400 600 100 900 900 7000



## Instructions per Packet vs Throughput





**Branch Mispredictions per Packet vs Throughput** 120 C SIM PNK 100.3 99.2 100.2100.9 99.2 97.8 96.2 94.2 93.7 Branch Mispredictions per Packet 92.1 91.8 87.8 84.0 80 74.7 73.4 58.3 60 49.7 47.6 20 0 100 200 200 300 NOO 500 600 800 900 2000 20 20 50 Relative Difference (PNK vs C SIM) 50.7% 50.4% 50.5% 50 39.4% 40 Relative Difference (%) 24.1% 20.5% 20.3% 16.3% 10.7% 10 8.1% 6.1% 0.6% 0 -1.2%

30

SO

20

200

200

300

NOO

Requested Throughput (Mb/s)

500

600

100

900

900

7000





