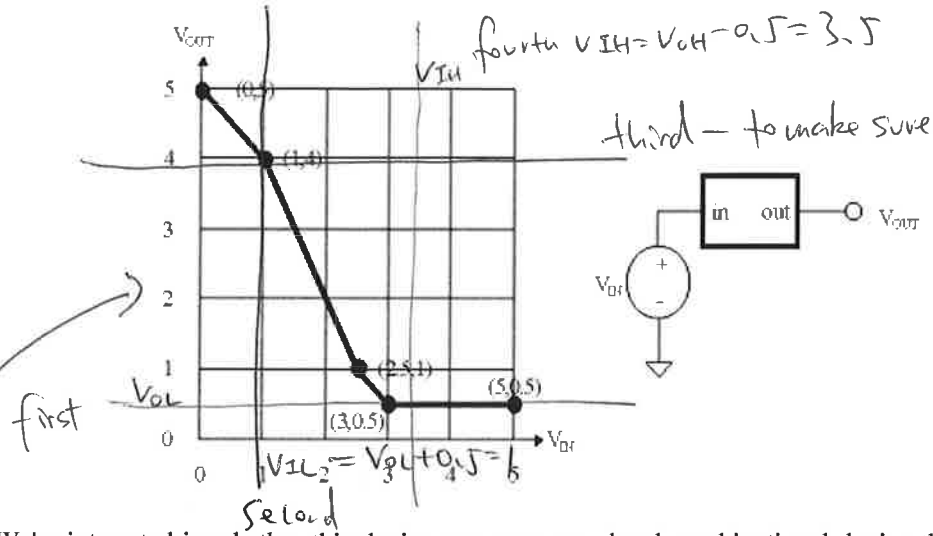
Problem 1. The behavior of a 1-input, 1-output device is measured by hooking a voltage source to its input and measuring the voltage at the output for several different input voltages:



fourth $V_{IH} = V_{OH} - 0.5 = 3.5$

third — to make sure valid 1 → valid 0 @ V_{OH} = 4

first

$V_{IL} = V_{OL} + 0.5 = 0.5$

second

We're interested in whether this device can serve as a legal combinational device that obeys the static discipline. For this device, obeying the static discipline means that

if $V_{IN} <= V_{IL}$ then $V_{OUT} >= V_{OH}$, and if $V_{IN} >= V_{IH}$ then $V_{OUT} <= V_{OL}$.

When answering the questions below, assume that all voltages are constrained to be in the range 0V to 5V.

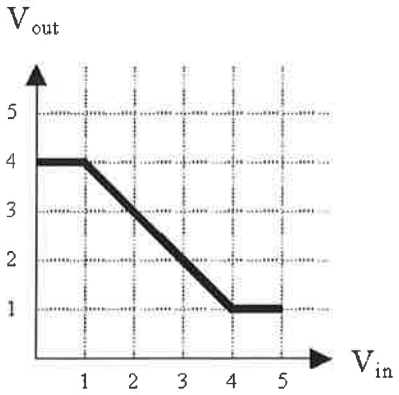
A. Can one choose a V_{OL} of 0V for this device? Explain. no, not reachable

B. What's the smallest V_{OL} one can choose and still have the device obey the static discipline? Explain. 0.5V, reachable

C. Assuming that we want to have 0.5V noise margins for both "0" and "1" values, what are appropriate voltage levels for V_{OL}, V_{IL}, V_{IH}, and V_{OH} so that the device obeys the static discipline. Hint: there are many possible choices, just choose one that obeys the constraints listed above. choose noise margin 0.5

Problem 2. Inverter madness.

A. The following graph plots the voltage transfer characteristic for a device with one input and one output.

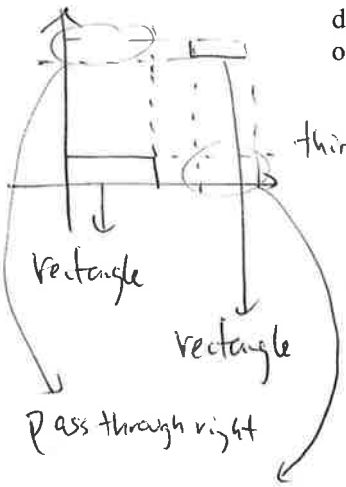


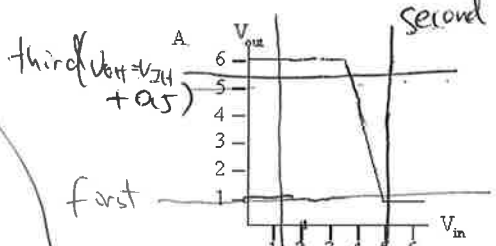
Can this device be used as a combinational device in a logic family with 0.75V noise margins?

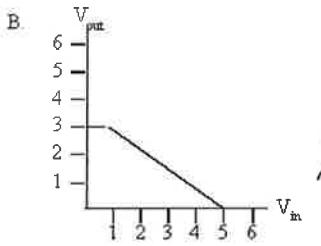
no.

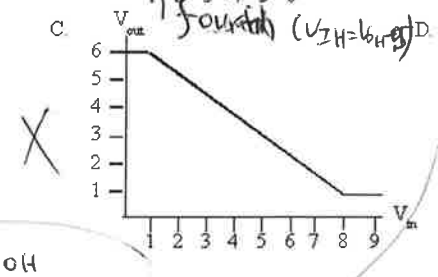
B. You are designing a new logic family and trying to decide on values of the four parameters V_{IL}, V_{OL}, V_{IH}, V_{OH} that lead to non-zero noise margins for various possible inverter designs. Four proposed inverter designs exhibit the voltage transfer characteristics shown in the diagrams below. For each design, either (1) specify suitable values of V_{IL}, V_{OL}, V_{IH}, V_{OH}. or (2) explain why no values for these parameters satisfy the static discipline.

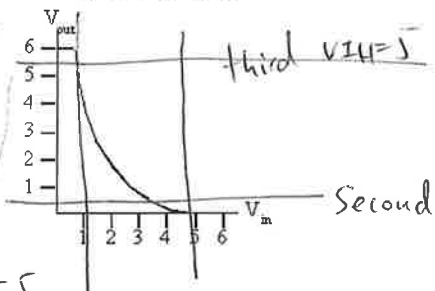
remember











$V_{IN} \geq V_{IH} \rightarrow V_{OUT} \geq V_{OH}$

$V_{OUT} < V_{OH} \rightarrow V_{IN} < V_{IH}$

$V_{IN} \leq V_{IL} \rightarrow V_{OUT} \leq V_{OL}$

$V_{OUT} < V_{OL}$

Problem 3. Static discipline.

A. Consider a combinational *buffer* with one input and one output. Suppose we set its input to some voltage (V_{IN}), wait for the device to reach a steady state, then measure the voltage on its output (V_{OUT}) and find $V_{OUT} < V_{OL}$. What can we say about V_{IN}?

$V_{OUT} < V_{OH} \rightarrow V_{IN} < V_{IH}$

B. Now consider an inverter. Suppose we set its inputs to some voltage (V_{IN}), wait for the device to reach a steady state, then measure the voltage on its output (V_{OUT}) and find $V_{OUT} > V_{OH}$. What can we say about V_{IN}?

$V_{OUT} > V_{OL} \rightarrow V_{IN} < V_{IH}$

$V_{IN} \leq V_{IL} \rightarrow V_{OUT} \geq V_{OH}$

$V_{IN} \geq V_{IH} \rightarrow V_{OUT} \leq V_{OL}$ $\rightarrow$ $V_{OUT} > V_{OL} \rightarrow V_{IN} < V_{IH}$