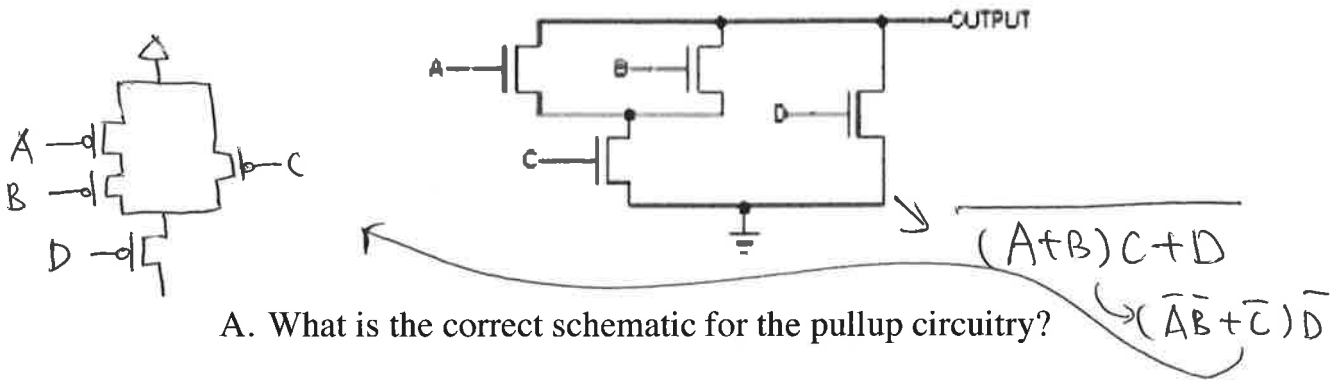
Problem 1. The following diagram shows a schematic for the pulldown circuitry for a particular CMOS gate:



A. What is the correct schematic for the pullup circuitry?

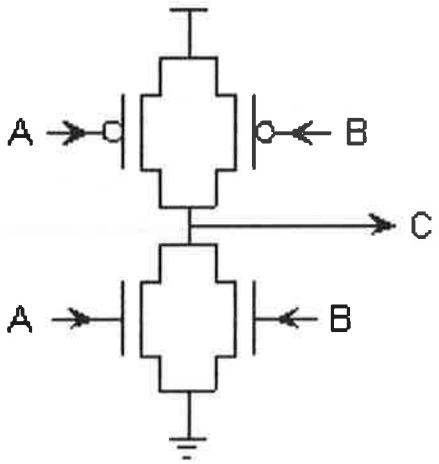
B. Assuming the pullup circuitry is designed correctly, what is the logic function implemented this gate?

C. Assuming the pullup circuitry is designed correctly, when the output of the CMOS gate above is a logic "0", in the steady state what would we expect the voltage of the output terminal to be? What would be the voltage if the output were a logic "1"?

→ 0

→ VDD

Problem 2. Anna Logue, a circuit designer who missed several early [redacted] 50.002 lectures, is struggling to design her first CMOS logic gate. She has implemented the following circuit:



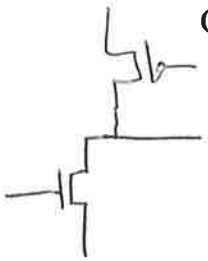
Anna has fabricated 100 test chips containing this circuit, and has a simple testing circuit which allows her to try out her proposed gate statically for various combinations of the A and B inputs. She has burned out 97 of her chips, and needs your help before destroying the remaining three. She is certain she is applying only valid input voltages, and expects to find a valid output at terminal C. Anna also keeps noticing a very faint smell of smoke.

A. What is burning out Anna's test chips? Give a specific scenario, including input values together with a description of the failure scenario. For what input combinations will this failure occur?

short circuit.

A=0, B=1 or A=1 B=0

B. Are there input combinations for which Anna can expect a valid output at C? Explain. A=1, B=1 A=0, B=0



C. One of Anna's test chips has failed by burning out the pullup connected to A as well as the pulldown connected to B. Each of the burned out FETs appears as an open circuit, but the rest of the circuit remains functional. Can the resulting circuit be used as a combinational device whose two inputs are A and B? Explain its behavior for each combination of valid inputs. Inverter

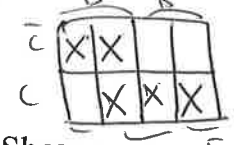
D. In order to salvage her remaining three chips, Anna connects the A and B inputs of each and tries to use it as a single-input gate. Can the result be used as a single-input combinational device? Explain.

Yes, Inverter.

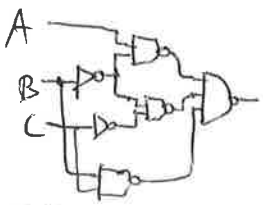
Problem 3. A certain function F has the following truth table:

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

$\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + ABC$



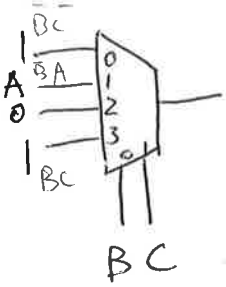
A. Write a sum-of-products expression for F.



B. Write a minimal sum-of-products expression for F. Show a combinational circuit that implements F using only INV and NAND gates.

$\bar{B}A + \bar{B}\bar{C} + BC$

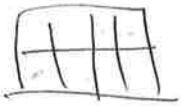
C. Implement F using one 4-input MUX and inverter.



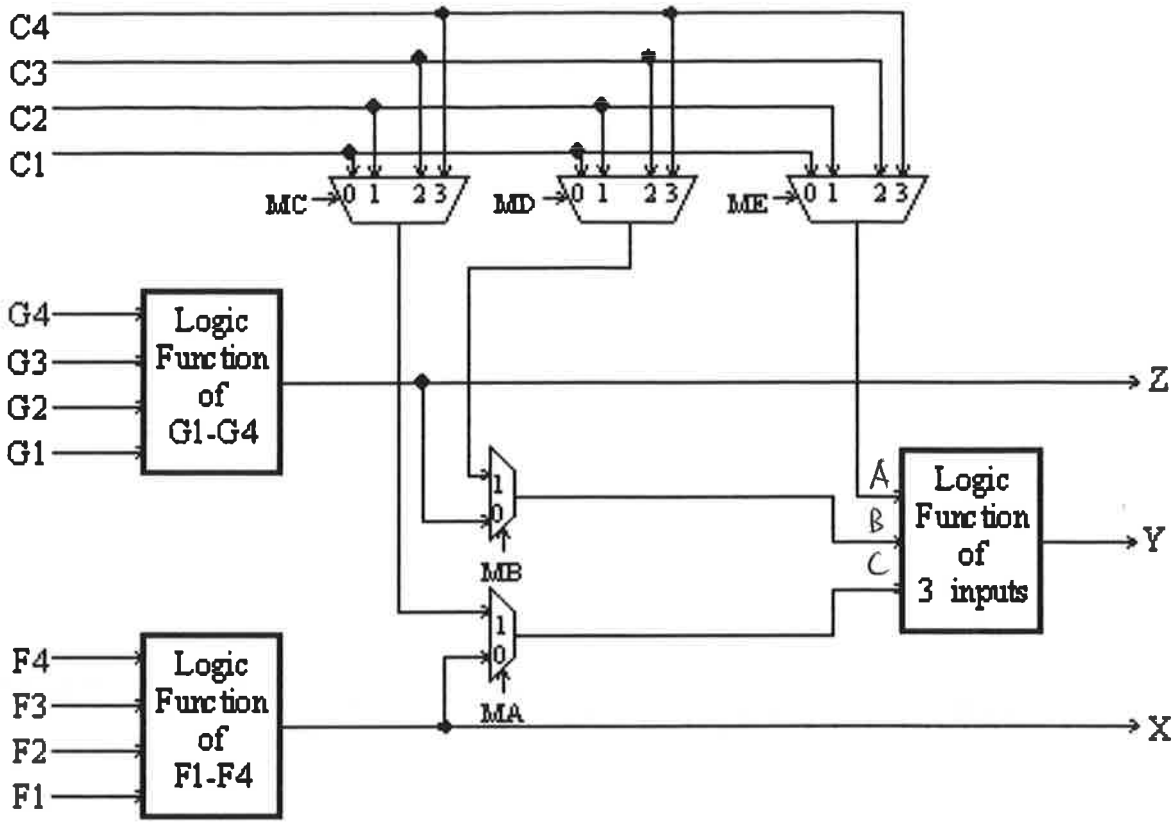
D. Write a minimal sum-of-products expression for NOT(F).

$\bar{A}\bar{B}C + \bar{A}B\bar{C} + AB\bar{C}$

$\bar{A}\bar{B}C + B\bar{C}$



Problem 4. The Xilinx 4000 series field-programmable gate array (FPGA) can be programmed to emulate a circuit made up of many thousands of gates; for example, the XC4025E can emulate circuits with up to 25,000 gates. The heart of the FPGA architecture is a configurable logic block (CLB) which has a combinational logic subsection with the following circuit diagram:



There are two 4-input function generators and one 3-input function generator, each capable of implementing an arbitrary Boolean function of its inputs.

The function generators are actually small 16-by-1 and 8-by-1 memories that are used as lookup tables; when the Xilinx device is "programmed" these memories are filled with the appropriate values so that each generator produces the desired outputs. The multiplexer select signals (labeled "Mx" in the diagram) are also set by the programming process to configure the CLB. After programming, these Mx signals remain constant during CLB operation.

The following is a list of the possible configurations. For each configuration indicate how each the control signals should be programmed, which of the input lines (C1-C4, F1-F4, and G1-G4) are used, and what output lines (X, Y, or Z) the result(s) appear on.

A. An arbitrary function F of up to four input variables, plus another arbitrary function G of up to four unrelated input variables, plus a third arbitrary function H of up to three unrelated input variables.

X=F Z=G Y=H → MC=1 MD=2 ME=3 MA=1 MB=1

B. An arbitrary single function of five variables.

G1/F1 G2/F2 G3/F3 G4/F4 C1

↓

Y → MA=0 MB=0 ME=0 Y=MUX(A=0→B A=1→C)

G1-G4, C1, C2 → F

C. An arbitrary function of four variables together with some functions of six variables. Characterize the functions of six variables that can be implemented. MA=1 MB=0 MC=0 ME=1 Y(Z(G1-G4), C1, C2)

D. Some functions of up to nine variables. Characterize the functions of up to nine variables that can be implemented.

E. [Optional challenge] Can every function of six inputs be implemented? If so, explain how. If not, give a 6-input function and explain why it can't be implemented in the CLB.

no.

6 input

Y(X(F1-F4), C1, C2)

we must be able to factor out 4 variables.

F1-F4, G1-G4, C1 → MA=0 MB=0 ME=0, Y(X(F1-F4), Z(G1-G4), C1)

Counter: $Y = ABCD\bar{E} + ABCDF + ABCEF + ABDEF + ACDEF + BCDEF$