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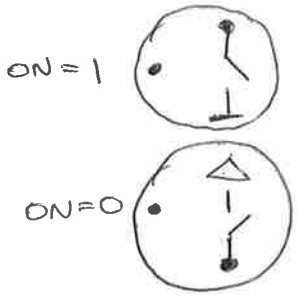
Computation Structures 2014. Yue Zhang

S4
- ☐ Designing gates using CMOS
- ☐ Simplifying gate circuits using Karnaugh maps
- ☐ mux and ROM

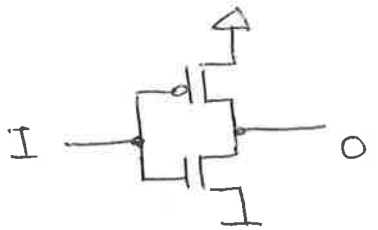
• Designing gates using CMOS

- NFET = PULL DOWN 
  PFET = PULL UP 

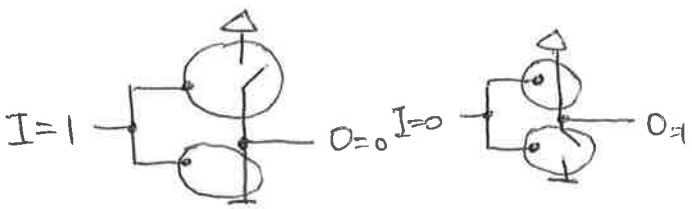
- The two types of MOSFETS serve as switches



- The two switches complement each other



inverter



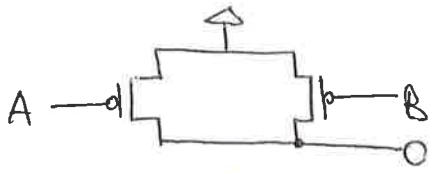
- All CMOS components have a pull up part and a pull down part. Pull-up NFETS only, pull down PFETS only!
- Switches have connections with logic

parallel ↔ OR 

cascade ↔ AND 

- Use the connection to build more complex pull up and pull down elements.

parallel ↑
(must be NFETs)



PARALLEL ($\bar{A}$, $\bar{B}$)

↓

O=1 when A=0 or B=0 → $\bar{A}+\bar{B}$

↓

De Morgan's Law

↓

complement? ← $\overline{AB}$ ← O=0 when A=1 and B=1

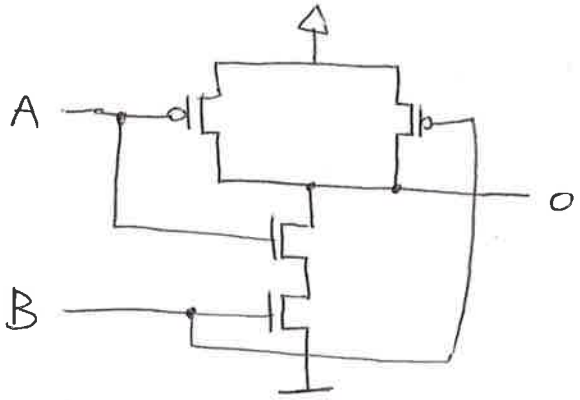
↓

parallel ↓
(must be PFETS)

$\overline{\text{CASCADE}(A,B)}$

↓

This is the rule of translating logic to circuit



$O = \bar{A}+\bar{B} = \overline{AB}$

(NAND gate)

Q: how to make CMOS AND gate? / A or $\overline{B \text{ and } C}$

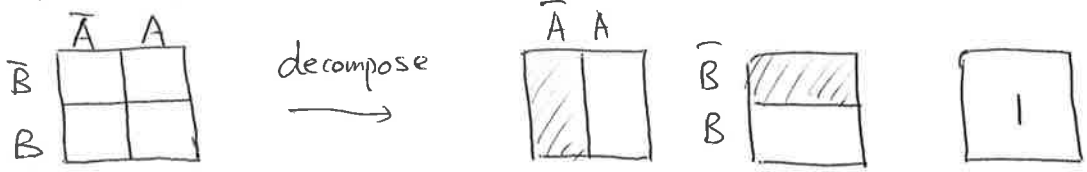
Should know how to translate circuit to logic

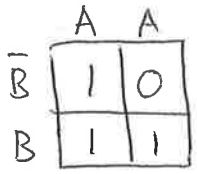
- NAND gate is universal — AND. OR. NOT.

Simplifying gate circuits using Karnaugh maps

- We have learned using algebra to simplify circuits
- a more intuitive method uses graphs
- Karnaugh maps { advantage: simple
  disadvantage: only works for 2–5 inputs

- 2 input case

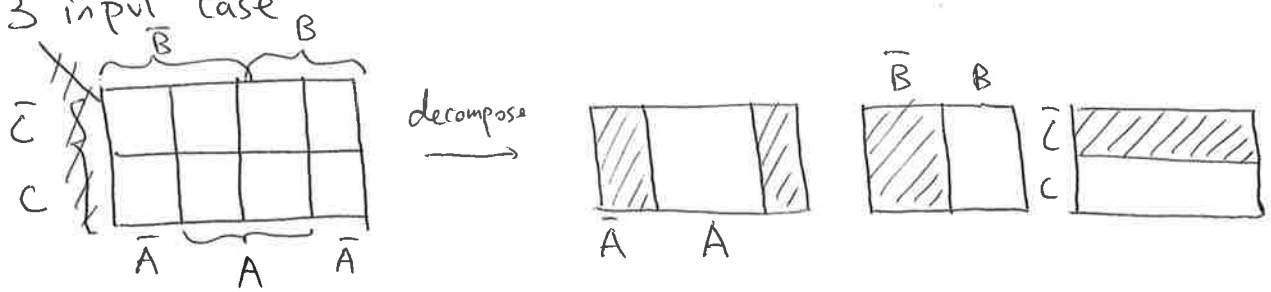


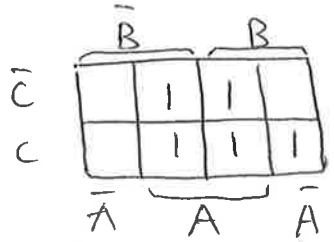


complex → $\bar{A}\bar{B} + \bar{A}B + AB$

Simple → $\bar{A} + B$

- 3 input case

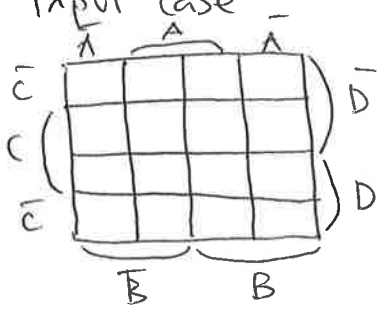


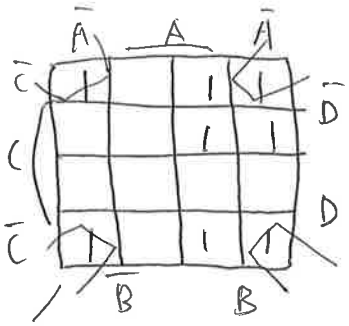


complex → $A\bar{B}\bar{C} + AB\bar{C} + A\bar{B}C + ABC + \bar{A}BC$

Simple → $A + BC$

- 4 input case





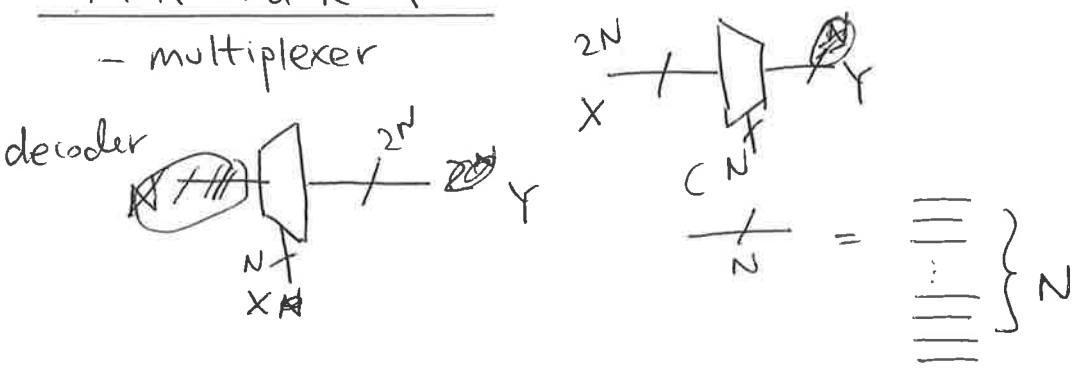
$B\bar{D}$

$\bar{A}\bar{C}$

$B\bar{C}$

• MUX and ROM

- multiplexer

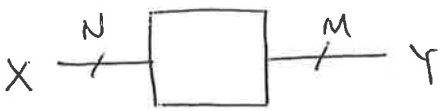


The (2^{i-1})th output

$$Y_{(2^{i-1})} = \bar{X}_0 \bar{X}_1 \cdots \bar{X}_{i-1} X_i \bar{X}_{i+1} \cdots X_N$$

(one-hot)

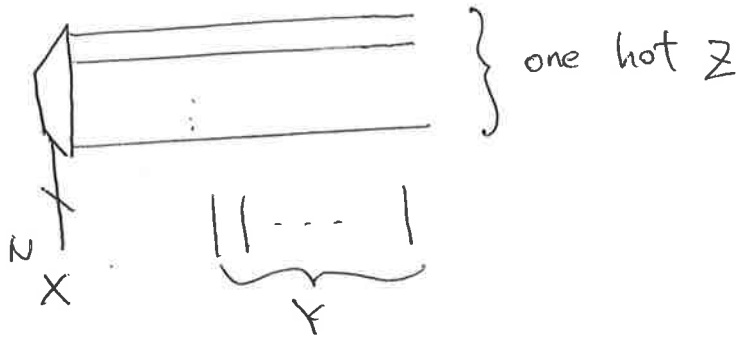
- ROM



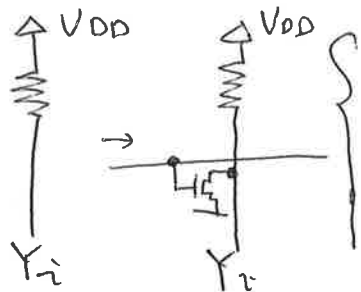
X is address $0 \sim 2^N$

Y is data item

- ROM can be made of ~~MUX~~ decoder.



how to connect Y & Z



without external signal $Y_i = 1$

what if $Y_i = 0$? use pull-down, driven by default 0? negate $\overline{Z}$ $\overline{Y_i}$