Computation Structures 2014. Yue Zheng

S2
- [ ] recap
- [ ] how to represent 0/1 in a circuit
- [ ] voltage transfer curves for devices and components
- [ ] MOSFETs and CMOS technology.
- [ ] contamination delay, propagation delay.

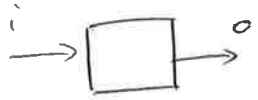
• Recap

- We will learn two types of digital circuits

  combinational logic: e.g. adder; rom; given student ID, get score

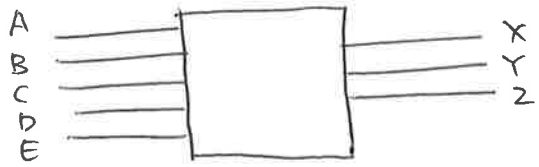
  sequential logic: e.g. a computer.

  Both take integer inputs, and yield integer outputs. The difference is instance vs. sequence.



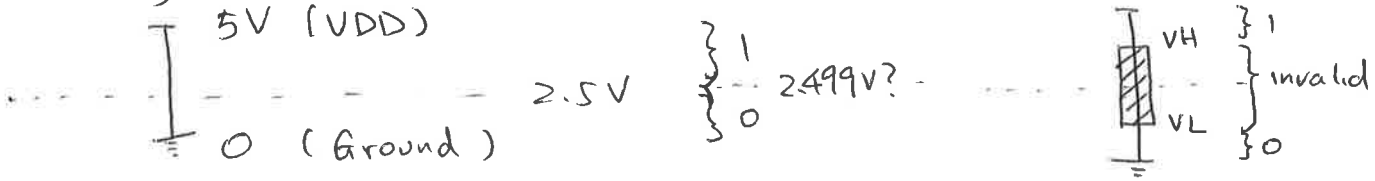
- Both inputs and outputs are represented by binary numbers, representing abstract information (bits).
- The advantage of abstract information representation in the digital abstraction is that it is easy to record and transfer without noise.
- The abstract information is powerful — it can be interpreted as any physical presentation: sounds, images, videos, robotic movement, temperature, floats...
- The 2's complement form of integer representation is commonly used.

· How to represent bits in a circuit?

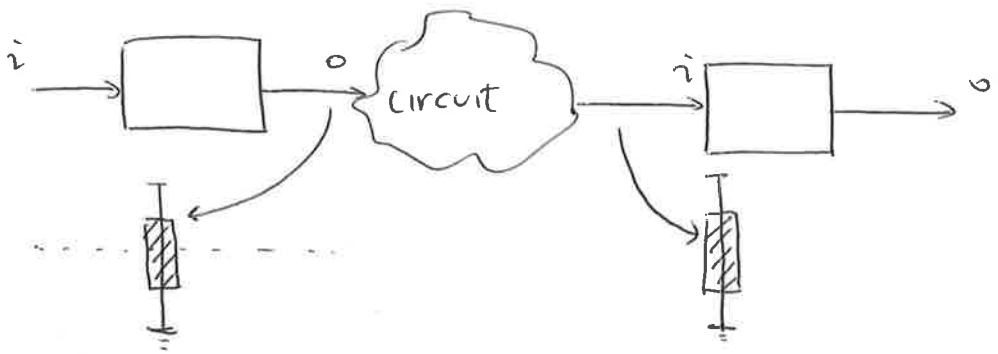


Zoom in

- how many integers can the input represent?
- each line is a wire
- a most intuitive way to encode 0/1 — voltage.
- Theory



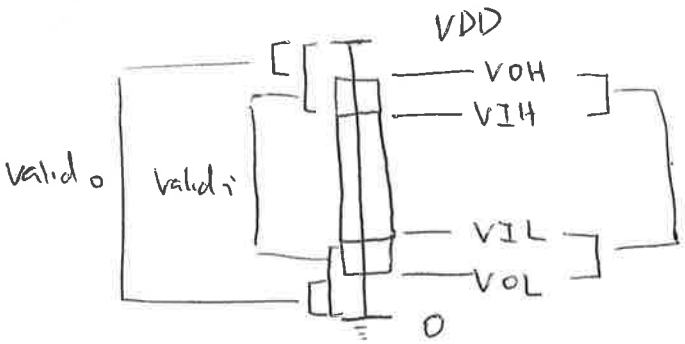
- Practice



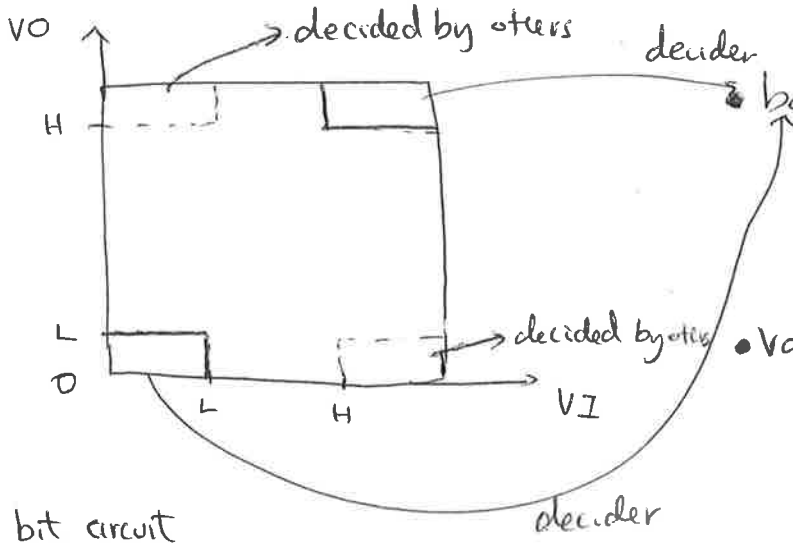
Signal invalid after some resistor in the circuit.

- Solution?

make output range more strict than input range



- Voltage transfer curves



both input/output valid

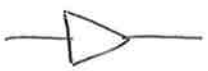
$\begin{cases} V_{IH} < V_{OH} \\ V_{IL} > V_{OL} \end{cases}$

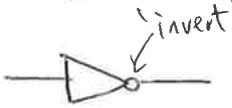
- valid input → valid out signal

can only cross

whole box okay

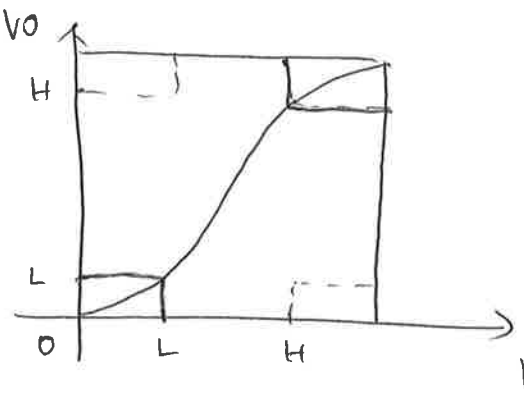
Single bit circuit

buffer  0 → 1, 1 → 0

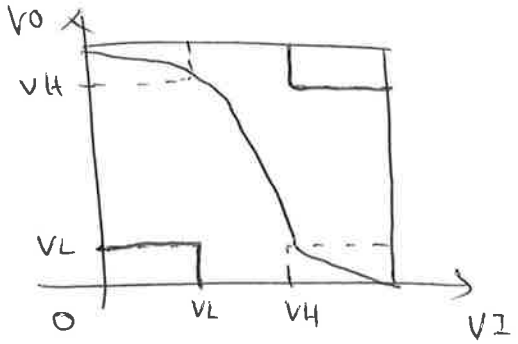
inverter  1 → 0, 0 → 1

('invert')

(are there others?)



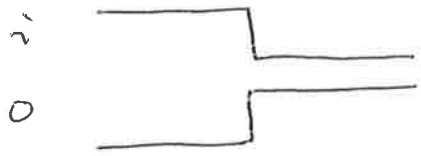
buffer's better 'recharge' the input signal (can wires be buffers?)



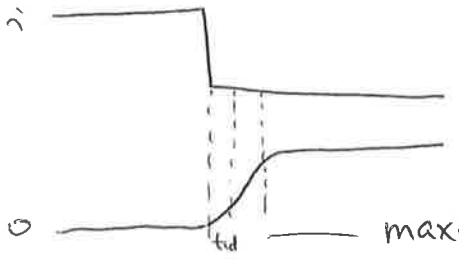
Inverter.

- Contamination delay, propagation delay

Theory



Practice (static discipline)



tcd —— maximum before invalid

tpd —— minimum before valid-again

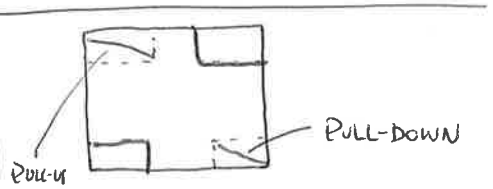
- MOSFETS and CMOS technology

how does one implement a buffer and a converter?

- carve silican (SiO_2) —— MO

dope with p/n material - S

field effect transistor - FET

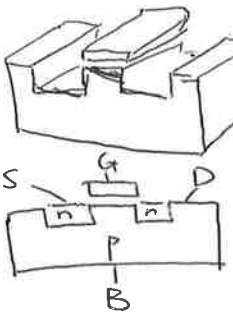


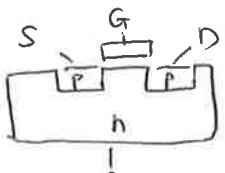
PULL-DOWN: G > threshold → D → 0

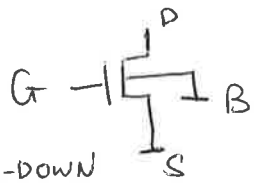
G ≤ threshold → D disconnected

PULL-UP: G < threshold → D → VDD

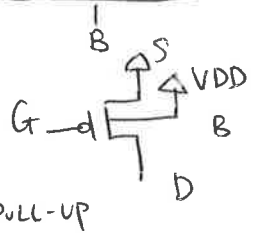
G ≥ threshold → D disconnected





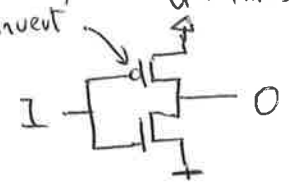


PULL-DOWN



PULL-UP

CMOS



(B omitted)