

Adder Design Using Basic Logic Gates

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Introduction to Logic Design

Introduction

Arithmetic Logic Unit (ALU) is the most fundamental unit in any modern circuit in digital domain. In this design exercise, you are required to design a simple ALU using logic gate of your choice, which is basically a logic adder.

This design exercise starts with examining the behavior of a few logic gates, followed by a design of a half-adder using the existing logic gates. It begins by studying the static input-output relationship of the logic gates. You have to refer to the datasheet of the respective IC to figure out the pins (input, output, supply voltage (VCC), ground (GND)). You also need to find out the required supply voltage for the respective IC. The available logic gates are listed in Table 1.

Table 1: Logic Gates.

Component	Description	Datasheet
74HC00	Quad 2-input NAND gate	74HC00.pdf
74HC02	Quad 2-input NOR gate	74HC02.pdf
74HC04 / 74H04	Hex inverting buffer gate	74HC04.pdf
74HC08	Quad 2-input AND gate	74HC08.pdf
74HC32	Quad 2-input OR gate	74HC32.pdf
74HC86	Quad 2-input exclusive OR gate	74HC86.pdf

You should complete the Pre-Design Exercises in this document before coming to the laboratory to perform the experiment. Then, carry out the In-Lab Exercises on your preferable schedule. After completing the In-Lab Exercises, you have to approach an instructor, teaching assistant (TA) or laboratory assistant (LA) to check your work and sign your report. Before asking to be checked off, make sure you have completed the check-off requirements at the end of the **In-Lab Exercises**. Finally, complete the **Mini-3D**, and turn in your design and report.

Instruction

- Prepare a softcopy report in **Microsoft Word**, record your work and results in this report.
- You must submit the report in both hardcopy and softcopy to your instructor, with TA or LA signature.
- This design exercise (**Pre-Design, In-Lab, Mini-3D**) has to be completed in maximum one session (in three weeks period), and you are encouraged to perform the design independently with minimum instruction from the instructor.
- You are allowed to loan a **myDAQ** and perform the design exercise during your free time, but you must attend the formal lab session.
- This design exercise can be performed by a group with maximum of **4 to 5 students: 3 to 4 from EPD and 2 from ISTD**. Please submit your group member name list in https://docs.google.com/spreadsheets/d/1_3US7Ft8vTMxT7_y2SzbpGuH5MmH62KXj5BEjesACEk/edit?usp=sharing
- Summarize your work in one A2 page poster in Microsoft Powerpoint format (< 2Mb) and submit together with the project video to 30.002 edimension.
- Record your demonstration in video format (< 5 Mb) and submit the video together with the project poster to 30.002 edimension.

Equipment

- NI ELVIS II⁺ (or myDAQ), NI ELVISmx (software)
- Breadboard
- Logic gates (74HC00, 74HC02, 74H04, 74HC08, 74HC32, 74HC86)
- Common electronics e.g. strip-board, wire, resistor, capacitor and etc.

Objectives

In this design exercise you will:

- Measure the static input-output relationship of the logic gates
- Design a simple digital adder
- Examining the functionality of a simple digital adder
- Implement a simple ALU on strip-board with user interface

Deliverables

- Submit your work in the form of a **Poster** according to the requirements of your instructor.
- Submit your work for each exercise (**Pre-Design, In-Lab, mini-3D**), and clearly label the item with its section letter and task number in your poster.
- A demonstration of a working prototype. You need to create a video of the demonstration and submit the video to your instructor for evaluation.

Pre-Design Exercises

(Pre 1-1) Complete the truth table for logic gates: 74HC00, 74HC02, 74H04/74HC04, 74HC08, 74HC32, 74HC86. In the table below, assuming inputs are A, B, output is Y for respective logic gate.

Table 2: Truth Table for Logic Gates.

		74HC00 2-input NAND	74HC02 2-input NOR	74HC08 2-input AND	74HC32 2-input OR	74HC86 2-input XOR
A	B	Y	Y	Y	Y	Y
0	0	1	1	0	0	0
0	1	1	0	0	1	1
1	0	1	0	0	1	1
1	1	0	0	1	1	0

Table 3: Truth Table for Logic Gate (Invertor).

	74HC04 / 74H04 Invertor
A	Y
0	1
1	0

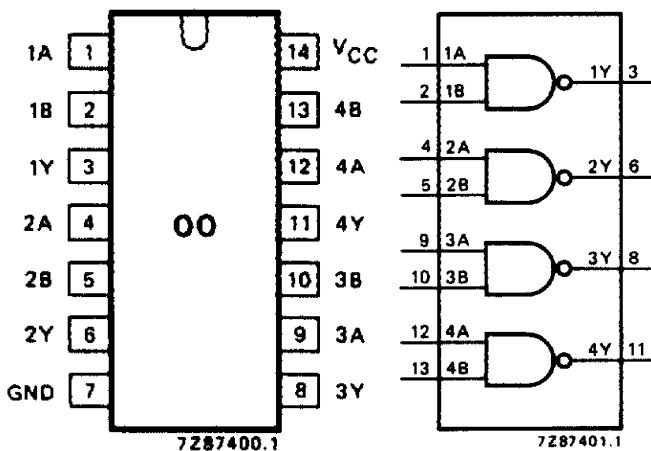
In-Lab Exercises

(In 1-1) Perform a trial test of any of the logic gate in Table 1 using Digital I/O in **NI ELVIS II⁺**. For instance, we would like to determine the functionality of a NAND gate, 74HC00. Recall that the Boolean expression for 2-inputs NAND gate is $Y = \overline{AB}$. The IC diagram and truth table is depicted in Figure 1. You are also encouraged to perform the testing and verification for other logic gates.

- Connect a test circuit for this 2-input NAND gate (74H00) on the NI ELVIS II prototyping board, select one of the NAND gate for testing, e.g. $n=1$, Pin-1 (**1A**), Pin-2 (**1B**), and Pin-3 (**1Y**) forms a 2-input NAND gate input/output
- To supply the power to the IC, you must connect the VCC (Pin-14) to +5.0 V, and GND (Pin-7) to ground
- Connect input pins Pin-1 to DIO1 and Pin-2 to DIO0 (DIO1, DIO0 are two input/output ports on NI ELVIS II)
- Connect output pin Pin-3 to LED0 (LED0 is one output port on NI ELVIS II)
- Turn on the prototyping board power
- Launch **NI ELVISmx Instrument Launcher** on the computer (National Instruments -> NI ELVIS for NI ELVIS & NI myDAQ -> NI ELVISmx Instrument Launcher, Figure 13), and click on **NI ELVISmx Digital Writer (DigOut)**, Figure 14.
- In Digital Writer, set the DIO1 and DIO0 as shown in Table 4, observe the output LED0, and record the result if the LED0 is turned on (logic 1) or turn off (logic 0)
- Is your observation match the result in Figure 2?

Table 4: Test Result of 2-input NAND Gate (74HC00), ($n \in 1, 2, 3$).

Input		Output
DIO1 (nA)	DIO0 (nB)	LED0 (nY)
0	0	1
0	1	1
1	0	1
1	1	0

**Figure 1: Examples of basic logic gate: 2-input NAND gate (74HC00)**

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

Figure 2: Examples of basic logic gate: 2-input NAND gate (74HC00), truth table ($n \in 1, 2, 3$)

(In 1-2) Perform a **literature search** about logic gate adder, which is the most fundamental logic function in ALU. Complete the truth table for a 1-bit half-adder and full-adder below.

Table 5: Truth Table for 1-bit Half-Adder.

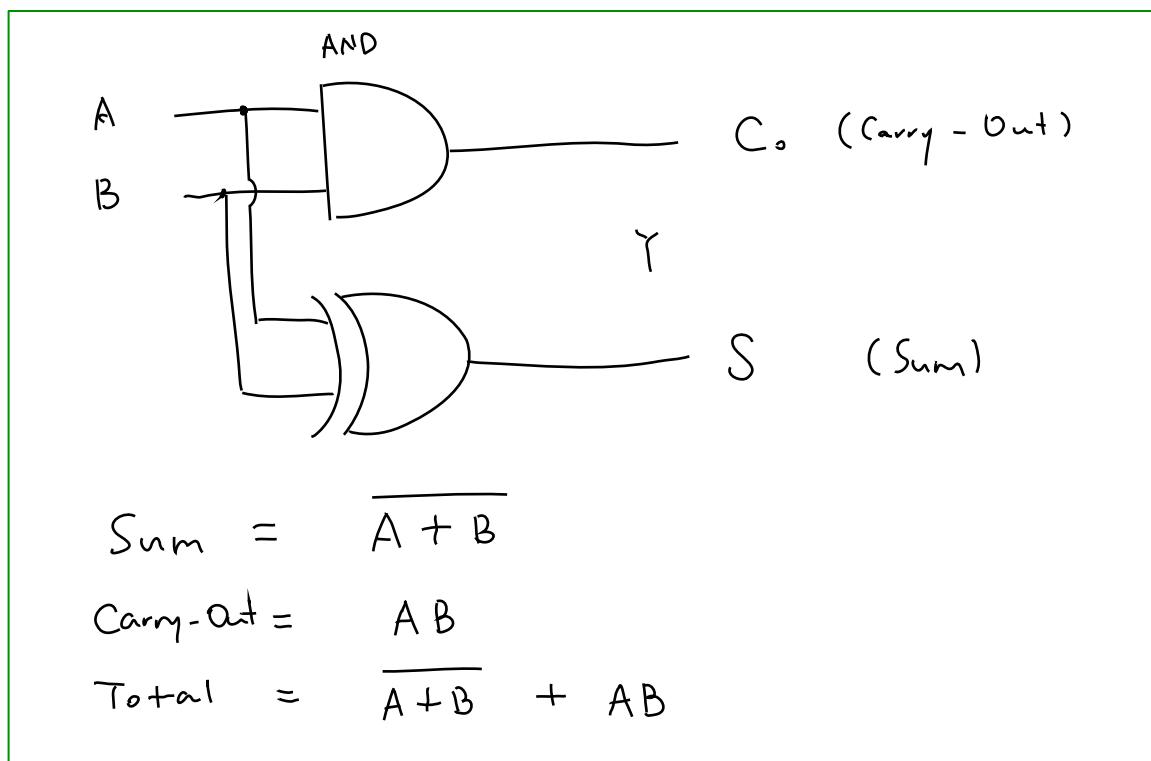
A	B	C _o (Carry-out)	S (Sum)
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Table 6: Truth Table for 1-bit Full-Adder.

C _i (Carry-in)	A	B	C _o (Carry-out)	S (Sum)
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(In 1-3) Construct a 1-bit half-adder using logic gates in Table 1. You should consider using a logic gate that could minimize the number of gates in the half-adder design. The basic goals in digital circuit design are the optimization of speed, power, size and cost.

(In 1-4) You should select the logic gates that you want to use to construct this half-adder. Draw the schematic of the gate level half-adder. Show the Boolean expression of the half-adder also.



Mini-3D

In this mini-3D, you need to implement the simple ALU on strip-board. You only need to perform one design below.

- I. Part I (Compulsory for 30.002, Extra Credit for 50.002): After verification of the 1-bit full-adder design using breadboard and ELVIS II+, implement the full-adder on a strip-board. You may consider using logic gate, switch, resistor, LED, battery and etc. to design your simple ALU. A basic ALU demo board is prepared for your reference. You can perform a simulation using circuit simulator, **Multisim** in computer before implement the design on the strip-board. You can also explore the design using PCB.
- A simple YouTube tutorial about how to use strip-board and doing soldering is suggested here;
 - <http://www.youtube.com/watch?v=DSk5DQhi1r0>, strip-board design
 - http://www.youtube.com/watch?v=jr2Z_fztpxg, soldering skill
 - A possible list of components is summarized in the table below.

Table 7: List of Components for 1-bit Full-Adder.

S/N	Description	Part number	Quantity	Photo
1	470 Ω resistor		2	
2	12 k Ω resistor		2	
3	Red LED		2	
4	XOR gate	PC74HC86P	1	
5	AND gate	PC74HC08P	1	
6	4 way switch		1	
7	Slide switch		1	
8	Jumper wire			
9	Battery holder		1	
10	1.5 V battery		4	
11	OR gate	PC74HC32	1	

12	Strip-board		1	
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- c. An example of simulation setup schematic in **Multisim** is also depicted in the figure below. Please refer to document "Introduction to Multisim and Ultiboard" if interested. There is an error in the following figure, please identify and correct it during your simulation.

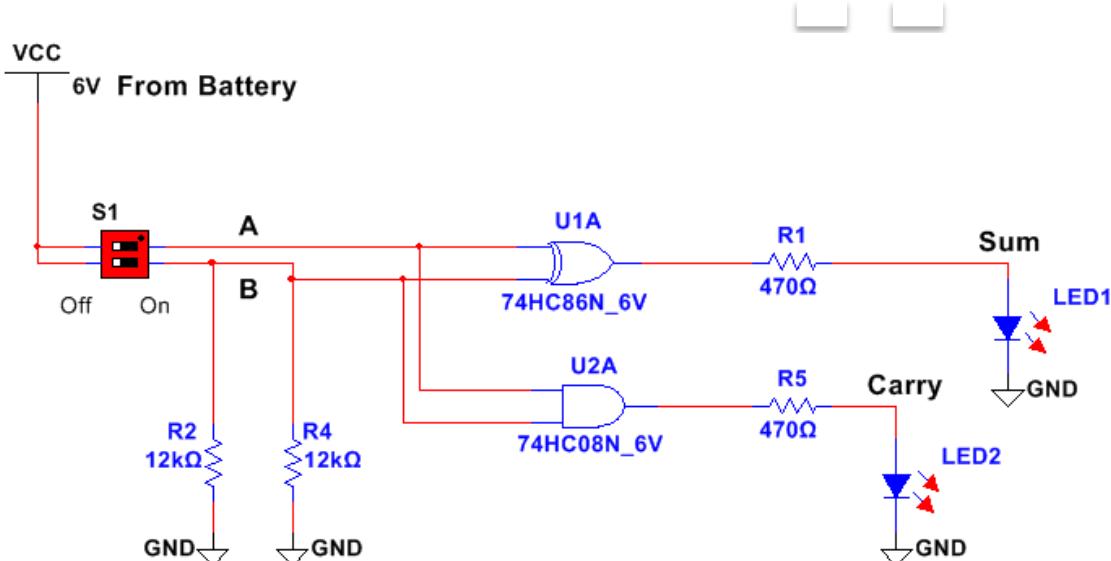
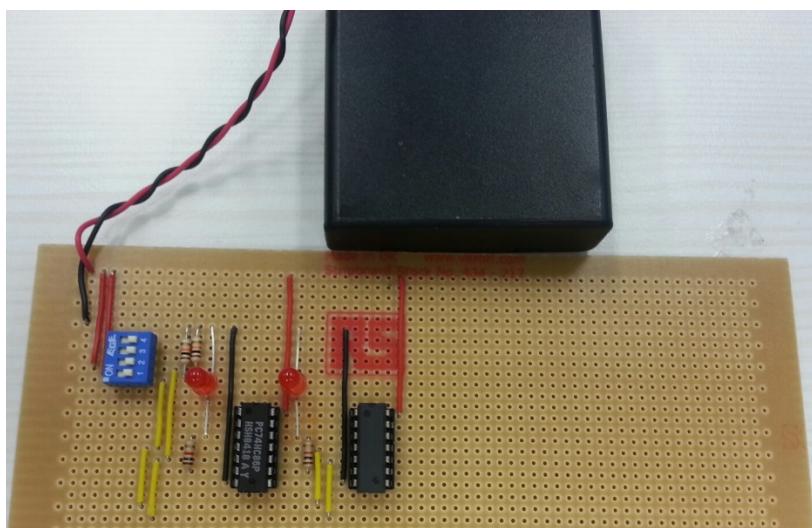
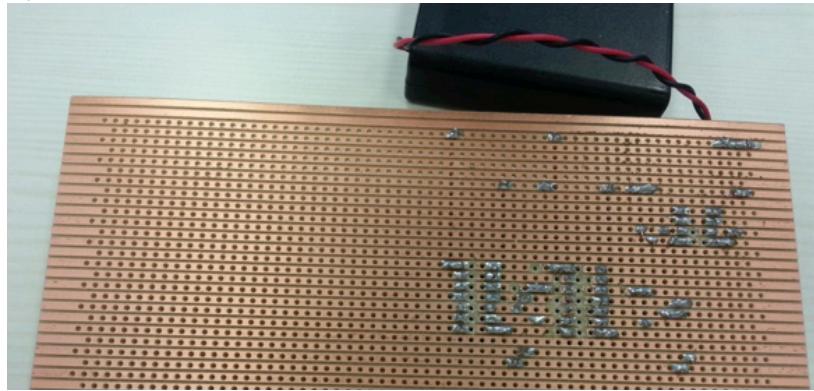


Figure 3: 1-bit half-adder simulation setup in Multisim

- d. A demo board that is designed with a strip-board is shown in the snapshots below.



(a) Front view



(b) Back view

Figure 4: Demo board view

II. Part II (Extra Credit for 30.002, Compulsory for 50.002):

- Design a multi-bit adder by combining your 1-bit full adder with other team in your cohort, minimum 4-bits. You can also construct additional 1-bit full adders and combine them in the same strip-board yourself.
- In this step, we want to verify the functionality of your combined multi-bit adder using FPGA. Use Mojo – V3 FPGA board and Lucid HDL, and create one module that generates input to your multi-bit adder and check whether the output of your multi-bit adder is correct. You are free to design the test cases and whether any interface like buttons or LEDs are required. No microcontroller is allowed in this case, but only FPGA. Note that you are required to use Lucid and Mojo IDE for your project.
- Submit separate Poster and Video in Week-4 for this activity to 50.002 eDimension. ISTD students need to keep their Mojo – V3 FPGA for their use in 1D projects.

Check-off

Before you ask to be checked off, make sure you have completed the following tasks:

- Complete the pre-lab exercises in your poster. You need to submit only **one** single page poster. You should include all members name, ID, and pillar.
- Record the in-lab measurements in your report. Be sure to read the in-lab exercises carefully to note what measurements should be made.
- A working circuit (on breadboard) as described in **In-Lab Exercise 1-3**. You do not need to complete this design in the lesson. This design serves as a verification step of your final design on the strip-board.
- A working circuit (on strip-board) as described in **Mini-3D**. You need to make a video of your demonstration and submit to your instructors for evaluation.

Quick Start for Breadboard and Logic Gate IC

This section means to give a basic idea regarding the use of logic gates.

- Figure 5 shows the basic configuration of a prototyping board (breadboard).

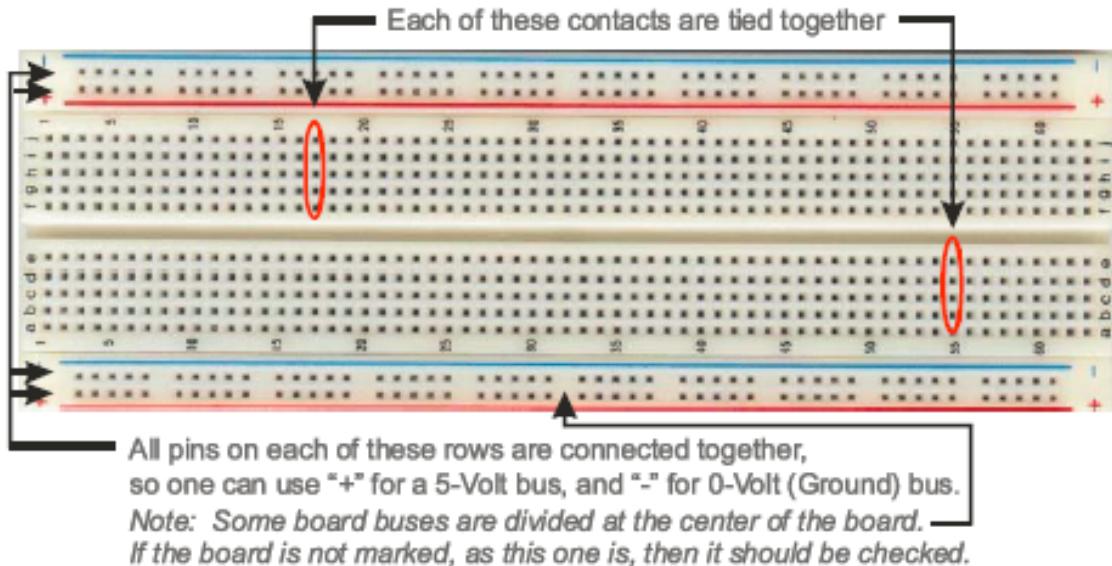


Figure 5: Prototyping board

- Figure 6 shows the wiring connection between ICs and the power supply.

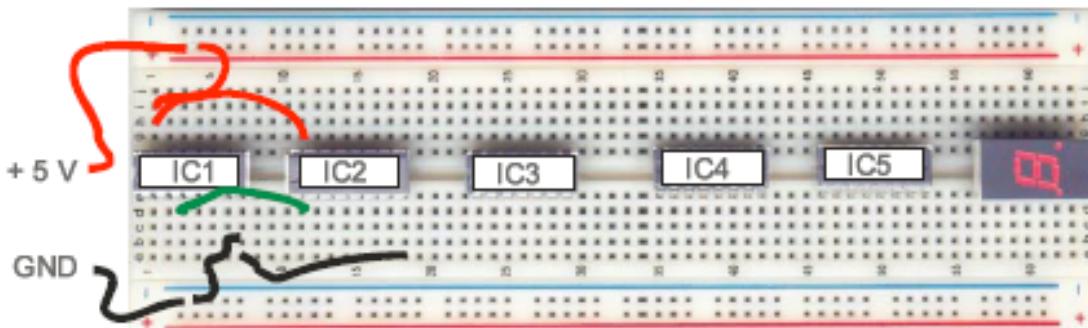


Figure 6: Insert IC and wire in a prototyping board

- It is important to identify the 1st pin on the ICs. Figure 7 shows the orientation of typical ICs, take note about how to find the pin no. You should refer to the datasheet of the ICs. Figure 2 shows a portion of the datasheet with its internal gate level schematic.

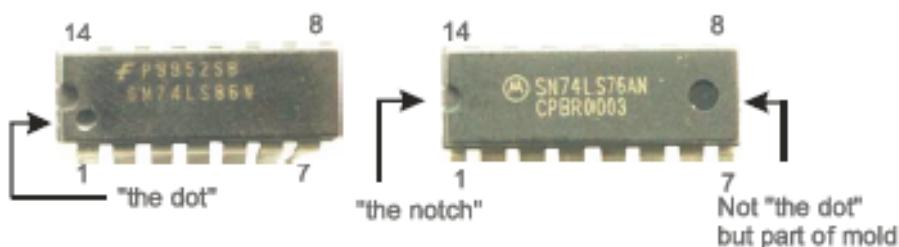


Figure 7: IC numbering (Pin 1 is designated by a dot or a notch and numbering follows counter clock wise direction, there are exceptions to this rule)

Quick Starts for NI ELVIS II+ Prototyping Board Setup

- 1) Place the NI ELVIS II⁺ board on the table



Insert the NI ELVIS II prototyping board

Figure 8: NI ELVIS II⁺ board

- 2) Put the NI ELVIS II prototyping board on the NI ELVIS II⁺ board

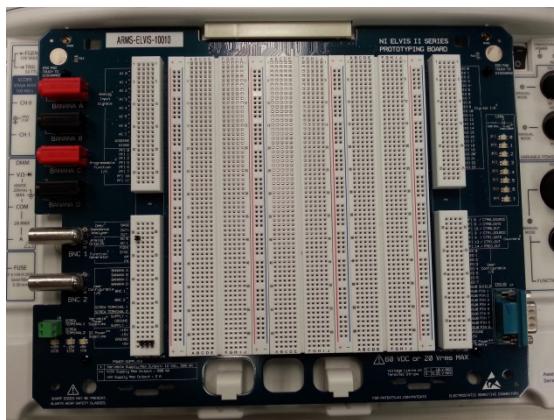
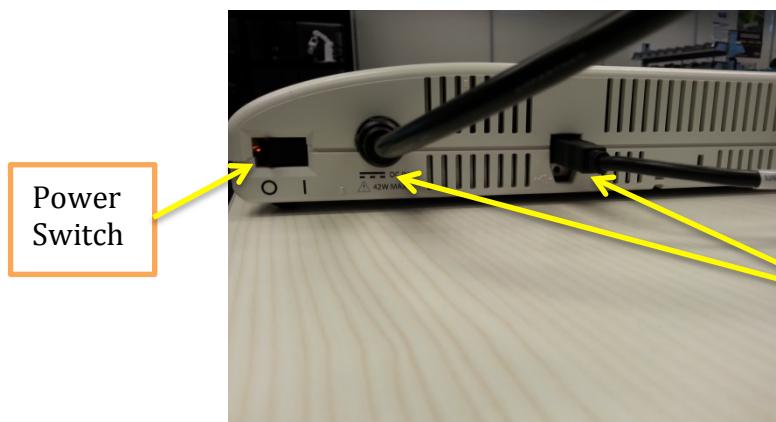


Figure 9: NI ELVIS II prototyping board setup

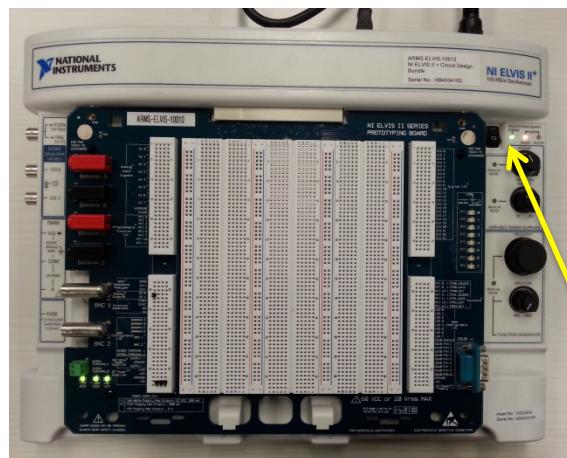
- 3) Plug in the two cables in the respective ports and switch on the power.



Insert power cable and USB cable to the NI ELVIS II⁺

Figure 10: Power plug and USB cables connection

- 4) The NI ELVIS II⁺ prototyping board is ready to use if the green light is ON.



Switch on the switch and check the green light beside the switch

Figure 11: NI ELVIS II⁺ prototyping board is ready if green light turns on

1. A sample setup for NAND Gate testing using **Digital Inputs / Outputs** is shown in the figure below.

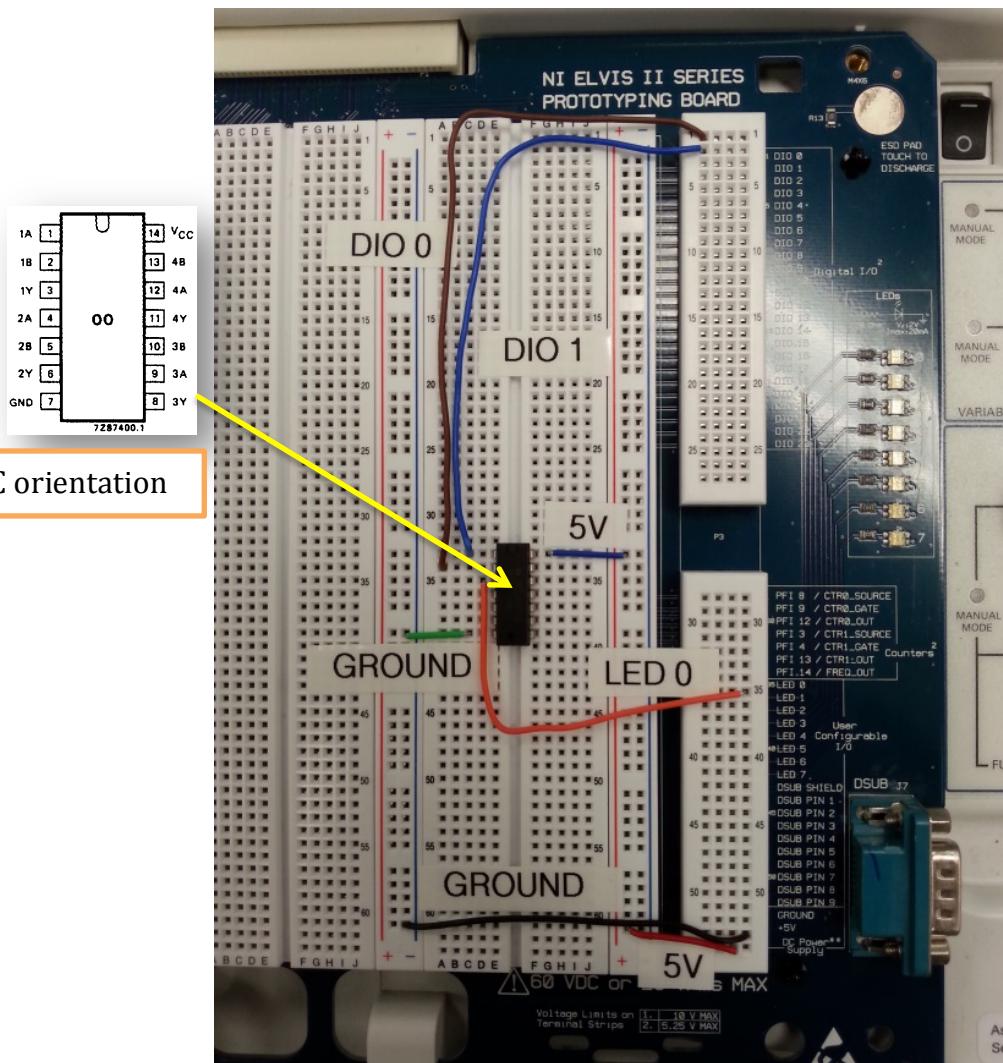


Figure 12: Digital Inputs / Outputs connections for a NANG Gate

2. To launch the **NI ELVISmx Instrument Launcher**, (National Instruments -> NI ELVIS for NI ELVIS & NI myDAQ -> NI ELVISmx Instrument Launcher)

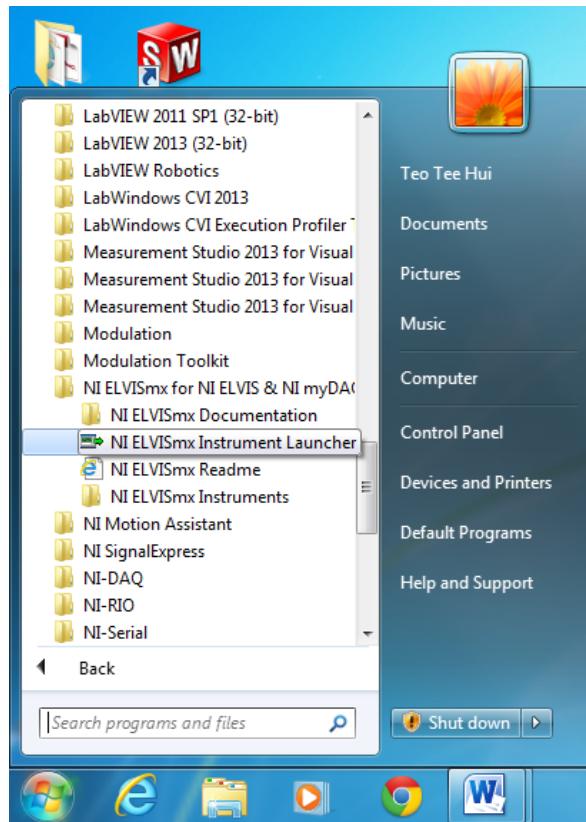


Figure 13: NI ELVISmx Instrument Launcher

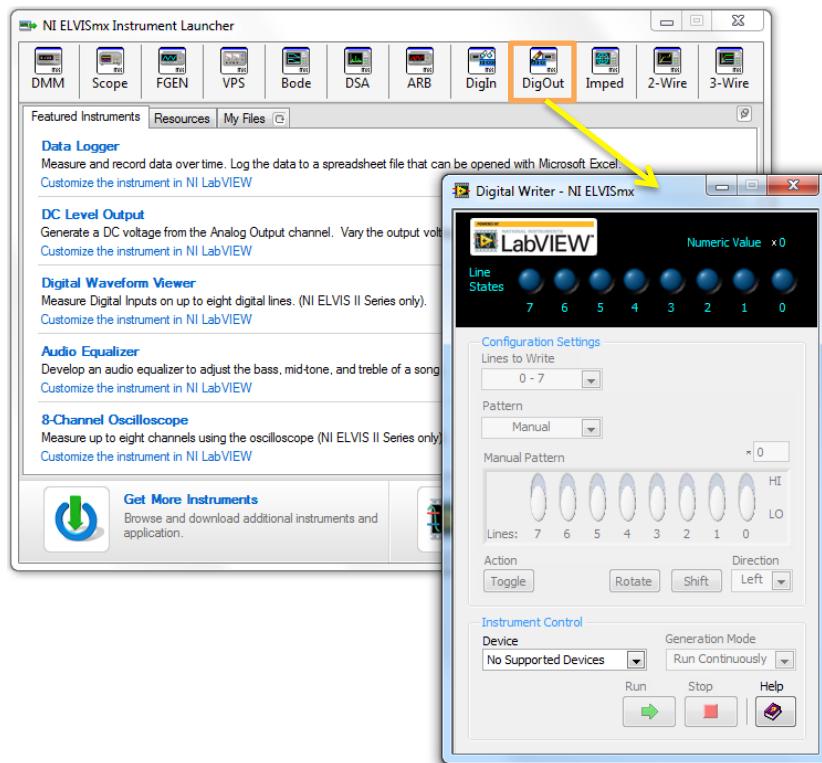


Figure 14: NI ELVISmx Instrument Launcher interface and Digital Writer (DigOut)

3. Testing Results of NAND Gate using Digital Inputs / Outputs using Digital Writer (DigOut), the detail image of Digital Writer is shown in Figure 14.

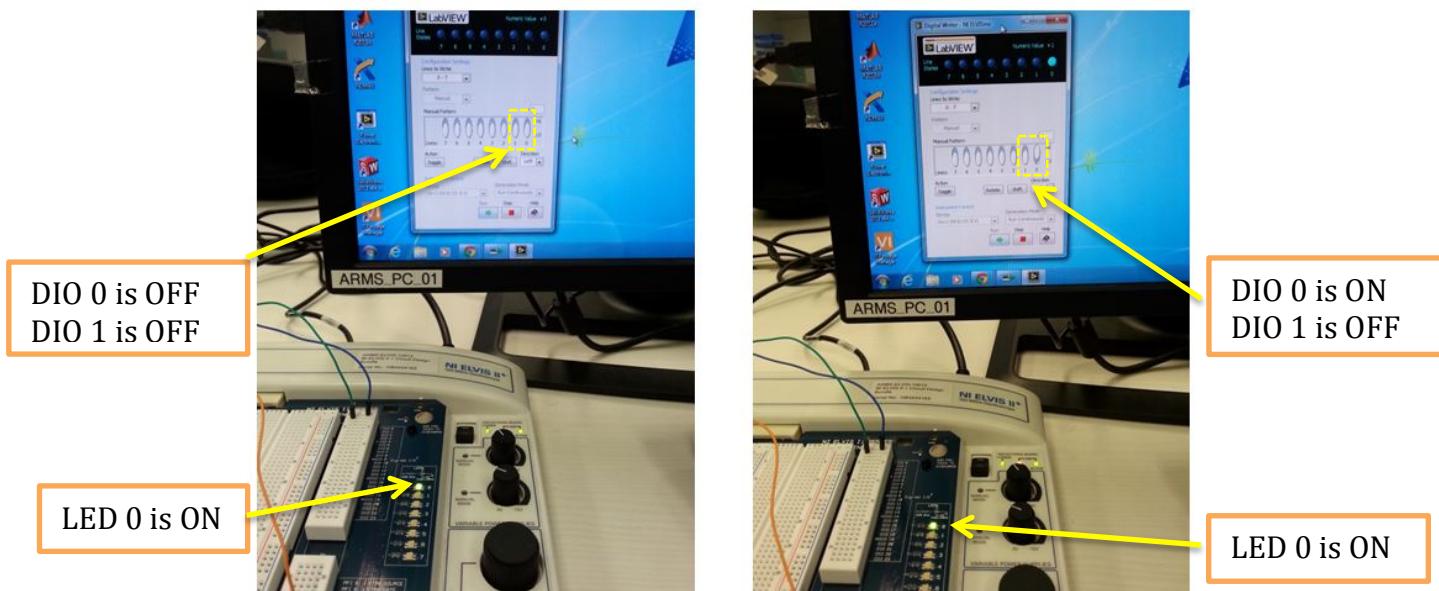


Figure 15: Test Results of NAND Gate 001 (Left) & 011 (Right)

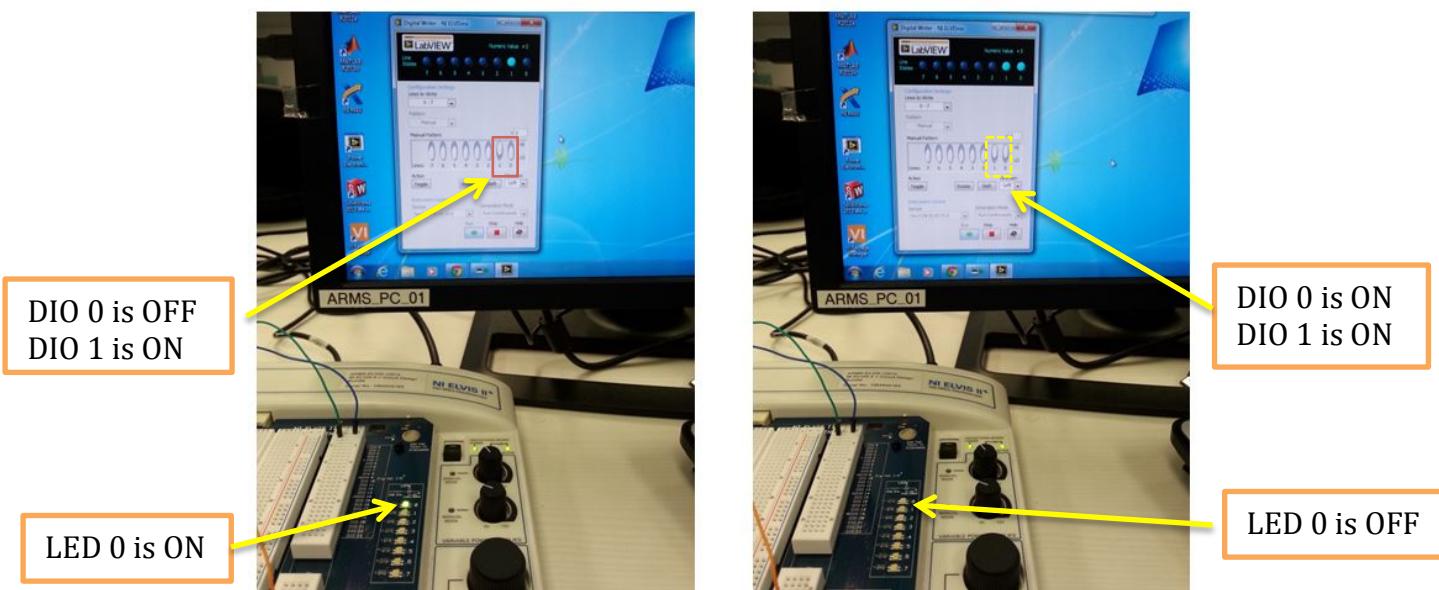


Figure 16: Test Results of NAND Gate 101 (Left) & 110 (Right)

JIT Video Tutorial for 3D Project

Week01: mini-3D In-Lab activity video instruction-1 (NI ELVIS II Setup - YouTube)

<http://www.youtube.com/watch?v=WqTe76VSH1c&feature=youtu.be>

Week01: mini-3D In-Lab activity video instruction-2 (Digital NAND gate - YouTube)

<http://www.youtube.com/watch?v=l-27ILetjcQ&feature=youtu.be>

Mojo – V3 Tutorial for 3D Project

Mojo – Lucid Tutorial: <https://embeddedmicro.com/tutorials/lucid>

First FPGA Project: <https://embeddedmicro.com/tutorials/lucid/your-first-fpga-project>

Creating module (Synchronous Logic): <https://embeddedmicro.com/tutorials/lucid/synchronous-logic-tutorial>

Adding Components: <https://embeddedmicro.com/tutorials/lucid/components>

External IO: <https://embeddedmicro.com/tutorials/lucid/external-io-tutorial>

Creating ROM and FSM: <https://embeddedmicro.com/tutorials/lucid/roms-and-fsms-tutorial>