Neurocomputing 2 (1990) 29 – 34
Elsevier

Neurocomputing R&D in Japan

Tatsumi Furuya
Electrotechnical Laboratory, 1-1-4 Umezono, Tsukuba-city, Ibaraki 305, Japan

1. Introduction

Neurocomputing is recognized as an important information processing technology for the next generation in Japan. For the last two or three years, various organizations have already started research and development (R&D) efforts. This paper surveys the recent R&D in the field of neurocomputing and describes the government support R&D programs in Japan.

2. Neurocomputing in Japan

Neurocomputing is a rapidly growing field, from theory to application. This section describes the neurocomputing from the following points of view: (1) theories and models, (2) applications, and (3) neurocomputers.

2.1. Theories and models

Many research activities about mathematical theories and models were conducted even in the so-called winter season of neurocomputing. Prof. Amari's (University of Tokyo) research efforts are well known and they cover a wide area of mathematical theory for neurocomputing. The neocognitron by Fukushima (NHK) [11], the associatron by Nakano (University of Tokyo) [32], and the HASP by Hirai (University of Tsukuba) [15] are famous models. In the following subsections, the recent research activities about theory and model are presented.

2.1.1. Theories

Network theories. Recent research activities which are classified to be the network structure are as follows.

Multi-layer neural network:

- Irie (ATR) showed the capabilities of neural networks [21].
- Funahashi (ATR) proved that any continuous mapping can be approximately realized by multi-layer networks [12].
- Arai (Toshiba) showed the mapping ability of neural networks [6].
- Asoh (ETL:Electrotechnical Laboratory) showed that the multi-layer perceptron with nonlinear elements approximates the nonlinear data analysis methods [7].

Hopfield neural network:

- Abe (Hitachi) studied the convergence characteristics [1].

Others:

- Shinomoto (Kyoto University) introduced a physiological constraint in the auto-correlation matrix memory. It enables to find out unexpected input patterns [36].
- Tanaka (NEC) proposed a theory of self-organization of cortical maps [37].
- Aihara (Tokyo Denki University) proposed a theory of the caotic neuron [2].

Learning theory. There are many proposed papers regarding the speed-up method of the back-propagation learning and the improvement of its convergence written in Japanese. Some of the

papers published in English are the following.
- Baba (University of Tokushima) showed an approach for finding the global minimum of error function of neural networks [8].
- Ishikawa (ETL) proposed a structural learning algorithm which generates a skeletal structure of neural networks [24].
- Yamada (NEC) proposed an improvement to the method of convergence by changing the characteristics of transfer function [40].

2.1.2. Models
- Kawato (ATR) proposed a hierarchical model for voluntary movement. The model includes the inverse-dynamics model which provides an internal feedback loop [28].
- Akiyama (Keio University) proposed a model called the "Gaussian machine". It has graded output responses as well as stochastic behavior caused by random noise added to the input of each neuron. The model is a general model of the Pitts model, the Hopfield model, and the Boltzmann machine [3].
- Tsutsumi (Kobe University) proposed a structured neural network for manipulator configuration control. It consists of the back-propagation network and the Hopfield network. The former works for acquiring the arbitrary mapping and the latter functions for energy minimization [38].
- Doya (University of Tokyo) proposed the Adaptive Neural Oscillator (ANO). The ANO is a recurrent network of continuous-time continuous-output model neurons. The network can memorize and regenerate various time-periodic patterns [9].
- Furuya (ETL) proposed a structured neural network for the artificial intelligence. The model enables building up various types of AI system by association operations and the associative control structure [13]. The neuro fuzzy inference system is used in the model [14].

2.2. Applications

Lots of application examples have been reported until now. In this subsection, applications which were published as original papers or applications which were announced on a newspaper are shown.

Pattern recognition

Speech.
- Iso (NEC) proposed a speech recognition model, Neural Prediction Model (NPM). The model uses a sequence of multi-layer perceptrons as a nonlinear predictor for each recognition class. Each predictor outputs a speech pattern at time t using the speech patterns before t as an input. The difference between the predicted speech pattern and the actual one is regarded as a distance measure in recognition. Efficient training algorithms are presented based on the combination of the dynamic-programming and the back-propagation techniques [23].
- Matsuoka (NTT) proposed an integrated neural network for syllable recognition. The network consists of a control network and several subnetworks. The syllables are partitioned into several groups. The control network identifies the group, and each subnetwork recognizes the syllables in each group [31].
- Sawai (ATR) proposed a structured neural network (called the Time-Delay Neural Network) for the C/V syllables or phoneme spotting. The network consists of subnetworks and a control network as the NTT's. However, the subnetwork has two hidden layers, and its neuron unit has links which have delay [35].
- Amano (Hitachi) proposed a rule-based phoneme recognition method. Neural networks are used for acoustic feature detection such as fricative, nasal, plosive, etc. The outputs of the neural network are information for fuzzy rule-based operation [5].

Image.
- Omori (Tokyo University of Agriculture Tech.) proposed a model for image understanding. The model is based on the neocognitron [33].
- Hosokawa (University of Tokushima) proposed

a pattern recognition algorithm involving the invariance network and the adaptive descrambler [18].

• Uchiyama (NTT) proposed a modified leaky integrator for temporal pattern processing. The integrator is a neuron model which generates continuous output based on its activation history [39].

• Yamada (NEC) applied a multi-layer feed-forward neural network to the handwritten numeral recognition [40].

Though many papers were published in this field, most of them are written in Japanese [19]. For example:

• Image prediction and concealment by Doi (Hitachi);

• image coding by Sakaue (Matsushita Electric);

• color-space mapping by Nakauchi (Toyohashi University of Technology);

• handprinted character recognition:
  - Alphanumerical by Tamura (Matsushita Electric),
  - Kanji character by Mori (ATR),
  - Kana character by Hatano (Toshiba).

Others.

• Hiramatsu (NTT) proposed a control method for high-speed packet switching network for data transmission. A neural network is used to decide the accept/rejection depending on the cell arrival [17].

• Matsuda (Tokyo Electric Power Company) applied the Hopfield neural networks to the economical load dispatching problem of electric power [30].

• Akiyama (Keio University) solved the n-queen and the polyomino puzzle by Gaussian machines (cf. 2.1) [4].

• Iwata (Nagoya Institute of Technology) proposed a data-compressing algorithm for digital holter recording using neural network [25].

Reported on newspapers.

• NEC: Face identification of 3500 persons.

• Nippon Steel Co.: Blast furnace control.

• Hitachi: Diagnosis of a leukocyte.

2.3. Neurocomputers

There are many challenges to implement neurocomputers ranging from neurochip approach to optical approach.

2.3.1. Neurochips

The following neurochips have already been fabricated. They implemented artificial neuron models on chips by the digital or the analog VLSI technologies.

• Keio University: A conductance programmable neurochip was fabricated by using a 3 micron CMOS. The switched resistors are used for neuron and it enables the simulated annealing operation [3].

• Fujitsu: A neurochip was developed by using the BiCMOS technology. The chip has one neuron processor with an analog data processing.

• Hitachi: A wafer scale integration neural network has been developed. 540 neurons and 34 560 synapses are implemented in one silicon wafer [41].

• University of Tsukuba: A digital neurochip has been fabricated by using a 1.2 micron CMOS gate array. The chip contains six neurons and 84 synapses. Each synapse has 64 levels of modifiable weights. The output and input of neurons are represented by impulse densities [16].

2.3.2. Neurocomputers

There are two basic approaches to the neurocomputer. The first one is the fully implemented system which implements one neuron on one processor. The second one is the hardware simulator. Neurocomputers which are described below and in the succeeding section belong to the hardware simulator.

• NEC developed a neurocomputer called NeuMan. In this machine, N processing units are connected by a multi-stage interconnection network. Each processing unit runs on MIMD mode [27].

• Nagoya Institute of Technology developed a neural network accelerator. The accelerator is a

MIMD type parallel processor having coupled 4 DSPs (MB86220) and 4 dual port memories [26].
• SONY announced a parallel processor for neurocomputing. It consists of 128 INTEL80860 processors.
• FUJITSU announced a neurosystem with 256 DSP chips.

2.3.3. Commercial neurocomputers

The following neurocomputers are already found in the market.
• NEC: The personal neurocomputer (NEURO-7) uses a neuro-engine board in a PC-9800 personal computer. The neuro-engine uses data flow chips (ImPP) to accelerate the operation speed. The operating speed is 216 000 links per second, using up to 82 000 neurons or 246 000 possible links.
• FUJITSU: The personal neurocomputer (NEUROSIM/L) is a neurosimulator which works on a Fujitsu personal computer (FMR). The neurocomputer has a neuroboard which has a DSP (MB86232). The operation speed is at 1.5 MCPS (for training) and at 4 MCPS (for execution) (CPS: connections per second).
• Nippon Steel Corporation: A neuroboard for the NEC personal computer is on the market. Transputers (4-16) are used for the neural network simulation. In case of the four transputer version, the operation speed is 1 MCPS.

2.3.4. Optical neurocomputers

• Industrial Products Research Institute: An optical associative memory was constructed. The model is based on Nakano's associatron [32]. The system utilizes some microchannel spatial light modulators [22].
• NTT: Optical multi-layer network with back-propagation learning capability was constructed. The modifiable connection weights and unit plane were realized by using a photorefractive crystal and microchannel spatial light modulator [29].
• MITSUBISHI: An optical neurochip was fabricated using the GaAs technology. The device consists of a light-emitting-diode array, an interconnection matrix, and a photodiode array which were integrated into a hybrid-layered structure on a GaAs substrate. The fabricated device can simulate a 32 neuron system. They implemented the Hopfield associative memory with three stored vectors [34].

3. Government research projects

This section introduces two government R&D projects which are related to the neurocomputing.

3.1. Human Frontier Science Program (HFSP)

The HFSP is an international program which aims at promoting basic research focusing on the elucidation of the sophisticated and complex mechanisms of living organisms. Research areas of HFSP:

(A) Basic research for the elucidation of brain functions.
  (1) Perception and cognition,
  (2) movement and behaviour,
  (3) memory and learning,
  (4) language and thinking.
(B) Basic research for the elucidation of biological functions through molecular level approaches.
  (1) Expression of genetic information,
  (2) morphogenesis,
  (3) molecular recognition and responses,
  (4) energy conversion.

The organization was established in Strasbourg (France).

Address for information:

International Human Frontier Science Program Organization (HFSPO),
Tour Europe 20 Place des halles,
Strasbourg 67000, France
FAX: (France33) 88 32 88 97,
Phone: (France33) 88 32 88 33.

3.2. Bio-electronic devices

The Ministry of International Trade and In-

dustry started the project which deals with revolutionary basic technology essential to establishment of the new industries expected to flourish in the 1990s. This research aims at applications of biofunctions to new electronic devices. Functions of neural systems are investigated to elucidate biological information processing. New techniques to fabricate well-organized molecular system are developed to construct engineering models of biofunctions. The association (RESEARCH DEVELOPMENT ASSOCIATION for FUTURE ELECTRON DEVICES) organizes international workshops and symposia. Seven workshops and two symposia were already held [10].

Address for information:

RESEARCH DEVELOPMENT ASSOCIATION
for FUTURE ELECTRON DEVICES,
Fukide Building No. 2, 4-1-21,
Toranomon, Minato-ku,
Tokyo 105, Japan
FAX: +81-3434-7320,
Phone: +81-3434-3893.

4. Conclusion

The progress of R&D in the field of neurocomputing is very rapid. While I am writing this paper, many news have been reported. There had been numerous published papers about neurocomputing in Japan. However, most of them are written in Japanese. I had selected some topics which were published in English and of special interests to this paper.

Acknowledgment

The author wishes to thank Mr. A. Kokubu, Manager of Computer Models Section, and persons who submitted various information for this paper.

References

[1] S. Abe, Theories on the Hopfield networks, *IJCNN89* (1989).
[2] K. Aihara et al., Structures of attractors in periodically forced neural oscillators, *Phys. Lett. A* **116** (1986).
[3] Y. Akiyama et al., Conductance programmable 'neural' chips employing switched resistors, in: *Proceedings JTC-CSCC88* (1989).
[4] Y. Akiyama et al., Combinatorial optimization with Gaussian machines, *IJCNN89* (1989).
[5] A. Amano et al., On the use of neural networks and fuzzy logic in speech recognition, *IJCNN89* (1989).
[6] M. Arai, Mapping abilities of three-layer neural networks, *IJCNN89* (1989).
[7] H. Asoh and N. Otsu, Nonlinear data analysis and multilayer perceptrons, *IJCNN89* (1989).
[8] N. Baba, A new approach for finding the global minimum of error function of neural network, *Neural Networks* **2** (5) (1989).
[9] K. Doya and S. Yoshizawa, Memorizing oscillation patterns in analog neuron networks, *IJCNN89* (1989).
[10] FED, An outline of the research and development association for future electron devices, 1989.
[11] K. Fukushima, Neocognitron: A hierarchical neural network capable of visual pattern recognition, *Neural Networks* **1** (2) (1988).
[12] K. Funahashi, On the approximate realization of continuous mappings by neural networks, *Neural Networks* **2** (3) (1989).
[13] T. Furuya, μBRAIN: A structured neural network for connectionist intelligent systems, ETL Tech. Rept. 89-8, 1989.
[14] T. Furuya, NFS: Neuro fuzzy inference system, Int. Work. Fuzzy System Applications, 1989.
[15] Y. Hirai, Representation of control structures by a model of an associative processor, HASP, *ICNN87* (1987).
[16] Y. Hirai et al., A digital neuro-chip with unlimited connectability for large scale neural networks, *IJCNN89* (1989).
[17] A. Hiramatsu, ATM communication network control by neural network, *IJCNN89* (1989).
[18] M. Hosokawa et al., A new approach for pattern recognition by neural networks with scramblers, *IJCNN89* (1989).
[19] IEIC, 1989 Autumn National Convention Record- Part 6, The Institute of Electronics, Information and Communication, 1989.
[20] Iinuma, Neural computing studies at NEC, in: *The 3rd European Seminar on Neural Computing* (1990).
[21] B. Irie and S. Miyake, Capabilities of three-layered perceptrons, *IJCNN88* (1988).

[22] M. Ishikawa, Optical Associatron: A simple model for optical associative memory, *Appl. Optics* **28** (2) (1989).
[23] K. Iso and T. Watanabe, Speaker-independent word recognition using a neural prediction model, *ICASSP91* (1990).
[24] M. Ishikawa, A structured learning algorithm with forgetting of link weights, ETL Tech. Rept., 1990.
[25] A. Iwata et al., A digital holter monitoring system with dual 3 layers neural networks, *IJCNN89* (1989).
[26] A. Iwata et al., An artificial neural network accelerator using general purpose 24 bit floating point digital signal processors, *IJCNN89* (1989).
[27] N. Kajihara et al., Parallel neural network simulation machine, *INNS88* (1988).
[28] M. Kawato et al., A hierarchical model for voluntary movement and its application to robotics, *ICNN87* (1987).
[29] K. Kitayama and H. Yoshinaga, Experiments of learning in optical perceptron-like and multilayer neural networks, *IJCNN89* (1989).
[30] S. Matsuda and Y. Akimoto, The representation of large numbers in neural networks and its application to economical load dispatching of electric power, *IJCNN89* (1989).
[31] T. Matsuoka et al., Syllable recognition using integrated neural networks, *IJCNN89* (1989).
[32] K. Nakano, Associatron—A model of associative memory, *IEEE Trans. Systems Man Cybernet.* **2** (1972).
[33] T. Omori and T. Nagasue, Image understanding by neuron networks: Representation and operation of internal image, *IJCNN89* (1989).
[34] J. Ohta et al., GaAs/AlGaAs optical synaptic interconnection device for neural network, *Optical Lett.* **14** (16) (1989).
[35] H. Sawai et al., Parallelism, hierarchy, scaling in time-delay neural networks for spotting Japanese phonemes/CV-syllables, *IJCNN89* (1989).
[36] S. Shinomoto, A cognitive and associative memory, *Biol. Cybernet.* **57** (1987).
[37] S. Tanaka, Theory of self-organization of cortical maps, in: *Advances in Neural Information Processing Systems 1* (Morgan Kaufmann, Los Altos, CA, 1989).
[38] K. Tsutsumi, A multi-layered neural network composed of backpropagation and Hopfield nets and internal space representation, *IJCNN89* (1989).
[39] T. Uchiyama et al., A modified leaky integrator network for temporal pattern processing, *IJCNN89* (1989).
[40] K. Yamada et al., Handwritten numeral recognition by multi-layered neural network with improved learning algorithm, *IJCNN89* (1989).
[41] M. Yasunaga et al., A wafer scale integration neural network utilizing completely digital circuits, *IJCNN89* (1989).

Tatsumi Furuya is a senior research scientist at Electrotechnical Laboratory. He joined the laboratory in 1973 and is currently carrying out research on neural networks for artificial intelligence and digital neural networks.

Furuya received the BS (1971), the MS (1973), and Ph.D. in electrical engineering (1985) from the Seikei University. Furuya is a member of the IEEE.