MONASH University

Unit Guide

ECE3062
Electronic systems and control

Semester 2, 2017

Table of contents

Unit handbook information

Synopsis

The unit further explores the integration of multiple devices on a chip. MOS and BJT single ended as well as differential amplifier circuits, along with basic analogue circuit blocks like the current mirror, are introduced and developed using small signal models. Practical Operational Amplifiers are considered where properties deviate from ideal in terms of frequency response, CMMR, noise, stability and input/output impedance. The use of feedback in electronic circuits is studied, and ways to improve arising stability issues in operational amplifiers (eg using pole compensation) are discussed. Nyquist is presented and frequency domain analysis and design shall be explicitly explored via Bode plots. Concepts of State Space representation, transfer functions, canonical realisation, observability and controllability and discrete-time systems are presented.

Mode of delivery

Malaysia (Day)
Clayton (Day)

Workload requirements

2 hours lectures, 3 hours laboratory/practice classes and 7 hours of private study per week

Unit relationships

Prerequisites

ECE2031 and ECE2061

Prohibitions

ECE2062

Co-requisites

None

Chief Examiner(s)

Professor Manos Varvarigos

Unit Coordinator(s)

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Clayton/Malaysia staff contact details

Clayton campus	
Campus Coordinator	Name: Dr Jean-Michel Redoute Email: Jean-Michel.Redoute@monash.edu Building: 72, Room: 206 Consultation hours: Appointment per email
Lecturer(s)	Name: Dr Jean-Michel Redoute Email: Jean-Michel.Redoute@monash.edu Building: 72, Room: 206 Name: Dr James Saunderson Email: James.Saunderson@monash.edu Building: 72, Room: 222 Consultation hours: Appointment per email

Malaysia campus	
Campus Coordinator	Name: Dr Masuduzzaman Bakaul Email: Bakaul.Masuduzzaman@monash.edu Building: 2-4-25, Room: Consultation hours: Appointment per email
Lecturer(s)	Name: Dr Masuduzzaman Bakaul Email: Bakaul.Masuduzzaman@monash.edu Building: 2-4-25, Room: Consultation hours: Appointment per email

Section A: For Clayton students

Academic Overview

Engineers Australia Stage 1 competencies

The Engineers Australia Policy on Accreditation of Professional Engineering Programs requires that all programs ensure that their engineering graduates develop to a substantial degree the stage 1 competencies. Listed below are the activities in this unit that will help you to achieve these competencies.

Note: that not all stage 1 competencies are relevant to each unit.

TBD by the Faculty.

Teaching and learning method

Lecture and tutorials or problem classes seminars

Lectures will provide the theoretical foundations of this unit. Practice classes will supplement this material with design examples. Laboratories will provide students a hands-on learning.

Learning outcomes

1. To extend semiconductor theory to additional electronic devices and to integrated circuit structures.
2. To gain more detailed knowledge and understanding of electronic amplifier circuits, and to understand how transistors and electronics are used in higher frequency and oscillator applications.
3. Introduce feedback, stability and dominant pole compensation.
4. To understand SISO control systems, state space modelling and their relationship to transfer functional representation.
5. To introduce discrete-time/sampled-data control systems.

To extend the ability and practical skills to:

6. design electronic circuits using simulation tools and construct, debug and verify the operation of electronic circuits in the laboratory.
7. design and experimentally verify the operation of SISO control systems.

Your feedback to us

One of the formal ways students have to provide feedback on teaching and their learning experience is through the Student Evaluation of Teaching and Units (SETU) survey. The feedback is anonymous and provides the Faculty with evidence of aspects that students are satisfied with and areas for improvement.

Previous student evaluations of this unit

In response to previous SETU results of this unit, the following changes have been made:

- Practical examples of transistor circuits will be added.

Student feedback has highlighted the following strength(s) in this unit:

- Recording of lectures and tutorials.

If you wish to view how previous students rated this unit, please go to:
https://unitevaluations.connect.monash.edu.au/unitevaluations/index.jsp

Unit schedule - Clayton campus

Week	Lecture	Prac	Lab	Assignment activity
1 **24 July**	One transistor amplifiers (FET's and BJT's) – Jaeger chapter 14			
	One transistor amplifiers (FET's and BJT's) – Jaeger chapter 14			
2 **31 July.**	One transistor amplifiers (FET's and BJT's) – Jaeger chapter 14	Exercises on single transistor amplifiers	Design of one transistor amplifiers	Lab mark
	Differential amplifiers – Jaeger chapter 15			
3 **7 Aug.**	Differential amplifiers – Jaeger chapter 15	Exercises on differential pairs	Current mirrors	Lab mark
	Differential amplifiers –			

	Jaeger chapter 15			
4 **14 Aug**	Current mirrors – Jaeger chapter 16	Exercises on current mirrors	Multistage amplifiers	Lab mark
	Current mirrors – Jaeger chapter 16			
5 **21 Aug**	Current mirrors – Jaeger chapter 16	Exercises on opamp design	Differential amplifiers	Lab mark
	Frequency response – Jaeger chapter 17			
6 **28 Aug**	Frequency response – Jaeger chapter 17 + REVISION	Exercises on Miller compensation and pole splitting		
7 **4 Sept**	Input-output model and analysis of discrete time control systems	Exercise on continuous feedback control systems	Analogue control of dc motor speed (group 1+2)	Lab mark
8 **11 Sept**	Sampled data control systems and discrete equivalents	Exercise on discrete time I /O models and analysis	Analogue control of dc motor speed (group 3+4)	Lab mark
9 **18 Sept**	Emulation and direct designs of digital control	Exercise on digital controller design	Digital control of dc motor speed (group 1+2)	Lab mark
Semester break				
10 **2 Oct**	State Space Model and Analysis of discrete time systems	Exercise on direct designs of digital control	Digital control of dc motor speed (group 3+4)	Lab mark
11 **9 Oct**	State Space Based Design of Digital Control Systems	Exercise on state space analysis and control design	State feedback control of DC motor speed (group 1+2)	Lab mark
12 **16 Oct**	State Space Based Design of Digital Control Systems	Exercise on state space analysis and control design	State feedback control of DC motor speed (group 3+4)	Lab mark

	Revision			
13	**SWOTVAC**			
	Examination period LINK to Assessment Policy: http://www.policy.monash.edu/policy-bank/academic/education/assessment/assessment-in-coursework-policy.html			

Assessment requirements

Assessment summary

Continuous assessment: 40%
Examination (2 hours): 60%
Students are required to achieve at least 45% in the total continuous assessment component (assignments, tests, mid-semester exams, laboratory reports) and at least 45% in the final examination component and an overall mark of 50% to achieve a pass grade in the unit. Students failing to achieve this requirement will be given a maximum of 45% in the unit.

Assessment task	Value	Due date
Laboratory safety and equipment briefing	Compulsory before attending any laboratory session	Week 2
Laboratory experiments	15% of the total mark (7.5% for the electronics laboratories, and 7.5% for the control laboratories)	N/A
Assignments evaluating the electronics and control part of the unit	25% of the total mark (12.5% for each assignment)	Weeks 6 and 12
Final examination	60% of the total mark	To be advised

Hurdle requirements

Students are required to achieve at least 45% in the total continuous assessment component (assignments, tests, mid-semester exams, laboratory reports) and at least 45% in the final examination component and an overall mark of 50% to achieve a pass grade in the unit. Students failing to achieve this requirement will be given a maximum of 45% in the unit.

Assessment tasks

Assessment title: Laboratory safety and equipment briefing
Mode of delivery: Moodle.
Details of task: Laboratory safety and equipment briefing. Completing this assignment is compulsory.
Release dates (where applicable): Week 1
Word limit (where applicable): N/A
Due date: Week 2
Value: Compulsory before attending any laboratory session
Presentation requirements: N/A.
Hurdle requirements (where applicable): Compulsory before attending the labs
Individual assessment in group tasks (where applicable): N/A
Criteria for marking: Completing the laboratory safety and briefing session in Moodle is a mandatory requirement before students are allowed to undertake laboratory work. Students who have not completed and obtained full marks on the safety briefing quiz on Moodle will not be allowed to participate in the laboratory. In order to complete the laboratory and safety briefing quiz, students need to read and understand the Laboratory Safety Procedures and Electrical Safety lecture slides (Moodle).
Additional remarks: N/A

Assessment title: Laboratory experiments
Mode of delivery: Laboratory
Details of task: Each student will do 4+3 specified experiments, scheduled throughout the semester. Students will work in groups of 2. Laboratory sessions are 2 hours. Each laboratory will be marked out of 10 for laboratory achievement, work quality and cooperation.
Release dates (where applicable): N/A
Word limit (where applicable): N/A
Due date: N/A
Value: 15% of the total mark (7.5% for the electronics laboratories, and 7.5% for the control laboratories)
Presentation requirements: N/A
Hurdle requirements (where applicable): 45% hurdle for the total continuous assessment component (laboratory experiments + the two assignments).
Individual assessment in group tasks (where applicable): N/A
Criteria for marking: Students coming more than 10 minutes late to an experimental session will not be allowed to do the experiment. Laboratory achievement will be assessed by demonstrators at the end of the laboratory, and will be based on level of student preparedness, level of completion of experimental work and general level of competency and understanding shown during the laboratory session. The assessment will also be based on completeness of procedure and results recorded during the laboratory session, and level of understanding reflected in any comments recorded as part of the experimental work. Results need be entered in only one laboratory record book for each group for each experiment. Students will be marked as a group of 2 for this part of the assessment.
Additional remarks: N/A

Assessment title: Assignments evaluating the electronics and control part of the unit
Mode of delivery: Moodle
Details of task: Students will need to complete two assignments: the first will assess the electronics part of the unit, and the second will assess the control part of the unit.
Release dates (where applicable): Weeks 6 and 12
Word limit (where applicable): N/A
Due date: Weeks 6 and 12

Value: 25% of the total mark (12.5% for each assignment)
Presentation requirements: N/A
Hurdle requirements (where applicable): 45% hurdle for the total continuous assessment component (laboratory experiments + the two assignments).
Individual assessment in group tasks (where applicable): N/A
Criteria for marking: N/A
Additional remarks: N/A

Examination(s)

Exam title: Final examination
Weighting: 60% of the total mark
Length: 2 hours writing time
Type (Open/closed book): closed book
Hurdle requirements (where applicable): 45%
Electronic devices allowed: Faculty approved calculator
Remarks (where applicable): The formal examination will be held after the completion of the unit, and constitutes 60 % of the overall assessment of this unit. The test will be marked out of 100 (45 % hurdle).

Calculators
A list of the Faculty of Engineering approved calculators and the process for obtaining a sticker is available online at:
http://www.eng.monash.edu.au/current-students/calculators.html

IMPORTANT: Only these listed calculators with the **authorised Monash University-Science or Monash University-Engineering STICKER** will be allowed into the examination by the invigilators.

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Section B: For Malaysia students

Academic Overview

Program Education Objectives
The Electrical and Computer Systems engineering discipline expects to produce graduates, who are:
1. competent in Electrical and Computer Systems engineering
2. responsible and effective global citizens
3. leaders in their chosen profession or society at large.

Program Outcomes
The Electrical and Computer Systems engineering discipline has developed a set of Program Outcomes (POs) for all of its graduates based on the competencies required by the Malaysian Engineering Accreditation Council.

Program Outcomes (POs)	Activities used in this unit to develop POs, achievement of Bloom's domains and complex problem solving
PO1 **Electrical and Computer Systems Engineering Knowledge:** Apply knowledge of mathematics, natural science, engineering fundamentals and specialisation in Electrical and Computer Systems engineering to the solution of complex engineering problems	Cognitive: 1. Apply underlying principles of semiconductor components such as diodes, BJTs, FETs, resistors, capacitors and inductors to design complex electronic subsystems and integrated circuits including single and multistage electronic amplifiers, differential amplifiers, current mirrors and operational amplifiers. 2. Apply underlying principles of control engineering such as feedback, stability, dominant pole compensation, controllability, observability etc. to design complex control systems for discrete data SISO/MIMO systems including transform based emulations and state-space modelling representations
PO2 **Problem Analysis:** Identify, formulate, survey research literature and analyse complex Electrical and Computer Systems engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences	Cognitive:
PO3 **Design/Development of Solutions:** Design solutions for complex Electrical and Computer Systems engineering problems and design systems, components or processes that meet specified needs.	Cognitive: Psychomotor:
PO4 **Research-based Investigation:** Conduct investigations of complex Electrical and Computer Systems engineering problems using research-based knowledge and research methods including design of experiments, (analysis and interpretation of data, and synthesis of information to provide valid conclusions.	Cognitive:

Program Outcomes (POs)	Activities used in this unit to develop POs, achievement of Bloom's domains and complex problem solving
PO5 **Modern Tool Usage:** Create, select and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modelling, to complex Electrical and Computer Systems engineering problems, with an understanding of the limitations	Cognitive: Psychomotor:
PO6 **Engineer and Society:** Apply reasoning informed by contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to professional engineering practice and solutions to complex Electrical and Computer Systems engineering problems	Affective:
PO7 **Environment and Sustainability:** Understand and evaluate the sustainability and impact of professional engineering work in the solution of complex Electrical and Computer Systems engineering problems in environmental contexts.	Cognitive: Affective:
PO8 **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of engineering practice.	Affective:
PO9 **Communication:** Communicate effectively on complex Electrical and Computer Systems engineering activities with the engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions	Affective:
PO10 **Individual and Team work:** Function effectively as an individual, and as a member or leader in diverse teams and in multi-disciplinary settings	Affective:
PO11 **Lifelong Learning:** Recognise the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change	Affective:
PO12 **Project Management and Finance:** Demonstrate knowledge and understanding of engineering management principles and economic decision-making and apply these to manage projects	Cognitive: Affective:

Teaching and learning method

Lecture, Tutorials and Laboratory-based classes

Face-to-face lectures will provide a learning environment for theoretical fundamentals of the unit. Several active learning and engaging strategies such group discussion, pause for reflection, think-pair-share and informal quiz are embedded to the face-to-face lectures to enhance students learning experience. These active learning and engaging strategies are also expected to provide an opportunity for ongoing feedback.

Tutorials will provide an opportunity for problem-based learning; taking the concepts from the lectures and providing concrete examples of their application.

Laboratory-based classes will also provide a problem-based learning environment with elements of enquiry-based and hands-on approaches. They allow students to work on their skills in analysis.

Learning outcomes

1. To extend semiconductor theory to additional electronic devices and to integrated circuit structures.
2. To gain more detailed knowledge and understanding of electronic amplifier circuits, and to understand how transistors and electronics are used in higher frequency and oscillator applications.
3. Introduce feedback, stability and dominant pole compensation.
4. To understand SISO control systems, state space modelling and their relationship to transfer functional representation.
5. To introduce discrete-time/sampled-data control systems.

To extend the ability and practical skills to:

6. design electronic circuits using simulation tools and construct, debug and verify the operation of electronic circuits in the laboratory.
7. design and experimentally verify the operation of SISO control systems.

OBE requirements to learning outcomes (LOs)

Learning Outcomes (LOs) for Outcome Based Education (OBE) requirements	*Handbook Learning Outcomes (LOs)*
LO1) Apply underlying principles of semiconductor components such as diodes, BJTs, FETs, resistors, capacitors and inductors to design complex electronic subsystems and integrated circuits including single and multistage electronic amplifiers, differential amplifiers, current mirrors and operational amplifiers.	LO1) To extend semiconductor theory to additional electronic devices and to integrated circuit structures. LO2) To gain more detailed knowledge and understanding of electronic

Learning Outcomes (LOs) for Outcome Based Education (OBE) requirements	*Handbook Learning Outcomes (LOs)*
	amplifier circuits, and to understand how transistors and electronics are used in higher frequency and oscillator applications. LO6) Design electronic circuits using simulation tools and construct, debug and verify the operation of electronic circuits in the laboratory.
LO2) Apply underlying principles of control engineering such as feedback, stability, dominant pole compensation, controllability, observability etc. to design complex control systems for discrete data SISO/MIMO systems including transform based emulations and state-space modelling representations	LO3) To understand SISO control systems, state space modelling and their relationship to transfer functional representation. LO4) To introduce discrete-time /sampled-data control systems. LO5) To introduce discrete-time /sampled-data control systems. LO7) Design and experimentally verify the operation of SISO control systems.

Relationship between unit learning outcomes and program outcomes

No.	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
LO1	√											
LO2	√											
LO3												
LO4												
LO5												
LO6												
LO7												

Your feedback to us

One of the formal ways students have to provide feedback on teaching and their learning experience is through the Student Evaluation of Teaching and Units (SETU) survey. The feedback is anonymous and provides the Faculty with evidence of aspects that students are satisfied with and areas for improvement.

Previous student evaluations of this unit

In response to previous SETU results of this unit, the following changes have been made:

Based on the SETU comments of the last offer on learning activities and materials, for example, "improvement in the lecture material as they are hard to understand" and "a bit more interactive and more interesting so students are engaged and involve", following changes are introduced:

1. introduce several in-class active learning sessions including brainstorming-in-a-group, think-pair-share, quiz and pause-for-reflection. These are expected to offer immediate feedback on the amount of learning happening and can be used to upgrade/update the course delivery tasks.

2. complexity of the harder topics will be toned down by introducing post-class directed practices.

Student feedback has highlighted the following strength(s) in this unit:

Tutorial sessions were good

The mid semester exams were helpful.

If you wish to view how previous students rated this unit, please go to:
https://emuapps.monash.edu.au/unitevaluations/index.jsp

Unit schedule - Malaysia campus

Week	Lecture	Prac	Lab	Assignment activity
1	Introduction to the unit	N/A	N/A	N/A
	Revision: One transistor amplifiers (FET's and BJT's) – Jaeger chapter 14			
2	Revision: One transistor amplifiers (FET's and BJT's) – Jaeger chapter 14	Elec. Tute 1	N/A	N/A
	Differential amplifiers – Jaeger chapter 15			
3	Differential amplifiers – Jaeger chapter 15	Elec. Tute 2	Elec. Lab 1	N/A
	Differential amplifiers – Jaeger chapter 15			
4	Current mirrors – Jaeger chapter 16	Elec. Tute 3	N/A	N/A
	Current mirrors – Jaeger chapter 16			
5	Current mirrors – Jaeger chapter 16	Elec. Tute 4	Elec. Lab 2	Elec. Lab Report 1
	Frequency response – Jaeger chapter 17			
6		Elec. Tute 5	N/A	N/A

	Frequency response – Jaeger chapter 17 + Electronics Mid-Sem Exam			
7	Input-output model and analysis of discrete time control systems	Control Tute 1	Elec. Lab 3	Elec. Lab Report 2
8	Sampled data control systems and discrete equivalents	Control Tute 2		N/A
9	Emulation and direct designs of digital control	Control Tute 3	Control Lab 1	Elec. Lab Report 3
10	State Space Model and Analysis of discrete time systems + Control Mid Semester Exam	Control Tute 4		N/A
11	State Space Based Design of Digital Control Systems	Control Tute 5	Control Lab 2	Control Lab Report 1
12	State Space Based Design of Digital Control Systems + Revision	Revision		Control Lab Report 2
13	**SWOTVAC**			
	Examination period LINK to Assessment Policy: http://www.policy.monash.edu/policy-bank/academic/education/assessment/assessment-in-coursework-policy.html			

Assessment Summary

Continuous assessment: 40%
Examination (2 hours): 60%

Students are required to achieve at least 45% in the total continuous assessment component (assignments, tests, mid-semester exams, laboratory reports) and at least 45% in the final examination component and an overall mark of 50% to achieve a pass grade in the unit. Students failing to achieve this requirement will be given a maximum of 45% in the unit.

Assessment task	Value	Due date
Laboratory Exercise - participating in lab classes - producing satisfactory lab results - submitting lab reports	15%	Submit previous week's lab report before resuming the current week's lab activity
Two Mid Semester Examinations (MSE) - MSE, Electronics 10% - MSE, Control 10%	20% (10% each)	6th and 10th weeks of the semester
In-class Active Learning Activity	5%	On going
Final Exam	60%	TBA

Hurdle requirements

Students are required to achieve at least 45% in the total continuous assessment component (assignments, tests, mid-semester exams, laboratory reports) and at least 45% in the final examination component and an overall mark of 50% to achieve a pass grade in the unit. Students failing to achieve this requirement will be given a maximum of 45% in the unit.

Bloom's Taxonomy:
Three domains of educational activities have been identified under the general taxonomy known as Bloom's.

- **Cognitive**: mental skills (*Head*)
- **Affective**: growth in feelings or emotional areas (*Heart*)
- **Psychomotor**: manual or physical skills (*Hand*)

The *cognitive* domain involves knowledge and the development of intellectual skills. This includes the recall or recognition of specific facts, procedural patterns, and concepts that serve in the development of intellectual abilities and skills.

The *affective* domain includes the attitudes with which someone deals with things emotionally, such as feelings, values, appreciation, enthusiasms and motivations.

The *psychomotor* domain includes physical movement, coordination, and use of the motor-skill areas. Development of these skills requires practice and is measured in terms of speed, precision, distance, procedures, or techniques in execution.

Key for the LO-assessment relationship table above:

Cognitive

C1	C2	C3	C4	C5	C6
Knowledge: Remembers previously learned material	**Comprehension:** Grasps the meaning of material (lowest level of understanding)	**Application:** Uses learning in new and concrete situations (higher level of understanding)	**Analysis:** Understands both the content and structure of material	**Synthesis:** Formulates new structures from existing knowledge and skills	**Evaluation:** Judges the value of material for a given purpose

Psychomotor

P1	P2	P3	P4	P5	P6	P7
Perception: Senses cues that guide motor activity	**Set:** Is mentally, emotionally and physically ready to act	**Guided Response:** Imitates and practices skills, often in discrete steps	**Mechanism:** Performs acts with increasing efficiency, confidence and proficiency	**Complete Overt Response:** Performs automatically	**Adaption:** Adapts skill sets to meet a problem situation	**Organisation:** Creates new patterns for specific situations

Affective

A1	A2	A3	A4	A5
Receiving: Selectively attends to stimuli	**Responding:** Responds to stimuli	**Valuing:** Attaches value or worth to something	**Organisation:** Conceptualises the value and resolves conflict between it and other values	**Internalising:** Integrates the value into a value system that controls behaviour

Relationship between Assessments and OBE Learning Outcomes (LOs)

	Assessment	Learning Outcomes				
		LO1	LO2			
1	Laboratory Exercise	P6	P6			
2	Mid-Semester Exam	C6	C6			
3	Final Exam	C6	C6			
4	In-class Active Learning Activity	C5	C5			

Relationship between Assessments and Complex Problems /Activities

		Complex Problems (CP)							Complex Activities (CA)		O en L
	Assessment	WP1	WP2	WP3	WP4	WP5	WP6	WP7	EA1	...	
1	Laboratory Exercise	x	x					x			
2	Mid-Semester Exam	x	x					x			
3	Final Exam	x	x					x			
4	In-class Active Learning Activity	x	x					x			

Assessment requirements

Assessment tasks

Assessment title: Lab Activity: Participating in lab classes, producing satisfactory lab results and submitting lab reports
Mode of delivery: On Campus
Details of task: Lab participation, completion of tasks, and submitting reports
Release dates (where applicable): Ongoing
Word limit (where applicable): N/A
Due date: .
Value: 15%
Presentation requirements: No
Hurdle requirements (where applicable): Built-in within continuous assessment's hurdle requirements. Lab attendance is essential
Individual assessment in group tasks (where applicable): Yes
Criteria for marking: Proactive lab participation (30%), producing satisfactory results (30%), and timely completion and submission of lab report (40%)
Additional remarks: ..

Assessment title: Two Mid-Semester Exams
Mode of delivery: On Campus
Details of task: Written examination, closed book, calculator allowed. Preparation on the lecture notes and tutorials as of approximately 50% (25% each) of total course contents altogether.
Release dates (where applicable): .

Word limit (where applicable): N/A
Due date: Exam will be held on Tuesday's lecture time at the lecture venue on the 6th and 10th week of the semester. Exam time 20-30 minutes each.
Value: 20% (10% each)
Presentation requirements: No
Hurdle requirements (where applicable): Built-in within continuous assessment's hurdle requirements
Individual assessment in group tasks (where applicable): N/A
Criteria for marking: Answering the questions correctly. Partial marking may be considered if the steps towards correct answers are correct, but made mistakes in calculations.
Additional remarks: .

Assessment title: In-class Active Learning Activity
Mode of delivery: On Campus
Details of task: Group discussion, pause for reflection, think-pair-share and brianstorming sessions during the face-to-face lectures

Release dates (where applicable): On going
Word limit (where applicable): N/A
Due date: On going
Value: 5%
Presentation requirements: N/A
Hurdle requirements (where applicable): Built-in within continuous assessment's hurdle requirements
Individual assessment in group tasks (where applicable): Yes
Criteria for marking: Proactive participation to the planned activities. Only the activities undertaken in the first lecture of the week (Mondays) will be graded.

Additional remarks: .

Examination(s)

Exam title: Final Exam
Weighting: 60%
Length: 2 hours
Type (Open/closed book): Closed book
Hurdle requirements (where applicable): Yes
Electronic devices allowed: Calculators are allowed
Remarks (where applicable): Answering the questions correctly. Partial marking may be considered if the steps towards correct answers are correct but made mistakes in calculations.

Calculators

A list of the Faculty of Engineering approved calculators and the process for obtaining a sticker is available online at:
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Section C: All students

Plagiarism and collusion

Intentional plagiarism or collusion amounts to cheating under Part 7 of the Monash University (Council) Regulations.

Plagiarism: Plagiarism means taking and using another person's ideas or manner of expressing them and passing them off as one's own. For example, by failing to give appropriate acknowledgement. The material used can be from any source (staff, students or the internet, published and unpublished works).

Collusion: Collusion means unauthorised collaboration with another person on assessable written, oral or practical work and includes paying another person to complete all or part of the work. Where there are reasonable grounds for believing that intentional plagiarism or collusion has occurred, this will be reported to the Associate Dean (Education) or delegate,

Referencing requirements

N/A

To build your skills in citing and referencing, and using different referencing styles, see the online tutorial Academic Integrity: Demystifying Citing and Referencing at http://www.lib.monash.edu.au/tutorials/citing/

Assignment submission

Hard Copy Submission:

N/A

Online Submission: If Electronic Submission has been approved for your unit, please submit your work via the Moodle site or other; as directed by your demonstator for this unit.
Please keep a copy of tasks completed for your records.

Feedback to you

Feedback will be verbal.

Learning resources

Prescribed textbooks

- Richard C. Jaeger, Travis N. Blalock, “Microelectronic Circuit Design”, McGraw-Hill, 4th Ed., 2011.
- G. F. Franklin, D. Powell, A. Emami-Naeini, “Feedback Control of Dynamic Systems”, Sixth Edition, Prentice-Hall, 2009.

Monash Library Unit Reading List (if applicable to the unit):
http://readinglists.lib.monash.edu/index.html

Required resources

Students generally must be able to complete the requirements of their course without the imposition of fees that are additional to the student contribution amount or tuition fees. However, students may be charged certain incidental fees or be expected to make certain purchases to support their study. For more information about this, go to Administrative Information for Higher Education Providers: Student Support, Chapter 21, Incidental Fees at: http://www.innovation.gov.au/HigherEducation/TertiaryEducation/ResourcesAndPublications/Pages/default.aspx

Technological requirements

Required software (and/or hardware)

- Altium (licenses are available in the lab).
- Sunway: Matlab

Equipment and consumables required or provided

- Electronic prototyping board (supplied by department).
- Electronics components for laboratory sessions (supplied by department).

Other information

Policies

Monash has educational policies, procedures and guidelines, which are designed to ensure that staff and students are aware of the University's academic standards, and to provide advice on how they might uphold them. You can find Monash's Education Policies at:
http://www.policy.monash.edu/policy-bank/academic/education/index.html

Graduate Attributes Policy

http://www.monash.edu/policy-bank/academic/education/course-governance-and-design/course-design-policy

Student Charter

http://www.monash.edu/students/policies/student-charter.html

Student Services

The University provides many different kinds of services to help you gain the most from your studies. Contact your tutor if you need advice and see the range of services available at http://www.monash.edu/students.

Malaysia students go to: http://www.monash.edu.my/Student-services/.

Monash University Library

The Monash University Library provides a range of services, resources and programs that enable you to save time and be more effective in your learning and research.
Go to http://www.monash.edu/library or the library tab in http://my.monash.edu.au portal for more information.

For Malaysia students the Library and Learning Commons, Monash University Malaysia Campus, provides a range of services and resources that enable you to save time and be more effective in your learning and research.
Go to http://www.lib.monash.edu.my or the library tab in my.monash portal for more information.

Disability Support Services

Students who have a disability, ongoing medical or mental health condition are welcome to contact Disability Support Services.

Disability Support Services also support students who are carers of a person who is aged and frail or has a disability, medical condition or mental health condition.

Disability Advisers visit all Victorian campuses on a regular basis.

- Website: monash.edu/disability
- Telephone: 03 9905 5704 to book an appointment with an Adviser;
- Email: disabilitysupportservices@monash.edu
- Drop In: Level 1, Western Annexe, 21 Chancellors Walk (Campus Centre) Clayton Campus

At Malaysia campus, for information and referral, telephone: Student Adviser, Student Community Services at 03 55146018 or, drop in at Student Community Services Department, Level 2 Building 2, Monash University Malaysia Campus.