Optimizing Distributed ML Communication with Fused Computation-Collective Operations

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Abstract—In order to satisfy their ever increasing capacity and compute requirements, machine learning models are distributed across multiple nodes using numerous parallelism strategies. As a result, collective communications are often on the critical path, and hiding their latency by overlapping kernel-granular communication and computation is difficult due to the absence of independent computation.

In this work, we propose fusing computation with dependent collective communication by leveraging GPUs' massive parallelism and GPU-initiated communication. We have developed self-contained GPU kernels where threadblocks/workgroups (WGs) immediately communicate their results to remote GPUs when they complete their computation. Meanwhile, other WGs within the same kernel perform overlapping computation, maintaining high ALU utilization. Such fine-grain overlapping provides the additional benefit that peak network bandwidth demand is reduced and communication is spread across the entire lifetime of application rather than only at kernel boundaries. Furthermore, we propose zero-copy optimizations for scale-up communication where the data computed by one GPU is directly communicated to peer GPUs, eliminating intermediate stores and buffering.

We demonstrate our approach by creating three prototype fused operators (embedding + All-to-All, GEMV + AllReduce, and GEMM + All-to-All) to address the pervasive communication overheads observed in deep learning recommendation models (DLRM), Transformers and Mixture of Experts (MoE) model architectures. In order to demonstrate that our approach can be integrated into ML frameworks for wide adoption in production environments, we expose our fused operators as new PyTorch operators as well as extend the Triton framework to enable them. Our evaluations show that our approach can effectively overlap communication with computations, subsequently reducing their combined execution time than the current collective library-based approaches. Our scale-up GEMV + AllReduce and GEMM + All-to-All implementations achieve 13% (up to 22%) and 12% (up to 20%) lower execution time, while our fused embedding + All-to-All reduces execution time by 20% and 31% for intra-node and inter-node configurations. Large scale-out simulations indicate that our approach reduces DLRM execution time by 21% for 128 node system.

Index Terms—GPU, distributed ML, collective communication, DLRM, Transformers, MoE

I. INTRODUCTION

Machine learning is currently being used across a wide variety of applications ranging from classification (e.g., fraud detection, medical diagnostics, facial recognition), pattern analysis (e.g., product recommendations, stock price prediction) to content generation (e.g., code generation, chatbots, image/video generation). Machine learning (ML) models are increasing in size to tackle more complex problems. Studies [57]

(a) Traditional node design
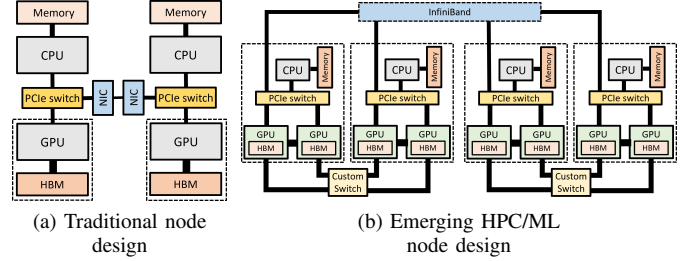
(b) Emerging HPC/ML node design

Fig. 1: System architecture trends.

have shown that the model sizes have increased by five orders of magnitude between 2018 to 2022. Large ML models have consequently fueled the development of distributed systems capable of meeting their capacity and compute requirements. Subsequently, parallelization techniques have been developed to efficiently map ML models on to distributed systems [11]. The resulting communication in distributed ML models (e.g., weight updates, activation exchanges between layers, etc.) are difficult to hide due to absence of independent computation and thereby become a significant bottleneck [39], [47] as the system scale grows.

ML trends are also influencing system design and architecture development. Figure 1 compares a traditional CPU-GPU multi-node system with a state-of-the-art node design optimized for HPC/ML. Other than compute and memory improvements, we notice two broad trends. Firstly, intra- and inter-node communication bandwidth and latency have been improved using proprietary interconnects [4], [18] and high-bandwidth network interface cards (NICs). Secondly, given the increased preference to use GPUs for ML workloads, GPUs are becoming the primary computation engine tightly integrated with on-node CPUs, GPUs and are directly communicating with the network using high-radix switches [16] or direct-attached NICs [2], [27]. However, applications have yet to fully embrace these trends and often rely on the CPU [34], [46] to perform remote communication. While progress has been made to remove CPUs from the data path, for example, GPUDirect RDMA [6], [9] enables data to be directly moved between GPU memory and NIC, communication is still triggered by the host CPU and often at kernel boundaries. Such approaches are mostly suitable for bulk-synchronous applications where communication can be overlapped with independent computation at the kernel granularity and the kernel-launch overhead is amortized using large kernels.

In this paper, we aim to address the growing bottleneck of collective communication by fusing and overlapping communication and dependent computation using intra-kernel GPU-initiated networking. Recent GPU micro-architectural features (e.g., GPU cache flush instructions [5], threadblock cluster [17]) have made GPU-initiated networking operations performant and thus a pragmatic option. Our approach is easy to apply and leverages the existing threadblock/workgroup[1]-level work partitioning in GPU applications and does not require any hardware changes. We have developed self-contained, persistent GPU kernels [45] where one or more logical WGs upon completing their share of computations, issue non-blocking transactions to communicate their results to remote GPUs. By immediately scheduling non-blocking network transactions, data fragments are communicated as they are computed without waiting for kernel completion.

We demonstrate our approach by creating fused communication-computation kernels, to address the collective bottlenecks in popular ML architectures, such as deep learning recommendation models (DLRM), Transformers, and mixture of experts (MoE). Specifically, we create prototype kernels which fuse embedding pooling, matrix-vector multiplication (GEMV), matrix-matrix multiplications (GEMM) with collectives (All-to-All, and AllReduce). Our approach can be used to fuse both inter-node (e.g., RDMA) and intra-node GPU communication. For the locally communicated data, we develop zero-copy fused kernels where the GPU threads directly store their computed results to collective destination buffers. We also demonstrate the different ways such fused operators can be integrated within ML frameworks. Specifically we expose the new fused communication-computation kernel as a new operator within PyTorch [21] and extend *Triton* (Python-like language framework to develop highly efficient GPU code [29] integrated with PyTorch [1]) to include the necessary communication primitives to develop custom fused kernels.

This paper makes the following key contributions:

- We propose a novel approach to fuse computation and collective communication within the same kernel, thus overlapping collective communication, and reducing peak bandwidth. Further, we propose zero-copy fused kernels where the results are directly written to the peer GPU memory thereby eliminating intermediate buffering and copy operations.
- We develop three first of their kind fused communication-computation prototype kernels to address the collective overhead in DLRM, Transformers, and MoE architectures. Specifically, we develop *embedding pooling + All-to-All*, *GEMV + AllReduce*, and *GEMM + All-to-All* fused operators. Our evaluations show that our fused operators achieve 31%, 13% and 12% lower latency respectively.
- We implement two different approaches to integrate fused operators within ML frameworks. 1) We expose fused

communication-computation kernel as a new operator within PyTorch to be transparently used by developers. 2) We extend Triton framework to include communication primitives allowing users to develop custom fused kernels catering to their needs. In this work, we use our Triton extensions to develop *GEMM + All-to-All* kernel.
- We evaluate the trade-offs for using GPU-initiated communication and highlight the factors critical (e.g., occupancy) to achieve effective overlap with low overhead.

II. BACKGROUND

In this section, we first illustrate the communication bottleneck observed in several distributed ML applications: DLRM, Transformers, and MoEs. We then provide a background on GPU-initiated communication and intra-kernel networking.

A. Collectives in Distributed ML Models

Large ML models use parallelism strategies (e.g., tensor parallelism, model parallelism, fully-sharded data parallelism (FSDP) [8]) to avoid data duplication across distributed nodes. However, such strategies result in additional collective communication to train and execute the models.

DLRM (Embedding + All-to-All): Recommendation models are widely deployed for ranking and click through rate predictions tasks. Due to the large memory requirements of embedding tables, DLRMs typically employ model parallelism for distributing embedding tables (table, row, and column parallelism [47]) across GPUs [48]. The top multi-layer perceptron (MLP) layers of DLRM use data parallelism for scaling across multiple GPUs. In order to switch from model parallelism execution (for embedding operations) to data parallelism (for top MLP layers), All-to-All collective operations are used [48] as shown in Figure 2. Note that bottom MLP layers are the only independent computation available to be overlapped with the All-to-All collective but are usually small and thus cannot hide communication effectively. Prior research has shown that All-to-All latency is significantly exposed (>35%) and has direct impact on overall latency in state-of-the-art systems [47].
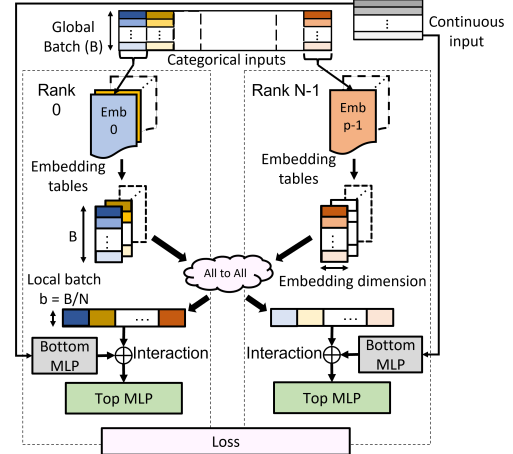

Fig. 2: DLRM forward pass.

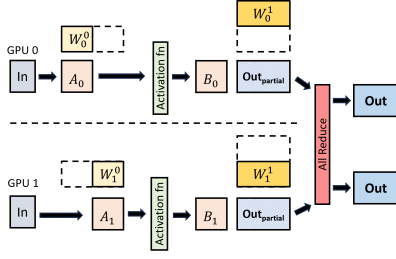[1]Workgroup is the OpenCL equivalent of CUDA threadblock

Fig. 3: Model parallelism in Transformer MLP layer [55].

Hiding the All-to-All collective will require overlapping it with dependent computations (embedding pooling or top MLP), which is not possible with the existing bulk-synchronous kernel execution. In this work, we overlap All-to-All communication with the embedding pooling operator by communicating fragments of pooling output data as they are computed. Since embedding pooling operation is parallelized across independently executing WGs, output computed by single or cluster of WGs can be communicated independent of others without violating data-dependencies.

Transformers (GEMV + AllReduce): Transformers have become a popular ML model architecture for natural language processing, machine translation, and text generation tasks. Auto-regressive Transformers (e.g., GPT, Llama2) leverage the prior tokens and predict the next tokens iteratively. Their inference consists of two phases [49] 1) *Prompt (or pre-fill) phase*: all input tokens are processed to generate the first token. 2) *Token (or decode) phase*: iterative phase where tokens generated previously along with the inputs are used to predict the next token. Typical models consist of a self-attention layer followed by feed-forward layer and this building block is repeatedly instantiated to create the entire model. The computations associated with these layers are matrix-matrix multiplications (during training, prompt phase of inference) or matrix-vector multiplications (token phase of inference) [50], and are usually combined with element-wise operations (e.g., normalization, addition).

Transformer architectures used in modern language models are too large to fit within a single GPU device and are thus partitioned. Figure 3 shows an example of model parallelism on Transformer feed forward layers as proposed in Megatron-LM [55]. The feed forward layer consists of two linear layers with an activation layer in-between. The weights corresponding to each of the MLP layer are partitioned across the two GPUs, such that weights of the first layer are partitioned column-wise (W_0^0, W_1^0), while weights of second layer are partitioned row-wise (W_0^1, W_1^1). The input is duplicated across both GPUs and multiplied with half of the weights (W^0) in each GPU. The outputs (A_0, A_1) are passed through the activation function before being multiplied with weights of second layer (W^1) to generate the partial outputs ($Out_{partial}$). Finally, the partial outputs are reduced using AllReduce to obtain the final results. This AllReduce operation contributes significantly (up to 46% [50]) towards the inference latency.

Due to lack of independent computation, the AllReduce

collective can only be overlapped with the preceding computation. Since inference latency is very dominated by the token-phase [49] which performs matrix-vector multiplication (assuming no batching), we focus on fusing AllReduce with GEMV computation in this work. GPU kernels for GEMV operation [26] typically divide the computation across WGs, where each WG is responsible for computing a tile of the output vector. These output tiles can be communicated and reduced independently of other tiles. We exploit this opportunity to develop a fused *GEMV + AllReduce* operator.

Mixture of Experts (GEMM + All-to-All): Mixture of Expert (MoE) [54] model architectures are growing in popularity as they allow increasing the model parameters without linearly scaling the computation cost. MoE architectures introduce parallel sub-layers called *experts*, where different MoE layer inputs are passed to only a subset of experts as determined by a gating function. The expert sub-layers are typically feed-forward layers which translate to matrix-matrix multiplication (GEMM) kernels. MoEs' expert-level parallelism [51] [33] map different sub-layers across different GPUs, resulting in two All-to-All collectives, one for distributing the inputs across experts (All-to-All Dispatch) and another to gather the outputs from different experts (All-to-All Combine) as shown in Figure 4. Inputs from four GPUs (In_{0-3}) are distributed to the individual experts (assuming uniform distribution) based on the gating function (G) using All-to-All (dispatch). The All-to-All output is passed as input to individual expert feed forward layer (one per GPU), the output of which is again returned to the original GPU using All-to-All (combine). These All-to-All collectives are in the critical path and adds significant overhead (up to 43% [39]) to the MoE execution time.

The All-to-All collectives can only be overlapped with dependent GEMM operations. Similar to GEMV, WGs of the MoE GEMM kernels compute output tiles independently and thus can be communicated as soon as they are computed. In this work, we consider top-2 routing i.e. each token is communicated to two experts and assume equal workload across experts. We demonstrate our approach by fusing MoE GEMM computation with All-to-All Combine communication.

B. GPU-initiated intra-kernel communication

GPU-based HPC and ML systems typically use GPU-Direct Remote Direct Memory Access (RDMA) [9] and associated
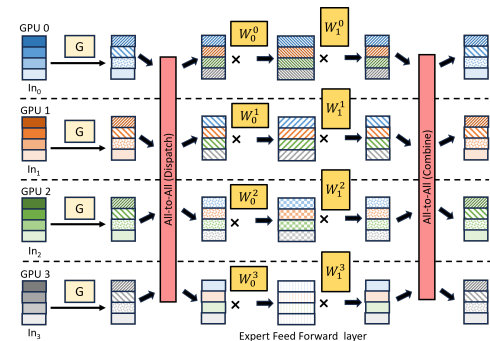

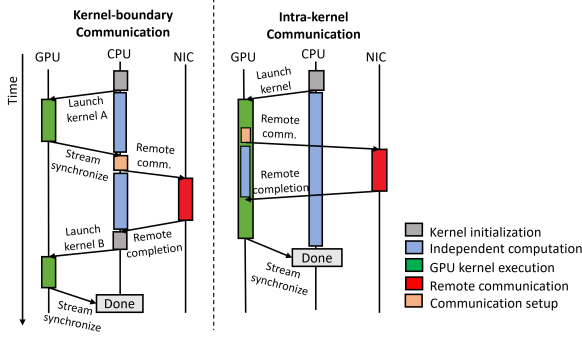Fig. 4: MoE layers distributed across GPUs [39].

Fig. 5: Kernel boundary vs intra-kernel communication

programming models (e.g., CUDA-Aware MPI [6]) to enable direct data transfers between GPU and NIC. Bypassing CPU memory helps achieve better latency and thus these approaches are widely used in HPC [36], [43] and ML (RCCL [23], NCCL [15]). However, such communication is performed at kernel boundaries typically by the host CPU.

GPU-initiated intra-kernel communication allows GPU threads to directly initiate communication with NICs and peer GPUs. Vendor-specific GPU libraries (e.g., NVSHMEM [19], ROC_SHMEM [25], MSCCL++ [14]) have been developed that enable applications to perform intra-kernel GPU-initiated communication. Moreover, recent GPU micro-architecture features are facilitating GPU-initiated networking further. For example, prior versions of ROC_SHMEM required data to be allocated as un-cacheable in order to prevent stale data from being communicated to remote nodes. However, the recent introduction of intra-kernel cache flush instructions [5] allows GPU threads to flush data while the kernel executes to initiate network transactions, while allowing data to be cached during computation. Further, new programming abstractions such as threadblock cluster [17] can enable faster coordination between WGs to perform intra-kernel network communication.

Figure 5 compares and contrasts the system interactions during conventional kernel boundary versus intra-kernel communication. Kernel boundary communication requires the entire computation kernel to complete before the remote/network communication can be triggered (usually by the host CPU). On its completion, CPU then launches the dependent kernel. To overlap communication, techniques such as double-buffering and GPU streams need to be deployed. In the absence of independent work, applications are broken into smaller independent kernels where each smaller kernel is executed as a separate stream and computation of one stream is overlapped with the communication of another. This can result in large number of small kernels and add significant kernel launch and stream management overhead [44], [47], [60]. In contrast, GPU-initiated intra-kernel communication allows GPU threads to issue remote communication while other threads perform their computation, enabling fine-grained communication and computation overlap within a single kernel. Illustration in Figure 5 shows GPUs directly communicating with NICs [37], instead GPU threads can alternatively trigger NIC communi-

cation using a CPU proxy [14].

III. FUSED COMPUTATION AND COMMUNICATION

In this section, we illustrate our fused communication + computation approaches for both scale-out and scale-up configurations. We discuss the design and implementation of *embedding + All-to-All* fused operator to demonstrate our scale-out approach, while we use *GEMV + AllReduce* operator as an example to explain our scale-up approach which avoids intermediate buffering and copy operations.

A. Scale-out: Fused Embedding + All-to-All Operator

We develop the fused embedding + All-to-All operator as a persistent GPU HIP [10] kernel, which performs both embedding pooling (reduction-like) computations and All-to-All communication. We use the ROC_SHMEM [25] library to issue intra-kernel communication and Figure 6 shows its execution. It illustrates a two-node system where embedding tables are distributed in model parallel fashion such that there are four tables per node. The All-to-All output and send buffers are allocated within each GPU's symmetric heap (using *roc_shmem_malloc()* API). Memory allocated within symmetric heap are registered with the NICs, thus allowing NICs to directly move data between these GPU buffers. We implemented our fused *embedding + All-to-All* operator as a persistent thread kernel [35], [45] which multiplexes multiple logical embedding pooling operations onto the long-running WGs executing in the GPU. This allows us to schedule logical WGs computing the same slice (output fragment) together (similar to the approach used in [45]) and further reduces the number of kernel invocations. The kernel is launched with a fixed, input-independent grid size (less than or equal to maximum occupancy as determined from the HIP occupancy API [20]). Each long-running (a.k.a. persistent) WG executes a task loop where every iteration corresponds to the computation performed by a logical WG of the original embedding kernel (*EmbeddingBag_updateOutputKernel_sum_mean*).

Figure 6a shows the logical WGs and is color coded to indicate which tables are processed by the WGs. Our fused kernel takes in categorical inputs and embedding tables as kernel arguments. The illustrated example assumes a global batch size of four, the slice size to be two embedding output vectors, and that each output embedding vector is computed by one WG. The pooled output embedding vectors from each table are shuffled equally across both nodes, with the first half of the global batch stored in node 0 and the second half in node 1. Depending on their embedding slice, the WGs may need to store their results locally or communicate them to the remote node. The index of the slice computed by a WG can be determined using the output embedding entry and the size of the slice. The slice index along with the global batch size and node count can then be used to determine if the slice needs to be communicated remotely. Logical WGs *WG 00 - WG 13* compute the output corresponding to the first half of global batch, while *WG 20 - WG 33* compute the latter half. For node 0, *WG 00 - WG 13* compute the output entries

(a) Example embedding + All-to-All operation

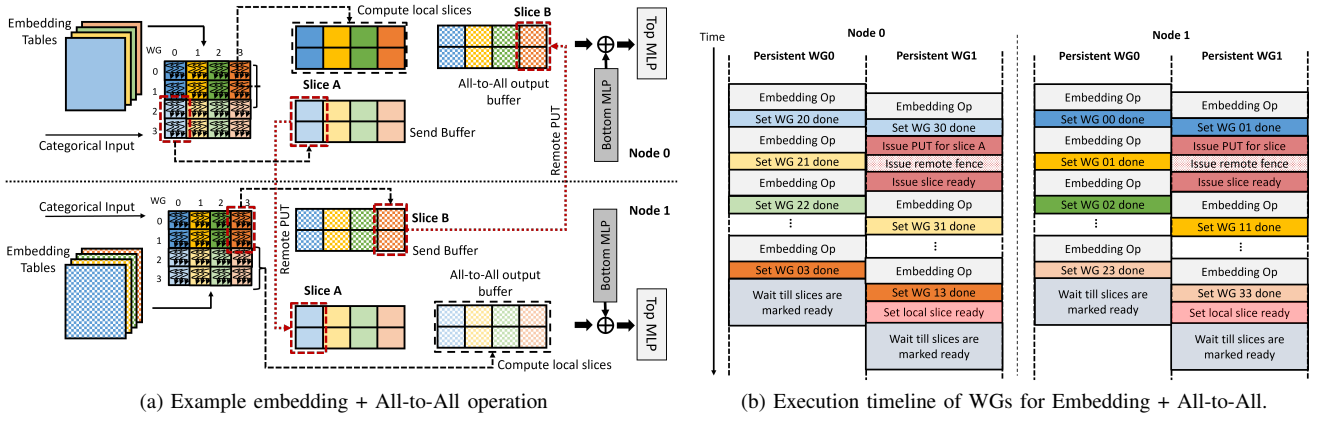(b) Execution timeline of WGs for Embedding + All-to-All.

Fig. 6: Embedding + All-to-All fused operator.

consumed locally, and results of *WG 20 - WG 33* will have to be communicated to node 1. While for node 1, results from *WG 00 - WG 13* are communicated to node 0 and *WG 20 - WG 33* store their results locally.

As described earlier, our approach performs communication at a granularity of a *slice*. The size of each slice is set to match the output computed by one or more WGs. In the example shown in Figure 6a, *WG 20* and *WG 30* compute slice A on node 0. While there can be multiple WGs responsible for computing a single slice, the remote communication to move the slice is initiated by the last WG that finishes the corresponding slice. In the example shown, assume *WG 30* finished its computation for slice A after *WG 20*. Then, a thread from *WG 30* will issue the remote communication (Remote PUT) to move slice A to node 1. We track the completion of logical WGs corresponding to every slice to identify the last completing WG and trigger communication accordingly. Implementing All-to-All using point-to-point transactions allows the communicating WGs to move the slice data to the destination in a layout required by any subsequent kernel (e.g., the interaction operation in DLRM). The output data can be shuffled at a slice granularity without requiring explicit shuffling or rearrangement. In our approach, we generate output with the shape: {local batch size, (numTables × embedding dimension)}, which can then be passed to the *interaction* operator.

Book-keeping Flags: In our approach, we maintain two sets of flags (not shown in Figure 6a) per GPU to synchronize WG communication and determine the end of communication. First, we maintain a *WG_Done* bitmask per slice where each bit indicates the completion status of the logical WGs. This bitmask is used to identify the last finishing WG and issue remote communication. Second, we maintain a *sliceRdy* flag per slice (both locally computed and received remotely) to indicate if all the individual slices have been received or computed. The *sliceRdy* flags are set by GPUs computing and communicating the slices and thus are allocated in symmetric memory. The receiver GPUs poll on *sliceRdy* flags to determine if the slices are ready for consumption.

Communication-aware Scheduling: Figure 6b shows the execution timeline of the persistent WGs for the illustrated example. Consider two persistent WGs per node, where each iteratively performs the work of 16 logical WGs. In our remote communication aware approach, the logical WGs computing slices for remote communication are computed ahead of the WGs computing locally consumed slices, thereby maximizing the opportunity to overlap remote communication. For example, the persistent WGs in node 0 compute *WG 20* and *WG 30* ahead of *WG 00* and *WG 10* so that the remote communication can be overlapped with local slice computation.

Synchronization: Upon completion of each logical WG (an iteration within the task loop), a leader thread sets the bit corresponding to the logical WG in the *WG_Done* bitmask as shown in the timeline. The WG also checks if it is the last one to complete by testing if all the other bits in the bitmask are set. This design allows the WGs to make forward progress after setting their respective *WG_Done* flags instead of waiting on an inter-WG barrier. The last completing WG issues two remote PUT calls separated by a remote fence. The first call is to move the slice data, while the second sets its corresponding *sliceRdy* flag on the remote node. The remote fence ensures that the *sliceRdy* flag is only set after the prior PUT has completed. After executing all the logical WGs, the persistent WGs poll on a distinct subset of *sliceRdy* flags before exiting. This ensures that the data from all slices are ready for subsequent kernels while incurring less overhead than having all WGs poll on the entire set of *sliceRdy* flags. Alternatively, synchronization can be performed using a *quiet()* call along with a barrier per GPU.

B. Scale-up: GEMV + AllReduce

Unlike remote GPUs (scale-out) which require RDMA network transactions to communicate, scale-up communication can be performed using native GPU load/store instructions over Infinity Fabric™ connections [4] or NVLink [18]. We exploit this feature to further optimize our fused kernel for scale-up communication. We create an optimized zero-copy fused kernel, where in-addition to overlapping dependent communication and computation, we eliminate the stores to intermediate buffers by directly writing the output to the peer

GPU 0

Persistent WG0	Persistent WG1
Compute Tile (k/2) / Issue xGMI store	Compute Tile (k/2) + 1 / Issue xGMI store
Compute Tile (k/2) + 2 / Issue xGMI store	Compute Tile (k/2) + 3 / Issue xGMI store
⋮	⋮
Compute Tile k - 2 / Issue xGMI store	Compute Tile k - 1 / Issue xGMI store
Set WG 0 done	Set WG 1 done
Compute Tile 0 / Issue local store	Compute Tile 1 / Issue local store
⋮	⋮
Compute Tile (k/2) - 2 / Issue local store	Compute Tile (k/2) - 1 / Issue local store
Wait for peer WG 0 done	Wait for peer WG 1 done
Reduce Tiles	Reduce Tiles
Broadcast results	Broadcast results

GPU 1

Persistent WG0	Persistent WG1
Compute Tile 0 / Issue xGMI store	Compute Tile 1 / Issue xGMI store
Compute Tile 2 / Issue xGMI store	Compute Tile 3 / Issue xGMI store
⋮	⋮
Compute Tile (k/2) - 2 / Issue xGMI store	Compute Tile (k/2) - 1 / Issue xGMI store
Set WG 0 done	Set WG 1 done
Compute Tile (k/2) / Issue local store	Compute Tile (k/2) + 1 / Issue local store
⋮	⋮
Compute Tile k - 2 / Issue local store	Compute Tile k - 1 / Issue local store
Wait for peer WG 0 done	Wait for peer WG 1 done
Reduce Tiles	Reduce Tiles
Broadcast results	Broadcast results

(a) Example GEMV + AllReduce operation. (b) Execution timeline of WGs for GEMV + AllReduce.
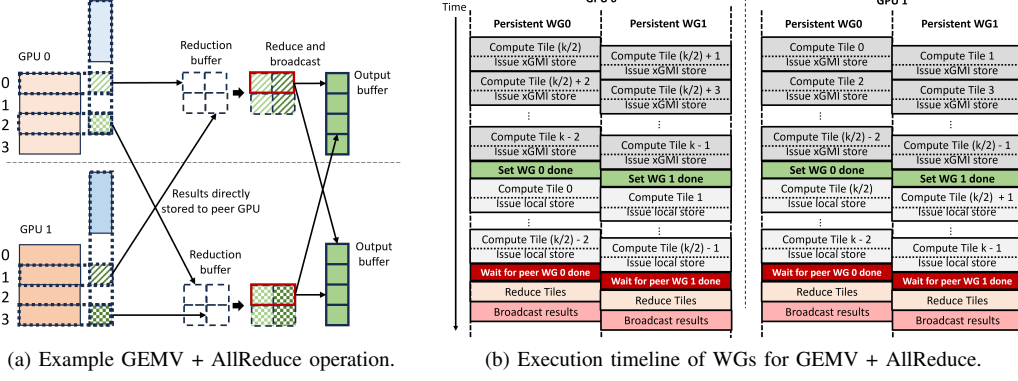
Fig. 7: GEMV + AllReduce Operator.

GPU memory. The remainder of this section describes the fused *GEMV + AllReduce* operator and contrasts this scale-up approach to our scale-out approach described in the previous subsection.

Figure 7 illustrates our proposed fused *GEMV + AllReduce* operator. It assumes two GPUs connected via Infinity Fabric™ within a single node and each GPU uses a temporary buffer to perform the reduction. We implement our fused operator as a persistent kernel where each physical WG iteratively executes multiple logical WGs responsible for computing individual output tiles. Every physical WG is responsible for computing the same output tiles across GPUs to simplify dependency during reduction. In our approach, we use a two-phase direct algorithm for AllReduce as it has the least number of steps and achieves lower latency for fully connected GPUs [32]. Every GPU is responsible for reducing $\frac{1}{\#GPUs}$ number of tiles (reduce scatter phase) and broadcast the result to other GPUs (all gather phase) as shown in Figure 7a. In this example, each GPU will compute the entire GEMV output vector but one half of the tiles will be reduced locally while the other will be communicated to peer GPU for the reduction. For example, GPU 0 will reduce the first two tiles, while GPU 1 will reduce the last two.

We perform communication-aware scheduling of logical WGs similar to scale-out approach, where logical WGs computing tiles which need to be communicated are executed ahead of the logical WGs generating locally consumed tiles. In the example timeline shown in Figure 7b, we can see that WGs in GPU 0 compute and communicate tiles $\frac{k}{2} : k - 1$ (k=total output tiles) ahead of tiles $0 : \frac{k}{2} - 1$ which are locally reduced. The scale-up communication is performed using GPU stores over Infinity Fabric™, so unlike our scale-out approach where a single thread initiated the network communication, all the threads within the WG computing the outputs directly store the results into the destination buffer, eliminating any local copy and intermediate buffering. In order to reduce the amount of synchronization between GPUs, every physical WG only sets one ready flag per peer GPU indicating that the communication of all the tiles (from the specific physical WG) to the peer GPU has finished as shown in Figure 7b. Once the WGs have computed their local tiles, they wait for the flag to be set by the counterpart physical WGs from peer GPUs. On verifying that the flag is set, they reduce the tiles and broadcast the output to other peer GPUs.

Our fused *GEMM + All-to-All* operator also has a similar implementation as explained above except it is implemented in Triton with communication extensions. GPUs perform GEMM operations and the output tiles are communicated to peer GPUs. In this case, no reduction is performed as GEMM operation is fused with All-to-All collective.

C. Overheads

Having GPU threads initiate communication within kernels consumes GPU resources which can impact performance. This subsection describes those overheads.

API Latency: An obvious overhead of having GPU threads initiate networking transactions is the latency of issuing the APIs. The impact of this overhead is limited as the communication is only triggered once per slice. However, there are other book-keeping operations (e.g., setting *WG_Done* flags) which need to be performed which adds additional overhead.

Occupancy: Invoking ROC_SHMEM API calls consume GPU registers which otherwise would have been used by the application. Reduced register availability can result in lower occupancy or increased register spilling, impacting performance. Our fused *embedding + All-to-All* kernel achieves 12.5% lower occupancy compared to the original embedding pooling kernel. Despite lower occupancy, our approach achieves better performance as shown in Section IV.

Inter-WG Synchronization: In our approach, communication is triggered once for every slice of data. Since multiple WGs could be computing an individual slice, inter-WG synchronization is required. Our implementation does not use inter-WG barrier instructions, but rather uses cross-lane operations [3] to reduce the *WG_Done* bitmask and ensure only the last completing WG per slice issues the remote communication.

D. Integration with ML Frameworks

While our approach uses the multi-threaded nature of GPU execution to perform fine-grain overlap of collective communication with computation that would not be possible at the

TABLE I: System Setup.

GPU	AMD Instinct™ MI210
Software	PyTorch v2.0, ROCm v5.4, ROC_SHMEM v1.6
Scale-up	4 GPUs (fully connected over Infinity Fabric™ (80GB/s)
Scale-out	2 nodes (with x1 GPU), connected over IB (20 GB/s)

TABLE II: Scale-out simulation setup.

DLRM Model Parameters [47]	
Embedding dimension	92
MLP layer	Avg. size: 682, # layers: 43
Avg. pooling size	70
ASTRA-Sim Network Parameters [53]	
Topology	2D Torus (BW: 200Gb/s, lat: 700ns)

kernel granularity, it has to be integrated within existing ML frameworks to be considered a pragmatic solution for wider adoption. In this work, we have implemented two integration approaches and this section describes how these approaches minimize programmers/developers effort.

PyTorch Integration: Our fused *embedding + All-to-All* and *GEMV + AllReduce* operators are implemented in HIP [10] and have been integrated within PyTorch. Specifically, we have created new APIs in PyTorch for 1) allocating device memory in symmetric heap and moving a tensor from the CPU's host memory to the allocated device memory (similar to existing $torch.tensor.to()$ API) and 2) launching fused kernel operations (e.g., $torch.embeddingAll2AllOp()$). Such interface reduces programmer overhead as the underlying implementation is hidden from the user. Furthermore, their use can be automated using existing graph transformation optimizations within ML frameworks [28], [30].

Extending Triton Framework: Effortless development of fused operators is vital for our approach to be widely adopted. We make a crucial step in this direction by extending the Triton [56] framework to include communication primitives. We chose Triton because it offers a Python-like language which is widely used by ML developers [29]. In addition, Triton is already integrated with PyTorch [1] allowing code written in Triton to be executed from PyTorch. Triton's Python-like interface enables low-overhead development of new operators. We extended it by creating a Python wrapper for the ROC_SHMEM library and its scale-up communication APIs and used it to develop our *GEMM + All-to-All* fused operator (our extensions currently support scale-up communication). It is possible to automate the generation of fused kernels using compilers that can track workgroup dependencies across GPU kernels [42] and expose communication operations at an intermediate representation level [12]. However, implementing such a compiler flow is beyond the scope of this work.

IV. EVALUATION

We evaluated the scale-up fused operators on four GPUs connected via Infinity Fabric™ , while our scale-out operators are evaluated using both real hardware (two GPU nodes connected via Infiniband) and simulation (128 GPU nodes).

A. Setup

We compared our fused operators against bulk-synchronous execution of computation and communication kernels (blit kernel-based collectives for intra-node or GPU-Direct RDMA-based collectives for inter-node, both from RCCL [23]). Table I shows the system setup used for our evaluations.

Embedding + All-to-All: We evaluated embedding operations (embedding dim=256 [47]) implemented in the public DLRM [7] code with All-to-All. In our fused kernel, a cluster of 32 logical WGs compute an output slice to achieve a much higher degree of fine-grain communicaiton-computation overlap than what would be possible by splitting the kernel. For example, batch size=2048, tables/GPU=256 configuration resulting in 512k total logical WGs, will require 16384 additional kernel launches, resulting in such a significant overhead [44], [47], [60] that we did not evaluate it.

We varied the global batch-size and the number of embedding tables processed per GPU across different inter-node and intra-node configurations. Each configuration is labeled as: {global batch size | embedding tables per GPU} in the graphs. For inputs, we used the data generator in DLRM. For large scale-out simulation, we evaluated the entire DLRM [7] application in ASTRA-Sim [52]. We modified ASTRA-Sim's execution graph to model our fused *embedding + All-to-All* kernel. The DLRM model and simulator parameters are shown in Table II. The per-kernel execution times used in ASTRA-Sim were collected on an AMD Instinct™ MI210 GPU using ROC-profiler [22].

GEMV + AllReduce: This operator is specific to inference, so we evaluate them in a scale-up configuration. The computation involved is relatively smaller (inference workload) and thus splitting them into smaller kernels to achieve computation-communication overlap will under-utilize GPUs and exacerbate kernel launch overheads. Thus, we compare our approach against a bulk-synchronous RCCL-based baseline. We select the input matrix and vector dimensions to reflect the sizes in current and future transformer models [50].

GEMM + All-to-All: The evaluated fused operator is implemented in Triton. We use the publicly available Triton GEMM implementation [13], [24] and modify it to perform All-to-All using our communication extensions. The input matrix sizes are based on commonly seen dimensions in MoE layers [39].

B. Scale-up evaluation

We evaluated the benefits of the zero-copy, fused kernel on a single node with four GPUs. All communicaiton is performed at the GPU thread granularity (not slice) using stores across the Infinity Fabric™ links.

Embedding + All-to-All: Figure 8 shows the execution time of our approach normalized against the time taken by the bulk-synchronous baseline. Overall, our approach achieves on average 20% (and up to 32%) lower execution time. The benefits achieved are lower for smaller batch sizes (e.g., 512) due to the small All-to-All latency. While for larger batches, we observe higher benefits than what could be achieved by
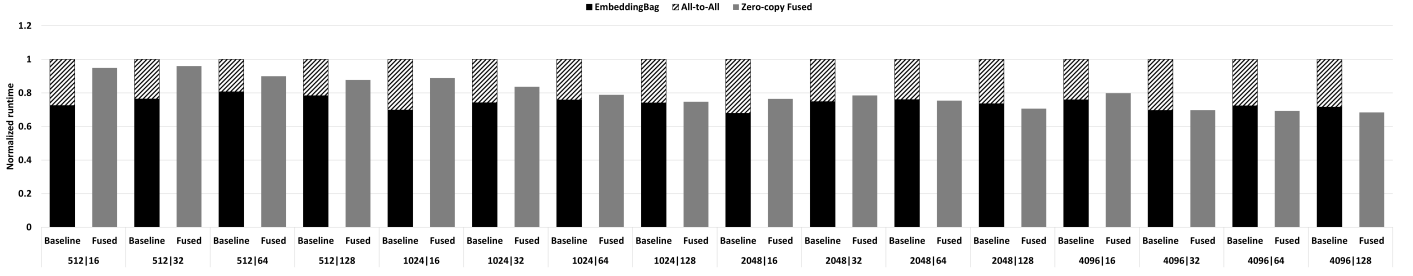
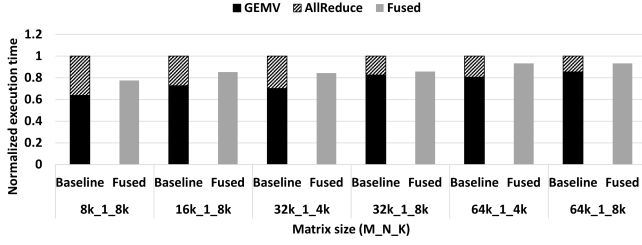Fig. 8: Normalized execution time (intra-node).

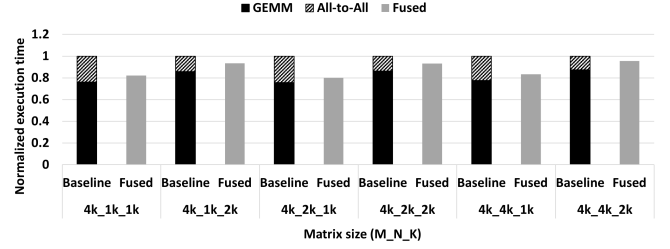Fig. 9: Normalized execution time: GEMV + AllReduce.

Fig. 10: Normalized execution time: GEMM + All-to-All.

fully overlapping All-to-All due to the zero-copy optimizations which eliminate stores to intermediate local buffer.

GEMV + AllReduce: Figure 9 shows the execution time of our *GEMV + AllReduce* fused operator normalized against time taken for bulk-synchronous execution of GEMV and intra-node AllReduce for different matrix sizes. Our approach achieves on average 13% (and up to 22%) lower execution time. The latency reduction is lower for the larger inputs (M = 64k) because as the output vector size grows, the contention for the Infinity Fabric™ links increases, lowering the benefits.

GEMM + All-to-All: Figure 10 shows the execution time of our *GEMM + All-to-All* fused operator normalized against time taken for the bulk-synchronous execution of the GEMM and intra-node All-to-All kernels. Our approach lowers execution time by 12% on average and up to 20%. Since we are using a generic GEMM implementation provided with Triton, the GEMM dominates the overall execution time and limits the benefits of our approach.

C. Inter-node evaluation

WG Profiling: We first demonstrate the effectiveness of overlapping embedding operations with All-to-All communication. We profile the persistent WGs' execution timeline for a configuration with batch size = 2048, tables/GPU = 256, and with slice size such that each slice is computed by 16 WGs. WGs computing the same slice (cluster of 16) are sorted based on their time to complete embedding pooling operations (earliest first). Figure 11 illustrates the execution timelines for the first 32 persistent WGs along with the points in time when non-blocking network transactions were issued. Figure 11 also shows the instances when the locally consumed slices are computed (marked as *Local slice completion*) to illustrate the effect of communication-aware scheduling. We can see that some persistent WGs are issuing remote communication while

others are performing the computation, demonstrating our approach achieves fine-grained communication-computation overlap. Furthermore, asynchronous network transactions allow the communicating WGs (e.g., WG 15 and 31) to continue performing embedding pooling without being blocked. Figure 11 shows that the last WGs (WG 15 and WG 31) within each cluster of 16 WGs issues most of the communication. This is because each persistent WG iteratively computes individual slices. The last completing WG for one slice often stays the last across multiple slices (recall that only the last completing WG issues the remote non-blocking PUT). Additionally, we can see that the remote communication calls are issued before computing the local slices, maximizing the opportunity to hide remote communication. The time spent waiting on data differs across WGs because each WG waits for a distinct subset of the *sliceRdy* flags.

Execution time: Figure 12 shows the time taken by our fused embedding + All-to-All kernel normalized to the baseline executing separate embedding operation and All-to-All collective kernels. Our fused kernel uses a slice size of 32
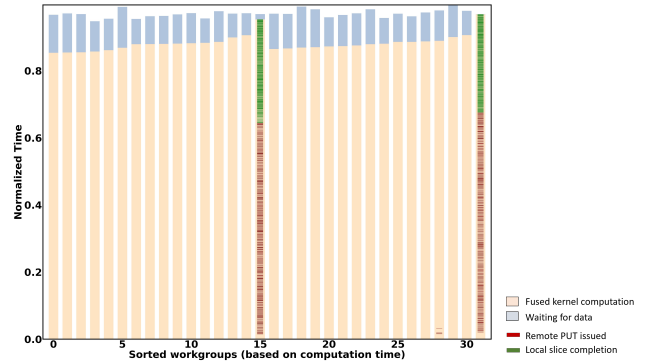

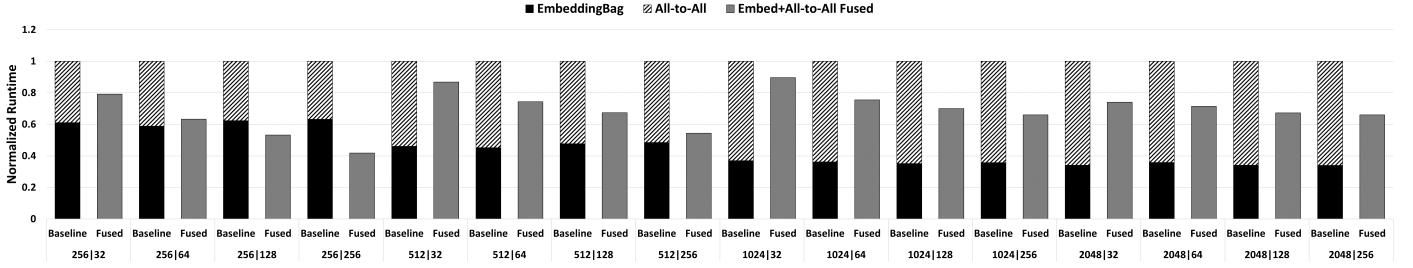Fig. 11: Profiled timeline of persistent WG.

Fig. 12: Normalized execution time (inter-node).

embeddings and Figure 12 demonstrates that our approach benefits a wide set of batch sizes and embedding table counts, achieving 31% average reduction in execution time (up to 58%). For smaller global batch sizes (e.g., 256), we note that the performance benefit is more than what could be achieved by fully overlapping communication. This is because smaller batch sizes result in poor compute utilization for the baseline, while our approach achieves much higher compute utilization by processing all tables within a single fused kernel.

Occupancy effect: Our fused kernel implementation results in 12.5% lower GPU occupancy than the baseline due to the extra registers required by GPU-initiated networking operations. However, this loss of occupancy does not degrade performance. Figure 13 shows the variation in the execution time (global batch size: 1024, tables/GPU: 256) across different GPU occupancy. The figure only shows results up to 87.5% occupancy because that was the maximum achievable occupancy relative to baseline. We see that as the occupancy is increased from 25% to 75%, the parallelism increases and consequently the execution time reduces by 46%. However, increasing the occupancy further from 75% to 87.5% results in the execution time increasing by 25%. At this higher occupancy level, the memory intensive embedding operations encounter significant memory contention, exemplifying the trade-off between parallelism and memory contention.

Communication-aware Scheduling: In our approach, we implement communication-aware WG scheduling to maximize the opportunity to hide remote communication. Figure 14 shows the fused *embedding + All-to-All* kernel execution time of both nodes (normalized to baseline:node 0) with and without communication-aware scheduling. The baseline communication-oblivious scheduling starts from WG (0,0,0) and then proceeds sequentially. In baseline scheduling, node 0 and 1 have an average execution time skew of ∼7% while using communication-aware scheduling exhibits only a ∼1%
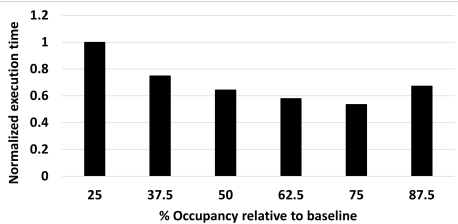
average execution time skew. Many distributed ML models, including DLRM, periodically synchronize across nodes (e.g., during synchronous gradient descent), and thus execution skew can reduce the overall performance. The higher skew in the baseline is due to the higher execution time for node 1. As part of our fused kernel implementation, WGs in node 1 will wait for slices from node 0 and vice-versa. Node 1 has the same logical WG schedule under both strategies, where it first computes the slices to be communicated to node 0 (please see Figure 6b). However, with communication-oblivious scheduling, node 0 computes the slices to be remotely communicated after the locally consumed slices. Thus the remote communication is not hidden behind local slice computation, delaying the completion of node 1.

D. Large scale-out evaluation

We evaluated the benefits of our approach on DLRM training distributed across 128 nodes (with one GPU each) using ASTRA-Sim. Figure 15 shows the normalized execution time for performing one DLRM training pass. The embedding operations in both the forward and backward passes are over-lapped with their dependent All-to-All collective operations using WG-level parallelism. We can see that our approach is able to hide most of embedding operations , achieving on average a ∼21% reduction in the overall execution time.

V. RELATED WORK

In this section, we discuss prior research done on optimizing distributed ML models, overlapping computation with CPU-initiated inter-node and DMA-assisted intra-node communication. We also discuss previous work on GPU-initiated communication.

T3 [50] proposes hardware track and trigger mechanisms to detect GPU stores and initiate intra-node DMA communi-

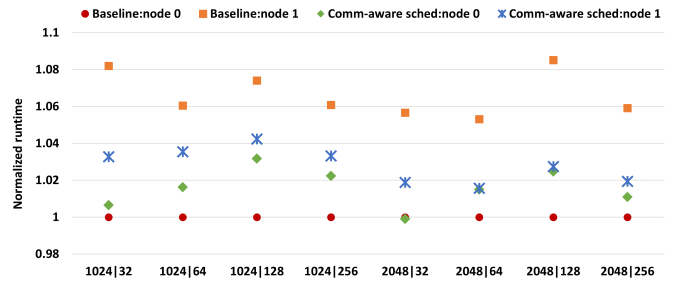Fig. 13: Impact of WG occupancy on execution time.

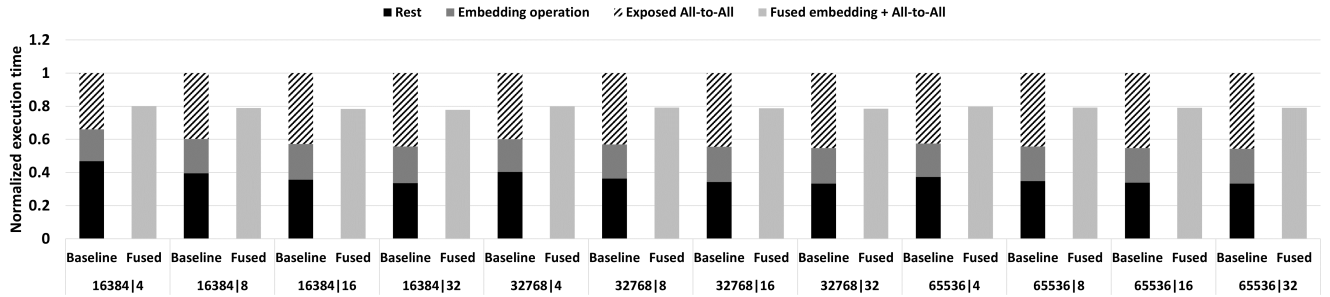Fig. 14: Impact of communication-aware WG scheduling.

Fig. 15: Scale-out simulation normalized execution time.

cation to overlap it with computation. While this work aims to achieve communication-computation overlap, it requires hardware modifications to track GPU stores using a new widget invisible to programmers that can be difficult to debug. In contrast, our approach requires no hardware changes and has been implemented in commercially available frameworks.

Wang et. al [58] propose decomposing the original collective communication and its dependent computation into smaller pieces. The communication of an individual data shard can be overlapped with the computation of another. Our approach is conceptually similar to this as both aim at overlapping communication of a portion of data with the computation of another. However, unlike us, Wang et al.'s approach will result in a higher number of kernel invocations where each sharded kernel is smaller than the original one. For their use case [58], the sharded kernels are sufficiently large to amortize the kernel invocation overhead but this is not always the case [47]. Further, their approach requires additional operations to combine the individual partial results. Jangda et. al [41] also proposes similar optimizations but they use a new domain-specific language to express ML programs in the form of computation and communication operations. Our approach instead uses GPU-initiated networking integrated within existing ML frameworks, to hide communication without requiring additional kernel launches, and computations.

Mudigere et al. [47] proposed Neo system to improve distributed DLRM execution. This system employs 4D parallelism strategy (table-wise, row-wise, column-wise, and data parallelism) for distributing embedding computations evenly across GPUs. Furthermore, they fuse compute kernels to minimize kernel-launch overheads and memory requirements, and employ software-managed caching to leverage hardware memory hierarchy. However, in this paper, we try to address the large All-to-All communication latency exposed in distributed DLRM training by fusing and overlapping All-to-All with embedding operations.

Wang et. al. [59] propose using GPU-initiated networking to hide remote access latency in GNNs. While this work uses GPU-initiated communication, it focuses on optimizing irregular communication by interleaving local neighbor aggregation with remote neighbour access. Their work targets a different problem than that addressed in this paper and requires a completely different implementation.

Unlike our approach which aims at hiding the collective communication latency, there have been efforts to reduce them. Cai et. al. [31] have proposed an approach to synthesize collective algorithms tailored for a specific hardware topology. ARK [40] proposes offloading intra-node communication to DMA driven by GPU to reduce control-plane overhead and data-plane interference. Others [38], [53] have proposed optimal communication schedule for specific collectives aimed at reducing contention and improving link utilization. These optimizations are orthogonal to our approach.

VI. CONCLUSION

In this paper, we hide the collective communication with dependent computation at a fine granularity. GPU-initiated intra-kernel communication enables wavefront/warp-, WG- or WG-cluster granular communication unlike CPU-initiated networking which provides only kernel-granular communication. We developed prototype fused *embedding + All-to-All*, *GEMV + AllReduce* and *GEMM + All-to-All* kernels where fragments of computed outputs are communicated in parallel to other WGs performing the remainder of the computation. We propose remote communication-aware scheduling where the logical WGs computing the remote slices are executed before the WGs computing the local slices, maximizing the opportunity to overlap remote communication. We further optimize scale-up communication among GPUs by developing zero-copy fused kernels. Here, GPU threads perform the computation and store the results directly to the destination address at the peer GPU, thereby eliminating intermediate stores to local memory. We expose our fused operators as new PyTorch operators as well as develop fused operators (*GEMM + All-to-All*) using our Triton framework extensions which include communication primitives to demonstrate integration with ML frameworks.

We evaluated our approach both on actual hardware and using simulation. Our scale-up evaluations show that zero-copy fused *embedding + All-to-All* kernel on average achieves 20% (and up to 32%) lower execution time than the baseline. Our *GEMM + All-to-All* and *GEMV + AllReduce* evaluations show that our approach achieves 13% (up to 22%) and 12% (up to 20%) lower execution time respectively. Our inter-node evaluations show that the execution time taken by fused kernel *embedding + All-to-All* is on average 31% (and up to 58%) lower than that of baseline embedding operations and All-to-All collective. We evaluated the impact of proposed communication-aware WG scheduling and show that

it achieves 6% lower execution skew than communication-oblivious scheduling. Finally, we used ASTRA-Sim to perform large scale-out simulations to evaluate the benefits of our approach on the entire DLRM training run. Our evaluations show that using fused embedding + All-to-All kernels reduce the training time by 21% for a 128 node system.

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