sinudoidal waveform through a 10-bit R-2R ladder digital-to-analog converte

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1. Introduction

- Objective: Generate a sinusoidal waveform using an R-2R DAC.
- Use a lookup table with 128 9-bit samples and exploit symmetry for efficiency.
- Implement using SystemVerilog and verify with simulations and oscilloscope measurements.

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2. Design Overview

```
logic [8:0] address = 0;
logic [9:0] data;
logic [6:0] quarter_address; // 2^7
logic [1:0] quarter; //2^2 for 4 parts
logic [9:0] quarter_data;


assign quarter = address[8:7];

always_comb begin
    case(quarter)
        2'b00, 2'b01: data = quarter_data;
        2'b10, 2'b11: data = ~quarter_data + 1; // Invert
    endcase
end

always_comb begin
    case(quarter)
        2'b00: quarter_address = address[6:0]; //q1
        2'b01: quarter_address = 7'd127 - address[6:0]; //flip q1
        2'b10: quarter_address = address[6:0]; //invert q1
        2'b11: quarter_address = 7'd127 - address[6:0]; //flip inverted q1
    endcase
end
```

Assign 2-bit for the 4 quarters and 7-bits for the quarter_address to fulfill 28 9-bit samples of thefirst quarter cycle of a sine wave

- For first quarter: 0~90 of sine wave, memory look up of 28 9-bit samples of the first quarter cycle of a sine wave
- For second quarter: 90~180 of sine wave, reverse the look up to flip the 1st quarter
- For third quarter: 180~270 of sine wave, invert the first quarter
- For fourth quarter: 270~360/0 of sine wave, flip the inverted first quarter

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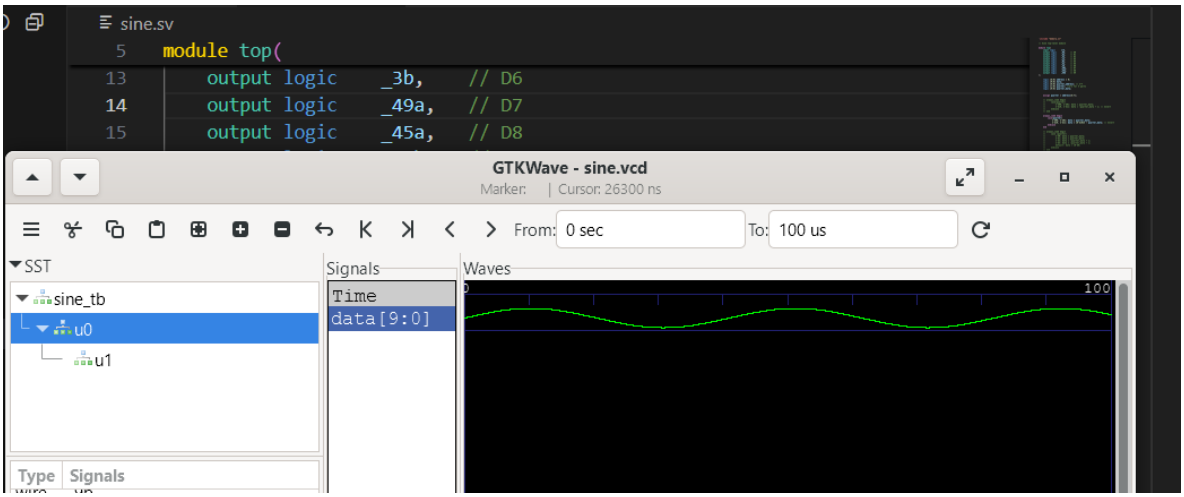
3. Simulation and Results



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4. Hardware Measurement