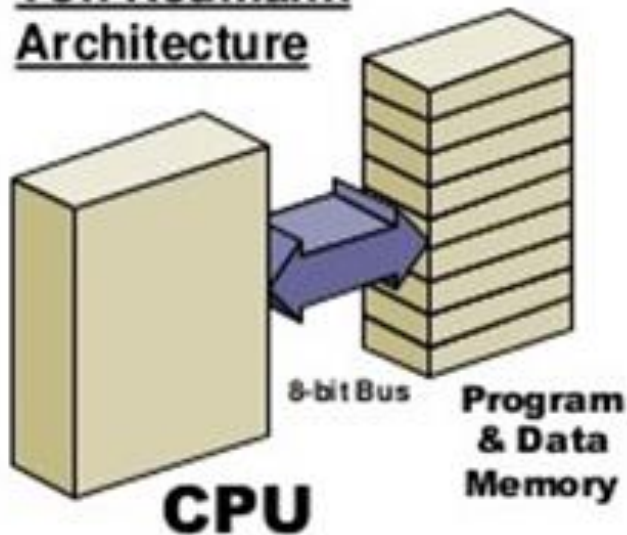


Machine Architecture - Lecture 3

Von Neumann Architecture



Ioannis Ivrissimtzis

ioannis.ivrissimtzis@durham.ac.uk

The von Neumann architecture

von Neumann architecture

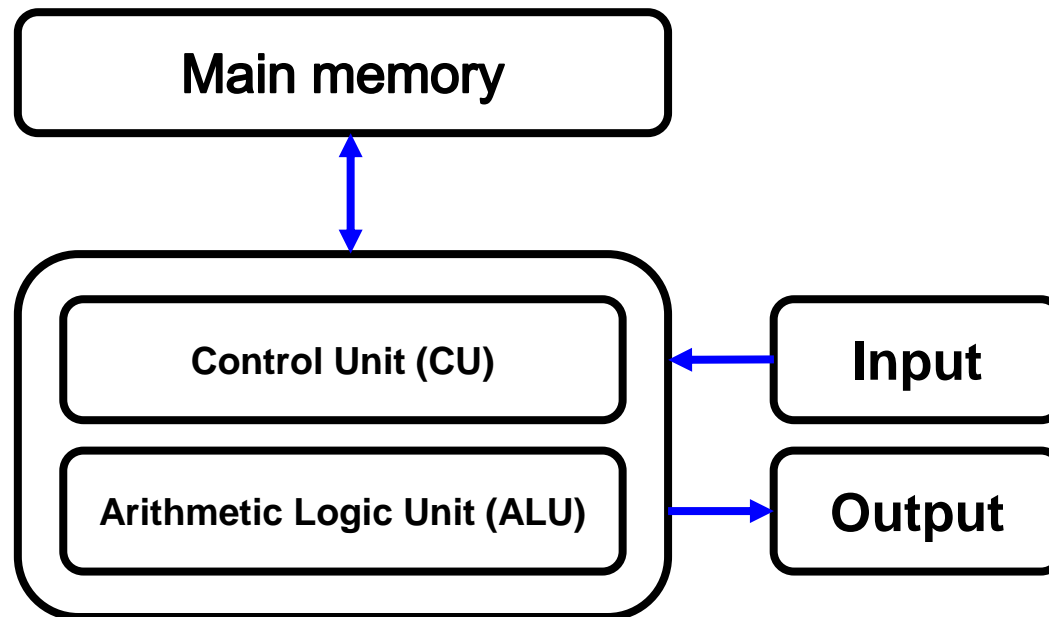
An architecture of computing devices developed by the EDVAC design team for the U.S. Army 1945-51.

Commonly attributed to [John von Neumann](#) due to the 1945 publication: [First Draft of a Report on the EDVAC](#) which you can download it from DUO (of historical only interest).

The main elements of computers are still virtually unchanged.

[illegible]

von Neumann architecture



By zooming in on each of these components we can produce more and more detailed, but less and less general, architectures.

von Neumann architecture

Central Processing Unit (CPU):

Control Unit (CU): responsible for directing the flow of instructions and data.

Arithmetic Logic Unit (ALU) : responsible for performing operations on the data.

Main memory.

Input / Output devices.

Communication between components through buses.

Harvard architecture

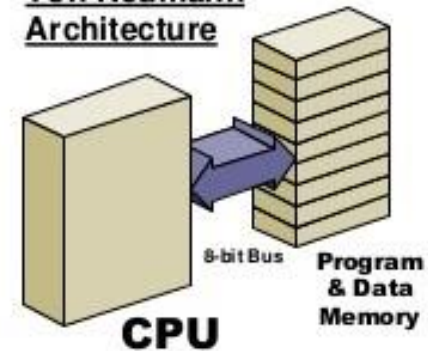
Are there any architecture that are not of the von-Neumann type?

Yes, the Harvard architecture.

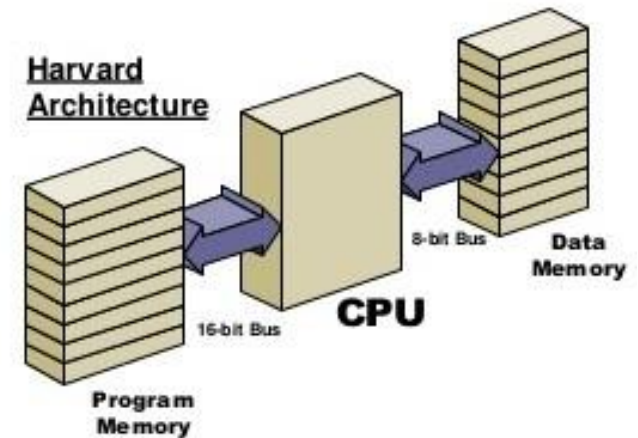
Two separate memory spaces for program instructions and data.

Two separate buses.

Von Neumann Architecture



Harvard Architecture



Harvard architecture

Imagine I use mailboxes 00-79 of the LMC for storing op codes only, and mailboxes 80-99 for storing data only.

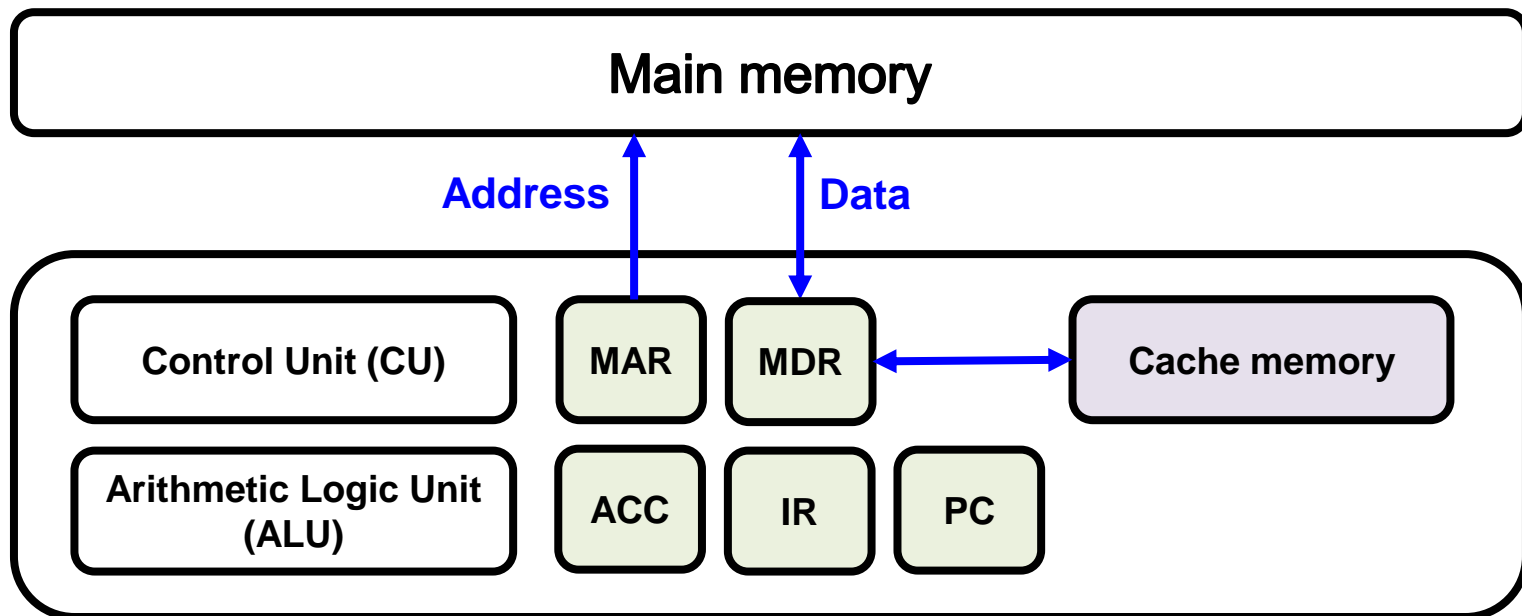
Does it make the architecture Harvard?

No, as long as we have one only Minion.

A single bus for both instructions and data is considered the litmus test of von Neumann architecture.

Mailboxes									
00	01	02	03	04	05	06	07	08	09
000	000	000	000	000	000	000	000	000	000
10	11	12	13	14	15	16	17	18	19
000	000	000	000	000	000	000	000	000	000
20	21	22	23	24	25	26	27	28	29
000	000	000	000	000	000	000	000	000	000
30	31	32	33	34	35	36	37	38	39
000	000	000	000	000	000	000	000	000	000
40	41	42	43	44	45	46	47	48	49
000	000	000	000	000	000	000	000	000	000
50	51	52	53	54	55	56	57	58	59
000	000	000	000	000	000	000	000	000	000
60	61	62	63	64	65	66	67	68	69
000	000	000	000	000	000	000	000	000	000
70	71	72	73	74	75	76	77	78	79
000	000	000	000	000	000	000	000	000	000
80	81	82	83	84	85	86	87	88	89
000	000	000	000	000	000	000	000	000	000
90	91	92	93	94	95	96	97	98	99
000	000	000	000	000	000	000	000	000	000

von Neumann architecture



By zooming in on each component (including the bus) we can produce more and more detailed, but less and less general, architectures.

Components of the CPU

Registers: special memory locations that can be accessed very fast.

Five registers were shown:

- Accumulator (ACC)

- Program Counter (PC)

- Instruction Register (IR)

- Memory Address Register (MAR)

- Memory Data Register (MDR)

Buses: bundles of tiny wires that carry data between components.

Registers

The 'work space' of the CPU. Hold a value temporarily for:

storage

manipulation

calculation

Manipulated directly by the Control Unit (CU).

Their size of registers can vary from 1 to 128 bits.

Handwritten notes:

- CPU read data
- register : 1 cycle
- RAM : 120 cycle
- SSD : 10000 cycle
- HDD : 300000 cycle
- USB : 12000000 cycle
- Cloud : 3400000000 cycle
- Cache: 4
L1: 20
L3: 60

Registers

Accumulators are often seen as part of the ALU.

General purpose registers used for:

- Holding data.

- Holding interim and final results of arithmetic operations.

- Holding data waiting to be transferred between different memory locations.

- Holding data waiting to be transferred between I/O and main memory.

Registers

The Program Counter (PC), Instruction Register (IR) and the Flags are often seen as part of the Control Unit.

The **Program Counter** holds the address of the next instruction to be executed.

The **Instruction Register** holds the actual instruction being executed.

Flags are 1 bit registers used to keep track of special conditions, such as: arithmetic carry, overflow, power failure, internal computer error

Flags are grouped together in one or more **Status Registers** (SR).

Registers

The Memory Address Register (MAR) and the Memory Data Register (MDR) are used for memory management.

The **Memory Address Register** holds the address of a memory location to be accessed.

Connects to the memory with a one-way bus.

The **Memory Data Register** holds the value that is being stored to or retrieved from the memory location currently addressed by the MAR.

Connects to the memory with a two-way bus. Also known as the **Memory Buffer Register** (MBR).

Buses

The physical connection that makes it possible to transfer data from one location in the system to another is called a **bus**.

A bus is a group of electrical conductors (lines) used to carry signals.

Four general categories of lines: Data, Address, Control, and Power.

Buses are used to:

- Transfer data between different points on the CPU.

- Transfer data between the CPU and main memory.

- Transfer data between computer peripherals and the CPU.

Bus types

Point-to-point buses carries the signal from a specific source to a specific destination.

Broadcast buses carry signals to many different destinations.

Bus Interface Bridges allow communications between the different buses:

- External bus

- PCI: Peripheral Control Interface bus

- USB: Universal Serial Bus