CPU with Five-Stage MIPS Pipeline

Zhijian LIU

September 8, 2016

Course:	Computer System
Instructor:	Professor Alei Liang
Teaching Assistant:	Shusheng He

Contents

1 Introduction

This report is a detailed summary on the final project of the "Computer System" course. In this project, I implemented a toy CPU with five-stage MIPS pipeline.
The project has the following features:

- It supports almost all of the MIPS standard integer instructions (except those related to the coprocessors).
- It supports the full bypassing in order to mitigate the data hazards.
- It supports the automatic testing.

The project is written in Verilog HDL and is available under the open-source MIT License at https://github.com/zhijian-liu/mips-cpu.

2 Main Modules

2.1 Stage Modules

In the five-stage MIPS pipeline, there are obviously five separate pipeline stages:

- stage IF (instruction fetch)
- stage ID (instruction decode)
- stage EX (execution)
- stage MEM (memory access)
- stage WB (write back)

In my design philosophy, each of them should be implemented as a single module.

2.1.1 Instruction Fetch

The main function of this module is to maintain the program counter and send it to the instruction ROM in order to fetch the current instruction.

Interface	Type	Usage
clock	in	clock signal
reset	in	reset signal
stall	in	stall signal
register_pc_read_data	out	register PC
register_pc_write_enable	in	
register_pc_write_data	in	

Table 1: the interfaces of the stage IF

This module is implemented in `src/cpu/stage/stage_if.v`.

2.1.2 Instruction Decode

The main function of this module is to decode the instruction and extract the operator, category, operands and destination from it.

Interface	Type	Usage
reset	in	reset signal
instruction_i	in	instruction
instruction_o	out	
operator	out	operator
category	out	category of the operator
operand_a	out	operands
operand_b	out	
register_read_enable_a	out	read port A of the register file
register_read_address_a	out	
register_read_data_a	in	
register_read_enable_b	out	read port B of the register file
register_read_address_b	out	
register_read_data_b	in	
register_write_enable	out	write port of the register file
register_write_address	out	
register_write_data	out	
register_pc_read_data	in	register PC
register_pc_write_enable	out	
register_pc_write_data	out	
ex_operator	in	data forwarding from the stage EX
ex_register_write_enable	in	
ex_register_write_address	in	
ex_register_write_data	in	
mem_register_write_enable	in	data forwarding from the stage MEM
mem_register_write_address	in	
mem_register_write_data	in	
stall_request	out	whether or not is to request stall

Table 2: the interfaces of the stage ID

In order to mitigate the data hazards[1], some interfaces are designed to fetch the latest data forwarding[2] from the stage EX and the stage MEM.
After implementing the full bypassing, there is only one kind of data hazard: a load instruction immediately followed by an instruction which has data dependency on it. In this case, we have to enable the "`stall_request`" signal in order to stall the pipeline for one cycle.
This module is implemented in `src/cpu/stage/stage_id.v`.

[1] https://en.wikipedia.org/wiki/Hazard_(computer_architecture)#Data_hazards
[2] https://en.wikipedia.org/wiki/Operand_forwarding

2.1.3 Execution

The main function of this module is to calculate the operation result according to the operator and operands received from the stage ID.

Interface	Type	Usage
reset	in	reset signal
instruction_i	in	instruction
instruction_o	out	
operator_i	in	operator
operator_o	out	
category	in	sub-category of the operator
operand_a_i	in	operands
operand_a_o	out	
operand_b_i	in	
operand_b_o	out	
register_write_enable_i	in	write port of the register file
register_write_enable_o	out	
register_write_address_i	in	
register_write_address_o	out	
register_write_data_i	in	
register_write_data_o	out	
register_hi_write_enable	out	register HI
register_hi_write_data	out	
register_lo_write_enable	out	register LO
register_lo_write_data	out	
mem_register_hi_write_enable	in	data forwarding from the stage MEM
mem_register_hi_write_data	in	
mem_register_lo_write_enable	in	
mem_register_lo_write_data	in	
wb_register_hi_read_data	in	data forwarding from the stage WB
wb_register_hi_write_enable	in	
wb_register_hi_write_data	in	
wb_register_lo_read_data	in	
wb_register_lo_write_enable	in	
wb_register_lo_write_data	in	
stall_request	out	whether or not is to request stall

Table 3: the interfaces of the stage EX

In order to mitigate the data hazards, some interfaces are designed to fetch the latest data forwarding from the stage MEM and the stage WB.
Note that the "`stall_request`" signal is actually redundant because in the functional simulation[3], all kinds of calculation can be finished in a single cycle.
This module is implemented in `src/cpu/stage/stage_ex.v`.

[3] https://en.wikipedia.org/wiki/Logic_simulation

2.1.4 Memory Access

The main function of this module is to handle the memory access instruction: calculate the effective memory address[4] and send it to the data RAM in order to execute the load or store operation.

Interface	Type	Usage
reset	in	reset signal
instruction	in	instruction
operator	in	operator
operand_a	in	operands
operand_b	in	
memory_read_enable	out	read port of the data RAM
memory_read_address	out	
memory_read_data	in	
memory_write_enable	out	write port of the data RAM
memory_write_address	out	
memory_write_select	out	
memory_write_data	out	
register_write_enable_i	in	write port of the register file
register_write_enable_o	out	
register_write_address_i	in	
register_write_address_o	out	
register_write_data_i	in	
register_write_data_o	out	
register_hi_write_enable_i	in	register HI
register_hi_write_enable_o	out	
register_hi_write_data_i	in	
register_hi_write_data_o	out	
register_lo_write_enable_i	in	register LO
register_lo_write_enable_o	out	
register_lo_write_data_i	in	
register_lo_write_data_o	out	

Table 4: the interfaces of the stage MEM

This module is implemented in `src/cpu/stage/stage_mem.v`.

[4] https://www.cs.umd.edu/class/sum2003/cmsc311/Notes/Mips/addr.html

2.1.5 Write Back

The main function of this module is to maintain the register HI and register LO.

Interface	Type	Usage
clock	in	clock signal
reset	in	reset signal
register_hi_read_data	out	register HI
register_hi_write_enable	in	
register_hi_write_data	in	
register_lo_read_data	out	register LO
register_lo_write_enable	in	
register_lo_write_data	in	

Table 5: the interfaces of the stage WB

This module is implemented in `src/cpu/stage/stage_wb.v`.

2.2 Latch Modules

In the five-stage MIPS pipeline, there are totally four pipeline latches which act as the buffers between the neighbouring pipeline stages.
These modules are implemented in:

- `src/cpu/latch/latch_if_id.v`
- `src/cpu/latch/latch_id_ex.v`
- `src/cpu/latch/latch_ex_mem.v`
- `src/cpu/latch/latch_mem_wb.v`

Note that all of the pipeline latches propagate the data on the rising edge of the clock signal.

2.3 Storage Modules

In my implementation, all of the storage modules write the data on the falling edge of the clock signal. Otherwise, some additional codes will be needed to support the bypassing inside the storage modules.

2.3.1 Instruction ROM

Because the instructions cannot be modified at runtime, the instruction ROM has only one major function: memory read. It uses a set of input wires to read the program counter and outputs the corresponding instruction.
This module is implemented in `src/rom.v`.

2.3.2 Data RAM

Unlike the instruction ROM, the data RAM has two major functions: memory read and memory write. It uses a set of input wires to read the address and outputs the corresponding data. At the meantime, it also provides a set of wires for writing.
This module is implemented in `src/ram.v`.

2.3.3 Register File

The register file provides two sets of input wires for querying the value of a given register, and a set of wires for writing a register.
This module is implemented in `src/cpu/register.v`.

2.4 Control Module

The main function of the control module is to receive the stall request from the pipeline stages and send the stall signal to the pipeline latches.
This module is implemented in `src/cpu/control.v`.

3 Test Summary

3.1 Test Case

There are nine test cases in total:

- `test/test-logic`: check the logical instructions.
- `test/test-shift`: check the shift instructions.
- `test/test-move`: check the move instructions.
- `test/test-arithmetic`: check the arithmetic instructions.
- `test/test-jump`: check the jump instructions.
- `test/test-branch`: check the branch instructions.
- `test/test-memory`: check the memory instructions.
- `test/test-stall`: check the stall detection.
- `test/test-forwarding`: check the data forwarding.

In each test folder, there are totally three files:

- `asm.s`: the testing MIPS assembly code.
- `test.v`: the automatic testing code written in Verilog HDL.
- `Makefile`: the testing script.

A detailed guide to running the automatic test is written in `README.md`.

4 Acknowledgements

I would like to thank Professor Alei Liang for bringing me such a wonderful course, Shusheng He for his hard work and warm devotion, and Yurong You, Zihao Ye and Lequn Chen for valuable discussions.