Zhipeng Wei

714, Ryan Court, Raleigh, NC, 27606

+1 984 500 8855 • zwei5@ncsu.edu • heuristichub.blogspot.com/

Education

North Carolina State University **Raleigh, U.S.**
Master of Computer Science *09/2015 – 05/2018*

University of Chinese Academy of Sciences **Beijing, China**
Master of Science, Computer Architecture *09/2012 – 06/2015*

Huazhong University of Science and Technology **Wuhan, China**
Bachelor of Engineering, Computer Science and Technology, 87.01/100 *09/2008 – 06/2012*

Projects

Network Device Buffer Sizing *08/2016 – 03/2017*

On network devices, there are buffers. On the condition that there is a difference between the price of SRAM and DRAM, if the buffer can be fit into SRAM, the manufactuincost will be reduced. This problem tries to figure out the correct buffer size. With the emerging of IoT devices, the traffic pattern will be different.

User Level Cache Control *07/2014 – 06/2015*

In computer system, cache is an important part to improve performance. When the process is executing, it will request the kernel to allocate physical pages for the virtual pages. At this point, the mapping between virtual page and physical page is established. Depending on the mapping between physical pages and cache sets are specified, if the physical pages which the virtual pages of one process are mapped to share the same cache sets, interference becomes a performance issue. To solve this problem, page coloring assign different colors to physical pages, so that consecutive physical pages in virtual space are mapped to physical pages which are mapped into different cache sets. Based on the results of previous project, the mapping between physical address and cache sets, we enable the process to control the allocation of physical pages for specific virtual pages.

Cracking Intel Sandy Bridge Cache Hash Function *08/2014 – 02/2015*

Cache plays an important role in bridging the gap between the speed of processor and the speed of main memory. Many cache architectures have been proposed in history. Hash is an important technique to improve cache performance, such as hash-rehash cache. On Sandy Bridge processor, last level cache is divided into several slices which are connected by a ring bus. Given a data block, the location of this data block on LLC is determined by an undocumented hash function. This project tries to find out this undocumented hash function. The method is classification. We firstly make the following hypothesis: part of the physical address will be used to serve as cache set, part of the physical address will be used to hash these physical addresses sharing the same cache index to different cache slices. To verify this hypothesis, We start a process which issues memory access to the same cache set. When the number of accessed data blocks exceeds the associativity of cache set. Using the memory reference trace collecting tool HMTT, we can capture this eviction relationship. Thus, the physical address of the accessed data blocks are classified into different groups. All the data blocks in one group are mapped into one cache set. Based on this information, we get the mapping between physical address and cache set. The result is consistent with our hypothesis.

Hardware-based Kernel SamePage Merging (KSM) Optimization *03/2013 – 10/2013*

Kernel same-page merging is a kernel a feature that makes it possible for a hypervisor system to share identical memory pages among different processes or virtualized guests. Given a series of virtual machines, each of them

will use a number of virtual pages, this feature reduces the number of physical pages actually used, so that with the physical pages merged, more virtual machines or processes can run on the same machine. As the comparison process is a traverse and search which contributes a significant amount to the running time. In current implementation, only two global red black trees are constructed in KSM. The problem in this project is to figure out a mechanism to optimize the searching and traversing process. The solution is based on the memory reference characteristics extracted from traces collected using HMTT, the physical pages are classified into different categories based on these characteristics. One tree is constructed to hold the pages in each category. In case of comparison, the physical pages only needs to be compared with the pages that share the same characteristics (in the same tree). As a result, the candidate page only need to be compared with the page category that shares the same characteristics with itself. The scheme achieved 68.5% reduction of futile page comparison.

HMTT: A Hybrid Memory Trace Toolkit for the Real Systems *03/2014 – 06/2014*

Physical reference traces can be used to characterized application behavior. This tool is to get the physical reference traces. Assume one process issue some memory access, the whole path of these memory reference traces. The next question to ask is how. From the processes which issue these processes to the DRAM chips, there is a path. Then the objective becomes to capture these references some point on the path. The solution is a printed circuit board. On this board, there is an FPGA, a DIMM slot, PCIe cable. All the signals are connected to the FPGA chip. The FPGA makes it programmable and configurable. When in working status, this PCB is inserted into the DIMM slot on motherboard, the DRAM chip is inserted into the DIMM on this PCB. Inside the FPGA, based on the interface protocol, an finite state machine is maintained in the FPGA chip. And the inferred address is sent to another host to be stored through PCIe.

Publications

∘ **Zhipeng Wei**, Zehan Cui, Mingyu Chen. Cracking Intel Sandy Bridge Hash function. arXiv:1508.03767

∘ Licheng Chen, **Zhipeng Wei**, Zehan Cui, Mingyu Chen, Haiyang Pan, Yungang Bao. CMD: classification-based memory deduplication through page access characteristics. In Proceedings of VEE, 2014.

Honors and Awards

2014: Merit Student, University of Chinese Academy of Sciences;

2014: Third Place at the IET Present around the World Competition held at Institute of Computing Technology, Chinese Academy of Sciences, the Institution of Engineering and Technology;

2009: National Encouragement Scholarship, Ministry of Education of China (awarded to the top 1% students);

2009, 2010, 2011: Model Student of Academic, Huazhong University of Science and Technology;

2008: Self-Improvement Scholarship, Huazhong University of Science and Technology.

Teaching Experience

2017 Fall: CSC501 Operating System Principles with Dr. Hung-Wei Tseng

2016 Fall: CSC501 Operating System Principles with Dr. Vincent Freeh

2016 Spring: CSC501 Operating System Principles with Dr. Vincent Freeh

2015 Fall: CSC541 Advanced Data Structure with Professor Dr. Rada Chirkova