Mid-Term Chip Design for Communications Systems-Spring 2020

Due: June 15 2020

An FIR filter has the following coefficients given by:

0.098891890744637
0.002579421311410
-0.084589441437739
-0.047578154855338
0.179439401283587
0.413044584947859
0.413044584947859
0.179439401283587
-0.047578154855338
-0.084589441437739
0.002579421311410
0.098891890744637

Let the seed be 123. Generate 512 input samples with command randn with zero mean and unit variance.

Let the quantization bit-width assignment of the input signal be B=20 and B_I=6 and that of the filter coefficient be B=20 and B_I=3, In addition, let us perform quantization after each addition and multiplication with bit-width assignment B=20 and B_I=6. Answer the following questions:

1. Matlab program: Use data broadcast form to implement this filter. Show the output of this filter (confirm your answer with TAs). Show the 1st, 100th and 200th output values in your report.
2. Following (1), implement this filter via Verilog. Show the output of this filter (confirm your answer with TAs). Let the clock rate be 100MHz. Synthesize the filter. Then show the gate counts and indicate the critical path.
3. Let the parallel processing factor be 3 and use the fast algorithm in Ch9. Implement this parallel processed filter using Matlab and Verilog. Show the output of these two implementations. The results of these two implementations should be the same (confirm your answer with TAs).

- ✓ Plot “detailed architecture” of this parallel processed filter.
- ✓ Synthesize the filter. Then show the gate counts and indicate the critical path. Comparing it to the architecture without parallel processing in (2), indicate increased gate count. Discuss whether the increasing rate of gate count is reasonable or not according to the knowledge learned in the lecture.

4. Following (3), use the CSD subexpression elimination to further reduce the gate count of the polyphaser filters.
   - ✓ Implement this parallel processed filter using Matlab and Verilog. Show the output of these two implementations. The results of these two implementations should be the same (confirm your answer with TAs).
   - ✓ Show the subexpression elimination “tables” (like p. 17) and “detailed architecture” (like p. 22) of this filter.
   - ✓ Synthesize the filter. Then show the gate counts and indicate the critical path. Indicate how many gate count can be further reduced by subexpression elimination
5. Now let the parallel processing factor be 4. Repeat (3).

Report Guidance:

Your report should contains “at least (and can be more to obtain plus)”

1. The architectures of your filters.
2. The synthesis report, critical path and number of gate counts.
3. For all four problems, TAs will assist to test whether your Matlab and Verilog programs lead to correct results. Hence, you need to pass TAs’ examination after sending the report to get the credit.