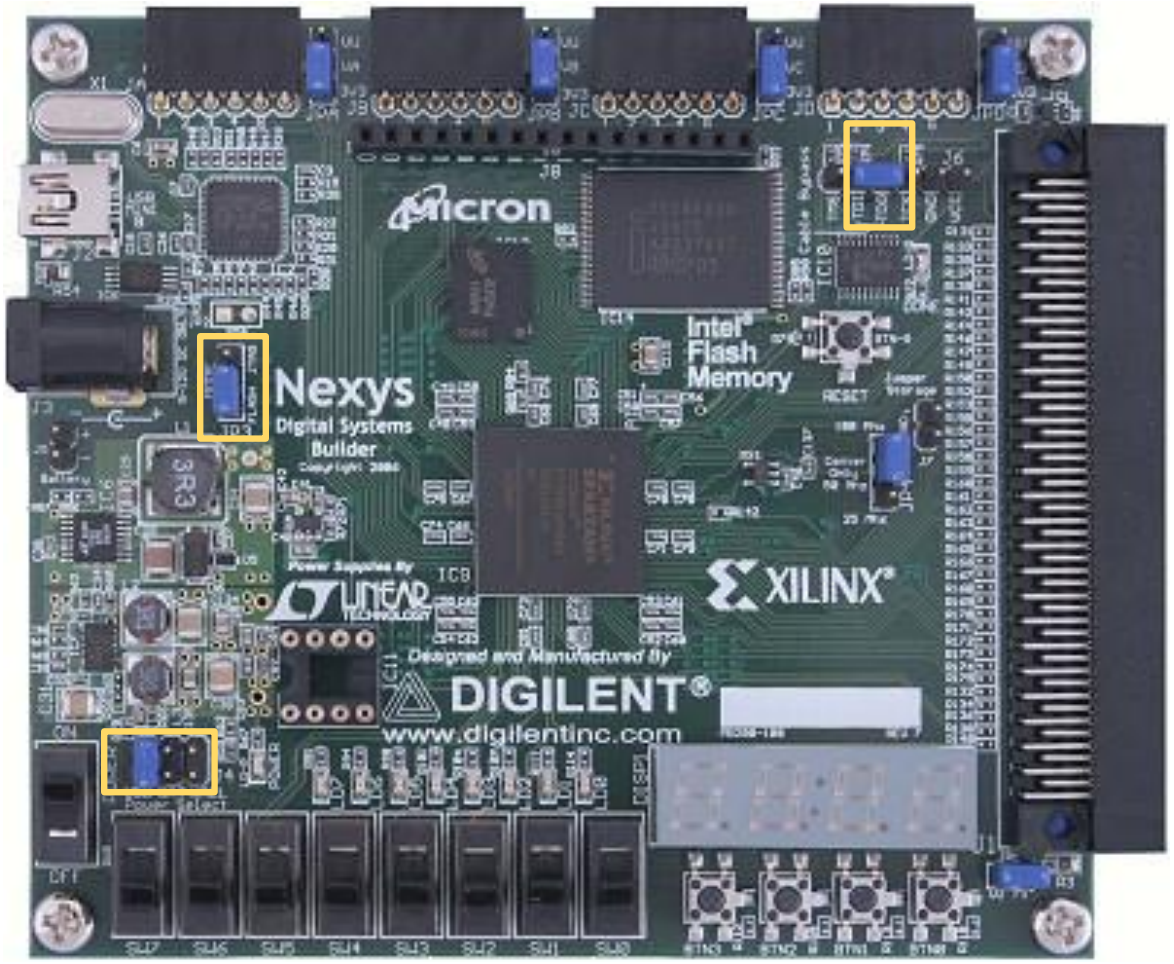
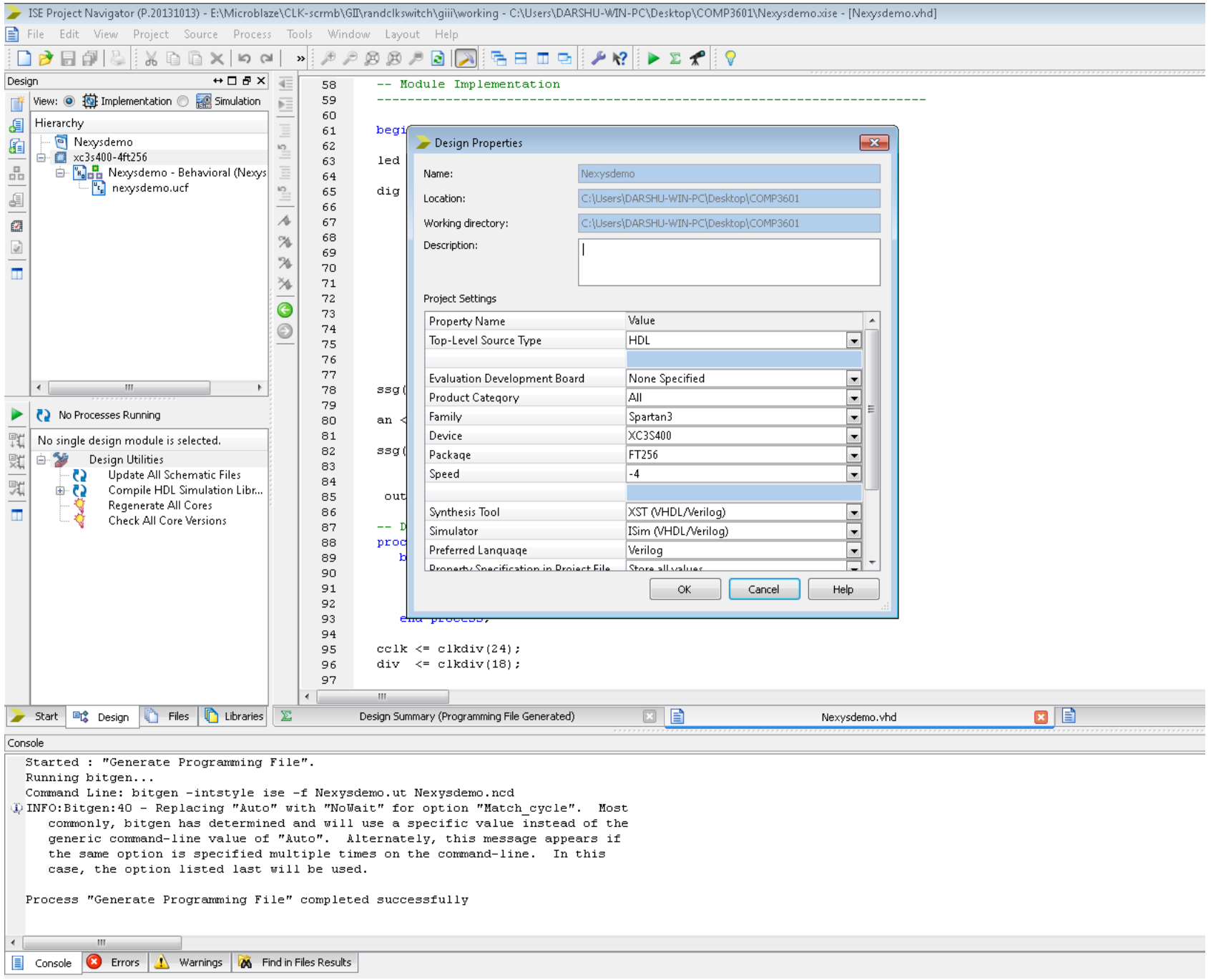
Digilent Nexys FPGA Board

Digilent Nexys FPGA Board



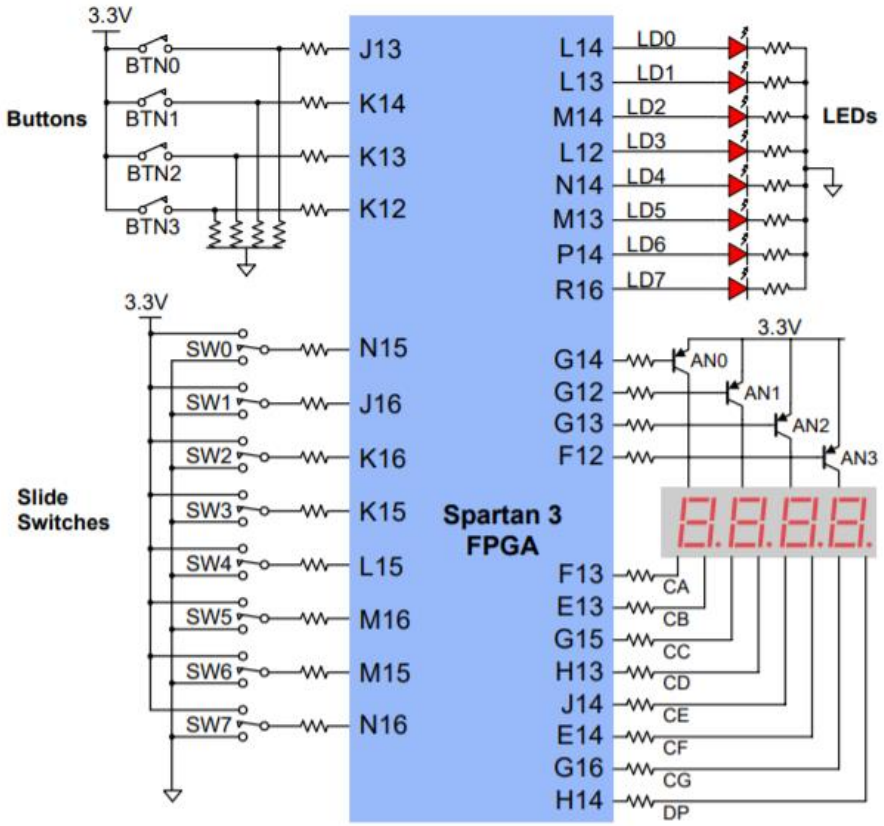
1. Schematic
2. Adept
3. Nexys Board Constraint file
4. SDK

- Xilinx Spartan 3 XC3S400 FPGA with 500+MHz operation
- USB2 port for FPGA configuration and data transfers
  16MB of fast Micron SDRAM
  and 4MB of Intel Flash ROM
- Xilinx Platform Flash ROM
- 50 MHz Oscillator (25MHz or 100MHz)
- 60 FPGA I/Os routed to expansion connectors (one high-speed Hirose FX2 connector and four 6-pin headers)
- 8 LEDs, 4-digit seven-segment display, 4 pushbuttons, 8 slide switches



- Make sure you set XC3S400 as Device if you download sample project from Digilent
- Make sure you install Xilinx ISE (not VIVADO) on your computer

Switches and LEDs



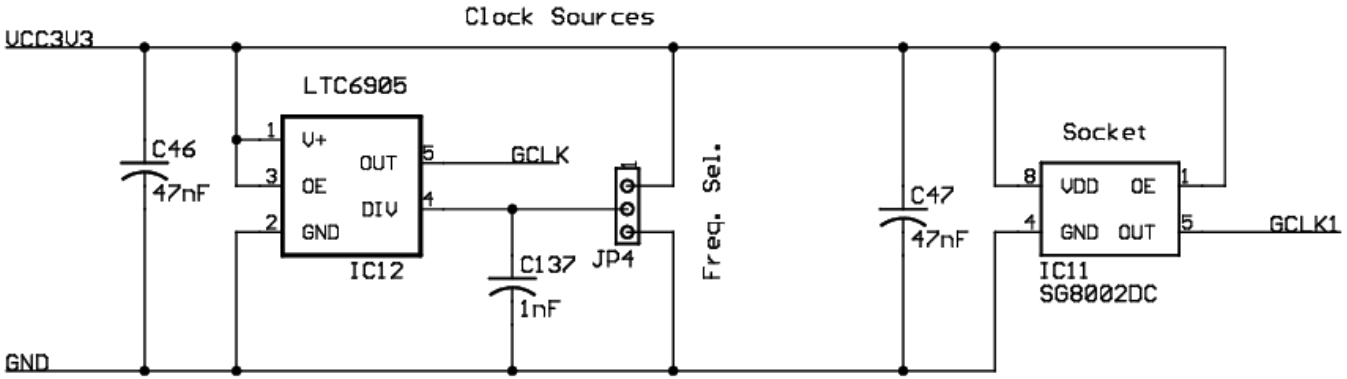
nexys_demo_simple.zip

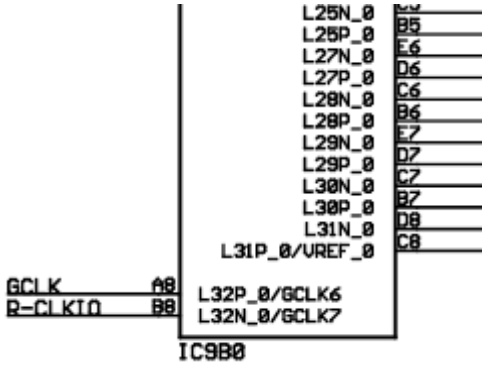
nexysdemo.ucf

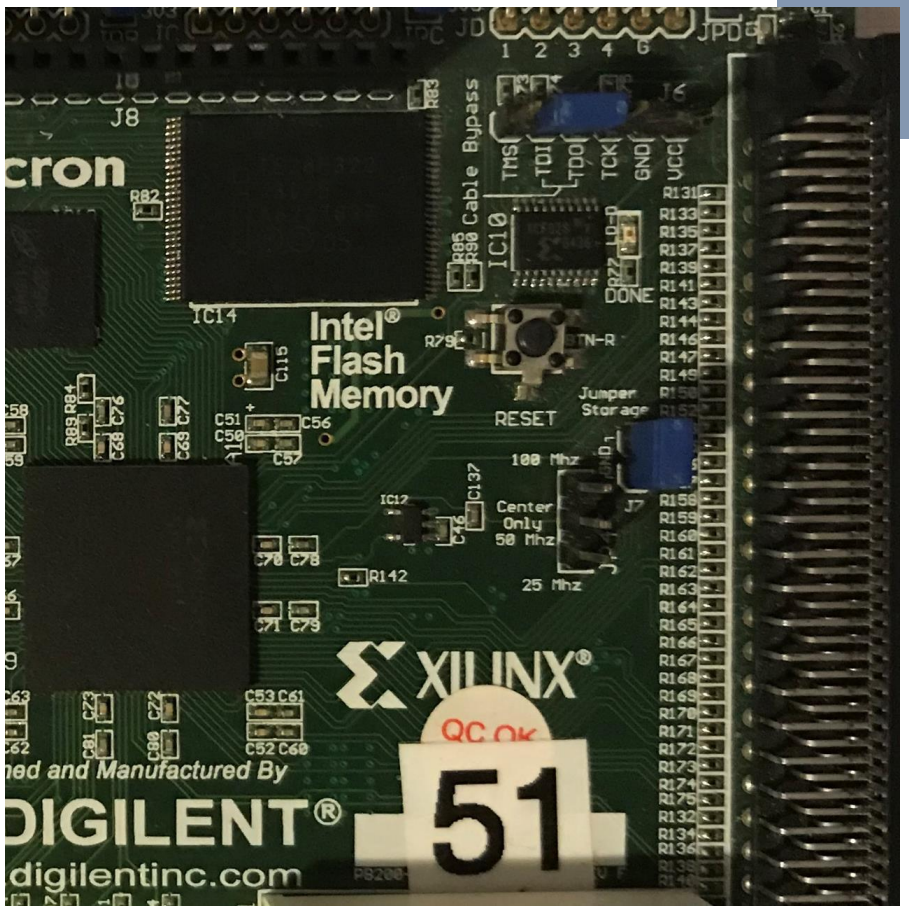
```
NET “CLK" LOC = "A8";

NET “BTN<0>” LOC = "J13";
NET “BTN<1>” LOC = "K14";
NET “BTN<2>” LOC = "K13";
NET “BTN<3>” LOC = "K12";

NET “SW<0>” LOC = "N15";
NET “SW<1>” LOC = "J16";
NET “SW<2>” LOC = "K16";
NET “SW<3>” LOC = "K15";
NET “SW<4>” LOC = "L15";
NET “SW<5>” LOC = "M16";
NET “SW<6>” LOC = "M15";
NET “SW<7>” LOC = "N16";

NET “AN<0>”  LOC = "G14";
NET “AN<1>”  LOC = "G12";
NET “AN<2>”  LOC = "G13";
NET “AN<3>”  LOC = "F12";
NET “CA<0>” LOC = "F13";
NET “CB” LOC = "E13";
NET “CC” LOC = "G15";
NET “CD” LOC = "H13";
NET “CE” LOC = "J14";
NET “CF” LOC = "E14";
NET “CG” LOC = "G16";
NET “DP” LOC = "H14";

NET “LD<0>” LOC = "L14";
NET “LD<1>” LOC = "L13";
NET “LD<2>” LOC = "M14";
NET “LD<3>” LOC = "L12";
NET “LD<4>” LOC = "N14";
NET “LD<5>” LOC = "M13";
NET “LD<6>” LOC = "P14";
NET “LD<7>” LOC = "R16";
```

Clock Supply

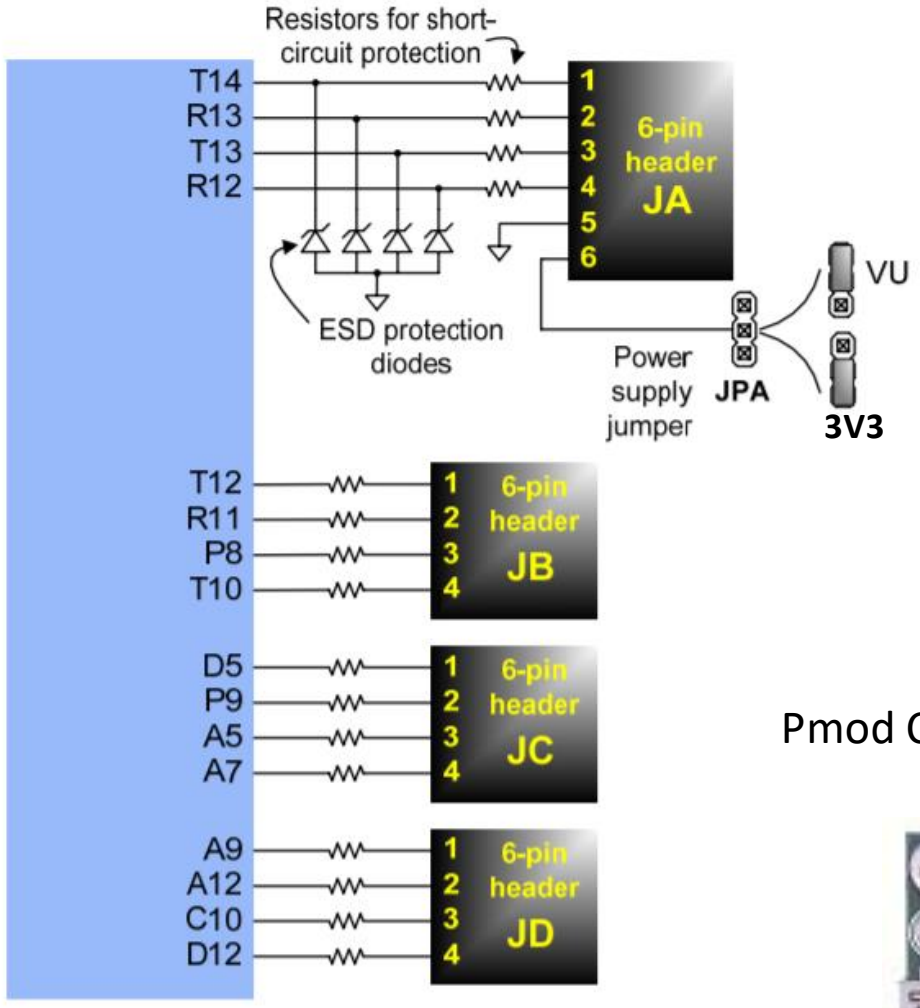
Clock is supplied by a ~~50~~ 100 MHz oscillator (25MHz or 50MHz)
JP4 can change the input clock frequency to the FPGA







Pmod - Peripheral Module Interface



- 4 Pmod connectors
- Don’t worry to explore Digilent FPGA board
- You can use power from the FPGA board drive low power and low voltage components
- Power supply jumper (JPA, .., JPD) change voltage 6th pin of PMOD-> 3.0-3.3V (3V3) or 5V (VU)

Pmod Connectors

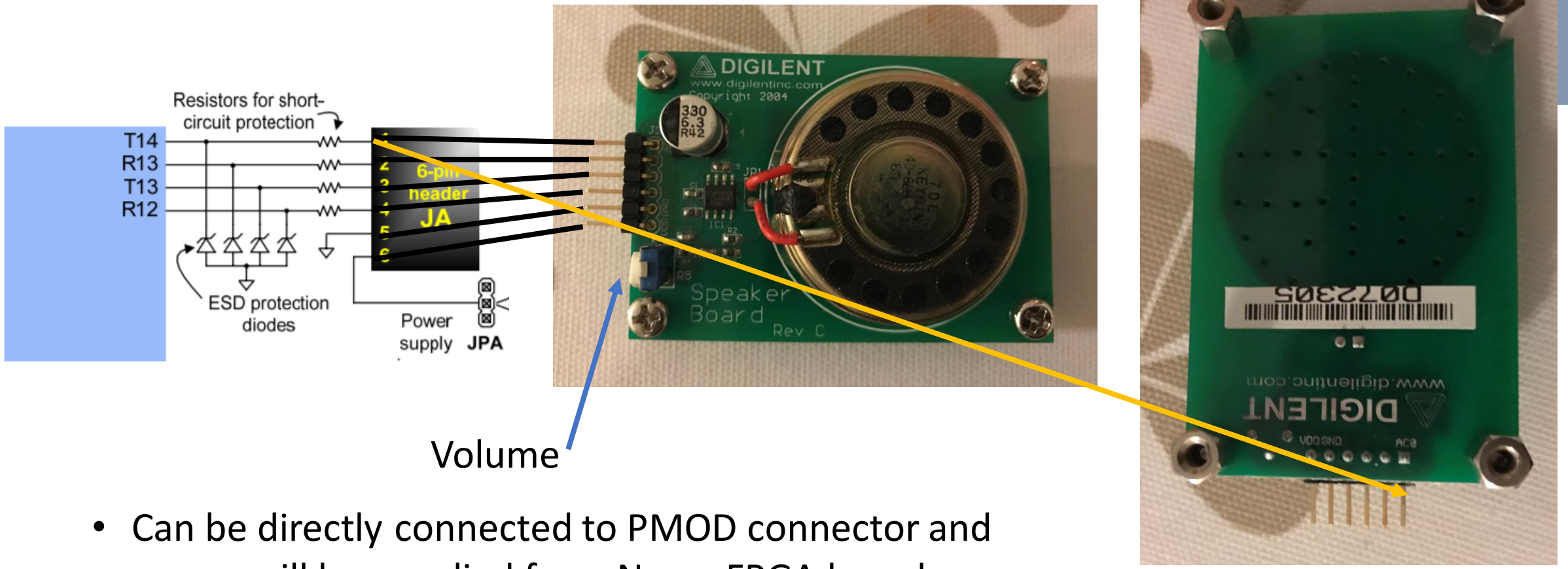
FX2 Breadboard Expansion Add-On Board

- Eight 6-pin headers (Pmod)
- Breadboard is to implement your circuit

- For those who have not used a bread board,

https://learn.sparkfun.com/tutorials/how-to-use-a-breadboard/all

Digilent PMOD Speaker



- Can be directly connected to PMOD connector and power will be supplied from Nexys FPGA board
- Supply audio signal – wave to AC0 pin
- In this example, set T14 pin in the constraint file

Adept

- From Digilent
- Can program Xilinx XC3S400 FPGA on Nexys board
- Can program flash memory
- Can send/receive data (user) from/to Nexys board to/from PC via EPP- Enhanced Parallel Port

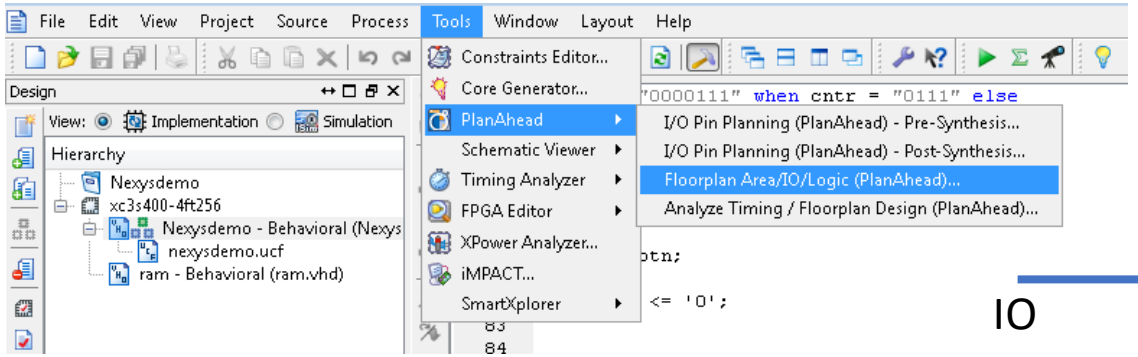
SDK

- URL: https://reference.digilentinc.com/reference/software/adept/start
- Communicate with USB controller to send/receive user data from your programs (not via Adept).

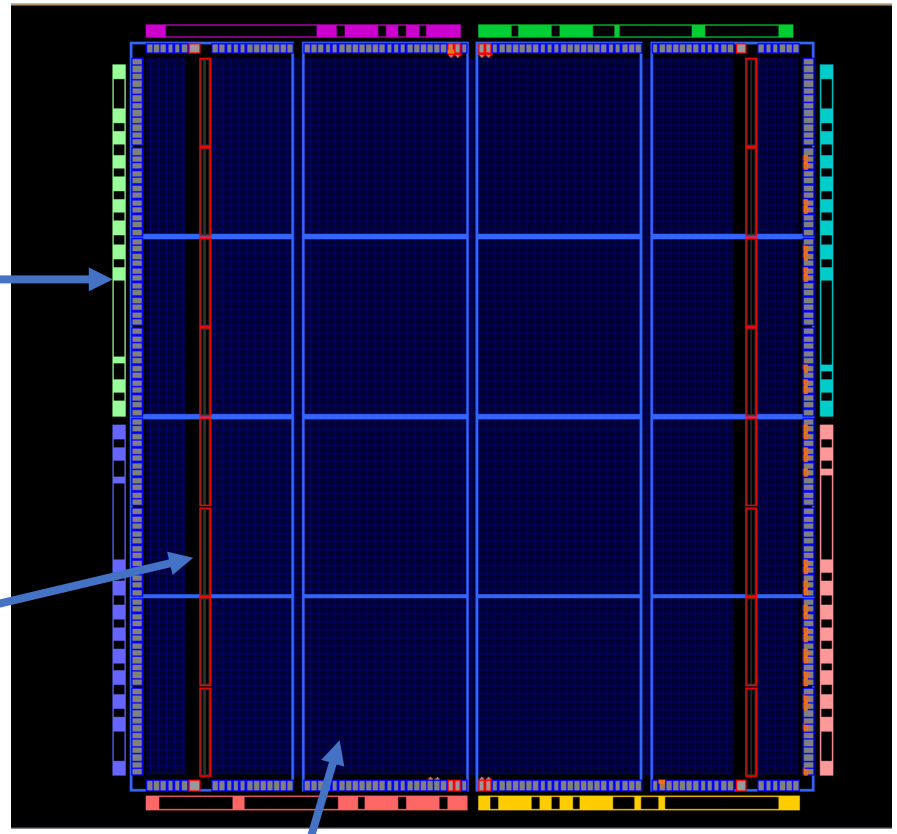
On-chip Memory

- Distributed Memory
  - Can be Asynchronous – does not need a clock
  - Implemented using Flip Flops/ latches or LUTs (Lookup Tables) in the FPGA
  - Might not have enough capacity to hold music file(s)
  - 56Kb memory in Xilinx XC3S400 <- you need resources for logic
- Block Ram
  - Synchronous (negative edge or positive edge of the clock)
  - Fabricated circuit in FPGA
  - Implemented in 36Kb blocks (can be divided into 2x18kb blocks)
  - Dual port -> read and write simultaneously
  - 288Kb memory in Xilinx XC3S400
  - manually instantiated (complex) - Xilinx Spartan-3 Libraries Guide for HDL Designs

Floor Plan



Xilinx XC3S400



IO

Block RAMs

Slices -> logic

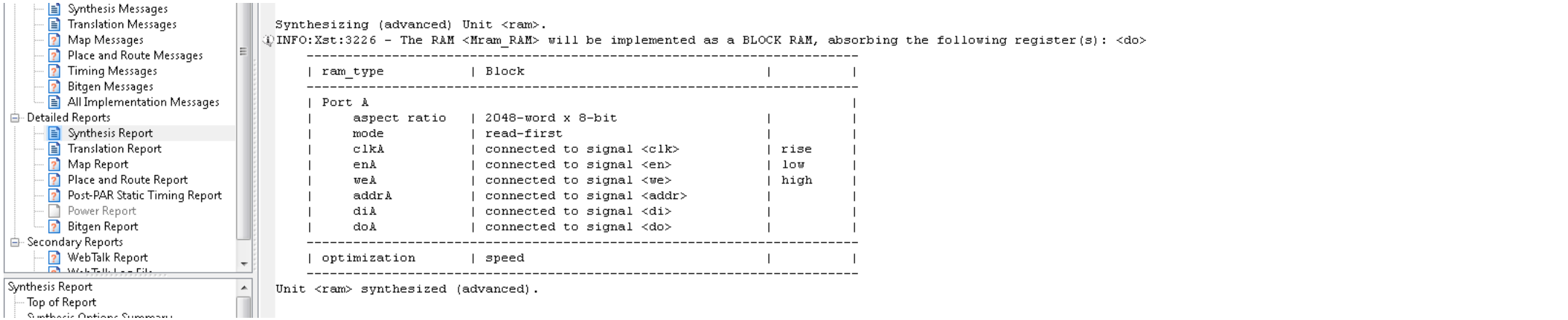
Block RAM

Automatic RAM Recognition:
UG627, XST User Guide…
page 133

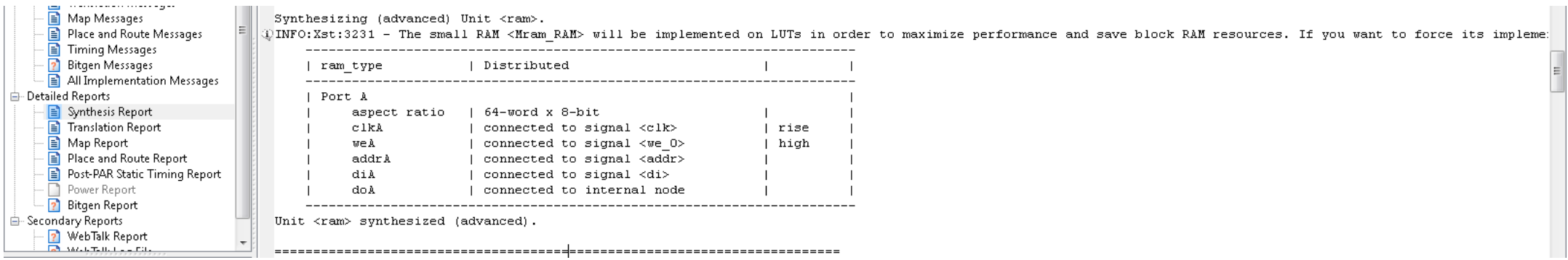
```
-- Read-First Mode –
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

ENTITY rams_01 IS
    PORT (clk : in std_logic;
    we : in std_logic;
    en : in std_logic;
    addr : in std_logic_vector(5 downto 0);
    di : in std_logic_vector(15 downto 0);
    do : out std_logic_vector(15 downto 0));
END rams_01;
ARCHITECTURE syn OF rams_01 IS
    TYPE ram_type IS array (63 downto 0) OF std_logic_vector (15 downto 0);
    SIGNAL RAM: ram_type;

BEGIN
    PROCESS (clock)
    BEGIN
        IF rising_edge(clock) THEN
            IF en = '1' THEN
                IF we = '1' THEN
                    RAM(conv_integer(addr)) <= di;
                END IF;
                do <= RAM(conv_integer(addr)) ;
            END IF;
        END IF;
    END PROCESS;
END SYN;
```

Synthesis report

- 2048 x 8bit RAM

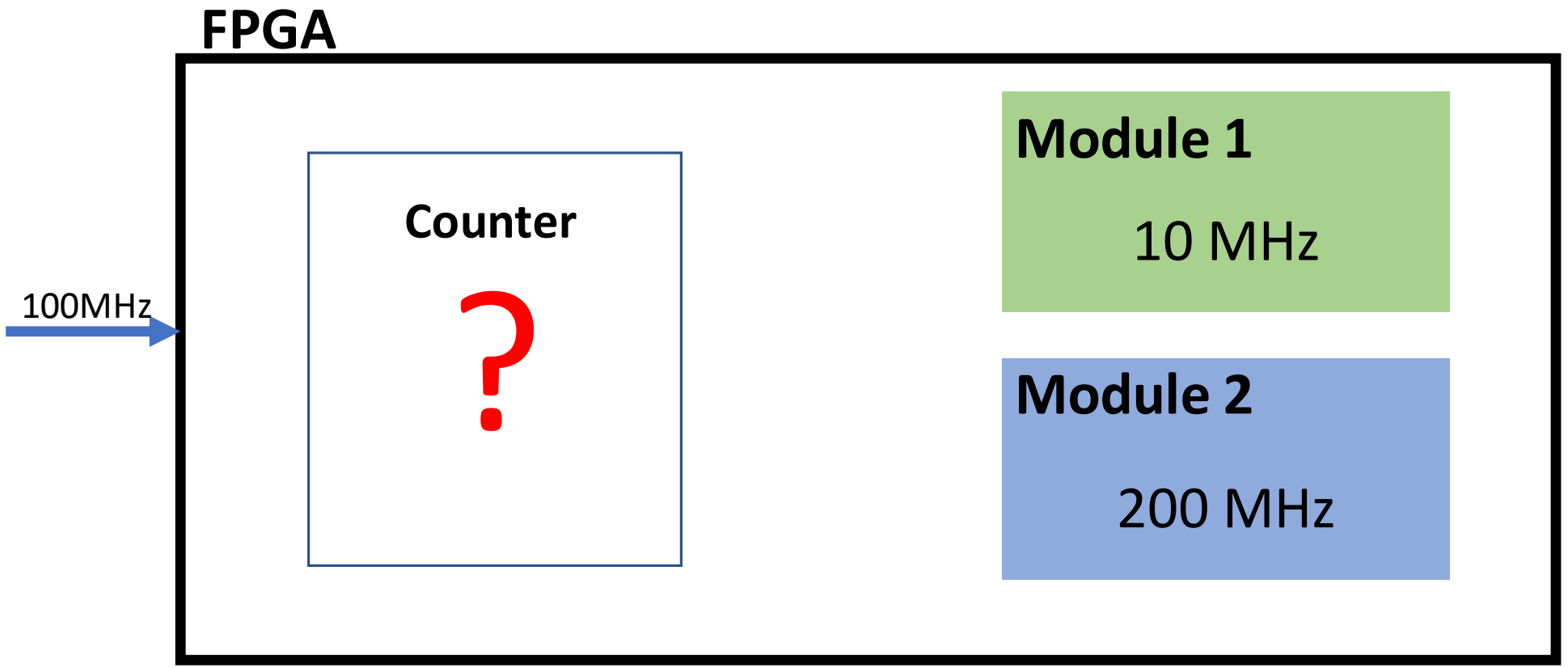


- 64 x 8bit RAM



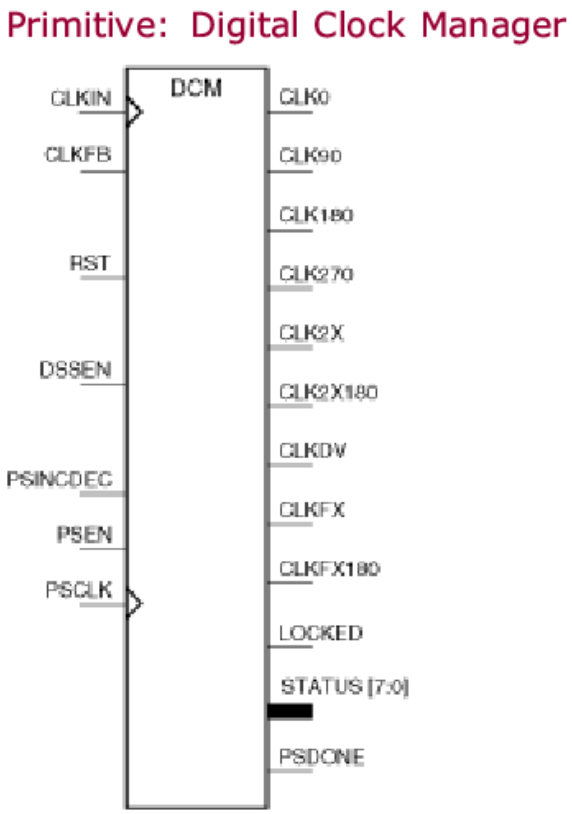
Managing Clocks

- Clocks determine the latency/throughput of your hardware design



Clock Tree

- Xilinx FPGAs have multiple clock trees – dedicated clock routes to balance skew and minimize the delay
  - Xilinx Spartan 3 FPGAs have 8 clock networks
- Use Digital Clock Manager (DCM)
- More information on DS485 - Digital Clock Manager (DCM) Module Data Sheet (v1.9)




```
DCM_inst : DCM
generic map (
CLKDV_DIVIDE => 2.0, --  Divide by: 1.5,2.0,2.5,3.0,3.5,4.0,4.5,5.0,5.5,6.0,6.5
--     7.0,7.5,8.0,9.0,10.0,11.0,12.0,13.0,14.0,15.0 or 16.0
CLKFX_DIVIDE => 1,   --  Can be any interger from 1 to 32
CLKFX_MULTIPLY => 4, --  Can be any integer from 1 to 32
CLKIN_DIVIDE_BY_2 => FALSE, --  TRUE/FALSE to enable CLKIN divide by two feature
CLKIN_PERIOD => 0.0,          --  Specify period of input clock
CLKOUT_PHASE_SHIFT => "NONE", --  Specify phase shift of NONE, FIXED or VARIABLE
CLK_FEEDBACK => "1X",         --  Specify clock feedback of NONE, 1X or 2X
DESKEW_ADJUST => "SYSTEM_SYNCHRONOUS", --  SOURCE_SYNCHRONOUS, SYSTEM_SYNCHRONOUS or
--     an integer from 0 to 15
DFS_FREQUENCY_MODE => "LOW",     --  HIGH or LOW frequency mode for frequency synthesis
DLL_FREQUENCY_MODE => "LOW",     --  HIGH or LOW frequency mode for DLL
DUTY_CYCLE_CORRECTION => TRUE, --  Duty cycle correction, TRUE or FALSE
FACTORY_JF => X"C080",          --  FACTORY JF Values
PHASE_SHIFT => 0,        --  Amount of fixed phase shift from -255 to 255
SIM_MODE => "SAFE", -- Simulation: "SAFE" vs "FAST", see "Synthesis and Simulation
```

Lab Equipment

- GW Instek GDS-820s Digital Oscilloscope
- Available in Lyre Lab

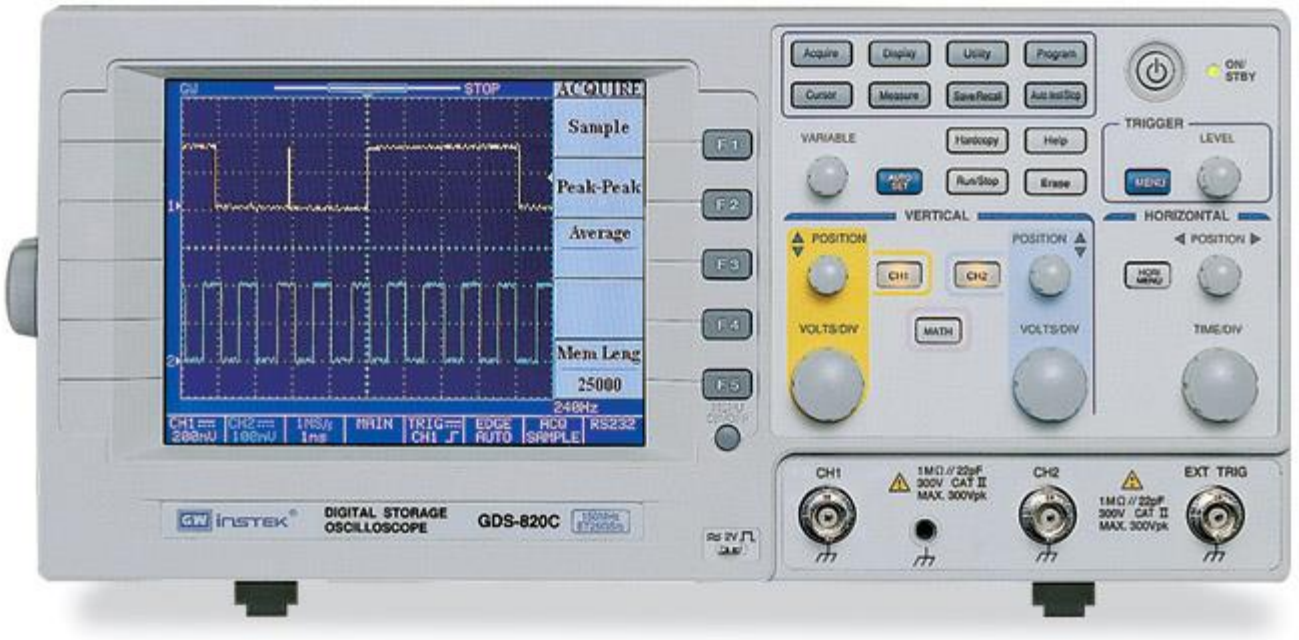


Image Source: http://www.elettronicaetruria.it