

# ReadyPower: A Reliable, Interpretable, and Handy Architectural Power Model Based on Analytical Framework

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**Abstract**—Power is a primary objective in modern processor design, requiring accurate yet efficient power modeling techniques. Architecture-level power models are necessary for early power optimization and design space exploration. However, classical analytical architecture-level power models (e.g., McPAT) suffer from significant inaccuracies. Emerging machine learning (ML)-based power models, despite their superior accuracy in research papers, are not widely adopted in the industry. In this work, we point out three inherent limitations of ML-based power models: unreliability, limited interpretability, and difficulty in usage.

This work proposes a new analytical power modeling framework named ReadyPower, which is ready-for-use by being reliable, interpretable, and handy. We observe that the root cause of the low accuracy of classical analytical power models is the discrepancies between the real processor implementation and the processor’s analytical model. To bridge the discrepancies, we introduce architecture-level, implementation-level, and technology-level parameters into the widely adopted McPAT analytical model to build ReadyPower. The parameters at three different levels are decided in different ways. In our experiment, averaged across different training scenarios, ReadyPower achieves  $> 20\%$  lower mean absolute percentage error (MAPE) and  $> 0.2$  higher correlation coefficient  $R$  compared with the ML-based baselines, on both BOOM and XiangShan CPU architectures.

## I. INTRODUCTION

Power is a primary design objective in modern processor design, requiring accurate yet efficient power modeling techniques. The standard power estimation process requires the full VLSI design flow—requiring Register-Transfer Level (RTL) implementation, followed by RTL simulation, logic synthesis, and gate-level power analysis with EDA tools [1]–[3]. While this process delivers high accuracy, it incurs substantial manpower and runtime, making it impractical for rapid design iterations. As a result, architecture-level power models are in high demand for early power optimization and design space exploration. There are two types of architecture-level power models: 1) conventional analytical models, and 2) recent machine learning (ML)-based models, as we introduce below.

**Analytical Power Model:** Conventional architecture-level power models are analytical models, such as McPAT [4] and Wattch [5]. These models require engineers to meticulously characterize each microarchitectural component within a target processor [6]. As a result, they typically suffer from significant inaccuracies when applied to new architectures, as indicated in many existing studies [6].

**ML-based Power Model:** In recent years, machine learning (ML)-based architecture-level power models emerged to address the accuracy limitations of traditional analytical models. These data-driven models construct either black-box [7] or gray-box [8] representations of power consumption. The models are trained with known processor design configurations with ground-truth power values. When trained with appropriate data, these ML-based models have demonstrated high accuracy compared to analytical models.

**Rethinking: why are ML-based models not widely adopted?** Despite the clearly superior accuracy of recent ML-based power models [7]–[9], unexpectedly, we notice that these new ML-based methods are not widely adopted in the industry. Instead, architects continue to utilize analytical models such as McPAT, although substantial engineering effort is required to fix the inaccuracies. This observation motivates this work, which starts with rethinking the problem of existing research on ML-based power models. We point out three inherent limitations of ML-based power models below.

- 1) **Unreliability:** ML models are inherently weak at *extrapolation*, since ML models are performing *interpolation*<sup>1</sup> based on training data. As a result, ML models can become extremely unreliable when the testing data falls *out of the distribution* of training data. For instance, models trained only on small processor

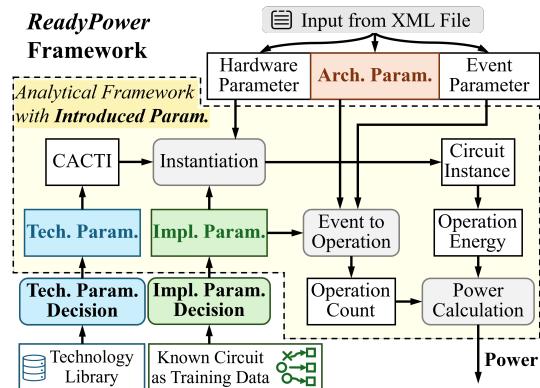


Fig. 1: The ReadyPower framework. ReadyPower fixes the discrepancies between real processor implementation and classical power models. It introduces new architecturally interpretable parameters at the architecture, implementation, and technology levels within the analytical framework.

configurations will be highly inaccurate when applied to large configurations, and vice versa<sup>2</sup>.

- 2) **Limited Interpretability:** ML-based power models are inherently black-box, preventing the interpretation of their power calculation mechanism. The parameters (i.e., weights) of ML-based power models are calculated by directly fitting training data, without representing any realistic physical information.
- 3) **Difficulty for Usage:** Existing ML-based power models are mostly research works and involve complex training stages before being ready for use. They do not provide a consistent user interface that can be easily used by designers or incorporated into the existing design environment.

Besides these three inherent limitations, some recent ML-based power models [8] further require significant designer expertise to customize the model towards each new target processor architecture, setting an additional barrier to the adoption of ML-based models.

**ReadyPower:** In this work, we propose a novel architecture-level power model named ReadyPower, addressing the aforementioned challenges. As its name suggests, ReadyPower stands for a ready-for-use power model by being reliable, interpretable, and handy<sup>3</sup>. Different from all existing ML-based power models, as shown in Fig. 1, our solution adopts the original framework and interface of a classical analytical model (i.e., McPAT [4]) for easy deployment and usage. Specifically, we introduce new parameters internally inside McPAT’s analytical framework, and decide the parameter values based on a few known designs (i.e., training data).

ReadyPower is designed based on a key observation: the root cause of inaccurate analytical models is the *discrepancies between the real processor implementation and the processor’s analytical model*, and the discrepancies exist in all three major levels (architecture, implementation, and technology levels). We will further elaborate on this observation in Sec. III. As Fig. 1 shows, ReadyPower bridges the discrepancies by introducing *new parameters* at all three levels into the analytical framework: 1) Architecture-level new parameters capture important microarchitecture design decisions. These parameters can be directly set by designers as input, since they directly reflect architecture decisions. 2) Implementation-level new parameters capture power characteristics that depend on RTL and downstream design implementation. These parameters’ values are decided based on training data. The gradient of each new parameter is approximated,

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<sup>1</sup>Interpolation is performing inference within the range (i.e., distribution) of the known training data, while extrapolation goes beyond the range.

<sup>2</sup>All existing ML-based power modeling works [7]–[9] evade this limitation by using very similar training and testing configurations in the experiment.

<sup>3</sup>Our proposed ReadyPower framework has been fully open-sourced at <https://github.com/hkust-zhiyao/ReadyPower>. It adopts the same user interface as McPAT, ready for designers to directly use it.

and then gradient descent is performed for training. 3) Technology-level new parameters reflect the process technology. These parameters are design-agnostic, decided solely based on technology libraries.

ReadyPower solves the three inherent limitations of ML-based power models: 1) *Reliable*: ReadyPower maintains consistent high accuracy even when testing data falls out of the training data distribution. Instead of directly fitting the ultimate total power value, ReadyPower fixes discrepancies at each level within the analytical framework. Moreover, it set a reasonable range for all introduced parameters. This framework prevents the unexpected large variations in complex ML models' predictions. 2) *Interpretable*: Unlike black-box alternatives, each new parameter introduced in ReadyPower corresponds to an explicit physical parameter in the processors. Each step of the power calculation is also explicitly defined and architecturally interpretable. 3) *Ready-to-use*: ReadyPower adopts the same user interface as the McPAT [4]. Therefore, when deployed in the industry, it can be easily integrated into the existing frameworks with McPAT as a component, without any modification to other components.

## II. BACKGROUND

### A. Architecture-Level Power Model

Generally, architecture-level power model takes hardware parameters and event parameters as input to estimate processor power consumption when running a workload. The hardware parameters  $H$  represent processor configurations, such as FetchWidth and DCacheWay. Event parameters  $E$  are architecture-level events when a processor executes a workload, such as the number of branch mispredictions and the number of data cache misses. Event parameters are collected from architecture-level performance simulators, such as gem5 [10], by simulating a workload on a specific processor configuration.

In recent years, ML solutions are widely adopted in EDA applications [8], [11]–[20]. Existing architecture-level power models include the analytical model and the ML-based model [8]. Analytical power models [4], [5] derive individual models for each component based on the background knowledge of model developers. It first models the energy consumption of each event based on hardware parameters  $H$ , and then calculates the final power with event parameters  $E$ .

ML-based power models [7], [8], [21] directly learn the correlation between the input features (i.e., hardware parameters  $H$  and event parameters  $E$ ) and the final power consumption with an ML model automatically. However, as mentioned in the Introduction, ML solutions can be unreliable, uninterpretable, and difficult to use.

### B. Analytical Model Framework

We introduce the representative analytical power model, McPAT [4], whose analytical framework is adopted in ReadyPower. McPAT takes an XML file as its input. The XML file includes the hardware parameters  $H$  and event parameters  $E$ .

With the input XML file, McPAT estimates the power consumption in two steps, as shown in Fig. 1. **Step 1:** With hardware parameters  $H$ , McPAT instantiates each component based on the CACTI [22] to collect energy consumption of each operation. For example, for ICache, McPAT first calculates the configuration, such as cache size `cache_sz` and tag width `tag_w`, from the hardware parameters `icache_config`. Then McPAT uses the configuration to instantiate an array from CACTI. The generated instance provides the energy consumption of an ICache read `readOp` and an ICache write `writeOp`. **Step 2:** With event parameters  $E$  and energy per operation collected from the first step, McPAT transforms events into operations based on the component microarchitecture and then calculates the component energy. Power is energy divided by execution time. Following ICache example, each hit is transformed into a `readOp`, each miss is transformed into a `readOp` and a `writeOp`. Then energy consumption is calculated based on the total number of `readOp` and `writeOp` and energy consumption per operation.

## III. RETHINKING: HOW TO IMPROVE ANALYTICAL MODEL

**Observation:** The root cause of the low accuracy when applying analytical models to a new processor architecture is the *discrepancies between the real processor implementation and the processor's analytical model*. The discrepancies exist in all three major levels, including microarchitecture design, RTL implementation, and technology.

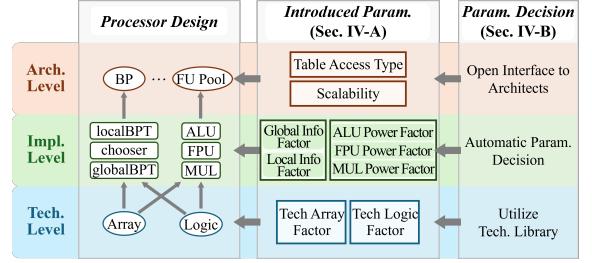


Fig. 2: The methodology overview of ReadyPower.

At each level, different processor architectures may adopt different design options, while the analytical models only support one or very few options, resulting in discrepancies: 1) For the microarchitecture design, each component has multiple design options. For example, for the ICache, some processors adopt a low-latency design where the tag array and data array are accessed simultaneously to reduce the ICache access latency. Some other low-power processors may access the data array after the tag array access, reducing the power consumption with fewer data array accesses. 2) For the RTL implementation, the same component can be implemented differently, even with similar functions. For the array structure, continuing with the ICache example, the tag array width may differ in different implementations, because it may hold different numbers of extra bits to represent status. For the logic structure, such as control logic, its design is even more flexible and leads to different power consumption [23]. 3) For the technology, analytical methods model the technology node by setting and scaling empirical built-in values, such as CACTI [22]. These empirical values cannot always accurately reflect the real technology library, such as TSMC [24] across various process nodes.

Existing ML-based power models [7] are fixing the discrepancy-induced inaccuracies with data-driven approaches. They typically *walk around* the discrepancy problem by directly calibrating the ultimate total power value towards ground-truth with a black-box ML model. As a result, they work well when the test designs fall within the distribution of training designs, but suffer from serious unexpected accuracy degradation when inferring out-of-distribution test data. We demonstrate this with detailed experiments in Section V-D.

Instead of directly calibrating the total power, ReadyPower bridges the discrepancies at each level by introducing new parameters, each with a realistic meaning in power calculation. These ReadyPower-introduced parameters capture the design option of the real target processor architecture (i.e., BOOM, XiangShan) internally in its analytical framework. Please note that ReadyPower only adopts data-driven methods to decide the values of its introduced new parameters for the target architecture. It is a purely white-box analytical model without an ML component during its power calculation.

## IV. METHODOLOGY

This section introduces the detailed methodology of ReadyPower, with an overview shown in Fig. 2. In Sec. IV-A, we elaborate on the introduced parameters at each level. In Sec. IV-B, we introduce our proposed customized parameter decision methods for each level. We also describe our implementation of ReadyPower in Sec. IV-C.

### A. Introduced New Parameters

We introduced architecture-level, implementation-level, and technology-level parameters into the widely adopted McPAT analytical model. In this section, we will first introduce the general out-of-order processor architecture, and then describe introduced new parameters of each level.

**CPU Architecture:** Before elaborating on our introduced parameters, we first introduce a general CPU core architecture adopted by ReadyPower. Our target Out-of-Order CPU core includes 10 major components with: Branch Predictor (BP), Instruction Fetch Unit (IFU), Instruction Cache (ICache), Renaming Unit (RNU), Reorder Buffer (ROB), Instruction Schedule Unit (ISU), Register File (Regfile), the pool of functional units (FU Pool), Load Store Unit (LSU), and Data Cache (DCache). Other circuits not covered above are referred to as Other Logic.

**Architecture-Level Parameter:** Architecture-level parameters capture major microarchitecture design decisions. The introduced architecture-level parameters satisfy two points: 1) The parameters

can be easily identified at the microarchitecture design level by architects. 2) The parameters have a significant impact on the power consumption. Therefore, the number of architecture-level parameters can be controlled at an acceptable level for ease of use.

The first part of Table I summarizes 5 architecture-level parameters introduced in our framework. 1) For the ICache, the processors may adopt a *Low Latency* design or a *Low Power* design for the data array. We refer to its relevant new parameter as *Table Access Type*. Besides, in some high-performance processors like BOOM [25], the ICache line size may scale up with the *FetchWidth* to provide scalable throughput. We refer to it as *Scalability*. 2) For the BP, similar to the ICache, as a part of Frontend, it also adopts two architecture-level parameters *Table Access Type* and *Scalability*. 3) For the DCache, in superscalar processors, it should support multi-port access. The design has multiple options, so we introduce *Multi-Port Design* as a parameter, with two options: *Multi-Banking* and *Duplicated Array*.

**Implementation-Level Parameter:** Implementation-level parameters capture differences across different RTL implementations. The implementation-level parameters mainly tackle three major problems: 1) For the logic structure, the estimations in analytical models are usually too rough because of the lack of RTL implementation information. Therefore, parameters should be introduced to capture the real logic implementation in the processor. 2) For the array structure, while it is architecturally visible and well-defined, its actual RTL implementation, including precise width and physical size, remains indeterminate at the architecture level. This uncertainty stems from the multiple implementation options available for any given architectural function. 3) In addition to the two points above, which target parameters related to the hardware design, the inaccuracy of event parameters also introduces the inaccurate prediction of the power model. Therefore, we introduce the most important parameters to deal with the event inaccuracy.

The second part of Table I lists our introduced 18 implementation-level parameters. 1) For BP, as discussed above, parameters are required to model an equivalent implementation for a variety of processors. Therefore, we set *Global Info Factor* to scale array size of global table and chooser, and *Local Info Factor* to scale array size of local table. 2) For ICache and DCache, data array size is determined at architecture level, however, the width of tag array should be configurable because processors usually integrate some metadata beyond tag, such as security-related bits and some other bits to represent status. Therefore, we introduce *ICache MetaData Bit* and *DCache MetaData Bit* as the number of additional bits beyond tag. 3) For IFU, RNU, LSU, and Other Logic, these components have logic as their major circuits. Parameters are required to capture the scale of general logic designs. Therefore, we introduce *IFU Logic Factor*, *RNU Logic Factor*, *LSU Logic Factor*, and *Other Logic Factor*. 4) For Regfile, Regfile in modern processors is physical register file. The width is larger than architectural registers, with some bits to keep information related to, for example, renaming. Therefore, we introduce *Physical Regfile Width* representing the ratio between the real and architectural register width. 5) For ISU and ROB, status bits are usually included to store instruction status to assist scheduling. Therefore, *Inst. Window Width* and *ROB Entry Width* are introduced to represent status bits. 6) For FU Pool, the FPU, ALU, and MUL are included for computation. To capture the real power consumption of computation, we introduce *FPU Power Scale*, *ALU Power Scale*, and *MUL Power Scale* to represent the bias between target real design and default design in original analytical model. 7) For ICache and DCache, to tackle inaccurate event parameters, we scale the number of hits and misses linearly with our introduced *Access Coefficient* and *Access Bias*.

**Technology-Level Parameter:** Technology-level parameters represent the difference among different technology libraries. Although analytical models such as McPAT [4] account for technology library differences, their estimations rely on empirical knowledge and thus lack sufficient accuracy. As a result, detailed technology-level parameters are still necessary.

However, capturing all details of the technology library is infeasible. We observe that logic cells generally follow one consistent scaling trend, while array macros adhere to another. To incorporate the impact of the technology node while maintaining model simplicity, we represent its effect using 2 parameters, as shown in the third part

Component	Arch.-Level Param.	Type	Range	Default
ICache	Table Access Type	Enum	Low Latency / Low Power	Low Power
	Scalability	Bool	Yes / No	No
BP	Table Access Type	Enum	Low Latency / Low Power	Low Power
	Scalability	Bool	Yes / No	No
DCache	Multi-Port Design	Enum	Multi-Banking / Duplicated Array	Multi-Banking
Component	Impl.-Level Param.	Type	Range	Default
BP	Global Info Factor	Int	1-64	1
	Local Info Factor	Int	1-64	1
ICache	ICache MetaData Bit	Int	0-64	0
IFU	IFU Logic Factor	Float	0-2	1
RNU	RNU Logic Factor	Float	0-2	1
LSU	LSU Logic Factor	Float	0-2	1
DCache	DCache MetaData Bit	Int	0-64	0
Regfile	Physical Regfile Width	Int	1-16	1
ISU	Inst. Window Width	Int	0-64	0
ROB	ROB Entry Width	Int	0-64	0
FU Pool	FPU Power Scale	Float	0-16	1
	ALU Power Scale	Float	0-16	1
	MUL Power Scale	Float	0-16	1
Other Logic	Other Logic Factor	Float	0-2	1
ICache	Access Coefficient	Float	0-32	1
	Access Bias	Float	0-32	0
DCache	Access Coefficient	Float	0-32	1
	Access Bias	Float	0-32	0
Circuit	Tech.-Level Param.	Type	Range	Default
Logic	Tech Logic Factor	Float	-	1
Array	Tech Array Factor	Float	-	1

TABLE I: Our introduced new parameters in ReadyPower, including 5 architecture-level parameters, 18 implementation-level parameters, and 2 technology-level parameters.

of Table I: *Tech Logic Factor* and *Tech Array Factor*. 1) *Tech Logic Factor* represents the ratio of logic power in the target real technology node to that of the originally modeled node in the analytical model. 2) *Tech Array Factor* represents the analogous ratio for array power. Note that for all processors implemented in the same technology library, these factors remain identical.

### B. Parameter Decision

Building on our proposed analytical power model with our introduced new parameters, ReadyPower provides customized parameter decision methods for each level. 1) For architecture-level parameters that directly reflect microarchitectural decisions, we open the interface for architects' input. 2) For implementation-level parameters, similar to ML-based methods, parameter values are decided automatically by training with a few known design configurations. 3) For technology-level parameters, parameters are decided automatically based on the technology library data. Parameters are decided in the order of: Architecture → Technology → Implementation.

**Architecture-Level Decision:** Architecture-level parameters are visible to architects. Therefore, we open the interface to architects, allowing them to configure architecture-level parameters regarding their target processors. The interface is an extension to the original hardware parameters in the McPAT input XML file. As discussed in Sec. IV-A, we only identify the major microarchitecture decisions that have a significant impact on power consumption, so the number of parameters is acceptable for architects to configure, maintaining the ease of use while ensuring the correctness of these parameters.

**Implementation-Level Decision:** For the implementation-level parameters, we propose an automatic parameter decision algorithm, based on a few known configurations of the target processor architecture as training data. We decide the implementation-level parameters for each component independently.

**Problem Formulation:** Given known configuration-workload combinations as training data, we have their hardware parameters  $H$  and event parameters  $E$  for each component, as power model inputs. We then collect the ground-truth power label  $L$  of each component. We denote the number of implementation-level parameters as  $N$ , the  $i$ -th parameter as  $p_i$ , and the analytical power model as  $f$  with hardware parameters  $H$  and event parameters  $E$  as input. The goal of this automatic parameter decision algorithm is to find the implementation-level parameters  $\{p_1, \dots, p_i, \dots, p_N\}$  that can minimize the error between the model prediction  $P$  denoted as Eq.(1) and the ground truth power  $L$ . We adopt the MSE error as our loss function, as shown in Eq.(2).

$$P = f(H, E, p_1, \dots, p_i, \dots, p_N) \quad (1)$$

$$\text{Loss} = (P - L)^2 \quad (2)$$

*Automatic Parameter Decision Algorithm:* We derive an automatic parameter decision algorithm based on gradient descent, as shown in Eq.(3)(4)(5). For each iterative step during training, parameter  $p_i$  is updated based on its partial gradient and learning rate  $lr$ , as shown in Eq.(3). Partial gradient with respect to  $p_i$  is calculated in Eq.(4).

$$\forall i \in [i, N], p_i \leftarrow p_i - lr * \frac{\partial \text{Loss}}{\partial p_i} \quad (3)$$

$$\frac{\partial \text{Loss}}{\partial p_i} = 2(P - L) \frac{\partial P}{\partial p_i} \quad (4)$$

The task is to calculate the  $\frac{\partial P}{\partial p_i}$  in Eq.(4). As indicated in Eq.(1), power  $P$  is calculated based on the analytical power model  $f$ , which is not directly differentiable. To solve this, we approximate the  $\frac{\partial P}{\partial p_i}$  by slightly changing the parameter  $p_i$  by a tiny  $\delta$  and calculating the slope. Specifically, we first run the analytical model  $f$  to collect the prediction, denoted as  $f(H, E, p_1, \dots, p_i, \dots, p_N)$ , and then increase  $p_i$  by a tiny  $\delta$  to collect the new prediction, denoted as  $f(H, E, p_1, \dots, p_i + \delta, \dots, p_N)$ , finally we approximate  $\frac{\partial P}{\partial p_i}$  as below:

$$\frac{\partial P}{\partial p_i} = \frac{f(H, E, p_1, \dots, p_i + \delta, \dots, p_N) - f(H, E, p_1, \dots, p_i, \dots, p_N)}{\delta} \quad (5)$$

Combining Eq.(3)(4)(5), we can decide all parameters with gradient descent, through multiple iterations. In addition, some introduced parameters  $p_i$  are actually linearly correlated with the analytical model's power estimation  $P$ . For these linear parameters, the  $\frac{\partial P}{\partial p_i}$  is unchanged across iterations and only needs calculation once.

**Technology-Level Decision:** To decide the technology-level parameters, including *Tech Logic Factor* and *Tech Array Factor*, we utilize the information from the technology library. Only these two parameters are introduced to maintain model simplicity.

*Tech Array Factor:* To determine the *Tech Array Factor*, we generate a basic SRAM macro with memory compiler in the technology library, for example, a single-port SRAM with shape  $256 \times 64$ , and collect its read and write energy. Then, we create the same array with CACTI in the McPAT, and collect its read and write energy. Finally, we can calculate the ratio between the read energy of the SRAM macro generated by the memory compiler and the read energy of the array from the analytical model, and the ratio for write energy. We take the average between these two ratios as our *Tech Array Factor*.

*Tech Logic Factor:* Analytical models usually estimate the logic power based on the power estimation of the register, including clock pin power, switch power, and power consumption for keeping 0 and 1. For example, in McPAT, the worst-case power of DFF, where the clock is toggling, is estimated as a base unit for pipeline logic power estimation. Therefore, to align the worst-case power of DFF, we extract the real worst-case power of DFF from the technology library and the original estimation of the worst-case power from McPAT. The ratio between the two values is our decided *Tech Logic Factor*.

### C. Implementation and Interface

Finally, we summarize the implementation of our open-source ReadyPower based on the analytical framework. To introduce our new parameters into the McPAT, we directly modify the source code of McPAT to inject these parameters into the calculation flow of the original McPAT. 1) Architecture-level parameters are injected by modifying the transformation from event to operation. Some others are injected by instrumenting hardware parameters. 2) Implementation-level parameters are encoded by modifying the configuration provided for the circuit instantiation. Event-related ones are injected by scaling event parameters before transformation into operations. 3) We inject technology-level parameters by scaling the operation energy when instantiating circuits with CACTI.

With such a source-code level parameter injection, ReadyPower can maintain the identical user interface (with several additional architecture-level parameters) to the original McPAT.

## V. EXPERIMENTAL RESULTS

### A. Experiment Setup

In our experiment, we adopt two mainstream open-sourced Out-of-order CPU architectures, BOOM [25] and XiangShan [26], which

have been widely adopted in prior works [7], [8], [21], to evaluate our proposed solution. We generate 15 different configurations of BOOM CPU (B1-B15) and 10 configurations of XiangShan CPU (X1-X10) in our experiments, as shown in Table II. To simulate real workloads, we adopt eight workloads in riscv-tests [27], including dhrystone, median, multiply, qsort, resort, towers, spmv, and vvadd.

To collect the ground truth power labels, we perform RTL code generation and RTL simulation of BOOM with Chipyard framework [28] v1.8.1 and XiangShan with the OpenXiangShan framework [26], where Synopsys VCS® [1] is utilized. We then perform logic synthesis with Synopsis Design Compiler® [3]. We turn on the clock-gating option, which is often missed in prior works, during logic synthesis. The post-synthesis power simulation is performed with PrimePower [2]. The whole synthesis and simulation flow is performed based on TSMC 40nm standard cell library [24] and the associated Memory Compiler for SRAM generation. TSMC 28nm library [29] is additionally adopted for the cross-technology-node transfer experiment. To collect the event parameters, we perform architecture-level performance simulation based on gem5 [10].

### B. Training and Testing Data Setup

We introduce our setup of training and testing data in this section. To reflect the real scenarios where limited configurations are available, we set the number of available training configurations to 3. We evaluate each method under three training scenarios with different training data distributions: 1) *Balance*. We evenly select the configurations as available training configurations based on the scale: B1, B8, and B15 for BOOM, X1, X6, and X10 for XiangShan. 2) *Small*. We select the smallest configurations as available training configurations: B1, B2, and B3 for BOOM, X1, X2, and X3 for XiangShan. 3) *Large*. We select the largest configurations as available training configurations: B13, B14, and B15 for BOOM, X8, X9, and X10 for XiangShan. For each training scenario, all remaining configurations are for testing. In *Small* and *Large* training scenarios, the distribution of testing data falls out of the distribution of training data: For *Small* training scenario, *all* testing configurations are *larger* than training configurations. For *Large* training scenario, *all* testing configurations are *smaller* than training configurations. Because of the difference between the distribution of training and testing data, these two scenarios are very challenging and usually ignored by prior works [7], [21]. However, these two training scenarios are important and realistic because architects usually also work on configurations that have different scales from available known configurations.

### C. Summary of Baseline Methods

We compare ReadyPower with representative architecture-level power models as our baseline, including (a) the analytical power model McPAT [4] and (b) the ML-based power model McPAT-Calib [7]. Besides the two baselines proposed in prior works, we also include two extra baselines: (c) McPAT-Plus, an enhanced analytical model. We derive a scaling factor based on the prediction and ground-truth of the available training configurations, and scale the power prediction of McPAT for testing. (d) McPAT-Calib-Component, an enhanced ML-based model. It builds ML-based models for each component, with related hardware parameters and event parameters as features and per-component power as the label. XGBoost [30], the best algorithm reported by McPAT-Calib [7], is adopted as the algorithm for ML-based models.

ASP-DAC'23 [21] and PANDA [8] are beyond the scope of this work. ASP-DAC'23 [21] is a transfer learning method, explicitly requiring training and testing configurations to be similar to enable transfer learning. PANDA [8] requires significant engineering effort to analyze the design and develop resource functions for each component, which is not an automated power modeling method.

### D. Power Modeling Accuracy

Fig. 3 demonstrates the accuracy comparison between ReadyPower and our four baselines. The data shown is the average value across *Balance*, *Small*, and *Large* training scenarios. It shows that our proposed ReadyPower can significantly outperform all baseline methods, including existing analytical power models and ML-based power models, on both BOOM and XiangShan. Averaged across all training

Hardware Parameter	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	X1	X2	X3	X4	X5	X6	X7	X8	X9	X10	
FetchWidth	4	4	4	4	4	8	8	8	8	8	8	8	8	8	4	4	4	4	4	8	8	8	8	8		
DecodeWidth	1	1	1	2	2	2	3	3	3	4	4	5	5	5	2	2	2	3	3	3	4	4	4	5		
FetchBufferEntry	5	8	16	8	16	24	18	24	30	24	32	40	30	35	40	8	16	24	16	24	24	24	32	32	24	
RobEntry	16	32	48	64	64	80	81	96	114	112	128	136	125	130	140	16	32	48	64	64	80	81	96	114	112	
IntPhyRegister	36	53	68	64	80	88	88	110	112	108	128	136	108	128	140	36	53	68	64	64	80	88	88	110	112	108
FpPhyRegister	36	48	56	56	64	72	88	96	112	108	128	136	108	128	140	36	53	68	64	64	80	88	88	110	112	108
LDQ/STQEEntry	4	8	16	12	16	20	16	24	32	24	32	36	24	32	36	16	20	24	20	24	28	24	32	40	32	
BranchCount	6	8	10	10	12	14	14	16	16	18	20	20	18	20	20	7	7	7	7	7	7	7	7	7	7	
Mem/FpIssueWidth	1	1	1	1	1	1	1	1	2	1	2	2	2	2	2	2	2	2	2	2	2	2	2	2		
IntIssueWidth	1	1	1	1	2	2	2	3	3	4	4	4	5	5	5	2	2	2	2	4	4	4	4	6	6	
DCache/ICacheWay	2	4	8	4	4	8	8	8	8	8	8	8	8	8	4	4	8	4	4	8	8	8	8	8		
DTLBEntry	8	8	16	8	8	16	16	16	32	32	32	32	32	32	32	8	8	16	8	8	16	16	32	32		
MSHREntry	2	2	4	2	2	4	4	4	4	4	4	4	4	4	2	2	4	2	4	4	4	4	4	4		
ICacheFetchBytes	2	2	2	2	2	4	4	4	4	4	4	4	4	4	2	2	2	2	2	2	2	2	2	2		

TABLE II: The CPU configurations used in our experiment. The B1-B15 denote the 15 configurations of BOOM, and the X1-X10 denote the 10 configurations of XiangShan. The scales of these configurations are from small to large.

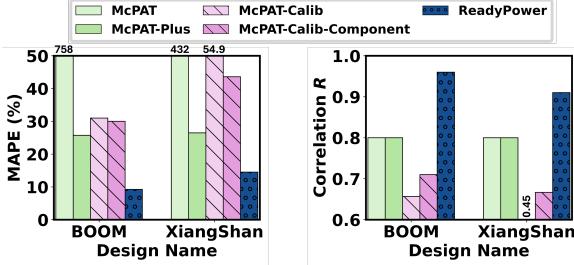


Fig. 3: Accuracy comparison between our proposed ReadyPower and four baseline methods on BOOM and XiangShan CPUs. Each bar is the average across all training scenarios, including *Balance*, *Small*, and *Large*.

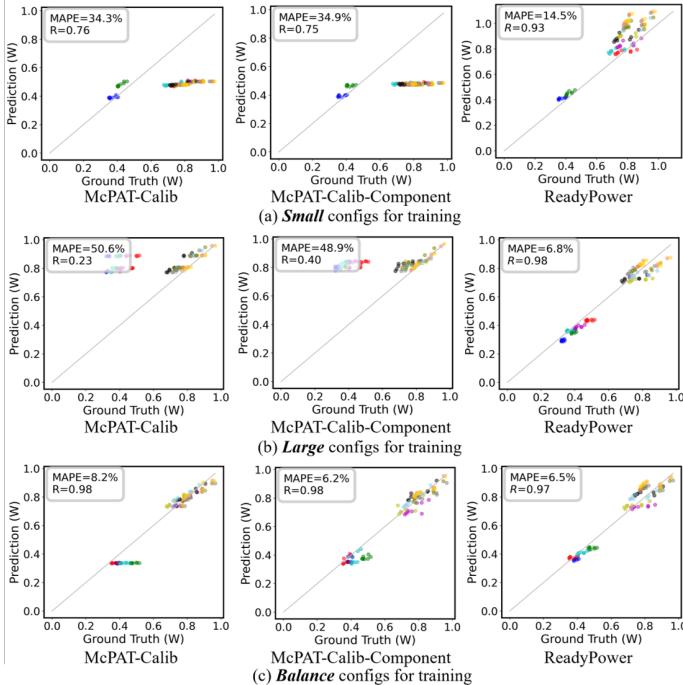


Fig. 4: Prediction visualization on BOOM CPU. It shows that ReadyPower can achieve high accuracy in ALL training scenarios while ML-based methods are inaccurate in *Small* and *Large* training scenarios on BOOM.

scenarios, ReadyPower can achieve the lowest MAPE (mean absolute percentage error) of 9.26% and 14.51%, and the highest correlation coefficient  $R$  of 0.96 and 0.91 on BOOM and XiangShan.

In detail, as shown in the figure, compared with the representative analytical method, the original McPAT and the enhanced version, McPAT-Plus, ReadyPower can consistently achieve much higher accuracy on both architectures, with a 16.49% and 11.99% lower MAPE and 0.16 and 0.11 higher correlation  $R$ . It demonstrates that the introduced new parameters and decisions in ReadyPower can improve the accuracy of the conventional analytical model, McPAT. Compared with the representative ML-based method, ReadyPower can surpass the McPAT-Calib and even McPAT-Calib-Component, with a 20.76% and 29.10% lower MAPE, and 0.25 and 0.24 higher correlation  $R$  on the two architectures. Such a superior accuracy over ML-based methods shows that ReadyPower is more reliable than the ML-based models under different training data distributions.

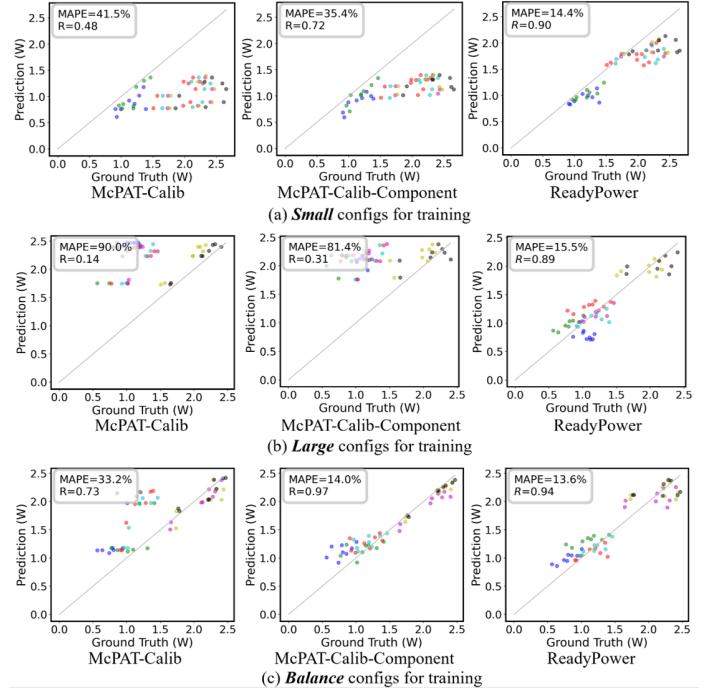


Fig. 5: Prediction visualization on XiangShan CPU. It shows ReadyPower can achieve high accuracy in ALL training scenarios while ML-based methods are inaccurate in *Small* and *Large* scenarios on XiangShan.

Fig. 4 and Fig. 5 provide more detailed prediction comparisons between ReadyPower and our baseline methods on BOOM and XiangShan CPUs, respectively. The detailed comparisons further demonstrate the unreliability of ML-based methods and the reliability of ReadyPower. Each point in the figure represents a configuration running a workload. Points with the same color are workloads on the same configuration. The gray line means the accurate prediction.

As shown in Fig. 4(a)(b) and Fig. 5(a)(b), ML-based methods, both McPAT-Calib and McPAT-Calib-Component, are significantly inaccurate in *Small* and *Large* training scenarios, in comparison with their accurate predictions in the *Balance* training scenario. In the (a) *Small* training scenario, as we expected, ML-based methods tend to underestimate the power consumption on testing data. This is because the model is only exposed to designs with lower power during training. In the (b) *Large* training scenario, for similar reasons, ML-based methods exhibit overestimation on testing data. This validates the unreliability of ML-based methods, which rely on the similarity between the distribution of training and testing data. Because of the low accuracy in *Small* and *Large* training scenarios, the average accuracy of ML-based methods across these three training scenarios, shown in Fig. 3, is very low. In comparison, ReadyPower can achieve high accuracy for all three training scenarios with different training data distributions, including not only *Balance* but also challenging *Small* and *Large*, as shown in Fig. 4(a)(b)(c) and Fig. 5(a)(b)(c). This demonstrates the reliability of ReadyPower, which can consistently make accurate predictions and is not affected by the distribution gap between training and testing data.

As for the runtime, ReadyPower is very fast for both inference and training. The inference time of ReadyPower is within 15 seconds

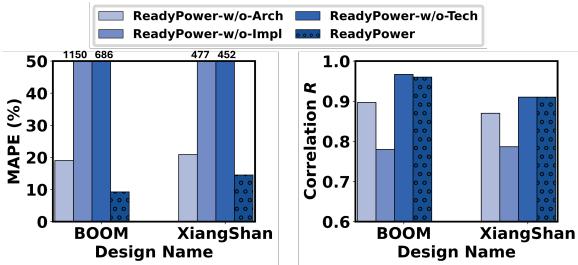


Fig. 6: Ablation studies of ReadyPower. We derive ablation studies, including ReadyPower-w/o-Arch, ReadyPower-w/o-Impl, and ReadyPower-w/o-Tech, for each level in ReadyPower, setting architecture, implementation, and technology-level parameters to default, respectively. Each bar is the average value across all training scenarios.

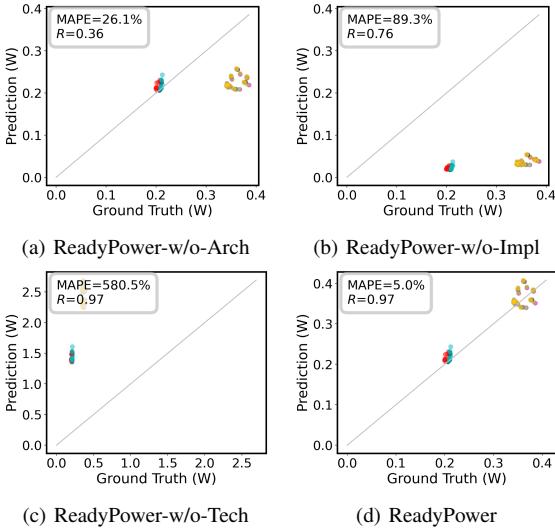


Fig. 7: Illustration of the predictions of ReadyPower and different ablation studies on BOOM branch predictor (BP) as an example.

on our server, which is a similar speed to the original McPAT. The training time is within 10 minutes. Notice that only one training process is required for each architecture, and then it can be used for different configurations and different workloads.

#### E. Ablation Study

Besides the four baselines discussed above, we also include three methods derived from ReadyPower for ablation studies: ReadyPower-w/o-Arch, ReadyPower-w/o-Impl, and ReadyPower-w/o-Tech, where the architecture-level, implementation-level, and technology-level parameters of ReadyPower are set to the default value in McPAT, respectively. Fig. 6 shows the comparison between three derived methods and ReadyPower, with each bar showing the average accuracy value across all training scenarios. It demonstrates that ReadyPower can consistently achieve the lowest MAPE and the highest correlation  $R$ , indicating that the introduced parameters at all levels are necessary for ReadyPower. Fig. 7 visualizes the prediction of three derived methods and ReadyPower for the branch predictor (BP), an important processor component, as an example to show the impact of parameters at each level more clearly.

The comparison between ReadyPower and ReadyPower-w/o-Arch validates the effect of the architecture-level parameters in capturing the microarchitecture design discrepancy. The MAPE and correlation gaps between ReadyPower-w/o-Arch and ReadyPower are mainly from the inaccurate prediction of BP and ICache. For the BP, by default, the McPAT regards the BP as an independent component, not depending on the parameters outside the BP. However, the table size of BP usually scales with the FetchWidth in the frontend. Therefore, the ReadyPower-w/o-Arch underestimates the configurations with large FetchWidth, as illustrated in Fig. 7(a).

The comparison between ReadyPower and ReadyPower-w/o-Impl proves the necessity of implementation-level parameters in capturing the RTL implementation discrepancy. The accuracy drop, including high MAPE and low correlation, of ignoring the implementation-level parameters is the most significant among the parameters of the three levels. The accuracy drop of ReadyPower-w/o-Impl is mainly

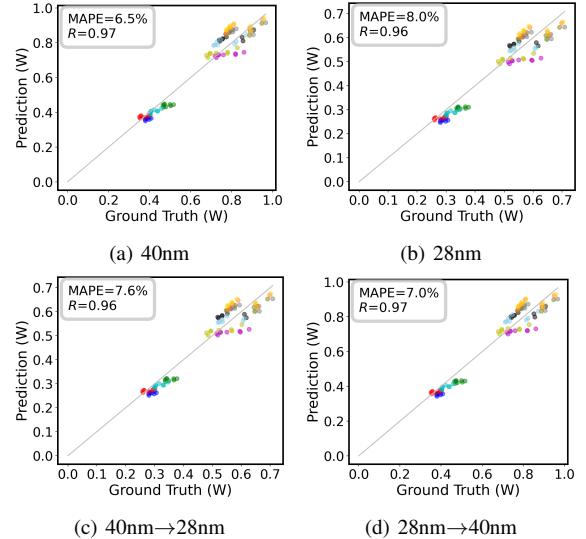


Fig. 8: The results of cross-technology-node transfer. (a)(b) Predictions in *Balance* training scenario on source technology node. (c)(d) Predictions in *Balance* training scenario on target technology node.

due to the inaccurate modeling of the logic scale and table size. Fig. 7(b) shows that the ReadyPower-w/o-Impl always significantly underestimates the power consumption of BP. It is because of the table size discrepancy of BP between the real processor and the modeled processor in McPAT, where BP is modeled as a simple fixed structure with a small table size.

The comparison between ReadyPower and ReadyPower-w/o-Tech emphasizes the effect of technology-level parameters in bridging the technology library discrepancy. ReadyPower-w/o-Tech can still retain a comparable correlation  $R$ , as shown in Fig. 6, but actually the MAPE drops dramatically. The reason is that the technology library discrepancy can globally affect each part of the processors. Fig. 7(c) shows the inaccuracy of BP power prediction incurred from the technology library discrepancy, which necessitates the introduction of technology-level parameters.

#### F. Cross-Technology-Node Transfer

A processor design can be implemented with different technology nodes. However, collecting power ground truth for each node requires substantial manpower and runtime overhead. To avoid this repeated cost, transferability across technology nodes is important.

We evaluate the cross-technology-node transferability of ReadyPower based on the BOOM CPUs implemented with TSMC 28nm and 40nm libraries. When transferring, we re-decide the technology-level parameters with the target technology library while the architecture-level and implementation-level parameters remain unchanged. We perform the transfer from 28nm (source) to 40nm (target) and from 40nm (source) to 28nm (target) with *Balance* training scenario, where *Small* and *Large* training scenarios have a similar trend. Fig. 8 shows the results, demonstrating the high transferability of ReadyPower.

## VI. CONCLUSION

In this work, we propose an architecture-level power model named ReadyPower. ReadyPower is ready-for-use by being reliable, interpretable, and handy. ReadyPower introduces architecture-level, implementation-level, and technology-level parameters into the widely adopted McPAT analytical model to bridge the discrepancies between the real processor and the modeled processor in McPAT. For each processor architecture, ReadyPower decides the parameters at each level differently. Such a ready-for-use framework has high reliability, which is a compelling addition to architects' toolbox.

#### ACKNOWLEDGEMENT

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