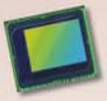
OmniVision



datasheet

PRODUCT SPECIFICATION

1/4" color CMOS QSXGA (5 megapixel) image sensor
with OmniBSI™ technology

OV5647

color CMOS QSXGA (5 megapixel) image sensor with OmniBSI™ technology

datasheet (COB)
PRODUCT SPECIFICATION

version 2.04
july 2011

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular phones
- toys
- PC multimedia
- digital still cameras

ordering information

- **OV05647-G04A** (color, chip probing, 200 µm backgrinding, reconstructed wafer)

features

- 1.4 µm x 1.4 µm pixel with OmniBSI technology for high performance (high sensitivity, low crosstalk, low noise)
- optical size of 1/4"
- automatic image control functions: automatic exposure control (AEC), automatic gain control (AGC), automatic white balance (AWB), automatic band filter (ABF), automatic 50/60 Hz luminance detection, and automatic black level calibration (ABLC)
- programmable controls for frame rate, AEC/AGC 16-zone size/position/weight control, mirror and flip, cropping, windowing, and panning
- image quality controls: lens correction, defective pixel canceling
- support for output formats: 8-/10-bit raw RGB data
- support for video or snapshot operations
- support for LED and flash strobe mode
- support for internal and external frame synchronization for frame exposure mode
- support for horizontal and vertical sub-sampling
- standard serial SCCB interface
- digital video port (DVP) parallel output interface
- MIPI interface (two lanes)
- 32 bytes of embedded one-time programmable (OTP) memory
- on-chip phase lock loop (PLL)
- embedded 1.5V regulator for core power
- programmable I/O drive capability, I/O tri-state configurability
- support for black sun cancellation

key specifications (typical)

- **active array size:** 2592 x 1944
- **power supply:**
  core: 1.5V ± 5% (with embedded 1.5V regulator)
  analog: 2.6 ~ 3.0V (2.8V typical)
  I/O: 1.7V ~ 3.0V
- **power requirements:**
  active: 96 mA
  standby: 20 µA
- **temperature range:**
  operating: -30°C to 70°C junction temperature (see **table 8-2**)
  stable image: 0°C to 50°C junction temperature (see **table 8-2**)
- **output formats:** 8-/10-bit RGB RAW output
- **lens size:** 1/4"
- **lens chief ray angle:** 24° (see **figure 10-2**)
- **input clock frequency:** 6~27 MHz
- **max S/N ratio:** 34 dB
- **dynamic range:** 67 dB @ 8x gain
- **maximum image transfer rate:**
  QSXGA (2592 x 1944): 15 fps
  1080p: 30 fps
  960p: 45 fps
  720p: 60 fps
  VGA (640 x 480): 90 fps
  QVGA (320 x 240): 120 fps
- **sensitivity:** 600mV/Lux-sec
- **shutter:** rolling shutter
- **maximum exposure interval:** 1968 x t_{ROW}
- **pixel size:** 1.4 µm x 1.4 µm
- **dark current:** 8 mV/s @ 50°C junction temperature
- **image area:** 3673.6 µm x 2738.4 µm
- **die dimensions:** 5520 µm x 4700 µm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pad numbers for the OV5647 image sensor. The die information is shown in section 9.

table 1-1 signal descriptions (sheet 1 of 3)

pad number	signal name	pad type	description	default status
01	AVDD	power	power for analog circuit, 2.8V	
02	AGND	ground	ground for analog circuit	
03	DOGND	ground	ground for digital I/O	
04	SCL	input	SCCB clock input	
05	SDA	I/O	SCCB data I/O	input
06	DVDD	power	power for digital core circuit, 1.5V (connect to ground via 0.1µF capacitor)	
07	SGND	ground	ground for pixel array	
08	GPIO1	I/O	general purpose I/O port 1	input
09	GPIO0	I/O	general purpose I/O port 2	input
10	STROBE	I/O	strobe	input
11	FREX	I/O	frame exposure control	input
12	DOVDD	power	power for digital I/O, 1.7 ~ 3.0V	
13	VREF2	reference	reference for analog circuit (connect to ground via 1µF capacitor)	
14	VREF1	reference	reference for analog circuit (connect to ground via 0.1µF capacitor)	
15	PWDN	input	power down control (active high with internal pull down resistor)	
16	DVDD	power	power for digital core circuit, 1.5V (connect to ground via 0.1µF capacitor)	
17	RESETB	input	hardware reset (active low with internal pull up resistor)	
18	AVDD	power	power for analog circuit, 2.8V	
19	AGND	ground	ground for analog circuit	
20	TM	input	test mode (active high with internal pull down resistor)	
21	DOGND	ground	ground for digital I/O	

table 1-1 signal descriptions (sheet 2 of 3)

pad number	signal name	pad type	description	default status
22	DVDD	power	power for digital core circuit, 1.5V (connect to ground via 0.1µF capacitor)	
23	DVDD	power	power for digital core circuit, 1.5V (connect to ground via 0.1µF capacitor)	
24	DOVDD	power	power for digital I/O, 1.7 ~ 3.0V	
25	DOGND	ground	ground for digital I/O	
26	AVDD	power	power for analog circuit, 2.8V	
27	HREF	I/O	DVP HREF output	input
28	PCLK	I/O	DVP PCLK output	input
29	VSYNC	I/O	DVP VSYNC output	input
30	DOVDD	power	power for digital I/O, 1.7 ~ 3.0V	
31	D0	I/O	DVP data bit 0	input
32	D1	I/O	DVP data bit 1	input
33	D2	I/O	DVP data bit 2	input
34	D3	I/O	DVP data bit 3	input
35	D9/MDN0	I/O	DVP data bit 9 / MIPI data lane0 negative output	input
36	D8/MDP0	I/O	DVP data bit 8 / MIPI data lane0 positive output	input
37	EVDD	power	power for MIPI circuit, 1.5V (connect to DVDD)	
38	D7/MCN	I/O	DVP data bit 7 / MIPI clock negative output	input
39	D6/MCP	I/O	DVP data bit 6 / MIPI clock positive output	input
40	EGND	ground	ground for MIPI TX circuit	
41	D5/MDN1	I/O	DVP data bit 5 / MIPI data lane1 negative output	input
42	D4/MDP1	I/O	DVP data bit 4 / MIPI data lane1 positive output	input
43	EGND	ground	ground for MIPI TX circuit	
44	PVDD	power	power for PLL circuit, 2.8V (connect to AVDD)	
45	XCLK	input	system input clock	
46	DOVDD	power	power for digital I/O, 1.7 ~ 3.0V	

table 1-1 signal descriptions (sheet 3 of 3)

pad number	signal name	pad type	description	default status
47	DVDD	power	power for digital core circuit, 1.5V (connect to ground via 0.1µF capacitor)	
48	DOGND	ground	ground for digital I/O	
49	AVDD	power	power for analog circuit, 2.8V	
50	AGND	ground	ground for analog circuit	

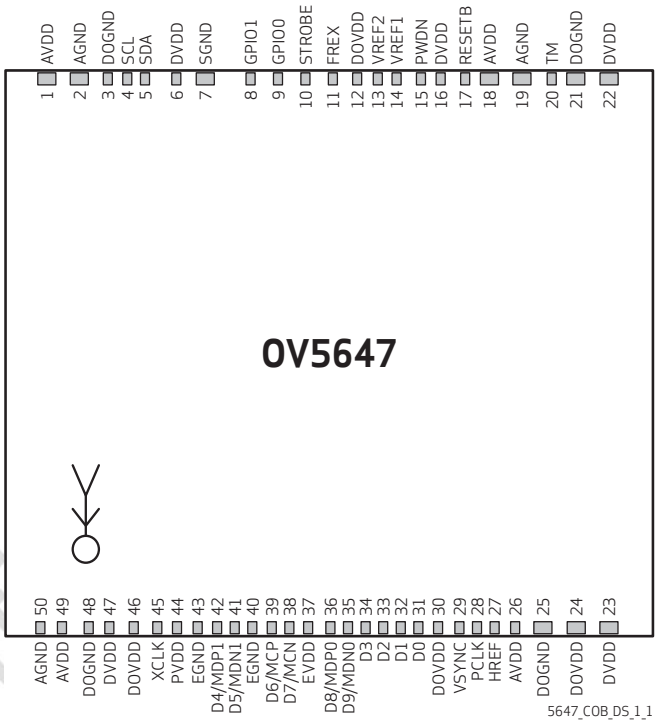
table 1-2 pad configuration under various conditions

signal	RESET[a]	RESET[b]	post-RESET	software sleep	hardware standby (power down pin = 1)
VSYNC	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
HREF	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
PCLK	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
D[9:0]	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
FREX	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
STROBE	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
GPIO0	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
GPIO1	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
XCLK	high-z	input	input	input	high-z
SDA	open drain	I/O	I/O	I/O	open drain
SCL	high-z	input	input	input	high-z

a. PWDN pin = 1 when chip power up

b. PWDN pin = 0 when chip power up

figure 1-1 pad diagram



2 system level description

2.1 overview

The OV5647 is a low voltage, high performance, 5 megapixel CMOS image sensor that provides 2592x1944 video output using OmniBSI™ technology. It provides multiple resolution raw images via the control of the serial camera control bus or MIPI interface.

The OV5647 has an image array capable of operating up to 15 fps in 2592x1944 resolution with user control of image quality, data transfer, camera functions through the SCCB interface. The OV5647 uses innovative OmniBSI technology to improve the sensor performance without the physical and optical trade-off.

The OV5647 includes a one-time programmable (OTP) memory.

2.2 architecture

The OV5647 sensor core generates streaming pixel data at a constant frame rate, indicated by HREF and VSYNC. **figure 2-1** shows the functional block of the OV5647 image sensor. **figure 2-2** shows an example application of the OV5647 sensor.

figure 2-1 OV5647 block diagram

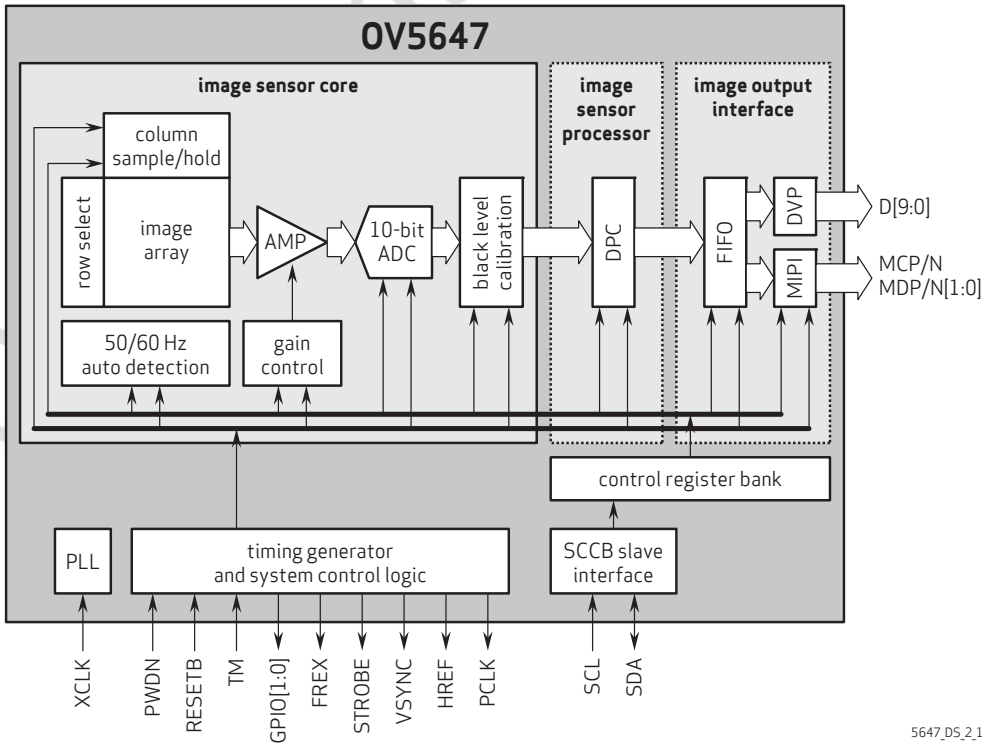
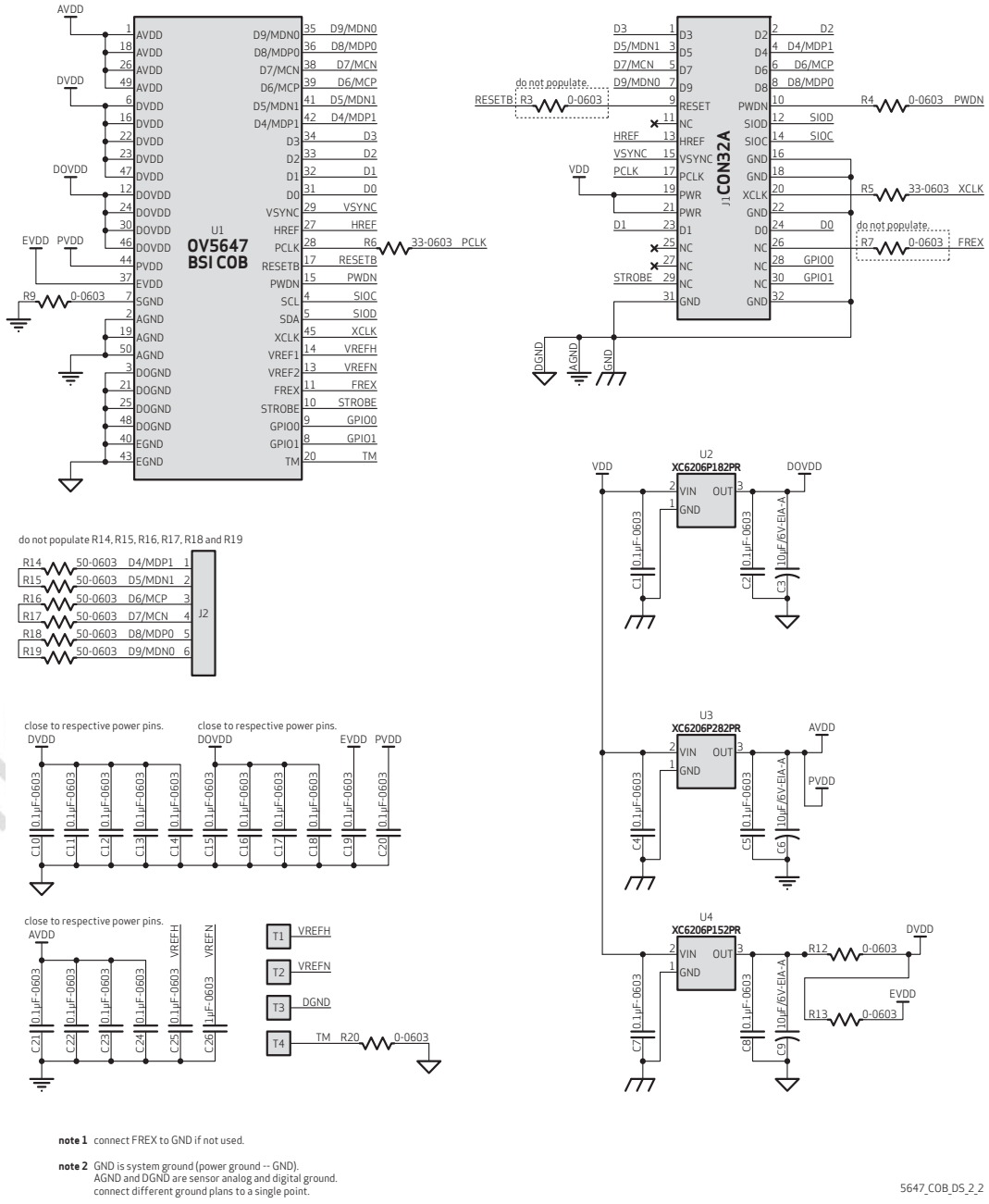


figure 2-2 reference design schematic



note 1 connect FREX to GND if not used.

note 2 GND is system ground (power ground -- GND).
AGND and DGND are sensor analog and digital ground.
connect different ground plans to a single point.

5647_COB_DS_2_2

2.3 format and frame rate

table 2-1 format and frame rate

format	resolution	frame rate	scaling method	pixel clock
5 Mpixel	2592x1944	15 fps	full resolution	96 MHz
1080p	1920x1080	30 fps	cropping	96 MHz
960p	1280x960	45 fps	cropping, subsampling/ binning	96 MHz
720p	1280x720	60 fps	cropping, subsampling/ binning	96 MHz
VGA	640x480	90 fps	cropping, subsampling/ binning	48 MHz
QVGA	320x240	120 fps	cropping, subsampling/ binning	24 MHz

2.4 I/O control

2.4.1 system clock control

The OV5647 has a on-chip PLL which generates a default 96 MHz clock from a 6~27 MHz input clock. A built-in programmable clock divider is used to generate different frame rate timing.

2.5 power up sequence

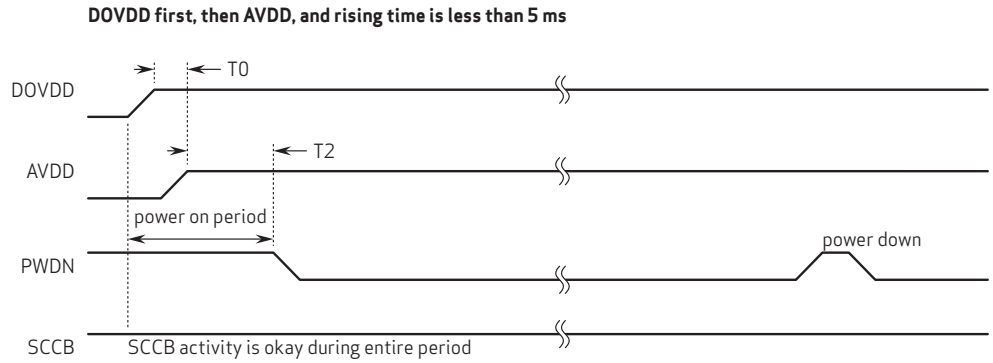
Based on the system power configuration (1.8V or 2.8V for I/O power), using external DVDD or internal DVDD, the power up sequence will differ. If 1.8V is used for I/O power, using the internal DVDD is preferred. If 2.8V is used for I/O power, due to a high voltage drop at the internal DVDD regulator, there is a potential heat issue. Hence, for a 2.8V power system, OmniVision recommends using an external DVDD source. Due to the higher power down current when using an external DVDD source, OmniVision strongly recommends cutting off all power supplies, including the external DVDD, when the sensor is not in use in the case of 2.8V I/O and external DVDD.

2.5.1 power up with internal DVDD

For powering up with the internal DVDD and SCCB access during the power ON period, the following conditions must occur:

1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
2. PWDN is active high with an asynchronized design (does not need clock)
3. PWDN must go high during the power up period
4. for PWDN to go low, power must first become stable (AVDD to PWDN ≥ 5 ms)
5. RESETB is active low with an asynchronized design
6. state of RESETB does not matter during power up period once DOVDD is up
7. master clock XCLK should provide at least 1 ms before host accesses sensor's registers
8. host can access SCCB bus (if shared) during entire period. 20 ms after PWDN goes low or 20 ms after RESETB goes high if reset is inserted after PWDN goes low, host can access sensor's registers to initialize sensor

figure 2-3 power up timing with internal DVDD



note T0 ≥ 0 ms: delay from DOVDD stable to AVDD stable
T2 ≥ 5 ms: delay from AVDD stable to sensor power up stable

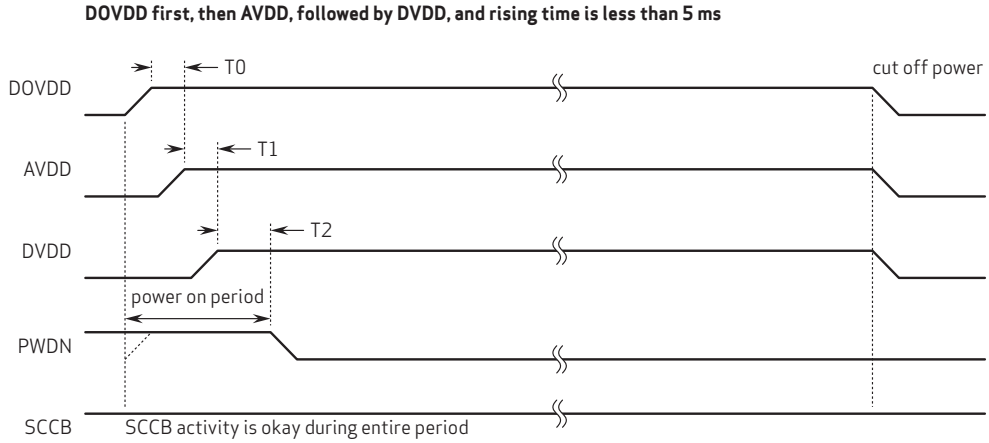
5647_DS_2_3

2.5.2 power up with external DVDD source

For powering up with an external DVDD source and SCCB access during the power ON period, the following conditions must occur:

1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
2. when AVDD and DVDD are turned ON, make sure AVDD becomes stable before DVDD becomes stable
3. PWDN is active high with an asynchronized design (does not need clock)
4. for PWDN to go low, power must first become stable (DVDD to PWDN ≥ 5 ms)
5. all powers are cut off when the camera is not in use (power down mode is not recommended
6. RESETB is active low with an asynchronized design
7. state of RESETB does not matter during power up period once DOVDD is up
8. master clock XVCLK should provide at least 1 ms before host accesses sensor's registers
9. host can access SCCB bus (if shared) during entire period. 20 ms after PWDN goes low or 20 ms after RESETB goes high if reset is inserted after PWDN goes high, host can access sensor's registers to initialize sensor

figure 2-4 power up timing with external DVDD source



note T0 ≥ 0 ms: delay from DOVDD stable to AVDD stable
T1 ≥ 0 ms: delay from AVDD stable to DVDD stable
T2 ≥ 5 ms: delay from DVDD stable to sensor power up stable

5647_DS_2_4

2.6 reset

Two reset modes are available for the OV5647:

- hardware reset
- SCCB software reset

The OV5647 sensor includes a RESETB pad that forces a complete hardware reset when it is pulled low (GND). The OV5647 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register 0x0103[0]to high.

The whole chip will be reset during power up. Manually applying a hard reset upon power up is recommended even though the on-chip power up reset is included. The hard reset is active low with an asynchronized design. The reset pulse width should be greater than or equal to 1 ms.

2.7 hardware and software standby

Two suspend modes are available for the OV5647:

- hardware standby
- software standby

To initiate hardware standby mode, the PWDN pad must be tied to high while in MIPI mode. Set register 0x3018[4:3] to 2'b11 before the PWDN pin is set to high. When this occurs, the OV5647 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software standby (0x0100[0]) through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in both modes.

2.8 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

2.8.1 data transfer protocol

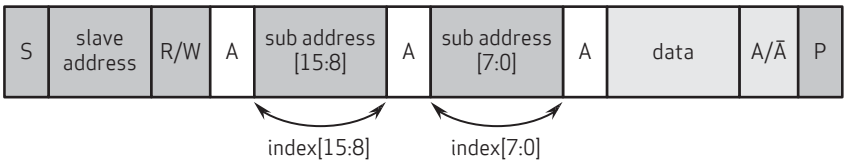
The data transfer of the OV5647 follows the SCCB protocol.

2.8.2 message format

The OV5647 supports the message format shown in **figure 2-5**. The 7-bit address of the OV5647 is 0x36 by default but can be programmed using register 0x3002[7:1]. The repeated START (Sr) condition is not shown in **figure 2-6**, but is shown in **figure 2-7** and **figure 2-8**.

figure 2-5 message type

message type: 16-bit sub-address, 8-bit data, and 7-bit slave address



	from slave to master	S	START condition	A	acknowledge
	from master to slave	P	STOP condition	Ā	negative acknowledge
	direction depends on operation	Sr	repeated START condition		

5647_DS_2_5

2.8.3 read / write operation

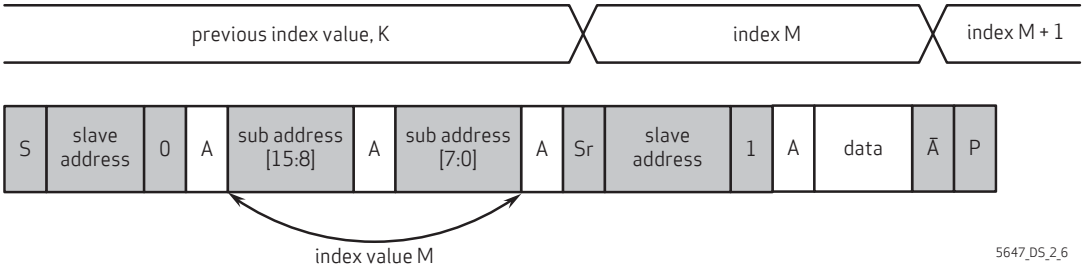
The OV5647 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

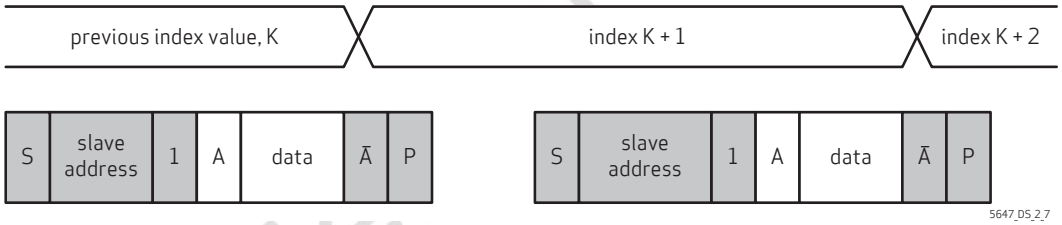
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 2-6**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-6 SCCB single read from random location



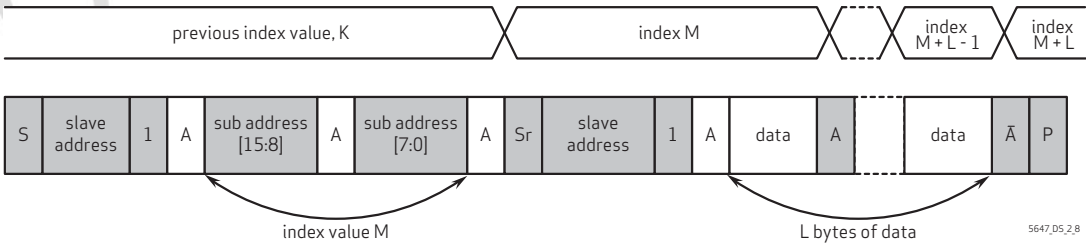
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 2-7**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-7 SCCB single read from current location



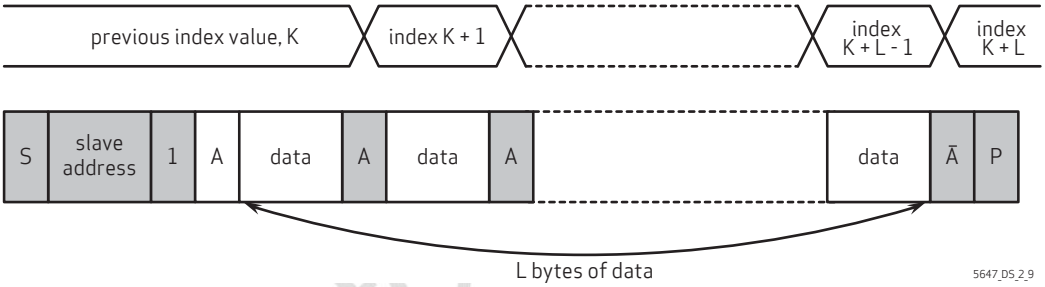
The sequential read from a random location is illustrated in **figure 2-8**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 2-8 SCCB sequential read from random location



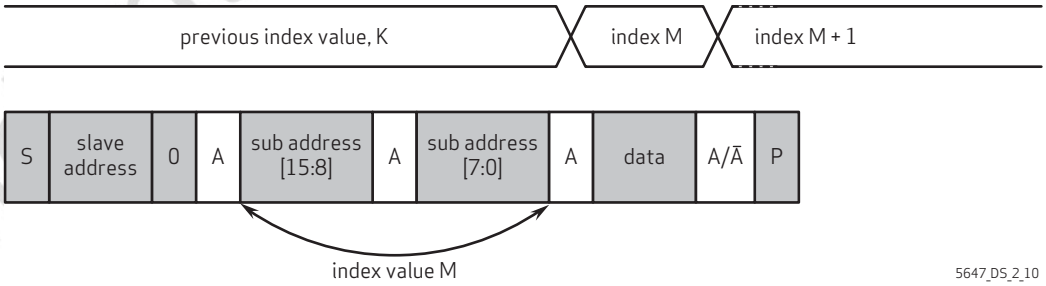
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation. as shown in **figure 2-9**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-9 SCCB sequential read from current location



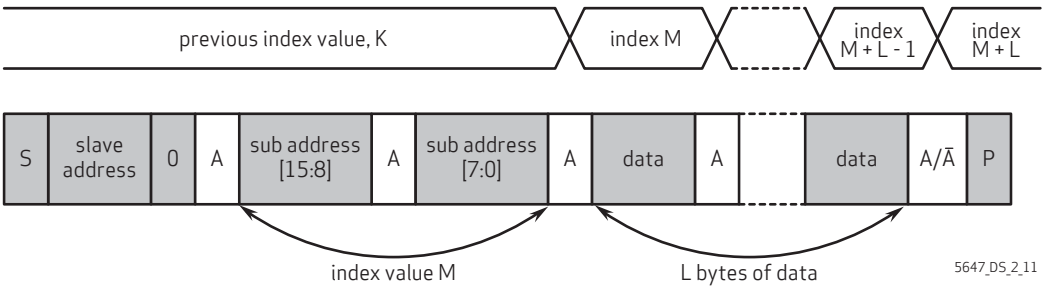
The write operation to a random location is illustrated in **figure 2-10**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 2-10 SCCB single write to random location



The sequential write is illustrated in **figure 2-11**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 2-11 SCCB sequential write to random location



2.8.4 SCCB timing

figure 2-12 SCCB interface timing

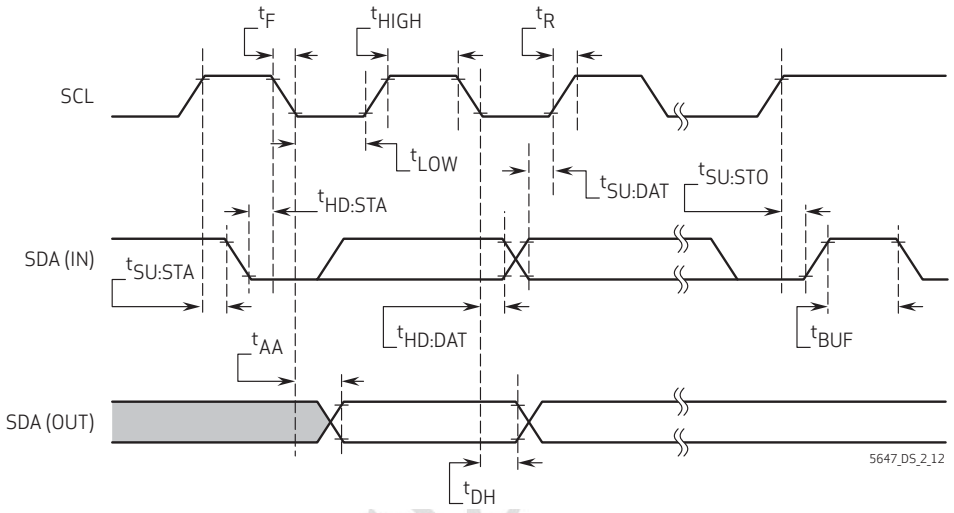


table 2-2 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency			400	KHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SCL low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400KHz mode

b. timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 10%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 90%

2.8.5 group write

Group write is supported in order to update a group of registers in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary.

The OV5647 supports up to four groups. These groups share 512 B RAM and the size of each group is programmable by adjusting the start address.

table 2-3 SCCB interface register

address	register name	default value	R/W	description
0x3104	SCCB_PLL	0x20	RW	Bit[6]: sda_vblank Bit[5]: r_sys_sel (sclk) 0: pll2_daclk 1: pll1_sclk Bit[4]: r_dac_sel (sen_clk) 0: pll2_daclk 1: pll1_sclk Bit[3]: r_daclk (dacclk) 0: pll2_daclk 1: pll1_sclk Bit[2:0]: Debug mode

table 2-4 group hold registers

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Group Access Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch others: Reserved Bit[3:0]: group_id 0000: Group bank 0, default start from address 0x00 0001: Group bank 1, default start from address 0x40 0010: Group bank 2, default start from address 0x80 0011: Group bank 3, default start from address 0xB0 others: Reserved
0x3209	GRP0_PERIOD	0x00	RW	Frames For Staying in Group 0
0x320A	GRP1_PERIOD	0x00	RW	Frames For Staying in Group 1
0x320B	GRP_SWCTRL	0x01	RW	Bit[3]: group_switch_repeat Bit[2]: context_en Bit[1:0]: Second group selection

3 block level description

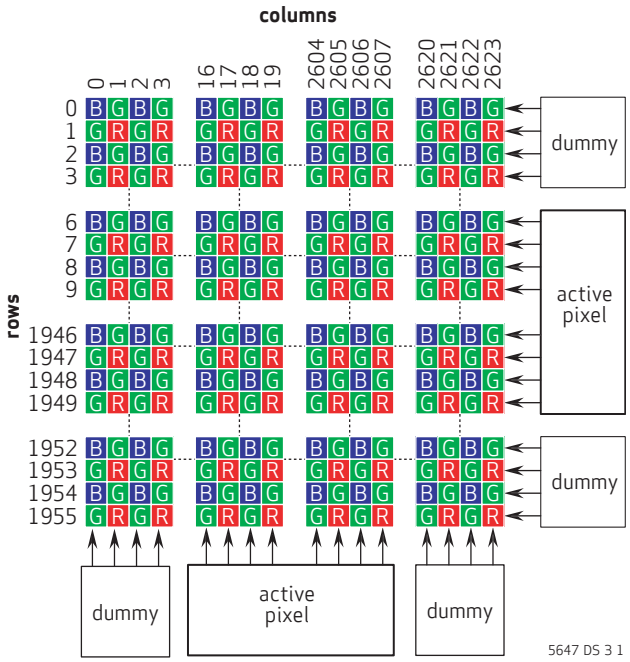
3.1 pixel array structure

The OV5647 sensor has an image array of 2624 columns by 1956 rows (5,132,544 pixels). figure 3-1 shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 5,132,544 pixels, 5,038,848 (2592x1944) are active pixels and can be output. The other pixels are used for black level calibration and interpolation. The center 2592x1944 is suggested to be output from the whole active pixel array. The backend processor can use the boundary pixels for additional processing.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



3.2 binning

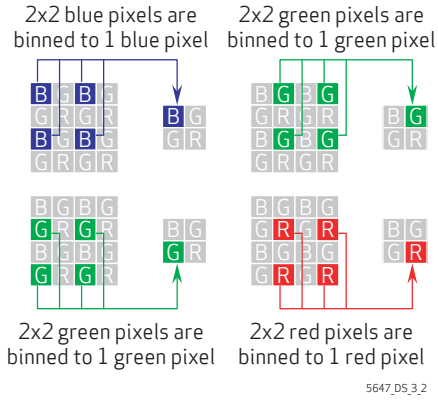
The OV5647 supports 2x2 binning for better SNR in low light conditions. See **table 3-1** for horizontal and vertical binning registers.

table 3-1 horizontal and vertical binning registers

address	register name	default value	R/W	description
0x3820	TIMING_TC_REG20	0x40	RW	Bit[0]: Vertical binning 0: Disable 1: Enable
0x3821	TIMING_TC_REG21	0x00	RW	Bit[0]: Horizontal binning 0: Disable 1: Enable

Sensor timing adjustment is necessary after applying binning. Please consult your local OmniVision FAE for details.

figure 3-2 example of 2x2 binning



3.3 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

3.4 10-bit A/D converters

The balanced signal is then digitized by the on-chip 10-bit ADC. The actual conversion rate is determined by the frame rate and resolution.

4 image sensor core digital functions

4.1 mirror and flip

The OV5647 provides mirror and flip read-out modes, which respectively reverse the sensor data read-out order horizontally and vertically (see **figure 4-1**). In flip mode, the OV5647 does not need additional settings because the ISP block will auto-detect whether the pixel is in the red line or blue line and make the necessary adjustments.

figure 4-1 mirror and flip samples

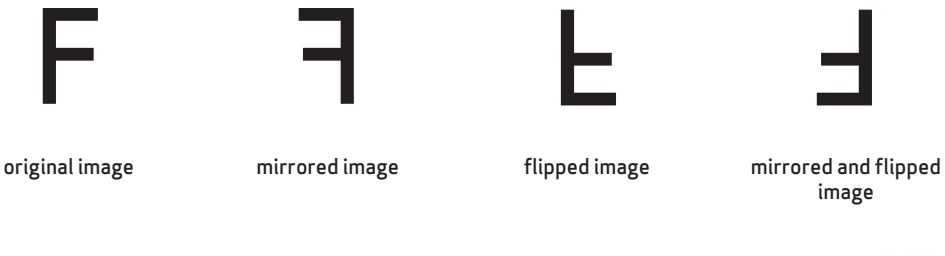


table 4-1 mirror flip control registers

address	register name	default value	R/W	description
0x3820	TIMING_TC_REG20	0x40	RW	Timing Control Bit[2]: ISP vertical flip Bit[1]: Sensor vertical flip
0x3821	TIMING_TC_REG21	0x00	RW	Timing Control Bit[2]: ISP mirror Bit[1]: Sensor mirror

4.2 image windowing

An image windowing area is defined by four parameters, x_addr_start, x_addr_end, y_addr_start, y_addr_end. By properly setting the parameters, any portion or size within the sensor array can be defined as an visible area. This windowing is achieved by simply masking the pixels outside the defined window; thus, it will not affect the original timing.

figure 4-2 image windowing

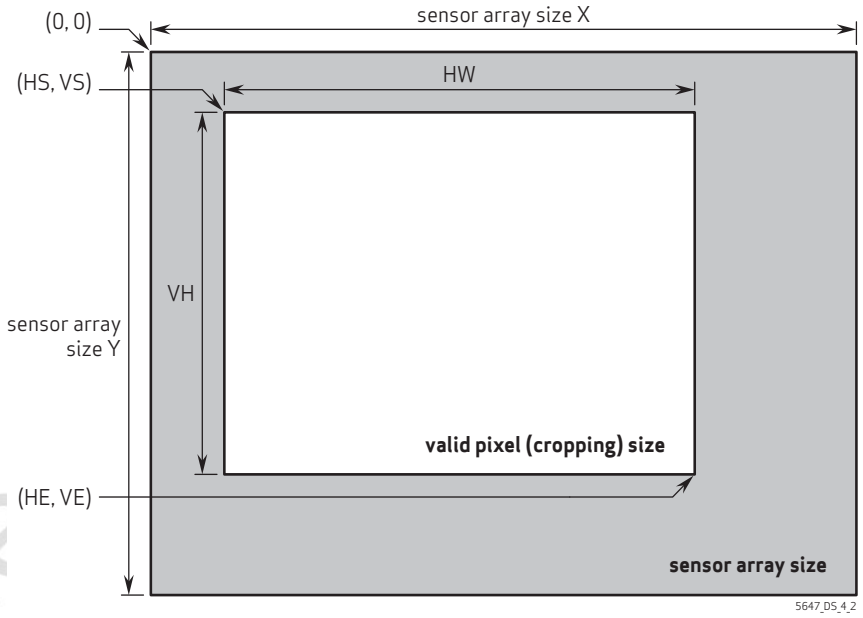


table 4-2 image windowing registers

address	register name	default value	R/W	description
0x3800	TIMING_X_ADDR_START	0x00	RW	Bit[3:0]: x_addr_start[11:8]
0x3801	TIMING_X_ADDR_START	0x0C	RW	Bit[7:0]: x_addr_start[7:0]
0x3802	TIMING_Y_ADDR_START	0x00	RW	Bit[3:0]: y_addr_start[11:8]
0x3803	TIMING_Y_ADDR_START	0x04	RW	Bit[7:0]: y_addr_start[7:0]
0x3804	TIMING_X_ADDR_END	0x0A	RW	Bit[3:0]: x_addr_end[11:8]
0x3805	TIMING_X_ADDR_END	0x33	RW	Bit[7:0]: x_addr_end[7:0]
0x3806	TIMING_Y_ADDR_END	0x07	RW	Bit[3:0]: y_addr_end[11:8]
0x3807	TIMING_Y_ADDR_END	0xA3	RW	Bit[7:0]: y_addr_end[7:0]

4.3 test pattern

For testing purposes, the OV5647 offers three types of test patterns, color bar, square and random data.The OV5647 also offers two effects: transparent effect and rolling bar effect. The output type of test pattern is controlled by register 0x503D[1:0] (test_pattern_type).

4.3.1 color bar

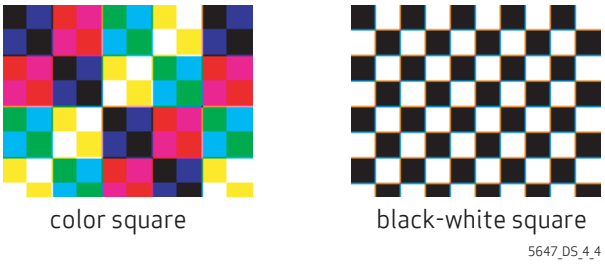
There are four types of color bars shown in **figure 4-3**. The output type of color the color bar can be selected by bar style register 0x503D[3:2].

figure 4-3 color bar types

4.3.2 square

There are two types of square patterns: color square and black-white square. Register 0x503D[4] (squ_bw) determines which type of square will be output.

figure 4-4 color, black and white square bars



4.3.3 random data

There are two types of random data test patterns: frame-changing and frame-fixed random data. The output type of random data is determined by register 0x503E[4] (rnd_same). The random seed is set by register 0x503E[3:0] (rnd_seed).

4.3.4 transparent effect

The transparent effect is enabled by register 0x503D[5] (transparent_mode). If this register is set, the transparent test pattern will be used. **figure 4-5** is an example which shows a transparent color bar image.

figure 4-5 transparent effect

5647_DS_4_5

4.3.5 rolling bar effect

The rolling bar is set by register 0x503D[6] (rolling_bar). If it is set, an inverted-color rolling bar will roll up and down. **figure 4-6** is an example which shows a rolling bar on a color bar image.

figure 4-6 rolling bar effect

5647_DS_4_6

table 4-3 test pattern registers

address	register name	default value	R/W	description
0x503D	ISP CTRL3D	0x00	RW	Bit[7]: test_pattern_en 0: Disable 1: Enable Bit[6]: rolling_bar 0: Disable rolling bar 1: Enable rolling bar Bit[5]: transparent_mode 0: Disable 1: Enable Bit[4]: squ_bw_mode 0: Output square is color square 1: Output square is black-white square Bit[3:2]: bar_style When set to different value, the different type color bar will be output Bit[1:0]: test_pattern_type 00: Color bar 01: Square 10: Random data 11: Input data
0x503E	ISP CTRL3E	0x00	RW	Bit[6]: win_cut_en Bit[5]: isp_test 0: Two lowest bits are 1 1: Two lowest bits are 0 Bit[4]: rnd_same 0: Frame changing random data pattern 1: Frame-fixed random data pattern Bit[3:0]: rnd_seed Initial seed for random data pattern

4.4 50/60Hz detection

When the integration time is not an integer multiple of the period of light intensity, the image will flicker. The function of the detector is to detect whether the sensor is under a 50 Hz or 60 Hz light source so that the basic step of integration time can be determined. Contact your local OmniVision FAE for auto detection settings.

table 4-4 50/60 Hz detection control registers

address	register name	default value	R/W	description
0x3C00	50/60 HZ DETECTION CTRL00	0x00	RW	Bit[5:3]: 50/60 Hz detection control Contact your local OmniVision FAE for the correct settings Bit[2]: band_def Band50 default value 0: 60 Hz as default value 1: 50 Hz as default value Bit[1:0]: 50/60 Hz detection control Contact your local OmniVision FAE for the correct settings
0x3C01	50/60 HZ DETECTION CTRL01	0x00	RW	Bit[7]: band_man_en Band detection manual mode 0: Manual mode disable 1: Manual mode enable Bit[6:0]: 50/60 Hz detection control Contact your local OmniVision FAE for the correct settings
0x3C02~ 0x3C0B	50/60 HZ DETECTION CTRL02	0x00	RW	Bit[7:0]: 50/60 Hz detection control Contact your local OmniVision FAE for the correct settings
0x3C0C	50/60 HZ DETECTION CTRL0C	–	R	Bit[0]: band50 0: Detection result is 60 Hz 1: Detection result is 50 Hz

4.5 AEC and AGC algorithms

4.5.1 overview

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allows the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control. The related registers are listed in **table 4-5**

table 4-5 AEC/AGC control function registers

address	register name	default value	R/W	description
0x3500	EXPOSURE	0x00	RW	Bit[3:0]: Exposure[19:16] Exposure in units of 1/16 line
0x3501	EXPOSURE	0x02	RW	Bit[7:0]: Exposure[15:8] Exposure in units of 1/16 line
0x3502	EXPOSURE	0x00	RW	Bit[7:0]: Exposure[7:0] Exposure in units of 1/16 line; lower four bits are a fraction of a line; they should be 0 since OV5647 does not support fraction line exposure
0x3503	MANUAL CTRL	0x00	RW	Bit[5:4]: Gain latch timing delay x0: Gain has no latch delay 01: Gain delay of 1 frame 11: Gain delay of 2 frames Bit[1]: AGC manual 0: Auto enable 1: Manual enable Bit[0]: AEC manual 0: Auto enable 1: Manual enable
0x350A	AGC	0x00	RW	Bit[1:0]: Gain[9:8] AGC real gain output high byte Gain = {0x350A[1:0], 0x350B[7:0]}/16
0x350B	AGC	0x10	RW	Bit[7:0]: Gain[7:0] AGC real gain output low byte

4.5.2 average-based algorithm

The average-based AEC controls image luminance using registers **WPT** (0x3A0F), **BPT** (0x3A10), **WPT2** (0x3A1B), and **BPT2** (0x3A1E). In average-based mode, the value of register **WPT** (0x3A0F) indicates the high threshold value for image change from unstable to stable state, and the value of register **BPT** (0x3A10) indicates the low threshold value for image change from unstable to stable state. The value of register **WPT2** (0x3A1B) indicates the high threshold value for image change from stable state to unstable state and the value of register **BPT2** (0x3A1E) indicates the low threshold value for image change from stable state to unstable state. When the target image luminance average value AVG (0x5693) is within the range specified by registers **WPT2** (0x3A1B) and **BPT2** (0x3A1E), the AEC keeps the image exposure and gain. When register AVG (0x5693) is greater than the value in register **WPT2** (0x3A1B), the AEC will decrease the image exposure and gain until it falls into the range of {0x3A10, 0x3A0F}. When register AVG (0x5693) is less than the value in register **BPT2** (0x3A1E), the AEC will increase the image exposure and gain until it falls into the range of {0x3A10, 0x3A0F}. Accordingly, the value in register **WPT** (0x3A0F) should be greater than the value in register **BPT** (0x3A10). The value of register **WPT2** should be no less than the value of register **WPT**(0x3A0F), and the value of register **BPT2** (0x3A1E) should be no greater than the value of **BPT** (0x3A10).

The AEC function supports both manual and auto speed selections in order to bring the image exposure into the range set by the values in registers **WPT** (0x3A0F) and **BPT** (0x3A10). For manual speed mode, the step is fixed and supports both normal and fast modes. Setting the AEC to normal mode will allow for the slowest step increment or decrement in image exposure to maintain the specified range. Setting the AEC to fast mode will provide for an approximate ten-step increment or decrement in image exposure to maintain the specified range. For auto speed mode, the step will automatically be adjusted according to the difference between the target and present values. The auto ratio of steps can be set by register bits AEC CTRL05[4:0](0x3A05).

Register HIGH VPT (0x3A11) and register LOW VPT (0x3A1F) controls the fast AEC range in manual speed mode. If the target image AVG (0x5693) is greater than HIGH VPT (0x3A11), AEC will decrease by half. If register AVG (0x5693) is less than LOW VPT (0x3A1F), AEC will double, as shown in **figure 4-7**. These registers have no effect in auto speed mode.

figure 4-7 desired convergence

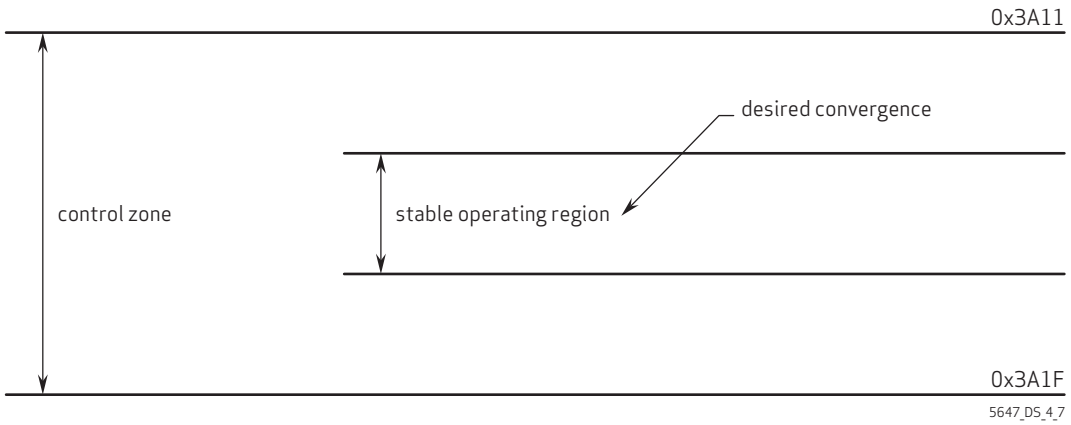


table 4-6 average based control function registers

address	register name	default value	R/W	description
0x3A0F	WPT	0x78	RW	Bit[7:0]: WPT Stable range high limit (from unstable state to stable state)
0x3A10	BPT	0x68	RW	Bit[7:0]: BPT Stable range low limit (from unstable state to stable state)
0x3A11	HIGH VPT	0xD0	RW	Bit[7:0]: vpt_high Fast zone high limit (when step ratio auto mode is disabled)
0x3A1B	WPT2	0x78	RW	Bit[7:0]: wpt2 Stable range high limit (from stable state to unstable state)
0x3A1E	BPT2	0x68	RW	Bit[7:0]: bpt2 Stable range low limit (from stable state to unstable state)
0x3A1F	LOW VPT	0x40	RW	Bit[7:0]: vpt_low Fast zone low limit (when step ratio auto mode is disabled)

For the average-based AEC/AGC algorithm, the measured window is horizontally and vertically adjustable and divided by sixteen (4x4) zones (see **figure 4-8**). Each zone (or block) is 1/16th of the image and has a 4-bit weight in calculating the average luminance (YAVG). The final YAVG is the weighted average of the sixteen zones. The 4-bit weight could be n/16 where n is from 0 to 15.

4.5.3 average luminance (YAVG)

Auto exposure time calculation is based on a frame brightness average value. By properly setting x_start, x_window, y_start, and y_window as shown in **figure 4-8**, a 4x4 grid average window is defined. It will automatically divide each zone into 4x4 zones. The average value is the weighted average of the 16 sections. **table 4-7** lists the corresponding registers.

figure 4-8 average-based window definition

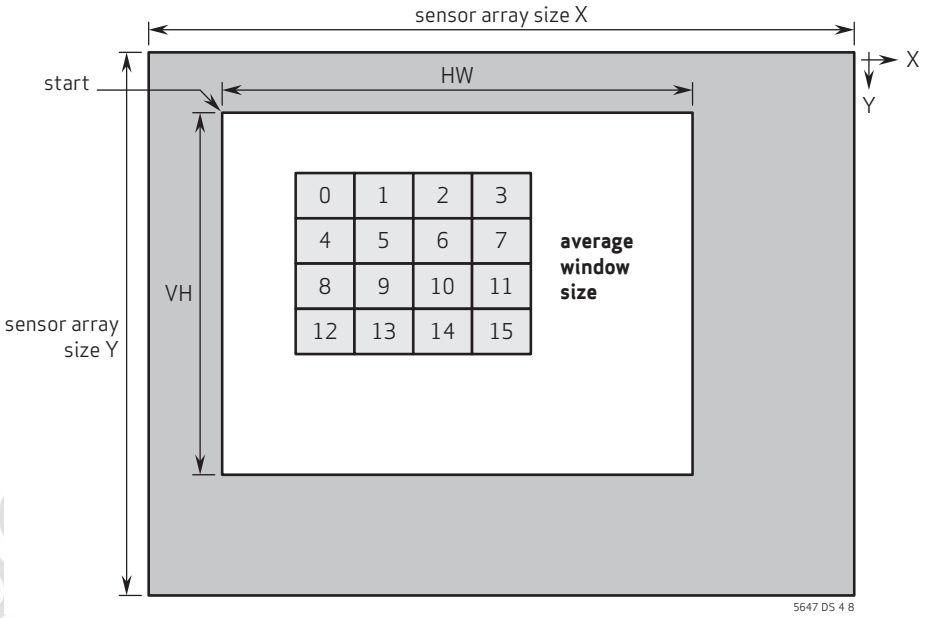


table 4-7 average luminance control function registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5680	XSTART	0x00	RW	Bit[3:0]: x_start[11:8] Horizontal start position for average window high byte
0x5681	XSTART	0x00	RW	Bit[7:0]: x_start[7:0] Horizontal start position for average window low byte
0x5682	YSTART	0x00	RW	Bit[3:0]: y_start[11:8] Vertical start position for average window high byte
0x5683	YSTART	0x00	RW	Bit[7:0]: y_start[7:0] Vertical start position for average window low byte

table 4-7 average luminance control function registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5684	X WINDOW	0x0A	RW	Bit[4:0]: x_window[12:8] Window X in manual average window mode high byte
0x5685	X WINDOW	0x20	RW	Bit[7:0]: x_window[7:0] Window X in manual average window mode low byte
0x5686	Y WINDOW	0x07	RW	Bit[3:0]: y_window[11:8] Window Y in manual average window mode high byte
0x5687	Y WINDOW	0x98	RW	Bit[7:0]: y_window[7:0] Window Y in manual average window mode low byte
0x5688	WEIGHT00	0x11	RW	Bit[7:4]: Window1 weight Bit[3:0]: Window0 weight
0x5689	WEIGHT01	0x11	RW	Bit[7:4]: Window3 weight Bit[3:0]: Window2 weight
0x568A	WEIGHT02	0x11	RW	Bit[7:4]: Window5 weight Bit[3:0]: Window4 weight
0x568B	WEIGHT03	0x11	RW	Bit[7:4]: Window7 weight Bit[3:0]: Window6 weight
0x568C	WEIGHT04	0x11	RW	Bit[7:4]: Window9 weight Bit[3:0]: Window8 weight
0x568D	WEIGHT05	0x11	RW	Bit[7:4]: Window11 weight Bit[3:0]: Window10 weight
0x568E	WEIGHT06	0x11	RW	Bit[7:4]: Window13 weight Bit[3:0]: Window12 weight
0x568F	WEIGHT07	0x11	RW	Bit[7:4]: Window15 weight Bit[3:0]: Window14 weight
0x5690	AVG CTRL10	0x02	RW	Bit[1]: avg_opt Bit[0]: avg_man 0: Auto average window 1: Manual average window
0x5693	AVG READOUT	–	R	Bit[7:0]: Avg value

4.6 AEC/AGC steps

The AEC and AGC work together to obtain adequate exposure/gain based on the current environmental illumination. In order to achieve the best signal-to-noise ratio (SNR), extending the exposure time is always preferred rather than raising the gain when the current illumination is getting brighter. Vice versa, under dark conditions, the action to decrease the gain is always taken prior to shortening the exposure time.

4.6.1 auto exposure control (AEC)

The function of the AEC is to calculate the necessary integration time of the next frame and send the information to the timing control block. Based on the statistics of previous frames, the AEC is able to determine whether the integration time should increase, decrease, fast increase, fast decrease, or remain the same.

To avoid image flickering under a periodic light source, the integration time can be adjusted in steps of integer multiples of the period of the light source. This new AEC step system is called the banding filter, suggesting that the exposure time is not continuous but falls in some steps.

4.6.2 night mode

The OV5647 supports long integration time larger than one frame in dark conditions. This is achieved by slowing down the original frame rate and waiting for exposure. Night mode ceiling can be set in register {0x3A14[15:8], 0x3A15[7:0]} and {0x3A02[15:8], 0x3A03[7:0]} for 50/60 Hz lighting, respectively. Night mode can be disabled by setting register bit 0x3A00[2]to 0. Also, when in night mode, the increase and decrease step can be based on either band or frames, depending on register 0x3A05[6]. The minimum increase/decrease step can be one band.

4.6.3 banding mode ON with AEC

In Banding ON mode, the exposure time will fall in steps of integer multiples of the period of light intensity. This design is to reject image flickering when the light source is not steady but periodical.

For a given light flickering frequency, the band step can be expressed in units of row period.

Band Step = period of light intensity × frame rate × rows per frame.

The band steps for 50Hz and 60Hz light sources can be set in registers {0x3A08[1:0], 0x3A09[7:0]} and {0x3A0A[1:0], 0x3A0B[7:0]}, respectively. Banding mode can be enabled by setting register 0x3A00[5].

4.6.4 banding mode OFF with AEC

When banding mode is OFF, integration time increases/decreases as normal. It is not necessarily multiples of band steps.

4.6.5 manual exposure control

To manually change exposure value, you must first set register 0x3503[0]to enable manual exposure control. The exposure value in registers 0x3500 ~ 0x3502 is in units of 1/16 line. The OV5647 only supports 0.n line exposure but does not support m.n line exposure, m is positive integer.

4.6.6 auto gain control (AGC)

Unlike prolonging integration time, increasing gain will amplify both signal and noise. Thus, AGC usually starts after AEC is full. However, in cases where adjacent AEC step changes are too large (>1/16), AGC steps should be inserted in between. Otherwise, the integration time will keep switching between two adjacent steps and the image flickers.

4.6.7 manual gain control

To manually change gain, first set register bit 0x3503[1]to enable manual control, then change the values in {0x350A[1:0], 0x350B[7:0]} for the manual gain.

Gain = {0x350A[1:0], 0x350B[7:0]} / 16

4.6.8 integration time between 1-16 rows

When integration time is less than 16 rows, the changes between adjacent AEC steps are larger than 1/16, which may possibly make the image oscillate between two AEC levels. Thus, some AGC steps are added in between.

4.6.9 gain insertion between AEC banding steps

When banding mode is ON, the integration time changes in step of the period of light intensity. For the first 16 band steps, since the exposure time change between adjacent steps is larger than 1/16, AGC steps are inserted to ensure image stability.

4.6.10 gain insertion between night mode steps

Between night mode steps (e.g., integration time = 1 frame and 2 frames), AGC steps are inserted to ensure no adjacent step change is larger than 1/16.

4.6.11 when AEC reaches maximum

When AEC reaches its maximum while the image is still too dark, the gain starts to increase until the new frame average falls into the stable range or AGC reaches its maximum. The AGC ceiling can be set in {0x3A18[9:8], 0x3A19[7:0]}.

Gain Ceiling = {0x3A18[1:0], 0x3A19[7:0]} / 16

table 4-8 AEC/AGC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3A00	AEC CTRL00	0x78	RW	Bit[5]: Band function Bit[2]: Night mode
0x3A02	MAX EXPO 60	0x3D	RW	Bit[7:0]: Max expo[15:8] Night mode ceiling of 60Hz
0x3A03	MAX EXPO 60	0x80	RW	Bit[7:0]: Max expo[7:0] Night mode ceiling of 60Hz
0x3A05	AEC CTRL05	0x30	RW	Bit[6]: frame_insert 0: In night mode, insert frame disable 1: In night mode, insert frame enable

table 4-8 AEC/AGC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3A08	B50 STEP	0x01	RW	Bit[1:0]: b50_step[9:8] Band step size of 50Hz
0x3A09	B50 STEP	0x27	RW	Bit[7:0]: b50_step[7:0] Band step size of 50Hz
0x3A0A	B60 STEP	0x00	RW	Bit[1:0]: b60_step[9:8] Band step size of 60Hz
0x3A0B	B60 STEP	0xF6	RW	Bit[7:0]: b60_step[7:0] Band step size of 60Hz
0x3A0D	B60 MAX	0x08	RW	Bit[5:0]: b60_max Max band step number of 60Hz
0x3A0E	B50 MAX	0x06	RW	Bit[5:0]: b50_max Max band step number of 50Hz
0x3A14	MAX EXPO 50	0x0E	RW	Bit[7:0]: max expo[15:8] Night mode ceiling of 50Hz
0x3A15	MAX EXPO 50	0x40	RW	Bit[7:0]: max expo[7:0] Night mode ceiling of 50Hz
0x3A17	NIGHT MODE GAIN BASE	0x01	RW	Bit[1:0]: gnight_thre Night mode gain threshold 00: 1x 01: 2x 10: 4x 11: 8x
0x3A18	AEC GAIN CEILING	0x00	RW	Bit[1:0]: gain_ceiling[9:8] Gain ceiling = {0x3A18[1:0], 0x3A19[7:0]} /16
0x3A19	AEC GAIN CEILING	0x7C	RW	Bit[7:0]: gain_ceiling[7:0]

4.7 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration. There are three main functions of the BLC:

- combining two ADC data paths into one data path
- adjusting all normal pixel values based on the values of the black levels
- applying multiplication to all pixel values based on digital gain

The target of BLC level can be set by register 0x4009.

table 4-9 BLC control functions

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x89	RW	BLC Control Bit[0]: BLC enable 0: Disable 1: Enable
0x4003	BLC CTRL03	0x08	RW	Bit[7]: blc_redo_en Writing 1 to this bit will trigger a BLC redo N frames begin Bit[6]: Freeze Bit[5:0]: manual_frame_num
0x4005	BLC CTRL05	0x18	RW	Bit[1]: blc_always_up_en 0: Normal freeze 1: BLC always update
0x4009	BLACK LEVEL TARGET	0x10	RW	Bit[7:0]: BLC black level target

4.8 strobe flash and frame exposure

4.8.1 strobe flash control

The strobe signal is programmable. It supports both LED and Xenon modes. The polarity of the pulse can be changed. The strobe signal is enabled (turned high/low depending on the pulse's polarity) by requesting the signal via the SCCB interface. Flash modules are triggered by the rising edge by default or by the falling edge if the signal polarity is changed. It supports the following flashlight modes (see **table 4-10**).

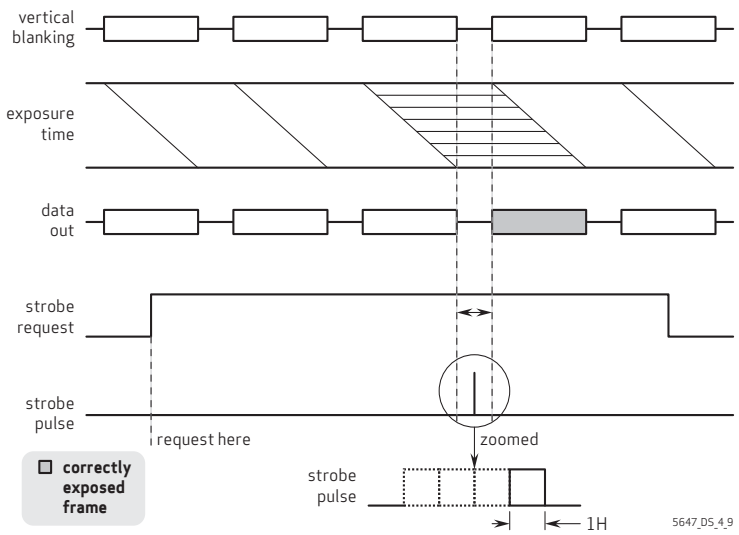
table 4-10 flashlight modes

mode	output	AEC / AGC	AWB
xenon	one-pulse	no	no
LED 1	pulse	no	no
LED 2	pulse	no	yes
LED 3	continuous	yes	yes

4.9 xenon flash control

After a strobe request is submitted, the strobe pulse will be activated at the beginning of the third frame (see **figure 4-9**). The third frame will be correctly exposed. The pulse width can be changed in Xenon mode between 1H and 4H, depending on register 0x3B00[3:2], where H is one row period.

figure 4-9 xenon flash mode



4.9.1 LED1 & 2 mode

Two frames after the strobe request is submitted, the third frame is correctly exposed. The strobe pulse will be activated only one time if the strobe end request is set correctly (see **figure 4-10**). If end request is not sent, the strobe signal is activated intermittently until the strobe end request is set (see **figure 4-11**). The number of skipped frames is programmable using registers {0x3A1C, 0x3A1D}.

figure 4-10 LED 1 & 2 mode - one pulse output

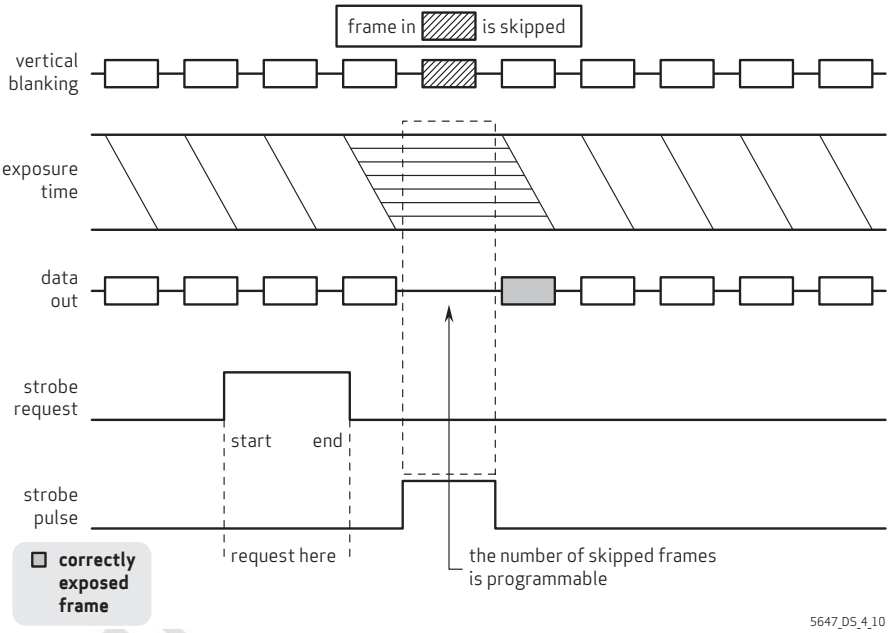
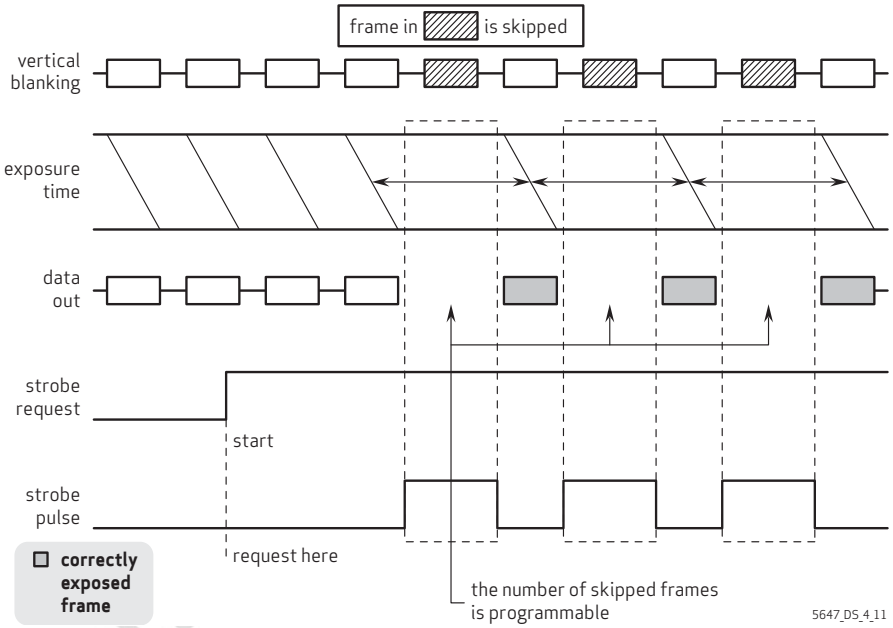


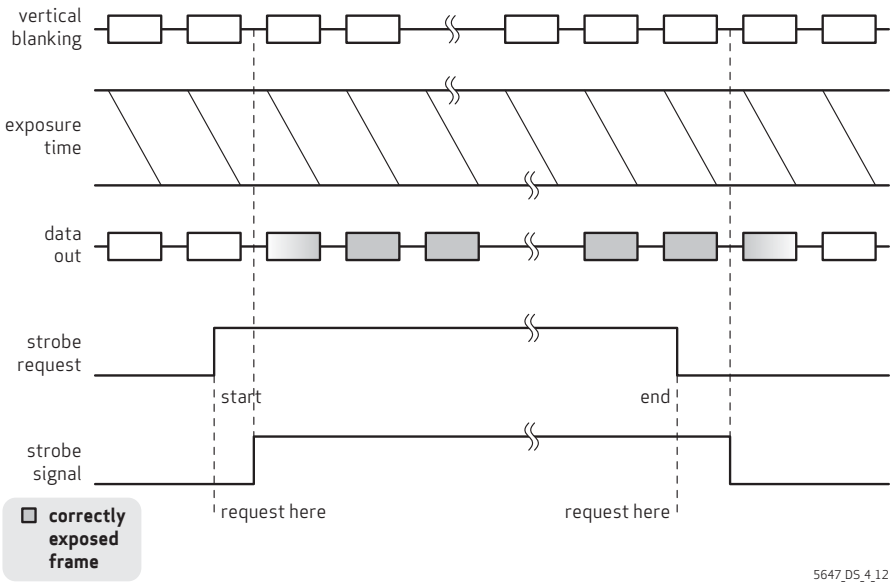
figure 4-11 LED 1 & 2 mode - multiple pulse output



4.9.2 LED 3 mode

In LED 3 mode, the strobe signal stays active until the strobe end request is sent (see figure 4-12).

figure 4-12 LED 3 mode

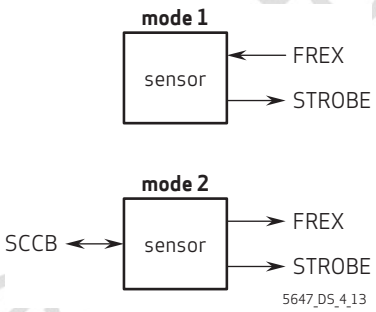


4.10 frame exposure (FREX) mode

4.10.1 FREX control

The OV5647 supports two modes of FREX (see **figure 4-13**). In FREX mode, whole frame pixels start integration at the same time, rather than integrating row by row. After the user-defined exposure time (either by external control in mode 1 or registers {0x3B01, 0x3B04, 0x3B05} in mode 2), the shutter closes, preventing further integration and the image begins to read out. After the readout finishes, the shutter opens again and the sensor resumes normal mode, waiting for the next FREX request. In mode 1, the FREX pin is configured as an input while it is configured as an output in mode 2. In both mode 1 and mode 2, the strobe output is irrelevant with the rolling strobe function. The strobe function of rolling shutter mode and FREX/shutter mode do not work at the same time.

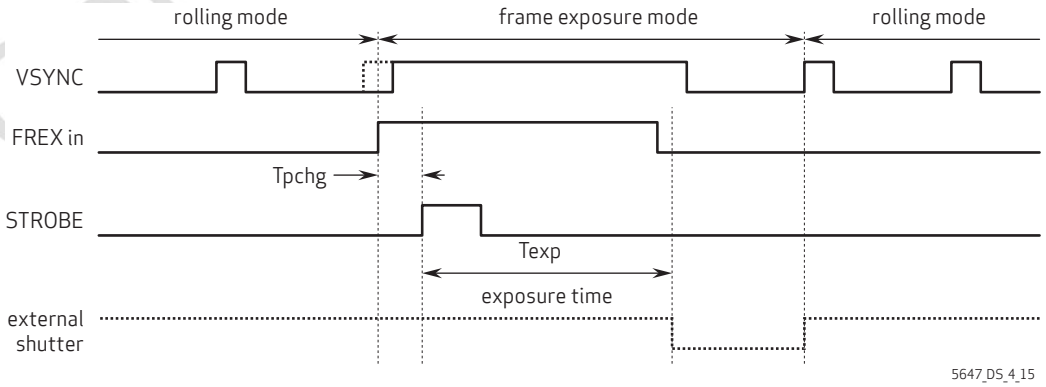
figure 4-13 FREX modes



note After frame exposure mode, the first output frame is invalid because of improper exposure during the readout time of the frame exposure image. From the second output frame, the images become normal.

Mode 1 (see **figure 4-14**) frame exposure and shutter control requests come from the external system via the FREX pin. The sensor will send a strobe output signal to control the flash light.

figure 4-14 FREX mode 1 timing diagram



Example setting:

6C 3002 EF; FREX mode selection: input

6C 3B06 14; STROBE width: fixed

6C 3B07 18; FREX mode 1 selection

6C 3B0A 24; STROBE output enable

6C 3011 00; enable FREX pin

Mode 2 (see **figure 4-15** and **figure 4-16**) frame exposure request comes from the external system via the I2C register 0x3B08[0]. The sensor outputs two signals, shutter control signal through the FREX pin and strobe signal through the STROBE pin. When the sensor is in FREX mode 2, by default the FREX output signal maintains a high status until the signal is triggered. After trigger the FREX pin outputs a low control signal. The polarity of the FREX output signal can be changed by setting 0x3B07[2]to 1'b1.

Frame exposure time is defined by {0x3B01[7:0], 0x3B04[7:0], 0x3B05[7:0]} with one step equal to 128tp/bit. If OV5647 works at 96MHz, each step is equal to 1.33µs and the minimum exposure time is 1.33µs with 0x3811 = 0x00, 0x3B04 = 0x00 and 0x3B05 = 0x01; the maximum exposure time is 22.37s with 0x3811 = 0xFF, 0x3B04 = 0xFF and 0x3B05 = 0xFF.

A shutter delay time is defined by {0x3B02[4:0], 0x3B03[7:0]} to compensate for the mechanical shutter delay. One step is equal to 128tp/bit. The minimum shutter delay time is 0 with 0x3B02 = 0x00 and 0x3B03 = 0x00. With PCLK = 96MHz, each step is equal to 1.33µs and the maximum shutter delay is 10.92ms with 0x3B02 = 0x1F and 0x3B03 = 0xFF.

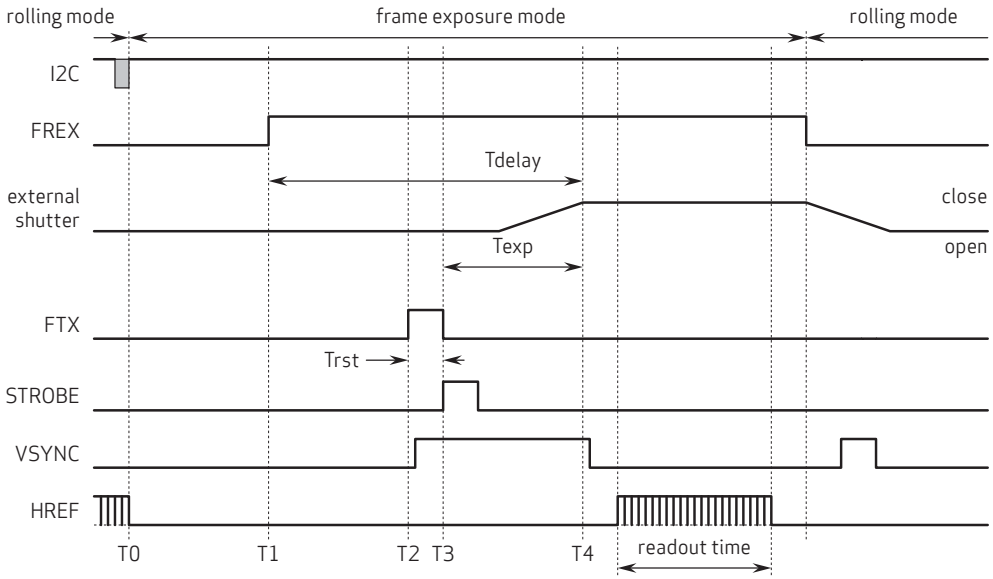
In **figure 4-15** and **figure 4-16** control of the relationship between shutter delay and the exposure time is realized by the following timing control. For FREXOUT signal, $T_4 - T_2 = T_{exp} + T_{pchg}$; For FTX signal, $T_4 - T_1 = T_{delay}$

table 4-11 FREX mode 2 timing point description

timing point	description
T_0	end of I2C request
T_1	beginning of FREX output
T_2	beginning of global reset
T_3	end of global reset (beginning of exposure)
T_4	external shutter close (end of exposure)

T_1 may be in front of or behind T_2 based on whether the T_{delay} is longer than $T_{pchg} + T_{exp}$ ($T_1 > T_2$ see **figure 4-15**) or T_{delay} is shorter than $T_{pchg} + T_{exp}$ ($T_1 < T_2$ see **figure 4-16**).

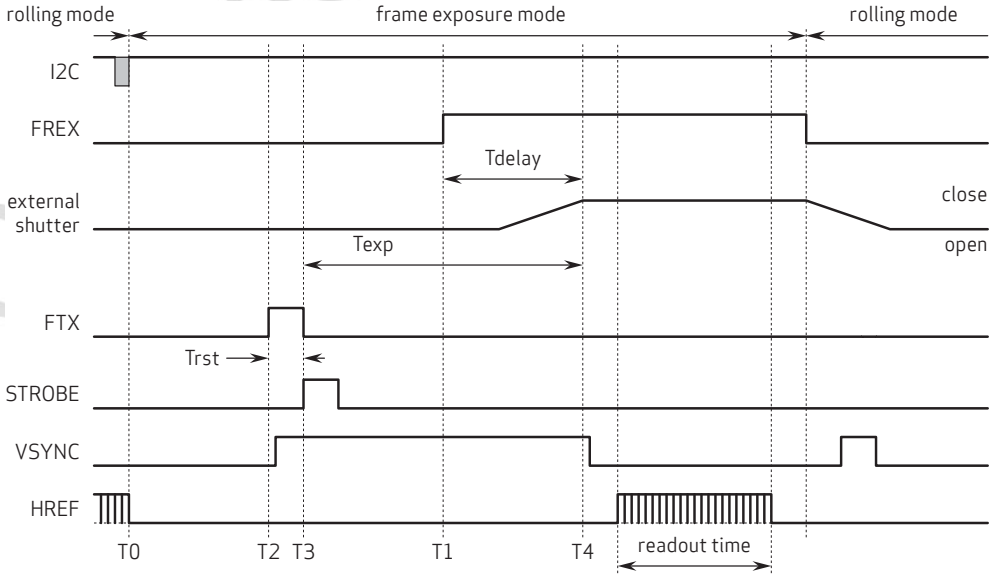
figure 4-15 FREX mode 2 timing diagram (when shutter delay is longer than exposure time)



note: Tdelay: shutter delay time
Texp: exposure time
Trst: global reset time

5647_DS_4_15

figure 4-16 FREX mode 2 timing diagram (when shutter delay is shorter than exposure time)



note: Tdelay: shutter delay time
Texp: exposure time
Trst: global reset time

5647_DS_4_16

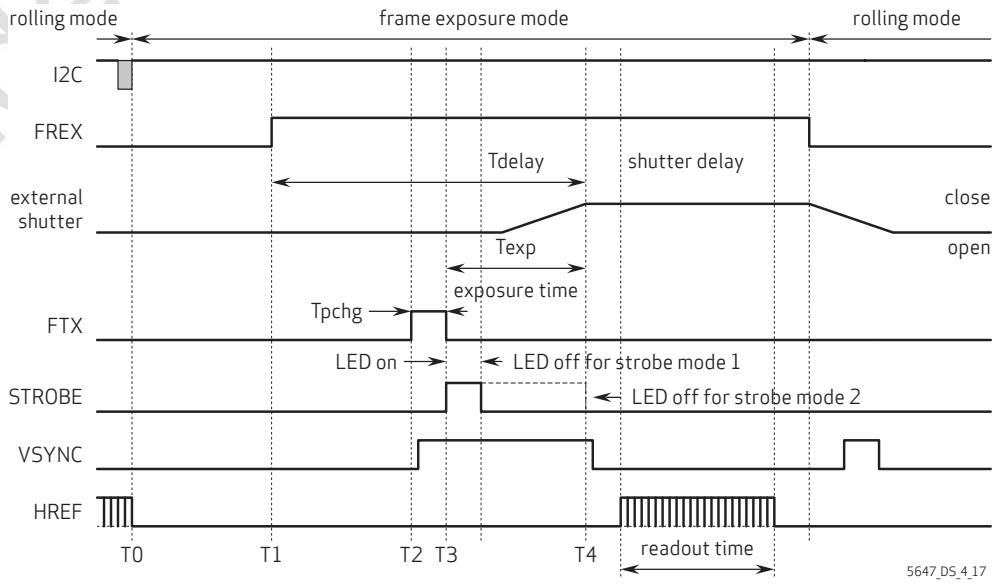
Example setting (see **figure 4-15**):

```
6C 3B06 14;
6C 3B07 1D;     FREX mode 2 selection and FREX polarity selection
6C 3002 FF;     FREX mode selection: output
6C 3B01 00;
6C 3B04 04;
6C 3B05 00;     with PCLK = 96MHz, exposure time = 1.37ms
6C 3B02 08;
6C 3B03 00;     with PCLK = 96MHz, shutter delay = 2.72ms
6C 3B08 01;     I2C FREX trigger
```

4.10.2 STROBE control in FREX mode

In FREX mode, two modes of STROBE control are provided in OV5647 (see **figure 4-17**). The first mode provides controllable STROBE output high signal (0x3B06[4]to 1'b0) from 1 to 16 tp (0x3B06[3:0]). The second mode provides STROBE output high signal (0x3B06[4]to 1'b1) during whole exposure period.

figure 4-17 STROBE control in FREX mode



4.11 FREX strobe flash control

See **table 4-12** for FREX strobe control functions.

table 4-12 FREX strobe control functions

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Strobe Control Bit[7]: Strobe request ON/OFF 0: OFF 1: ON Bit[6]: Strobe pulse reverse Bit[3:2]: width_in_xenon 00: 1 row period 01: 2 row period 10: 3 row period 11: 4 row period Bit[1:0]: Strobe mode 00: Xenon 01: LED 1 10: LED 2 11: LED 3
0x3B01	STROBE_FREX_EXP_H2	0x00	RW	Bit[7:0]: frex_exp[23:16]
0x3B02	STROBE_SHUTTER_DLY	0x08	RW	Bit[4:0]: shutter_dly[12:8]
0x3B03	STROBE_SHUTTER_DLY	0x00	RW	Bit[7:0]: shutter_dly[7:0]
0x3B04	STROBE_FREX_EXP_H	0x04	RW	Bit[7:0]: frex_exp[15:8]
0x3B05	STROBE_ FREX_EXP_L	0x00	RW	Bit[7:0]: frex_exp[7:0]
0x3B06	FREX CTRL	0x04	RW	FREX Control Bit[7:6]: frex_pchg_width Bit[5:4]: frex_strobe_option Bit[3:0]: frex_strobe_width[3:0]
0x3B07	STROBE_ FREX_MODE_SEL	0x08	RW	Bit[3]: fx1_fm_en Bit[2]: frex_inv Bit[1:0]: FREX mode select 00: frex_strobe mode1 01: frex_strobe mode2 1x: Rolling strobe
0x3B08	STROBE_FREX_EXP_REQ	0x00	RW	Bit[0]: frex_exp_req
0x3B09	FREX_SHUTTER_DELAY	0x00	RW	Bit[2:0]: frex end option
0x3B0A	STROBE_FREX_RST_ LENGTH	0x04	RW	Bit[2:0]: frex_rst_length[2:0]
0x3B0B	STROBE_WIDTH	0x00	RW	Bit[7:0]: frex_strobe_width[19:12]
0x3B0C	STROBE_WIDTH	0x3D	RW	Bit[7:0]: frex_strobe_width[11:4]

4.12 one-time programmable (OTP) memory

The OV5647 supports 256 bits of one-time programmable (OTP) memory to store chip identification and manufacturing information. It can be controlled through the SCCB (see **table 4-13**).

table 4-13 OTP control function registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3D00[a]	OTP_DATA_0	0x00	RW	OTP Buffer 0
0x3D01[a]	OTP_DATA_1	0x00	RW	OTP Buffer 1
0x3D02[a]	OTP_DATA_2	0x00	RW	OTP Buffer 2
0x3D03[a]	OTP_DATA_3	0x00	RW	OTP Buffer 3
0x3D04[a]	OTP_DATA_4	0x00	RW	OTP Buffer 4
0x3D05	OTP_DATA_5	0x00	RW	OTP Buffer 5
0x3D06	OTP_DATA_6	0x00	RW	OTP Buffer 6
0x3D07	OTP_DATA_7	0x00	RW	OTP Buffer 7
0x3D08	OTP_DATA_8	0x00	RW	OTP Buffer 8
0x3D09	OTP_DATA_9	0x00	RW	OTP Buffer 9
0x3D0A	OTP_DATA_A	0x00	RW	OTP Buffer A
0x3D0B	OTP_DATA_B	0x00	RW	OTP Buffer B
0x3D0C	OTP_DATA_C	0x00	RW	OTP Buffer C
0x3D0D	OTP_DATA_D	0x00	RW	OTP Buffer D
0x3D0E	OTP_DATA_E	0x00	RW	OTP Buffer E
0x3D0F	OTP_DATA_F	0x00	RW	OTP Buffer F
0x3D10	OTP_DATA_16	0x00	RW	OTP Buffer 10
0x3D11	OTP_DATA_17	0x00	RW	OTP Buffer 11
0x3D12	OTP_DATA_18	0x00	RW	OTP Buffer 12
0x3D13	OTP_DATA_19	0x00	RW	OTP Buffer 13
0x3D14	OTP_DATA_20	0x00	RW	OTP Buffer 14
0x3D15	OTP_DATA_21	0x00	RW	OTP Buffer 15
0x3D16	OTP_DATA_22	0x00	RW	OTP Buffer 16
0x3D17	OTP_DATA_23	0x00	RW	OTP Buffer 17

table 4-13 OTP control function registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D18	OTP_DATA_24	0x00	RW	OTP Buffer 18
0x3D19	OTP_DATA_25	0x00	RW	OTP Buffer 19
0x3D1A	OTP_DATA_26	0x00	RW	OTP Buffer 1A
0x3D1B	OTP_DATA_27	0x00	RW	OTP Buffer 1B
0x3D1C	OTP_DATA_28	0x00	RW	OTP Buffer 1C
0x3D1D	OTP_DATA_29	0x00	RW	OTP Buffer 1D
0x3D1E	OTP_DATA_30	0x00	RW	OTP Buffer 1E
0x3D1F	OTP_DATA_31	0x00	RW	OTP Buffer 1F
0x3D20[b]	OTP_PROGRAM_CTRL	0x00	RW	Bit[7]: OTP_wr_busy Bit[1]: OTP_program_speed 0: Fast 1: Slow Bit[0]: OTP_program_enable Changing from 0 to 1 initiates OTP programming
0x3D21	OTP_LOAD_CTRL	0x00	RW	Bit[7]: OTP_rd_busy Bit[1]: OTP speed 0: Fast 1: Slow Bit[0]: OTP_load_enable Changing from 0 to 1 initiates OTP read

a. 0x3D00~0x3D04 is reserved for OmniVision internal use.

b. AVDD must be 2.5V ± 5% when writing/programming OTP; otherwise, there will be reliability issues. There is no such limitation when reading OTP under normal operating conditions.

5 image sensor processor digital functions

5.1 ISP general controls

table 5-1 ISP general control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xFF	RW	ISP Control 00 (0: disable; 1: enable) Bit[7]: Lens shading correction Bit[2]: Black pixel correction Bit[1]: White pixel correction
0x5001	ISP CTRL01	0x01	RW	ISP Control 01 Bit[0]: AWB 0: Disable 1: Enable
0x5002	ISP CTRL02	0x41	RW	ISP Control 02 (0: disable; 1: enable) Bit[6]: win_en Bit[1]: otp_en Bit[0]: AWB gain
0x5003	ISP CTRL03	0x0A	RW	ISP Control 03 (0: disable; 1: enable) Bit[3]: buf_en Bit[2]: bin_man_set Bit[1]: bin_auto_en
0x5005	ISP CTRL05	0x14	RW	ISP Control 05 (0: disable; 1: enable) Bit[5]: awb_bias_on Bit[2]: lenc_bias_on
0x501F	ISP CTRL1F	0x03	RW	Bit[5]: enable_opt 0: Not latched by VSYNC 1: Enable latched by VSYNC Bit[4]: cal_sel 0: DPC cal_start using SOF 1: DPC cal_start using VSYNC Bit[2:0]: fmt_sel 011: ISP output data Others:ISP input data bypass
0x5025	ISP CTRL25	0x00	RW	Bit[1:0]: avg_sel 00: Inputs of AVG module are from LENC output 01: Inputs of AVG module are from AWB gain output 10: Inputs of AVG module are from DPC output 11: Inputs of AVG module are from binning output

table 5-1 ISP general control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x503D	ISP CTRL3D	0x00	RW	Bit[7]: test_pattern_en 0: Disable 1: Enable Bit[6]: rolling_bar 0: Disable rolling bar 1: Enable rolling bar Bit[5]: transparent_mode 0: Disable 1: Enable Bit[4]: squ_bw_mode 0: Output square is color square 1: Output square is black-white square Bit[3:2]: bar_style When set to a different value, a different type of color bar is output Bit[1:0]: test_pattern_type 00: Color bar 01: Square 10: Random data 11: Input data
0x503E	ISP CTRL3E	0x00	RW	Bit[6]: win_cut_en Bit[5]: isp_test 0: Two lowest bits are 1 1: Two lowest bits are 0 Bit[4]: rnd_same 0: Frame-changing random data pattern 1: Frame-fixed random data pattern Bit[3:0]: rnd_seed Initial seed for random data pattern
0x504B	ISP CTRL4B	0x30	RW	ISP Control (0: disable; 1: enable) Bit[5]: post_binning h_enable Bit[4]: post_binning v_enable Bit[3]: flip_man_en Bit[2]: flip_man Bit[1]: mirror_man_en Bit[0]: Mirror

5.2 lens correction (LENC)

The main purpose of the LENC is to compensate for lens fall off. According to the distance of each pixel to the lens center, the module calculates a gain for the pixel, correcting each pixel with its gain calculated. The LENC is also adaptive to the sensor gain.

table 5-2 LENC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x89	RW	Bit[7]: lenc_en 0: Disable 1: Enable
0x5800~ 0x5023	GMTRX	–	RW	Bit[5:0]: Green matrix
0x5824~ 0x503C	BRMTRX	–	RW	Bit[7:4]: Blue matrix Bit[3:0]: Red matrix
0x583D	LENC BR OFFSET	0x88	RW	Bit[7:4]: lenc_b_offset Bit[3:0]: lenc_r_offset
0x583E	MAX GAIN	0x40	RW	Bit[7:0]: max_gain
0x583F	MIN GAIN	0x20	RW	Bit[7:0]: min_gain
0x5840	MIN Q	0x18	RW	Bit[6:0]: min_q
0x5841	LENC CTRL59	0x0D	RW	Bit[3]: ADDBLC 0: Disable BLC add back function 1: Enable BLC add back function Bit[2]: blc_en 0: Disable BLC function 1: Enable BLC function Bit[1]: gain_man_en Bit[0]: autoq_en 0: Used constant Q (0x40) 1: Used calculated Q
0x5842	BR HSCALE	0x01	RW	Bit[3:0]: br_hscale[11:8] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block

table 5-2 LENC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5843	BR HSCALE	0x2B	RW	Bit[7:0]: br_hscale[7:0] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5844	BR VSCALE	0x01	RW	Bit[2:0]: br_vscale[10:8] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5845	BR VSCALE	0x8D	RW	Bit[7:0]: br_vscale[7:0] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5846	G HSCALE	0x01	RW	Bit[3:0]: g_hscale[11:8] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5847	G HSCALE	0x8F	RW	Bit[7:0]: g_hscale[7:0] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5848	G VSCALE	0x01	RW	Bit[2:0]: g_vscale[10:8] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5849	G VSCALE	0x09	RW	Bit[7:0]: g_vscale[7:0] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block

5.3 defect pixel cancellation (DPC)

Due to processes and other reasons, pixel defects in the sensor array will occur. Thus, these bad or wounded pixels will generate wrong color values. The main purpose of Defect Pixel Cancellation (DPC) function is to remove the effect caused by these bad or wounded pixels. Also, some special functions are available for those pixels located at the image boundary. To remove the defect pixel effect correctly, the proper threshold should first be determined.

table 5-3 defect pixel cancellation registers

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xFF	RW	Bit[2]: bc_en 0: Disable 1: Enable Bit[1]: wc_en 0: Disable 1: Enable

5.4 auto white balance (AWB)

The main function of Auto White Balance (AWB) is the process of removing unrealistic color casts so that objects which appear white in person in different color temperatures are rendered white in the image or video. It supports manual white balance and auto white balance. For auto white balance, simple AWB is supplied.

table 5-4 AWB control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x01	RW	Bit[0]: awb_en 0: Disable 1: Enable
0x5002	ISP CTRL02	0x41	RW	Bit[0]: AWB_gain_en 0: Disable 1: Enable

table 5-4 AWB control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5180	AWB CTRL	0x00	RW	Bit[6]: fast_awb 0: Disable fast AWB calculation function 1: Enable fast AWB calculation function Bit[5]: freeze_gain_en When it is enabled, the output AWB gains will be input AWB gains Bit[4]: freeze_sum_en When it is set, the sums and averages value will be same as previous frame Bit[3]: gain_man_en 0: Output calculated gains 1: Output manual gains set by registers Bit[2]: start_sel 0: Select the last HREF falling edge of before gain input as calculated start signal 1: Select the last HREF falling edge of after gain input as calculated start signal
0x5181	AWB DELTA	0x20	RW	Bit[7]: delta_opt Bit[6]: base_man_en Bit[5:0]: awb_delta Delta value to increase or decrease the gains
0x5182	STABLE RANGE	0x04	RW	Bit[7:0]: stable_range
0x5183	STABLE RANGEW	0x08	RW	Bit[7:0]: stable_rangew Wide stable range
0x5186	MANUAL RED GAIN MSB	0x04	RW	Bit[3:0]: red_gain_man[11:8]
0x5187	MANUAL RED GAIN LSB	0x00	RW	Bit[7:0]: red_gain_man[7:0]
0x5188	MANUAL GREEN GAIN MSB	0x04	RW	Bit[3:0]: grn_gain_man[11:8]
0x5189	MANUAL GREEN GAIN LSB	0x00	RW	Bit[7:0]: grn_gain_man[7:0]
0x518A	MANUAL BLUE GAIN MSB	0x04	RW	Bit[3:0]: blu_gain_man[11:8]
0x518B	MANUAL BLUE GAIN LSB	0x00	RW	Bit[7:0]: blu_gain_man[7:0]

table 5-4 AWB control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x518C	RED GAIN LIMIT	0xF0	RW	Bit[7:4]: red_gain_up_limit Bit[3:0]: red_gain_dn_limit They are only the highest 4 bits of limitation. Max red gain is {red_gan_up_limit,FF} Min red gain is {red_gain_dn_limit,00}
0x518D	GREEN GAIN LIMIT	0xF0	RW	Bit[7:4]: green_gain_up_limit Bit[3:0]: green_gain_dn_limit They are only the highest 4 bits of limitation. Max green gain is {green_gan_up_limit,FF} Min green gain is {green_gain_dn_limit,00}
0x518E	BLUE GAIN LIMIT	0xF0	RW	Bit[7:4]: blue_gain_up_limit Bit[3:0]: blue_gain_dn_limit They are only the highest 4 bits of limitation. Max blue gain is {blue_gan_up_limit,FF} Min blue gain is {blue_gain_dn_limit,00}

5.5 post binning filter

Sub-sample in raw domain will cause zigzag issues around slant edges and color shift because it is a non-uniform method in physical coordinate. Post binning filter will map these pixels to their physically correct location.

table 5-5 post binning control registers

address	register name	default value	R/W	description
0x5003	ISP CTRL3	0x0A	RW	Bit[2]: bin_en
0x504B	ISP CTRL75	0x30	RW	Bit[5]: h_en Bit[4]: v_en

6 image sensor output interface digital functions

6.1 system control

System control registers include clock, reset control, and PLL configure.

table 6-1 system control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3000	SC_CMMN_PAD_OEN0	0x00	RW	I/O Direction (0: input; 1: output) Bit[1:0]: D[9:8]
0x3001	SC_CMMN_PAD_OEN1	0x00	RW	I/O Direction (0: input; 1: output) Bit[7:0]: D[7:0]
0x3002	SC_CMMN_PAD_OEN2	0x00	RW	I/O Direction (0: input; 1: output) Bit[7]: VSYNC Bit[6]: HREF Bit[5]: PCLK Bit[4]: FREX Bit[3]: STROBE Bit[2]: SDA Bit[1]: GPIO1 Bit[0]: GPIO0
0x3006	SC_CMMN_PLL_CTR13	0x00	RW	Bit[5:2]: SDIV Clock divider for 50/60 Hz detection block
0x3008	SC_CMMN_PAD_OUT0	0x00	RW	I/O Output Value Bit[1:0]: D[9:8]
0x3009	SC_CMMN_PAD_OUT1	0x00	RW	I/O Output Value Bit[7:0]: D[7:0]
0x300A	SC_CMMN_CHIP_ID	0x56	R	Chip ID High Byte
0x300B	SC_CMMN_CHIP_ID	0x47	R	Chip ID Low Byte
0x300C	SC_CMMN_SCCB_ID	0x6C	RW	SCCB ID
0x300D	SC_CMMN_PAD_OUT2	0x00	RW	I/O Output Value Bit[7]: VSYNC Bit[6]: HREF Bit[5]: PCLK Bit[4]: FREX Bit[3]: STROBE Bit[2]: SDA Bit[1]: GPIO1 Bit[0]: GPIO0
0x300E	SC_CMMN_PAD_SEL0	0x00	RW	I/O Pad Select Bit[1:0]: D[9:8]

table 6-1 system control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x300F	SC_CMMN_PAD_SEL1	0x00	RW	I/O Pad Select Bit[7:0]: D[7:0]
0x3010	SC_CMMN_PAD_SEL2	0x00	RW	I/O Pad Select Bit[7]: VSYNC Bit[6]: HREF Bit[5]: PCLK Bit[4]: FREX Bit[3]: STROBE Bit[2]: SDA Bit[1]: GPIO1 Bit[0]: GPIO0
0x3011	SC_CMMN_PAD_PK	0x02	RW	Bit[7]: pd_dato_en Bit[6:5]: IO drive strength 00: 1x 01: 1x 10: 2x 11: 2x Bit[1]: FREX pad enable
0x3013	SC_CMMN_A_PWC_PK_O	0x00	RW	Bit[3]: bp_regulator 0: Enable internal regulator 1: Disable internal regulator
0x3014	SC_CMMN_A_PWC_PK_O	0x0B	RW	Bit[6:4]: apd[2:0] Bit[3:0]: dio
0x3016	SC_CMMN_MIPI_PHY	0x00	RW	Bit[7:6]: lph Bit[3]: mipi_pad_enable Bit[2]: pgm_bp_hs_en_lat Bypass the latch of hs_enable Bit[1:0]: ictl[1:0] Bias current adjustment
0x3017	SC_CMMN_MIPI_PHY	0x10	RW	Bit[7:6]: pgm_vcm[1:0] High speed common mode voltage Bit[5:4]: pgm_lptx[1:0] Driving strength of low speed transmitter 01 Bit[3]: ihalf Bias current reduction Bit[2]: pgm_vicd CD input low voltage Bit[1]: pgm_vih CD input high voltage-dummy Bit[0]: pgm_hs_valid Valid delay-dummy

table 6-1 system control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3018	SC_CMMN_MIPI_SC_CTRL	0x58	RW	Bit[7:5]: mipi_lane_mode 001: One lane mode 010: Two lane mode others: Not used Bit[4]: r_phy_pd_mipi 1: Power down PHY HS TX Bit[3]: r_phy_pd_lprx 1: Power down PHY LP RX module Bit[2]: mipi_en 0: DVP enable 1: MIPI enable Bit[1]: mipi_susp_reg MIPI system suspend register 1: Suspend Bit[0]: lane_dis_op 0: Use mipi_release1/2 and lane_disable1/2 to disable two data lane 1: Use lane_disable1/2 to disable two data lane
0x3019	SC_CMMN_MIPI_SC_CTRL	0x10	RW	Bit[7:0]: MIPI ULPS resume mark1 detect length
0x3021	SC_CMMN_MISC_CTRL	0x23	RW	Bit[5]: fst_stby_ctr 0: Software standby enter at v_blk 1: Software standby enter at l_blk Bit[4]: mipi_ctr_en 0: Disable the function 1: Enable MIPI remote reset and suspend control SC Bit[3]: mipi_rst_sel 0: MIPI remote reset all registers 1: MIPI remote reset all digital modules Bit[2]: gpio_pclk_en Bit[1]: frex_ef_sel Bit[0]: cen_global_o
0x3022	SC_CMMN_MIPI_SC_CTRL	0x00	RW	Bit[3]: lptx_ck_opt Bit[2]: pull_down_clk_lane Bit[1]: pull_down_data_lane2 Bit[0]: pull_down_data_lane1
0x302A	SC_CMMN_SUB_ID	0xB1	R	Bit[7:4]: Process Bit[3:0]: Version

table 6-1 system control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3034	SC_CMMN_PLL_ CTRL0	0x1A	RW	Bit[6:4]: pll_charge_pump Bit[3:0]: mipi_bit_mode 0000: 8 bit mode 0001: 10 bit mode
0x3035	SC_CMMN_PLL_ CTRL1	0x11	RW	Bit[7:4]: system_pll_div Bit[3:0]: scale_divider_mipi
0x3036	SC_CMMN_PLL_ MULTIPLIER	0x69	RW	Bit[7:0]: PLL_multiplier (4~252) This can be any integer during 4~127 and only even integer during 128~252
0x3037	SC_CMMN_PLL_ CTR13	0x03	RW	Bit[4]: pll_root_div 0: Bypass 1: /2 Bit[3:0]: pll_prediv 1, 2, 3, 4, 6, 8
0x3038	SC_CMMN_PLL_ DEBUG_OPT	0x00	RW	Bit[7]: pll_mult_debug_en Bit[1:0]: pll_mult1_debug
0x3039	SC_CMMN_PLL_ CTRL_R	0x00	RW	Bit[7]: pll_bypass
0x303A	SC_CMMN_PLLS_ CTRL0	0x00	RW	Bit[7]: plls_bypass
0x303B	SC_CMMN_PLLS_ CTRL1	0x19	RW	Bit[4:0]: plls_multiplier
0x303C	SC_CMMN_PLLS_ CTRL2	0x11	RW	Bit[6:4]: plls_cp Bit[3:0]: plls_sys_div
0x303D	SC_CMMN_PLLS_ CTRL3	0x30	RW	Bit[5:4]: plls_pre_div 00: /1 01: /1.5 10: /2 11: /3 Bit[2]: plls_div_r 0: /1 1: /2 Bit[1:0]: plls_seld5 00: /1 01: /1 10: /2 11: /2.5

6.2 SCCB

table 6-2 system control registers

address	register name	default value	R/W	description
0x300C	SC_CMMN_SCCB_ID	0x6C	RW	SCCB ID

6.3 group register write

The OV5647 supports group register write with up to four groups. Each group could have up to 16 registers.

Example settings:

6C 0x3208 0x00; Group 0 begin

6C 0x3503 0x03; register 1

6C 0x3501 0x7A; register 2

6C 0x3502 0xA0; register 3

6C 0x3208 0x10; Group 0 end

6C 0x3208 0xA0; write register group 0

table 6-3 group hold control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Group0 Start Address in SRAM, actual address is {0x3200[3:0], 4'h0}
0x3201	GROUP ADR1	0x04	RW	Group1 Start Address in SRAM, actual address is {0x3201[3:0], 4'h0}
0x3202	GROUP ADR2	0x08	RW	Group2 Start Address in SRAM, actual address is {0x3202[3:0], 4'h0}
0x3203	GROUP ADR3	0x0B	RW	Group3 Start Address in SRAM, actual address is {0x3203[3:0], 4'h0}
0x3204	GROUP LEN0	–	R	Length of Group0
0x3205	GROUP LEN1	–	R	Length of Group1
0x3206	GROUP LEN2	–	R	Length of Group2
0x3207	GROUP LEN3	–	R	Length of Group3

table 6-3 group hold control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Bit[7:4]: Group_ctrl 0000: Enter group write mode 0001: Exit group write mode 1010: Initiate group write Bit[3:0]: Group ID 0000: Group 0 0001: Group 1 0010: Group 2 0011: Group 3

6.4 timing control

table 6-4 timing control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	TIMING_X_ADDR_START	0x00	RW	Bit[3:0]: x_addr_start[11:8]
0x3801	TIMING_X_ADDR_START	0x0C	RW	Bit[7:0]: x_addr_start[7:0]
0x3802	TIMING_Y_ADDR_START	0x00	RW	Bit[3:0]: y_addr_start[11:8]
0x3803	TIMING_Y_ADDR_START	0x04	RW	Bit[7:0]: y_addr_start[7:0]
0x3804	TIMING_X_ADDR_END	0x0A	RW	Bit[3:0]: x_addr_end[11:8]
0x3805	TIMING_X_ADDR_END	0x33	RW	Bit[7:0]: x_addr_end[7:0]
0x3806	TIMING_Y_ADDR_END	0x07	RW	Bit[3:0]: y_addr_end[11:8]
0x3807	TIMING_Y_ADDR_END	0xA3	RW	Bit[7:0]: y_addr_end[7:0]
0x3808	TIMING_X_OUTPUT_SIZE	0x0A	RW	Bit[3:0]: DVP output horizontal width[11:8]
0x3809	TIMING_X_OUTPUT_SIZE	0x20	RW	Bit[7:0]: DVP output horizontal width[7:0]
0x380A	TIMING_Y_OUTPUT_SIZE	0x07	RW	Bit[3:0]: DVP output vertical height[11:8]
0x380B	TIMING_Y_OUTPUT_SIZE	0x98	RW	Bit[7:0]: DVP output vertical height[7:0]
0x380C	TIMING_HTS	0x0A	RW	Bit[4:0]: Total horizontal size[12:8]
0x380D	TIMING_HTS	0x8C	RW	Bit[7:0]: Total horizontal size[7:0]
0x380E	TIMING_VTS	0x07	RW	Bit[7:0]: Total vertical size[15:8]
0x380F	TIMING_VTS	0xB0	RW	Bit[7:0]: Total vertical size[7:0]
0x3810	TIMING_ISP_X_WIN	0x00	RW	Bit[3:0]: ISP horizontal offset[11:8]

table 6-4 timing control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3811	TIMING_ISP_X_WIN	0x04	RW	Bit[7:0]: ISP horizontal offset[7:0]
0x3812	TIMING_ISP_Y_WIN	0x00	RW	Bit[3:0]: ISP vertical offset[11:8]
0x3813	TIMING_ISP_Y_WIN	0x02	RW	Bit[7:0]: ISP vertical offset[7:0]
0x3814	TIMING_X_INC	0x11	RW	Bit[7:4]: h_odd_inc Horizontal subsample odd increase number Bit[3:0]: h_even_inc Horizontal subsample even increase number
0x3815	TIMING_Y_INC	0x11	RW	Bit[7:4]: v_odd_inc Vertical subsample odd increase number Bit[3:0]: v_even_inc Vertical subsample even increase number
0x3816	TIMING_HSYNCST	0x00	RW	Bit[3:0]: HSYNC start point[11:8]
0x3817	TIMING_HSYNCST	0x00	RW	Bit[7:0]: HSYNC start point[7:0]
0x3818	TIMING_HSYNCW	0x00	RW	Bit[3:0]: HSYNC window[11:8]
0x3819	TIMING_HSYNCW	0x00	RW	Bit[7:0]: HSYNC window[7:0]
0x3820	TIMING_TC_REG20	0x40	RW	Bit[2]: ISP vertical flip Bit[1]: Sensor vertical flip Bit[0]: Vertical binning
0x3821	TIMING_TC_REG21	0x00	RW	Bit[2]: ISP mirror Bit[1]: Sensor mirror Bit[0]: Horizontal binning

6.5 frame control (FC)

Frame control (FC) is used to mask some specified frame by setting the appropriate registers.

table 6-5 frame control registers

address	register name	default value	R/W	description
0x4200	FRAME CONTROL00	0x00	RW	Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: Frame counter reset
0x4201	FRAME CONTROL01	0x00	RW	Control Passed Frame Number Bit[3:0]: Frame ON number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode
0x4202	FRAME CONTROL02	0x00	RW	Control Masked Frame Number Bit[3:0]: Frame OFF number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode
0x4203	FRAME CONTROL03	0x00	RW	Bit[6]: rblue_mask_dis Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

6.6 digital video port (DVP)

The Digital Video Port (DVP) provides 10-bit parallel data output in all formats supported and extended features including compression mode, HSYNC mode, CCIR656 mode, and test pattern output.

table 6-6 DVP registers (sheet 1 of 2)

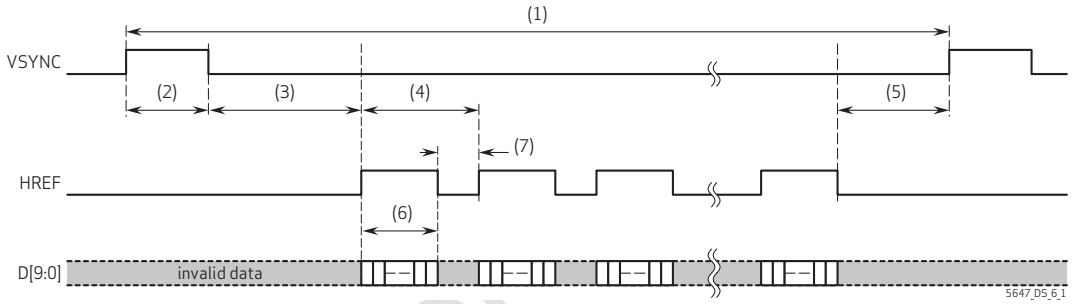
address	register name	default value	R/W	description
0x4700	DVP MODE SELECT	0x04	RW	Bit[3]: CCIR v select Bit[2]: CCIR f select Bit[1]: CCIR656 mode enable Bit[0]: HSYNC mode enable
0x4701	DVP VSYNC WIDTH CTRL	0x01	RW	VSYNC Width (in terms of number of lines)
0x4702	DVP_HSYVSY_NEG_WIDTH	0x01	RW	Bit[7:0]: VSYNC length[15:8] (in terms of pixel count)

table 6-6 DVP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4703	DVP_HSYVSY_NEG_WIDTH	0x00	RW	Bit[7:0]: VSYNC length[7:0] (in terms of pixel count)
0x4704	DVP VSYNC MODE	0x00	RW	Bit[3:2]: r_vsyncount_sel Bit[1]: r_vsync3_mod Bit[0]: r_vsync2_mod
0x4705	DVP_EOF_VSYNC DELAY	0x00	RW	Bit[7:0]: eof_vsync_delay[23:16] SOF/EOF negative edge to VSYNC positive edge delay
0x4706	DVP_EOF_VSYNC DELAY	0x00	RW	Bit[7:0]: eof_vsync_delay[15:8] SOF/EOF negative edge to VSYNC positive edge delay
0x4707	DVP_EOF_VSYNC DELAY	0x00	RW	Bit[7:0]: eof_vsync_delay[7:0] SOF/EOF negative edge to VSYNC positive edge delay
0x4708	DVP_POL_CTRL	0x01	RW	Bit[7]: Clock DDR mode enable Bit[5]: VSYNC gated clock enable Bit[4]: HREF gated clock enable Bit[3]: No first for FIFO Bit[2]: HREF polarity reverse Bit[1]: VSYNC polarity reverse Bit[0]: PCLK polarity reverse
0x4709	BIT_TEST_PATTERN	0x00	RW	Bit[7]: FIFO bypass mode Bit[6:4]: Data bit swap Bit[3]: Bit test mode Bit[2]: 10-bit bit test Bit[1]: 8-bit bit test Bit[0]: Bit test enable
0x470A	DVP_BYP_CTRL	0x00	RW	Bit[7:0]: bypass_ctrl[15:8]
0x470B	DVP_BYP_CTRL	0x00	RW	Bit[7:0]: bypass_ctrl[7:0]
0x470C	DVP_BYP_SEL	0x00	RW	Bit[4]: HREF select Bit[3:0]: Bypass select

6.6.1 DVP timing

figure 6-1 DVP timing diagram



note
Timing values shown in table 6-7 may vary depending upon register settings.

table 6-7 DVP timing specifications (sheet 1 of 2)

mode	timing
5 Megapixel 2592x1944	(1) 5,313,600 tp (2) 2,956 tp (3) 29,624 tp (4) 2,700 tp (5) 32,328 tp (6) 2,592 tp (7) 108 tp where tp = 1 pclk
1080p 1920x1080	(1) 2,720,256 tp (2) 2,720 tp (3) 27,464 tp (4) 2,464 tp (5) 29,496 tp (6) 1,920 tp (7) 544 tp where tp = 1 pclk
960p 1280x960	(1) 1,857,792 tp (2) 2,144 tp (3) 13,640 tp (4) 1,888 tp (5) 30,136 tp (6) 1,280 tp (7) 608 tp where tp = 1 pclk

table 6-7 DVP timing specifications (sheet 2 of 2)

mode	timing
720p 1280x720	(1) 1,404,672 tp (2) 2,144 tp (3) 21,192 tp (4) 1,888 tp (5) 22,584 tp (6) 1,280 tp (7) 608 tp where tp = 1 pclk
VGA 640x480	(1) 927,360 tp (2) 2,096 tp (3) 12,056 tp (4) 1,840 tp (5) 31,208 tp (6) 640 tp (7) 1,200 tp where tp = 1 pclk
QVGA 320x240	(1) 675,840 tp (2) 2,816 tp (3) 17,416 tp (4) 2,560 tp (5) 43,448 tp (6) 320 tp (7) 2,240 tp where tp = 1 pclk

6.7 mobile industry processor interface (MIPI)

The OV5647 provides one clock lane and two data lanes for the communications link between sensor (transmitter) and receiver inside a mobile device. It follows MIPI specifications D-PHY 0.89 and above and CSI2-V1, and supports all mandatory MIPI features. Most of the optional features (e.g., LP transfer mode) are not supported unless otherwise specified in this specification. For any further questions, contact your local OmniVision FAE for more details.

table 6-8 MIPI transmitter registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x4800	MIPI CTRL 00	0x04	RW	MIPI Control 00 Bit[7:6]: Debug mode Bit[5]: Clock lane gate enable 0: Clock lane is free running 1: Gate clock lane when no packet to transmit Bit[4]: Line sync enable 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Lane select 0: Use lane1 as default data lane 1: Use lane2 as default data lane Bit[2]: Idle status 0: MIPI bus will be LP00 when no packet to transmit 1: MIPI bus will be LP11 when no packet to transmit Bit[1:0]: Debug mode

table 6-8 MIPI transmitter registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x4801	MIPI CTRL 01	0x0F	RW	MIPI Control 01 Bit[7]: Long packet data type manual enable 0: Use mipi_dt 1: Use dt_man_o as long packet data (see register 0x4814[5:0]) Bit[6]: Short packet data type manual enable 1: Use dt_spkt as short packet data (see register 0x4815[5:0]) Bit[5]: Short packet word counter manual enable 0: Use frame counter or line counter 1: Select spkt_wc_reg_o (see {0x4812, 0x4813}) Bit[4]: PH bit order for ECC 0: {DI[7:0],WC[7:0],WC[15:8]} 1: {DI[0:7],WC[0:7],WC[8:15]} Bit[3]: PH byte order for ECC 0: {DI,WC_l,WC_h} 1: {DI,WC_h,WC_l} Bit[2]: PH byte order2 for ECC 0: {DI,WC} 1: {WC,DI} Bit[1:0]: Debug mode

table 6-8 MIPI transmitter registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x4802	MIPI CTRL 02	0x00	RW	MIPI Control 02 Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail.min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]
0x4805	MIPI CTRL 05	0x10	RW	MIPI Control 05 Bit[7]: MIPI lane1 disable 1: Disable MIPI data lane1, lane1 will be LP00 Bit[6]: MIPI lane2 disable 1: Disable MIPI data lane2, lane2 will be LP00 Bit[5]: lpx_p_sel 0: Auto calculate t_lpx_o in pclkex domain, unit pclk2x 1: Use lp_p_min[7:0] Bit[4]: lp_rx_intr_sel 0: Send lp_rx_intr_o at the first byte 1: Send lp_rx_intr_o at the end of receiving Bit[3:1]: Debug mode Bit[0]: Not used
0x4810	MIPI MAX FRAME COUNT	0xFF	RW	High Byte of Max Frame Count of Frame Sync Short Packet

table 6-8 MIPI transmitter registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x4811	MIPI MAX FRAME COUNT	0xFF	RW	Low Byte of Max Frame Count of Frame Sync Short Packet
0x4814	MIPI CTRL14	0x2A	RW	MIPI Control 14 Bit[7:6]: Virtual channel of MIPI Bit[5:0]: Data type in manual mode
0x4815	MIPI_DT_SPKT	0x00	RW	Bit[6]: Debug Mode Bit[5:0]: Manual data type for short packet
0x4818	HS_ZERO_MIN	0x00	RW	High Byte of the Minimum Value for hs_zero Unit ns
0x4819	HS_ZERO_MIN	0x96	RW	Low Byte of the Minimum Value for hs_zero, unit ns hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	HS_TRAIL_MIN	0x00	RW	High Byte of the Minimum Value for hs_trail, unit ns
0x481B	HS_TRAIL_MIN	0x3C	RW	Low Byte of the Minimum Value for hs_trail, hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	CLK_ZERO_MIN	0x01	RW	High Byte of the Minimum Value for clk_zero, unit ns
0x481D	CLK_ZERO_MIN	0x86	RW	Low Byte of the Minimum Value for clk_zero, clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	CLK_PREPARE_MIN	0x00	RW	High Byte of the Minimum Value for clk_prepare, unit ns Bit[1:0]: clk_prepare_min[9:8]
0x481F	CLK_PREPARE_MIN	0x3C	RW	Low Byte of the Minimum Value for clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	CLK_POST_MIN	0x00	RW	High Byte of the Minimum Value for clk_post, unit ns Bit[1:0]: clk_post_min[9:8]
0x4821	CLK_POST_MIN	0x56	RW	Low Byte of the Minimum Value for clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o
0x4822	CLK_TRAIL_MIN	0x00	RW	High Byte of the Minimum Value for clk_trail, unit ns Bit[1:0]: clk_trail_min[9:8]
0x4823	CLK_TRAIL_MIN	0x3C	RW	Low Byte of the Minimum Value for clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	LPX_P_MIN	0x00	RW	High Byte of the Minimum Value for lpx_p, unit ns Bit[1:0]: lpx_p_min[9:8]
0x4825	LPX_P_MIN	0x32	RW	Low Byte of the Minimum Value for lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o

table 6-8 MIPI transmitter registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x4826	HS_PREPARE_MIN	0x00	RW	High Byte of the Minimum Value for hs_prepare, unit ns Bit[1:0]: hs_prepare_min[9:8]
0x4827	HS_PREPARE_MIN	0x32	RW	Low Byte of the Minimum Value for hs_prepare hs_prepare_real = hs_prepare_min_o + Tui*ui_hs_prepare_min_o
0x4828	HS_EXIT_MIN	0x00	RW	High Byte of the Minimum Value for hs_exit, unit ns Bit[1:0]: hs_exit_min[9:8]
0x4829	HS_EXIT_MIN	0x64	RW	Low Byte of the Minimum Value for hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	UI_HS_ZERO_MIN	0x05	RW	Minimum UI Value of hs_zero, unit UI
0x482B	UI_HS_TRAIL_MIN	0x04	RW	Minimum UI Value of hs_trail, unit UI
0x482C	UI_CLK_ZERO_MIN	0x00	RW	Minimum UI Value of clk_zero, unit UI
0x482D	UI_CLK_PREPARE_MIN	0x00	RW	Minimum UI Value of clk_prepare, unit UI
0x482E	UI_CLK_POST_MIN	0x34	RW	Minimum UI Value of clk_post, unit UI
0x482F	UI_CLK_TRAIL_MIN	0x00	RW	Minimum UI Value of clk_trail, unit UI
0x4830	UI_LPX_P_MIN	0x00	RW	Minimum UI Value of lpx_p, unit UI
0x4831	UI_HS_PREPARE_MIN	0x04	RW	Minimum UI Value of hs_prepare, unit UI
0x4832	UI_HS_EXIT_MIN	0x00	RW	Minimum UI Value of hs_exit, unit UI
0x4833	MIPI_REG_MIN	0x00	RW	MIPI Register Address, Lower Bound (High Byte) Address range of MIPI RW registers is from mipi_reg_min to mipi_reg_max
0x4834	MIPI_REG_MIN	0x00	RW	MIPI Register Address, Lower Bound (Low Byte)
0x4835	MIPI_REG_MAX	0xFF	RW	MIPI Register Address, Upper Bound (High Byte)
0x4836	MIPI_REG_MAX	0xFF	RW	MIPI Register Address, Upper Bound (Low Byte)
0x4837	PCLK_PERIOD	0x15	RW	Period of pclk2x, pclk_div = 1, and 1-bit decimal
0x4838	WKUP_DLY	0x02	RW	Wakeup delay for MIPI
0x483A	DEBUG MODE	–	–	Debug Mode

table 6-8 MIPI transmitter registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x483B	MIPI_LP_GPIO	0x33	RW	Bit[7]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 as mipi_lp_dir1_o Bit[6]: lp_dir_man1 0: Input 1: Output Bit[5]: lp_p1_o Bit[4]: lp_n1_o Bit[3]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 as mipi_lp_dir2_o Bit[2]: lp_dir_man2 0: Input 1: Output Bit[1]: lp_p2_o Bit[0]: lp_n2_o
0x483C	MIPI CTRL 33	0x4F	RW	Bit[7:4]: t_lpx Unit: sclk cycles Bit[3:0]: t_clk_pre Unit: sclk cycles
0x483D~ 0x483F	DEBUG MODE	–	–	Debug Mode
0x4843	SNR_PCLK_DIV	0x00	RW	Bit[0]: PCLK divider 0: PCLK/SCLK = 2 and pclk_div = 1 1: PCLK/SCLK = 1 and pclk_div = 1

7 register tables

The following tables provide descriptions of the device control registers contained in the OV5647. For all registers enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x6C for write and 0x6D for read.

7.1 system control [0x3000 - 0x3209]

table 7-1 system control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x3000	SC_CMMN_PAD_OEN0	0x00	RW	I/O Direction (0: input; 1: output) Bit[7:2]: Not used Bit[1:0]: D[9:8]
0x3001	SC_CMMN_PAD_OEN1	0x00	RW	I/O Direction (0: input; 1: output) Bit[7:0]: D[7:0]
0x3002	SC_CMMN_PAD_OEN2	0x00	RW	I/O Direction (0: input; 1: output) Bit[7]: VSYNC Bit[6]: HREF Bit[5]: PCLK Bit[4]: FREX Bit[3]: STROBE Bit[2]: SDA Bit[1]: GPIO1 Bit[0]: GPIO0
0x3003~ 0x3005	DEBUG MODE	–	–	Debug Mode
0x3006	SC_CMMN_PLL_CTR13	0x00	RW	Bit[7:6]: Debug control Changing these registers is not recommended Bit[5:2]: SDIV Clock divider for 50/60 Hz detection block Bit[1:0]: Debug control Changing these registers is not recommended
0x3007	DEBUG MODE	–	–	Debug Mode
0x3008	SC_CMMN_PAD_OUT0	0x00	RW	I/O Output Value Bit[7:2]: Not used Bit[1:0]: D[9:8]
0x3009	SC_CMMN_PAD_OUT1	0x00	RW	I/O Output Value Bit[7:0]: D[7:0]
0x300A	SC_CMMN_CHIP_ID	0x56	R	Chip ID High Byte
0x300B	SC_CMMN_CHIP_ID	0x47	R	Chip ID Low Byte

table 7-1 system control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x300C	SC_CMMN_SCCB_ID	0x6C	RW	SCCB ID
0x300D	SC_CMMN_PAD_OUT2	0x00	RW	I/O Output Value Bit[7]: VSYNC Bit[6]: HREF Bit[5]: PCLK Bit[4]: FREX Bit[3]: STROBE Bit[2]: SDA Bit[1]: GPIO1 Bit[0]: GPIO0
0x300E	SC_CMMN_PAD_SEL0	0x00	RW	I/O Pad Select Bit[7:2]: Not used Bit[1:0]: D[9:8]
0x300F	SC_CMMN_PAD_SEL1	0x00	RW	I/O Pad Select Bit[7:0]: D[7:0]
0x3010	SC_CMMN_PAD_SEL2	0x00	RW	I/O Pad Select Bit[7]: VSYNC Bit[6]: HREF Bit[5]: PCLK Bit[4]: FREX Bit[3]: STROBE Bit[2]: SDA Bit[1]: GPIO1 Bit[0]: GPIO0
0x3011	SC_CMMN_PAD_PK	0x02	RW	Bit[7]: pd_dato_en Bit[6:5]: IO drive strength 00: 1x 01: 1x 10: 2x 11: 2x Bit[4:2]: Not used Bit[1]: FREX pad enable 0: Enable 1: Disable Bit[0]: Not used
0x3012	DEBUG MODE	–	–	Debug Mode
0x3013	SC_CMMN_A_PWC_PK_O	0x00	RW	Bit[7:4]: Debug control Changing these registers is not recommended Bit[3]: bp_regulator 0: Enable internal regulator 1: Disable internal regulator Bit[2:0]: Debug control Changing these registers is not recommended

table 7-1 system control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x3014	SC_CMMN_A_PWC_PK_O	0x0B	RW	Bit[7]: Not used Bit[6:4]: apd[2:0] Bit[3:0]: dio
0x3016	SC_CMMN_MIPI_PHY	0x00	RW	Bit[7:6]: lph Bit[5:4]: Not used Bit[3]: mipi_pad_enable Bit[2]: pgm_bp_hs_en_lat Bypass the latch of hs_enable Bit[1:0]: ictl[1:0] Bias current adjustment
0x3017	SC_CMMN_MIPI_PHY	0x10	RW	Bit[7:6]: pgm_vcm[1:0] High speed common mode voltage Bit[5:4]: pgm_lptx[1:0] Driving strength of low speed transmitter 01 Bit[3]: ihalf Bias current reduction Bit[2]: pgm_vicd CD input low voltage Bit[1]: pgm_vih CD input high voltage-dummy Bit[0]: pgm_hs_valid Valid delay-dummy
0x3018	SC_CMMN_MIPI_SC_CTRL	0x58	RW	Bit[7:5]: mipi_lane_mode 001: One lane mode 010: Two lane mode others: Not used Bit[4]: r_phy_pd_mipi 0: Not used 1: Power down PHY HS TX Bit[3]: r_phy_pd_lprx 0: Not used 1: Power down PHY LP RX module Bit[2]: mipi_en 0: DVP enable 1: MIPI enable Bit[1]: mipi_susp_reg MIPI system suspend register 0: Not used 1: Suspend Bit[0]: lane_dis_op 0: Use mipi_release1/2 and lane_disable1/2 to disable two data lane 1: Use lane_disable1/2 to disable two data lane

table 7-1 system control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x3019	SC_CMMN_MIPI_SC_CTRL	0x10	RW	Bit[7:0]: MIPI ULPS resume mark1 detect length
0x301A~0x3020	DEBUG MODE	–	–	Debug Mode
0x3021	SC_CMMN_MISC_CTRL	0x23	RW	Bit[7:6]: Not used Bit[5]: fst_stby_ctr 0: Software standby enter at v_blk 1: Software standby enter at l_blk Bit[4]: mipi_ctr_en 1: Enable MIPI remote reset and suspend control SC 0: Disable the function Bit[3]: mipi_rst_sel 0: MIPI remote reset all registers 1: MIPI remote reset all digital modules Bit[2]: gpio_pclk_en Bit[1]: frex_ef_sel Bit[0]: cen_global_o
0x3022	SC_CMMN_MIPI_SC_CTRL	0x00	RW	Bit[7:4]: Not used Bit[3]: lptx_ck_opt Bit[2]: pull_down_clk_lane Bit[1]: pull_down_data_lane2 Bit[0]: pull_down_data_lane1
0x302A	SC_CMMN_SUB_ID	0xB1	R	Bit[7:4]: Process Bit[3:0]: Version
0x3034	SC_CMMN_PLL_CTRL0	0x1A	RW	Bit[7]: Not used Bit[6:4]: pll_charge_pump Bit[3:0]: mipi_bit_mode 1000: 8 bit mode 1010: 10 bit mode
0x3035	SC_CMMN_PLL_CTRL1	0x11	RW	Bit[7:4]: system_pll_div Bit[3:0]: scale_divider_mipi
0x3036	SC_CMMN_PLL_MULTIPLIER	0x69	RW	Bit[7:0]: PLL_multiplier (4~252) This can be any integer during 4~127 and only even integer during 128~252

table 7-1 system control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x3037	SC_CMMN_PLL_ CTR13	0x03	RW	Bit[7:5]: Debug mode Bit[4]: pll_root_div 0: Bypass 1: /2 Bit[3:0]: pll_prediv 1, 2, 3, 4, 6, 8
0x3038	SC_CMMN_PLL_ DEBUG_OPT	0x00	RW	Bit[7]: pll_mult_debug_en Bit[1:0]: pll_mult1_debug
0x3039	SC_CMMN_PLL_ CTRL_R	0x00	RW	Bit[7]: pll_bypass Bit[6:0]: Not used
0x303A	SC_CMMN_PLLS_ CTRL0	0x00	RW	Bit[7]: plls_bypass Bit[6:0]: Not used
0x303B	SC_CMMN_PLLS_ CTRL1	0x19	RW	Bit[7:5]: Not used Bit[4:0]: plls_multiplier
0x303C	SC_CMMN_PLLS_ CTRL2	0x11	RW	Bit[6:4]: plls_cp Bit[3:0]: plls_sys_div
0x303D	SC_CMMN_PLLS_ CTRL3	0x30	RW	Bit[7:6]: Not used Bit[5:4]: plls_pre_div 00: /1 01: /1.5 10: /2 11: /3 Bit[2]: plls_div_r 0: /1 1: /2 Bit[1:0]: plls_seld5 00: /1 01: /1 10: /2 11: /2.5
0x3040~ 0x3044	DEBUG MODE	–	–	Debug Mode
0x3106	SRB CTRL	0xF9	RW	Bit[7:4]: Not used Bit[3:2]: PLL clock divider 00: pll_sclk 01: pll_sclk/2 10: pll_sclk/4 11: pll_sclk Bit[1]: rst_arb 0: Not used 1: Reset arbiter Bit[0]: sclk_arb 0: Not used 1: Enable SCLK to arbiter

7.2 group hold control [0x3200 - 0x3208]

table 7-2 group hold control registers

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Group0 Start Address in SRAM, actual address is {0x3200[3:0], 4'h0}
0x3201	GROUP ADR1	0x04	RW	Group1 Start Address in SRAM, actual address is {0x3201[3:0], 4'h0}
0x3202	GROUP ADR2	0x08	RW	Group2 Start Address in SRAM, actual address is {0x3202[3:0], 4'h0}
0x3203	GROUP ADR3	0x0B	RW	Group3 Start Address in SRAM, actual address is {0x3203[3:0], 4'h0}
0x3204	GROUP LEN0	–	R	Length of Group0
0x3205	GROUP LEN1	–	R	Length of Group1
0x3206	GROUP LEN2	–	R	Length of Group2
0x3207	GROUP LEN3	–	R	Length of Group3
0x3208	GROUP ACCESS	–	W	Bit[7:4]: Group_ctrl 0000: Enter group write mode 0001: Exit group write mode 1010: Initiate group write Bit[3:0]: Group ID 0000: Group 0 0001: Group 1 0010: Group 2 0011: Group 3
0x3209	DEBUG MODE	–	–	Debug Mode

7.3 AEC/AGC [0x3500 - 0x373A, 0x3A00 - 0x3A21, 0x5680 - 0x5A41]

table 7-3 AEC/AGC registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x3500	EXPOSURE	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Exposure[19:16] Exposure in units of 1/16 line
0x3501	EXPOSURE	0x02	RW	Bit[7:0]: Exposure[15:8] Exposure in units of 1/16 line
0x3502	EXPOSURE	0x00	RW	Bit[7:0]: Exposure[7:0] Exposure in units of 1/16 line; lower four bits are a fraction of a line; they should be 0 since OV5647 does not support fraction line exposure
0x3503	MANUAL CTRL	0x00	RW	Bit[7:6]: Not used Bit[5:4]: Gain latch timing delay x0: Gain has no latch delay 01: Gain delay of 1 frame 11: Gain delay of 2 frames Bit[2]: Not used Bit[1]: AGC manual 0: Auto enable 1: Manual enable Bit[0]: AEC manual 0: Auto enable 1: Manual enable
0x350A	AGC	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gain[9:8] AGC real gain output high byte Gain = {0x350A[1:0], 0x350B[7:0]}/16
0x350B	AGC	0x10	RW	Bit[7:0]: Gain[7:0] AGC real gain output low byte
0x3600~ 0x3637	ANALOG_CONTROL	–	RW	Analog Control Registers
0x3700~ 0x373A	ANALOG_CONTROL	–	RW	Analog Control Registers
0x3A00	AEC CTRL00	0x78	RW	Bit[7:6]: Not used Bit[5]: Band function Bit[4]: Band low limit mode Bit[3]: start_sel Bit[2]: Night mode Bit[1]: Not used Bit[0]: Freeze

table 7-3 AEC/AGC registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x3A01	MIN EXPO	0x01	RW	Bit[7:0]: Min expo
0x3A02	MAX EXPO 60	0x3D	RW	Bit[7:0]: Max expo[15:8] Night mode ceiling of 60 Hz
0x3A03	MAX EXPO 60	0x80	RW	Bit[7:0]: Max expo[7:0] Night mode ceiling of 60 Hz
0x3A05	AEC CTRL05	0x30	RW	Bit[7]: f50_reverse 0: Hold 50, 60Hz detect input 1: Switch 50, 60Hz detect input Bit[6]: frame_insert 0: In night mode, insert frame disable 1: In night mode, insert frame enable Bit[5]: step_auto_en 0: Step manual mode 1: Step auto mode Bit[4:0]: step_auto_ratio In step auto mode, set the step ratio setting to adjust speed
0x3A06	AEC CTRL06	0x10	RW	Bit[7:5]: Not used Bit[4:0]: step_man1 Step manual Increase mode fast step
0x3A07	AEC CTRL07	0x18	RW	Bit[7:4]: step_man2 Step manual, slow step Bit[3:0]: step_man3 Step manual, decrease mode fast step
0x3A08	B50 STEP	0x01	RW	Bit[7:2]: Not used Bit[1:0]: b50_step[9:8] Banding step size for 50 Hz
0x3A09	B50 STEP	0x27	RW	Bit[7:0]: b50_step[7:0] Banding step size for 50 Hz
0x3A0A	B60 STEP	0x00	RW	Bit[7:2]: Not used Bit[1:0]: b60_step[9:8] Banding step size for 60 Hz
0x3A0B	B60 STEP	0xF6	RW	Bit[7:0]: b60_step[7:0] Banding step size for 60 Hz
0x3A0C	AEC CTRL0C	0xE4	RW	Bit[7:4]: e1_max Decimal line high limit zone Bit[3:0]: e1_min Decimal line low limit zone

table 7-3 AEC/AGC registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x3A0D	B60 MAX	0x08	RW	Bit[7:6]: Not used Bit[5:0]: b60_max Max banding step number for 60 Hz
0x3A0E	B50 MAX	0x06	RW	Bit[7:6]: Not used Bit[5:0]: b50_max Max banding step number for 50 Hz
0x3A0F	WPT	0x78	RW	Bit[7:0]: WPT Stable range high limit (from unstable state to stable state)
0x3A10	BPT	0x68	RW	Bit[7:0]: BPT Stable range low limit (from unstable state to stable state)
0x3A11	HIGH VPT	0xD0	RW	Bit[7:0]: vpt_high Fast zone high limit (when step ratio auto mode is disabled)
0x3A12	MANUAL AVG	0x00	RW	Bit[7:0]: avg_man
0x3A13	PRE GAIN	0x40	RW	Bit[7]: Not used Bit[6]: Pre-gain enable Bit[5:0]: Pre-gain value
0x3A14	MAX EXPO 50	0x0E	RW	Bit[7:0]: Maximum expo[15:8] Night mode ceiling of 50 Hz
0x3A15	MAX EXPO 50	0x40	RW	Bit[7:0]: Maximum expo[7:0] Night mode ceiling of 50 Hz
0x3A17	NIGHT MODE GAIN BASE	0x01	RW	Bit[7:2]: Not used Bit[1:0]: gnight_thre Night mode gain threshold 00: 1x 01: 2x 10: 4x 11: 8x
0x3A18	AEC GAIN CEILING	0x00	RW	Bit[7:2]: Not used Bit[1:0]: gain_ceiling[9:8] Gain ceiling = {0x3A18[1:0], 0x3A19[7:0]}/16
0x3A19	AEC GAIN CEILING	0x7C	RW	Bit[7:0]: gain_ceiling[7:0]
0x3A1A	DIFF MAX	0x04	RW	Bit[7:0]: diff_max
0x3A1B	WPT2	0x78	RW	Bit[7:0]: wpt2 Stable range high limit (from stable state to unstable state)

table 7-3 AEC/AGC registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x3A1C	LED ADD ROW	0x06	RW	Bit[7:0]: led_add_row[15:8] Exposure values added when STROBE is ON
0x3A1D	LED ADD ROW	0x18	RW	Bit[7:0]: led_add_row[7:0] Exposure values added when STROBE is ON
0x3A1E	BPT2	0x68	RW	Bit[7:0]: bpt2 Stable range low limit (from stable state to unstable state)
0x3A1F	LOW VPT	0x40	RW	Bit[7:0]: vpt_low Fast zone low limit (when step ration auto mode is disabled)
0x3A20	AEC CTRL20	0x00	RW	Bit[7:2]: Not used Bit[1]: man_avg_en_i 0: Disable 1: Enable Bit[0]: Not used
0x3A21	AEC CTRL21	0x70	RW	Bit[7:]: Not used Bit[6:4]: Frame insert number Bit[3:0]: Not used
0x5680	X START	0x00	RW	Bit[7:5]: Not used Bit[4:0]: x_start[11:8] Horizontal start position for average window high byte
0x5681	X START	0x00	RW	Bit[7:0]: x_start[7:0] Horizontal start position for average window low byte
0x5682	Y START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: y_start[10:8] Vertical start position for average window high byte
0x5683	Y START	0x00	RW	Bit[7:0]: y_start[7:0] Vertical start position for average window low byte
0x5684	X WINDOW	0x0A	RW	Bit[7:5]: Not used Bit[4:0]: x_window[12:8] Window X in manual average window mode high byte
0x5685	X WINDOW	0x20	RW	Bit[7:0]: x_window[7:0] Window X in manual average window mode low byte

table 7-3 AEC/AGC registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x5686	Y WINDOW	0x07	RW	Bit[7:4]: Not used Bit[3:0]: y_window[11:8] Window Y in manual average window mode high byte
0x5687	Y WINDOW	0x98	RW	Bit[7:0]: y_window[7:0] Window Y in manual average window mode low byte
0x5688	WEIGHT00	0x11	RW	Bit[7:4]: window1_weight Bit[3:0]: window0_weight
0x5689	WEIGHT01	0x11	RW	Bit[7:4]: window3_weight Bit[3:0]: window2_weight
0x568A	WEIGHT02	0x11	RW	Bit[7:4]: window5_weight Bit[3:0]: window4_weight
0x568B	WEIGHT03	0x11	RW	Bit[7:4]: window7_weight Bit[3:0]: window6_weight
0x568C	WEIGHT04	0x11	RW	Bit[7:4]: window9_weight Bit[3:0]: window8_weight
0x568D	WEIGHT05	0x11	RW	Bit[7:4]: window11_weight Bit[3:0]: window10_weight
0x568E	WEIGHT06	0x11	RW	Bit[7:4]: window13_weight Bit[3:0]: window12_weight
0x568F	WEIGHT07	0x11	RW	Bit[7:4]: window15_weight Bit[3:0]: window14_weight
0x5690	AVG CTRL10	0x02	RW	Bit[7:2]: Not used Bit[1]: avg_opt Bit[0]: avg_man 0: Auto average window 1: Manual average window
0x5691	AVG WEIGHT SUM	–	R	avg_wt_sum_o
0x5692	DEBUG MODE	–	–	Debug Mode
0x5693	AVG READOUT	–	R	Bit[7:0]: AVG value
0x5A00	DIGC CTRL0	0x00	RW	Bit[7:4]: Not used Bit[3]: Debug mode Bit[2]: dig_comp_bypass Bit[1]: dig_comp_man_opt Bit[0]: dig_comp_man_en
0x5A02	DIG COMP MAN	0x02	RW	Bit[7:2]: Not used Bit[1:0]: dig_comp_man[9:8]
0x5A03	DIG COMP MAN	0x00	RW	Bit[7:0]: dig_comp_man[7:0]

table 7-3 AEC/AGC registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x5A20	SENSOR GAIN MAN	0x00	RW	Bit[7:1]: Not used Bit[0]: gainc_sensorgain_man[8]
0x5A21	SENOR GAIN MAN	0x00	RW	Bit[7:0]: gainc_sensorgain_man[7:0]
0x5A22	DIG COMP MAN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: gainc_dgc_man[9:8]
0x5A23	DIG COMP MAN	0x00	RW	Bit[7:0]: gainc_dgc_man[7:0]
0x5A24	GAINC CTRL0	0x00	RW	Bit[7:3]: Not used Bit[2]: Debug mode Bit[1]: bypass_opt Bit[0]: gainc_man_en
0x5A40	GAINF ANA NUM	0x07	RW	Bit[7:0]: gainf_ana_bit_num
0x5A41	GAINF DIG GAIN	0x00	RW	Bit[7:0]: gainf_dig_gain

7.4 timing control [0x3800 - 0x3834]

table 7-4 system timing registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3800	TIMING_X_ADDR_ START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: x_addr_start[11:8]
0x3801	TIMING_X_ADDR_ START	0x0C	RW	Bit[7:0]: x_addr_start[7:0]
0x3802	TIMING_Y_ADDR_ START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: y_addr_start[11:8]
0x3803	TIMING_Y_ADDR_ START	0x04	RW	Bit[7:0]: y_addr_start[7:0]
0x3804	TIMING_X_ADDR_ END	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: x_addr_end[11:8]
0x3805	TIMING_X_ADDR_END	0x33	RW	Bit[7:0]: x_addr_end[7:0]
0x3806	TIMING_Y_ADDR_END	0x07	RW	Bit[7:4]: Not used Bit[3:0]: y_addr_end[11:8]
0x3807	TIMING_Y_ADDR_END	0xA3	RW	Bit[7:0]: y_addr_end[7:0]
0x3808	TIMING_X_OUTPUT_SIZE	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: DVP output horizontal width[11:8]

table 7-4 system timing registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3809	TIMING_X_OUTPUT_SIZE	0x20	RW	Bit[7:0]: DVP output horizontal width[7:0]
0x380A	TIMING_Y_OUTPUT_SIZE	0x07	RW	Bit[7:4]: Not used Bit[3:0]: DVP output vertical height[11:8]
0x380B	TIMING_Y_OUTPUT_SIZE	0x98	RW	Bit[7:0]: DVP output vertical height[7:0]
0x380C	TIMING_HTS	0x0A	RW	Bit[7:5]: Not used Bit[4:0]: Total horizontal size[12:8]
0x380D	TIMING_HTS	0x8C	RW	Bit[7:0]: Total horizontal size[7:0]
0x380E	TIMING_VTS	0x07	RW	Bit[7:0]: Total vertical size[15:8]
0x380F	TIMING_VTS	0xB0	RW	Bit[7:0]: Total vertical size[7:0]
0x3810	TIMING_ISP_X_WIN	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ISP horizontal offset[11:8]
0x3811	TIMING_ISP_X_WIN	0x04	RW	Bit[7:0]: ISP horizontal offset[7:0]
0x3812	TIMING_ISP_Y_WIN	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ISP vertical offset[11:8]
0x3813	TIMING_ISP_Y_WIN	0x02	RW	Bit[7:0]: ISP vertical offset[7:0]
0x3814	TIMING_X_INC	0x11	RW	Bit[7:4]: h_odd_inc Horizontal subsample odd increase number Bit[3:0]: h_even_inc Horizontal subsample even increase number
0x3815	TIMING_Y_INC	0x11	RW	Bit[7:4]: v_odd_inc Vertical subsample odd increase number Bit[3:0]: v_even_inc Vertical subsample even increase number
0x3816	TIMING_HSYNCST	0x00	RW	Bit[7:4]: Not used Bit[3:0]: HSYNC start point[11:8]
0x3817	TIMING_HSYNCST	0x00	RW	Bit[7:0]: HSYNC start point[7:0]
0x3818	TIMING_HSYNCW	0x00	RW	Bit[7:4]: Not used Bit[3:0]: HSYNC window[11:8]
0x3819	TIMING_HSYNCW	0x00	RW	Bit[7:0]: HSYNC window[7:0]

table 7-4 system timing registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3820	TIMING_TC_REG20	0x40	RW	Bit[7]: Not used Bit[6:4]: For testing only Bit[3]: Not used Bit[2]: ISP vertical flip Bit[1]: Sensor vertical flip Bit[0]: Vertical binning
0x3821	TIMING_TC_REG21	0x00	RW	Bit[7:5]: For testing only Bit[4]: Not used Bit[3]: For testing only Bit[2]: ISP mirror Bit[1]: Sensor mirror Bit[0]: Horizontal binning
0x3822~ 0x3834	DEBUG MODE	–	–	Debug Mode

7.5 strobe/frame exposure [0x3B00 - 0x3B0C]

table 7-5 strobe/frame exposure control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B00	STROBE_RSTRB	0x00	RW	Strobe Control Bit[7]: Strobe request ON/OFF 0: OFF/BLC 1: ON Bit[6]: Strobe pulse reverse Bit[3:2]: width_in_xenon 00: 1 row period 01: 2 row period 10: 3 row period 11: 4 row period Bit[1:0]: Strobe mode 00: xenon 01: LED 1 10: LED 2 11: LED 3
0x3B01	STROBE_FREX_EXP_H2	0x00	RW	Bit[7:0]: frex_exp[23:16]
0x3B02	STROBE_SHUTTER_DLY	0x08	RW	Bit[7:0]: shutter_dly[12:8]
0x3B03	STROBE_SHUTTER_DLY	0x00	RW	Bit[7:0]: shutter_dly[7:0]
0x3B04	STROBE_FREX_EXP_H	0x04	RW	Bit[7:0]: frex_exp[15:8]

table 7-5 strobe/frame exposure control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B05	STROBE_ FREX_EXP_L	0x00	RW	Bit[7:0]: frex_exp[7:0]
0x3B06	STROBE_FREX_CTRL0	0x04	RW	Bit[7:6]: frex_pchg_width Bit[5:4]: frex_strobe_option Bit[3:0]: frex_strobe_width[3:0]
0x3B07	STROBE_FREX_MODE_SEL	0x08	RW	Bit[4]: frex_sa1 Bit[3]: fx1_fm_en Bit[2]: frex_inv Bit[1:0]: FREX strobe 00: frex_strobe mode1 01: frex_strobe mode2 1x: Rolling strobe
0x3B08	STROBE_FREX_EXP_REQ	0x00	RW	Bit[7:1]: Not used Bit[0]: frex_exp_req
0x3B09	FREX_SHUTTER_DELAY	0x00	RW	Bit[7:3]: Not used Bit[2:0]: FREX end option
0x3B0A	STROBE_FREX_RST_LENGTH	0x04	RW	Bit[7:3]: Not used Bit[2:0]: frex_rst_length[2:0]
0x3B0B	STROBE_WIDTH	0x00	RW	Bit[7:0]: frex_strobe_width[19:12]
0x3B0C	STROBE_WIDTH	0x3D	RW	Bit[7:0]: frex_strobe_width[11:4]

7.6 50/60 Hz detection [0x3C00 - 0x3C1E]

table 7-6 50/60 Hz detection registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3C00	50/60 HZ DETECTION CTRL00	0x00	RW	Bit[7:6]: Debug control Changing these registers is not recommended Bit[5:3]: 50/60 Hz detection control Contact your local OmniVision FAE for the correct settings Bit[2]: band_def Band50 default value 0: 60 Hz as default value 1: 50 Hz as default value Bit[1:0]: 50/60 Hz detection control register Contact your local OmniVision FAE for the correct settings

table 7-6 50/60 Hz detection registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3C01	50/60 HZ DETECTION CTRL01	0x00	RW	Bit[7]: band_man_en Band detection manual mode 0: Manual mode disable 1: Manual mode enable Bit[6:0]: 50/60 Hz detection control Contact your local OmniVision FAE for the correct settings
0x3C02~ 0x3C0B	50/60 HZ DETECTION CTRL02	–	RW	50/60 Hz detection Control Contact your local OmniVision FAE for the correct settings
0x3C0C	50/60 HZ DETECTION CTRL0C	–	R	Bit[7:1]: Debug control Changing these registers is not recommended Bit[0]: band50 0: Detection result is 60 Hz 1: Detection result is 50 Hz
0x3C0D~ 0x3C1E	DEBUG INFORMATION	–	RW	50/60 Hz Detection Control Contact your local OmniVision FAE for the correct settings

7.7 OTP control [0x3D00 - 0x3D21]

table 7-7 OTP control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3D00[a]	OTP_DATA_0	0x00	RW	OTP Buffer 0
0x3D01[a]	OTP_DATA_1	0x00	RW	OTP Buffer 1
0x3D02[a]	OTP_DATA_2	0x00	RW	OTP Buffer 2
0x3D03[a]	OTP_DATA_3	0x00	RW	OTP Buffer 3
0x3D04[a]	OTP_DATA_4	0x00	RW	OTP Buffer 4
0x3D05	OTP_DATA_5	0x00	RW	OTP Buffer 5
0x3D06	OTP_DATA_6	0x00	RW	OTP Buffer 6
0x3D07	OTP_DATA_7	0x00	RW	OTP Buffer 7
0x3D08	OTP_DATA_8	0x00	RW	OTP Buffer 8
0x3D09	OTP_DATA_9	0x00	RW	OTP Buffer 9

table 7-7 OTP control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3D0A	OTP_DATA_A	0x00	RW	OTP Buffer A
0x3D0B	OTP_DATA_B	0x00	RW	OTP Buffer B
0x3D0C	OTP_DATA_C	0x00	RW	OTP Buffer C
0x3D0D	OTP_DATA_D	0x00	RW	OTP Buffer D
0x3D0E	OTP_DATA_E	0x00	RW	OTP Buffer E
0x3D0F	OTP_DATA_F	0x00	RW	OTP Buffer F
0x3D10	OTP_DATA_16	0x00	RW	OTP Buffer 10
0x3D11	OTP_DATA_17	0x00	RW	OTP Buffer 11
0x3D12	OTP_DATA_18	0x00	RW	OTP Buffer 12
0x3D13	OTP_DATA_19	0x00	RW	OTP Buffer 13
0x3D14	OTP_DATA_20	0x00	RW	OTP Buffer 14
0x3D15	OTP_DATA_21	0x00	RW	OTP Buffer 15
0x3D16	OTP_DATA_22	0x00	RW	OTP Buffer 16
0x3D17	OTP_DATA_23	0x00	RW	OTP Buffer 17
0x3D18	OTP_DATA_24	0x00	RW	OTP Buffer 18
0x3D19	OTP_DATA_25	0x00	RW	OTP Buffer 19
0x3D1A	OTP_DATA_26	0x00	RW	OTP Buffer 1A
0x3D1B	OTP_DATA_27	0x00	RW	OTP Buffer 1B
0x3D1C	OTP_DATA_28	0x00	RW	OTP Buffer 1C
0x3D1D	OTP_DATA_29	0x00	RW	OTP Buffer 1D
0x3D1E	OTP_DATA_30	0x00	RW	OTP Buffer 1E
0x3D1F	OTP_DATA_31	0x00	RW	OTP Buffer 1F
0x3D20[b]	OTP_PROGRAM_CTRL	0x00	RW	Bit[7]: OTP_wr_busy Bit[6:2]: Debug control Changing these registers is not recommended Bit[1]: OTP_program_speed 0: Fast 1: Slow Bit[0]: OTP_program_enable Changing from 0 to 1 initiates OTP programming

table 7-7 OTP control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3D21	OTP_LOAD_CTRL	0x00	RW	Bit[7]: OTP_rd_busy Bit[1]: OTP speed 0: Fast 1: Slow Bit[0]: OTP_load_enable Changing from 0 to 1 initiates OTP read

a. 0x3D00~0x3D04 is reserved for OmniVision internal use.

b. AVDD must be 2.5V ± 5% when writing/programming OTP; otherwise, there will be reliability issues. There is no such limitation when reading OTP under normal operating conditions.

7.8 BLC control [0x4000 - 0x4067]

table 7-8 BLC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x89	RW	BLC Control Bit[7:1]: Debug mode Bit[0]: BLC enable 0: Disable 1: Enable
0x4001	BLC CTRL01	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: start_line
0x4002	BLC CTRL02	0x45	RW	Bit[7]: Debug mode Bit[6]: blc_auto_en Bit[5:0]: reset_frame_num
0x4003	BLC CTRL03	0x08	RW	Bit[7]: blc_redo_en Bit[6]: Freeze writing 1 to this bit will trigger a BLC redo N frames begin Bit[5:0]: manual_frame_num
0x4004	DEBUG MODE	0x08	RW	Bit[7:0]: Black line num
0x4005	BLC CTRL05	0x18	RW	Bit[7:2]: Debug mode Bit[1]: blc_always_up_en 0: Normal freeze 1: BLC always update Bit[0]: Not used
0x4006~ 0x4008	DEBUG MODE	–	–	Debug Mode

table 7-8 BLC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4009	BLACK LEVEL	0x10	RW	Bit[7:0]: blc_blackleveltarget0 Black level target
0x400A~ 0x4067	DEBUG MODE	–	–	Debug Mode

7.9 frame control [0x4200 - 0x4202]

table 7-9 frame control registers

address	register name	default value	R/W	description
0x4200	FRAME CTRL0	0x00	RW	Bit[7:3]: Not used Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fcnt_reset
0x4201	FRAME ON NUMBER	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Frame ON number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode
0x4202	FRAME OFF NUMBER	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Frame OFF number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode

7.10 DVP control [0x4700 - 0x470C]

table 7-10 DVP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4700	MODE SELECT	0x04	RW	Bit[7:4]: Not used Bit[3]: CCIR V select Bit[2]: CCIR F select Bit[1]: CCIR656 mode enable Bit[0]: HSYNC mode enable
0x4701	VSYNC WIDTH	0x01	RW	VSYNC Length in Terms of Line Count

table 7-10 DVP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4702	VSYNC NEG_WIDTH_H	0x01	RW	Bit[7:0]: VSYNC length in terms of pixel count[15:8]
0x4703	VSYNC NEG_WIDTH_L	0x00	RW	Bit[7:0]: VSYNC length in terms of pixel count[7:0]
0x4704	VSYNC MODE	0x00	RW	Bit[7:4]: Not used Bit[3:2]: r_vsyncout_sel Bit[1]: VSYNC mode3 Bit[0]: VSYNC mode2
0x4705	EOF VSYNC_DELAY_2	0x00	RW	Bit[7:0]: eof_vsync_delay[23:16] SOF/EOF negative edge to VSYNC positive edge delay
0x4706	EOF VSYNC_DELAY_1	0x00	RW	Bit[7:0]: eof_vsync_delay[15:8] SOF/EOF negative edge to VSYNC positive edge delay
0x4707	EOF VSYNC_DELAY_0	0x00	RW	Bit[7:0]: eof_vsync_delay[7:0] SOF/EOF negative edge to VSYNC positive edge delay
0x4708	POLARITY CTRL	0x01	RW	Bit[7]: Clock DDR mode enable Bit[6]: Not used Bit[5]: VSYNC gate clock enable Bit[4]: HREF gate clock enable Bit[3]: No first for FIFO Bit[2]: HREF polarity reverse option Bit[1]: VSYNC polarity reverse option Bit[0]: PCLK polarity reverse option
0x4709	BIT TEST ORDER	0x00	RW	Bit[7]: FIFO bypass mode Bit[6:4]: Data bit swap Bit[3]: Bit test mode Bit[2]: 10-bit bit test Bit[1]: 8-bit bit test Bit[0]: Bit test enable
0x470A	BYP CTRL1	0x00	RW	Bit[7:0]: bypass_ctrl[15:8]
0x470B	BYP CTRL0	0x00	RW	Bit[7:0]: bypass_ctrl[7:0]
0x470C	BYP SEL	0x00	RW	Bit[7:5]: Not used Bit[4]: href_sel Bit[3:0]: bypass_sel

7.11 MIPI control [0x4800 - 0x4843]

table 7-11 MIPI registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x4800	MIPI CTRL 00	0x04	RW	MIPI Control 00 Bit[7:6]: Debug mode Bit[5]: Clock lane gate enable 0: Clock lane is free running 1: Gate clock lane when no packet to transmit Bit[4]: Line sync enable 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Lane select 0: Use lane1 as default data lane 1: Use lane2 as default data lane Bit[2]: Idle status 0: MIPI bus will be LP00 when no packet to transmit 1: MIPI bus will be LP11 when no packet to transmit Bit[1:0]: Debug mode
0x4801	MIPI CTRL 01	0x0F	RW	MIPI Control 01 Bit[7]: Long packet data type manual enable 0: Use mipi_dt 1: Use dt_man_o as long packet data (see register 0x4814[5:0]) Bit[6]: Short packet data type manual enable 1: Use dt_spkt as short packet data (see register 0x4815[5:0]) Bit[5]: Short packet WORD COUNTER manual enable 0: Use frame counter or line counter 1: Select spkt_wc_reg_o (see {0x4812, 0x4813}) Bit[4]: PH bit order for ECC 0: {DI[7:0],WC[7:0],WC[15:8]} 1: {DI[0:7],WC[0:7],WC[8:15]} Bit[3]: PH byte order for ECC 0: {DI,WC_l,WC_h} 1: {DI,WC_h,WC_l} Bit[2]: PH byte order2 for ECC 0: {DI,WC} 1: {WC,DI} Bit[1:0]: Debug mode

table 7-11 MIPI registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x4802	MIPI CTRL 02	0x00	RW	MIPI Control 02 Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail.min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]
0x4803	MIPI CTRL 03	0x50	RW	Bit[7:0]: Debug mode
0x4804	MIPI CTRL 04	0x8D	RW	Bit[7:0]: Debug mode

table 7-11 MIPI registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x4805	MIPI CTRL 05	0x10	RW	MIPI Control 05 Bit[7]: MIPI lane1 disable 0: Not used 1: Disable MIPI data lane1, lane1 will be LP00 Bit[6]: MIPI lane2 disable 0: Not used 1: Disable MIPI data lane2, lane2 will be LP00 Bit[5]: lpx_p_sel 0: Auto calculate t_lpx_o in pclkex domain, unit pclk2x 1: Use lp_p_min[7:0] Bit[4]: lp_rx_intr_sel 0: Send lp_rx_intr_o at the first byte 1: Send lp_rx_intr_o at the end of receiving Bit[3:1]: Debug mode Bit[0]: Not used
0x4806	DEBUG MODE	–	–	Debug Mode
0x4810	MIPI MAX FRAME COUNT	0xFF	RW	High Byte of Max Frame Count of Frame Sync Short Packet
0x4811	MIPI MAX FRAME COUNT	0xFF	RW	Low Byte of Max Frame Count of Frame Sync Short Packet
0x4814	MIPI CTRL14	0x2A	RW	MIPI Control 14 Bit[7:6]: Virtual channel of MIPI Bit[5:0]: Data type in manual mode
0x4815	MIPI_DT_SPKT	0x00	RW	Bit[7]: Not used Bit[6]: Debug mode Bit[5:0]: Manual data type for short packet
0x4818	HS_ZERO_MIN	0x00	RW	High Byte of the Minimum Value for hs_zero Unit ns
0x4819	HS_ZERO_MIN	0x96	RW	Low Byte of the Minimum Value for hs_zero, unit ns hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	HS_TRAIL_MIN	0x00	RW	High Byte of the Minimum Value for hs_trail, unit ns
0x481B	HS_TRAIL_MIN	0x3C	RW	Low Byte of the Minimum Value for hs_trail, hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	CLK_ZERO_MIN	0x01	RW	High Byte of the Minimum Value for clk_zero, unit ns

table 7-11 MIPI registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x481D	CLK_ZERO_MIN	0x86	RW	Low Byte of the Minimum Value for clk_zero, clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	CLK_PREPARE_ MIN	0x00	RW	High Byte of the Minimum Value for clk_prepare, unit ns Bit[7:2]: Not used Bit[1:0]: clk_prepare_min[9:8]
0x481F	CLK_PREPARE_ MIN	0x3C	RW	Low Byte of the Minimum Value for clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	CLK_POST_MIN	0x00	RW	High Byte of the Minimum Value for clk_post, unit ns Bit[7:2]: Not used Bit[1:0]: clk_post_min[9:8]
0x4821	CLK_POST_MIN	0x56	RW	Low Byte of the Minimum Value for clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o
0x4822	CLK_TRAIL_MIN	0x00	RW	High Byte of the Minimum Value for clk_trail, unit ns Bit[7:2]: Not used Bit[1:0]: clk_trail_min[9:8]
0x4823	CLK_TRAIL_MIN	0x3C	RW	Low Byte of the Minimum Value for clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	LPX_P_MIN	0x00	RW	High Byte of the Minimum Value for lpx_p, unit ns Bit[7:2]: Not used Bit[1:0]: lpx_p_min[9:8]
0x4825	LPX_P_MIN	0x32	RW	Low Byte of the Minimum Value for lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x4826	HS_PREPARE_MIN	0x00	RW	High Byte of the Minimum Value for hs_prepare, unit ns Bit[7:2]: Not used Bit[1:0]: hs_prepare_min[9:8]
0x4827	HS_PREPARE_MIN	0x32	RW	Low Byte of the Minimum Value for hs_prepare hs_prepare_real = hs_prepare_min_o + Tui*ui_hs_prepare_min_o
0x4828	HS_EXIT_MIN	0x00	RW	High Byte of the Minimum Value for hs_exit, unit ns Bit[7:2]: Not used Bit[1:0]: hs_exit_min[9:8]
0x4829	HS_EXIT_MIN	0x64	RW	Low Byte of the Minimum Value for hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	UI_HS_ZERO_MIN	0x05	RW	Minimum UI Value of hs_zero, unit UI

table 7-11 MIPI registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x482B	UI_HS_TRAIL_MIN	0x04	RW	Minimum UI Value of hs_trail, unit UI
0x482C	UI_CLK_ZERO_ MIN	0x00	RW	Minimum UI Value of clk_zero, unit UI
0x482D	UI_CLK_PREPARE _MIN	0x00	RW	Minimum UI Value of clk_prepare, unit UI
0x482E	UI_CLK_POST_ MIN	0x34	RW	Minimum UI Value of clk_post, unit UI
0x482F	UI_CLK_TRAIL_ MIN	0x00	RW	Minimum UI Value of clk_trail, unit UI
0x4830	UI_LPX_P_MIN	0x00	RW	Minimum UI Value of lpx_p, unit UI
0x4831	UI_HS_PREPARE_ MIN	0x04	RW	Minimum UI Value of hs_prepare, unit UI
0x4832	UI_HS_EXIT_MIN	0x00	RW	Minimum UI Value of hs_exit, unit UI
0x4833	MIPI_REG_MIN	0x00	RW	MIPI Register Address, Lower Bound (High Byte) Address range of MIPI RW registers is from mipi_reg_min to mipi_reg_max
0x4834	MIPI_REG_MIN	0x00	RW	MIPI Register Address, Lower Bound (Low Byte)
0x4835	MIPI_REG_MAX	0xFF	RW	MIPI Register Address, Upper Bound (High Byte)
0x4836	MIPI_REG_MAX	0xFF	RW	MIPI Register Address, Upper Bound (Low Byte)
0x4837	PCLK_PERIOD	0x15	RW	Period of pclk2x, pclk_div = 1, and 1-bit decimal
0x4838	WKUP_DLY	0x02	RW	Wakeup Delay for MIPI
0x483A	DEBUG MODE	–	–	Debug Mode

table 7-11 MIPI registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x483B	MIPI_LP_GPIO	0x33	RW	Bit[7]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 as mipi_lp_dir1_o Bit[6]: lp_dir_man1 0: Input 1: Output Bit[5]: lp_p1_o Bit[4]: lp_n1_o Bit[3]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 as mipi_lp_dir2_o Bit[2]: lp_dir_man2 0: Input 1: Output Bit[1]: lp_p2_o Bit[0]: lp_n2_o
0x4843	SNR_PCLK_DIV	0x00	RW	Bit[7:1]: Not used Bit[0]: PCLK divider 0: PCLK/SCLK = 2 and pclk_div = 1 1: PCLK/SCLK = 1 and pclk_div = 1

7.12 ISP control [0x5000 - 0x5059]

table 7-12 ISP control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xFF	RW	ISP Control 00 (0: disable; 1: enable) Bit[7]: Lens shading correction Bit[2]: Black pixel correction Bit[1]: White pixel correction Bit[0]: Not used
0x5001	ISP CTRL01	0x01	RW	ISP Control 01 Bit[7:1]: Not used Bit[0]: AWB 0: Disable 1: Enable

table 7-12 ISP control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x5002	ISP CTRL02	0x41	RW	ISP Control 02 (0: disable; 1: enable) Bit[7:5]: Not used Bit[6]: win_en Bit[1]: otp_en Bit[0]: AWB gain
0x5003	ISP CTRL03	0x0A	RW	ISP Control 03 (0: disable; 1: enable) Bit[7:4]: Not used Bit[3]: buf_en Bit[2]: bin_man_set Bit[1]: bin_auto_en
0x5004	ISP CTRL04	0x00	RW	ISP Control 04 Bit[7:4]: Not used Bit[3]: size_man_en 0: Disable 1: Enable Bit[2:0]: Not used
0x5005	ISP CTRL05	0x31	RW	ISP Control 05 Bit[7]: sof_man 0: SOF from BLC module 1: SOF from pre_isp module Bit[6]: awb_bias_man_en 0: AWB bias manual disable 1: AWB bias manual enable Bit[5]: awb_bias_on 0: Disable AWB bias 1: Enable AWB bias Bit[4:3]: Not used Bit[2]: lenc_bias_on 0: Disable LENC bias 1: Enable LENC bias Bit[1]: Disable LENC bias s2p_sw_en_o Bit[0]: Disable LENC bias avg_en 0: Disable 1: Enable
0x5006	ISP CTRL06	0x00	RW	ISP Control 06 (0: disable; 1: enable) Bit[7]: x_odd_inc_man_en Bit[6]: y_even_inc_man_en Bit[5]: x_odd_inc_man_en Bit[4]: y_even_inc_man_en Bit[3]: x_offset_man_en Bit[2]: y_offset_man_en Bit[1]: x_skip_man_en Bit[0]: y_skip_man_en

table 7-12 ISP control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x5007	ISP CTRL07	0x00	RW	ISP Control 07 (0: disable; 1: enable) Bit[7]: bin_mode_man_en Bit[6]: bin_mode_man Bit[5]: win_x_off_man_en Bit[4]: win_y_off_man_en Bit[3]: win_x_out_man_en Bit[2]: win_y_out_man_en Bit[1]: isp_input_h_man_en Bit[0]: isp_input_v_man_en
0x5008	X OFFSET MAN	0x00	RW	Bit[7:4]: Not used Bit[3:0]: x_offset_man[11:8]
0x5009	X OFFSET MAN	0x00	RW	Bit[7:0]: x_offset_man[7:0]
0x500A	Y OFFSET MAN	0x00	RW	Bit[7:3]: Not used Bit[2:0]: y_offset_man[10:8]
0x500B	Y OFFSET MAN	0x00	RW	Bit[7:0]: y_offset_man[7:0]
0x500C	WIN X OFFSET MAN	0x00	RW	Bit[7:4]: Not used Bit[3:0]: win_x_offset_man[11:8]
0x500D	WIN X OFFSET MAN	0x00	RW	Bit[7:0]: win_x_offset_man[7:0]
0x500E	WIN Y OFFSET MAN	0x00	RW	Bit[7:3]: Not used Bit[2:0]: win_y_offset_man[10:8]
0x500F	WIN Y OFFSET MAN	0x00	RW	Bit[7:0]: win_y_offset_man[7:0]
0x5010	WIN X OUT MAN	0x00	RW	Bit[7:4]: Not used Bit[3:0]: win_x_out_man[11:8]
0x5011	WIN X OUT MAN	0x00	RW	Bit[7:0]: win_x_out_man[7:0]
0x5012	WIN Y OUT MAN	0x00	RW	Bit[7:3]: Not used Bit[2:0]: win_y_out_man[10:8]
0x5013	WIN Y OUT MAN	0x00	RW	Bit[7:0]: win_y_out_man[7:0]
0x5014	ISP INPUT X MAN	0x00	RW	Bit[7:4]: Not used Bit[3:0]: isp_x_input_man[11:8]
0x5015	ISP INPUT X MAN	0x00	RW	Bit[7:0]: isp_x_input_man[7:0]
0x5016	ISP INPUT Y MAN	0x00	RW	Bit[7:3]: Not used Bit[2:0]: isp_y_input_man[10:8]
0x5017	ISP INPUT Y MAN	0x00	RW	Bit[7:0]: isp_y_input_man[7:0]
0x5018	ISP CTRL18	0x00	RW	Bit[7:4]: x_odd_inc_man Bit[3:0]: x_even_inc_man
0x5019	ISP CTRL19	0x00	RW	Bit[7:4]: y_odd_inc_man Bit[3:0]: y_even_inc_man

table 7-12 ISP control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x501A	ISP CTRL1A	0x00	RW	Bit[7:4]: Not used Bit[3:2]: x_skip_man Bit[1:0]: y_skip_man
0x501B~ 0x501C	DEBUG MODE	–	–	Debug Mode
0x501D	ISP CTRL1D	0x00	RW	Bit[7]: Not used Bit[6:4]: win_y_offset_adjust Bit[3:0]: Not used
0x501F	ISP CTRL1F	0x03	RW	Bit[7:6]: Not used Bit[5]: enable_opt 0: Not latched by VSYNC 1: Enable latched by VSYNC Bit[4]: cal_sel 0: DPC cal_start using SOF 1: DPC cal_start using VSYNC Bit[3]: Not used Bit[2:0]: fmt_sel 011: ISP output data Others: ISP input data bypass
0x5025	ISP CTRL25	0x00	RW	Bit[7:4]: Not used Bit[1:0]: avg_sel 00: Inputs of AVG module are from LENC output 01: Inputs of AVG module are from AWB gain output 10: Inputs of AVG module are from DPC output 11: Inputs of AVG module are from binning output
0x5026~ 0x503C	DEBUG MODE	–	–	Debug Mode

table 7-12 ISP control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x503D	ISP CTRL3D	0x00	RW	Bit[7]: test_pattern_en 0: Disable 1: Enable Bit[6]: rolling_bar 0: Disable rolling bar 1: Enable rolling bar Bit[5]: transparent_mode 0: Disable 1: Enable Bit[4]: squ_bw_mode 0: Output square is color square 1: Output square is black-white square Bit[3:2]: bar_style When set to a different value, a different type color bar will be output Bit[1:0]: test_pattern_type 00: Color bar 01: Square 10: Random data 11: Input data
0x503E	ISP CTRL3E	0x00	RW	Bit[7]: Not used Bit[6]: win_cut_en Bit[5]: isp_test 0: Two lowest bits are 1 1: Two lowest bits are 0 Bit[4]: Two lowest bits are rnd_same 0: Frame-changing random data pattern 1: Frame-fixed random data pattern Bit[3:0]: rnd_seed Initial seed for random data pattern
0x504B	ISP CTRL4B	0x30	RW	ISP Control 4B (0: disable; 1: enable) Bit[7:6]: Not used Bit[5]: post_binning h_enable Bit[4]: post_binning v_enable Bit[3]: flip_man_en Bit[2]: flip_man Bit[1]: mirror_man_en Bit[0]: Mirror
0x504C	ISP CTRL4C	0x04	RW	Bit[7:0]: bias_man

table 7-12 ISP control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x504D	ISP CTRL4D	0x00	RW	ISP Control 4D (0: disable; 1: enable) Bit[7:4]: Not used Bit[3]: lenc_xoff_man_en Bit[2]: lenc_yoff_man_en Bit[1]: lenc_gain_man_en Bit[0]: lenc_bias_man_en
0x504E	ISP CTRL4E	0x04	RW	Bit[7:4]: Not used Bit[3:0]: lenc_xoff_man[11:8]
0x504F	ISP CTRL4F	0x00	RW	Bit[7:0]: lenc_xoff_man[7:0]
0x5052	ISP CTRL52	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: lenc_yoff_man[11:8]
0x5053	ISP CTRL53	0x00	RW	Bit[7:0]: lenc_yoff_man[7:0]
0x5054	ISP CTRL54	0x00	RW	Bit[7:2]: Not used Bit[1:0]: lenc_gain_man[9:8]
0x5055	ISP CTRL55	0x00	RW	Bit[7:0]: lenc_gain_man[7:0]
0x5056	ISP CTRL56	0x00	RW	Bit[7:6]: Not used Bit[5]: lenc_skipx_man Bit[4]: lenc_skipy_man Bit[3:2]: lenc_skipy_man Bit[1:0]: lenc_skipx_man
0x5057	ISP CTRL57	0x00	RW	Bit[7]: sram_test_dpc1 Bit[6]: sram_test_dpc2 Bit[5]: sram_test_dpc3 Bit[4]: sram_test_dpc4 Bit[3:0]: Not used
0x5058	ISP CTRL58	0xAA	RW	Bit[7:4]: sram_rm_dpc1 Bit[3:0]: sram_rm_dpc2
0x5059	ISP CTRL59	0xAA	RW	Bit[7:4]: sram_rm_dpc3 Bit[3:0]: sram_rm_dpc4

7.13 AWB control [0x5180 - 0x51DF]

table 7-13 AWB registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5180	AWB CTRL	0x00	RW	Bit[7]: hsize_man_en Bit[6]: fast_awb 0: Disable fast AWB calculation function 1: Enable fast AWB calculation function Bit[5]: freeze_gain_en When it is enabled, the output AWB gains are input AWB gains Bit[4]: freeze_sum_en When it is set, the sums and averages value are the same as previous frame Bit[3]: gain_man_en 0: Output calculated gains 1: Output manual gains set by registers Bit[2]: start_sel 0: Select the last HREF falling edge of before gain input as calculated start signal 1: Select the last HREF falling edge of after gain input as calculated start signal Bit[1]: after_gma Bit[0]: Not used
0x5181	AWB DELTA	0x20	RW	Bit[7]: delta_opt Bit[6]: base_man_en Bit[5:0]: awb_delta Delta value to increase or decrease the gains
0x5182	STABLE RANGE	0x04	RW	Bit[7:0]: stable_range
0x5183	STABLE RANGEW	0x08	RW	Bit[7:0]: stable_rangew Wide stable range
0x5184~ 0x5185	AWB CTRL	–	–	Debug Mode
0x5185	HSIZE_MAN	0xE0	RW	Bit[7:0]: hsize_man[7:0]
0x5186	MANUAL RED GAIN MSB	0x04	RW	Bit[7:4]: Not used Bit[3:0]: red_gain_man[11:8]

table 7-13 AWB registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5187	MANUAL RED GAIN LSB	0x00	RW	Bit[7:0]: red_gain_man[7:0]
0x5188	MANUAL GREEN GAIN MSB	0x04	RW	Bit[7:4]: Not used Bit[3:0]: grn_gain_man[11:8]
0x5189	MANUAL GREEN GAIN LSB	0x00	RW	Bit[7:0]: grn_gain_man[7:0]
0x518A	MANUAL BLUE GAIN MSB	0x04	RW	Bit[7:4]: Not used Bit[3:0]: blu_gain_man[11:8]
0x518B	MANUAL BLUE GAIN LSB	0x00	RW	Bit[7:0]: blu_gain_man[7:0]
0x518C	RED GAIN LIMIT	0xF0	RW	Bit[7:4]: red_gain_up_limit Bit[3:0]: red_gain_dn_limit They are only the highest 4 bits of limitation. Maximum red gain is {red_gan_up_limit,FF} Minimum red gain is {red_gain_dn_limit,00}
0x518D	GREEN GAIN LIMIT	0xF0	RW	Bit[7:4]: green_gain_up_limit Bit[3:0]: green_gain_dn_limit They are only the highest 4 bits of limitation. Maximum green gain is {green_gan_up_limit,FF} Minimum green gain is {green_gain_dn_limit,00}
0x518E	BLUE GAIN LIMIT	0xF0	RW	Bit[7:4]: blue_gain_up_limit Bit[3:0]: blue_gain_dn_limit They are only the highest 4 bits of limitation. Maximum blue gain is {blue_gan_up_limit,FF} Minimum blue gain is {blue_gain_dn_limit,00}
0x518F	FRAME CNT	0x00	RW	Bit[7:4]: Not used Bit[3:0]: awb_frame_cnt
0x51DF	BASE MAN	0x10	RW	Bit[7:0]: base_man

7.14 LENC control [0x5800 - 0x5849]

table 7-14 LENC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5800~ 0x5823	GMTRX	–	RW	Bit[7:6]: Not used Bit[5:0]: Green matrix
0x5824~ 0x583C	BRMTRX	–	RW	Bit[7:4]: Blue matrix Bit[3:0]: Red matrix
0x583D	LENC BR OFFSET	0x88	RW	Bit[7:4]: lenc_b_offset Bit[3:0]: lenc_r_offset
0x583E	MAX GAIN	0x40	RW	Bit[7:0]: max_gain
0x583F	MIN GAIN	0x20	RW	Bit[7:0]: min_gain
0x5840	MIN Q	0x18	RW	Bit[6:0]: min_q
0x5841	LENC CTRL59	0x0D	RW	Bit[7:4]: Debug mode Bit[3]: ADDBLC 0: Disable BLC add back function 1: Enable BLC add back function Bit[2]: blc_en 0: Disable BLC function 1: Enable BLC function Bit[1]: gain_man_en Bit[0]: autoq_en 0: Used constant Q (0x40) 1: Used calculated Q
0x5842	BR HSCALE	0x01	RW	Bit[7:4]: Debug mode Bit[3:0]: br_hscale[11:8] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5843	BR HSCALE	0x2B	RW	Bit[7:0]: br_hscale[7:0] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5844	BR VSCALE	0x01	RW	Bit[7:3]: Debug mode Bit[2:0]: br_vscale[10:8] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block

table 7-14 LENC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5845	BR VSCALE	0x8D	RW	Bit[7:0]: br_vscale[7:0] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5846	G HSCALE	0x01	RW	Bit[3:0]: g_hscale[11:8] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5847	G HSCALE	0x8F	RW	Bit[7:0]: g_hscale[7:0] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5848	G VSCALE	0x01	RW	Bit[2:0]: g_vscale[10:8] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5849	G VSCALE	0x09	RW	Bit[7:0]: g_vscale[7:0] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block

7.15 ISP output windows [0x5980 - 0x5988]

table 7-15 ISP output windows registers

address	register name	default value	R/W	description
0x5980	WINDOW XSTART	0x00	RW	Bit[7:5]: Not used Bit[4:0]: window_xstart[12:8]
0x5981	WINDOW XSTART	0x00	RW	Bit[7:0]: window_xstart[7:0]
0x5982	WINDOW YSTART	0x00	RW	Bit[7:4]: Not used Bit[3:0]: window_ystart[11:8]
0x5983	WINDOW YSTART	0x00	RW	Bit[7:0]: window_ystart[7:0]
0x5984	WIN X WIN	0x10	RW	Bit[7:5]: Not used Bit[4:0]: window_x_win[12:8]
0x5985	WIN X WIN	0xA0	RW	Bit[7:0]: window_x_win[7:0]
0x5986	WIN Y WIN	0x0C	RW	Bit[7:4]: Not used Bit[3:0]: window_y_win[11:8]
0x5987	WIN Y WIN	0x78	RW	Bit[7:0]: window_y_win[7:0]
0x5988	WIN MAN	0x00	RW	Bit[7:1]: Not used Bit[0]: Window manual enable 0: Auto mode 1: Manual mode

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		±200 mA

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-30°C to +70°C junction temperature
stable image temperature[b]	0°C to +50°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics (-30°C < T_J < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-DO}	supply voltage (digital I/O)	1.7	1.8	3.0	V
V_{DD-D}	supply voltage (digital core)[a]	1.425	1.5	1.575	V
V_{DD-E}	supply voltage (MIPI)	1.425	1.5	1.575	V
internal DVDD, EVDD short to DVDD, DVP output, AVDD = 2.8V, DOVDD = 2.8V					
I_{DD-A}	active (operating) current 2592 x 1944 @ 15 fps[b]		31	45	mA
I_{DD-DO}			65	85	mA
I_{DD-A}	active (operating) current 1080p @ 30fps		32	45	mA
I_{DD-DO}			60	78	mA
I_{DD-A}	active (operating) current 720p @ 60fps		34	45	mA
I_{DD-DO}			58	75	mA
I_{DD-A}	active (operating) current 720p @ 30fps		34	45	mA
I_{DD-DO}			35	48	mA
I_{DD-A}	active (operating) current VGA @ 60fps		34	45	mA
I_{DD-DO}			32	44	mA
I_{DD-A}	active (operating) current VGA @ 30fps		34	45	mA
I_{DD-DO}			20	28	mA
internal DVDD, EVDD short to DVDD, MIPI output, AVDD = 2.8V, DOVDD = 2.8V					
I_{DD-A}	active (operating) current 2592 x 1944 @ 15 fps[c]		31	45	mA
I_{DD-DO}			60	78	mA
I_{DD-A}	active (operating) current 1080p @ 30fps		32	45	mA
I_{DD-DO}			56	73	mA
I_{DD-A}	active (operating) current 720p @ 60fps		34	45	mA
I_{DD-DO}			56	74	mA
I_{DD-A}	active (operating) current 720p @ 30fps		34	45	mA
I_{DD-DO}			32	44	mA
I_{DD-A}	active (operating) current VGA @ 60fps		34	45	mA
I_{DD-DO}			32	44	mA
I_{DD-A}	active (operating) current VGA @30fps		34	45	mA
I_{DD-DO}			20	28	mA

table 8-3 DC characteristics (-30°C < T_J < 70°C)

symbol	parameter	min	typ	max	unit
standby current					
$I_{DDS-SCCB}$[d]	standby current[e]		20	50	µA
$I_{DDS-PWDN}$			20	50	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}[f]	output voltage HIGH	1.62			V
V_{OL}[f]	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[f]	SCL and SDA	-0.5	0	0.54	V
V_{IH}[f]	SCL and SDA	1.26	1.8	2.3	V

a. when internal regulator is bypassed

b. using internal regulator for DVDD and short DVDD with EVDD; DOVDD = 2.8V. The currents are for DVP output. MIPI output will results 5%-10% lower active current on I_{DD-DO}

c. using internal regulator for DVDD and short DVDD with EVDD; DOVDD = 2.8V. The currents are for DVP output. MIPI output will results 5%-10% lower active current on I_{DD-DO}

d. external clock is stopped during measurement

e. standby current is based on room temperature

f. based on DOVDD = 1.8V

8.4 AC characteristics

table 8-4 timing characteristics

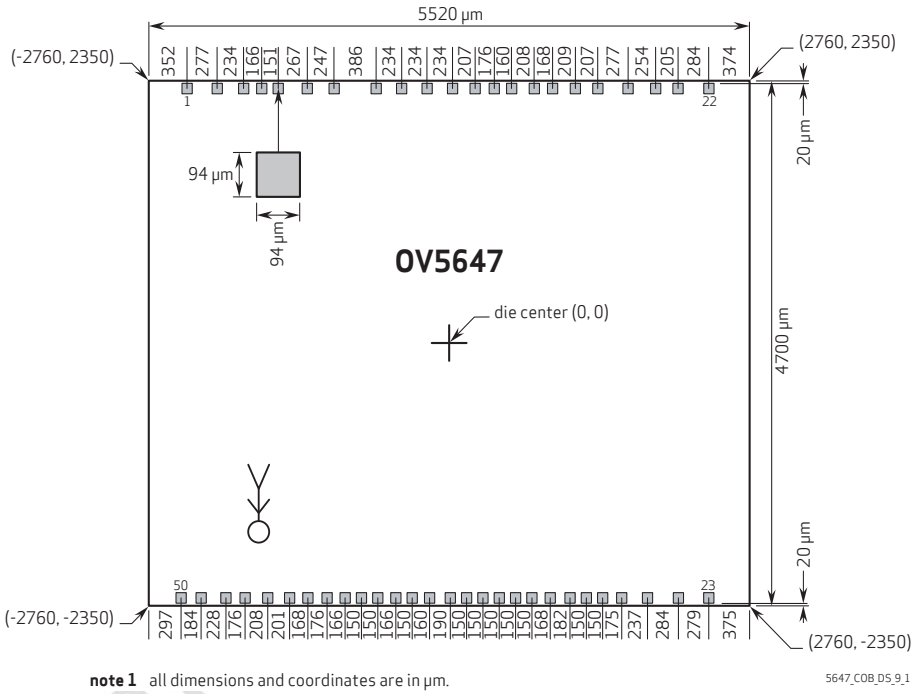
symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XCLK)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns

a. if using the internal PLL

9 mechanical specifications

9.1 physical specifications

figure 9-1 die specifications



note 1 all dimensions and coordinates are in µm.

table 9-1 pad location coordinates (sheet 1 of 3)

pad number	pad name	x coordinate	y coordinate	x pitch	y pitch	pad size
1	AVDD	-2408	2280			94x94
2	AGND	-2131	2280	277	–	94x94
3	DOGND	-1888	2280	243	–	94x94
4	SCL	-1722	2280	166	–	94x94
5	SDA	-1571	2280	151	–	94x94
6	DVDD	-1304	2280	267	–	94x94
7	SGND	-1057	2280	247	–	94x94
8	GPIO1	-671	2280	386	–	94x94

table 9-1 pad location coordinates (sheet 2 of 3)

pad number	pad name	x coordinate	y coordinate	x pitch	y pitch	pad size
9	GPIO0	-437	2280	234	–	94x94
10	STROBE	-203	2280	234	–	94x94
11	FREX	31	2280	234	–	94x94
12	DOVDD	238	2280	207	–	94x94
13	VREF2	414	2280	176	–	94x94
14	VREF1	574	2280	160	–	94x94
15	PWDN	782	2280	208	–	94x94
16	DVDD	950	2280	168	–	94x94
17	RESETB	1159	2280	209	–	94x94
18	AVDD	1366	2280	207	–	94x94
19	AGND	1643	2280	277	–	94x94
20	TM	1897	2280	254	–	94x94
21	DOGND	2102	2280	205	–	94x94
22	DVDD	2386	2280	284	–	94x94
23	DVDD	2385	-2280	-1	-4560	94x94
24	DOVDD	2106	-2280	-279	–	94x94
25	DOGND	1822	-2280	-284	–	94x94
26	AVDD	1585	-2280	-237	–	94x94
27	HREF	1410	-2280	-175	–	94x94
28	PCLK	1260	-2280	-150	–	94x94
29	VSYNC	1110	-2280	-150	–	94x94
30	DOVDD	928	-2280	-182	–	94x94
31	D0	760	-2280	-168	–	94x94
32	D1	610	-2280	-150	–	94x94
33	D2	460	-2280	-150	–	94x94
34	D3	310	-2280	-150	–	94x94
35	D9/MDN0	160	-2280	-150	–	94x94
36	D8/MDP0	10	-2280	-150	–	94x94
37	EVDD	-180	-2280	-190	–	94x94
38	D7/MCN	-340	-2280	-160	–	94x94

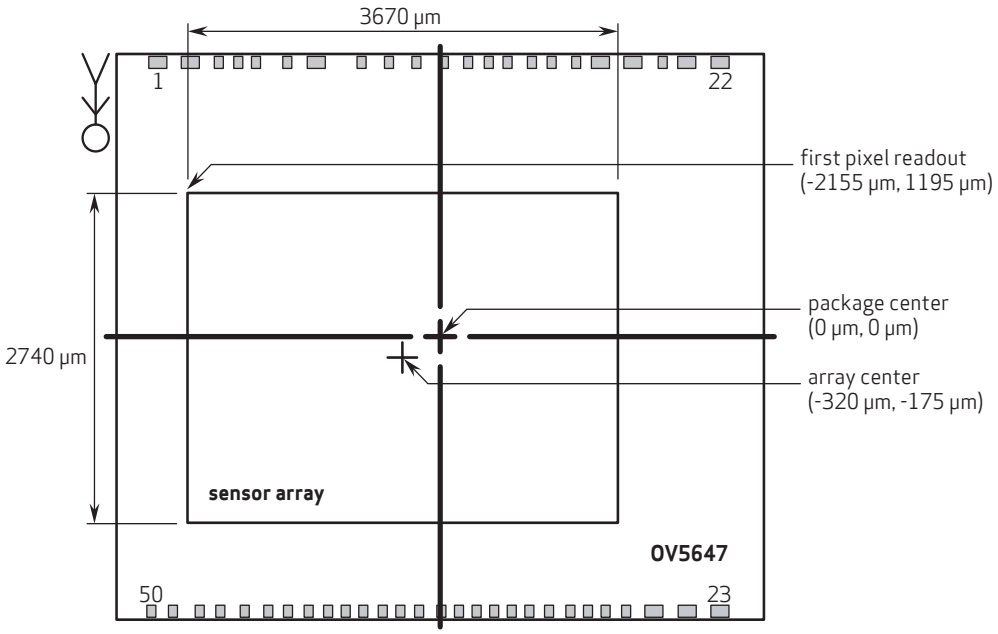
table 9-1 pad location coordinates (sheet 3 of 3)

pad number	pad name	x coordinate	y coordinate	x pitch	y pitch	pad size
39	D6/MCP	-490	-2280	-150	–	94x94
40	EGND	-656	-2280	-166	–	94x94
41	D5/MDN1	-806	-2280	-150	–	94x94
42	D4/MDP1	-956	-2280	-150	–	94x94
43	EGND	-1122	-2280	-166	–	94x94
44	PVDD	-1298	-2280	-176	–	94x94
45	XCLK	-1466	-2280	-168	–	94x94
46	DOVDD	-1667	-2280	-201	–	94x94
47	DVDD	-1875	-2280	-208	–	94x94
48	DOGND	-2051	-2280	-176	–	94x94
49	AVDD	-2279	-2280	-228	–	94x94
50	AGND	-2463	-2280	-184	–	94x94

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pad 1 oriented down on the PCB.

5647_COB_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

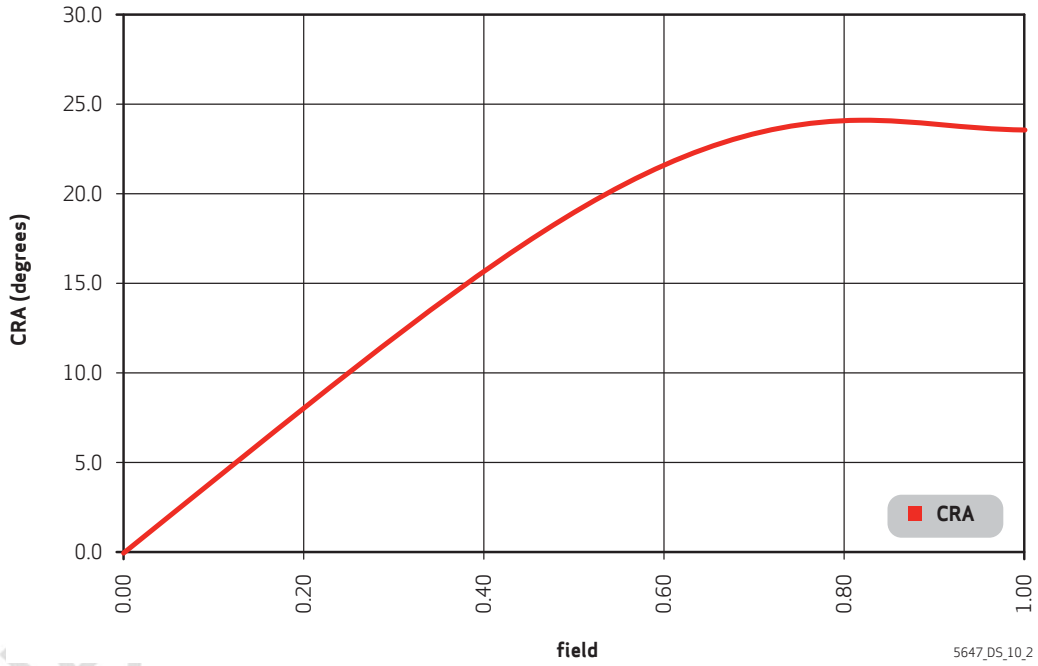


table 10-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0.00	0.000	0.0
0.05	0.114	2.0
0.10	0.227	4.1
0.15	0.341	6.1
0.20	0.454	8.1
0.25	0.568	10.1
0.30	0.681	12.0
0.35	0.795	13.8
0.40	0.908	15.6
0.45	1.022	17.3
0.50	1.135	18.9

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.55	1.249	20.4
0.60	1.362	21.6
0.65	1.476	22.6
0.70	1.589	23.4
0.75	1.703	23.9
0.80	1.816	24.1
0.85	1.930	24.1
0.90	2.043	23.9
0.95	2.157	23.7
1.00	2.270	23.6

appendix A handling of RW devices

A.1 ESD /EOS prevention

1. Ensure that there is 500V ESD control in all work areas.
2. Use ESD safety shoes, ground strap, and static control smocks in test areas.
3. Use grounded work carts and tables in inspection areas.
4. OmniVision recommends the use of ionized air in all work areas.

A.2 particles and cleanliness of environment

1. All production, inspection and packaging areas should meet Class10 environment requirements.
2. Use optical microscopes with 50X and 100X magnifications for particle inspection.
3. Ensure that there is good cassette sealing for particle protection during storage.
4. OmniVision recommends air blowing to remove removable particles.
5. RW die should be stored in nitrogen gas purged cabinets with temperature less than 30°C and relative humidity of 60% before assembly.

A.3 other requirements

1. Reliability assurance of RW or COB bare die is certified by product reliability of the bare die in a CLCC, CSP or QFP package form factor. Precautions should be taken if the packaging form factor of the bare die is other than these specified.
2. Avoid exposure to strong sunlight for extended periods of time as the color filter of the image sensor may become discolored.
3. Avoid direct exposure of the sensor bare die to high temperature and/or humidity environment as sensor characteristics will be affected. Extra precautions should be exercised if the bare die experiences temperatures exceeding 260°C for more than 75 seconds.

revision history

version 1.0 11.03.2009

- initial release

version 1.1 04.05.2010

- in chapter 1, updated VREF2 description from "reference analog circuit (connect to 0.1uF capacitor to ground)" changed to reference analog circuit (connect to 1 µF capacitor to ground)"
- in chapter 2, updated figure 2-2 reference design schematic
- in chapter 2, updated table 2-1 format and frame rate; update all pixel clock values
- in chapter 4, updated the following registers in table 4-5 AEC/AGC control functions: 0x3501, 00x3502, 0x3503, 0x350B, 0x350C, 0x350D
- in chapter 4, updated the overview for section 4.5.3 average luminance (YAVG)
- in chapter 4, updated entire section 4.10 frame exposure (FREX) mode
- in chapter 5, updated the overview for section 5.2 lens correction (LENC)
- in chapter 6, updated the entire table 6-8 DVP specifications
- in chapter 7, updated the following registers: 0x3000, 0x3001, 0x3002, 0x3008, 0x3009, 0x300A, 0x300B, 0x300D, 0x300E, 0x300F, 0x3010, 0x3011, 0x3018, 0x3035, 0x3501, 0x3502, 0x3503, 0x350C (removed), 0x350D (removed), 0x3800, 0x3802, 0x3804, 0x3806, 0x3808, 0x380A, 0x380C, 0x380E, 0x380F, 0x3810, 0x3812, 0x3816, 0x3818
- in chapter 9, updated figure 9-1 and table 9-1 pad location coordinates

version 1.2 06.24.2010

- in the key specifications section, removed "global shutter"
- in chapter 1, updated table 1-1 signal description "Strobe" to "strobe"
- in chapter 1, added to table 1-1 signal description default status column
- in chapter 1, updated table 1-2 pad configuration under various conditions
- in chapter 2, updated figure 2-2 reference design schematic
- in chapter 4, updated table 4-1 mirror flip control registers from:

0x3820	TIMING_TC_REG20	0x40	RW	Timing Control Bit[2]: r_vflip_isp Bit[1]: r_vflip_snr
0x3821	TIMING_TC_REG21	0x00	RW	Timing Control Bit[2]: r_mirror_isp Bit[1]: r_mirror_snr

changed to

0x3820	TIMING_TC_REG20	0x40	RW	Timing Control Bit[2]: ISP vertical flip Bit[1]: Sensor vertical flip
0x3821	TIMING_TC_REG21	0x00	RW	Timing Control Bit[2]: ISP mirror Bit[1]: Sensor mirror

- in chapter 4, updated table 4-5 AEC/AGC control function registers
- in chapter 4, updated section 4.7 black level calibration and table 4-8 BLC control functions
- in chapter 4, updated figure 4-15 FREX mode 2 timing diagram (when shutter delay is longer than exposure time
- in chapter 4, updated 4-17 Strobe control in FREX mode
- in chapter 4, updated table 4-11 FREX strobe control functions register 0x3B00 and 0x3B07
- in chapter 5, updated table 5-4 AWB control registers changed register 0x5001 and added 0x50020
- in chapter 6, updated all values for table 6-1 system control registers
- in chapter 6, removed section 6.5 strobe
- in chapter 7, in table 7-1 system control registers; updated the following registers: 0x3008, 0x3009, 0x300E, 0x3011, 0x302A, 0x3034, 0x3500, 0x3501, 0x3502, 0x350A, 0x380E, 0x3820, 0x3821, 0x3A00, 0x3A02, 0x3A03, 0x3A08, 0x3A09, 0x3A0A, 0x3A0D, 0x3A0E, 0x3A14, 0x3A15, 0x3A17, 0x3A18, 0x3A19, 0x3B07, 0x4000~0x4067
- added appendix A

version 2.0 11.19.2010

- changed document from Preliminary Specification to Product Specification
- under key specifications on page iii, changed power requirements active and standby from "TBD" to "96, 20"
- under key specifications on page iii, added "max" to S/N ratio and changed from "TBD" to "34 dB"
- under key specifications on page iii, changed dynamic range from "TBD" to "67 dB@8xgain"
- under key specifications on page iii, changed sensitivity from "TBD" to "600mV/Lux-sec"
- under key specifications on page iii, removed well capacity and fixed pattern noise (FPN)
- under key specifications on page iii, changed dark current from "TBD" to "8mV/s @ 50°C junction temperature"
- in table 1-1, changed description to "connect to ground via..." for DVDD, VREF1, VREF2,
- in table 1-1, changed pin type to "ground" for DOGND, AGND, SGND, and EGND
- in table 1-2, removed "Some customer assume" from note a
- in section 2, updated figure 2-2, 2-1 and removed "For customized.." from last sentence of section 2.1
- in table 2-1, changed pixel clock values from 79.7 to 96, 81.6 to 96, 83.6 to 96, 84.3 to 96, 83.5 to 48, and 81.1 to 24
- in sub-sections 2.5.1 and 2.5.2 changed "if" to "when", "V_{DD-IO} to DOVDD", "V_{DD-A}" to "AVDD", "SCCB" to registers", removed "at the same", updated figures 2-3 and 2-4
- in section 2.7, changed section title to hardware and software standby, bullet "SCCB software sleep" to "software standby" and "sleep" to "standby" in the body text
- in sub-section 2.8.5, removed the last sentence and 0x320D~0x320F from table 2-4
- in section 2.7, added sentence, "While in MIPI mode,..."
- in section 2, added section 2.8
- in table 2-4, changed table title to "group hold registers"
- in section 3.2, removed "Sub-sampling is..."
- in section 3.4 removed "It can operate at up to 27 MHz..." and added "and resolution"

- in section 4.12, removed "a maximum"
- in table 4-13, added footnotes a and b
- in section 5, removed registers 0x5780~0x5791 and 0x5184~0x5185
- in section 5.2, updated paragraph by changing "imperfection" to "fall off", "the area where..." to "the distance of each...", removed "to compensate..."
- in section 5.4, updated paragraph by moving "in different color.." to after "...appear white in person", removed "Thus, the AWB makes sure..." and "For auto white balance..."
- in section 5.5, changed section title from "function" to "filter", "CFA image subsample" to "Sub-sample in raw...", "suffer" to "cause", "for" to "because" and added "filter" after "Post Binning..."
- in table 6-2, removed registers 0x3100~0x3106
- in section 6.7, removed "uni-directional", "bi-directional", and "The two data lanes have..."
- in table 6-7, added comas where necessary and "where tp = 1 pclk" to each cell in timing column
- in table 6-8, changed register bit description for 0x4800[7:6], 0x4800[1:0], and 0x4801 to "Debug mode"
- in table 6-8, removed registers 0x4803, 0x4804, 0x4806, 0x480A, 0x483A, 0x483C~0x483F, 0x4860~0x4867
- in table 6-8, changed register bit description for 0x4805[3:1] to "Debug mode" and 0x4805[0] to "Not used"
- in section 7, added section titles to each register table, removed table 7-2, moved register 0x3106 to table 7-1, merged tables 7-6, 7-17, and 7-22 to 7-3
- in table 7-9, added footnotes a and b
- in table 7-10, changed bit description for register 0x4001[7:6] to "Debug mode", 0x4001[5:0] to "start_line" and changed default value to "0x00"
- in table 7-10, changed bit description for register 0x4004[7:0] to "black line num" changed default value to "0x08"
- in table 7-11, removed register 0x4203
- in table 7-13, changed bit description for register 0x4800[7:6], 0x4800[1:0], 0x4801[1:0], 0x4803, 0x4804, 0x4805[3:1], 0x4806, 0x4815[6], 0x483A, 0x483D~0x483F to "Debug mode"
- in table 7-13, removed registers 0x4860~0x4867 and "top" from table title
- in section 7, removed table 7-14
- in table 7-15, changed byte for register 0x501F from "010" to "011" and "011" to "others" and removed "TOP" from table title
- in table 7-16, changed bit description for 0x5184~0x5185 to "Debug Mode"
- in section 7, removed table 7-18
- in table 7-19, changed register address for 0x5800~0x5023 to 0x5800~0x5823 and 0x5824~0x503C and 0x5824~0x583C
- in section 7, removed table 7-20 and added "ISP output" to table title for table 7-22
- in table 7-22, changed register description for register 0x5A00[7:4] to "Not used", 0x5A00[3] to "Debug mode", 0x5A00[1] to "dig_comp_man_opt", 0x5A00[0] to "dig_comp_man_en", 0x5A20[0] to "gainc_sensorgain_man[8]", 0x5A21[7:0] to "gainc_sensorgain[7:0]", 0x5A22[1:0] to "gainc_dgc_man", 0x5A23[9:8] to "gainc_dgc_man[7:0]", 0x5A24[2] to "Debug mode"
- in table 7-22, changed register name from "SNR" to "SENSOR" for 0x5A20 and 0x5A21
- in table 7-22, changed register name from "GAIN" to "COMP" for 0x5A22 and 0x5A23

- in table 8-3, replaced TBDs, added sections for DVP and MIPI outputs, added note e to V_{OH}, V_{OL} and changed note d to note e for V_{IH}
- in section 8.4, removed table 8-4
- added appendix A

version 2.01 12.07.2010

- in the key specifications section, added "junction temperature" to temperature range
- in chapter 8, added "junction temperature" to table 8-2 functional temperature
- added appendix A

version 2.02 04.11.2011

- in chapter 8, updated table 8-3 title to DC characteristics (-30°C < T_J < 70°C) and added table footnote c, standby current is based on room temperature
- added appendix A

version 2.03 05.26.2011

- in chapter 3, replaced figure 3-2
- in chapter 4, updated table 4-5 AEC/AGC control function register 0x3502 description
- in chapter 7, updated table 7-3 AEC/AGC register 0x3502 description

version 2.04 07.29.2011

- replaced paragraph in section 6.7

the clear advantage™

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