Imperial College
London

MSC ADIC LAB
DIGITAL SYSTEM DESIGN

V1.0 – Christos Bouganis

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Requirements to complete this coursework:

Vivado 2014.2;

Xilinx SDK 2014.2;

Vivado HLS;

ZedBoard (Zynq system);

Coursework source files including Xilinx tutorial documentation;

On-line references from Xilinx.

Legend:

 Important information.

 Reference material that you should read before proceeding.

 Work you should deliver. A set of tasks for you to do, and deliverables to include in your report.

 Debug hints

 Helpful information

Please read this document carefully before starting the coursework as it will guide you to complete the coursework efficiently. There are links to references that explain, and exemplify, procedures you will need to know how to do. You're advised to read and understand them.

INTRODUCTION

In this coursework you will acquire experience in the design of digital systems. As a case study, we will focus on the design of a SoC system (i.e. processor + accelerator), and we will see how to integrate an IP (i.e. accelerator) in your CPU-centric system.

The system design will target a Field-Programmable Gate Array (FPGA) from Xilinx. It is a generic programmable digital device that supports the implementation of any digital hardware design after its fabrication. The FPGA board that you're going to use is the ZedBoard that contains the Zynq-7000 All Programmable SoC, a SoC that contains a hard ARM processor and FPGA fabric. More information about ZedBoard can be found here:

http://zedboard.org

The main application for the configuration of the FPGA is Vivado from Xilinx. It allows to design and program digital systems based on FPGAs. The ARM processor can be coded using Xilinx SDK.

The coursework is structured in two parts and it will be completed in two 3 hour sessions.

- Part 1. In the first part of the coursework you will become familiar with designing a Zynq-based system. You will learn how to instantiate such a system in the FPGA, how to program it, and how to control a basic peripheral of the board (i.e. LEDs)
- Part 2. In this part, you will learn how to add extra modules (IPs) on the FPGA fabric and instantiate an appropriate interface to access them. You will become familiar with interfacing IPs that have been designed using VHDL and Vivado HLS.

In order to get a better view of the project, it is advisable to get some background on the Zynq processor. Read Chapters 1 to 3 from the "The Zynq Book". If you want, you can read chapters 4 and 5 of the same book that focus on the performance of the Zynq processor and its applications. Finally, Chapter 6 introduces the Zedboard.

Part 1: Introduction to a Zynq system

In this task you will get familiar with the design of a Zynq system and how you can interface your ARM core with HW modules that reside in the FPGA fabric.

This part of the coursework is based on Exercise 1 of "The Zynq Book Tutorials" book. An overview of the exercise is given in Chapter 8 of "The Zynq book". In this exercise you will learn how to create a Zynq system in Vivado and how to write a small software application that runs on the system.

Perform Exercise 1 of "The Zynq Book Tutorials" (1-A to 1-C).

Alter the SW code so the system counts up. Report the resources used by your system (This is in the Project Summary under utilisation). Does your system have any timing violations?

Extend the code by adding a SW function that calculates the following function f(N) and displays the result in binary using the LEDs as well as it prints the value on a terminal.

$$f(N) = \sum_{i=1}^{N} i$$

☺ Good to know: A good tutorial in how you can debug your code is given in VivadoHelloWorldTutorial.pdf.

☺ Good to know: In order to print to a terminal please do the following. Within Xilinx SDK, click on Window->Show View->Terminal. This will open a terminal, but it will not be connected to your system. In order to connect it, click on the Terminal, click on the Settings (yellow icon) and select:

Connection Type: Serial, Baud Rate 115200, Data Bits: 8, Stop Bits: 1, Parity: None, Flow Control: None.

For the port, you need to go to the *Device and Printers* of your Windows system and check to which port the USB Serial Port has been connected to. Click OK.

When you run your code, the printf statements should appear on the terminal.

Part 2: IP creation and Integration with the ARM

In this task you will learn how to integrate an IP core (designed in VHDL or Vivado HLS) to the rest of the system. You have seen a basic example of the above process when you drive the LEDs, but here we consider something more complex.

This part of the coursework is based on Exercise 4 of "The Zynq Book Tutorials" book.

When HLD is used to create your module, you start from an AXI-lite interface wrapper template and then you add your indented functionality. Finally, you package the resulting IP core as IP integrator compatible so it can be used by the Xilinx design tool flow.

🛠 Perform Exercise 4-A of "The Zynq Book Tutorials".

🛠 Modify the IP core in order to present to the LEDs the inverted value (bit-wise) of the value that is sent to the IP core.

🛠 Modify the IP core so it performs addition of two fixed-point numbers and present the result to the LEDs.

You will focus now on the process that needs to be followed when you want to add as an IP core a design that has been implemented using Vivado HLS. This part is based on Exercise 4-C of the "The Zynq Book Tutorials". In summary, you will learn how to specify the necessary interfaces through Vivado HLS for integration with the Zynq system. Please note that Vivado HLS is treated as a black box here.

🛠 Perform Exercise 4-C of "The Zynq Book Tutorials".

Finally, you need to be able to use the IP core that has been designed in the previous step using Vivado HLS. This is explained in Exercise 5-A from the "The Zynq Book Tutorials".

🛠 Perform Exercise 5-A of "The Zynq Book Tutorials".

ASSESMENT AND MARKING SCHEME

The two parts of the lab carry equal weight. You will be assessed on your understanding of the material based on a short interview that will take place during the lab as well as on the tasks that you have performed.

Part	**Mark**
Part 1: Introduction to Zynq	50 %
Part 2: Introduction to Vivado HLS	50 %

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