DAC Top level cell

DAC\_CORE Capacitor array

DFF D-type flip-flop

DFF\_N D-type flip-flop with inverted clock

INV Inverter

NAND NAND

opamp 2-stage operational amplifier

REF Reference voltages

RingOsc Ring oscillator

SR\_N Shift register with inverted clock

SW NANDs for pull inputs low during resetting

TB\_DAC DAC test cell

test\_DAC DAC test bench

Figure 1: Top level schematic

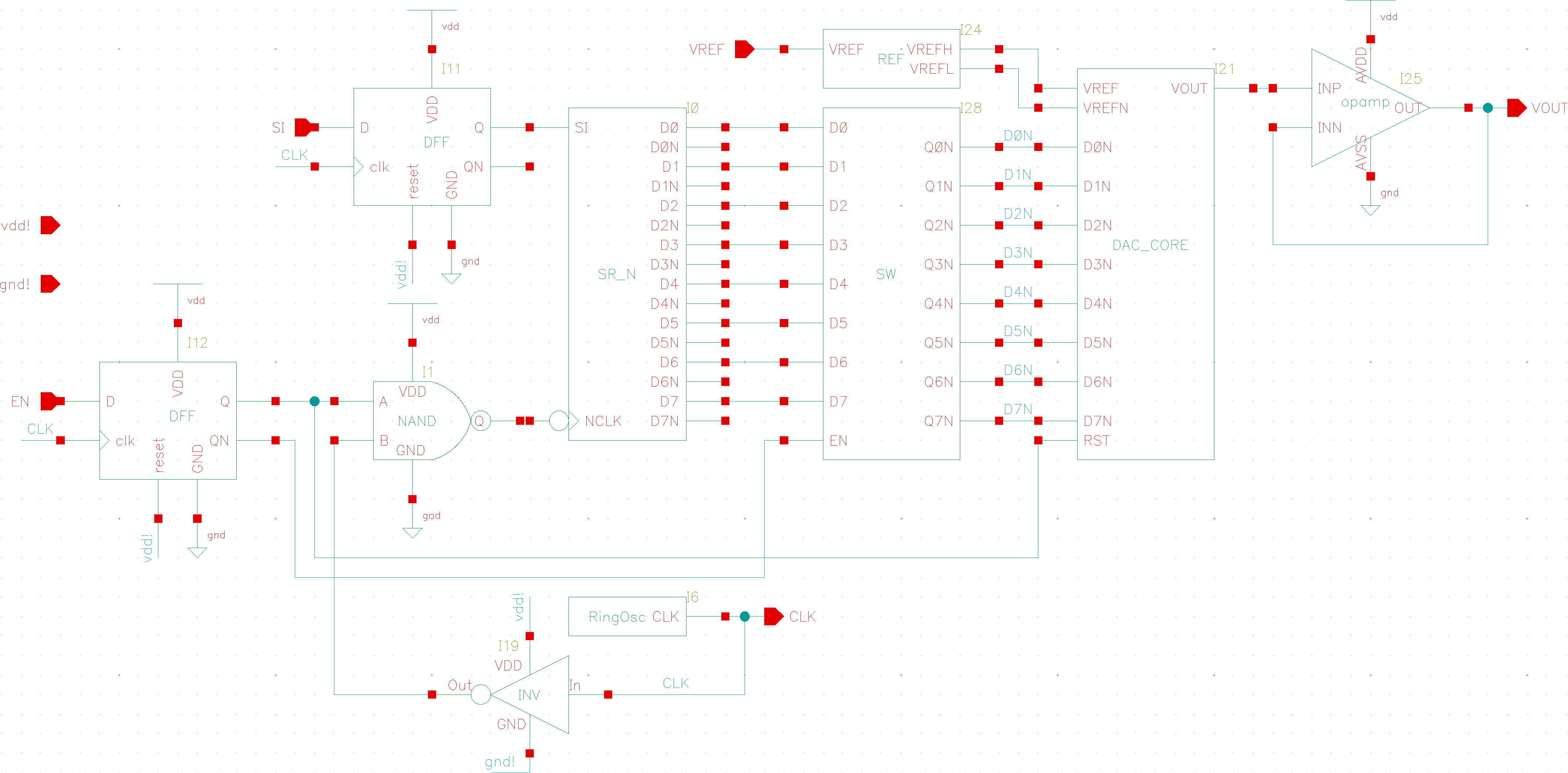


Figure 2: Capacitor array

