

# EEE103 Lab – Digital Electronics

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## Abstract

Digital electronics including logic gates, combinational logic circuit, half adders, flip-flops, timers, counters, and a shift register are the most important part in electronic study. This experiment aims to make students understand the basic feature of different kinds of logic gates and apply them as half adders, flip-flops, timers, counters, and a shift register. The procedures of the experiment are usually divided into three steps; first, set up the circuit; next, vary the inputs to obtain all the possible combinations; finally, complete a truth table. In conclusion, logic gates have various applications such as half adders, flip-flops, timers, counters, and a shift register. In short, logic gates are the most important and fundamental devices which helps student learn more about electricity.

## 1. Introduction

The logic gates are the most fundamental devices in the digital electronics and can be combine together for different objective. In this experiment, the applications of combinational logic circuit as half adders, flip-flops, timers, counters, and shift registers will be focused and analyzed. The working principles and the purposes of these applications will also be analyzed.

The equipment we used are: A dc voltage supply, Multimetre, Collect hook-up wire and ICs from demonstrator (74LS00 × 1, 74LS02 × 1, 74LS04 × 1, 74LS08 × 1, 74LS32 × 1, 74LS86 × 1, 74LS74 × 2, 74LS112 × 2, 330Ω × 4, LED × 4 )

This report will firstly provide an introduction part and then experimental procedure with results will follow up. The conclusion will be given at the end of the report.

## 2. Experimental Procedure

### Section 1. Test of Basic Logic Gates

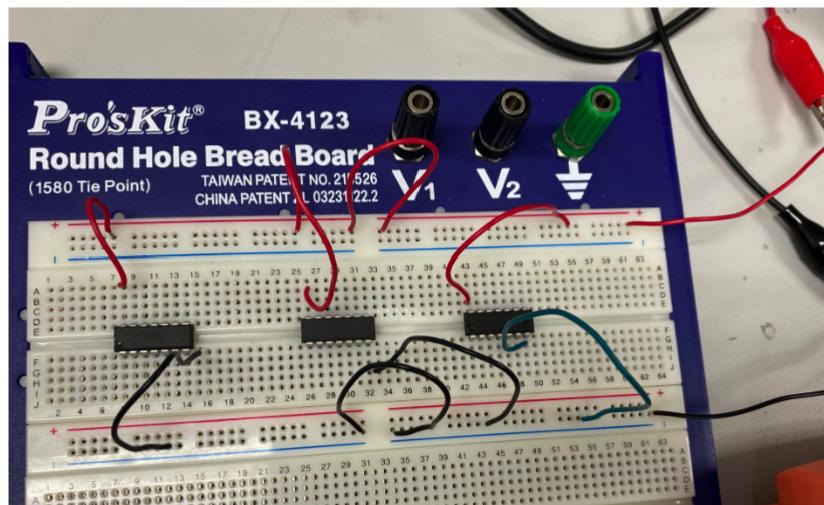


Fig. 1 The circuit for section1

First, the circuit with three basic logic gates (NOT, AND, NOR) should be constructed as shown in the above figure. And then we varied the input A (and input B) by changing the connection from it to the Vcc or ground following the truth table. The output F was measured by a digital voltmeter with exact value recorded.

### Results:

(a) The truth table and the exact voltage of the output F for NOT gate is shown below.

A	F	The exact voltage of the output F
0	1	4.74V
1	0	0.05V

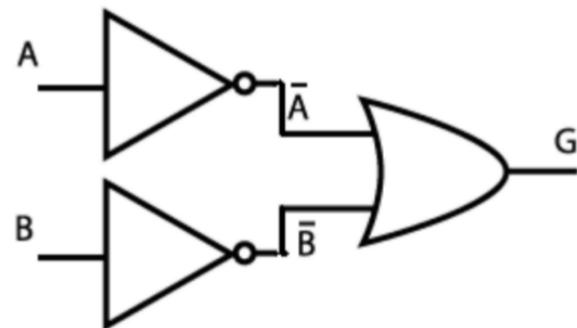
(b) The truth table for AND gate is shown below.

A	B	F	The exact voltage of the output F
0	0	0	0.02V
0	1	0	0.01V
1	0	0	0.01V
1	1	1	4.55V

(c) The truth table for NOR gate is shown below.

A	B	F	The exact voltage of the output F
0	0	1	5.02V
0	1	0	0.01V
1	0	0	0.01V
1	1	0	0.01V

## Section 2. DeMorgan's Theorem



**Fig. 2** Proving De Morgan's Theorem.

First, the two circuits should be constructed as shown in the above figure. And then we varied the input A and input B by changing the connection from it to the Vcc or ground following the truth table. The output F and G was viewed by the LED connected with the output.

Results:

The truth table is shown below:

A	B	F	G
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

And the situations of LED are shown in figure 3-10.

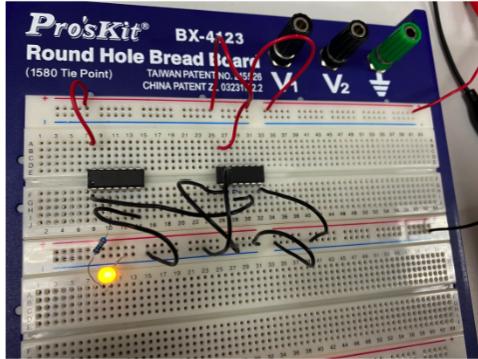


Fig. 3 A=0, B=0, The output of F

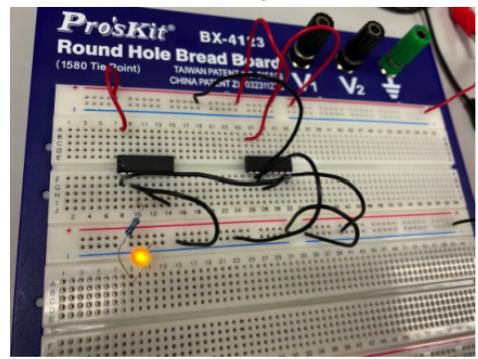


Fig. 4 A=0, B=1, The output of F

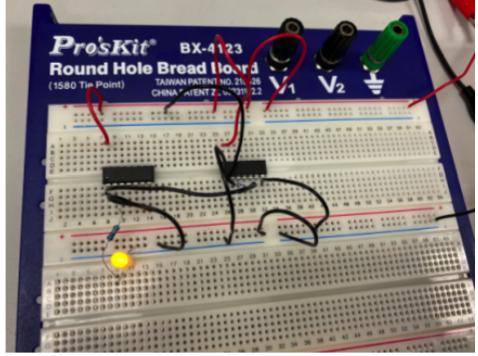


Fig. 5 A=1, B=0, The output of F

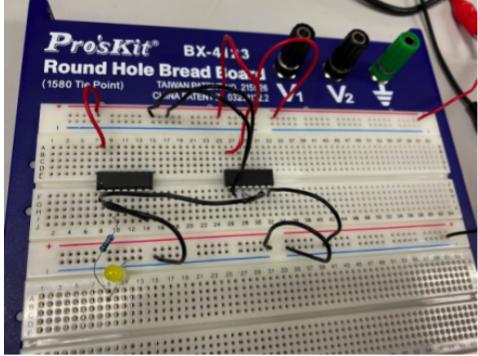


Fig. 6 A=1, B=1, The output of F

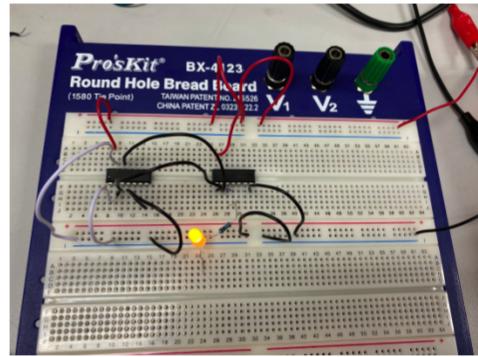


Fig. 7 A=0, B=0, The output of G

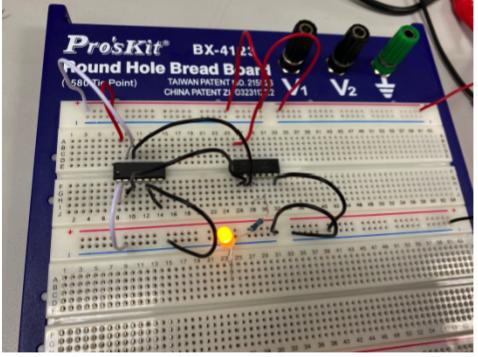


Fig. 8 A=0, B=1, The output of G

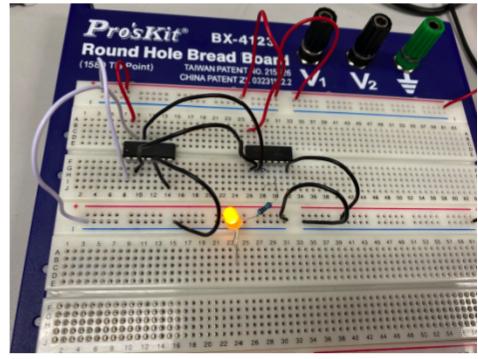


Fig. 9 A=1, B=0, The output of G

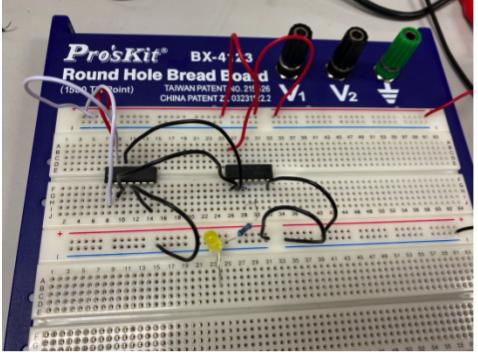


Fig. 10 A=1, B=1, The output of G

The Boolean equation for F is  $\overline{A}^* B$  and the Boolean equation for G is  $\overline{A} + \overline{B}$ .

Moreover,  $\overline{A^*B} = \overline{A} + \overline{B}$ , therefore, the outputs of two different circuits are the same.

### Section 3. Combinational Logic Circuits

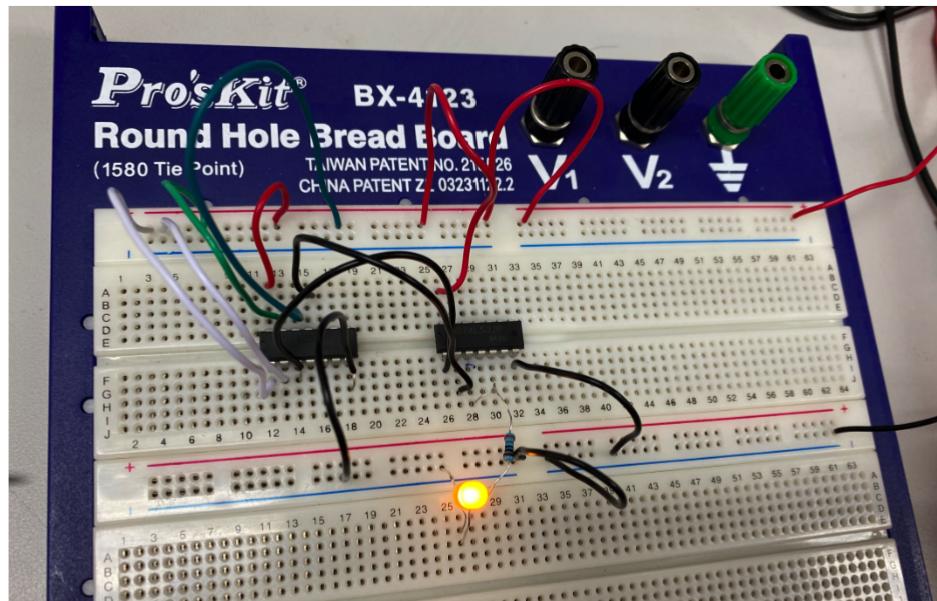


Fig. 11 The circuit for section 3

Since the Boolean equation for the section 3 is  $F = (A + B) * (C + D)$ , the circuit above was built.

And the truth table is shown below.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	1	0	1
1	1	1	1	1

For the real question, only when at least one of Mary's parents gives her permission and at least one of Joe and Tom picks her up can Mary go to the cinema.

#### Section 4. Implementation of a Half Adder

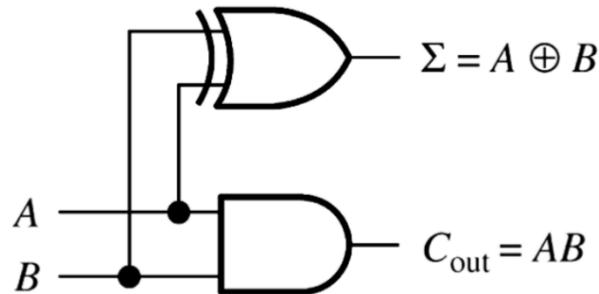


Fig. 12 The Half adder circuit

First, the circuit as shown above was constructed. And then the inputs A and B was varied to obtain all the possible combinations. Finally, the truth table for the sum output  $\Sigma$  and the carry output C was completed.

Results:

(a) The truth table is shown below.

A	B	C	$\Sigma$
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

(b) The half adder is not suitable for all addition operations for the reason that the half adder does not consider the low-order carry, and the full adder considers the low-order carry, so the full adder can calculate more binary additions.

#### Section 5. The S-R Latch

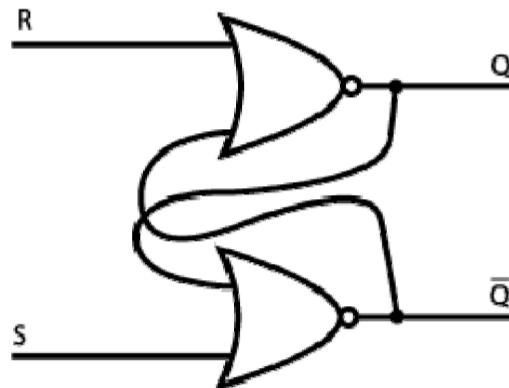
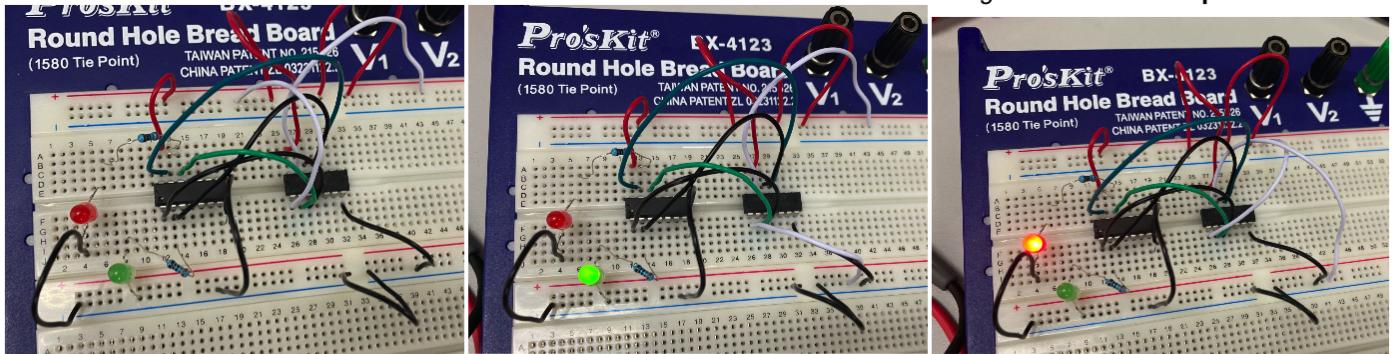


Fig. 13 An S-R latch created using NOR gates

First, the circuit as shown above was constructed. And then the inputs R and S was varied to obtain all the possible combinations. Finally, the truth table for the output Q and  $\bar{Q}$  was completed.

Results:



(b) The truth table is shown below.

$Q_n$	$/Q_n$	R	S	$Q_{n+1}$	$/Q_{n+1}$
0	1	0	0	0	1
1	0	0	0	1	0
0	1	0	1	1	0
1	0	0	1	1	0
0	1	1	0	0	1
1	0	1	0	0	1
0	1	1	1	0	0
1	0	1	1	0	0

(c) The working principles of the S-R latch:

When the output Q is HIGH,  $\bar{Q}$  is LOW, the latch is in the SET state. When R is LOW and S is HIGH, the output of gate G2 is forced HIGH. And then the input gate G1 is HIGH. Therefore, the  $\bar{Q}$  remains HIGH even when R is HIGH. When the output Q is LOW, the latch is in the RESET state until a momentary LOW is applied to the input S.

In conclusion, when S and R is both HIGH, there is no change to the latch and the latch remains in present state. When S is LOW and R is HIGH, latch SET (stores a 1). When S is HIGH and R is LOW, latch RESET (stores a 0). When both S and R is LOW, the latch loses its function.

## Section 6. The Edge-Triggered D Flip-Flop

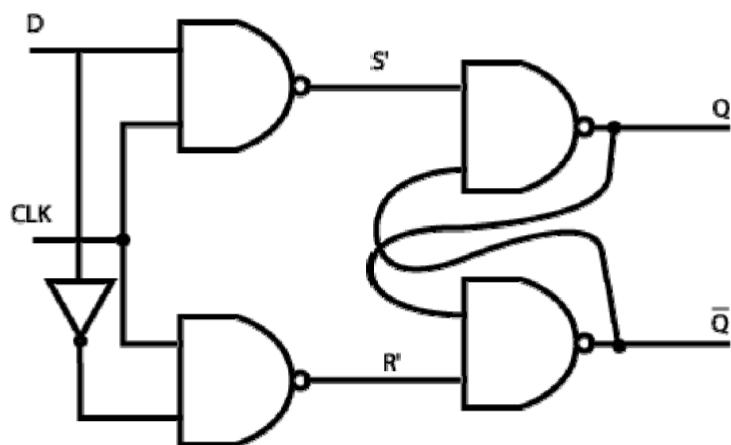
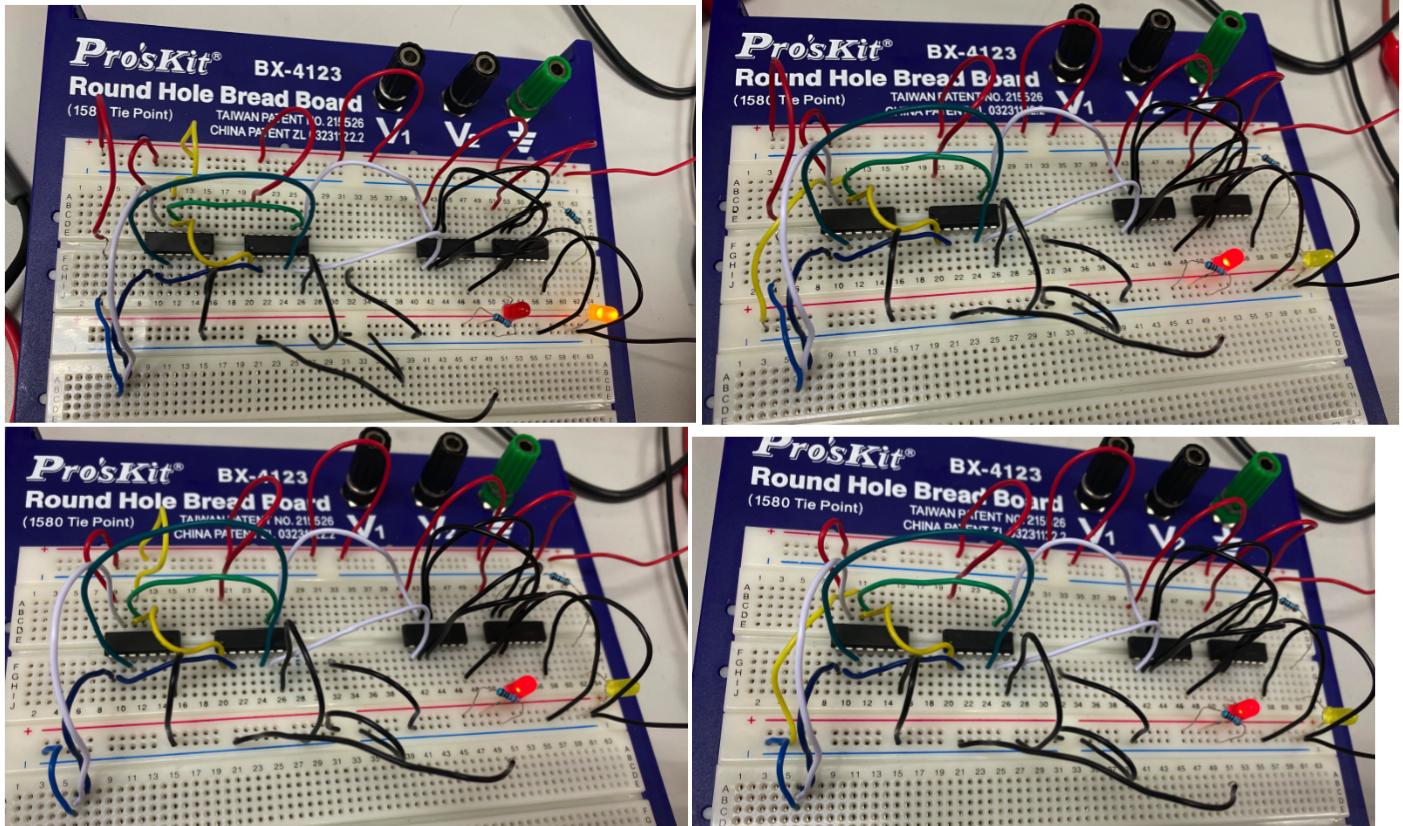


Fig. 14 The D-type flip-flop

First, the circuit shown above was constructed. And then the input D and CLK was varied from low to high and back to low. Finally, the truth table was completed.

Results:



(b) The truth table is shown below.

$Q_n$	$/Q_n$	$D$	$Q_{n+1}$	$/Q_{n+1}$
0	1	0	0	1
1	0	0	0	1
0	1	1	1	0
1	0	1	1	0

The output is followed by the state of D, when D is LOW, the output Q is LOW; when D is HIGH, the output Q is HIGH. The D-type flip-flop can be used to store a single data since the input D can be stored in it.

## Section 7. The Asynchronous Counter

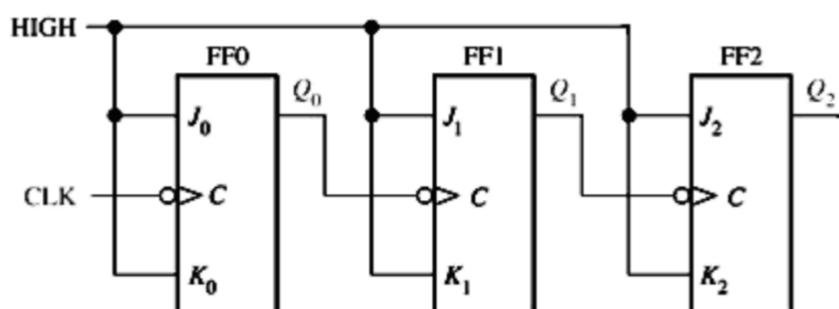
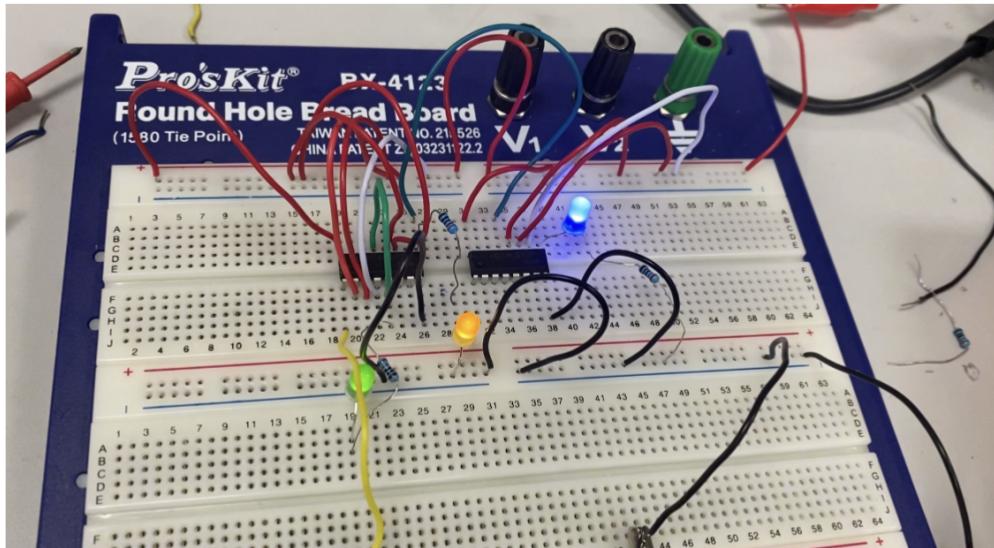


Fig. 15 The Asynchronous Counter

First, the circuit as shown above is constructed. And then we reset the J-K flip-flops, and applied the 2 Hz clock pulse, 5V magnitude, 2.5V offset. Finally, we measured the output at outputs Q1, Q2, Q3 and completed the table.

**Result:**

The circuit is shown below:



The results we obtained is shown below.

	Q0	Q1	Q2
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1
7	0	1	1
8	1	1	1
9	0	0	0
10	1	0	0

(c) This counter have 8 states for a 3-Bit flip-flops.

The working principle of the circuit is that asynchronously set 0 terminal C plus a negative pulse, each flip-flop is in the 0 state, in the counting process, the Q0 bit is high. As long as the low flip-flop flips from the 1 state to the 0 state and the adjacent high flip-flop receives a valid trigger edge, the state of Q flips.

It is called asynchronous counter because some flip-flops are directly controlled by the input count pulse, and some flip-flops use the output signal of other flip-flops as their own clock pulse. Therefore, the time of each flip-flop state change is different, so it is called "asynchronous counter".

## Section 8. The Shift Register

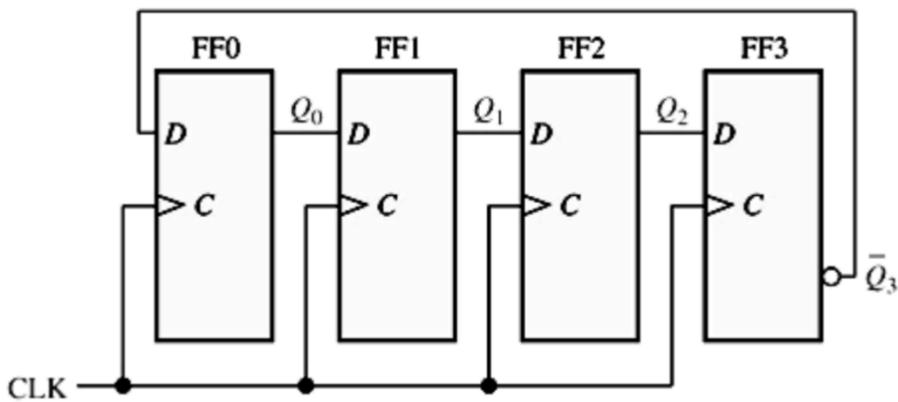


Fig. 16 The 4-bit shift register

First, the circuit shown above is constructed. And then we applied 2 Hz clock pulse to the terminal C.

Results:

The results are as shown below:

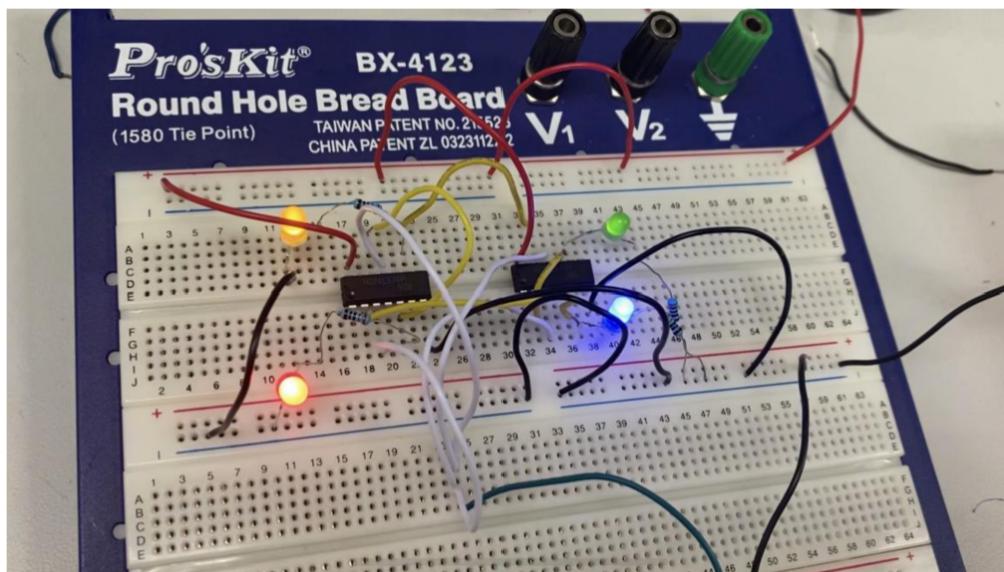


Fig. 17 The results of the section 8

The process of the circuit is shown below.

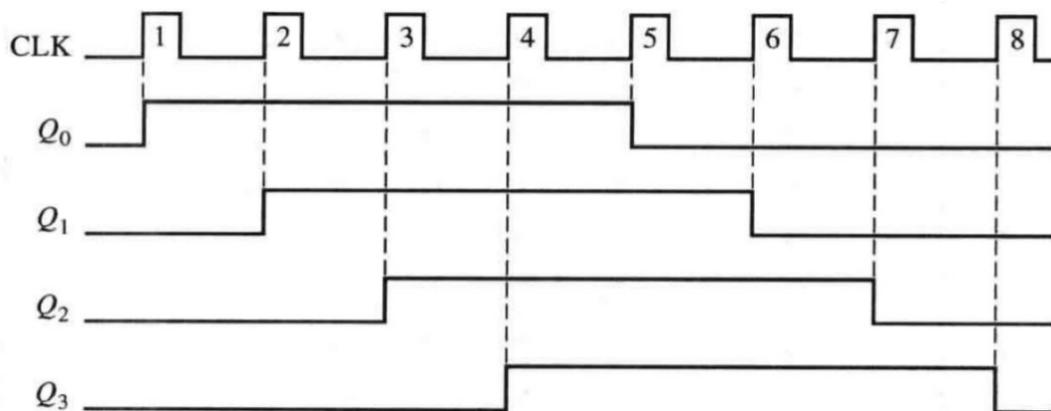


Fig. 18 The Timing diagram

The table for the results is shown below.

	Q0	Q1	Q2
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1	0	0	0
2	1	0	0
3	1	1	0
4	1	1	1
5	1	1	1
6	0	1	1
7	0	0	1
8	0	0	0

### 3. Conclusions

(a) In conclusion, from this experiment, we learned more about the several circuit combinations such as half adders, flip-flops, timers, counters, and shift registers. We used combinational logic circuit as half adders, flip-flops, timers, counters, and shift registers. During the experiment, we reinforced the usage of lab equipment such as multimeters, oscilloscope.

In the experiment, for different action we can do is that we can firstly forecast the results and verify if they are correct.

With another group member, we first checked out the handbook before doing the experiment individually, and then discussed the difficulties may appear in the experiment. During the experiment, we cooperated to build the circuit, and I changed the input, group member recorded the results.

We had a completed plan before action.

I suggest that the laboratory manager should clean up and replace the broken components such as LED in time. Since we had met four broken LED during the lab session.

(b) Comment:

I enjoy the lab very much for the interesting results appear at the section 7 and section 8. I would use more accurate electric components to do the lab session. One thing I liked is the results of section 8 which is fascinating. The problem is that we had met four broken LED during the lab session.