EEE104 - Digital Electronics Laboratory Manual

Introduction

There is a one-day laboratory session in Digital Electronics. It is a necessary part of the course at which attendance is compulsory. The laboratory experiment will be marked and the total mark will contribute to 10% of your overall mark for this module. You will be marked according to

1. Your attendance.
2. The circuits which you build up. After your finishing **each** section, the demonstrator will test your circuit and mark for you.
3. The lab report, which must be based on the experiment outcomes.

The Laboratory Notebook:

The student must have their own laboratory notebooks. Your notebook must be clearly labelled on the cover with the following information: Name, student ID and Lab partner name. There is no need to copy the questions or other material from the pre-lab or laboratory questions into your lab-book. Only your clearly numbered answers are required.

Building the Circuit

Throughout these experiments we will use TTL chips to build circuits. The steps for wiring a circuit should be completed in the order described below:

1. Turn the power off before you build anything!
2. Connect the +5V and ground (GND) leads of the power supply to the power and ground bus strips on your breadboard. Before connecting up, use a multimeter to check that the voltage is 5V.
3. Plug the chips you will be using into the breadboard. Point all the chips in the same direction with the notch pointing to the

left to save confusion at a later stage

4. Connect +5V and GND pins of each chip to the power and ground bus strips on the breadboard.
5. Select a connection on your schematic and place a piece of hook-up wire between corresponding pins of the chips on your breadboard. Mark each connection on your schematic as you go, so as not to try to make the same connection again at a later stage.
6. Unused gate inputs should be connected to the logic level HIGH for AND/NAND gates and to the logic level LOW for OR/NOR gates.
7. Get one of your group members to check the connections, **before you turn the power on**.
8. If an error is made and is not spotted before you turn the power on. Turn the power off immediately before you begin to rewire the circuit.
9. At the end of the laboratory session, collect you hook-up wires, chips and all equipment and return them to the demonstrator.
10. Tidy the area that you were working in and leave it in the same condition as it was before you started.

Common Causes of Problems

- Not connecting the ground and/or power pins for all chips.
- Not turning on the power supply before checking the operation of the circuit.
- Leaving out wires.
- Plugging wires into the wrong holes.
- Driving a single gate input with the outputs of two or more gates
- Modifying the circuit with the power on.
- Unused gate inputs are not connected to the appropriate logic levels.

Example Implementation of a Logic Circuit

Build a circuit to implement the Boolean function $F = \overline{\overline{A} \cdot \overline{B}}$. See Appendix for IC pin definitions.

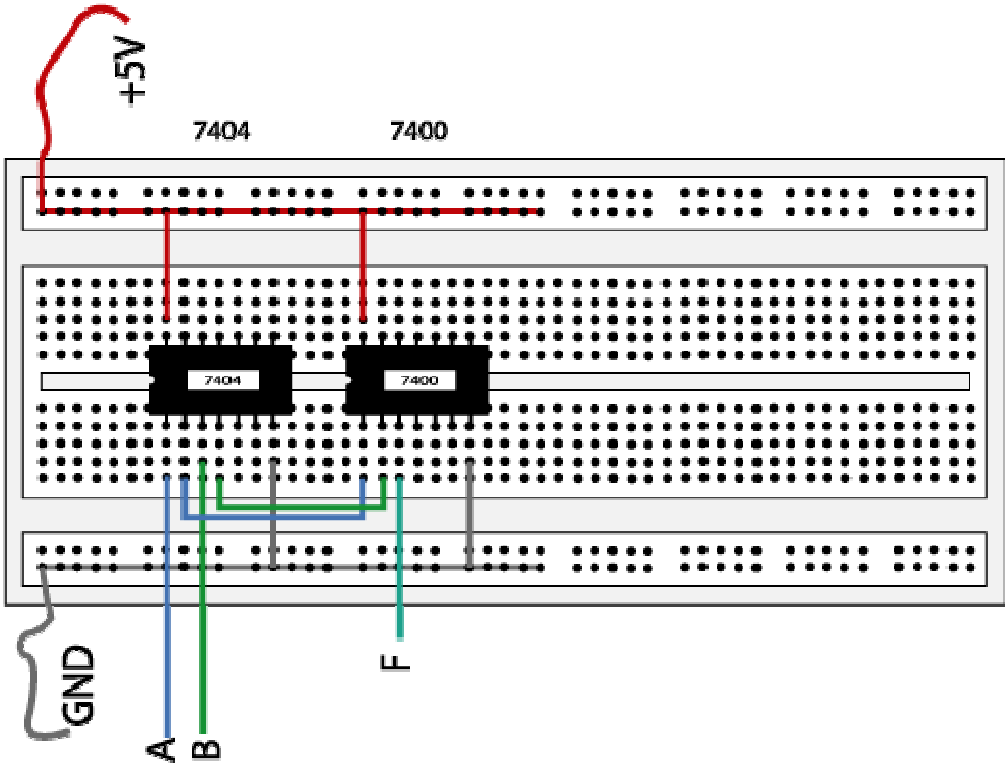


Fig 1. The complete designed and connected circuit

EE10312 - Digital Electronics Laboratory

Preliminary Discussions

There are several tasks that you must perform **prior** to sitting this laboratory:

1. Read the laboratory handout in full.
2. Draw up the truth tables for an inverter, a 2-input AND, a 2-input OR gate, a 2-input NAND gate, a 2-input NOR gate and a 2-input Exclusive-OR gate.
3. Use Boolean expressions to express De Morgan's Theorem.
4. Draw up the truth tables for a half adder.

Structure of the Experiment

1. Tests of basic logic gates.
2. To demonstrate DeMorgan's theorem
3. Implementation of a combinational logic circuit.
4. Implementation of a half adder.
5. To study the fundamentals of basic flip-flops.
6. To construct various types of counters.
7. To implement a shift register.

You must have read the *Digital Electronics Laboratory Manual*.

Equipment List

The equipment you require is as follows:

- Your own lab kit (borrowed from the technicians).
- A dc voltage supply
- Multimetre
- Collect hook-up wire and ICs from demonstrator (74LS00 $\times$ 1, 74LS02 $\times$ 1, 74LS04 $\times$ 1, 74LS08 $\times$ 1, 74LS32 $\times$ 1, 74LS86 $\times$ 1, 74LS74 $\times$ 2, 74LS112 $\times$ 2, 330Ω $\times$ 4, LED $\times$ 4). See Appendix for the IC pin definitions.

Experiment Procedures:

Section 1. Tests of Basic Logic Gates

(a) Connect one of the NOT gates (74LS04). Remember also to leave the dc power supply turned off, until you are sure that your circuit is wired correctly. Vary the input A (i.e. 0 and +5V) to obtain all the possible combinations and complete the Truth table for the NOT gate. Measure the output F using a Digital Voltmeter. Give the exact voltages that you obtained for each state of the gate.

(b) Connect one of the 2-input AND gates (74LS08). Measure the output F using a Digital Voltmeter. Give the exact voltages that you obtained for each state of the gate.

(c) Connect one of the 2-input NOR gates (74LS02). Measure the output F using a Digital Voltmeter. Give the exact voltages that you obtained for each state of the gate.

Section 2. DeMorgan's Theorem

Connect inputs A and B to an AND gate and their complements $\overline{A}$ and $\overline{B}$ to an OR gate as shown in Fig. 2. You will have to use NOT gates to obtain these states. Vary inputs A and B and enter the output values F and G into a truth table. Also, what is the Boolean equation for F and G in terms of A and B?

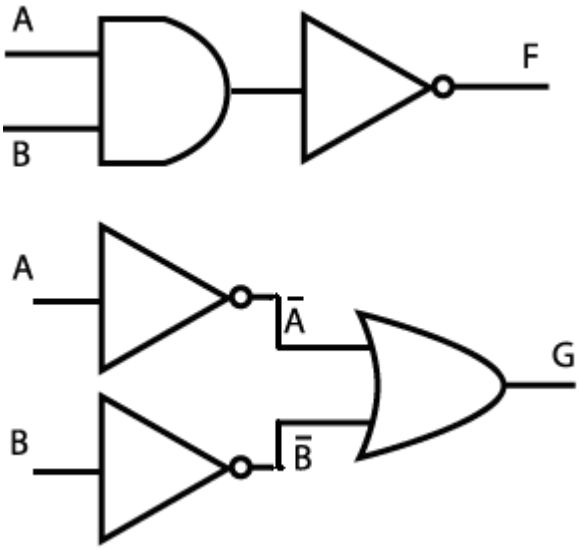


Fig. 2 Proving De Morgan's Theorem.

Section 3. Combinational Logic Circuits

Consider the logic statement: "If Mary obtains permission from her mother or her father and if Joe or Tom pick her up, she may go to the cinema". This statement may be expressed as a Boolean equation using the following Boolean variables:

F = Mary will go to the cinema (true/false)
A = Her mother will give her permission (true/false)
B = Her father will give her permission (true/false)
C = Joe will pick her up (true/false)
D = Tom will pick her up (true/false)

Then F = (A+B).(C+D) is the Boolean equation that describes this statement. Implement the circuit for this logic equation and complete the Truth Table.

Section 4. Implementation of a Half Adder

(a) Construct the circuit as shown in Fig. 3. Vary the inputs A and B (i.e. 0 and +5V) to obtain all the possible combinations and complete a Truth table for the sum output Σ and the carry output C.

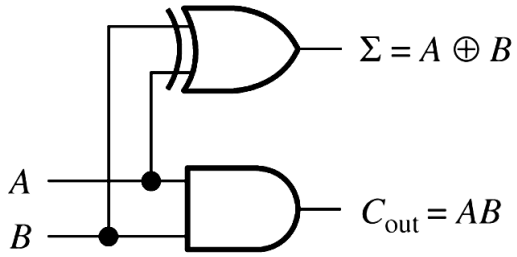


Fig. 3 The Half adder circuit

(b) Is this as you expected? Why is the half adder not suitable for all addition operations? (i.e. why do we need a full adder?)

In all the following sections, each of the outputs can be grounded through an LED and a 330 Ω resistor.

Section 5. The S-R Latch

(a) Connect the two NOR gates as shown in Fig. 4.

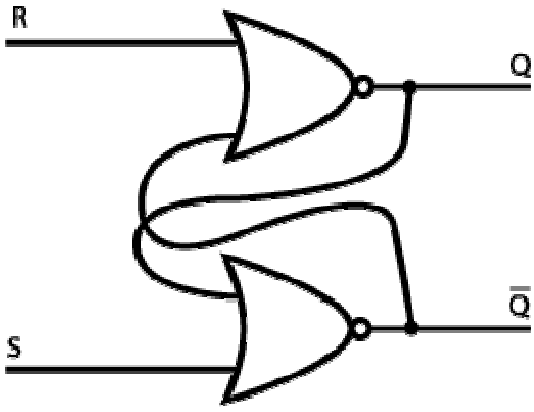


Fig. 4. An S-R latch created using NOR gates.

(b) Vary the inputs R and S (i.e. 0 and +5V) to obtain all the possible combinations for Q and /Q.

Qn	/Qn	R	S	Qn+1	/Qn+1
0	1	0	0		
1	0	0	0		
0	1	0	1		
1	0	0	1		
0	1	1	0		
1	0	1	0		
0	1	1	1		
1	0	1	1		

(c) How does this circuit work?

Section 6. The Edge-Triggered D Flip-Flop

(a) Implement the circuit in Fig. 5. You can simulate a clock signal by moving the clock line from low to high and back again to low.

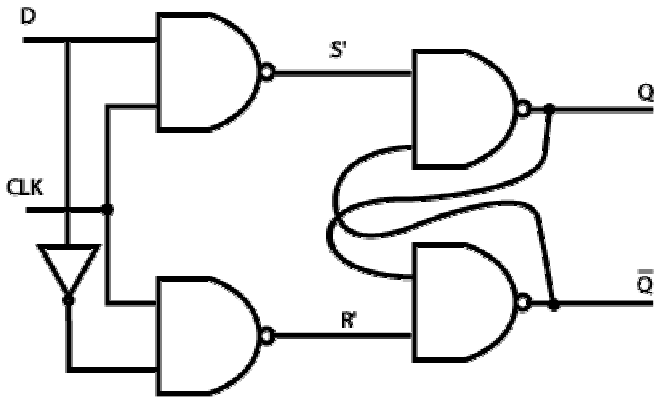


Fig. 5 The D-type flip-flop

(b) Draw up the truth table for the D-type flip flop. In your opinion how does it work? what could this circuit be useful for?

Qn	/Qn	D	Qn+1	/Qn+1
0	1	0		
1	0	0		
0	1	1		
1	0	1		

Section 7. The Asynchronous Counter

(a) Connect the circuit for the asynchronous counter as shown in Fig. 6. It consists of 3 J-K flip-flops (74LS112) with the J and K inputs set to high.

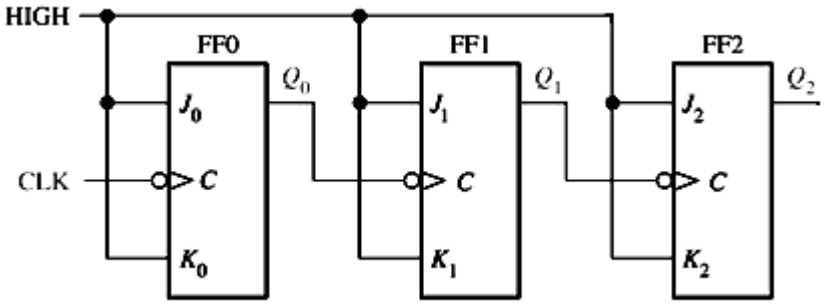


Fig. 6 The Asynchronous Counter.

(b) Reset all the J-K flip-flops. Then apply the clock pulses (1~2Hz for the function generator) and measure the outputs at the Qn outputs. What values did you observe?

	Q0	Q1	Q2
1			
2			
3			
4			
5			
6			
7			
8			
9			
etc..			

(c) How many states can this counter have for N flip-flops? In your opinion how does this circuit work? Why is this called an asynchronous counter?

Section 8. The Shift Register

(a) Connect up the 4-bit shift register (a Johnson counter)as shown in Fig. 7.

(b) Apply clock pulses (1~2Hz for the function generator) to see what will happen.

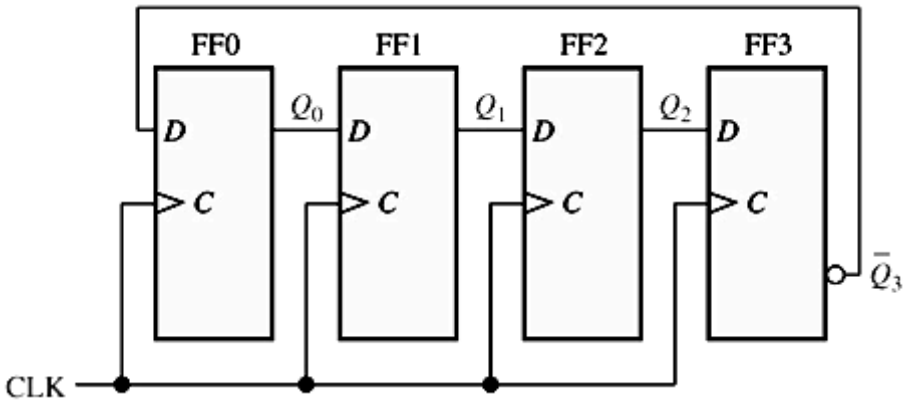


Fig. 7 The 4-bit shift register

Conclusions

(a) State briefly, but clearly, what you have gained from this laboratory. Outline aspects that you have noted within the experiment outside of the questions asked. Make comments on the procedure of the lab - Is there anything that you could have done differently? How did you split the work between group members? Did you have a plan of action? What else would you suggest that should be added to this lab session?

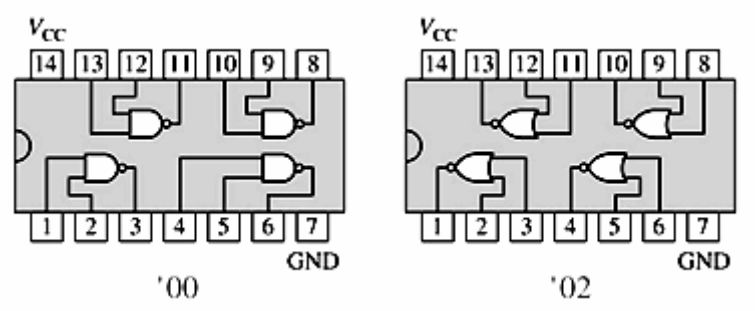
(b) **Comments**: Please write any comments that you may have here. Did you enjoy the lab? State one thing you would change? State one thing that you liked? Were there any problems during the laboratory session?

Notes:

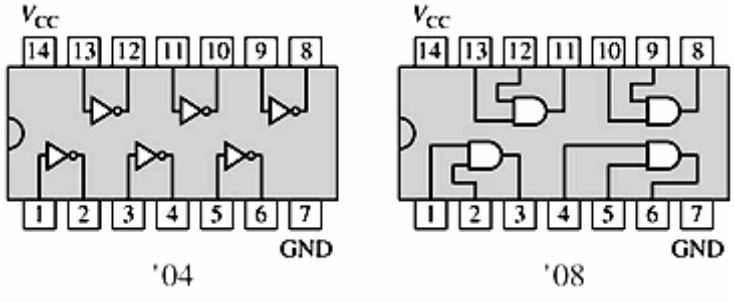
1. When you finish **each of Sections 3, 6 and 7**, please have a lab supervisor to mark for that section before continuing to the next section.

2. **DC Power Supply:** please use the Channel 3 (rightmost) which has a maximum output of 5.2 V.
3. **Function Generator**: use the "TTL Output", select 1Hz in the frequency range.
4. **Sections 5-8**: exact output voltage is not required; Instead, each output can be grounded through an LED **AND a 330 Ω resistor**. The output state, either HIGH (1) or LOW (0), is required.
5. **Section 5:** In the first step, you can change inputs R (for RESET) and S (for SET) to set the output Q to the desired state: R = 1 and S = 0 will lead to Q = 0; R = 0 and S = 1 will lead to Q = 1. In the second step, change the inputs R and S to the desired states and then observe the output.
6. **Section 7:** $\overline{PRE}$ and $\overline{CLR}$ of each J-K flip flop must be connected to HIGH.
7. **Section 8:** $\overline{PRE}$ of each D-type flip flop must be connected to HIGH; $\overline{CLR}$ of all the D-type flip flops can be wired to a single point. To touch this point to GND shortly will reset the output of the shift register to 0000, which is the recommended initial state.

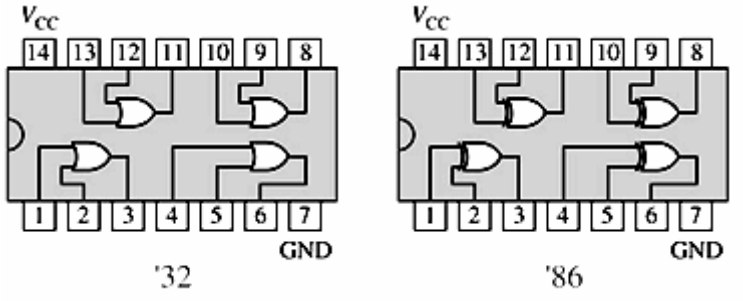
Appendix: Useful Chip Diagrams:



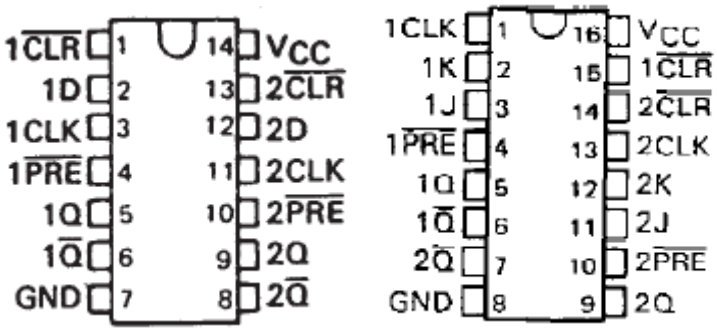
7400(NAND) **7402(NOR)**



7404(NOT) **7408(AND)**



7432(OR) **7486(XOR)**



7474 (D FF) 74112 (J-K FF)

Fig. 8 The IC chip diagrams