Analysis of Time Synchronization for Converged Wired and Wireless Networks

Maximilian Schüngel,
Steven Dietrich
Bosch Rexroth AG
Ulm, Germany
{maximilian.schuengel,
steven.dietrich}@boschrexroth.de

David Ginthör

Robert Bosch GmbH

Stuttgart, Germany
david.ginthoer@de.bosch.com

Shun-Ping Chen,
Michael Kuhn

Darmstadt University of Applied Sciences

Darmstadt, Germany
{shun-ping.chen,
michael.kuhn}@h-da.de

Abstract—Converged wired and wireless networks promise to meet both real-time and mobility requirements of factory automation scenarios. Time-Sensitive Networking (TSN) and 5G are auspicious technologies for future industrial communication. Hence, the combination of both wired and wireless communication is extensively discussed for industrial use cases. In this paper, we analyze the time synchronization in realistic wired and converged wired and wireless networks through IEEE 802.1AS. We provide a formulation of the time synchronization mechanisms and a system model for IEEE 802.1AS. Moreover, we investigate the synchronization accuracy for TSN and 5G/TSN networks given the requirements from IEEE, 3GPP, and IEC/IEEE.

Index Terms—5G, Ethernet, factory automation, TSN, realtime communication, synchronization, wireless communication

I. Introduction

Factory automation comprises precise and fast processes. Therefore, factory automation demands an ubiquitous and unified communication between different systems in horizontal and vertical domains. This leads to challenging requirements on the underlying information and communication technology regarding real-time capabilities, and the support of heterogeneous traffic. Further, factory automation scenarios start to leverage more and more mobile use cases such that mobility and scalability become key requirements for future real-time communication technologies [1].

Time-Sensitive Networking (TSN) is a set of standards for bridged industrial communication specified by IEEE 802.1. It extends IEEE 802.3 Ethernet standard to deliver deterministic (IEEE 802.1Qbv), low-latency (IEEE 802.2br) communication [2]. Thus, TSN adopts all benefits of standard Ethernet that are flexibility, ubiquity, and low cost infrastructure. Moreover, TSN provides the real-time capabilities of other Industrial Ethernet variants, such as Sercos III, EtherCAT, or PROFINET. Beyond that it provides also full horizontal and vertical connectivity from device to enterprise level. Dedicated to the application of TSN in industrial automation, IEC/IEEE 60802 specifies TSN profiles which define different TSN feature sets and requirements for industrial scenarios [2].

Converged wired and wireless networks (CWWN) through TSN and 5G promise to deliver both deterministic, low-latency communication, mobility, and scalability. The convergence of TSN and 5G, i.e. the integration of 5G with TSN, is a key

enabler for 5G to be suitable for future industrial scenarios as TSN shall serve as real-time interface to 5G in order to establish a unified data and control plane for industrial communication networks. Therefore, the 3GPP drives the specification of 5G for challenging industrial communication scenarios by supporting ultra-reliable low latency communication (URLLC) and integration with TSN together with IEEE [3].

Synchronization, i.e. a shared sense of time across all network components, is a key aspect for both TSN and 5G networks concerning e.g. time-triggered transmission, resource allocation, or sequence of events tracking [1]. Establishing an end-to-end synchronization brings several challenges. Therefore, in this work we analyze the synchronization through IEEE 802.1AS and investigate the impact on synchronization accuracy due to the integration of 5G with TSN.

II. RELATED WORK

Gutiérrez *et al.* [4] present an analysis of the synchronization quality of IEEE 802.1AS in large-scale wired networks. They provide a system model for time-aware systems (TAS) and introduce a clock model similar to Kim's continuous clock model [5]. They found that physical layer jitter and clock granularity impose a significant impact on time synchronization precision as well as the network topology itself.

Our contribution is a detailed formulation and error analysis of time synchronization in CWWN. We combine both proceedings and requirements from IEEE 802.1AS [6], 3GPP TR 23.734 [3], and IEC/IEEE 60802 [7] to establish a coherent analysis of time synchronization in converged TSN and 5G networks. Therefore, we adapt Gutiérrez *et al.* findings and derive an own mathematical formulation/theoretical analysis.

III. STANDARDIZATION EFFORTS OVERVIEW

This section provides an overview on standardization efforts regarding TSN time synchronization and TSN/5G integration driven by IEEE, 3GPP, and IEC. We establish a coherent mathematical description of the specified procedures.

A. Overview on IEEE 802.1AS

The IEEE 802.1AS standard [6] specifies the synchronization mechanism for TSN networks. Therefore, it defines a

specialized profile of the Precision Time Protocol (PTP) in reference to IEEE 1588 [8] for full-duplex Ethernet networks. The profile is referred to as generalized Precision Time Protocol (gPTP). gPTP is a packet based protocol for distribution of timing information across all network nodes.

gPTP defines two types of TAS that are 1) time-aware end stations (TAE) and 2) time-aware bridges (TAB). A TAS may be a slave or a master entity. There is only a single master entity per time-domain. The master entity, referred to as grandmaster (GM) in scope of gPTP, serves as source of time for all slave entities within the time-aware network (TAN). A TAN is associated with one or more time domains. Thus, TASs may be members in different time domains at once. IEEE 802.1AS specifies the use of two-step processing, i.e. the usage of *FollowUp*- and *Pdelay_Resp_FollowUp*-messages.

1) Propagation Delay Measurement: gPTP specifies a two-step peer delay mechanism for propagation delay (PD) measurement rather than an end-to-end approach. The peer delay mechanisms leverage the exchange and timestamping of messages to determine the mean PD $p\bar{d}_{i-1,i}$ between two peer TAS v_i and v_{i-1} as can be seen in Fig. 1. It does not consider link asymmetry such that the produced measurement is a (non-directional) mean value rather than a (directional) actual value. Beyond reception of the $Pdelay_Resp_FollowUp$, the initiator

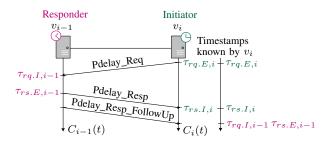


Fig. 1. Two-step peer delay measurement between initiator v_i and responder v_{i-1} according to IEEE 802.1AS; C(t): clock, t: reference time, τ : timestamp, rq: request, rs: response, I: ingress, E: egress

is aware of the four timestamps $\tau_{rq.E,i}$, $\tau_{rq.I,i-1}$, $\tau_{rs.E,i-1}$, and $\tau_{rs.I,i}$ hence can determine the mean PD $pd_{i-1,i}$ on the point-to-point link between initiator and responder following (1).

$$\bar{pd}_{i-1,i} = \frac{1}{2} \cdot \left((\tau_{rs.I,i} - \tau_{rq.E,i}) - nr_{i,i-1} \cdot (\tau_{rs.E,i-1} - \tau_{rq.I,i-1}) \right)$$
(1)

Here $\bar{pd}_{i-1,i}$ is expressed in relation to the clock of v_i . Thus the timestamps $\tau_{rq.I,i-1}$ and $\tau_{rs.E,i-1}$ have to be converted to the timescale of v_i accordingly using the neighbor rate ratio (NR) $nr_{i,i-1}$, which is defined as ratio between clock rates of direct adjacent TAS v_i and v_{i-1} . However IEEE 802.1AS does not provide a mechanism on measuring the NR.

2) Distribution of Timing Information: The mechanism for distribution of timing information specified in IEEE 802.1AS includes a) frequency syntonization and b) time synchronization to align the local clock of a TAS to the GM clock of the TAN to achieve a common sense of time. The distribution of

timing information according to IEEE 802.1AS is carried out in a two-step approach between two peers rather than end-to-end. A representative example is provided in Fig. 2. The mechanism for distribution of timing information leverages Sync- and FollowUp-messages. The following information is included in the FollowUp-message from v_{i-1} to v_i : a) precise origin timestamp $\tau_{s.E,0}$ which is the origin timestamp of Sync-message at GM v_0 , b) rate ratio rr_i which is the ratio between clock rate of v_i and GM v_0 , and c) correction field, cf_{i-1} which is the sum of delays since origin of the Sync-message at the GM v_0 , i.e. PD and residence times, on hierarchy S. The distribution of timing information for a network with three nodes (v_{i-1}, v_i, v_{i+1}) operates according to Fig. 2. The GM

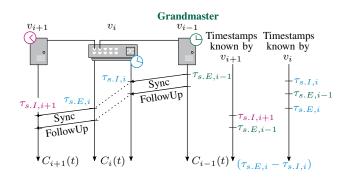


Fig. 2. Distribution of timing information according to IEEE 802.1AS within a TAN; $s: \mathit{Sync}\text{-}\mathsf{message}.$

starts with the Sync-message and registers the precise origin timestamp $\tau_{s.E,0}$. The GM then continues with the FollowUp-message. Upon reception of the FollowUp-message, the time-aware bridge v_i can determine the time offset $\theta_{i,0}$ and rate ratio rr_i of its local clock towards the GM clock following (2) and (3). In context of IEEE 802.1AS, the rate ratio rr_i is defined as ratio between clock rate of v_i and GM clock rate of v_0 . Here, $rr_0 = 1$ as v_0 represents the GM.

$$\theta_{i,0} = \tau_{s.I,i} - rr_i \cdot (\tau_{s.E,0} + cf_{i-1} + \bar{pd}_{i-1,i})$$
 (2)

$$rr_i = rr_{i-1} \cdot nr_{i,i-1} \tag{3}$$

Besides synchronizing itself, TABs also relay synchronization messages towards adjacent TAS, i.e. v_{i+1} . Therefore, the TAB sends out a new Sync-message and registers its departure with $\tau_{s.E,i}$. Then it can compute the correction field according to (4) which represents the total delay from Sync-message origin at the GM, i.e. $\tau_{s.E,0}$, to the origin at the TAB, i.e. $\tau_{s.E,i}$. The TAB continues with a FollowUp-message and attaches the correction field accordingly.

$$cf_i = cf_{i-1} + \bar{p}d_{i-1,i} + rr_i \cdot (\tau_{s.E,i} - \tau_{s.I,i})$$
 (4)

B. Overview on Converged TSN and 5G Networks

Converged TSN and 5G networks are able to provide deterministic end-to-end connectivity between stationary and mobile systems. Thus, they are key enabler for future industrial applications which place more emphasis on mobile use cases such as autonomous guided vehicles. The integration of 5G

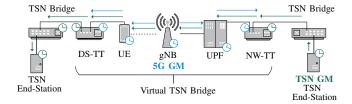


Fig. 3. Representative (user plane) architecture of converged TSN and 5G. There are two independent time domains that are *a*) a single TSN domain served by the TSN grandmaster and *b*) the 5G domain served by the gNB.

with TSN is planned to be transparent so that the 5G system (5GS) functionalities remain concealed to the TSN network and therefore enable a seamless integration with different TSN scenarios.

For integration with TSN, the 3GPP specifies that the 5GS introduces device- and network-sided TSN translators (DS-TT, NW-TT) as illustrated in Fig. 3 [3]. The DS-TT is integrated within the User Equipment (UE) while the NW-TT is integrated within the User Plane Function (UPF) on the network side. In scope of this paper, we only consider the 5G user plane as synchronization messages are transported over user plane only [3]. The 5GS (including both DS-TT and NW-TT) is further referred to as virtual TSN bridge (VTB). It includes only a single UPF, which is associated with a single NW-TT, but may included multiple UEs, i.e. DS-TTs. Wireless connectivity is provided to the UE by the next generation NodeB (gNB). The VTB appears as standard compliant TSN bridge following the black box paradigm. Thus, the TTs at the boundaries of the 5GS have to provide TSN bridge ingress and egress operations towards the TSN network [2].

The TT functionalities depends on the selected TSN class as specified in the IEC/IEEE 60802 profiles [7]. The TT has to adopt at least the minimal feature set (Class B).

C. Synchronization in Converged TSN and 5G Networks

The VTB supports time synchronization compliant with IEEE 802.1AS. Hence, the VTB may adopt either a boundary or a transparent clock behavior [3]. A boundary clock behavior is useful when 5G components have to be aware of the outer TSN timescale, for instance if the gNB serves also as TSN GM. In this work, we consider only a network-sided TSN GM. Accordingly, we will further investigate the transparent clock behavior only. It operates as follows:

As a transparent clock node, the VTB does not synchronize itself to an external GM. Instead it governs gPTP messages through the 5GS and utilizes the internal synchronization of the 5GS to determine the residence time of gPTP messages and applies corrections. Hence, the transparent clock behavior promises simplicity. For scenarios with multiple time domains there is no additional management effort introduced since the transparent clock, i.e. the residence time, is independent of the time domains.

IV. ANALYSIS OF SYNCHRONISATION THROUGH TSN

We start with an analysis of realistic wired TAN [4], [9] in order to analyze the time synchronization in realistic time-

aware CWWN. We model the behavior of relevant synchronization mechanisms according to IEEE 802.1AS under consideration of (partly preliminary) performance requirements specified in IEEE 802.1AS [6] and IEC/IEEE 60802 [7]. Investigations regarding multiple time domains are planned for further studies. Then we leverage our models to determine worst-case parameters with respect to IEEE 802.1AS and IEEE/IEC 60802. The worst-case parameters are the basis for our following simulation studies.

The gathered key requirements from IEEE 802.1AS and IEC/IEEE 60802 relevant to the time synchronization are presented in Tab. I. Consequently, our results are based on the given requirements.

TABLE I
REQUIREMENTS ON TIME-AWARE SYSTEMS ACCORDING TO IEEE
802.1AS [6, p. 409-414] AND IEC/IEEE 60802 [7, p. 20-24]

#	Symbol	IEEE 802.1AS	IEC/IEEE 60802
1	$\max(\delta rr)$	$\pm 0.1 \cdot 10^{-6}$	-
2	$\max(\rho)$	$\pm 100 \cdot 10^{-6}$	$\pm 100 \cdot 10^{-6}$
2	$\max(\rho')$	-	$\pm 3 \cdot 10^{-6} / s$
3	$\max(rt)$	$\pm 10 \cdot 10^{-3} \text{ s}$	-
4	$\max(tat)$	$\pm 10 \cdot 10^{-3} \text{ s}$	-
5	$\max(\theta_i)$	$\pm 1 \cdot 10^{-6} \text{ s}, i \leq 6$	$\pm 1 \cdot 10^{-6} \text{ s}, i \le 100$
6	$\max(\delta res)$	40/(1-0.0001) ns	-
7	$\max(\delta p d_0)$	-	$\pm 10 \cdot 10^{-9} \text{ s}$
7	$\max(\delta p d(t))$	-	0 s
8	$\max(\delta phy)$	-	$\pm 5 \cdot 10^{-9} \text{ s}$

Rate ratio
 Phase drift
 Residence time
 Turnaround time
 Time offset
 Timestamp resolution
 Propagation delay
 PHY jitter

A. Error Model

First, we want to define a generic error model as presented in (5). An arbitrary erroneous value \tilde{f} consists of two components that are the ideal value f and the error value δf .

$$\tilde{f} = f + \delta f \tag{5}$$

B. Clock Model

For the formal analysis we use the clock model presented in (6) which we adapted from Kim's continuous clock model [5]. We are neglecting random processes [5], since they are not accounted by the covered mechanisms. The clock model C(t) encompasses a phase offset θ at t=0, a constant phase drift ρ and a time-variant phase drift $\rho'(t)$ against an ideal global time reference t:

$$C(t) = (1 + (\rho + \rho'(t))) \cdot t + \theta \tag{6}$$

where $C_{i-1}(t)$ and $C_i(t)$ identify different clocks. The timevariant phase drift $\rho'(t)$ is omitted for the analysis of synchronization since it is out of scope of the mechanism described in IEEE 802.1AS. Though, $\rho'(t)$ is considered in the later simulations in order to investigate realistic networks. The relation between $C_{i-1}(t)$ and $C_i(t)$ is given in (7).

$$C_{i}(t) = (1 + \rho_{i,i-1}) \cdot C_{i-1}(t) + \theta_{i,i-1}$$

$$= r_{i,i-1} \cdot C_{i-1}(t) + \theta_{i,i-1}$$
(7)

where

$$r_{i,i-1} = \frac{1+\rho_i}{1+\rho_{i-1}}$$
 and $\rho_{i,i-1} = \frac{\rho_i - \rho_{i-1}}{1+\rho_{i-1}}$ (8)

$$\theta_{i,i-1} = \theta_i - (1 + \rho_{i,i-1}) \cdot \theta_{i-1}$$
 (9)

C. Timestamp Model

A timestamp τ is a defined point in time and is generated by a clock. The generation of timestamps is defined in (10). It is indexed by j and is relative to a specific clock source. Thus different timestamps generated at the same reference time t_i at different clocks cannot be identical, unless the clocks are identical¹:

$$\tau_{j,i-1} = C_{i-1}(t_j) \wedge \tau_{j,i} = C_i(t_j)
\tau_{j,i-1} \neq \tau_{j,i}, \quad \text{when} \quad r_{i,i-1} \neq 1 \vee \theta_{i,i-1} \neq 0.$$
(10)

There are different sources of error inherited when a timestamp is generated. First, we have to consider the limited resolution of a timestamp generated by a physical digital clock as shown in [4], [9]. A digital clock operates at a given frequency $f_{\rm clock}$, thus a timestamp generated by that clock exposes a resolution Δ_r and appears as an integer multiple of Δ_r [9] introducing the error δres . The limited timestamp resolution introduces a maximal error of $\max(\delta res) = \Delta_r$ and a minimal error of $min(\delta res) = 0$ [9]. An additional source of error is introduced when messages traverse the physical layer as found by Loschmidt et al. [9] in both ingress and egress directions. This error is referred to as physical layer (PHY) jitter δphy . The error results from asymmetric ingress/egress processing. It is allowed to be in range of ± 5 ns [7]. The generic timestamp error consists of two components due to 1) limited timestamp resolution and 2) PHY jitter. It results as:

$$\delta \tau = \delta res + \delta phy = \left(\left\lfloor \frac{\tau}{\Delta_r} \right\rfloor \cdot \Delta_r + \delta phy \right) - \tau \ .$$
 (11)

The timestamp error becomes maximal or minimal when both of its error components become maximal or minimal as well:

$$\max(\delta \tau) = \max(\delta res) + \max(\delta phy) \approx 45.004 \text{ ns}$$
 (12)

$$\min(\delta \tau) = \min(\delta res) - \max(\delta phy) = \underline{-5 \text{ ns}}$$
 (13)

A time interval $\Delta \tau$, which is measured by comparing two timestamps originated by the same clock, imposes a maximum error $\max(\delta \Delta \tau)$ in case of divergent timestamps, i.e. under consideration of (12) and (13):

$$\max(\delta \Delta \tau) = \max(\delta \tau) - \min(\delta \tau) = \Delta_r + 2 \cdot |\max(\delta phy)|$$

$$\approx \underline{50.004 \text{ ns}}.$$
(14)

 $^1 \text{There is an exception for } t = (\theta_i - \theta_{i-1})/(\rho_{i-1} - \rho_i) \text{ when } [\theta_i > \theta_{i-1} \, \wedge \, \rho_{i-1} > \rho_i] \text{ or } [\theta_{i-1} > \theta_i \, \wedge \, \rho_i > \rho_{i-1}].$

D. Synchronization Model

For the formal analysis of the time synchronization in realistic networks, we separate the synchronization mechanism into different sections. For the examined TAN we use 100 TASs [4], i.e. the number of TASs is I = 100, such that we can investigate the (preliminary) requirements set by the TSN profile for industrial automation [7].

1) Neighbor Rate Ratio: However, both IEEE 802.1AS and IEC/IEEE 60802 give the requirement for the maximum phase drift of a clock in a TAS. From that we can derive the maximum NR assuming that the fastest and slowest clock, which are still standard compliant to IEEE 802.1AS or IEC/IEEE 60802, are neighbors. The maximum value for the NR follows from (15) [4]:

$$\max(nr) = \frac{1 + \max(\rho)}{1 - \max(\rho)} = \underline{\frac{1.0002}{1.0002}}.$$
 (15)

2) Rate Ratio: The rate ratio is accumulated through the concatenation of NR quantities which are traversed through the synchronization hierarchy as can be observed in (3). Likewise to the maximum NR, the maximum rate ratio can be derived from the given requirements following (16). It is present when v_0 and v_i are slowest and fastest clock, which are still standard compliant to IEEE 802.1AS or IEC/IEEE 60802:

$$\max(rr_i) = \frac{1 + \max(\rho_i)}{1 - \max(\rho_0)} = \max(nr) = \underline{1.0002} \ . \tag{16}$$

Starting from (17), the maximum rate ratio error follows (18). Using (15) and the IEEE 802.1AS and IEC/IEEE 60802 requirements for the NR, we can determine the maximum rate ratio error for the chosen TAN. We consider a concatenation of (i-2) clocks with nr=1 and single slowest-faster clock neighbor pair with $nr = \max(nr)$. According to Gutiérrez et al., the maximum tolerated NR error is equivalent to the maximum tolerated rate ratio error [4]:

$$\delta r r_i = \prod_{j=1}^{i} (n r_{j,j-1} + \delta n r_{j,j-1}) - \prod_{j=1}^{i} n r_{j,j-1}$$
 (17)

$$\max(\delta r r_i) = \left(\max(nr) + \max(\delta nr)\right)$$

$$\cdot \left(1 + \max(\delta nr)\right)^{i-2} - \max(rr) \qquad (18)$$

$$\max(\delta r r_{99}) = \underline{9.9 \cdot 10^{-6}} \ .$$

3) Propagation Delay: The PD model does not depend on the TAN as it is limited to the peer domain in between two adjacent TAS. The error model from (19) depends on the timestamp accuracy, i.e. the measurement of time intervals, and the NR. Then given the requirements from IEEE 802.1AS and IEC/IEEE 60802 the maximum error results in (20):

$$\delta \bar{p} d_{i-1,i} = \frac{1}{2} \cdot \left(\delta \Delta \tau_{rqrs,i} - n r_{i,i-1} \cdot \delta \Delta \tau_{rsrq,i-1} - \delta n r_{i,i-1} \cdot \left(\Delta \tau_{rsrq,i-1} + \delta \Delta \tau_{rsrq,i-1} \right) \right)$$
(19)

$$\begin{split} |\max(\delta\bar{p}d_{i-1,i})| &= \left|\frac{1}{2}\cdot \left(-\max(\delta\Delta\tau) - \max(nr)\cdot \max(\delta\Delta\tau) \right. \right. \\ &\left. - \max(\delta nr)\cdot \left(\max(tat) + \max(\delta\Delta\tau)\right)\right)\right| \\ &= \underline{50.5~\text{ns}}~. \end{split}$$

4) Correction Field: The correction field accumulates at every TAS v_i along the synchronization hierarchy. In reference to (4) the correction field cf_i consists of different components that are the preceding correction field cf_{i-1} , the PD of link (v_{i-1}, v_i) , and the residence time at v_i . Note that all properties are scaled to the GM timescale. Starting from the error model in (21) we can find the maximum correction field error following (22):

$$\delta c f_i = \sum_{j=1}^{i} \left(\delta \bar{p} d_{j-1,j} + r r_j \cdot \delta \Delta \tau_{s,j} + \delta r r_j \cdot (\Delta \tau_{s,j} + \delta \Delta \tau_{s,j}) \right)$$
(21)

$$\max(\delta c f_i) = (i-1) \cdot \left(\max(\delta \bar{p} d) + \max(r r_i) \cdot \max(\delta \Delta \tau) + \max(\delta r r_i) \cdot \left(\max(\Delta \tau) + \max(\delta \Delta \tau) \right) \right)$$
$$\max(\delta c f_{98}) = \underbrace{\frac{14.26 \ \mu s}{12.26 \ \mu s}}. \tag{22}$$

Now we obtained all quantities to analyze the synchronization precision. In order to synchronize itself, the TAS v_i calculates the current GM time according to (23) using all the timing information obtained through reception of Sync- and FollowUp-messages and the peer delay mechanism:

$$\tilde{\tau}_{gm,i} = \tilde{\tau}_{s.E,0} + \tilde{cf}_{i-1} + \tilde{pd}_{i-1,i}$$
 (23)

$$\max(\delta \tau_{gm,i}) = \max(\delta \tau) + \max(\delta c f_{i-1}) + \max(\delta \bar{p} d)$$
$$\max(\delta \tau_{gm,99}) = \underline{14.35 \ \mu s} \ . \tag{24}$$

From that, we can determine the synchronization precision according to [4] as presented in (25). We consider a worst case scenario, thus we assume that the discrepancy in time-variant phase drift between GM v_0 and TAS v_i becomes maximum, i.e. $\rho_i'(t) = -\rho_{gm}'(t)$ with $\max\left(\rho'(t)\right) = 3\cdot 10^{-6}$ according to IEC/IEEE 60802 [7]. Moreover, we consider a synchronization interval of $T_s=125$ ms according to IEEE 802.1AS [6] and a maximum error of the computed GM time:

$$\max(p_i) = 2 \cdot T_s \cdot \max(\rho'(t)) + \max(\delta \tau_{gm,i})$$

$$\max(p_{99}) = 15.1 \ \mu s \ . \tag{25}$$

The above analysis of synchronization through TSN presents different sources of error for synchronization in a realistic TSN network. The main sources of error are erroneous timestamps due to limited resolution and PHY jitter as well as erroneous NR. The remaining quantities such as rate ratio, PD, and correction field depend on mechanisms which leverage timestamps and NRs as can be seen from (18), (20), and (22). Another major aspect is the network topology as can be observed in (22). The resulting correction field error scales with the number of hops (i-1) between GM v_0 and TAS

 v_i . Therefore, we can conclude that the network topology and timestamp accuracy majorly affect the synchronization quality in realistic wired TAN.

V. ANALYSIS OF SYNCHRONIZATION THROUGH CONVERGED TSN AND 5G NETWORKS

Now that we analyzed the synchronization performance in wired TAN, we follow with an analysis of realistic CWWN with regard to TSN and 5G integration as presented in Section III-B. For the analysis we use requirements presented in Tab. I as a starting point and further involve dedicated requirements on synchronization for the 5GS which are given in Tab. II. The synchronization requirements are presented in association to the type of 5G subcarrier spacing (SCS), i.e. the 5G numerology μ . The 5G requirements are related to the 5G frame structure with regard to frame time coordination [10].

TABLE II REQUIREMENTS ON TIME SYNCHRONIZATION FOR 5G [10]

Numerology μ	0	1	2	3
Subcarrier Spacing	15 kHz	30 kHz	60 kHz	120 kHz
Sync. Requirement	$\pm 1.5~\mu \mathrm{s}$	$\pm 780~\mathrm{ns}$	$\pm 390~\mathrm{ns}$	$\pm 190~\mathrm{ns}$

We use the synchronization model presented in Section III-C. Therefore, the VTB presents itself as standard compliant TSN bridge. It uses the internal synchronization of 5G to determine the residence time of gPTP messages and thus to apply corrections. The VTB sets itself apart from a conventional TSN bridge with regard to the determination of the residence time and thus the correction field calculation.

1) Residence Time: According to 3GPP TR 23.734 [3] the VTB registers an ingress timestamp τ_I and egress timestamps au_E to determine the residence time of gPTP messages. This approach leverages the internal synchronization of the 5GS which is also provided to the boundary NW-TT and DS-TT [3]. As the timestamps are registered at the very boundaries of the VTB, we can omit jitter that is introduced by the 5GS, e.g. scheduling or uplink/downlink asymmetry. We assume that the 5GS uses the telecom profile for gPTP [11] for the internal synchronization, thus we model NW-TT and DS-TT as TAS with independent clocks. Moreover, we assume the gNB to be the GM of the 5G time domain. The residence time is determined according to (26) where both ingress and egress timestamps, which are registered by NW-TT and DS-TT respectively, are expressed in GM timescale. NW-TT and DS-TT clocks are modeled in reference to (7):

$$\Delta \tilde{\tau}_{\text{vtb}} = ((1 + \rho_{\text{dstt},0}) \cdot \tau_{E,0}) - ((1 + \rho_{\text{nwtt},0}) \cdot \tau_{I,0}) + ((1 + \rho_{\text{dstt},0}) \cdot \delta \tau_{E,0} - (1 + \rho_{\text{nwtt},0}) \cdot \delta \tau_{I,0}$$
(26)
$$+ (\theta_{\text{dstt},0} - \theta_{\text{nwtt},0})) .$$

From (26) we can obtain the residence time error of a VTB according to (27). We assume that the 5G GM is an ideal clock, i.e. $\rho_0 = 0$ and $\theta_0 = 0$. Under consideration of the requirements on time synchronization for 5G, as depicted in Tab. I - II, we are able to determine the maximum residence time error of a VTB for different 5G numerology. We consider

NW-TT and DS-TT to be 5GS components which meet the synchronization requirements from Tab. II. (28) yields to the maximum residence time error as presented in Fig. 4:

$$\delta \Delta \tau_{\text{vtb}} = (\rho_{\text{dstt},0} \cdot \tau_{E,0}) - (\rho_{\text{nwtt},0} \cdot \tau_{I,0}) + ((\theta_{\text{dstt},0} - \theta_{\text{nwtt},0}) + (1 + \rho_{\text{dstt},0}) \cdot \delta \tau_{E,0} - (1 + \rho_{\text{nwtt},0}) \cdot \delta \tau_{I,0})$$
(27)

$$\max(\delta \Delta \tau_{\text{vtb}}) = \max(\rho_{i,0}) \cdot \max(\Delta \tau) + 2 \cdot \max(\theta_{i,0}) + 2 \cdot ((1 + \max(\rho_{i,0})) \cdot \max(\delta \tau))$$
(28)

with

$$\max(\rho_{i,0}) = \frac{\max(\rho_i) - \min(\rho_0)}{1 + \min(\rho_0)} , \qquad (29)$$

$$\max(\theta_{i,0}) = \max(\theta_i) - \left(1 + \max(\rho_{i,0})\right) \cdot \min(\theta_0) . \quad (30)$$

It gets clear that the maximum residence time error, which

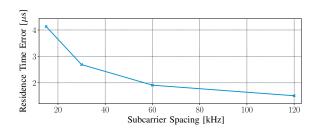


Fig. 4. Worst-case residence time error of a virtual TSN bridge leveraging requirements in time synchronization for 5G.

is calculated through (28), depends on the 5G requirements due to the association of SCS and time synchronization requirements. Larger SCS leads to smaller time slots [12] and thus to more stringent requirements on time synchronization [10]. Therefore, we see an reduced maximum residence time error for larger SCS when considering the associated time synchronization requirements.

2) Correction Field: Likewise to (4), the correction field is calculated at the VTB v_i . It is an aggregation of the preceding correction field value cf_{i-1} , the PD $pd_{i-1,i}$, and the residence time at the VTB itself, i.e. $\Delta \tau_{vtb}$. We are able to obtain the maximum correction field error according to (32) by leveraging (20), (22), and (28):

$$\tilde{cf}_{i,\text{vtb}} = \tilde{cf}_{i-1} + \Delta \tilde{\tau}_{\text{vtb}} + \tilde{pd}_{i-1,i}$$
 (31)

$$\max(\delta c f_{i,\text{vtb}}) = \max(\delta c f_{i-1}) + \max(\bar{p} d_{i-1,i}) + \max(\delta \Delta \tau_{\text{vtb}}).$$
(32)

Later we use the results from Fig. 4 in combination with (32) as parameter settings of our following simulation of converged TSN/5G networks.

After determining the maximum correction field error at a VTB, we can find the maximum synchronization error for converged TSN and 5G networks as presented in Fig. 5. It shows that the convergence of TSN and 5G networks does affect the synchronization performance. Here the main source of error are erroneous timestamps due to distributed clocks in NW-TT and DS-TT. As can be seen, increasing

the SCS, i.e. increasing the requirements on the internal synchronization of the 5GS components, reduces the overall synchronization error. Moreover, we found that reducing the number of hops may yield to a significant improvement of the overall synchronization. As a matter of fact, the integration of 5G with TSN indeed may lead to less complex networks, i.e. less number of hops, as 5G naturally provides direct access and wide connectivity in comparison to TSN.

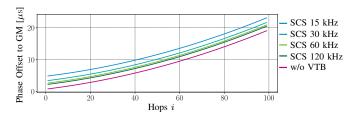


Fig. 5. Worst-case synchronization in a TAN with i hops with/without VTB.

VI. SIMULATION

In Sec. IV and V we discussed the synchronization in realistic TAN for both TSN and converged TSN/5G networks. We leveraged requirements given by the standards to model a TAN and to conduct worst case estimation for synchronization. In nature, networks involve random processes and are rather dynamic which affects the overall synchronization accuracy. Therefore, we use the discrete event simulator OMNEST [13] to simulate our theoretical models.

OMNEST is a discrete event simulator that allows us to investigate realistic scenarios with random processes. We use the INET [14] framework for Ethernet implementation in OMNEST, NeSTiNg [15] as basis for our TSN model, and IEEE8021AS [16] as basis for our gPTP model. We used probabilistic parameters according to Tab. III. The values are derived from the specified requirements.

TABLE III SIMULATION PARAMETERS

Description	Parameter
Bescription	1 tirameter
Number of Devices	I = 100
Link Delay	D=50 ns
Phase Offset	$\theta \sim \mathcal{U}(-50, 50)$ ms
Phase Drift	$\rho \sim \mathcal{U}(-100, 100) \cdot 10^{-6}$
	$\rho' \sim \mathcal{U}(-3,3) \cdot 10^{-6}/s$
Physical Layer Jitter	$\delta phy \sim \mathcal{N}(0, \frac{5}{3}) \text{ ns}$ $\Delta_r = 40 \cdot 10^{-9} \text{ s}$
Timestamp Resolution	$\Delta_r = 40 \cdot 10^{-9} \text{ s}$
Sync-Interval	$T_s = 125 \text{ ms}$
Pdelay-Interval	$T_p = 1 \text{ s}$

A. Timestamp Accuracy

First we want to discuss the timestamp model as it is the basis for the following considerations. We implemented a timestamp model according to Sec. IV-C and use the values for timestamp resolution and PHY jitter in reference to the standards and Tab. III. With that we obtain a normally distributed timestamp error as can be seen from Fig. 6. Further, we can see the two error components of timestamp resolution

error and PHY jitter. The timestamp resolution error due to limited clock granularity is uniformly distributed in the range of 0 ns to 40 ns as indicated in Sec. IV-C. The error due to PHY jitter follows a normal distribution in range of -5 ns to 5 ns (with a probability of $P(|\delta phy|<5)=99.8\%)$ in reference to Tab. III.

It follows a normally distributed timestamp error in range of -5 ns to 45 ns according to (12) and (13).

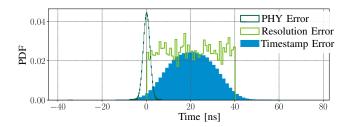


Fig. 6. Timestamp error due to limited timestamp resolution and PHY jitter.

B. Propagation Delay Accuracy

The PD measurement is a fundamental mechanism of IEEE 802.1AS since the PD is used to apply corrections to time synchronization. In order to investigate the PD accuracy we set up a network with two TAE only. The TAE are connected through a direct point-to-point link with a configured link delay of 50 ns which corresponds to a 10 m copper link. The clocks of both TAS are configured according to Tab. III.

Figure 7 shows a PD measurement over an observation interval of 500 s. The raw PD values (green) are mostly exposed to variations of ± 30 ns. Such errors are caused by inaccurate timestamps. The PD mechanism is very much affected by timestamp errors since at its core it leverages four different timestamps to determine the PD. We see that the PD errors are well under the predicted worst case error of $\max(\delta pd) = 90.004$ ns which is totally acceptable as a worst case scenario is very unlikely. Further, in realistic scenarios errors may compensate each other such that the overall error is low [4], e.g. two subsequent timestamps expose a similar error, maybe close to the average, then the error of the interval determined by both timestamps is low. Although the raw PD values seem to be rather inaccurate, the cumulative average, which is used to apply corrections in the end, does meet the configured PD fairly well and manages to keep the variations in range of ± 4 ns.

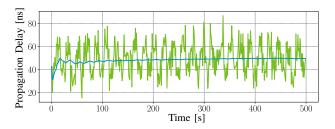


Fig. 7. Propagation delay; green: actual value, blue: average value.

C. Time Synchronization Accuracy

The time synchronization accuracy depends on the capability to compensate forwarding and processing delays. Its accuracy is very much affected by correction field errors. Thus it very much depends on PD measurements and processing/residence time compensations. In order to investigate the time synchronization accuracy in wired and CWWN, we modeled a line network with 100 hops. Each TAS includes the system model according to Sec. IV with a parameter selection in reference to Tab. III.

We define a mechanism for NR detection according to (33) where we utilize subsequent peer delay measurements to determine the NR accordingly. We basically compare two time intervals against each other where one interval is measured by v_i and the other one by v_{i-1} . We assume that the PD is constant, otherwise the measurement may be affected.

$$nr_i[n] = \frac{\tau_{rq.E,i}[n] - \tau_{rq.E,i}[n-1]}{\tau_{rq.I,i-1}[n] - \tau_{rq.I,i-1}[n-1]}$$
(33)

Further, we define the time synchronization accuracy as absolute offset between slave and master time in reference to IEEE 1588 [8]:

$$p_i = \tau_i - \tau_0 \ . \tag{34}$$

Here the timestamp τ_i is registered right before adjusting the local clock of v_i such that we observe the worst-case. The measurements itself are 50 repetitions of 100 s captures.

1) Wired Networks: For the analysis of time synchronization in wired networks, we wanted to observe the impact of our system and clock model on the time synchronization accuracy of the 99-th TAS in our line TAN. Therefore, we conducted 1) a reference measurement where we omitted PHY jitter and timestamp resolution errors, 2) a measurement where we configured a realistic clock frequency of 125 MHz, i.e. a timestamp resolution of 8 ns, but still omitted PHY jitter, and 3) a worst-case measurement with simulation parameters according to Tab. III.

The results of all measurements are presented in Fig. 8 as probability density function of the time synchronization error. As expected, we observe a narrow range of error for the reference measurement in between ± 1 ns. With a realistic clock frequency and a resulting limited timestamp resolution, the second measurement exposes a broader range of error in between $\pm 0.1~\mu s$. As expected for the worst-case measurement we observe the widest range of error in between $\pm 0.8~\mu s$. However, we do not see that our worst-case measurement reaches our predicted worst-case time synchronization error which is totally acceptable as the predicted worst-case scenario is far from likely to occur by nature. Furthermore, with realistic simulation parameters it is most likely that the interlinking of errors may yield to compensation by itself. e.g. when a following system introduced an error with opposite sign.

2) Converged Wired and Wireless Networks: For the analysis of time synchronization in CWWN we integrate a VTB into the line network. For the simulation of the VTB we modified our TSN bridge model in order to consider the

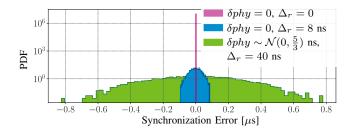


Fig. 8. Synchronization accuracy in a wired network with I = 100 hops.

residence time error inherited by asynchronous NW-TT and DS-TT. The residence time error depends on the SCS, i.e. the 5G numerology, since different SCS configurations impose different timing requirements on the 5G components as shown in Fig. 4. The artificial residence time error is defined as:

$$\delta \Delta \tau_{\text{vtb}}(scs) = \mathcal{U}(-\max(\delta \Delta \tau_{\text{vtb}}(scs)), \max(\delta \Delta \tau_{\text{vtb}}(scs)))$$
(35)

where $scs \in \{15, 30, 60, 120\}$ kHz is the configured SCS. Again, the measurements are 50 repetitions of 100 s captures.

From Fig. 9 we observe the impact of 5G/TSN integration for different SCS configurations. It gets clear that the resulting synchronization error rises with lower SCS as this yields to less stringent timing requirements on the 5G components including NW-TT and DS-TT. We observe a flattened top since we utilized a uniformly distributed residence time error for the VTB. Our simulation shows that the integration of 5G

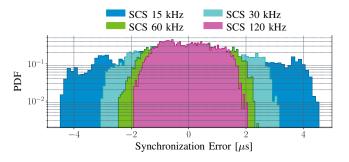


Fig. 9. Synchronization accuracy in a CWWN with $I=100~{\rm hops}$ and an integrated virtual TSN bridge (which replaces a hop).

does impact the synchronization accuracy. In comparison to our simulation for TSN only, we see that the synchronization error more than doubles for the converged TSN/5G networks considering a SCS of 120 kHz. The synchronization error keeps increasing for smaller SCS configurations.

VII. CONCLUSION AND FUTURE WORK

In this work, we presented a detailed analysis of time synchronization in both wired and CWWN. We identified the primary sources of inaccuracy for time synchronization through IEEE 802.1AS as limited timestamp resolution, PHY jitter, and the network topology itself, i.e. by means of concatenation of TAS. Further, we demonstrated the effects on time synchronization in converged TSN/5G networks.

We elaborated a mathematical formulation of time synchronization mechanisms and provided a system model for TAS in regards to IEEE 802.1AS. We found that the integration of 5G as VTB does introduce an additional error to the time synchronization and thus indeed degrades the accuracy. In the worst-case scenario, i.e. with a SCS of 15 kHz, the error due to the integration of 5G is equivalent to the error introduced by ≈ 36 additional hops. However, the integration of 5G with TSN will lead to changes in the network configuration and design. Therefore, in CWWN scenarios, the number of hops may be drastically reduced due to the use of 5G which may compensate for the additional error introduced by the integration of 5G itself.

So far we analyzed the time synchronization accuracy for a single network configuration. We will investigate other configurations especially when we consider 5G's capability of mobile communication. Moreover, we only considered a synchronization scenario where the GM is located at the network side (of the VTB, i.e. the 5GS). It would be interesting to investigate different synchronization scenarios such as device-sided GM (with respect to 5G even mobile GM), which may yield to device-to-device synchronization, or a GM located within the 5GS, i.e. the gNB.

REFERENCES

- "Integration of Industrial Ethernet Networks with 5g Networks," 5G ACIA, Tech. Rep., 2019.
- [2] J. Farkas, B. Varga, G. Miklos, and J. Sachs, "5g-TSN Integration for Industrial Automation," Ericsson, Tech. Rep., 2019.
- [3] "TR 23.734 V16.2.0 Study on enhancement of 5gs for Vertical and LAN Services (Release 16)," 3GPP, Standard 23.734, 2019.
- [4] M. Gutirrez, W. Steiner, R. Dobrin, and S. Punnekkat, "Synchronization Quality of IEEE 802.1as in Large-Scale Industrial Automation Networks," in 2017 IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), 2017, pp. 273–282.
- [5] K. S. Kim, "Comments on IEEE 1588 Clock Synchronization Using Dual Slave Clocks in a Slave," *IEEE Communications Letters*, vol. 18, no. 6, pp. 981–982, 2014.
- [6] "IEEE Standard for Local and Metropolitan Area Networks Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks," *IEEE Std 802.1AS-Rev/D8.3*, pp. 1–434, 2019.
- 7] "IEEE/IEC 60802 D1.1," IEC/IEEE, Tech. Rep., 2019.
- [8] "IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems - Redline," *IEEE Std* 1588-2008 (Revision of IEEE Std 1588-2002) - Redline, pp. 1–300, 2008. [Online]. Available: https://ieeexplore.ieee.org/document/7949184
- [9] P. Loschmidt, R. Exel, and G. Gaderer, "Highly Accurate Timestamping for Ethernet-Based Clock Synchronization," *Journal of Computer Networks and Communications*, vol. 2012, 2012.
- [10] H. Li, L. Han, R. Duan, and G. M. Garner, "Analysis of the Synchronization Requirements of 5g and Corresponding Solutions," *IEEE Communications Standards Magazine*, vol. 1, no. 1, pp. 52–58, 2017.
- [11] "ITU-T G.8275.1/Y.1369.1 Precision time protocol telecom profile for phase/time synchronization with full timing support from the network; Amendment 3," ITU-T, Tech. Rep., 2019.
- [12] "TR 38.211 V16.0.0 Physical Channels and Modulation (Release 15)," 3GPP, Standard 38.211, 2019.
- [13] OMNEST. [Online]. Available: https://omnest.com/
- [14] INET Framework. [Online]. Available: https://inet.omnetpp.org/
- [15] J. Falk, D. Hellmanns, B. Carabelli, N. Nayak, F. Drr, S. Kehrer, and K. Rothermel, "NeSTiNg: Simulating IEEE Time-sensitive Networking (TSN) in OMNeT++," in 2019 International Conference on Networked Systems (NetSys), 2019, pp. 1–8.
- [16] H. Puttnies, P. Danielis, E. Janchivnyambuu, and D. Timmermann, "A Simulation Model of IEEE 802.1as gPTP for Clock Synchronization in OMNeT++," in *Proceedings of the 5th International OMNeT++ Community Summit*, ser. EPiC Series in Computing, vol. 56. EasyChair, 2018, pp. 63–72.