RL78 Family
EEPROM Emulation Library Pack02 Ver.1.01
Release Note

R20UT2645EJ0101
Rev.1.01
Feb 29, 2016

Thank you for using the RL78 Family EEPROM Emulation Library Pack02 Ver.1.01.

This document contains precautionary and other notes regarding use of the EEPROM Emulation Library Pack02 Ver.1.01. Please read this document before using the library.

Contents

Chapter 1 Target Product

The following shows the target product for this release note.

Product Name	Ver.	ZIP File Name	Zip Ver.
RL78 Family EEPROM Emulation Library Pack02 for the CA78K0R Compiler	V1.01	JP_R_EEL_RL78_P02_V1.01_B_E	V1.01B

Chapter 2 User's Manual

The following user's manual covers this version of the library:

Title	Document Number
RL78 Family EEPROM Emulation Library Pack02 User's Manual	R01US0068EJ0101

Chapter 3 Revisions

The following shows the items upgraded in the new version.

No.	ZIP Ver.	Target Library	Contents
1	V1.01B	Library	There are no changes in the library from the previous Zip version (JP_R_EEL_RL78_P02_V1.01_A_E).
		User's Manual	Revised from Rev. 1.00 to Rev. 1.01. For details of the corrections to the user's manual in response to the revision, refer to the manual's revision history.

Chapter 4 Supported Tools

Use the following tool version when using tools in combination with this library:

Tool Used	Version
Integrated development environment CubeSuite+	V1.00.00 or later
Integrated development environment CS+	V3.00.00 or later

Chapter 5 Installation

This chapter describes how to install and uninstall the EEPROM Emulation Library Pack02.

5.1 Installation

Install the EEPROM Emulation Library Pack02 by using the following procedure:

(1) Start Windows.
(2) Decompress the folder that contains the EEPROM Emulation Library Pack02 files and copy the extracted folders to any location.

5.2 Uninstallation

Uninstall the EEPROM Emulation Library Pack02 by using the following procedure:

(1) Start Windows.
(2) Delete the folder that contains the EEPROM Emulation Library Pack02 files.

5.3 File Organization

The file organization after this library is installed is shown below.

```
Installation folder
└ EELRL78 Pack02
    └ Vx.xx
        ├ Read me
        │   └ TERMS AND CONDITIONS FOR USING THE SOFTWARE.pdf :
        │                                   Terms and conditions for using the software
        ├ doc
        │   ├ r01us0068ejxxxx_rl78.pdf      : User's Manual
        │   └ r20ut2645ejxxxx_rl78.pdf      : Release Note (this document)
        ├ librl78
        │   ├ eel.lib                       : EEPROM emulation library (EEL)
        │   └ fdl.lib                       : Data flash library (FDL)
        ├ incrl78
        │   ├ eel.h                         : EEL header file for C program
        │   ├ eel.inc                       : EEL header file for assembler
        │   ├ eel_types.h                   : EEL header file that specifies definitions for C program
        │   ├ eel_types.inc                 : EEL header file that specifies definitions for assembler
        │   ├ fdl.h                         : FDL header file for C program
        │   ├ fdl.inc                       : FDL header file for assembler
        │   └ fdl_types.h                   : FDL header file that specifies definitions for C program
        └ smprl78
            ├ asm
            │   ├ eel_descriptor.inc        : EEL descriptor header file
            │   ├ eel_descriptor.asm        : EEL descriptor source file
            │   ├ eel_sample_linker_file.dr : EEL sample directive file
            │   ├ fdl_descriptor.inc        : FDL descriptor header file
            │   └ fdl_descriptor.asm        : FDL descriptor source file
            └ C
                ├ eel_descriptor.h          : EEL descriptor header file
                ├ eel_descriptor.c          : EEL descriptor source file
                ├ eel_user_types.h          : EEL user-defined header file
                ├ eel_sample_linker_file.dr : EEL sample directive file
                ├ fdl_descriptor.h          : FDL descriptor header file
                ├ fdl_descriptor.c          : FDL descriptor source file
                ├ r_eel_sample_c.c          : EEL sample program file
                └ r_eel_sample_c.dr         : EEL sample Link directive file
```

Notes: 1. x indicates the omitted numerals in version or revision numbers.

2. If you wish to use the sample program, include both the program file (*.c) and the link directive file (*.dr).

Chapter 6 How To Build a Program

This chapter describes how to build a program using the EEPROM Emulation Library Pack02.

6.1 Software to be Used

Below are the system requirements for building programs using the EEPROM Emulation Library Pack02.

- Integrated development environment CubeSuite+ V1.00.00 or later or integrated development environment CS+ V3.00.00 or later

6.2 Building Using CS+ (Formerly CubeSuite+)

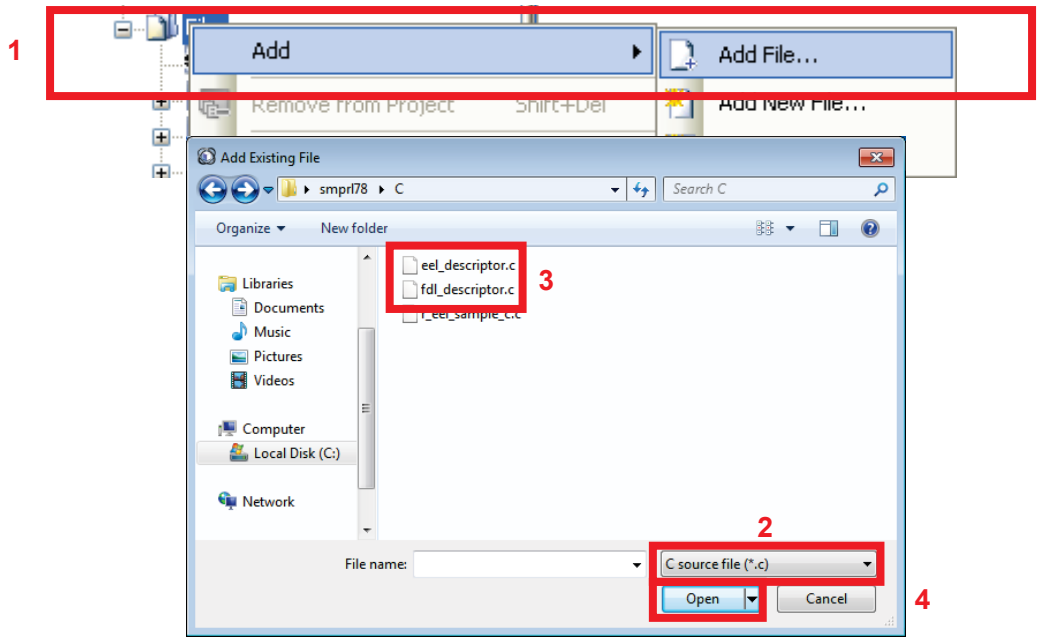
This section describes how to include the EEPROM Emulation Library Pack02 in a user-created program and build the user program by using CS+.

6.2.1 Building a C Program

(1) Creating a project and specifying the source files

Create a project by using CS+. In the Project Tree window displayed on the left, right-click the File node, click Add, and then click Add File. The Add Existing File dialog box is displayed (as shown in Figure 6-1).
Click the Files of type drop-down list, select C source file (*.c), and then register the user-created program file (r_eel_sample_c.c for the sample file of source code) and the descriptor files for the EEPROM emulation library and data flash library (eel_descriptor.c and fdl_descriptor.c) as the source files.

Figure 6-1. Specifying the Source Files



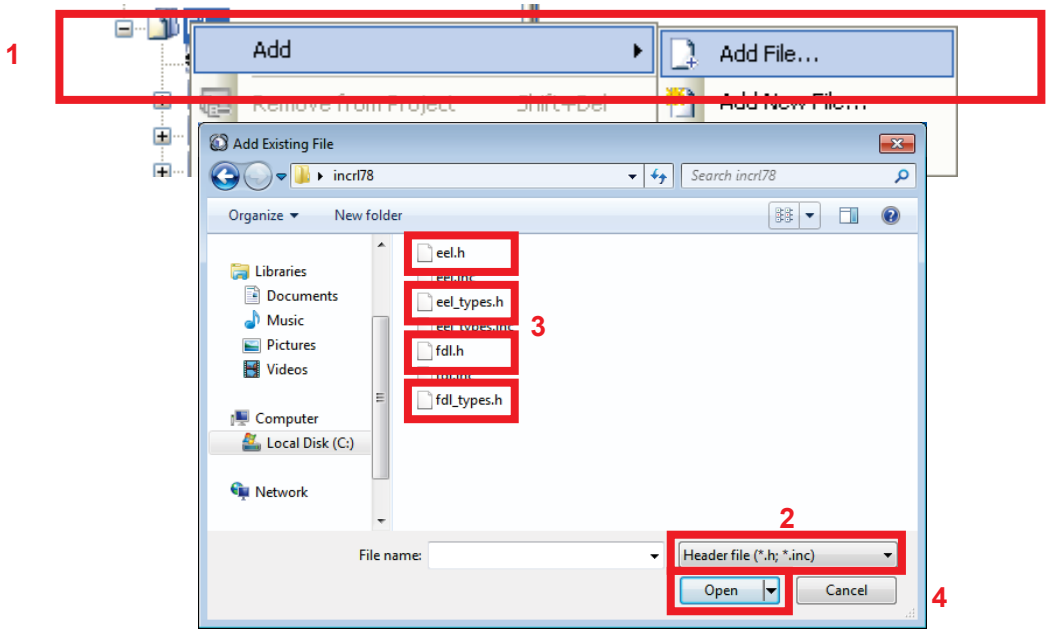
(2) Specifying the include file

In the CS+ Project Tree window, right-click the File node, click Add, and then click Add File.

The Add Existing File dialog box is displayed (as shown in Figure 6-2).

Click the Files of type drop-down list, select Header file (*.h;*.inc), and then register the header files and descriptor header files for the EEPROM emulation library and data flash library (eel.h, eel_types.h, fdl.h, fdl_types.h, eel_descriptor.h, fdl_descriptor.h, and eel_user_types.h).

Figure 6-2. Specifying the Include Files

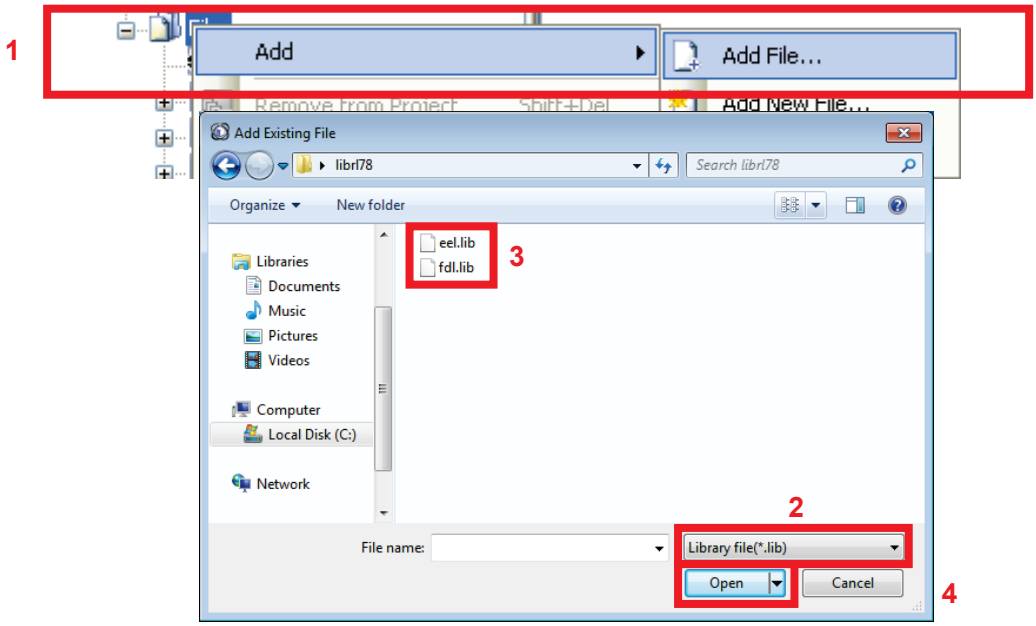


(3) Specifying the library file

In the CS+ Project Tree window, right-click the File node, click Add, and then click Add File. The Add Existing File dialog box is displayed (as shown in Figure 6-3).

Click the Files of type drop-down list, select Library file (*.lib), and then register the EEPROM emulation library and data flash library files (eel.lib and fdl.lib).

Figure 6-3. Specifying the Library Files

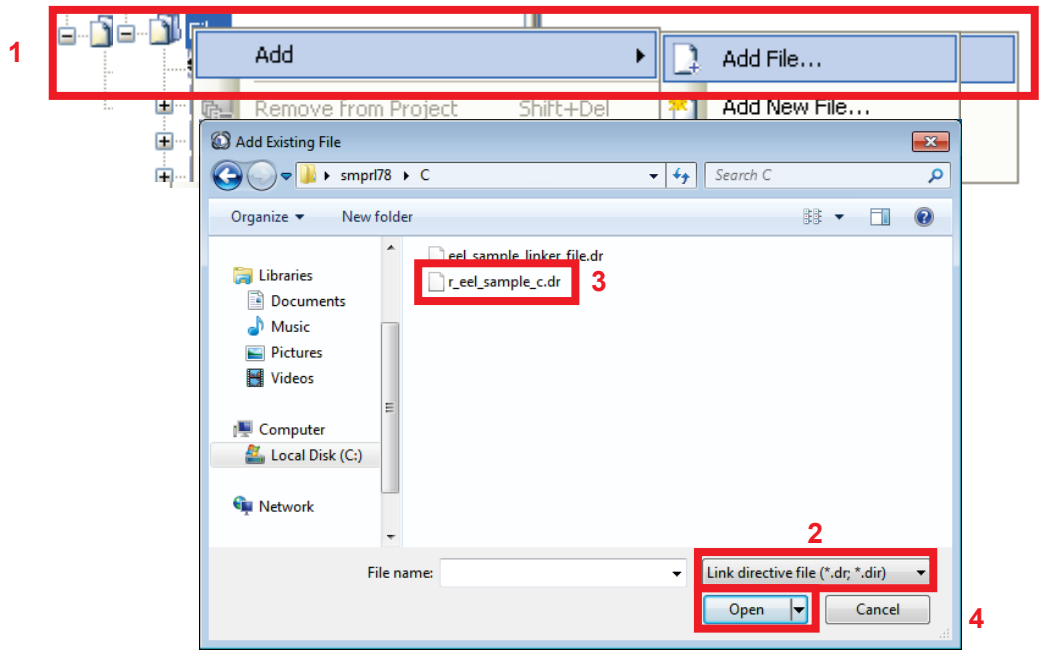


(4) Specifying the link directive file

In the CS+ Project Tree window, right-click the File node, click Add, and then click Add File. The Add Existing File dialog box is displayed (as shown in Figure 6-4).

Click the Files of type drop-down list, select Link Directive File (*.dr;*.dir), and then register the link directive file that has the same name as the user-created program (r_eel_sample_c.dr for the sample file of source code [Note]).

Figure 6-4. Specifying the Link Directive File



Note: The sample directive file that comes with the library may require editing or modification before use.

(5) Building

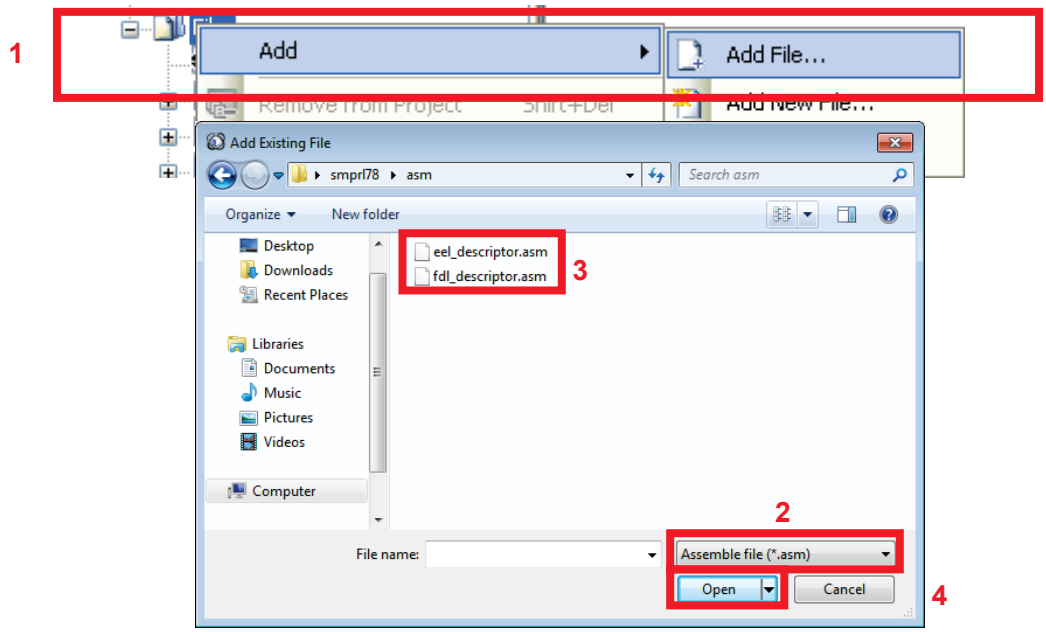
On the CS+ Build menu, click Build Project to build the project.

6.2.2 Building an Assembly Language Program

(1) Creating a project and specifying the source files

Create a project by using CS+. In the Project Tree window displayed on the left, right-click the File node, click Add, and then click Add File. The Add Existing File dialog box is displayed (as shown in Figure 6-5).
Click the Files of type drop-down list, select Assemble file (*.asm), and then register the user-created program file and the descriptor files for the EEPROM emulation library and data flash library (eel_descriptor.asm and fdl_descriptor.asm) as the source files.

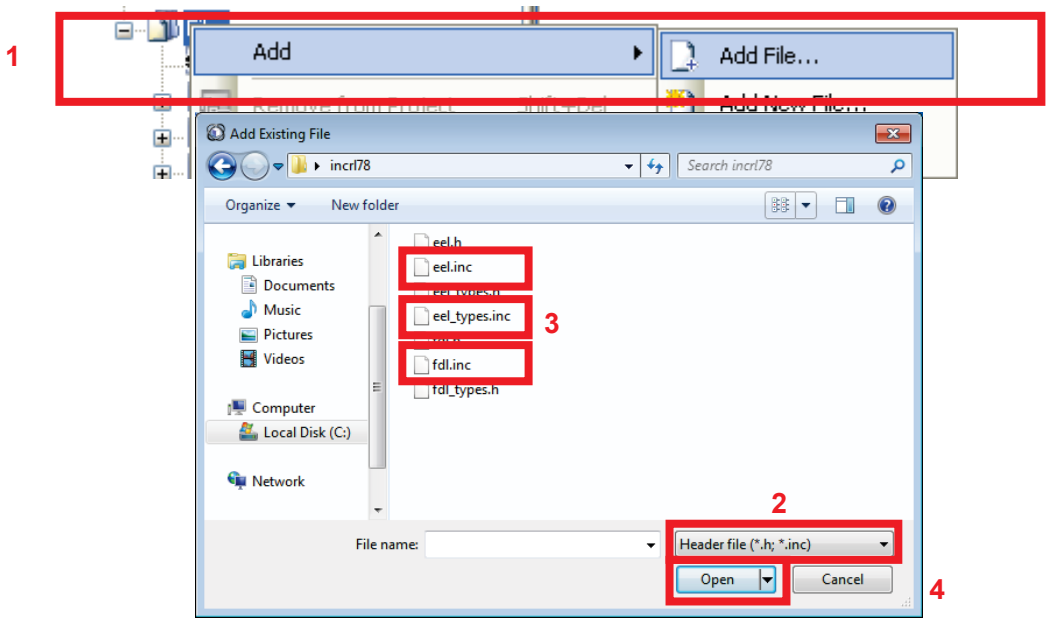
Figure 6-5. Specifying the Assemble Files



(2) Specifying the include file

In the CS+ Project Tree window, right-click the File node, click Add, and then click Add File.
The Add Existing File dialog box is displayed (as shown in Figure 6-6).
Click the Files of type drop-down list, select Header file (*.h;*.inc), and then register the header files and descriptor header files for the EEPROM emulation library and data flash library (eel.h, eel_types.h, fdl.h, fdl_types.h, eel_descriptor.h, fdl_descriptor.h, and eel_user_types.h)
include files and the descriptor include files for the EEPROM emulation library and data flash library (eel.inc, eel_types.inc, fdl.inc, eel_descriptor.inc, fdl_descriptor.inc).

Figure 6-6. Specifying the Include Files

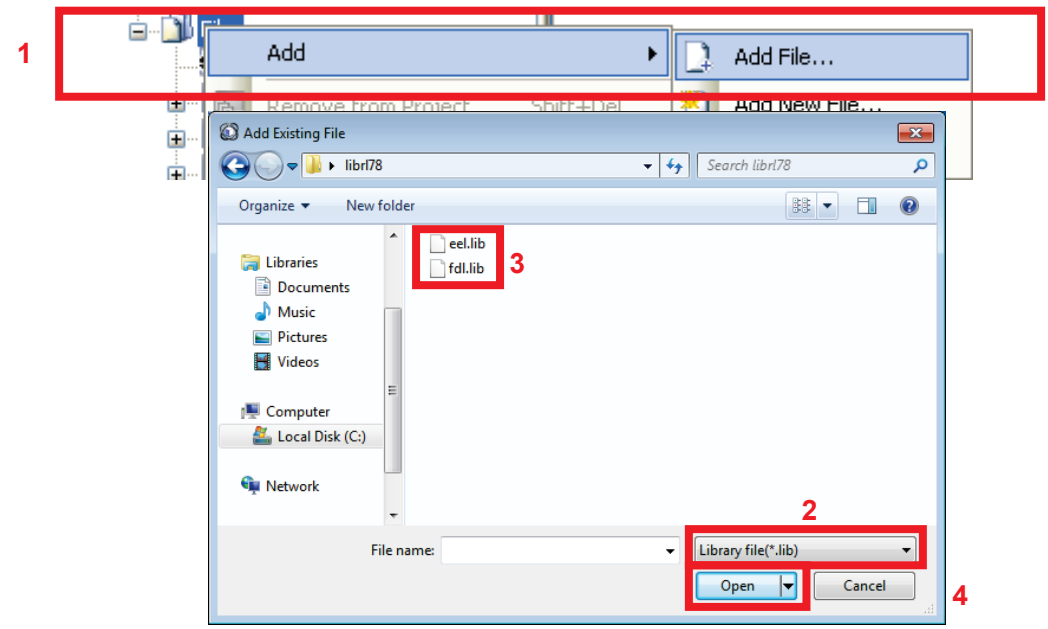


(3) Specifying the library file

In the CS+ Project Tree window, right-click the File node, click Add, and then click Add File. The Add Existing File dialog box is displayed (as shown in Figure 6-7).

Click the Files of type drop-down list, select Library file (*.lib), and then register the EEPROM emulation library and data flash library files (eel.lib and fdl.lib).

Figure 6-7. Specifying the Library Files

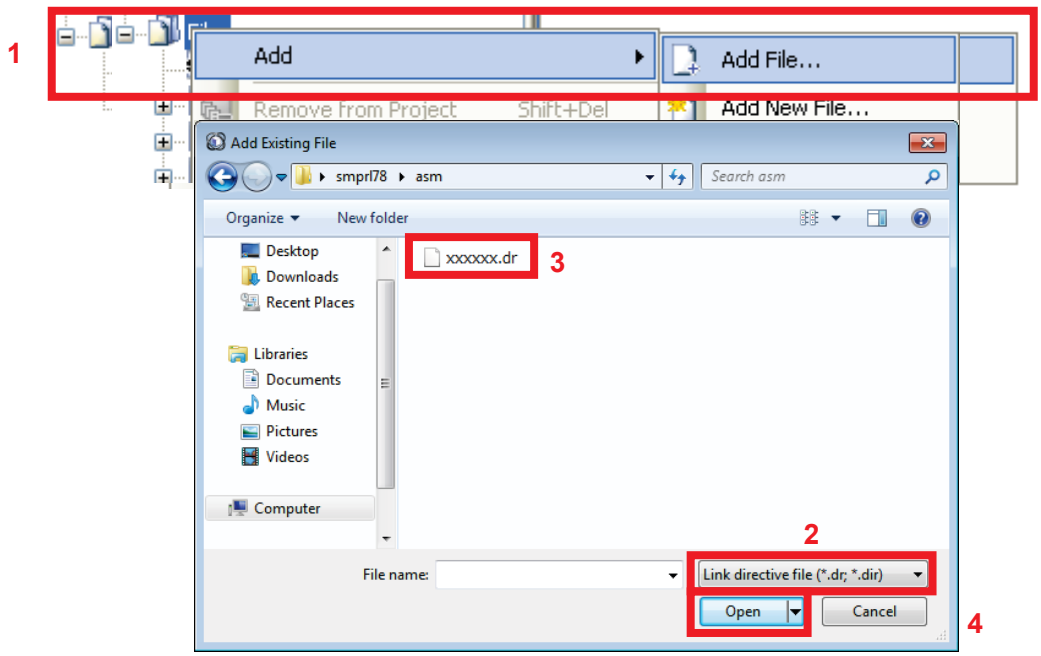


(4) Specifying the link directive file

In the CS+ Project Tree window, right-click the File node, click Add, and then click Add File. The Add Existing File dialog box is displayed (as shown in Figure 6-8).

Click the Files of type drop-down list, select Link Directive File (*.dr;*.dir), and then register the link directive file that has the same name as the user-created program.

Figure 6-8. Specifying the Link Directive File



(5) Building

On the CS+ Build menu, click Build Project to build the project.

6.3 Note at Build

(1) When the on-chip debugging function is in use

After the on-chip debugging function is enabled in the CS+, building a program generates the following type of error.

```
RA78K0R error E3212: Default segment can't allocate to memory - ignored
                     Segment '??OCDROM' at xxxxxH-200H
```

This error occurs when the segment for the monitor area (OCDROM) used by the on-chip debugging function cannot be allocated. Therefore, to avoid this error, add the following code to the link directive file (*.dr) embedded in the project and prepare a separate area for allocating the segment.

```
MEMORY OCD_ROM : ( 0xxxxxH, 00200H )
```

Notes: 1. xxxxx: Start address of the location where the error occurred

2. The area name “OCD_ROM” is an example of the notation.

Chapter 7 How To Debug a Program

For details about how to perform debugging by using IECUBE or the on-chip debug emulator E1 or E20, see the following document. Download the following document from the “Documentation” tabbed page at the “CS+” link from the “IDEs and Project Managers” page on the Renesas Electronics Web site.

Title
CubeSuite+ Integrated Development Environment User’s Manual: RL78 Debug
CS+ Integrated Development Environment User’s Manual: RL78 Debug Tool

7.1 Notes at Debug

The following describes notes apply when using the EEPROM Emulation Library Pack02 with the E1 or E20 on-chip debugging emulator.

(1) When a command of the EEPROM Emulation Library Pack02 Ver. 1.01 is executed in a version older than CubeSuite+ Ver. 1.01 and the E1 or E20 on-chip debugging emulator is in use, do not execute a break until you have confirmed completion of the command by the sequencer. The sequencer will malfunction if a break occurs before the sequencer has completed the command.

(2) The simulator cannot be used to debug the flash library.

Chapter 8 Sample Program

The attached sample program (r_eel_sample_c.c) is provided to enable the usage method of the EEPROM Emulation Library Pack02 to be easily confirmed on the QB-R5F100LE-TB boards with R5F100LEA (RL78/G13) as the target microcontrollers. The sample program is just a reference example and the user program does not have to be created to match the sample program. The sample program should be used as a simple program to confirm operation.

The link directive file (r_eel_sample_c.dr) for the sample program has a purpose to specify that a stack or data buffer used by the sample program is not allocated to an area where allocation is prohibited Note1. When using the sample program, this file should also be embedded with the sample program.Note2

Notes: 1. For details, refer to chapter 6.2 “Software Resource” in the user’s manual.

2. The data in usage may be placed at an unintended area depending on how the environment in use or the program is changed. After an execution module is generated, the map file and allocation state of programs or data must be confirmed. For the definition method and allocation conditions of each code or data, refer to the user’s manual of the CS+.

8.1 Initial Settings of the Sample Program

The sample program operates with the following initial settings. When these settings need to be changed, modify the sample program.

- CPU operating frequency: High-speed on-chip oscillator 32 MHz
- Voltage mode: Full-speed mode

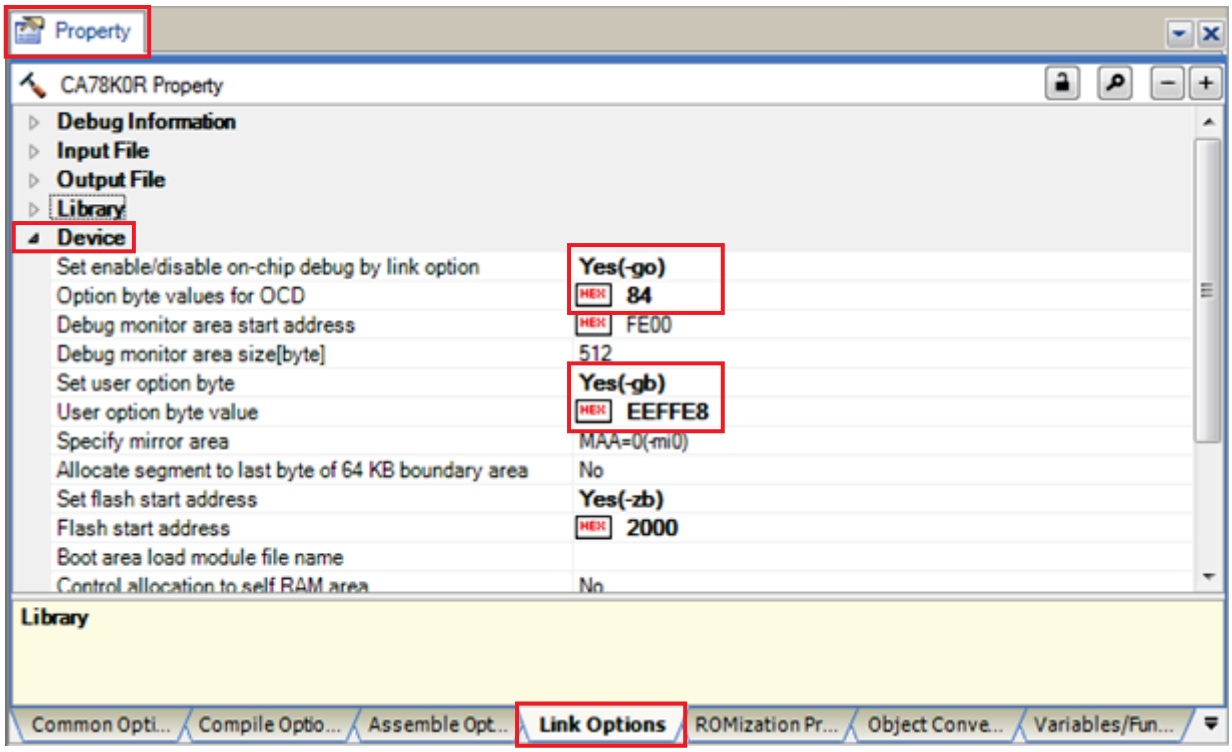
8.2 Settings of Option Byte and On-Chip Debugging

The sample program normally operates by setting the high-speed on-chip oscillator at 32 MHz.

After setting “Set user option byte” to “Yes” from the Link options of CA78K0R, specify “xxxxE8” for the value of the user option byte and set the high-speed on-chip oscillator at “32 MHz”.

When performing on-chip debug, set “Use on-chip debug” to “Yes” and specify “84” for ”Option byte values for OCD”.

Figure 8-1 Setting of Option Byte



8.3 Defining the On-Chip RAM Area

The following describes how to define the on-chip RAM area in the link directive file.

Normally, the entire on-chip RAM area is automatically defined as an area with the name "RAM" unless otherwise stated in the link directive file. The stack and data buffers are to be allocated to this area except when specifically stated otherwise[Note]. However, in this case, the stack and data buffers would be allocated by default to an area (FFE20H to FFEDFH in self-RAM) for which use by the EEPROM Emulation Library Pack02 is prohibited, so the program may not run correctly.

In the attached link directive file for the sample program, as a solution, re-define the area with the name "RAM" so that it does not include the above area, ensuring that stack and so on are not allocated to the area for which usage is prohibited.

```
MEMORY RAM          :(0FF300H, 000B20H)
```

The above statement redefines the area with the name "RAM" to be the B20H bytes area starting from the address FF300H (FF300H to FFE1FH)[Note]. This prevents attempted use of the area which the EEPROM Emulation Library Pack02 is prohibited to use by excluding the prohibited portion from the area with the name "RAM".

However, if this is the only change setting that is explicitly made, the area from FFE20H to FFEDFH is also unusable for any other purpose. Accordingly, separately add the following definition. No particular restrictions apply to the name of this area.

```
MEMORY SADDR_RAM:(0FFE20H, 0001E0H)
```

If there is a self-RAM area, automatic allocation of variables to this area can be restricted by defining its range as an area with the name "SELFRAM".

```
MEMORY SELFRAM    :(0FEF00H, 000400H)
```

An example of the settings for an RL78/G13 (the product with 4 KB of RAM and 64 KB of ROM) is given below.

(In this example, the general-purpose register and the SFR area are included in RAM_SADDR, however, they can be omitted.)

```
; ---------------------------------------------------------
; Define new memory entry for Self-RAM
; ---------------------------------------------------------
MEMORY SELFRAM     : ( 0FEF00H, 000400H )   <-- Definition of the self-RAM area

; ---------------------------------------------------------
; Redefined default data segment RAM
; ---------------------------------------------------------
MEMORY RAM         : ( 0FF300H, 000B20H )   <-- Definition of the RAM area to be used normally

; ---------------------------------------------------------
; Define new memory entry for saddr area
; ---------------------------------------------------------
MEMORY RAM_SADDR : ( 0FFE20H, 0001E0H )     <-- Definition of the area from FFE20H to FFFFFH
```

Note: The CA78K0R linker allocates data with a non-specified destination for allocation (segment types DSEG and BSEG) to the on-chip RAM area according to the re-allocation attribute of the data. Accordingly, specific data may not be allocated to the area with the name “RAM” in some situations.
For details on the methods of defining and allocating the individual categories of data, refer to the user’s manual for CS+.
Reference to the map file (*.map) generated at the time of building is required to confirm the state of allocation.

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