LVDS 接口学习笔记

作者：周始勇/Joe Zhou

介绍

Hello and welcome to TI Precision Labs. In this series, we're going to discuss Low Voltage Differential Signaling or LVDS for short. In this first session, we'll go over the fundamentals of LVDS-- what it is, how it works, and where it can be used. This will include the architecture, electrical characteristics, and application use cases. In future sessions, we will discuss variants of LVDS like multidrop LVDS and multipoint LVDS.

大家好，欢迎来到 TI Precision Labs。在本系列中，我们将讨论低压差分信号（简称 LVDS）。在第一部分中，我们将介绍 LVDS 的基本原理--它是什么、如何工作以及可用于何处。其中包括架构、电气特性和应用案例。在以后的课程中，我们将讨论 LVDS 的变体，如多点 LVDS 和多点 LVDS。

LVDS can be used in many ways depending on the system needs. There's the typical redriver/receiver pair. But there
are also transceivers for full duplex and half duplex communication and buffers for simply buffering the LVDS signals. Since LVDS can be used virtually any time there's a need to transport a signal from one point to
another, LVDS applications are ubiquitous, which makes it a popular interface.

LVDS 可根据系统需要以多种方式使用。有典型的再驱动器/接收器对。此外，还有用于全双工和半双工通信的收发器，以及用于简单缓冲 LVDS 信号的缓冲器。由于 LVDS 几乎可以在任何需要将信号从一个点传输到另一个点的时候使用，因此 LVDS 应用无处不在，这也使其成为一种流行的接口。

LVDS stands for Low Voltage Differential Signaling and is defined by TIA/EIA-644 standard. It
is a physical layer only, which means that it is purely electrical with no protocol for transferring data. We can see this by simply observing its architecture.

LVDS 是低压差分信号的缩写，由 TIA/EIA-644 标准定义。它只是一个物理层，这意味着它纯粹是电气层，没有传输数据的协议。我们只要观察一下它的结构就能明白这一点。

Its most basic form consists of a differential transmitter and differential receiver. Instead of measuring the difference between the signal and ground, like with single-ended signaling, LVDS measures the difference between the non-inverting and inverting levels of the signals.

其最基本的形式由差分发送器和差分接收器组成。LVDS 不像单端信号那样测量信号与地之间的差值，而是测量信号的非反相电平与反相电平之间的差值。

A termination resistor is placed at the end of the transmission line to terminate the signal. This termination resistor as well as the LVDS driver current is what generates differential voltage. This resistor must match the characteristic impedance of the transmission line. Typically, it'll be 100 ohms.

传输线末端有一个终端电阻器，用于终止信号。该终端电阻和 LVDS 驱动器电流产生差分电压。该电阻必须与传输线的特性阻抗相匹配。通常为 100 欧姆。

The resistor creates a stub in the transmission line, which can cause reflections. So the resistors should be placed as close to the receiver as possible to minimize the stub length. The signals are also centered around the common-mode voltage of 1.2 volts offset from the ground.

电阻器会在传输线上产生一个残端，从而导致反射。因此，电阻器应尽可能靠近接收器放置，以尽量减少残端长度。信号也以偏离地面 1.2 伏的共模电压为中心。

1.2 volts is typical for 2.5-volt, 3.3-volt 5-volt powered devices. However, other unofficial standards, like sub-LVDS, use the smaller offset voltage of 0.9 volts as they are powered off of a 1.8-volt supply.

1.2 伏通常用于 2.5 伏、3.3 伏和 5 伏供电设备。不过，其他非官方标准（如 sub-LVDS）使用的偏

移电压较小，为 0.9 伏，因为它们是由 1.8 伏电源供电的。

AC coupling can be used to isolate drivers and receivers that require different common-mode voltages. Speaking of AC coupling, if you've watched our previous TI PL video on display port, then this architecture should look familiar to you. Display port's physical layer is just AC coupled LVDS.

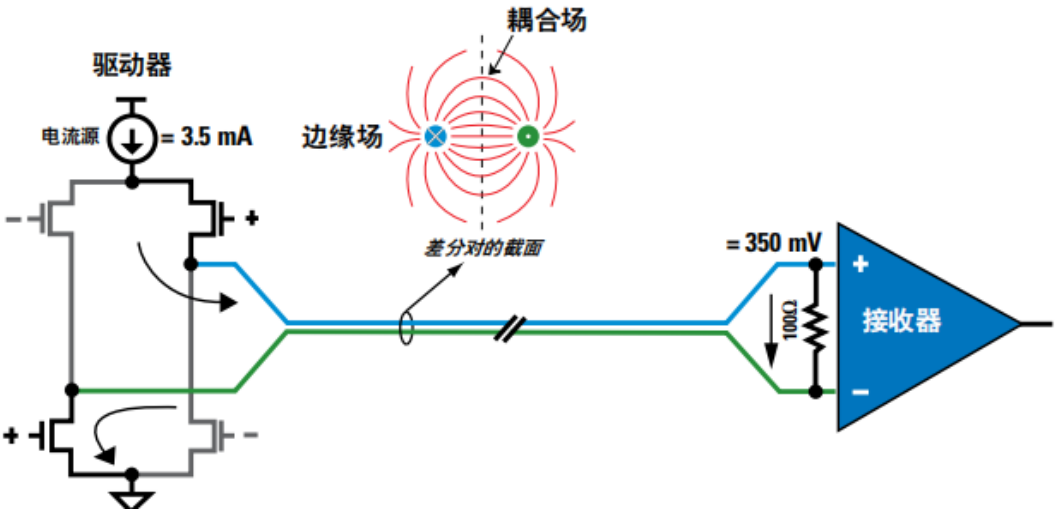
交流耦合可用于隔离需要不同共模电压的驱动器和接收器。说到交流耦合，如果您看过我们之前关于显示端口的 TI PL 视频，那么您应该会对这种架构感到熟悉。显示端口的物理层就是交流耦合 LVDS。

The source is the driver, and the sink is the receiver. One key difference between standard LVDS and display port is that display port is double-terminated with termination on both the source and the sink instead of just the sink. This is only a requirement for the DP standard and is not something you would typically see in other AC-coupled LVDS interfaces. There are other TI PL videos that go into more details about this interface. Links to these videos are provided at the end of the presentation.

源是驱动器，汇是接收器。标准 LVDS 与显示端口的一个主要区别是，显示端口是双端接的，源端和汇端都有端接，而不是只有汇端才有端接。这只是 DP 标准的要求，在其他交流耦合 LVDS 接口中通常看不到这一点。还有其他 TI PL 视频更详细地介绍了这种接口。演示文稿末尾提供了这些视频的链接。

Now, let's take a deeper look into the inner workings of LVDS. The driver has a 3.5 milliamp push-pull mode current source. And each line in the differential pair carries the 3.5 milliamps in opposite directions.

现在，让我们深入了解一下 LVDS 的内部工作原理。驱动器有一个 3.5 毫安推挽模式电流源。差分对中的每条线路都以相反的方向传输 3.5 毫安的电流。

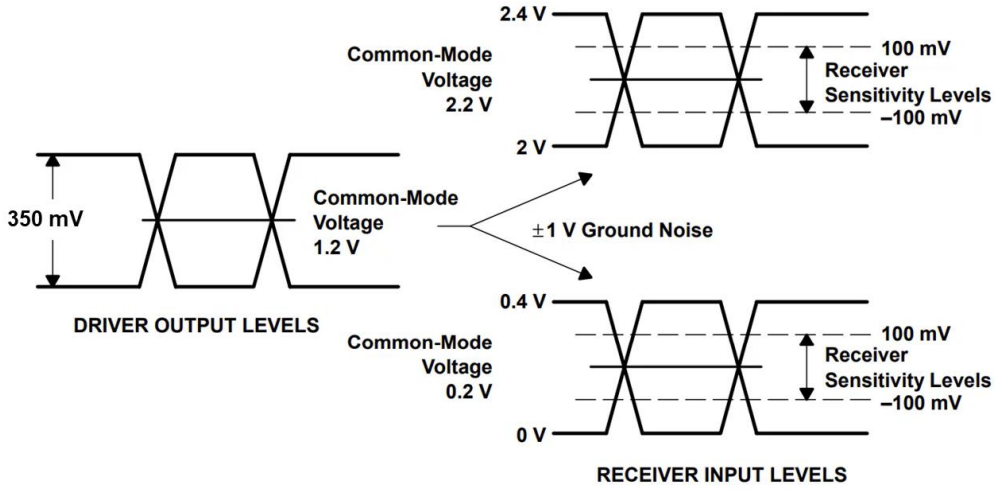


The output driver sets the common-mode voltage for the DC signals, and the receiver input is very high impedance. So virtually, all the current flows through the 100-ohm termination resistor. This, in turn, is what generates the differential voltage of 350 millivolts across the receiver inputs.

输出驱动器为直流信号设置共模电压，而接收器的输入阻抗非常高。因此，实际上所有电流都流经 100 欧姆的终端电阻。这反过来又在接收器输入端产生了 350 毫伏的差分电压。

A compliant receiver is specified to tolerate a minimum of plus or minus 1 volt of ground shift between driver ground and receiver ground. Since a typical driver is specified to have a common-mode voltage of 1.2 volts, this means the receiver will have a common-mode range of 0.2 volts to 2.2 volts. So if the driver and the receiver on different boards with different power supplies, the receiver will still be able to receive signals from the driver even with differences in ground potential.

符合标准的接收器可承受驱动器地线与接收器地线之间至少正负 1 伏的地线偏移。由于典型驱动器的共模电压为 1.2 伏，这意味着接收器的共模电压范围为 0.2 伏至 2.2 伏。因此，如果驱动器和接收器在不同的电路板上，且电源不同，即使地电位不同，接收器仍能接收驱动器的信号。

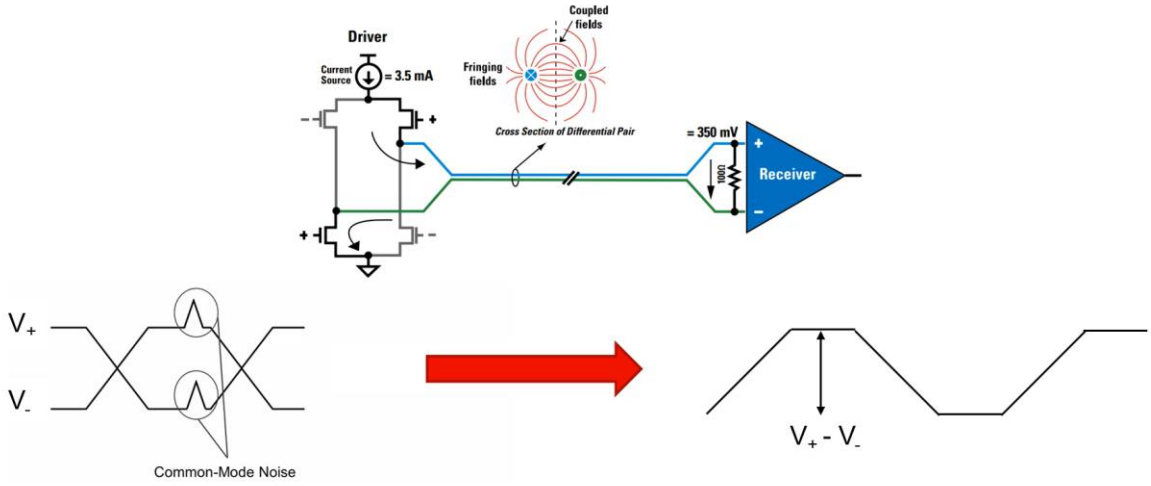


Additionally, the receiver is guaranteed to have a receiver threshold of 100 millivolts or less. The typical driver will have a differential voltage of 350 millivolts, which allows for almost 6 dB in losses caused by PCB traces or cables.

此外，接收器的接收阈值保证在 100 毫伏或更低。典型驱动器的差分电压为 350 毫伏，可减少 PCB 线路或电缆造成的近 6 分贝损耗。

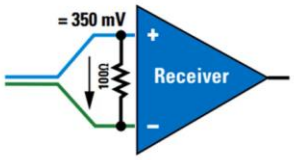
One major benefit of LVDS is noise immunity. Since the lanes are tightly coupled together, noise that appears on one lane will likely also be present on the other lane. This noise is canceled out since the receiver only responds to the differences between the two signals.

LVDS 的一个主要优点是抗噪。由于各通道紧密耦合在一起，一条通道上出现的噪声很可能也会出现在另一条通道上。由于接收器只对两个信号之间的差分做出响应，因此噪音会被抵消。



Because of the low-voltage nature of LVDS, another benefit is the low power. We can see this by taking a look at some quick calculations with some typical specifications from an LVDS driver datasheet. The power dissipated is 1.225 milliwatts. The input power is 23.1 milliwatts. And the power consumption is 10.325 milliwatts. Combining these, the total device power is only 33.425 milliwatts.

由于 LVDS 的低电压特性，它的另一个优点是功耗低。我们可以通过快速计算 LVDS 驱动器数据表中的一些典型规格来了解这一点。耗散功率为 1.225 毫瓦。输入功率为 23.1 毫瓦。功耗为 10.325 毫瓦。综合计算，设备总功率仅为 33.425 毫瓦。



- $P_d = \frac{V_{diff}^2}{R} = \frac{(350mV)^2}{100\Omega} = 1.225mW$
- $P_i = V_{DD} \times I_{DD} = 3.3V \times 7mA = 23.1mW$
- $P_o = V_{DD} \times I_{OD} = 3.3V \times 3.5mA = 11.55mW$
- $P_c = P_o - P_d = 10.325mW$
- $\boldsymbol{P_T = P_c + P_i = 33.425mW}$

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{DD})	3.0	3.3	3.6	V
Temperature (T_A)	-40	+25	+85	°C

I_{DD}	Power Supply Current	No Load	V_{IN} = V_{DD} or GND	V_{DD}		5	8	mA
		R_L = 100Ω				7	10	mA

Now, one of the most frequently asked questions is just how far and how fast can LVDS go? Typically, the ba ndwidth is a little more than one gigabits per second at 10 to 15 meters of distance with no signal conditioning. Un fortunately, this is very much a system-dependent parameter, so we can only give typical specs for these parameter s.

现在，一个最常见的问题是，LVDS 的传输距离有多远、速度有多快？通常情况下，在没有信号调节的情况下，10 至 15 米距离内的带宽略高于每秒千兆比特。遗憾的是，这在很大程度上取决于系统参数，因此我们只能给出这些参数的典型规格。

The best way to determine what the actual max speed and max distance is is to measure them in the system ei ther through simulation or with a prototype system. For example, a typical setup will include a BERT or function generator, EVMs, various length cables, and an oscilloscope.

确定实际最大速度和最大距离的最佳方法是通过模拟或原型系统在系统中进行测量。例如，典型的设置包括 BERT 或函数发生器、EVM、不同长度的电缆和示波器。

With the prototype setup, you can take eye
diagram measurements at the load to determine the max amount of jitter allowed for error-free transmission. You c an also use the eye diagram height to determine whether or not the 100 millivolt threshold for the receiver is being met.

利用原型设置，您可以在负载处进行眼图测量，以确定无差错传输所允许的最大抖动量。您还可以使用眼图高度来确定接收器是否达到 100 毫伏阈值。

For a recap of eye diagrams, a link to previous TI PL videos is provided at the end of the presentation. Be sur e to visit our E2E support forums at TI.com/E2E where we can help answer questions about designing with interfa ce technologies. Please also reference the previous TI PL videos like our videos on display port and eye diagrams.

如需回顾眼图，可在演示文稿末尾链接到以前的 TI PL 视频。请务必访问我们在 TI.com/E2E 上的 E2E 支持论坛，我们可以帮助您解答有关使用接口技术进行设计的问题。还请参考以前的 TI PL 视频，如关于显示端口和眼图的视频。

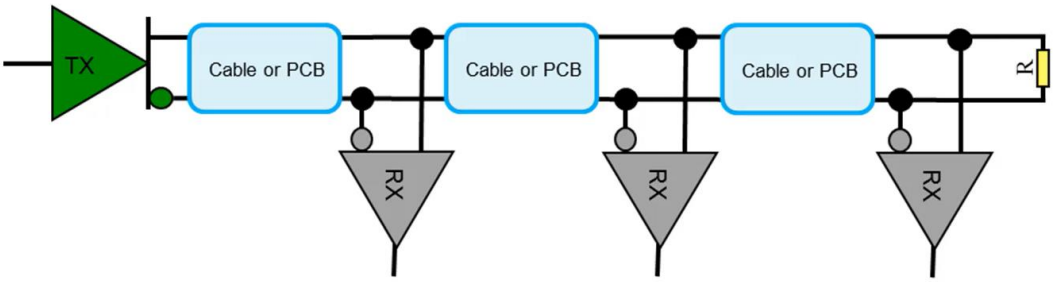
多路 LVDS

Hello in
the TI Precision Labs. In this series, we are going to discuss low voltage differential signaling-- or LVDS for short . In this session, we will go over the fundamentals of multidrop LVDS-- what it is, how it works, and where it can be used. This will include the architecture, electrical characteristics, and design considerations. If you have not wa tched the first part of this series, "What is LVDS?," please watch that before continuing this video.

Multidrop LVDS is defined by the TIA/EIA-644-A standard, which is an update of the TIA/EIA-644 standar

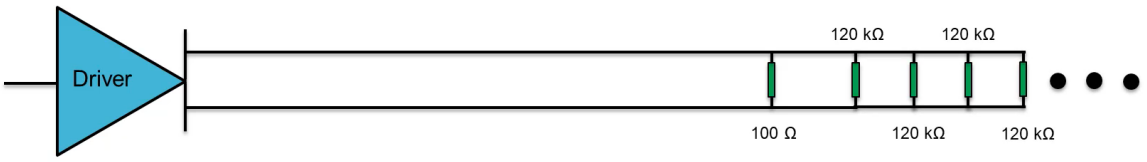
d that defines point-to-point LVDS. The update allows for up to 32 receivers to be connected to one driver and req uires only one termination resistor at the furthest receiver. Just like with regular LVDS, it's a physical layer only, which means it's purely electrical. The electrical characteristics are, for the most part, the same as regular point-to-point LVDS. The driver is typically a 3.5 milliamp current source that generates a 350 millivolt swing signal cente red around 1.2 volts when terminated with 100 ohms at the receiver.

多路 LVDS 由 TIA/EIA-644-A 标准定义，是对定义点对点 LVDS 的 TIA/EIA-644 标准的更新。更新后，一个驱动器最多可连接 32 个接收器，最远的接收器只需一个终端电阻。与普通 LVDS 一样，它只是一个物理层，这意味着它是纯电气的。大部分电气特性与普通点对点 LVDS 相同。驱动器通常是一个 3.5 毫安的电流源，当接收器端接 100 欧姆时，可产生以 1.2 伏特为中心的 350 毫伏摆幅信号。



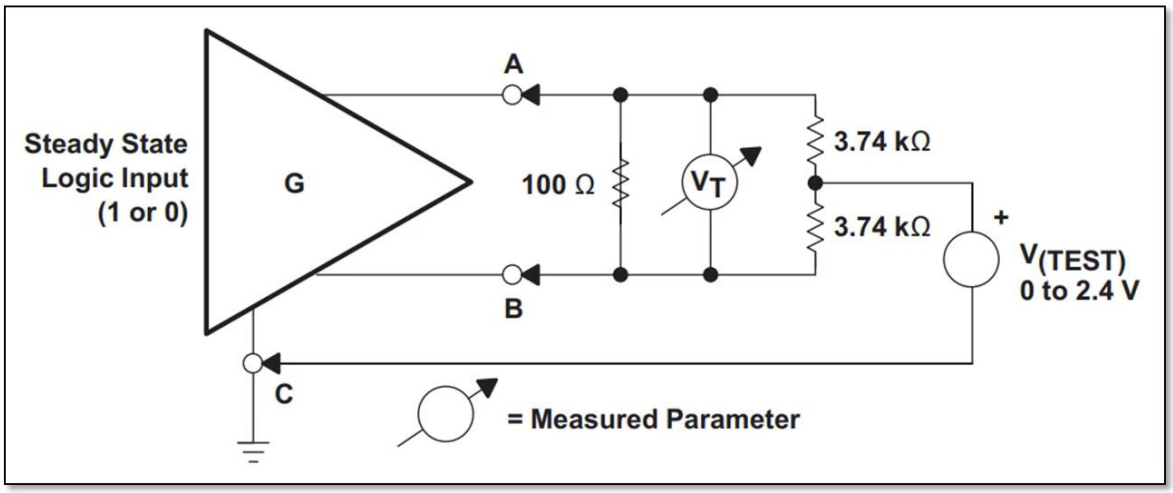
The key difference between the 644 standard and the 644-A standard is the addition of a leakage current limit ation spec. The 644-A standard requires receiver inputs to have less than 20 microamps of leakage current to ensu re that the receiver is high impedance across the entire common mode range. This ensures that the receiver is high impedance at least 120 kohm across the entire common mode range. This is important, because due to the increase d load of multiple receivers, the effective impedance that the driver sees is lowered. Think of multiple resistors bei ng connected in parallel.

644 标准与 644-A 标准的主要区别在于增加了漏电流限制规格。644-A 标准要求接收器输入的漏电流小于 20 微安，以确保接收器在整个共模范围内具有高阻抗。这确保接收器在整个共模范围内至少具有 120 千欧的高阻抗。这一点非常重要，因为由于多个接收器的负载增加，驱动器看到的有效阻抗会降低。就像多个电阻器并联一样。



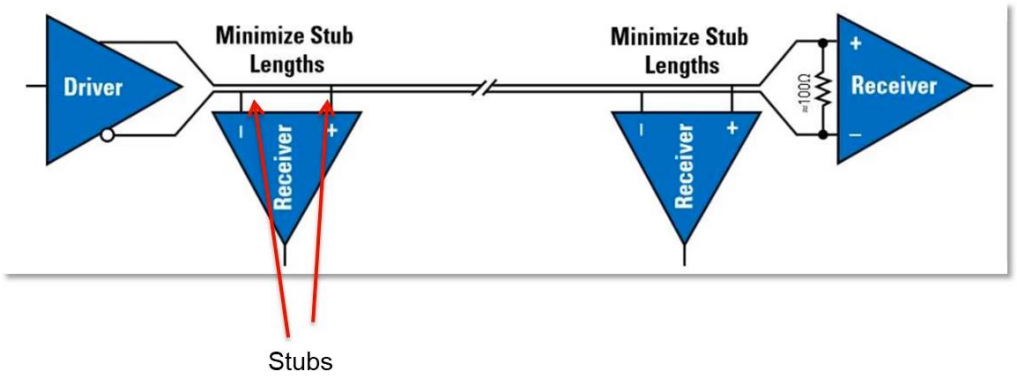
Remember, we want the receiver impedance to be as high as possible so that virtually all of the current flowi ng from the driver goes through the termination resistor to generate the differential voltage. You can see this illustr ated in the test circuit depicted in the 644-A standard. The 3.74 kilo ohm represents 32 receiver nodes-- 120 kilom eter each-- connected to one driver, and the
V Test represents the common mode voltage range of the receiver. The same design considerations as normal LVD S also apply to multidrop LVDS, with some additional parameters.

请记住，我们希望接收器的阻抗越高越好，这样从驱动器流出的几乎所有电流都会通过终端电阻产生差分电压。您可以从 644-A 标准中描述的测试电路中看到这一点。3.74 千欧代表 32 个接收器节点（每个节点 120 千欧）连接到一个驱动器，V 测试代表接收器的共模电压范围。与普通 LVDS 相同的设计考虑因素也适用于多路 LVDS，只是增加了一些参数。



The most important consideration is the stub length. Stubs are created each time an additional receiver is con nected to a driver. It is very important to keep this stub
lengths as short as possible because they create impedance mismatches that have a significant impact on signal int egrity. As a rule of thumb, stubs should be kept to less than
4 centimeters. So how many receivers can a driver really support?

最重要的考虑因素是**存根**长度。每次将额外的接收器连接到驱动器时，都会产生存根。尽可能缩短存根长度非常重要，因为存根会产生阻抗失配，对信号完整性产生重大影响。根据经验，存根长度应小于 4 厘米。那么，一个驱动器到底能支持多少个接收器呢？



Well, the theoretical max numbers of receivers supported by the spec is 32, but in practice, this number may be much lower. It is heavily dependent on the system, specifically stub
length, signal frequency, and trace or cable length. Signal integrity challenges caused by stubs as well as the numb er of receivers connected also limits the max data rate to 250 megabits per second in most instances.

理论上，规范支持的最大接收器数量是 32 个，但在实际应用中，这个数字可能会低得多。这在很大程度上取决于系统，特别是存根长度、信号频率以及**跟踪**或电缆长度。在大多数情况下，由存根和所连接的接收器数量引起的信号完整性挑战也将最大数据传输速率限制在每秒 250 兆比特。

As all of these parameters are dependent on each other, it is difficult to quantify them, as they're all very muc h system dependent. It's best to test the system with a prototype or simulate the system in an application environm ent. With a prototype set up, you can eye diagram measurements at the load to determine the max amount of jitter allowed for error-free transmission. You can also use the
eye diagram height to determine whether or not the 100 millivolt threshold for the receiver is being met.

由于所有这些参数都相互依赖，因此很难对其进行量化，因为它们在很大程度上都与系统有关。最好

使用原型测试系统或在应用环境中模拟系统。有了原型设备，您就可以在负载处进行眼图测量，以确定无差错传输所允许的最大抖动量。您还可以使用眼图高度来确定接收器是否达到 100 毫伏阈值。

For a recap of eye diagrams, a link to the [INAUDIBLE] Precision Lab videos is provided at the end of the presentation. Be sure to visit our E2E support forums at TI.com/E2E, where we can help answer questions about designing with interface technologies. Please also reference previous TI Precision Labs videos, like our video on eye diagrams, as well as our first video on LVDS.

Reference

[1] TI. Precision labs series: LVDS. Precision labs series: LVDS | TI.com

---

作者
周始勇/Joe Zhou[zhou_shiy_ong@163.com]
个人博客[github: zhoushiyong010718]
XX 电子科技有限公司 硬件工程师
嵌入式硬件爱好者