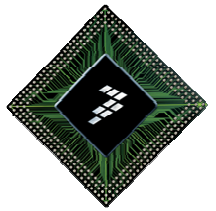
Dec., 2010

# i.MX28 Power management and L2 switch



Freescale / MX28 DFAE Training



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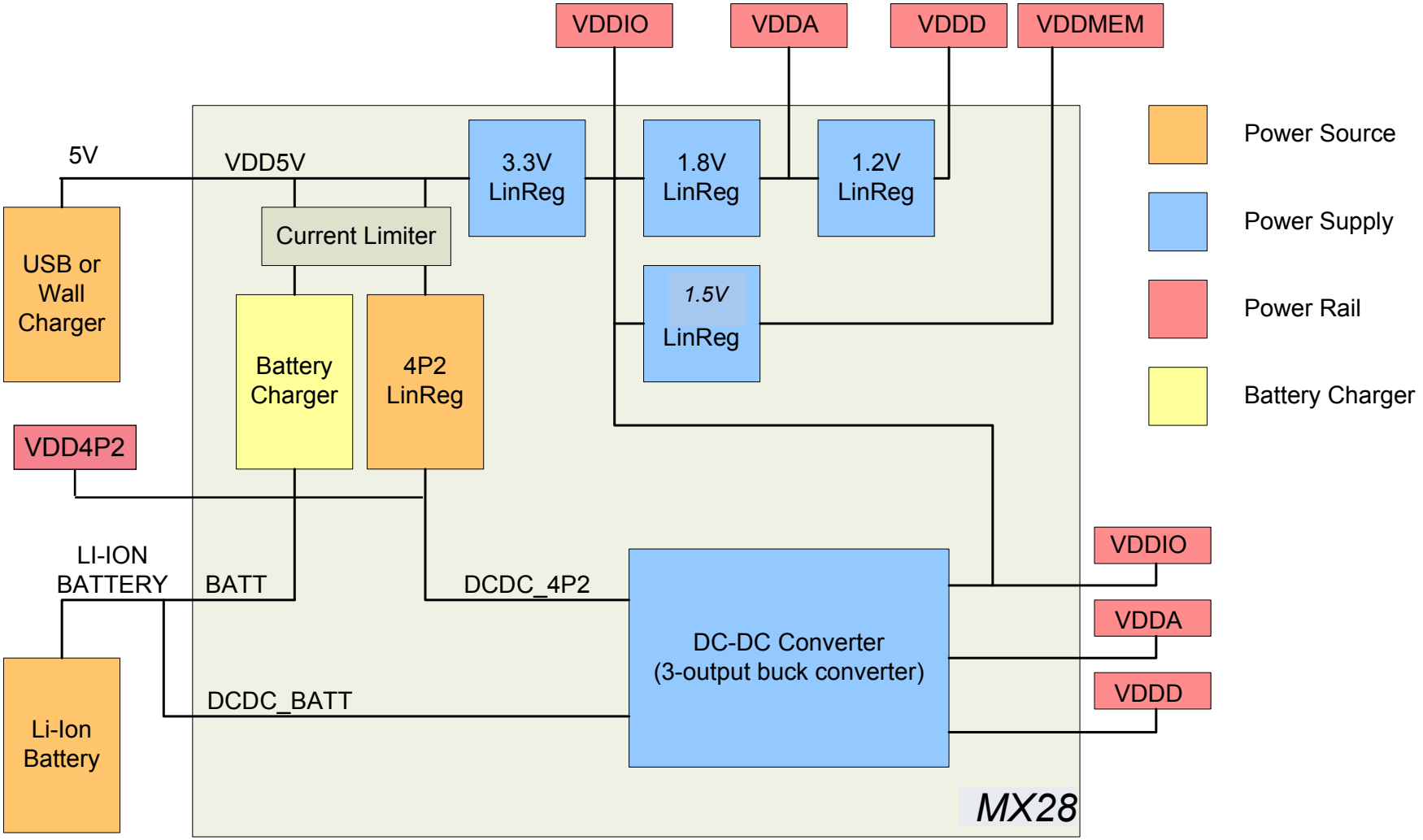
# i.MX28 - Power Management Unit

- Integration of a DC-DC switching converter and linear regulators that provide four output rails
  - Powers digital blocks and components such as system clocks
  - Powers I/O peripherals like NAND flash and SD/MMC cards
  - Powers 1.5V DDR2
- Power sources
  - Li-Ion batteries (2.9V – 4.2V)
  - Direct power from 5V source (USB, wall power or other source)
  - Internal 4.2V power source generated from 5V source
- Battery charging capability
  - Allows battery to be fully charged while device is in use
  - Current and voltage sensors allows firmware to monitor the voltage and current into the battery to determine “charged” status
- On-chip silicon speed and temp sensors
  - Hardware thermal protection and shutdown circuitry

# Interfaces of PMU



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# Battery Boot

- Li-Ion battery attached with no 5V present.
- Triggered by PSWITCH, RTC Alarm, or AUTO_RESTART bit
- Three stages of battery boot
  - Internal circuitry performs power-on sequence for rails and DC-DC
  - DC-DC takes control and provides power to rails.
  - Software executes and finishes DC-DC initialization and configuration

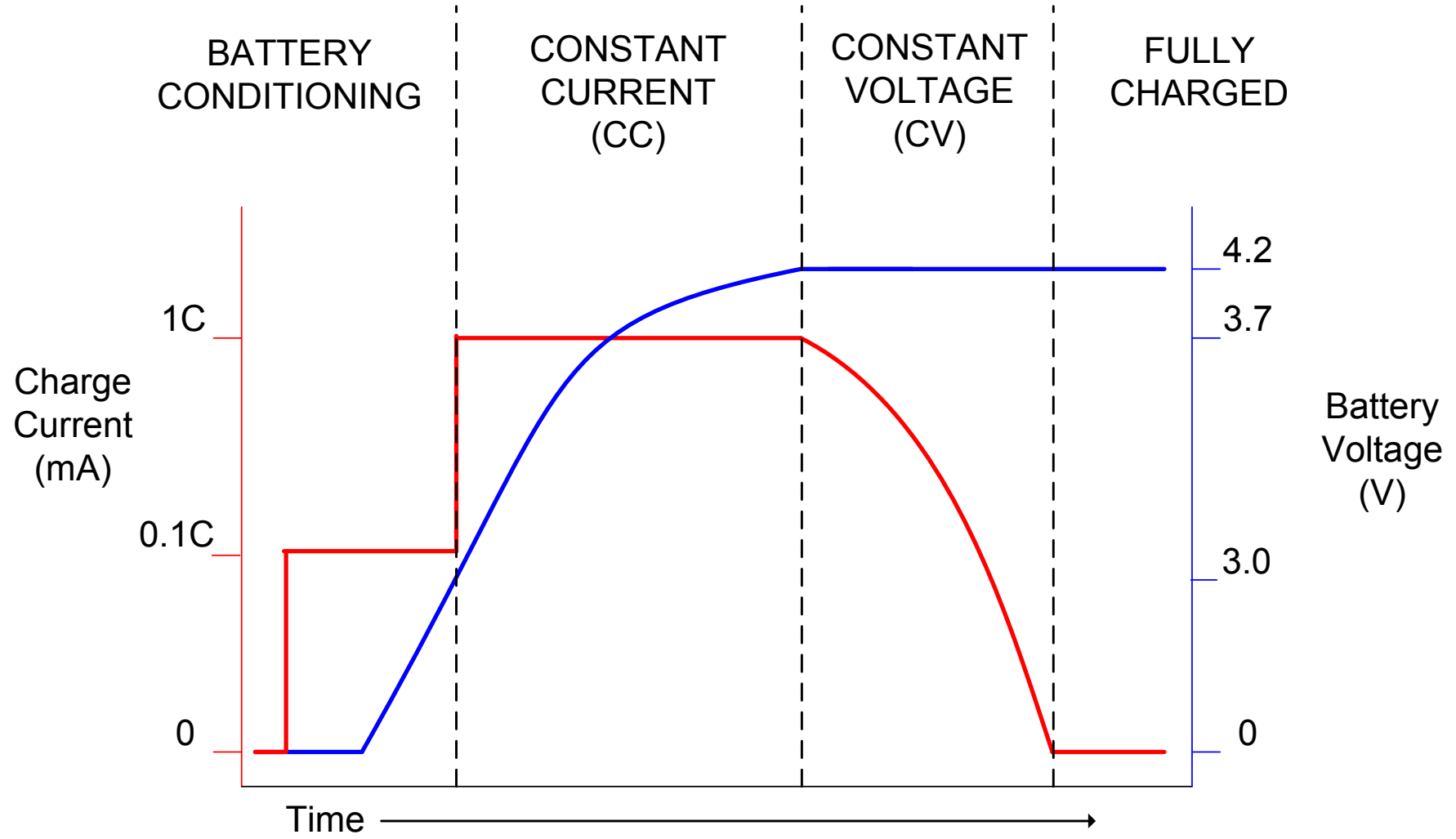
# 5V Boot

- VDD5V > ~3.9V causes chip to begin booting.
- Starts by using linear regulators, then switches to DC-DC power
- Three stages of 5V Boot
  - Internal PMU linear regulators pull output rails up to default levels.
  - Linear regulators supply output rail power.
  - DC-DC is initialized by software

# 5V Boot without Battery

- Same sequence as 5V boot except:
  - Device will shut down immediately when 5V is removed
  - 5V brownout enabled to shut down device.
  - Charger disabled

# Charging Profile





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# Battery Charger Options

- Charge Current
  - 0 – 780mA
- Stop Charge Current Threshold
  - 10 – 150mA
  - Clears status flag when current below threshold
- Charge Voltage
  - -1.00% to +0.75% from 4.2V in 0.25% increments

# *Frequent Questions*

- *Question: Is it possible to use MX28 w/o having a battery*.
  - *Answer: Yes. We have a special reference design showing this. Best way is to use 5V input on VDD5V pin. You must have 5V +-5%.*
- *Question: Can I also use 3.3V supply?*
  - Answer: Yes. *Use the BATT_DCDC input. Note: you must connect VDD_XTAL via 1K to PSWITCH. This triggers the startup w/o pressing the „start“ button (not the case on the EVK)*

# Operating States

**Table 2-12. Recommended Operating States - 169BGA Package**

| VDDD (V) | VDDD Brown-out (V) | HW_DIGCTRL ARMCACHE (note 1) | CPUCLK / clk_p Frequency (MHz) | HW_CLKCTRL CPU_DIV_CPU | HW_CLKCTRL FRAC_CPUFRC / PFD | AHBCLK / clk_h Frequency (MHz) | HW_CLKCTRL HBUS_DIV | EMICLK / clk_emi Frequency (MHz) | HW_CLKCTRL EMI_DIV_EMI | HW_CLKCTRL FRAC_EMIFRAC | SUPPORTED DRAM |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1.050 | 0.975 | | 24.00 | | | 24.00 | 1 | 24.00 | | | DDR, mDDR |
| 1.050 | 0.975 | 11 | 64.00 | 5 | 27 | 64.00 | 1 | 64.00 | 5 | 27 | DDR, mDDR |
| 1.275 | 1.175 | 00 | 261.82 | 1 | 33 | 130.91 | 2 | 130.91 | 2 | 33 | DDR, mDDR |
| 1.375 | 1.275 | 00 | 360.00 | 1 | 24 | 120.00 | 3 | 120.00 | 3 | 24 | DDR, mDDR |
| 1.475 | 1.375 | 00 | 392.73 | 1 | 22 | 196.36 | 2 | 130.91 | 2 | 33 | DDR, mDDR |
| 1.550 | 1.450 | 00 | 454.74 | 1 | 19 | 151.58 | 3 | 151.58 | 3 | 19 | mDDR |
| 1.550 | 1.450 | 00 | 454.74 | 1 | 19 | 151.58 | 3 | 130.91 | 2 | 33 | DDR |

# Power Consumption Calculator

- Add or remove configurations
  - Use pulldown menu to select “INCLUDE” or “EXCLUDE”
  - Use pulldown menu to select configuration values.
  - Refer to block diagram in calculator to see current/voltage definitions

- Results
  - Power Rail Summary
    - Estimated power used by each rail.  Includes internal and external consumers of power.
  - Total Power Summary
    - Estimated power used from the battery.
    - Final total accounts for DCDC efficiency.

- Validation through 0.02 Ohms resistors on EVK.

# Changing Clock Frequencies

- Use Linux sysfs to change the clock frequencies
  - cd /sys/devices/system/cpu/cpu0/cpufreq
- Check frequency
  - Minimum frequency: “cat scaling_min_freq”
  - Maximum frequency: “cat scaling_max_freq”
  - Current frequency: “cat scaling_cur_freq”
- Set frequency
  - Use “scaling_setspeed”
  - Ex. Set to 64MHz: “echo 64000 > scaling_setspeed”
  - Ex. Set to 261MHz: “echo 261818 > scaling_setspeed”

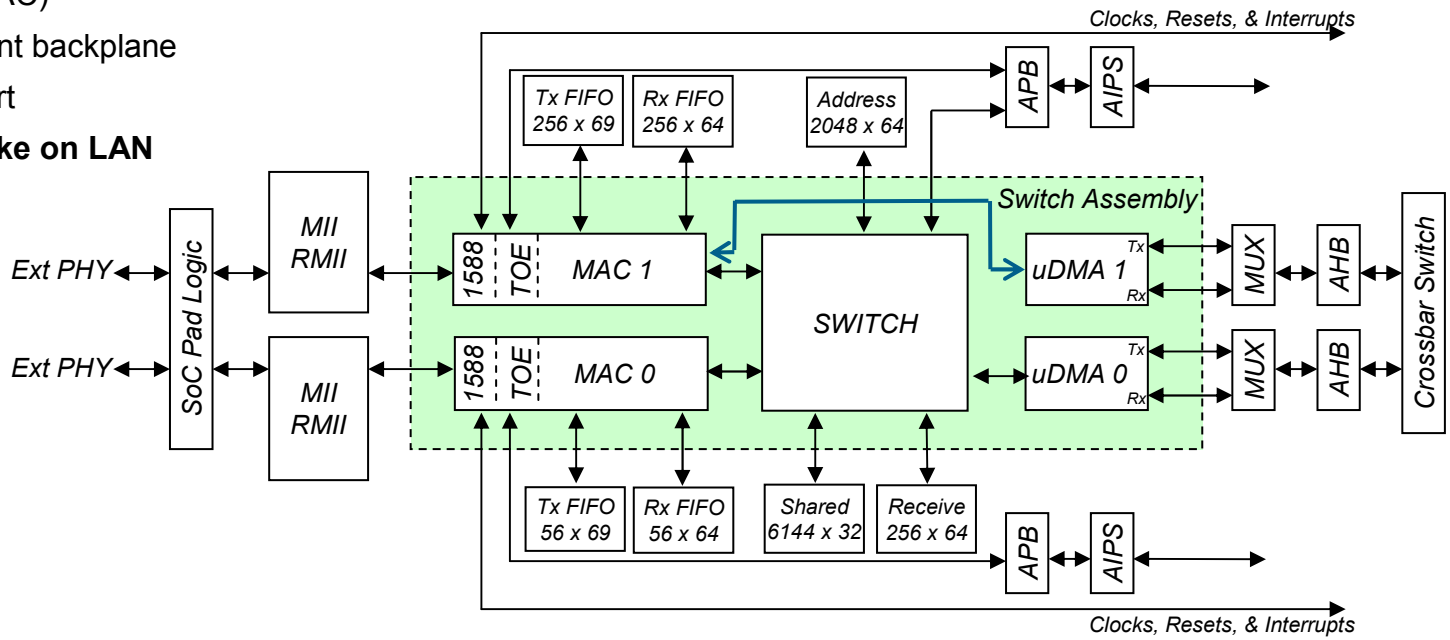
# L2 Switch

Product Features:

- **3 -Port Switch** (2 internals, one for bypass only)
- Separate dual-port FIFOs for max throughput
- TCP/IP Offload Engine (TOE)
- Hardware Time-stamping (IEEE 1588)
- Simple handshake programmable FIFO i/f
- Fast cut-through mode (MAC)
- Link aggregation, redundant backplane
- QoS with 8 queues per port
- Magic packet support, **Wake on LAN**
- Level 3 IP Snooping
- Port Mirroring

***System Benefits:***

- ***Cost-effective daisy-chain networks***
- ***Efficient ring networks with redundancy***
- ***Improved determinism using hardware time stamping of packets (1588)***





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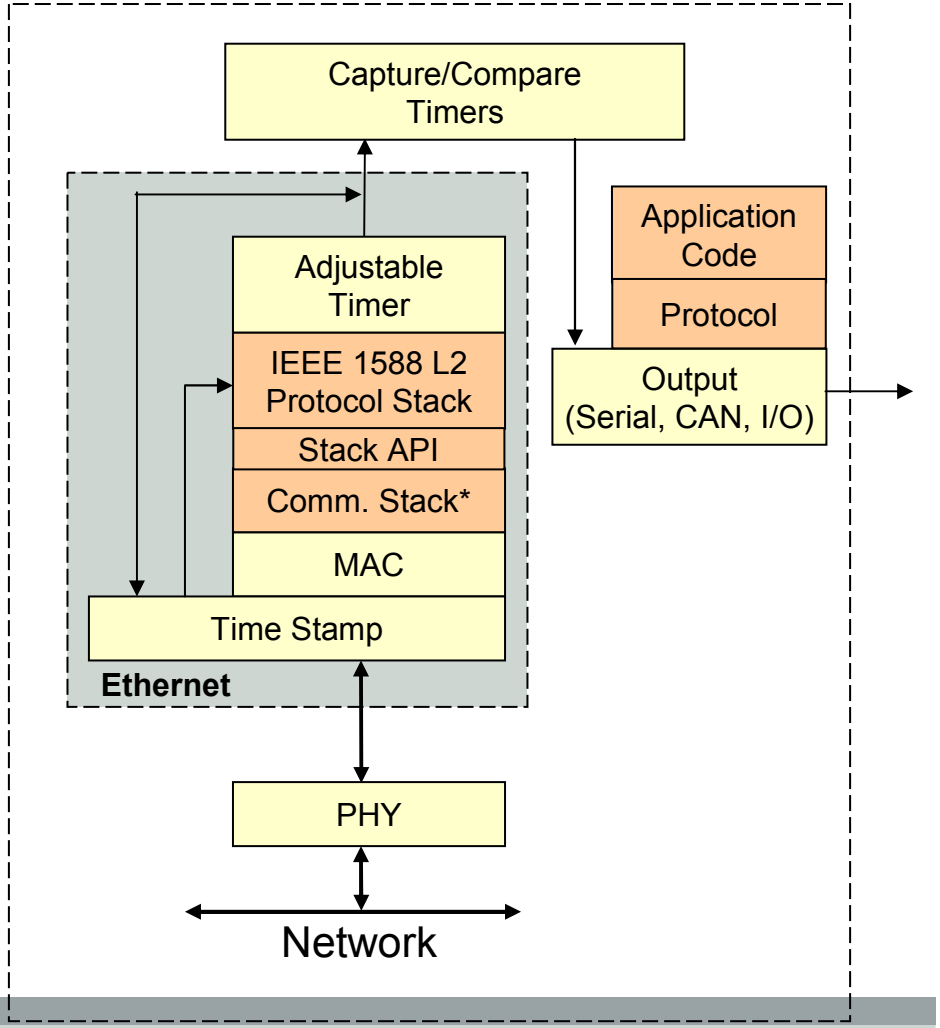
# IEEE1588 Real Time Ethernet

## HARDWARE

- The 1588 stack can adjust and update the internal timer used as a local clock reference.
- The 1588 time stamp is implemented as close to the external MAC as possible, to provide maximum precision.
- Each network connection can run independently, together, or with embedded L2 switch.
- Internal capture/compare timers allow for other outputs to be synchronized to the network time base.

## SOFTWARE

- Supports standard TCP/IP protocol, UDP protocol, and various proprietary protocols.
- Time Stamping (1588 based) stack easily integrated into new IP stacks using the API provided.



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# XXAT IEEE1588 Test procedure

- Two boards are needed which are connected back to back (with cross cables) through FEC0 or FEC1, one board run as master and the other runs as slave.FEC0 is used to transmit PTP message, and FEC1 is used to connect to NFS server
- Copy the application ptp_main to the /tmp directory of rootfs (CONFIG_FEC_1588 must be enabled in kernel)
- One board:

```
root@freescale ~$ cd /tmproot@freescale /tmp$ mknod /dev/ptp c 232 0
root@freescale /tmp$ ifconfig eth0 10.193.20.180 up
eth0: Freescale FEC PHY driver [Generic PHY] (mii_bus:phy_addr=0:00, irq=-1)
PHY: 0:00 - Link is Up - 100/Full
root@freescale /tmp$ ./ptp_main -d -o -m -l -w –z
IXXAT Automation Gmbh & FREESCALE=====================PTP IEEE1588-2008 stack for
IMX28V1.02.05
```

- other board:

```
root@freescale ~$ cd /tmproot@freescale /tmp$ mknod /dev/ptp c 232 0
root@freescale /tmp$ ifconfig eth0 10.193.20.240 up
eth0: Freescale FEC PHY driver [Generic PHY] (mii_bus:phy_addr=0:00, irq=-1)
PHY: 0:00 - Link is Up - 100/Full
root@freescale /tmp$ ./ptp_main -d -o -m -l -w –z
IXXAT Automation Gmbh & FREESCALE=====================PTP IEEE1588-2008 stack for
IMX28V1.02.05
ofm (msrd/filt); -18,679589120;  -18,679589120;mtsd (msrd/filt); -12,453058890;  -12,453058890;stmd
(msrd/filt);  12,453060460; 12 ,453060460;owd (msrd/filt);  6,226530230;   6,226530230
```


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