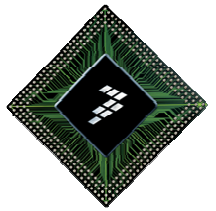
September, 2010

i.MX23, i.MX25, and i.MX28 Architecture Differences



Freescale / MX28 DFAE Training

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- 4. Audio Features
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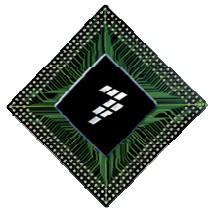
1. System Core



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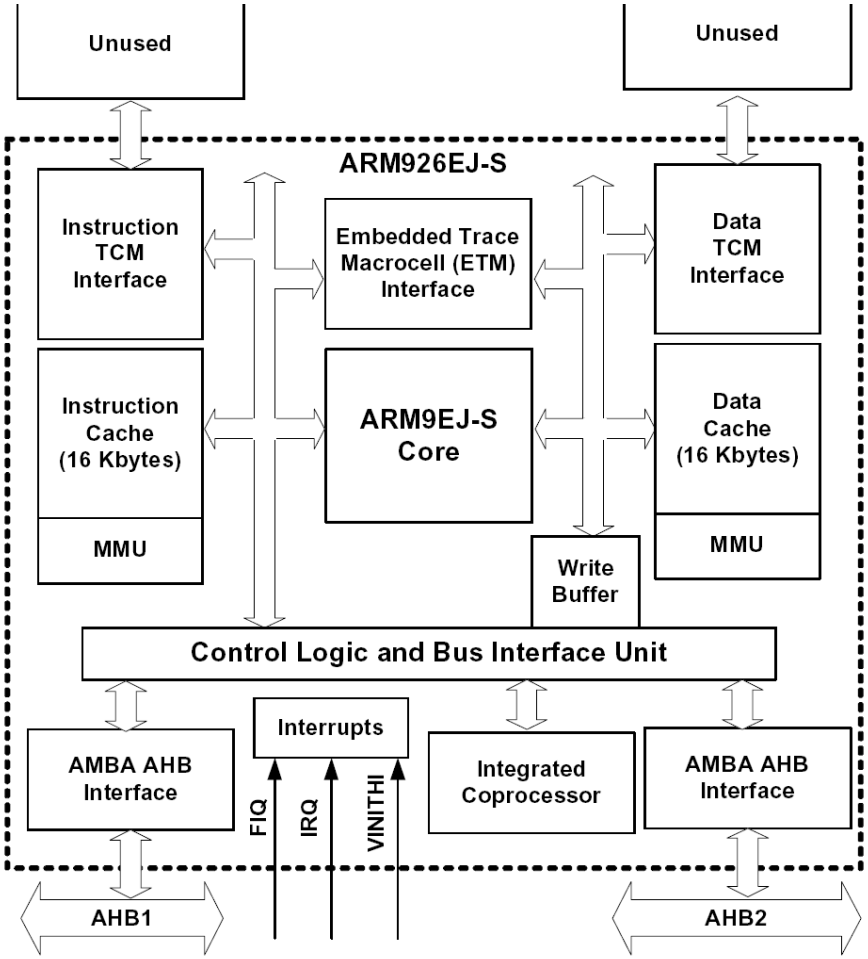
1. System Core

	i.MX23	i.MX25	i.MX28
MCU Core	ARM926EJ-S, 400+ MHz (Consumer – 454 MHz, Industrial - 400 MHz)	ARM926EJ-S, 400 MHz	ARM926EJ-S, 450+ MHz
Caches	16 KB data + 16 KB instruction	16 KB data + 16 KB instruction	32 KB data + 16 KB instruction
On-Chip RAM	32 KB	128 KB	128 KB
On-Chip ROM	64 KB	32 KB	128 KB
On-Chip Secure RAM	N/A	2 KB	N/A
OC One-Time-Programmable	1 Kbit OCOTP ROM	IC Identification Module (IIM)	1.25 Kbits OCOTP ROM
Embedded Trace Macrocell (ETM)	Yes	Yes	Yes
JTAG Interface	one-wire serial / six-wire parallel	Secure JTAG (parallel only)	Six wire parallel JTAG

ARM926 Processor Core



ARM926 RISC Processor Core

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OCOTP, IIM

i.MX23 / i.MX28 On-Chip One-Time-Programmable (OCOTP) ROM

- Housing of hardware and software capability bits.
- Housing of Freescale operations and unique-ID fields.
- Housing the customer-programmable cryptography key.
- Four words for customer general use.
- A 32-bit word is dedicated to controller read and write locking of the various OTP regions (copied into a shadow register).
- Storage of various ROM configuration bits.

i.MX25 IC Identification Module (IIM)

- Provides unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring permanent non-volatility.
- Provides up to 28 volatile control signals.
- Provides the means to generate a second 168-bit SCC key.
- Provides a set of volatile software-accessible signals which can be used for software control of hardware elements, not requiring non-volatility.

ETM, JTAG, Secure RAM

The ARM9 platform includes an ARM9 **Embedded Trace Macrocell (ETM9)** and Embedded Trace Buffer (ETB) supporting real-time instruction and data tracing.

i.MX23

- Serial JTAG module maps one-wire protocol to six-wire JTAG interface on the ARM926 core.
- The HW_DIGCTL_CTRL_USE_SERIAL_JTAG bit in the digital control block selects whether the serial JTAG interface or the alternative six-wire parallel JTAG interface is used.

i.MX25

- Secure JTAG protects JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- The Secure RAM provides secure storage of sensitive information

i.MX28

- Supports standard 6 wire parallel JTAG interface.

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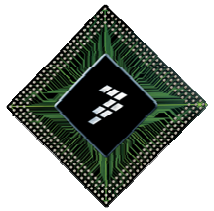
2. Security Features



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2. Security Features

	i.MX23	i.MX25	i.MX28
Security Hardware	Data Co-Processor: AES-128 encryption and SHA-1 hashing hardware	RTICv3: HASH Accelerator and Real-Time Integrity Checker SCCv3: Secure RAM and Security Monitor DRYICE	Data Co-Processor: AES-128 encryption, SHA-1, and SHA-256 hashing hardware.
Secure ROM	OCOTP ROM	IC Identification Module (IIM)	OCOTP ROM
Secure RAM	N/A	2KB	N/A
Secure JTAG	N/A	Yes	N/A
Secure Boot	128-bit AES hardware decryption	HAB - High Assurance Boot with SHA-256	128-bit AES hardware decryption, HAB - High Assurance Boot with SHA-256

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i.MX23 / i.MX28 Secure Boot

- ARM core jumps to on-chip ROM at reset. It cannot jump directly to user code.
- ROM code contains a secure boot loader (non-secure booting have to be enabled through OTP bits).
- The boot loader can boot from USB, NAND, SD/MMC, I2C or SPI.
- The boot loader authenticates and decrypts boot images.
- Proprietary authentication scheme (not HAB)
  - Based on CDC-MAC signature calculated using DCP and OTP key.
  - Only authenticated images are booted.
- Secure boot image are encrypted
  - Image data is encrypted using a randomly selected session key.
  - Session key is encrypted by the OTP key and is discovered by the ROM during the authentication process.
  - Boot images can be created by Freescale-supplied *elftosb* application.
- In addition to secure boot above, HAB is available on the MX28 and is enabled by default. HAB can be disabled by setting the OTP fuse bit.

i.MX25 Security Hardware

RTICv3 - HASH Accelerator and Real-Time Integrity Checker

- Ensure the integrity of the peripheral memory contents
- Assist with boot authentication.
- Verify the memory contents during system boot and during run-time execution.
- Include SHA-1 and SHA-256 message authentication.

SCCv3 - Secure RAM module and the Security Monitor

- The Secure RAM provides secure storage of sensitive information both in on-chip RAM and in off-chip, non-volatile memory.
- When used with on-chip memory, the data is stored in RAM that can be cleared, if necessary, to prevent unauthorized access.
- When used with off-chip memory, the data is stored in encrypted form, using an encryption key that is unique to each device and accessible only to the Secure RAM module.

DRYICE

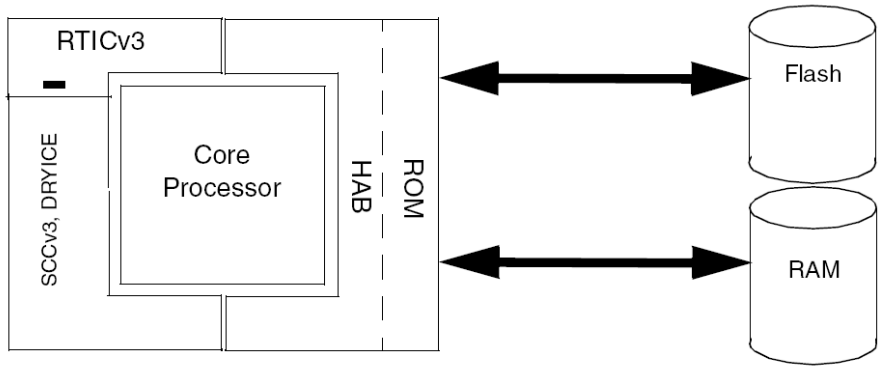
- Volatile key storage for Point Of Sale (POS) terminals
- Trusted time source for Digital Rights Management (DRM) schemes.

Secure JTAG

- Regulating or blocking the access to the system debug features

High Assurance Boot with SHA-256

- HAB component of the ROM protects against the potential threat of attackers modifying areas of code or data in programmable memory to make it behave in an incorrect manner.
- The HAB also prevents attempts to gain access to features which should not be available.



Secure Boot Components

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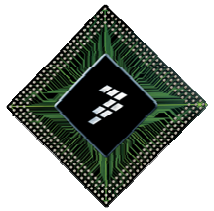
3. External Memory and Storage



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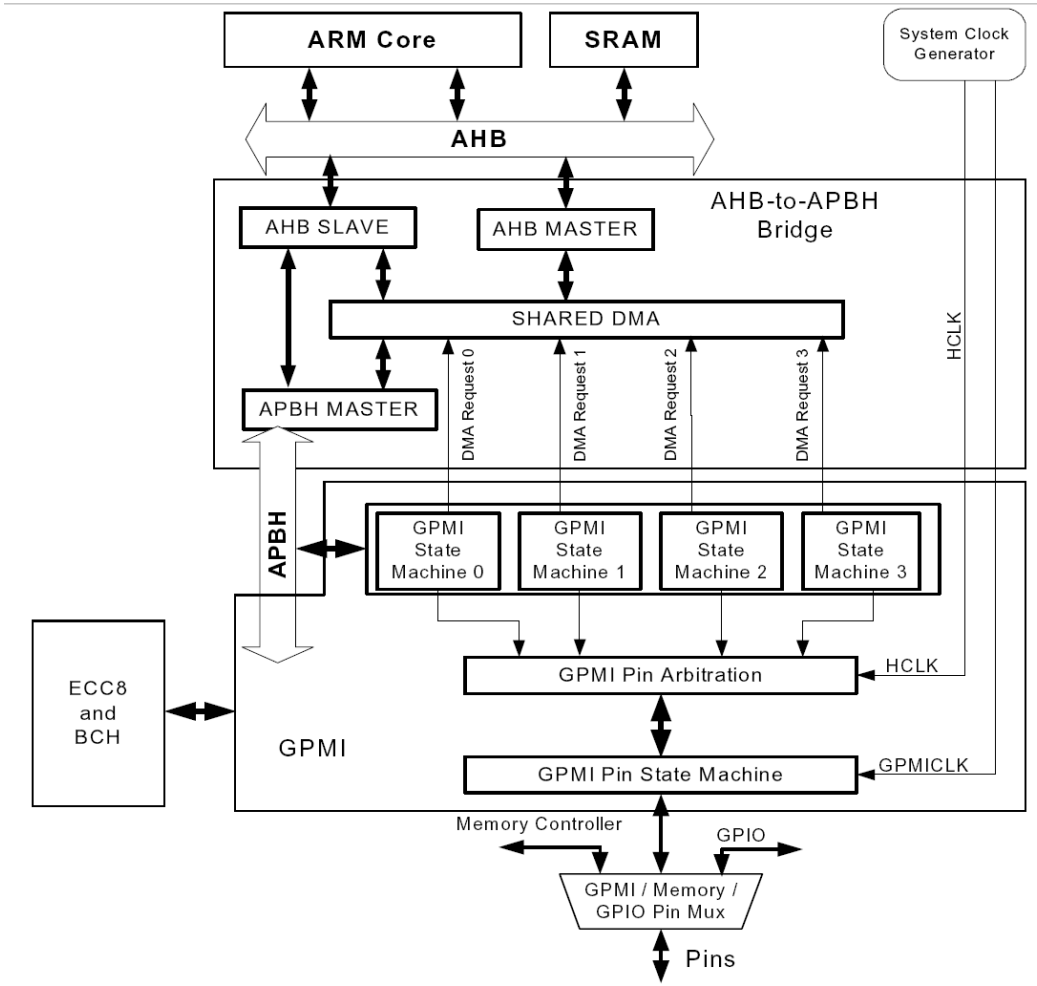
3. External Memory and Storage

	i.MX23	i.MX25	i.MX28
Memory and Storage Hardware Interface	External Memory Interface (EMI) General Purpose Media Interface (GPMI) - NAND Synchronous Serial Port (SSP) supporting MMC/SD/SDIO 1-bit, 4-bit, and 8-bit modes	External Memory Interface (EMI) - Multi-Master Memory Interface (M3IF) - Enhanced SD RAM Ctrl (ESDRAMC) - NAND Flash Controller - Wireless Ext. Interface module (WEIM), ATA, Enhanced SD Host Interface (eSDHC)	External Memory Interface (EMI) General Purpose Media Interface (GPMI) for NAND flash Synchronous Serial Port (SSP) supporting MMC/SD/SDIO 1-bit, 4-bit, and 8-bit modes, and eMMC4.4.
SDRAM	3.3V SDRAM 2.5V DDR1 1.8V Mobile SDRAM 1.8V Mobile DDR	3.3V SDRAM 1.8V DDR2 1.8V Mobile DDR	DDR2-400 (1.8V) LP-DDR1-400 (1.8V) (mDDR) LV-DDR2-400 (1.5V)
NAND Flash	Up to four 8-bit / 16-bit NAND SLC / MLC NAND 8-bit Reed-Solomon ECC 20-bit BCH ECC	Up to four 8-bit / 16-bit NAND SLC / MLC NAND 8-bit Reed Solomon ECC codes Internal RAM Buffer	Up to eight, 8-bit NAND SLC / MLC NAND 20-bit BCH ECC
Parallel NOR Flash	N/A	Yes	N/A
ATA	N/A	UDMA-5	N/A
SD / MMC	Yes	Yes	Yes

i.MX23 / i.MX28 GPMI



General-Purpose Media Interface Controller Block Diagram

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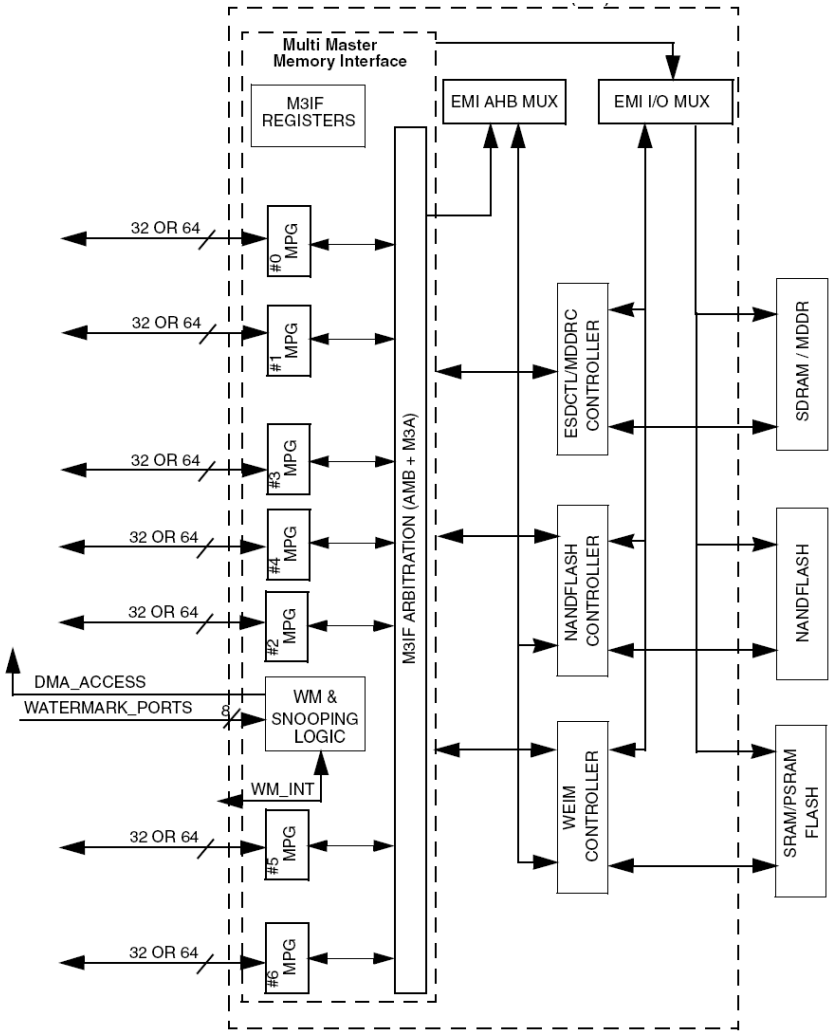
i.MX25 EMI



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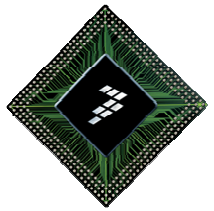
4. Audio Features



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4. Audio Features

	i.MX23	i.MX25	i.MX28
Serial Audio Interface	Dual Serial Audio Interface (SAIF)	Enhanced Serial Audio Interface (ESAI)	Dual Serial Audio Interface (SAIF)
SPDIF digital audio out	Yes	N/A	Yes
Digital Audio Mux	N/A	Yes	No
Analog Audio Outputs	Stereo Headphone Amplifier Mono Speaker Amplifier	N/A	N/A
Analog Audio Inputs	Mono microphone input Two stereo line inputs	N/A	N/A

i.MX23 / i.MX28 SAIF Similarities

- Two SAIF blocks, each with three stereo pairs, for interfacing external D/A and A/D converters or host processors.
  - 3-, 4-, or 5-wire serial interface to industry's most common analog codecs
  - Half-duplex operation
  - 16- to 24-bit serial stereo digital audio PCM play/record
  - Two, four or six channels supported
  - Generic frame control supports I2S, left- and right-justified frame formats
  - Master and slave BITCLK and LRCLK modes, and optional master MCLK mode
  - Supports sample rates from 8kHz to 192kHz with a high-resolution fractional divider driven by PLL
  - Programmable over-sample rate for MCLK output
  - Four-entry FIFOs (per sample pair) buffer either two-channel sample pairs (17-bit through 24-bit PCM) or four-packed-channel sample pairs (16-bit PCM)
- Sony-Philips Digital Interface Format (SPDIF) transmitter module transmits data according to the SPDIF digital audio interface standard (IEC-60958).

i.MX23 / i.MX28 SAIF Differences

- MX23:
  - Only one set of clock pins is provided for both ports.
  - Only one of the two SAIFs can be the master or drive the clock pins at a time. The other SAIF becomes a slave to the master.
  - Both SAIFs must operate at the same sample rate.
- MX28:
  - Each SAIF port has a set of clock pins and can operate in master mode simultaneously (if connected to different off-chip codecs, for example).

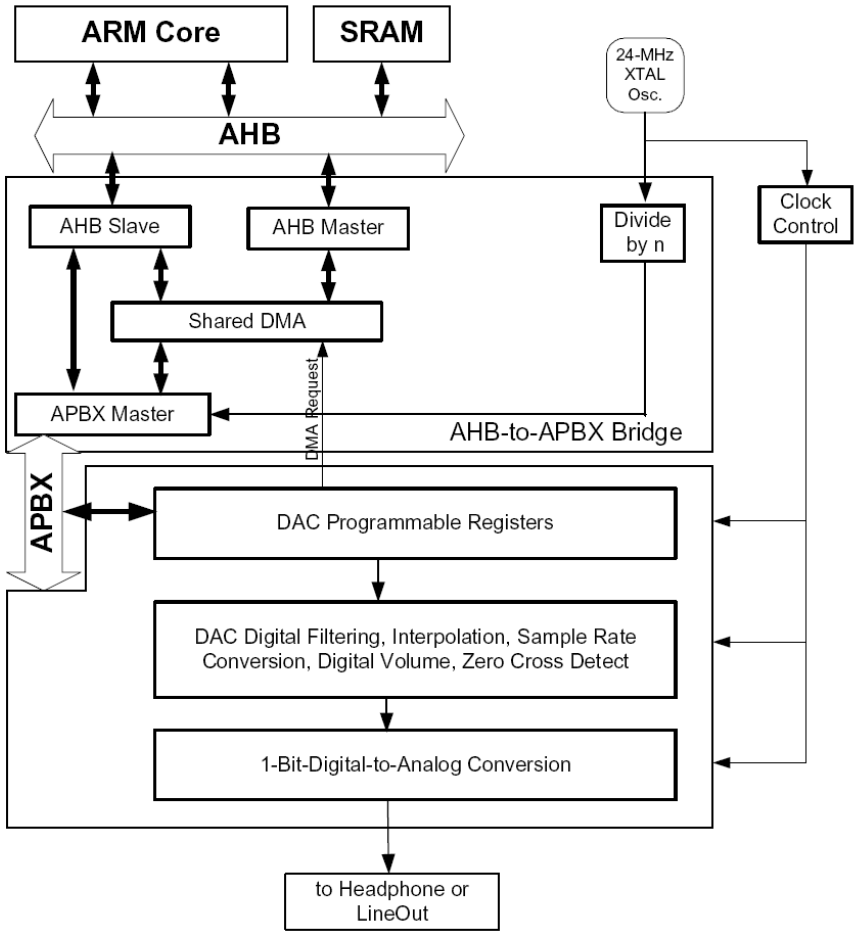
Possible Configurations	
MX23 & MX28	One SAIF in TX mode (the default clock master) while the other SAIF is in RX slave mode and is internally controlled by the TX SAIF's BITCLK and LRCLK.
MX23 & MX28	One SAIF in RX master mode while the other SAIF is in RX slave mode and again is internally controlled by the RX master SAIF's BITCLK and LRCLK.
MX23 & MX28	Both SAIFs in RX slave mode, with BITCLK and LRCLK controlled by the off-chip codec.
MX28 Only	Both SAIFs in master mode, driving their BITCLK and LRCLK.

i.MX25 ESAI

- The ESAI provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs.
  - Independent (asynchronous) or shared (synchronous) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in master or slave mode
  - Up to 6 transmitters and 4 receivers
  - Programmable data interface modes supported are I2S, LSB aligned and MSB aligned
  - Programmable word length (8, 12, 16, 20 or 24 bits)
  - Flexible selection between system clock and external oscillator as input clock sources, programmable clock divider and frame sync generation
  - AC97 support
  - Time Slot Mask Register for reduced GPU overhead (for both Tx and Rx)
  - 128-word transmit FIFO and receive FIFO.
- Digital Audio Mux (AUDMUX) provides a programmable interconnect device for voice, audio, and synchronous data routing between host serial interfaces (that is, SSI, SAP) and peripheral serial interfaces (that is, audio and voice codecs).

i.MX23 Analog Audio Output

- Stereo Headphone Amplifier Output
  - DAC with 99 dB SNR
  - Direct drive without bulky and expensive capacitors
  - Click/pop free operation
  - Short-circuit protection
- Speaker Amplifier Output
  - Up to 1.6W_{rms} output at 4.2V supply with 4 Ω loading.
  - Click/pop free operation



AUDIOOUT/DAC Block Diagram

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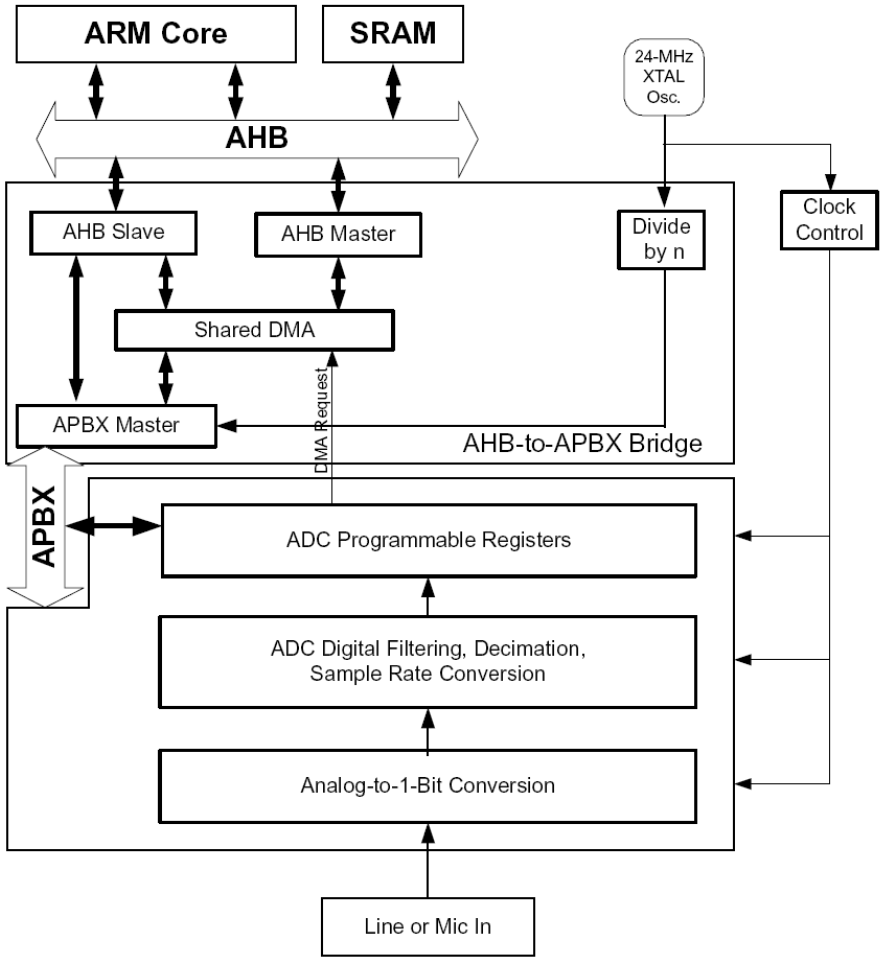
i.MX23 Analog Audio Input

- Mono microphone input
  - Built-in microphone bias generator
- Two stereo line inputs
  - ADC with 85 dB SNR
  - Looped back from the stereo headphone amplifier (for debug and development)



AUDIOIN/ADC Block Diagram

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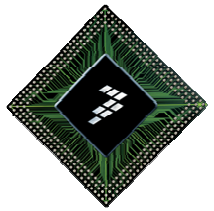
5. Display and Video Features



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5. Display and Video Features

	i.MX23	i.MX25	i.MX28
LCD Interface	Yes	Yes	Yes
Resolution	Up to 640 x 480	Up to 800 x 600	Up to 800 x 480
Bit/Pixel	8, 16, 18, 24 (color)	1, 2, 4 (mono) 4, 8, 12, 16, 18, 24 (color)	8, 16, 18, 24 (color)
TV-Out	Yes	N/A	N/A
Display Processing	Pixel Processing Pipeline (PXP) 8 Overlays Color Key / Alpha Blend Color Space Conversion and Scaling Rotation	1 Overlay (Graphic Window) Color key / Alpha Blend Panning	Pixel Processing Pipeline (PXP) 8 Overlays Color Key / Alpha Blend Color Space Conversion and Scaling Rotation

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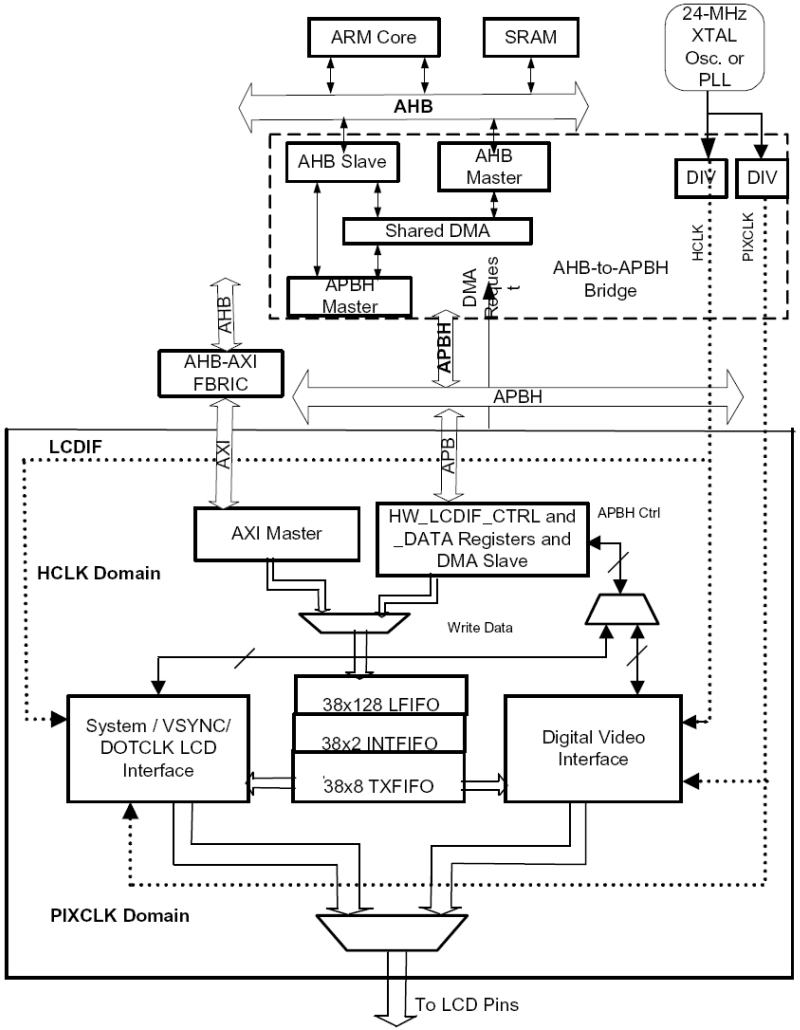
i.MX23 LCD Interface & TV-OUT

LCD Interface (LCDIF)

- Up to 24-bit RGB (DOTCK) modes
- Up to 18-bit system-mode including VSYNC and WSYNC modes.
- Up to VGA (640x480) resolution at 60Hz LCD panel support
- 8-bit data ITU-R/BT.656 D1 digital video stream output mode (PAL/NTSC), with on-the-fly RGB to YCbCr color-space-conversion.
- Flexible input formats

Integrated TV-Out Support

- Integrated PAL/NTSC TV-encoder fully pipelined to display controller D1 output stream
- Integrated low-power 10-bit Video DAC (VDAC) for composite analog video output.



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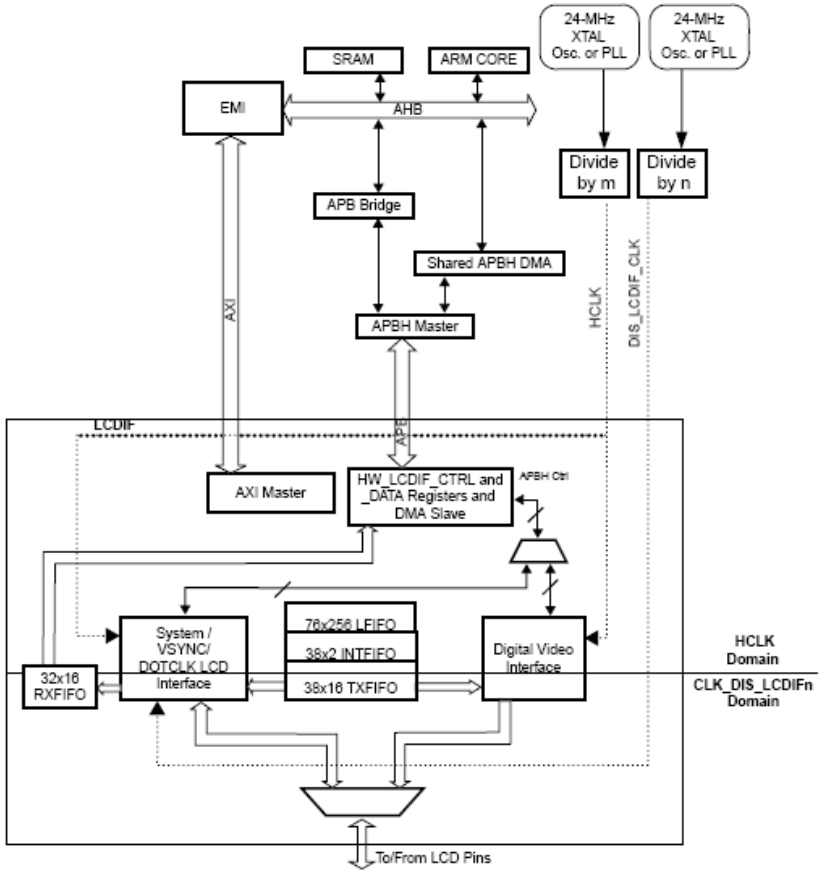
i.MX28 LCD Interface

LCD Interface (LCDIF)

- Up to 24-bit RGB (DOTCK) modes
- Up to 18-bit system-mode including VSYNC and WSYNC modes.
- ITU-R BT.656 mode (called Digital Video Interface or DVI mode) including progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation.
- Up to WVGA (800x480) resolution at 60Hz LCD panel support
- 8/16/18/24 bit LCD data bus support available depending on the package size.



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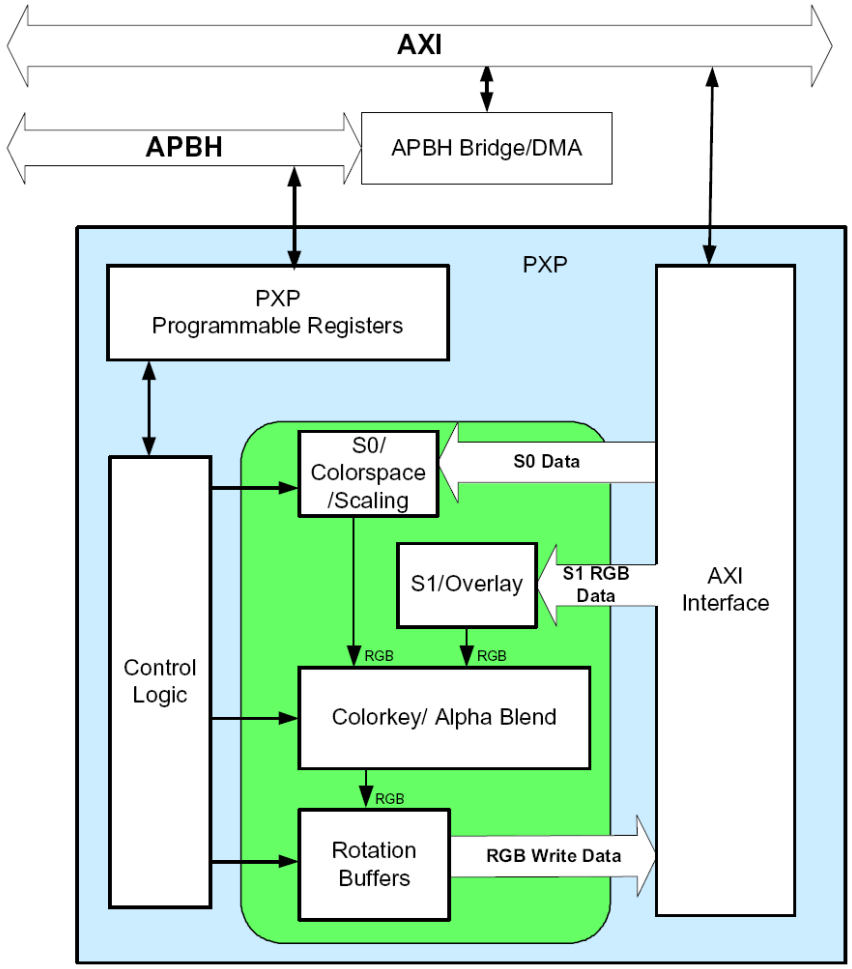
i.MX23 / i.MX28 Pixel Processing Pipeline

Pixel Processing Pipeline (PXP)

- Supports up to eight overlays
- Provides full path from color-space conversion, scaling, alpha-blending to rotation without intermediate memory access
- Bi-linear scaling algorithm with cropping and letterboxing
- Alpha-blend, BITBLT, color-keying
- Memory efficient block-based rotation engine



Pixel Pipeline (PXP) Block Diagram

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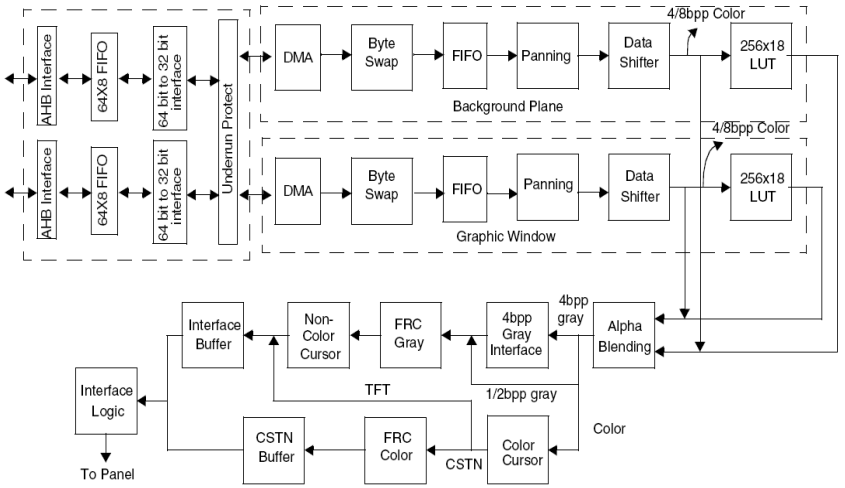
i.MX25 LCD Controller

i.MX25 Liquid Crystal Display Controller (LCDC)

- Standard panel interface for common LCD drivers, monochrome, passive and active color panels
- Hardware-generated cursor with blink, color, and size programmability
- Logical operation between color hardware cursor and background
- Hardware panning (soft horizontal scrolling)
- 8-bit pulse-width modulator for software contrast control
- Graphic window support for viewfinder function in color display
- Graphic window color keying for graphical hardware cursor
- 256 transparency levels for alpha blending between graphic window and background plane



LCDC Block Diagram

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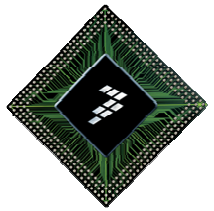
6. Power Management



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6. Power Management

	i.MX23 / i.MX28	i.MX25
Internal Power Supply	DC-DC switched converter 4 linear regulators • 3.3V • 1.8V • 1.2V • 2.5V (MX23 only) • 1.5V (MX28 only)	N/A
Power Management	Adaptive Voltage Control (AVC) Silicon speed and temperature sensors Multiple peripheral clock domains	DVFS – Dynamic Voltage and Frequency Scaling Clock gating Active well bias (AWB)
Low-power Mode	Standby Deep Sleep	Wait Doze Stop Sleep

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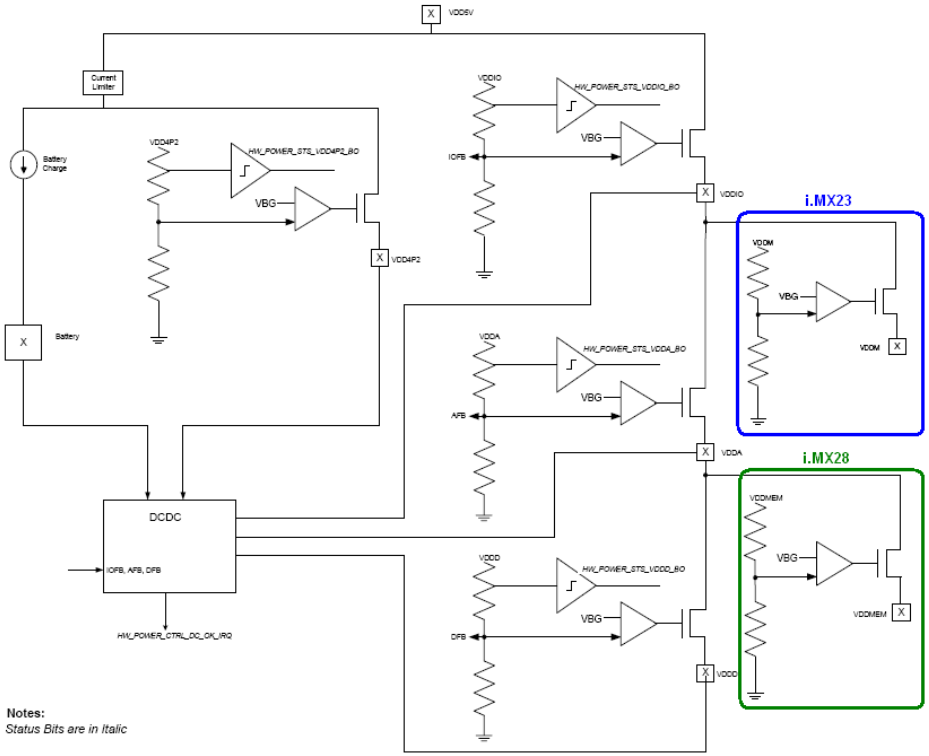
i.MX23 / i.MX28 Power Management

- Built-in DC-DC switched converter supporting Li-Ion batteries.
- Features multi-channel outputs for VDDIO (3.3 V), VDDD (1.2 V), VDDA (1.8 V), and regulated 4.2V source.
- i.MX23 has a 2.5V VDDM output regulator for supporting DDR1 memories.
- i.MX28 has a 1.5V VDDMEM output regulator for supporting LV-DDR2 memories.
- Direct power from 5-V source (USB, wall power, or other source), with programmable current limits for load and battery charge circuits.
- Silicon speed and temperature sensors enable adaptive power management over temperature and silicon process.
- Multiple peripheral clock domains save power while optimizing performance.
- Deep Suspend Mode – CPU reduced to minimum speed, with the peripherals shut down.



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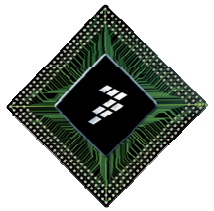
i.MX25 Power Management

- **Dynamic voltage frequency scaling (DVFS)** reduces active power consumption by scaling voltage and frequency according to required MIPs.
- **Clock gating** reduces active power consumption by gating the clock to each module while the module is in idle state.
- **Active well bias (AWB)** reduces static power consumption by applying back bias on transistors. AWB can be applied on ARM11P and EMI while they are not functioning (in low-power modes).
- **Low-power mode** can reduce the system power to several levels. ARM can be put into standby mode, clocks can be gated, in some cases PLLs can be stopped, and the oscillator can be powered off. Furthermore, the core logic voltage can be reduced to state-retention level when the device is idle.

i.MX25 Power Management

Power mode	Conditions
RUN	• ARM are active • Well bias is off • clocks are on • modules are active
Wait	• ARM is in wait for interrupt mode • Well bias is off • MCUPLL is on, • USBPLL is off • OSC24M is on • OSC32K is on • All other modules are off
Doze	• ARM platform clock is off • Well bias is on • MCUPLL is on, • USBPLL is off • OSC24M is on • OSC32K is on • All other modules are off
Stop	• All PLLs are off • Well bias is on • OSC24M is off • OSC32K is on • All the other modules are off.
Sleep	• All PLLs are off • Well bias is on • OSC24M is off • OSC32K is on • All the other modules are off. • Core voltage is dropped to 1V

7. Networking



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7. Networking

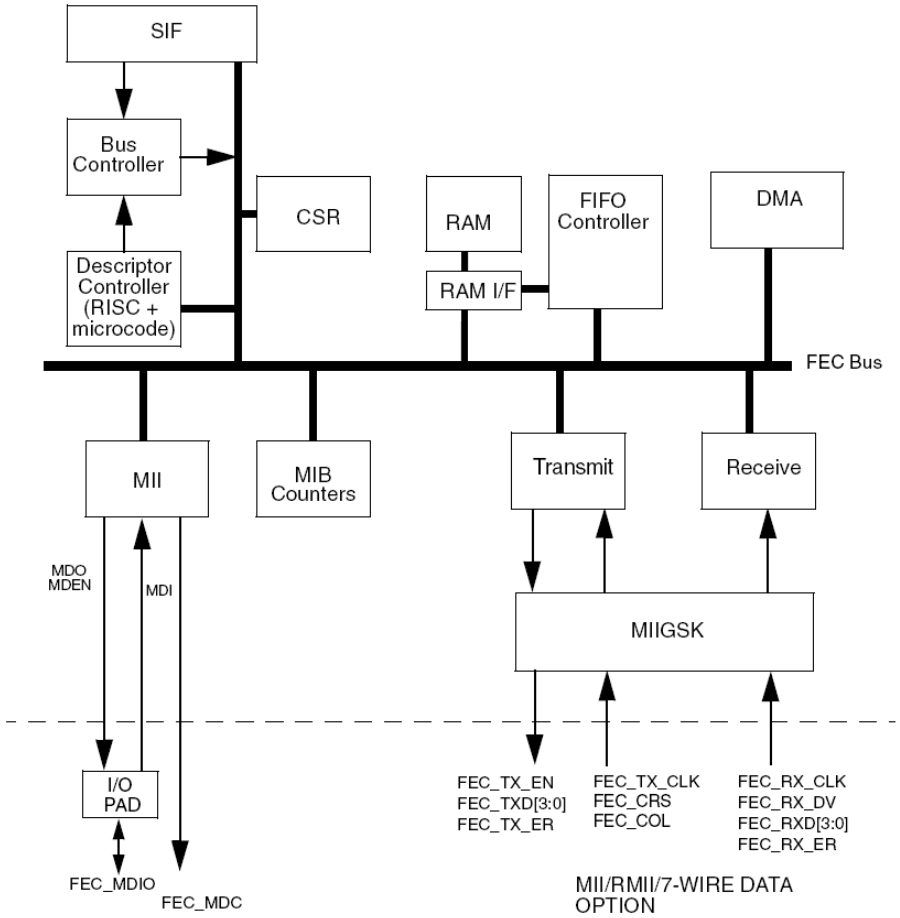
	i.MX23	i.MX25	i.MX28
Ethernet	N/A	1 Fast Ethernet Controller (FEC) 10/100 (RMII or MII)	2 RMII Fast Ethernet Controllers (FEC) 10/100 or 1 MII Fast Ethernet Controller
CAN	N/A	Controller Area Network (CAN) (2)	Controller Area Network (CAN) (2)

i.MX25 Networking - FEC

i.MX25

Fast Ethernet Controller (FEC)

- 100/10 Mbps
- IEEE 802.3



FEC Block Diagram

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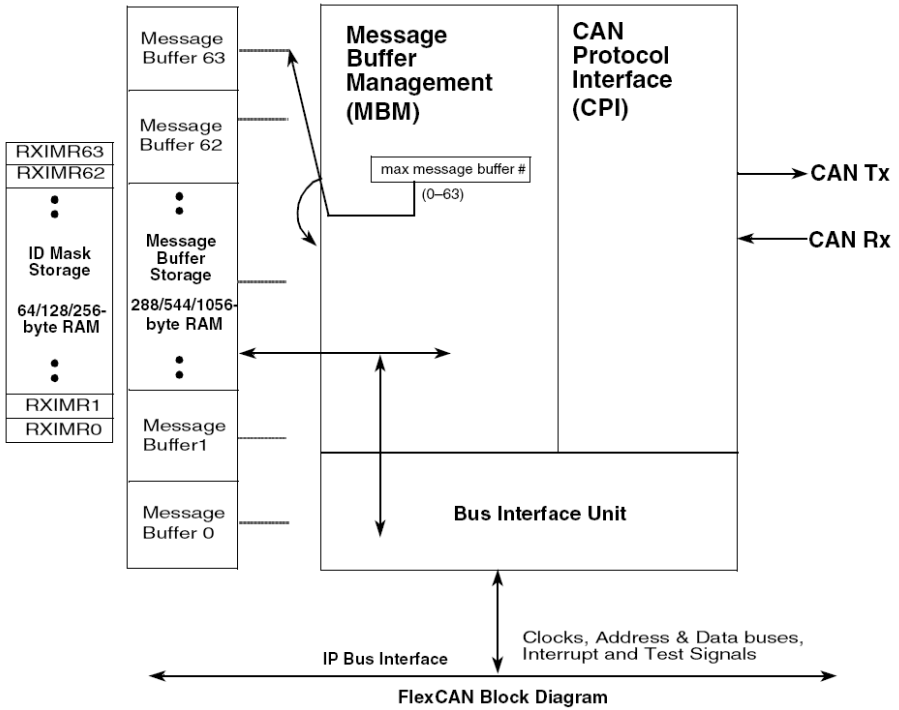
Controller Area Network (CAN) (2)

- Primarily, but not solely, designed as a vehicle serial data bus
- Real-time processing
- EMI environment



FlexCAN Block Diagram

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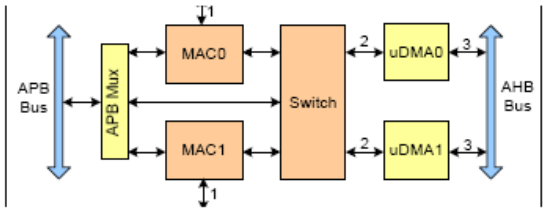
Ethernet Controller (ENET)

- 100/10 Mbps
- IEEE 802.3
- Different controller than the MX25.
- The ethernet controller (ENET) consists of two MACs (media access controllers), each with it's own dedicated uDMA (unified DMA) module.
- Supports either a single Medium Independent Interface (MII) working at 25 MHz or two Reduced Medium Independent interfaces (RMII) working at 50 MHz.
- The ENET MAC is backward compatible with the Freescale FEC controller (Such as the FEC used in i.MX25).
- Supports full duplex and configurable half duplex operations.
- Support for all IEEE 1588 frames.
- uDMA (unified DMA) is connected to the ENET MAC. Not general purpose and is highly specific to support ENET traffic.
  - Legacy mode – supports the legacy programming module used with the FEC – this is the default mode.
  - Enchanced mode – based on legacy mode, but allows for the support of additional features such as IEEE-1588 support, additional interrupts, error checking, etc.



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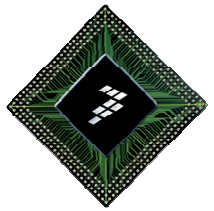
8. Communications



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8. Communications

	i.MX23	i.MX25	i.MX28
UART	2 UART + 1 Debug	5 UART	5 UARTs + 1 Debug
UART Speed	Up to 3.25 Mbps	Up to 4 Mbps	Up to 3.25 Mbps
IrDA	N/A	UART IrDA compatible	N/A
I2C Interface	One	Three	Two
Digital Radio Interface (DRI)	Yes	N/A	N/A
Serial Peripheral Interface	Synchronous Serial Port (SSP)	Configurable Serial Peripheral Interface (CSPI)	Synchronous Serial Port (SSP)
Synchronous Serial Interface (SSI)	N/A	Yes	N/A
Subscriber Identification Module (SIM)	N/A	Yes	N/A
1-Wire module	N/A	Yes	N/A

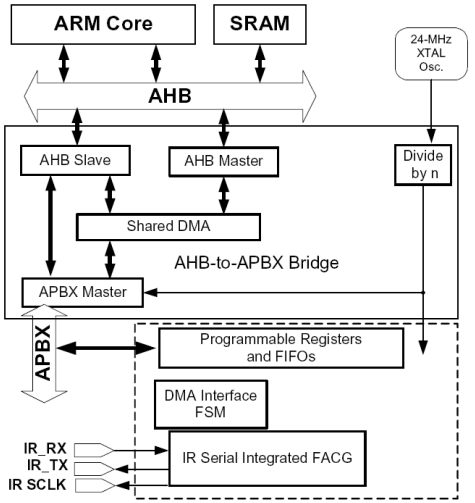
UART, IrDA, I2C

UART

- i.MX23/28: The application UARTs have speed up to 3.25 Mbps and the debug UART can run up to 115.2kbps.
- i.MX23: 3 EIA/TIA compatible UARTs. 2 for application use and 1 for debug use.
- i.MX28: 6 EIA/TIA compatible UARTs. 5 for application use and 1 for debug use.
- i.MX25: Five high-speed EIA/TIA compatible UARTs with speed up to 4 Mbps.

IrDA Controller

- i.MX23: Not supported.
- i.MX25: The functionality can be provided by UART with the use of external circuitry (low-speed, up to 115.2 kbps).
- i.MX28: Not supported



IrDA Controller Block Diagram

Inter IC (I2C)

- i.MX23/25/28: The I2C interface operates up in both standard speed (up to 100 kbps) and fast speed (up to 400 kbps).
- i.MX23: Single I2C module
- i.MX25: Three I2C modules
- i.MX28: Two I2C modules

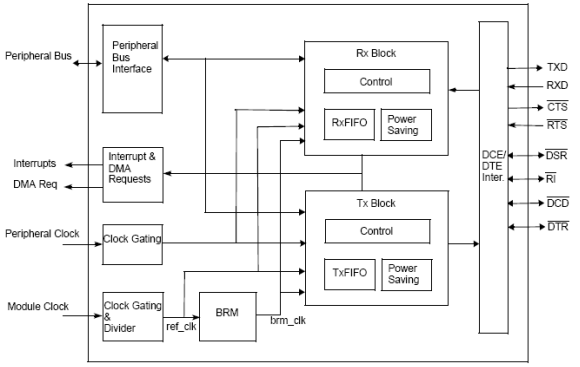


Figure 46-1. UART Block Diagram

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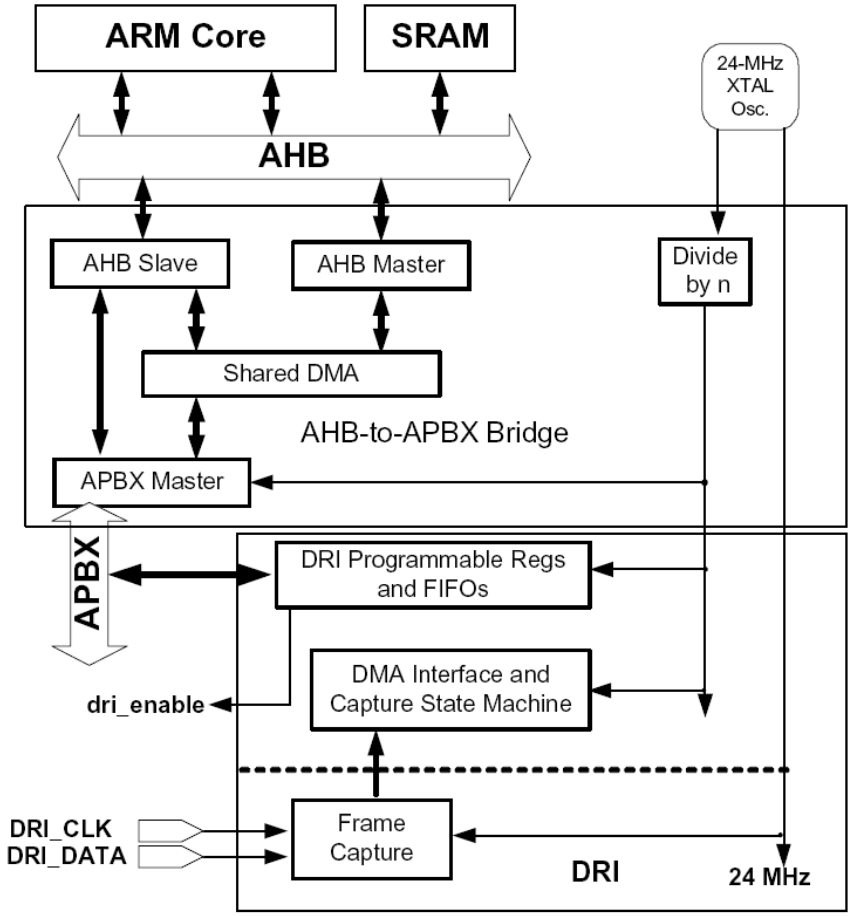
i.MX23 Digital radio interface (DRI)

- A digital interface to Freescale's digital radio receiver product, the STFM1000.
- Consists of two digital input signals (DRI_CLK and DRI_DATA) that share pins with analog line inputs.



Digital Radio Interface (DRI) Block Diagram

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i.MX25 CSPI, SSI, SIM, 1-Wire

Configurable Serial Peripheral Interface (CSPI)

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Max operation frequency up to the reference clock frequency

Synchronous Serial Interface (SSI)

- Full-duplex, serial communicate with a variety of serial devices, such as standard codecs, DSPs, microprocessors, peripherals, and codecs that implement the inter-IC sound bus standard (I2S) and Intel AC97 standard.

Subscriber Identification Module (SIM)

- Designed to facilitate communication to SIM cards or Eurochip pre-paid phone cards.

1-Wire module

- Provides battery characteristics information.

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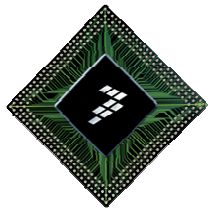
9. I/O Modules



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9. I/O Modules

	i.MX23	i.MX25	i.MX28
USB 2.0 High Speed	1 HS port (OTG) (does not support LS)	1 HS port (OTG) + 1 HS port (Host)	1 HS port (OTG) + 1 HS port (Host)
Pulse Width Modulator (PWM)	5 channels	4 channels	5 channels
General Purpose I/O (GPIO)	Yes	Yes	Yes
I/O Multiplexer	Pin Multiplexing Scheme	Yes	Pin Multiplexing Scheme
Low Resolution ADC	Yes (12-bit resolution)	Yes (12-bit resolution)	Yes (12-bit resolution)
Touch Screen Controller	Yes (4-wire resistive)	Yes (4/5-wire resistive)	Yes (4/5-wire resistive)
Keypad Port (KPP)	LRADC channel for button support	Yes	LRADC channel for button support
CMOS Sensor Interface (CSI)	N/A	Yes	N/A

USB, PWM, GPIO

USB

- Universal Serial Bus (USB) version 2.0 Standard.
- Capable of operating as either a USB device or a USB host
- i.MX23/28
  - High Speed operation (480 Mbps) and/or Full speed operation (12 Mbps).
- i.MX25
  - High Speed operation (480 Mbps) and/or Full/Low speed operation (12/1.5 Mbps).

Pulse-width modulator (PWM)

- Applications include LED brightness control and high voltage generators for electroluminescent lamp (E.L.) display backlights.
- i.MX25 PWM is optimized to generate sound from stored sample audio images; it can also generate tones.

GPIO

- GPIO operation may be dynamically programmed to be input or output.
- GPIO pin may also be used as an interrupt input, and the interrupt trigger type may be configured.

i.MX23 / i.MX28 IOMUX, LRADC, TSC

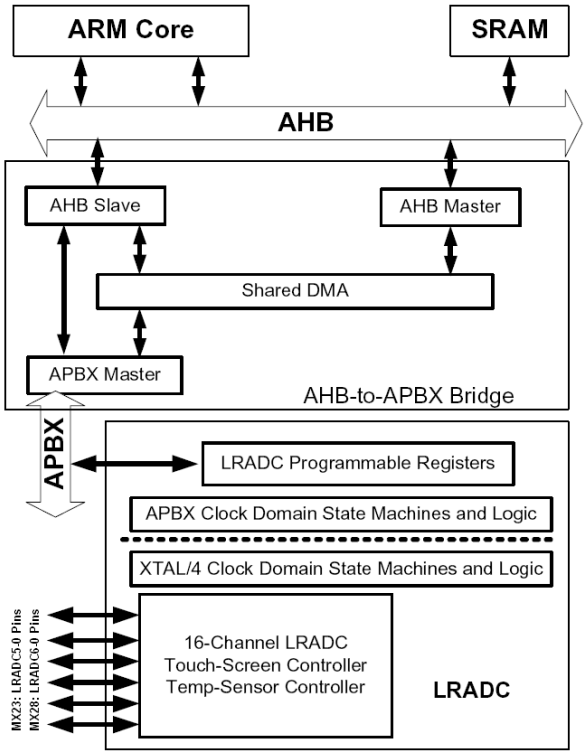
I/O Mux

- Designed for cost sensitive applications. It uses a pin multiplexing scheme to allow customers to choose which specialized interfaces to enable for their applications. Four deep multiplexing.
- Allows many digital pins to be used as GPIOs.

Low-Resolution ADC

- 16-Channel Low-Resolution ADC
- 12-bit resolution
- MX23: 6 independent channels for general use
  - ✓ 4 can be used for 4 wire touch screen
- MX28: 7 independent channels for general use
  - ✓ 5 can be used for 5 wire touch screen
- 9-10 dedicated channels, for internal voltage measurement.

The LRADC controller includes an integrated **touch-screen controller** with drive voltage generation for touch-screen coordinate measurement, as well as a touch-detection interrupt circuit.



Low-Resolution ADC and Touch-Screen Interface Block Diagram

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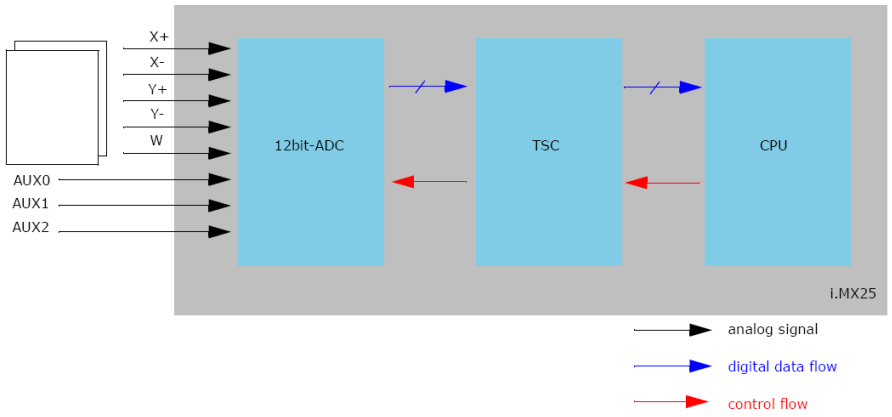
i.MX25

- **I/O Multiplexer (IOMUX):** Up to eight output sources multiplexed per pin. Up to four destinations for each input pin. Unselected input paths are held at constant level for reduced power consumption.

- **Touch screen controller (TSC)** and associated **analog-to-digital converter (ADC)** together provide a resistive touch screen solution for low cost PDAs, Cell Phones, ePOS devices, and multi-media players.



TSC in System

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i.MX25 KPP and CSI

Keypad Port (KPP)

- Interface with 2- or 3-point contact keypad
- Simplify software task of scanning a keypad matrix
- Capable of detecting, debouncing, and decoding one or multiple keys pressed simultaneously

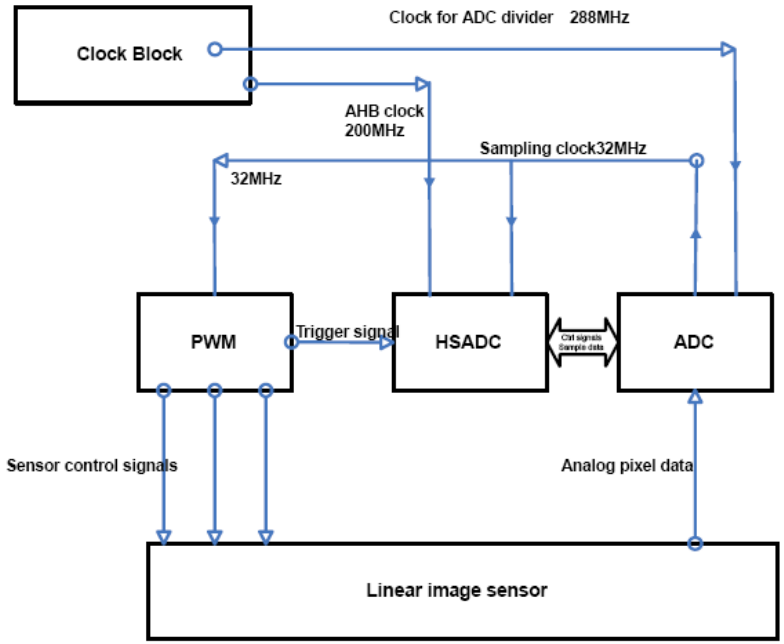
CMOS Sensor Interface (CSI)

- Configurable interface logic to support most CMOS sensors.
- Support for CCIR656 video interface and traditional sensor interface.
- Configurable master clock frequency output to sensor.
- Statistic data generation for Auto Exposure (AE) and Auto White Balance (AWB) control of the camera.

i.MX28 High Speed ADC

Features

- Specific to the i.MX28
- The high-speed ADC block is designed for driving a linear image scanner sensor (for example, TOSHIBA TCD1304DG linear image scanner sensor).
- Also supports some other general user cases which need to sample an analog source and then move the sample data to internal/external memory.
- 12 bit analog ADC.
- Up to 2 Msps data/sample rate.
- Can work in cooperation with the PWM block to generate driving signals of an external device such as a linear image scanner sensor.
- The PWM can also generate a trigger signal which is synchronous with high-speed ADC block to start the conversion of ADC.
- An APBH-DMA channel is connected to the high-speed ADC block to move the sample data from the asynchronous FIFO inside the high-speed ADC block to the internal/external memory.
- Can also be configured for 10-bit or 8-bit sample precision.



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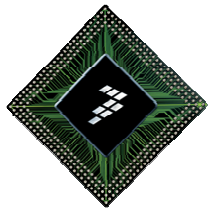
10. Boot Modes



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10. Boot Modes

	i.MX23 / i.MX28	i.MX25
I2C	Yes	Yes
SPI	Yes	Yes
SD/MMC	Yes	Yes
NAND	Yes	Yes
JTAG	Yes	Yes
NOR Flash	N/A	Yes
USB	Yes	N/A
UART	N/A	Yes
WEIM	N/A	Yes

i.MX23 / i.MX28 Boot Modes

- The boot mode can be selected to use either external resistors or the OTP eFuse bit settings.
- The boot mode pins are located on LCD_RS, LCD_DATA[5] and LCD_DATA[3:0] for i.MX23.
- The boot mode pins are located on LCD_RS and LCD_DATA[5:0] for i.MX28.
- For the i.MX28, LCD_DATA[4] is used to select the voltage of the boot interface:
  - 0 = 3.3V
  - 1 = 1.8V
- The Boot ROM probes LCD_RS pin on startup:
  - If LCD_RS is high, it will decode the boot mode vector from the boot mode pins.
  - If LCD_RS is low, it will be determined by OTP eFuse bits.

i.MX23 Boot Mode Selection Table

Table 39-3. Boot Mode Selection Map

ETM Enable/ LCD_ DATA[5]	BM3/ LCD_ DATA[3]	BM2/ LCD_ DATA[2]	BM1/ LCD_ DATA[1]	BM0/ LCD_ DATA[0]	PORT	BOOT MODE
0/1	0	0	0	0	USB	USB (unencrypted vs. encrypted is under OTP control)
0/1	0	0	0	1	I^2C	I^2C master
0/1	0	0	1	0	SPI	SPI master SSP1 boot from flash
0/1	0	0	1	1	SPI	SPI master SSP2 boot from flash
0/1	0	1	0	0	GPMI	NAND
0/1	0	1	0	1	–	Reserved
0/1	0	1	1	0	JTAG_WAIT	Startup waits for JTAG debugger connection
X	0	1	1	1	–	Reserved
0/1	1	0	0	0	SPI	SPI master SSP2 boot from EEPROM
0/1	1	0	0	1	SSP1	SD/MMC master on SSP1
0/1	1	0	1	0	SSP2	SD/MMC master on SSP2
X	1	0	1	1	–	Reserved
0/1	1	1	0	0	–	Reserved
0/1	1	1	0	1	–	Reserved
X	1	1	1	0	–	Reserved
X	1	1	1	1	–	Reserved

i.MX28 Boot Modes

i.MX28 Boot Mode Selection Table

LCD_ DATA[5]	VOLTAGE SELECT-OR/ LCD_ DATA[4]	BM3/ LCD_ DATA[3]	BM2/ LCD_ DATA[2]	BM1/ LCD_ DATA[1]	BM0/ LCD_ DATA[0]	PORT	BOOT MODE
x	x	0	0	0	0	USB0	USB (unencrypted vs. encrypted is under OTP control)
x	0	0	0	0	1	I2C0	I2C0 master, 3.3 V
x	1	0	0	0	1	I2C0	I2C0 master, 1.8 V
x	0	0	0	1	0	SPI2	SPI master SSP2 boot from flash, 3.3 V
x	1	0	0	1	0	SPI2	SPI master SSP2 boot from flash, 1.8 V
x	0	0	0	1	1	SPI3	SPI master SSP3 boot from flash, 3.3 V
x	1	0	0	1	1	SPI3	SPI master SSP3 boot from flash, 1.8 V
x	0	0	1	0	0	GPMI	NAND, 3.3 V
x	1	0	1	0	0	GPMI	NAND, 1.8 V
x	0	0	1	0	1		Reserved
x	0	0	1	1	0	JTAG	Wait JTAG connection mode
x	0	0	1	1	1		Reserved
x	0	1	0	0	0	SPI3	SPI master SSP3 boot from EEP-ROM, 3.3 V
x	1	1	0	0	0	SPI3	SPI master SSP3 boot from EEP-ROM, 1.8 V
x	0	1	0	0	1	SSP0	SD/MMC master on SSP0, 3.3 V
x	1	1	0	0	1	SSP0	SD/MMC master on SSP0 1.8 V
x	0	1	0	1	0	SSP1	SD/MMC master on SSP1, 3.3 V
x	1	1	0	1	0	SSP1	SD/MMC master on SSP1, 1.8 V
x	0	1	0	1	1		Reserved
x	0	1	1	0	0		Reserved
x	0	1	1	0	1		Reserved
x	0	1	1	1	0		Reserved
x	0	1	1	1	1		Manufacturing Test Mode

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i.MX25 Boot Modes

- Type of boot is controlled by the boot mode pins (BMOD[1:0]) value, sampled at exit of reset.
- There are four options:

BMOD[1:0]	Boot Type	Boot Details
0 0	Internal Boot	Executing ROM code, which handles booting from following sources. Refer to Section 7.3.3 for more details. • NOR Flash (via WEIM, 16-bit, slow asynchronous mode for debugging purpose only) • OneNAND • SPI (serial flash, Chip Select #1) / I^2C • NAND Flash, MLC NAND 0.5K/512 B, 2KB/4KB page / (e-fuse selectable). 4/8-bit ECC (e-fuse selectable) • SD/MMC (support high capacity)/MoviNAND boot (through MMC interface) A fallback to ALL above modes, on error exception: USB, UART boot.
0 1	FSL Test Mode	Freescale Test Mode, special mode reserved for device testing. Used for testing the device, by either executing pre-defined routines, or by allow download execute and log read out. Supported tests are: Security HW Tests (SCC Key validation) Put device in low power mode (DSM) Run of loaded tests using Test Executive method. Refer to Section 7.3.4 for more details.
1 0	External (Direct) Boot	• HW only (Direct boot via the interface, independent of boot ROM code) boot from WEIM interface Refer to Section 7.3.5 for more details.
1 1	UART Boot Loader	Load and execute code, via serial devices: • UART Refer to Section 7.3.6 for more details.

[1] For typical application board usage, the internal PHY options is recommended. The use of external Transceiver is not recommended, and would come at the expense of availability of pins.

i.MX25 Internal Boot

- Internal boot mode is the only mode, in which a secure boot is possible.
- It will support the following boot devices:
  - NOR flash with WEIM interface, located on CS0, bus with of 16 bits
  - OneNAND
  - SLC and MLC NAND with NFC interface
  - SD/MMC via eSDHC interface
  - EEPROM boot via SPI and I2C.
- The boot ROM determines the boot device by reading BT_MEM_CTL[1:0] bits on the eFuse.

BT_MEM_CTL[1:0]	Boot Memory Control Type (memory device)	00 = WEIM 01 = NAND Flash 10 = Reserved 11 = Expansion Device(SD/MMC/MoviNAND, support high storage, EEPROMs. See BT_MEM_TYPE[1:0] settings for details).

i.MX25 FSL Test Mode

- The test boot mode is reserved for Freescale use during validation and diagnostics.
- It is disabled on secure production devices.

i.MX25 External Boot from WEIM interface

- It is selected by driving value of “10” on BMOD[1:0] pins and fuse DIR_BT_DIS is not burned.
- The core boots directly from external memory, and is non-secure.
- It supports either muxed or non-muxed address data boot from WEIM interface.

i.MX25 UART Boot Loader

- For the UART, activity is detected via the Receive Data Ready (RDR) flag showing at least one character has been read into FIFO.
  - Bootable UART (UART1 to 5) is selected by BT_UART_SRC[2:0] fuses.


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