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Chip Errata for the i.MX28

This document details all known silicon errata for the i.MX28. Table 1 provides a revision history for this document.

Table 1. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	03/2010	Initial release
1.0	09/2010	• Updated Table 2 • Deleted ENGR119940

Table 2 provides a cross-reference to match the revision code to the revision level marked on the device.

Table 2. Revision Level to Part Marking Cross-Reference

MCIMX28 Revision	Package	Device Marking	Mask Revision
1.2	14 × 14	MCIMX283DVM4B	M06Z
1.2	14 × 14	MCIMX283CVM4B	M06Z
1.2	14 × 14	MCIMX286DVM4B	M06Z
1.2	14 × 14	MCIMX286CVM4B	M06Z
1.2	14 × 14	MCIMX287CVM4B	M06Z
1.2	14 × 14	MCIMX281AVM4B	M06Z
1.2	14 × 14	MCIMX285AVM4B	M06Z

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Table 3 summarizes all known errata.

Table 3. Summary of Silicon Errata and Applicable Revision

Errata	Name	Projected Solution
ENGR116296	HSADC: Soft reset causes unexpected request to DMA	No fix scheduled
ENGR116904	PXP: The HW_PXP_CSCCOEFF2_C3 register can not be reset correctly under some PVT corner	No fix scheduled
ENGR119650	USB: USB core INCR8 and INCR16 modes are inoperable	No fix scheduled
ENGR119653	USB: ARM to USB register error issue	No fix scheduled
ENGR119657	PWM: Register write sync issue when HSADC clock frequency is lower than APBX clock frequency	No fix scheduled
ENGR119956	CLKCTRL: ENET 1588 clock (CLK_ENET_TIME) is not under control of ENET disable control bit	No fix scheduled
ENGR121613	ENET: ENET big endian mode not compatible with ARM little endian	No fix scheduled
ENGR121616	DMA: APBH/APBX DMA channel can stall while waiting to access a APBH/APBX bus peripheral when the channel freeze bit is set	No fix scheduled

ENGR116296 HSADC: Soft reset causes unexpected request to DMA

Description:

When HSADC is initially powered on and performs a soft reset, the APBH-DMA may receive an unexpected request from the HSADC and enter into an unknown state.

Projected Impact:

HSADC operates incorrectly.

Workaround:

Software workaround 1:

Before completing a normal soft reset, make a timing sequence of CLKGATE and SFTRST by register programming to reset FIFO read and write pointer, and make RD_EMPTY to the known state of 1 before normal operation.

The register programming below can be used to generate the timing sequence of CLKGATE and SFTRST before a normal soft reset.

— HW_HSADC_CTRL0_CLR(BM_HSADC_CTRL0_SFTRST);

— HW_HSADC_CTRL0_WR((HW_HSADC_CTRL0_RD() | BM_HSADC_CTRL0_SFTRST) & (~BM_HSADC_CTRL0_CLKGATE));

— HW_HSADC_CTRL0_SET(BM_HSADC_CTRL0_CLKGATE);

— HW_HSADC_CTRL0_CLR(BM_HSADC_CTRL0_CLKGATE);

— HW_HSADC_CTRL0_SET(BM_HSADC_CTRL0_CLKGATE);

NOTE

This sequence is only required for the first reset after power up.

Software workaround 2:

Complete a HSADC DMA channel reset after the HSADC module soft reset and before configuring/enabling the HSADC DMA channel as shown below:

— HW_APBH_CHANNEL_CTRL.B.RESET_CHANNEL = 0x1000;

— HSADC_CTRL0_CLKGATE and HSADC_CTRL0_SFTRST address is 0x80002000.

Projected Solution:

No fix scheduled.

ENGR116904 PXP: The HW_PXP_CSCCOEFF2_C3 register can not be reset correctly under some PVT corner

Description:

The HW_PXP_CSCCOEFF2_C3 register does not receive the correct reset value after using the PXP software reset function or after power up.

Projected Impact:

The PXP operates incorrectly with wrong coefficient setting.

Workaround:

Always write the HW_PXP_CSCCOEFF2_C3 register with the expected value before using it. The PXP_CSCCOEFF2 register address is 0x8002A0F0.

Projected Solution:

No fix scheduled.

ENGR119650 USB: USB core INCR8 and INCR16 modes are inoperable

Description:

The USB controller may not operate properly when receiving a packet in INCR8 and INCR16 modes. The packet is completed correctly (ACK is sent) on the USB bus, but cannot be seen by software.

This issue exists when all of following conditions are met:

1. Controller is receiving data (Host Bulk IN or Device Bulk OUT)
2. Primary INCR8/INCR16 mode is selected (SBUSCFG. AHBBRST of the USB register is set to 0b010 or 0b011)
3. Length of data received is less than the total_byte field in TD
4. Data length is not a multiple of the burst size and the remainder is a sub-burst. For example, if the data length is 32n + 16 bytes in INCR8 mode, or 64n + 16/32/48 in INCR16 mode, this errata is triggered.

Projected Impact:

This is a low severity bug because INCR8 and INCR16 are not mandatory modes. Other modes should be used.

Workaround:

Set SBUSCFG.AHBBRST of the USB register to a modes other than 0b010 or 0b011.

Projected Solution:

No fix scheduled.

ENGR119653 USB: ARM to USB register error issue

Description:

The ARM writes a data error to the USB core register unless SRM SWP instruction is used.

The issue occurs when all of the following conditions are met:

1. Last AHB access is to the non-USB AHB slave
2. Current AHB access is to the USB
3. These two accesses are back-to-back
4. The last data phase of the last AHB access has a wait state
5. Only happens when D-cache is enabled

Projected Impact:

The USB register does not get correct data when writing to the USB slave through the AHB bus when D-cache is enabled.

Workaround:

All USB register write operations must use the ARM SWP instruction.

Projected Solution:

No fix scheduled.

ENGR119657 PWM: Register write sync issue when HSADC clock frequency is lower than APBX clock frequency

Description:

The PWM channel might not generate the required output signal when in HSADC driving mode. When in HSADC mode, if the HSADC input clock is much lower than the APBX bus clock (for example APBX Bus clock is 24 MHz and HSADC input clock is 4 MHz) the write signal to the PWM registers is missed. Write access to the following registers has no effect after HSADC mode is enabled:

- PWM Control and Status Register
- PWM Channel Active Register
- PWM Channel Period Register

As a result, dedicated PWM channel is not triggered.

Projected Impact:

HSADC or off chip linear sensor does not receive the required control signals.

Workaround:

If the HSADC input clock is lower than the 24 MHz APBX bus clock the APBX bus clock should be set to a lower frequency before every write to the PWM register. When the write access finishes, the APBX clock can be set back to normal.

Projected Solution:

No fix scheduled.

ENGR119956 CLKCTRL: ENET 1588 clock (CLK_ENET_TIME) is not under control of ENET disable control bit

Description:

The Ethernet 1588 clock (CLK_ENET_TIME) continues to toggle when the Ethernet module is disabled by setting ENET disable control bit in the HW_CLKCTRL_ENET register. The ethernet controller consumes 30 µA on the 4.2 V power supply.

Projected Impact:

The Ethernet 1588 clock consumes 30 µA on the 4.2 V power supply when the Ethernet module is disabled.

Workaround:

The Ethernet 1588 clock can be gated off by clearing the HW_CLKCTRL_ENET_DIV_TIME register. The HW_CLKCTRL_ENET_DIV_TIME register address is 0x80040140.

Projected Solution:

No fix scheduled.

ENGR121613 ENET: ENET big endian mode not compatible with ARM little endian

Description:

The endian mode of the Ethernet controller is designed to be big-endian mode which is not compatible with the ARM core and reset sections of the device.

Projected Impact:

The ARM core cannot establish data communication correctly to/from the Ethernet controller without software endian conversion.

Workaround:

When communicating with the Ethernet controller, an additional byte-swap routine has to be called by the ARM core.

Projected Solution:

No fix scheduled.

ENGR121616 DMA: APBH/APBX DMA channel can stall while waiting to access a APBH/APBX bus peripheral when the channel freeze bit is set

Description:

When the channel freeze bit is set, the APBH/APBX DMA channel can stall while waiting to access a peripheral on the APBH/APBX bus. This occurs if the channel freeze bit is set exactly at the same time as when the channel internal state machine changes from the PIO_REQ state to the REQ_WAIT state.

Projected Impact:

The data communication with the APBH/APBX DMA channel associated peripheral is stalled.

Workaround:

Do not use DMA PIO operation to configure the associated peripheral when using channel freeze function. Use ARM PIO operation instead.

Projected Solution:

No fix scheduled.

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