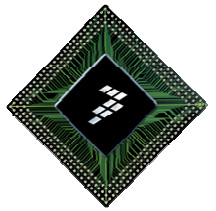
September, 2010

MX28 Overview of Device Architecture



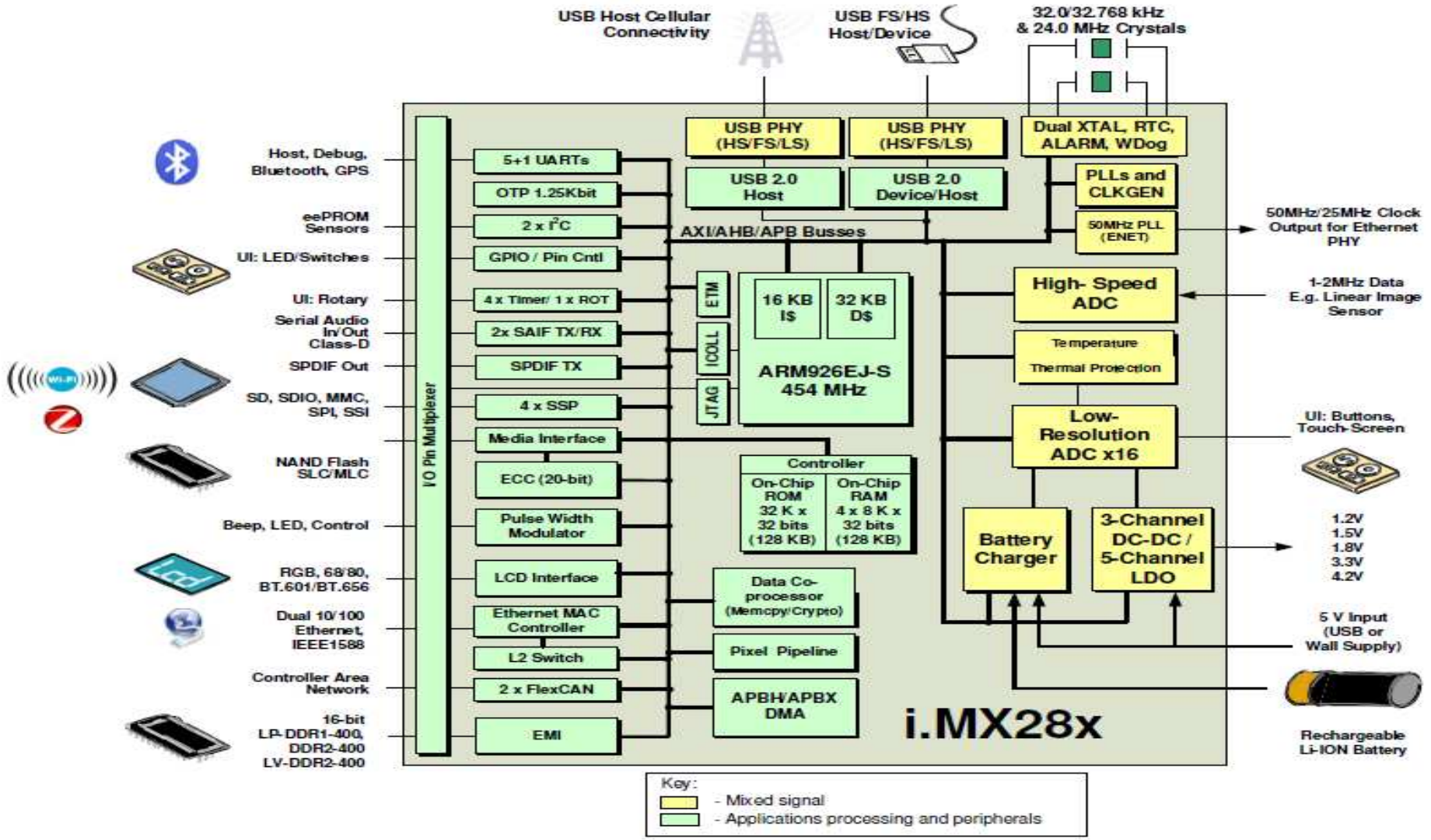
Freescale / MX28 DFAE Training

freescale™ semiconductor

i.MX28 Overview

- i.MX28 is a low-power high performance application processor aimed at the higher end 32-bit embedded general market and industrial/medical markets.

i.MX28x SoC Diagram



freescale semiconductor

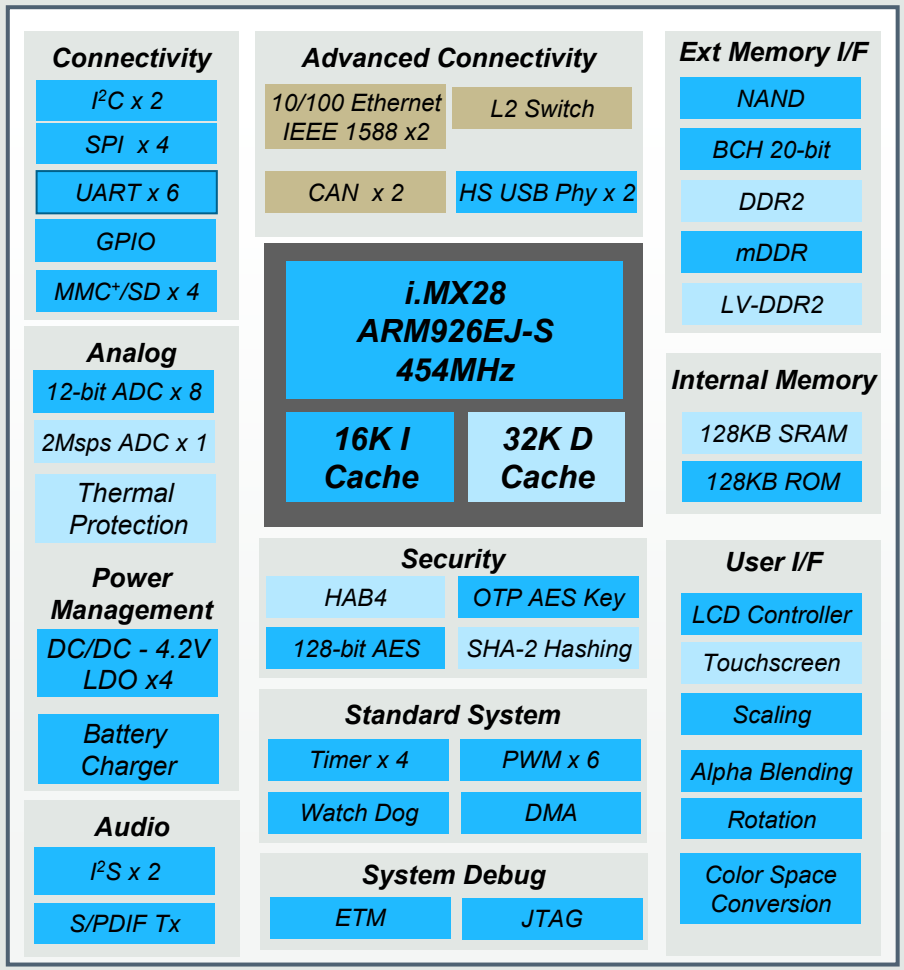
i.MX28x functionality

Key Features and Advantages

- 454MHz ARM926EJ-S core w/16KB I +32KB D Cache
- PMU with high efficiency on-chip DC/DC, supports Li-Ion batteries
- Dual Ethernet with RMII support and L2 Switch
- Dual CAN interfaces
- LCD Controller with Touchscreen
- NAND support – SLC/MLC and eMMC 4.4 managed
- Hardware BCH (up to 20-bit correction)
- 200 MHz 16-bit DDR2, LV-DDR2, mDDR external memory support
- Dual High speed USB with embedded PHY
- Up to 8 General purpose 12-bit ADC channels and single 2 Msps ADC channel
- LCD Controller with Touchscreen
- Temperature sensor for thermal protection
- Multiple connectivity ports (UARTs, SSP, SDIO, SPI, I2C, I2S)
- Family of products supporting various feature sets

Package and Temperature

- 289 BGA 14x14mm .8mm
- -40C to +85C (Industrial, Automotive)
- -20C to +70C (Consumer)



Shares common IP with i.MX233.

New or significantly changed functionality compared to i.MX233

New for i.MX28x but not available on all variants

freescale™ semiconductor

i.MX28 Family Product Comparison

Feature	i.MX283	i.MX286	i.MX287
On-chip RAM	128KB	128KB	128KB
Memory Interface	NAND Flash, DDR2, mDDR, LV-DDR2	NAND Flash, DDR2, mDDR, LV-DDR2	NAND Flash, DDR2, mDDR, LV-DDR2
LCD Interface	16-bit DDR2, mDDR, SDRAM	16-bit 150MHz DDR1, mDDR	16-bit 200MHz DDR2, mDDR
Touchscreen	Yes	Yes	Yes
Ethernet	X1	X1	x2
L2 Switch	-	-	Yes
CAN	-	x2	x2
12-bit ADC	x3	x5	x8
High Speed ADC	X1	X1	x1
USB2.0	OTG HS with HS PHY x1 HS Host with FS PHY x1	OTG HS with HS PHY x1 HS Host with FS PHY x1	OTG HS with HS PHY x1 HS Host with FS PHY x1
SDIO	x3	x3	x4
SPI	x3	X3	x4
UART	x3	x3	x6
PWM	x3	x3	x6
S/PDIF Tx	-	Y	Y
Package	14x14 0.8mm 289 BGA	14x14 0.8mm 289 BGA	14x14 0.8mm 289 BGA

Preliminary: Subject to Change

freescale™ semiconductor

i.MX28 – CPU Subsystem

- ARM926EJ-S Processor with up to 454MHz performance
- Custom Caches for maximum performance and low power (16K + 32K)
  - Improves video decode modeling results
- Low-power 90LP implementation
- 128KB of On-Chip SRAM
- Vectored interrupt controller with 128 fully programmable sources and up to 4 levels of IRQ nesting
- Coresight ETM9 for higher-speed trace (DDR data, better compression) debug
- Standard 6-wire JTAG for debug
- Support wait-for-interrupt low-power mode

i.MX28 – Low Power Features/Characteristics

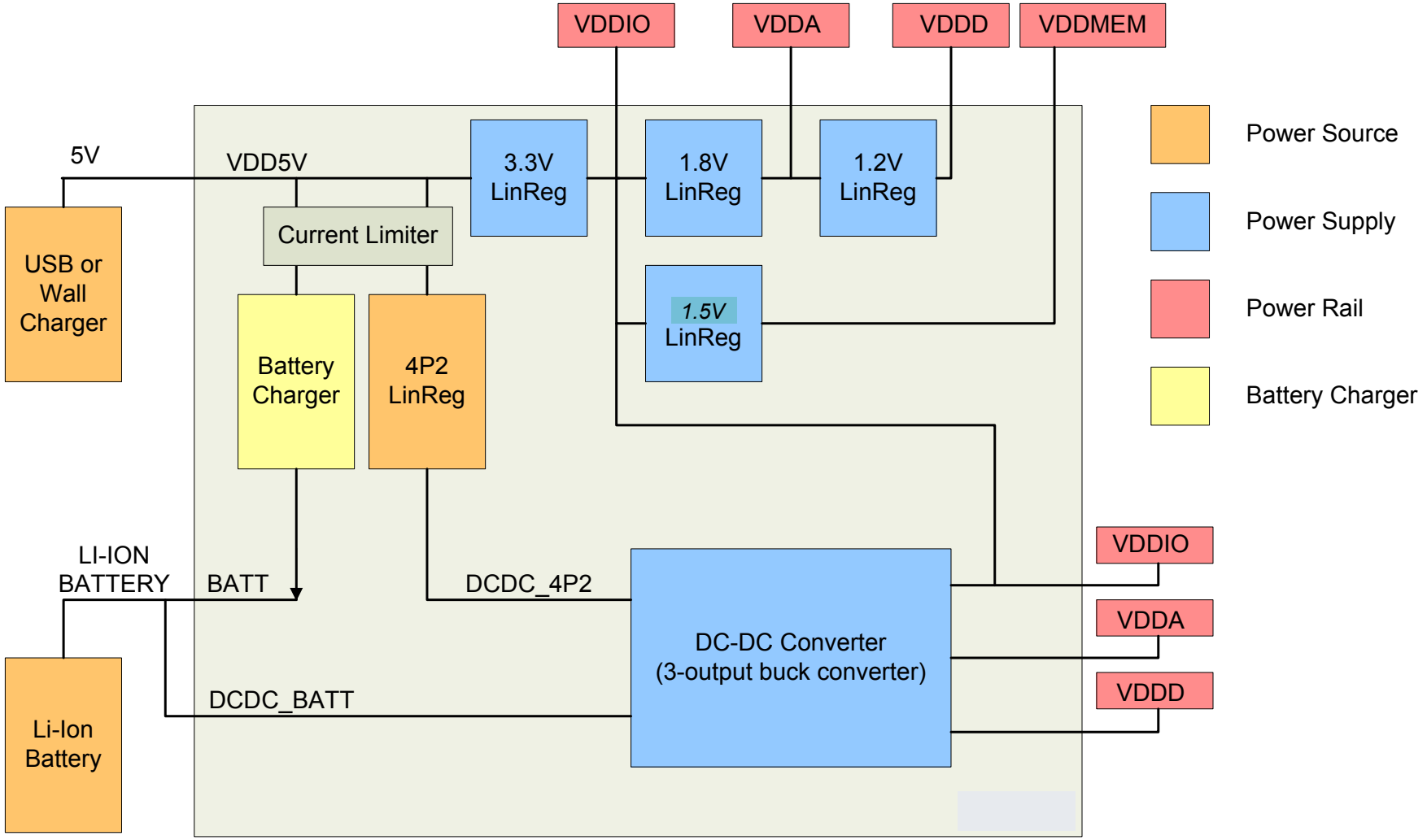
- Supports dynamic voltage frequency scaling (DVFS) which provides the most efficient power per MIPS for the application
- Architectural and automated clock gating
- External memory controller implement five levels of low-power modes
- Synchronous clocking mode from CPU, bus to memory controller, reduces latency and thus MHz/MIPS requirements
- Auto-slow on bus-clock (HCLK) with HW controlled slow-down/speed-up based on bus activity
- Wait-for-Interrupt standby mode system power < 2mA (~7.5mW)
  - CPU clock stopped, wakes up from interrupt
  - SRAM/DRAM retained
  - Supports Interrupt from press
  - Supports wake-up from touchscreen
  - Quick power up
- Power-down (RTC-only) power = 12uA
  - Only RTC active
  - Power up longer

i.MX28 - Power Management Unit

- Integration of a DC-DC switching converter and linear regulators that provide four output rails
  - Powers digital blocks and components such as system clocks
  - Powers I/O peripherals like NAND flash and SD/MMC cards
  - Powers 1.5V DDR2
- Power sources
  - Li-Ion batteries
  - Direct power from 5V source (USB, wall power or other source)
  - Internal 4.2V power source generated from 5V source
- Battery charging capability
  - Allows battery to be fully charged while device is in use
  - Current and voltage sensors allows firmware to monitor the voltage and current into the battery to determine “charged” status
- On-chip silicon speed and temp sensors
  - Hardware thermal protection and shutdown circuitry

freescale™ semiconductor

Basic Logical Diagram of Power Block



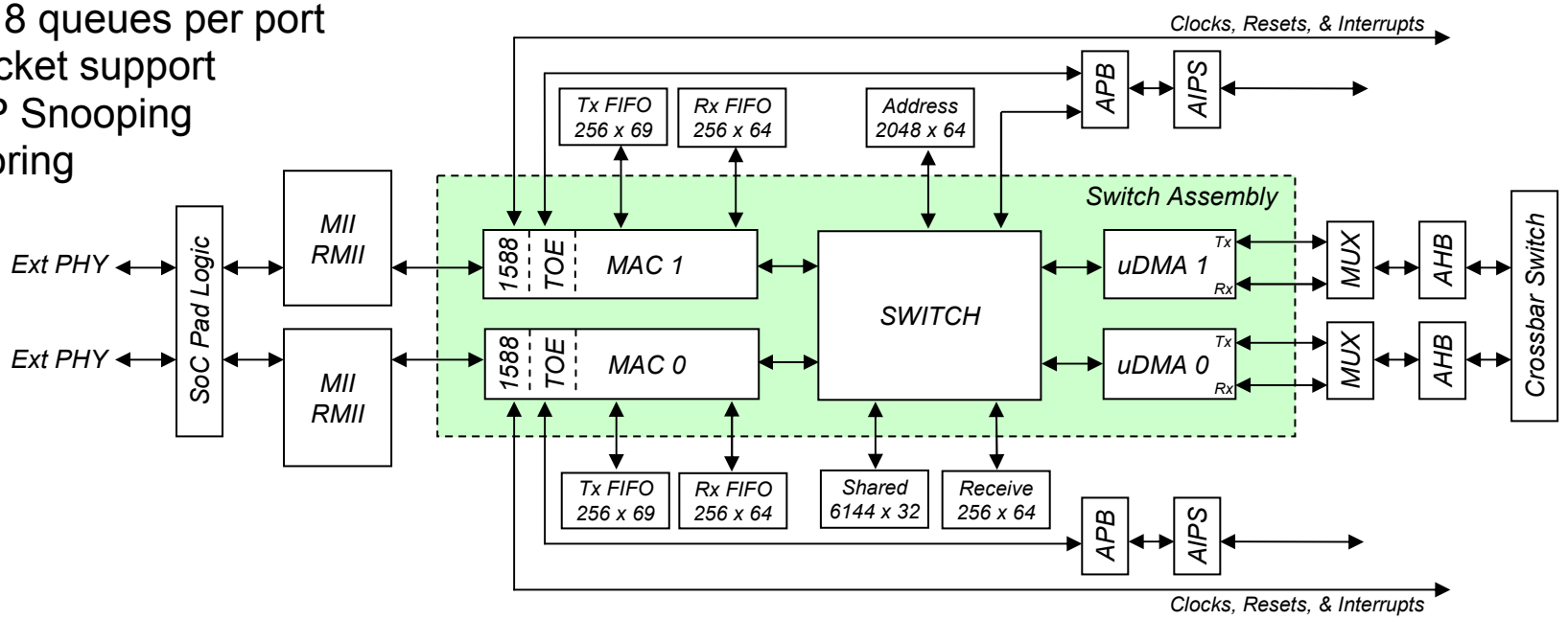
freescale semiconductor ™

Embedded Ethernet Assembly w/ L2 Switch

Product Features:

- 3-Port Switch (one internal)
- Separate dual-port FIFOs for max throughput
- TCP/IP Offload Engine (TOE)
- Hardware Time-stamping (IEEE 1588)
- Simple handshake programmable FIFO i/f
- Fast cut-through mode (MAC)
- Link aggregation, redundant backplane
- QoS with 8 queues per port
- Magic packet support
- Level 3 IP Snooping
- Port Mirroring

- ***System Benefits:***
  - ***Cost-effective daisy-chain networks***
  - ***Efficient ring networks with redundancy***
  - ***Improved determinism using hardware time stamping of packets (1588)***



freescale™ semiconductor

i.MX28 – Memory Support

- Off-Chip Memory Interface
  - Supports mDDR and 4 or 8 bank DDR2 or LV-DDR2 (not to be confused with LP-DDR2 which is not supported)
  - 200MHz, 16-bit wide data bus
- Flash Memory Types Supported
  - Raw SLC NAND
  - Raw MLC NAND
  - Managed NAND – eMMC 4.4, LBA
  - SPI NOR Flash
- Hardware BCH Interface
  - Provides a forward error-correction function to improve the reliability of raw NAND memory that may be attached to the i.MX28
  - BCH Engine with up to 20-bit correction (2-bit increments) with 13-bit parity.
- On-Chip 128KB SRAM
  - Ideal for low-power LCD refresh
  - Improved algorithmic performance

i.MX28 – Security

- Data Co-Processor (DCP) Peripheral
  - Hardware accelerated encryption/decryption and hashing functions (SHA-256) typically used for security
  - High Assurance Book (HAB4) – secure boot with authenticity checking
  - AES Crypto engine – AES boot provides encrypting the boot via a shared key
  - DCP OTP key can be used to wrap (encrypt) other keys or data
- On-Chip One Time Programmable (OTP) ROM
  - Enables / disables device functionality (i.e. JTAG)
  - Holds one customer specified encryption key
- SRAM storage for four additional temporary keys.
  - SW can select from the OTP or the additional keys via the descriptor interface.
  - Once the keys have been provisioned to the SRAM they cannot be read directly by SW. (Write-Once-Only)
- On-Chip Boot ROM
  - Integrated boot loader is only method for booting device
  - Can be configured to authenticate and decrypt boot images

i.MX28 – SSP

- Up to four independent Synchronous Serial Ports (SSP)
  - SD/MMC removable cards
  - eSD/eMMC/iNAND chips
  - SPI control and communication
    - Supports Winbond SPI dual/quad read modes up to 52MHz SCK frequency
  - SDIO for peripheral chips such as Wi-Fi or Bluetooth
  - Dedicated DMA channels

i.MX28 – Low Resolution A/D (LRADC)

- 12-bit Low-Resolution ADC, up to 0.5% battery level accuracy
- 16 total measurement nodes available
  - 8 physical channels available as external inputs
  - 8 “virtual” assignable channels for doing actual measurements can be mapped to any of the 16 measurement nodes
- Integrated 4-wire and 5-wire touch-screen controller (with wide range of impedance support, e.g 200-400 Ohm and 50K Ohm)
- Integrated temperature sensor function (on-die, and external with diode or thermistor) to monitor the internal die temperature
  - Three sigma temperature error of +/-1.5% in degrees Kelvin
  - Temperature sampling has a 3 sigma sample-to-sample variation of 2 degrees Kelvin which can be averaged out .
  - Thermal protection on i.MX28 - Safety switch will reset the part when the shutdown temperature is reached
- Single channel high speed ADC – 2Msps at 12-bits

i.MX28 Peripherals – Other I/O

- I^2C
  - EEPROM, Sensors
  - DMA controlled with M/S mode up to 400KHz
- 4-Channel 16-Bit Timers with Rotary Decoder
- Six-Channel Pulse Width Modulator (PWM)
- Real-Time Clock
  - Options for 24MHz, 32KHz or 32.768KHz
  - Storage of “persistent bits”
  - Wake from alarm

- *UARTs*
  - *2 or 5 x 3.25Mbps App UARTs*
  - *1 x 115Kbps Debug UART*
- *S/PDIF Transmit*
- *Dual Serial Audio Interface (SAIF), Two Stereo Pairs*
  - *Full-duplex stereo transmit and stereo receive operations (requires both SAIF interfaces)*
  - *Bluetooth hands-free connection*
  - *I^2S, left-justified, right-justified, and non-standard formats*

freescale™ semiconductor


freescale™
semiconductor