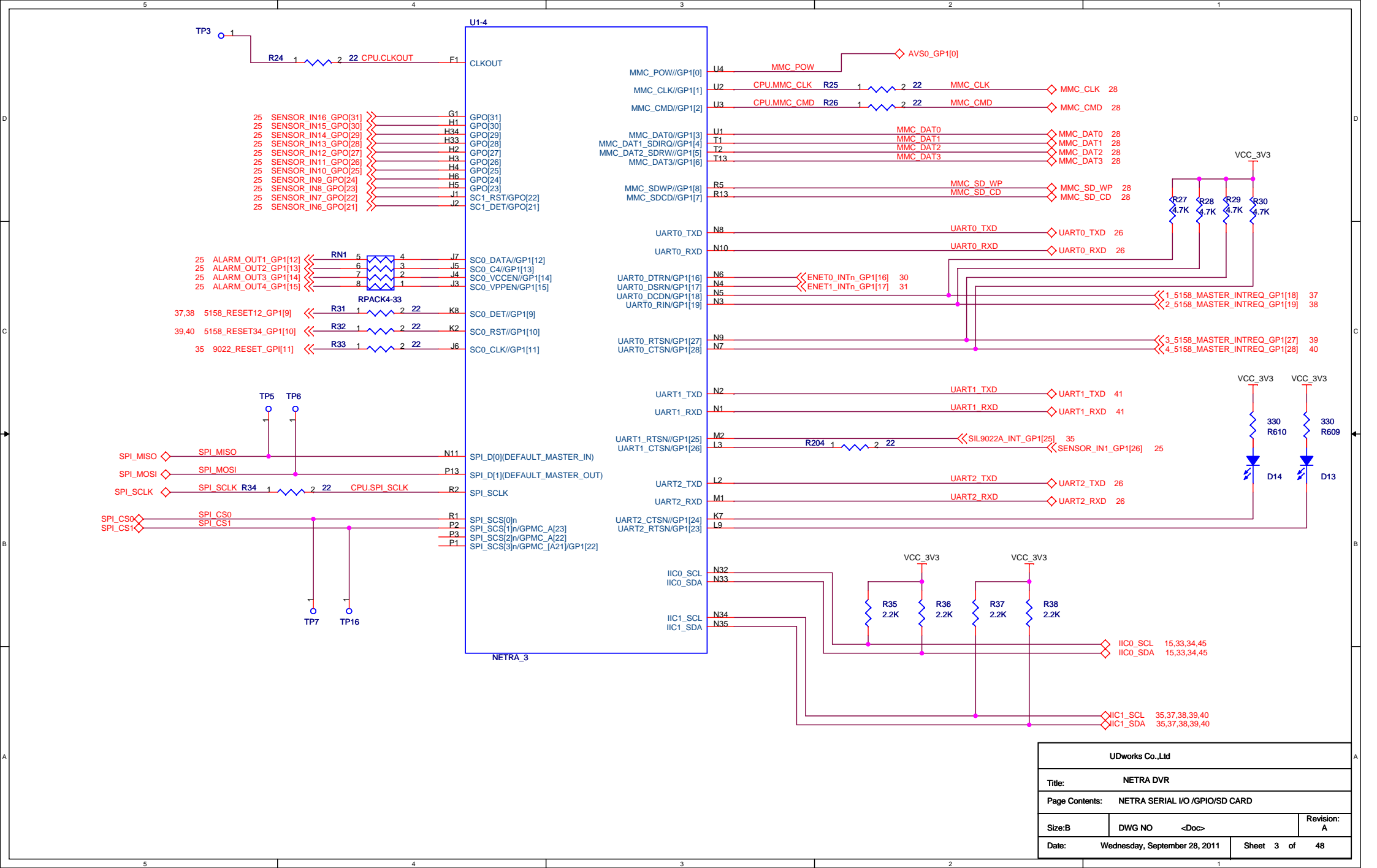
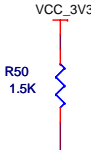
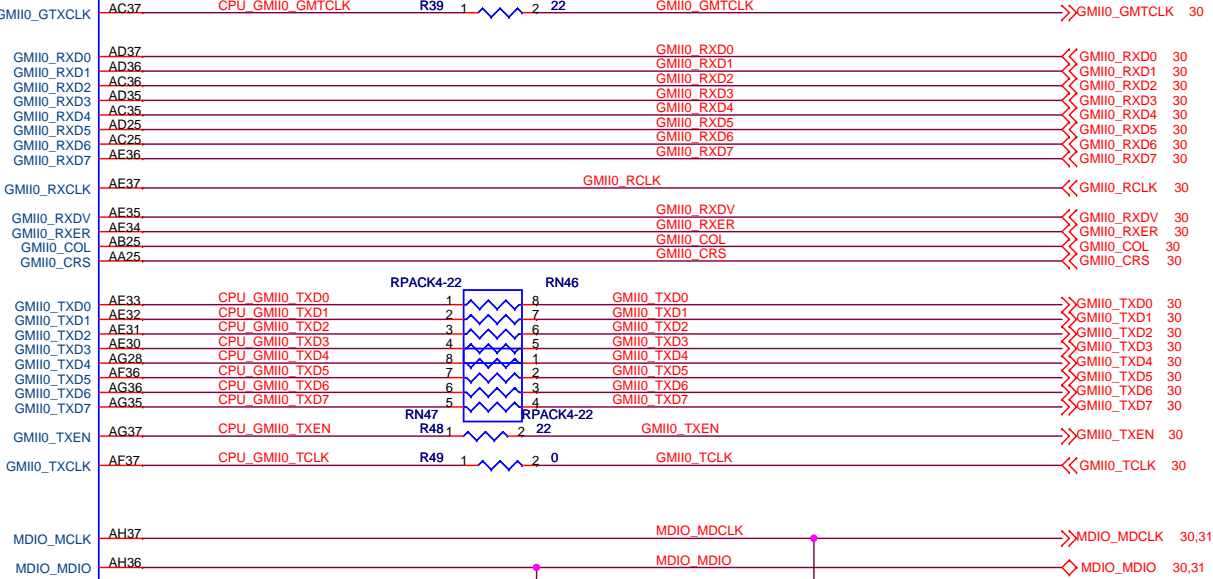


5					4					3					2					1									
Netra DVR RD																													
REV										DESCRIPTION										DATE					APPROVED				
A										Initial schematic for layout										07/12/2010					SDS				
rev0.2										change DDR2 to DDR3										12/02/2010					SDS				
rev0.3										change Q19, Q20(FDS8817) to FDS8812										01/25/2011					SDS				
rev0.3A										1. Modify SATA port LED GPIO numbers 2. Modify the Video Sync separator input circuit on the VGA output port. 3. Modify filter setting on the Video Amp(THS7360) 4. Change power devices (1V0_CON) 5. Change 5158 AUDIO IF MODE to cascade mode (McASP interface). 6. Change the Ethernet PHY initial Mode (Auto-negotiation enable) to the 100Mbit mode for GIGABIT mode issue. 7. Change the Capacitor value 22uF to 47uF (or add 22uF) on the Ethernet PHY's internal power. 8. Add reset signal on the AIC3101 audio Codec.										05/13/2011					SDS				
rev0.4										1. Change power devices (1V0_AVS, VCC_1.8V, VCC_1.1V, VCC_1.3V)										05/23/2011					SDS				
rev0.5										1. Modify VTT power enable signal. 2. Modify sync signals of the RGB(VGA) output for The PG2.0 netra. 3. Modify AC coupled capacitor value in the SATA port. 4. Change the ESD device in the USB port. 5. Change the TPS40400 PMBus address "00" to "70" (R706 : 10K -> 200K)										09/23/2011					SDS				
rev0.5A										1. eSATA port is changed to the JMB321's port1. Netra SATA port0 is connected to the SATA port (J15) for the ODD										09/26/2011					SDS				

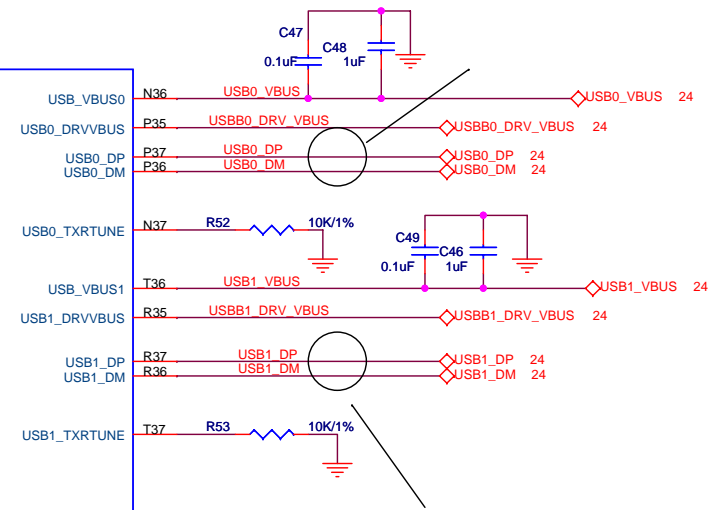
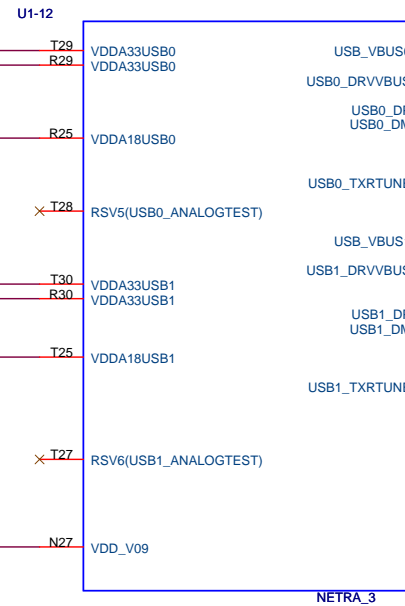
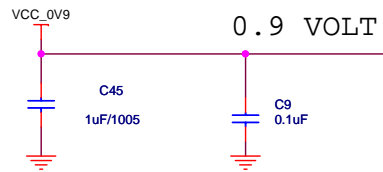
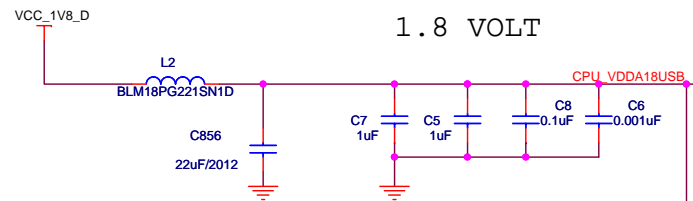
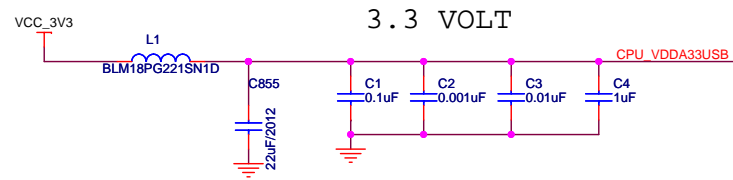


U1-10

NETRA_3

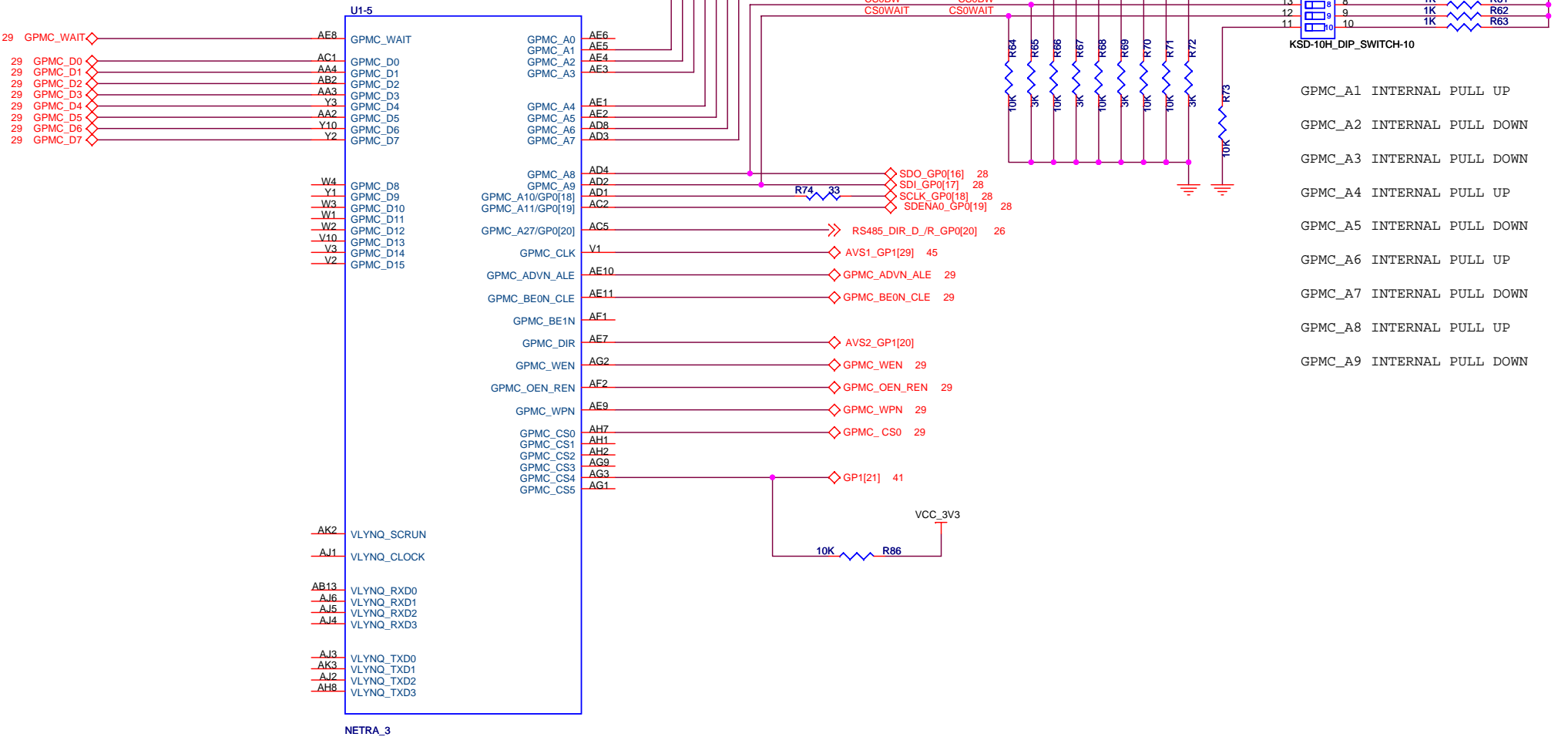


UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA ETHERNET PORT0			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Wednesday, September 28, 2011	Sheet 4 of	48

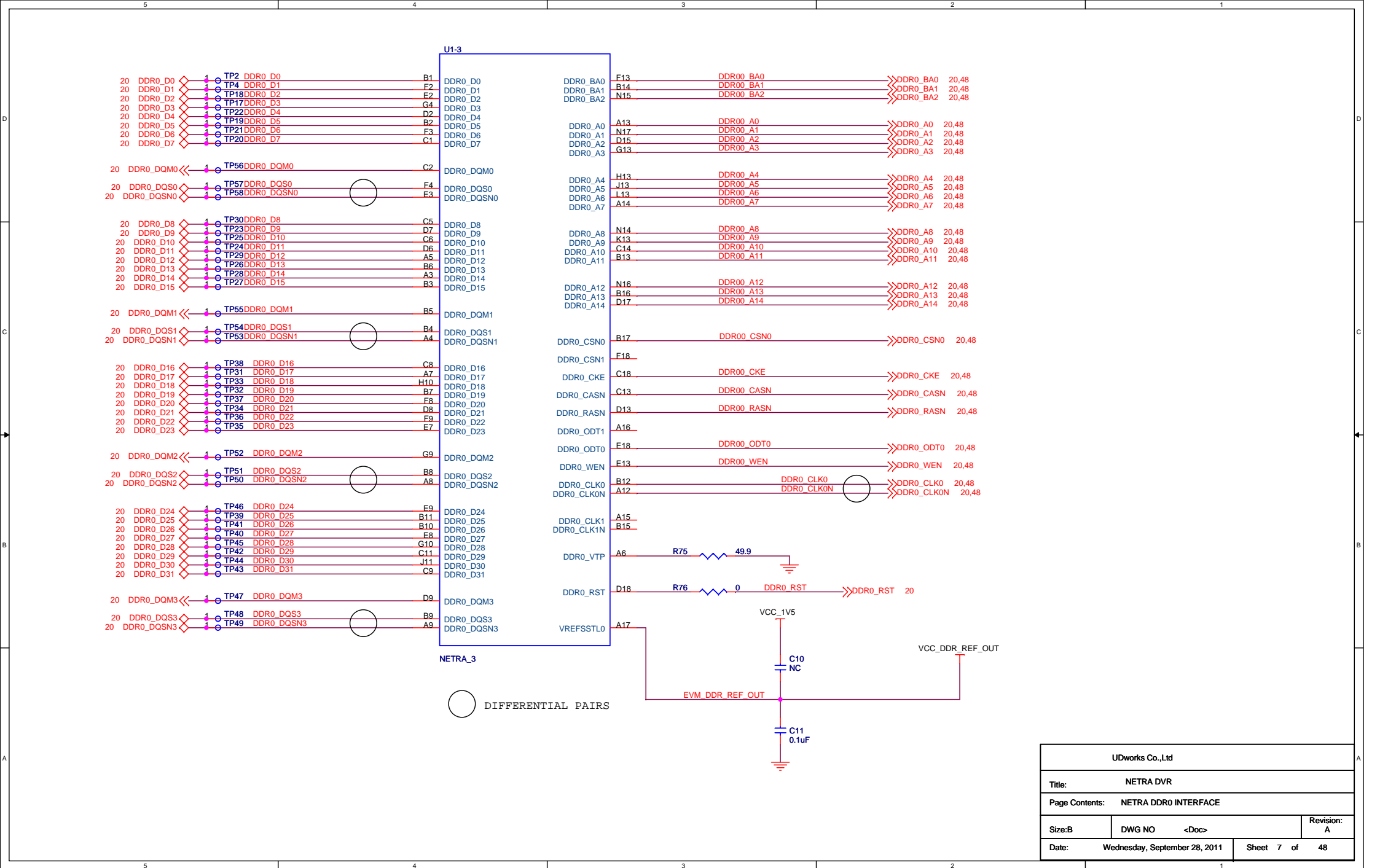


UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA USB			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Wednesday, September 28, 2011	Sheet 5 of	48

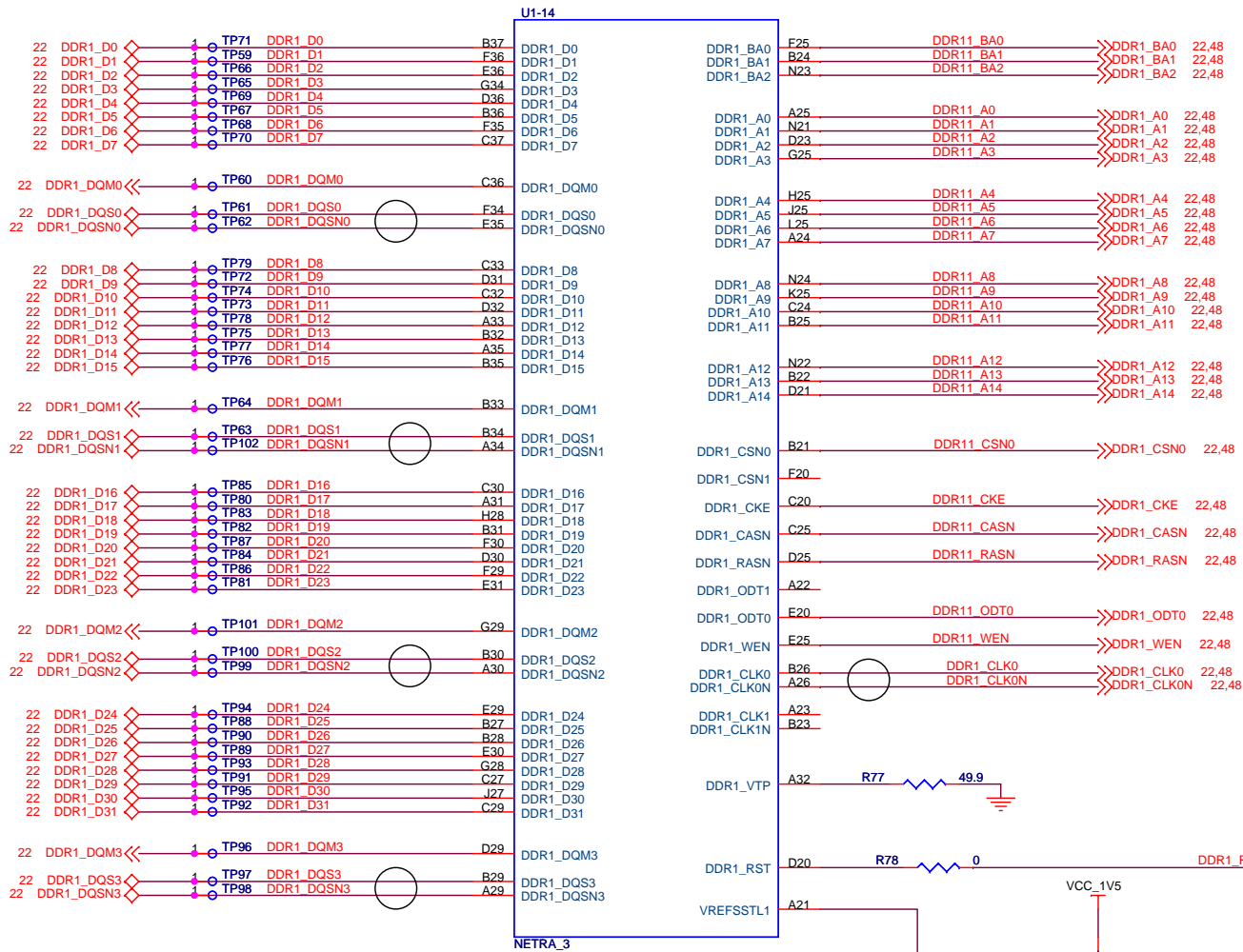
GPMC_A[9:1] = 0000 10010 -> NAND BOOT 8bit



UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA GPMC/GPIO			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Wednesday, September 28, 2011	Sheet 6 of	48

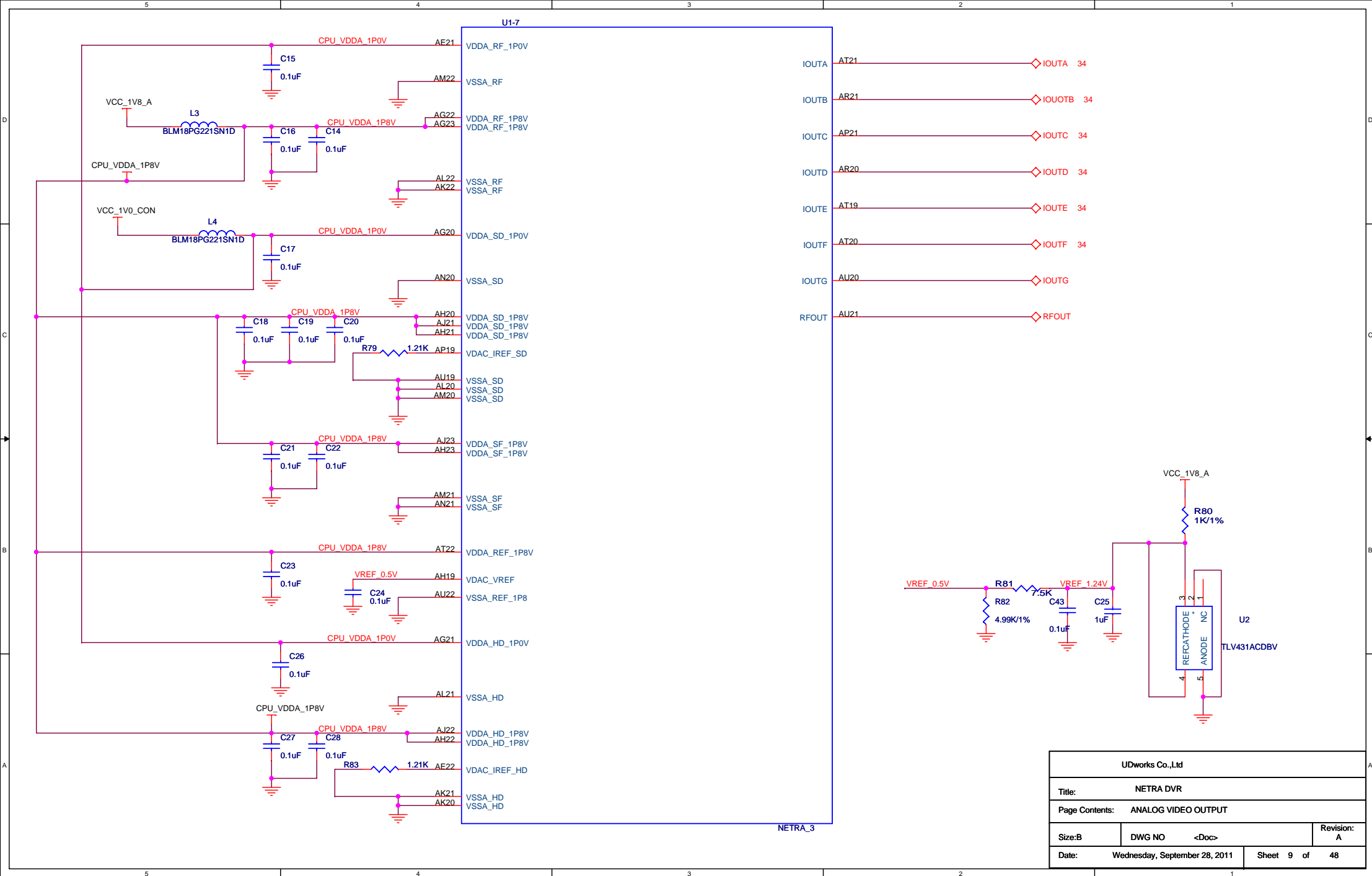


UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA DDR0 INTERFACE			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Wednesday, September 28, 2011	Sheet 7 of	48

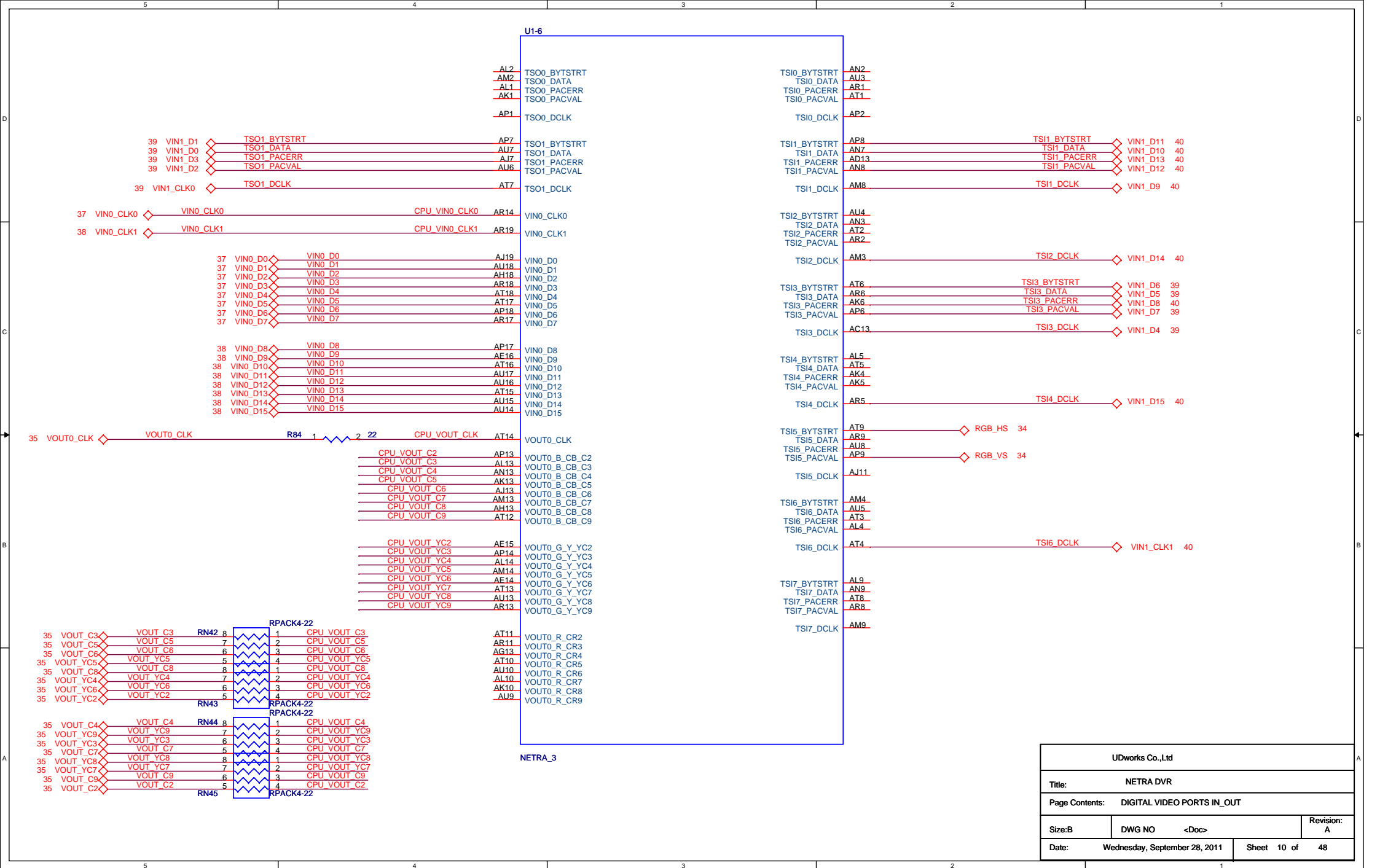


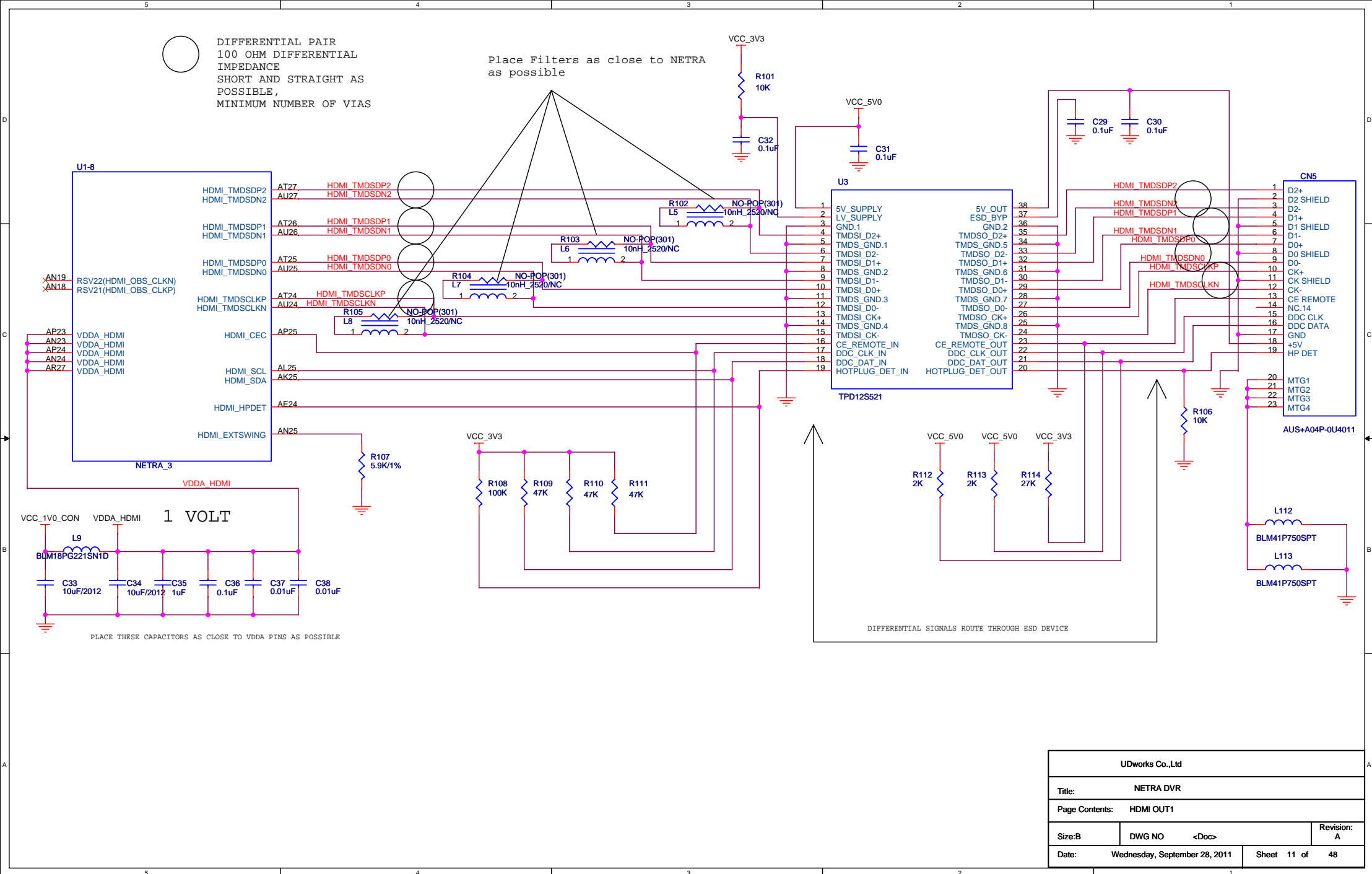
DIFFERENTIAL PAIRS

UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA DDR1 INTERFACE			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Wednesday, September 28, 2011	Sheet 8 of	48

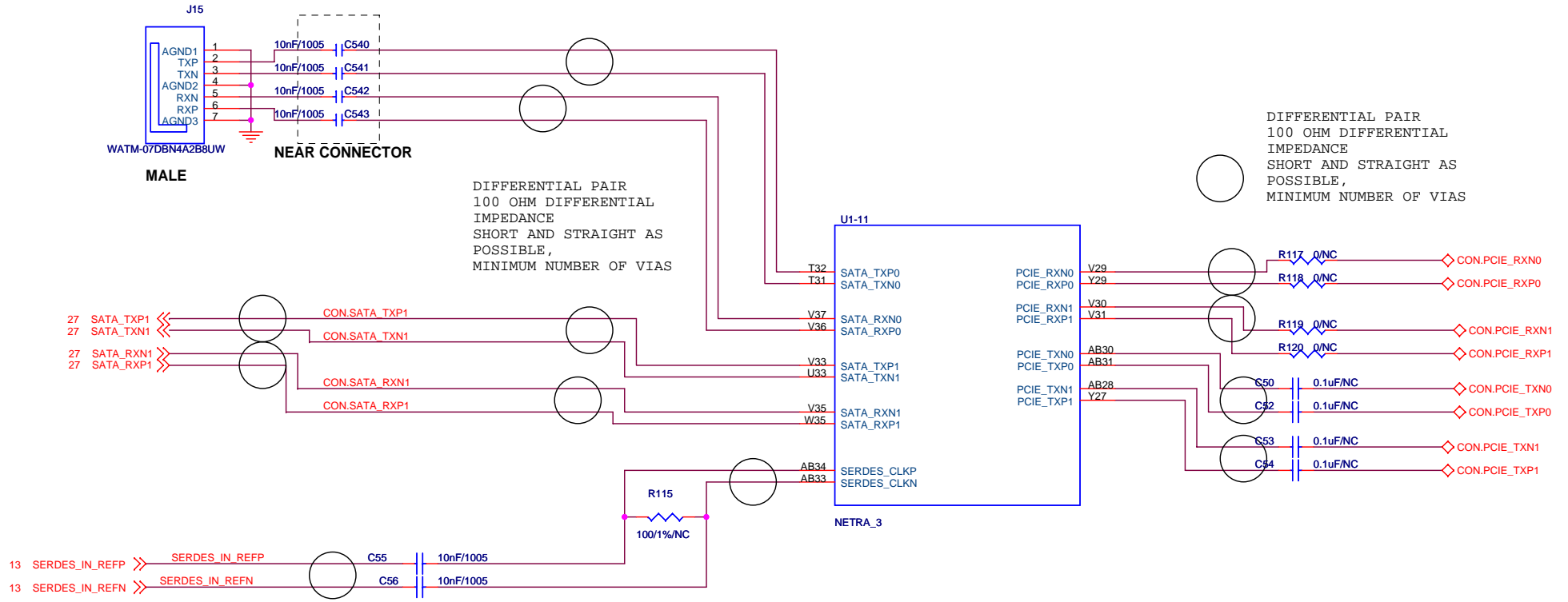


UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: ANALOG VIDEO OUTPUT			
Size:B	DWG NO <Doc>		Revision: A
Date:	Wednesday, September 28, 2011	Sheet 9 of	48

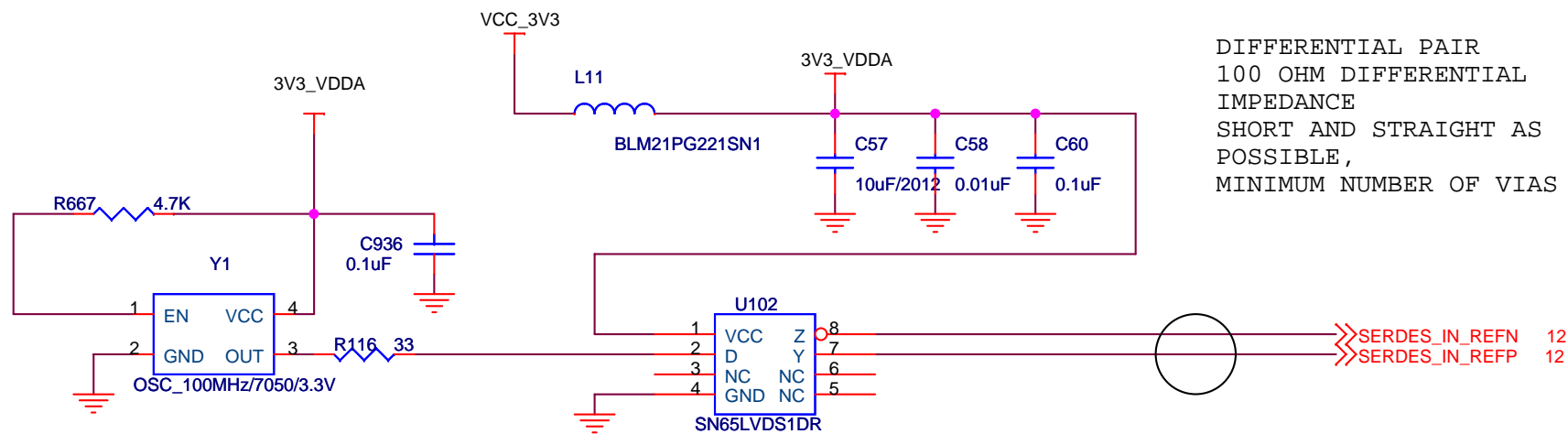




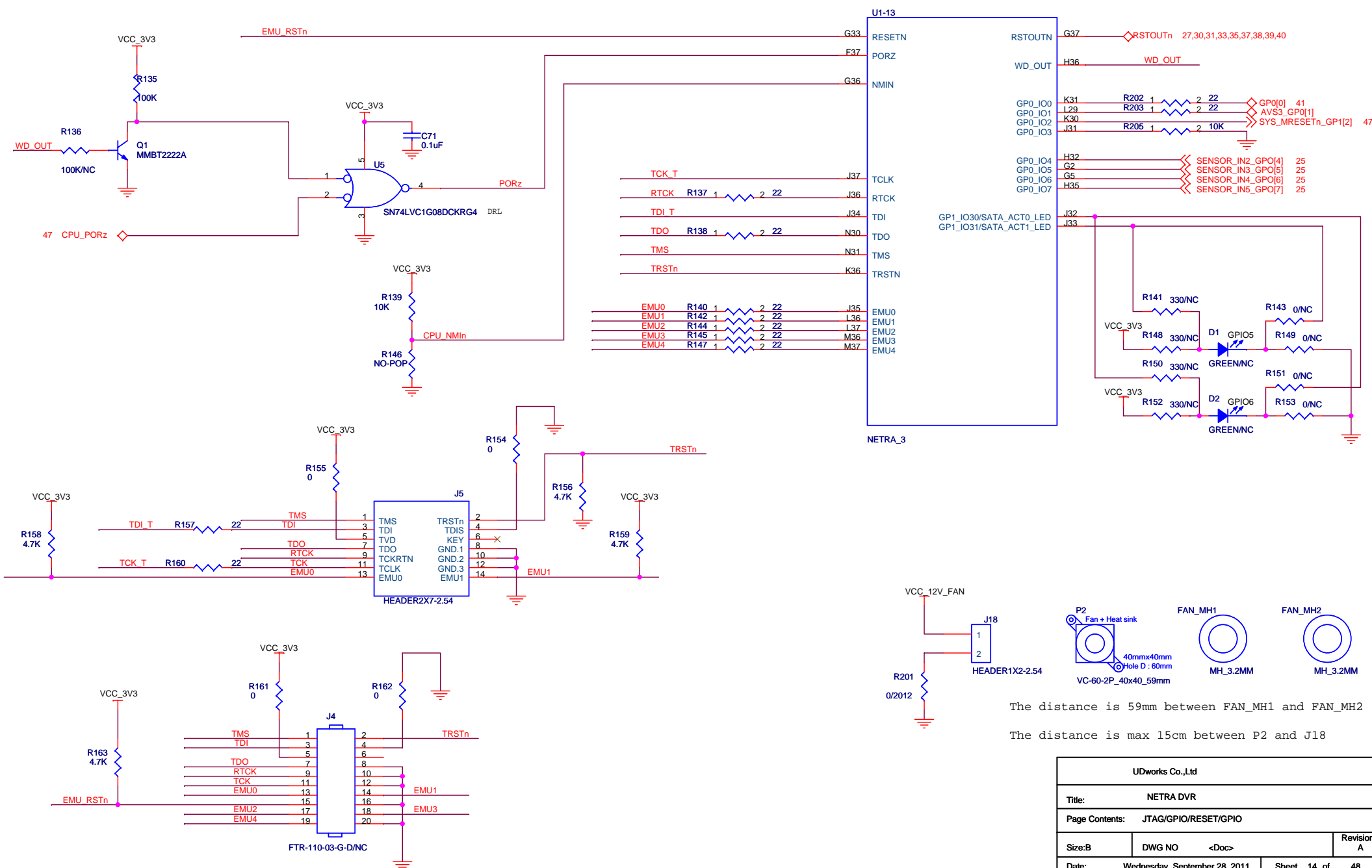
ODD SATA CONNECTOR



UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: SATA INTERFACE			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Wednesday, September 28, 2011	Sheet 12 of	48



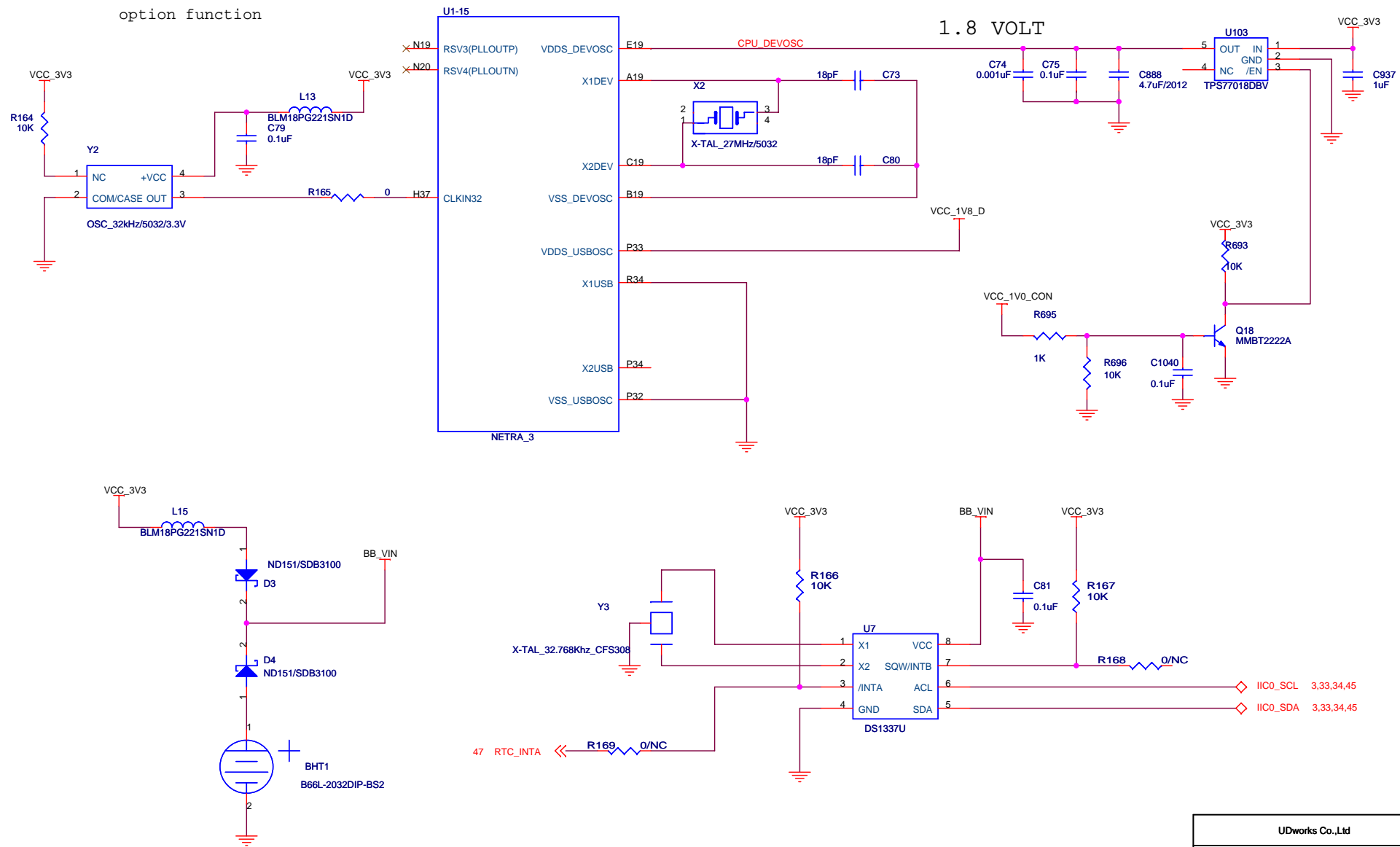
UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: SERDES CLOCKS			
Size:A	DWG NO	<Doc>	
Date:	Wednesday, September 28, 2011	Sheet 13 of	48



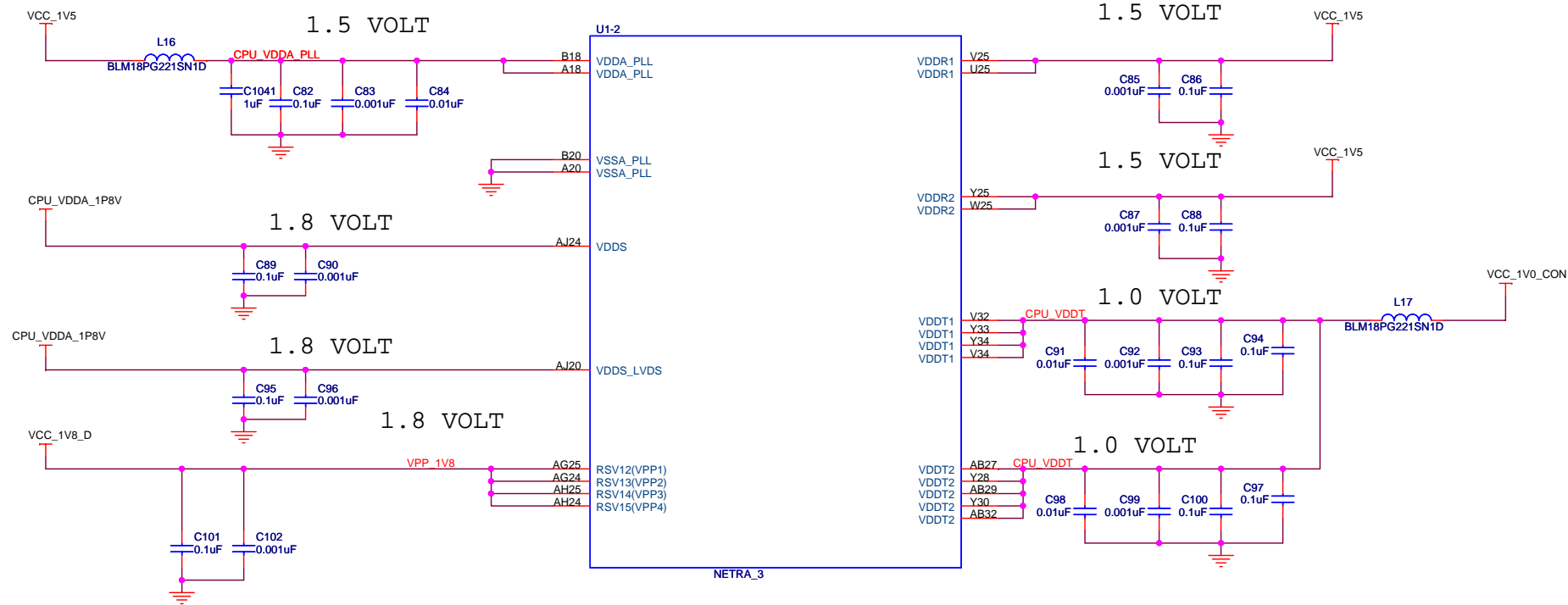
The distance is 59mm between FAN_MH1 and FAN_MH2

The distance is max 15cm between P2 and J18

UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: JTAG/GPIO/RESET/GPIO			
Size: B	DWG NO	<Doc>	Revision: A
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UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA CLOCKS/RTC			
Size: B	DWG NO	<Doc>	Revision: A
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U1-17

RSV10(THERMAL_P)

RSV11(THERMAL_N)

NETRA_3

U1-22

(AMUX_DDR)RSV20

(AMUX_MAIN)RSV8

(PCIE_AMUX)RSV1

(SATA_AMUX)RSV2

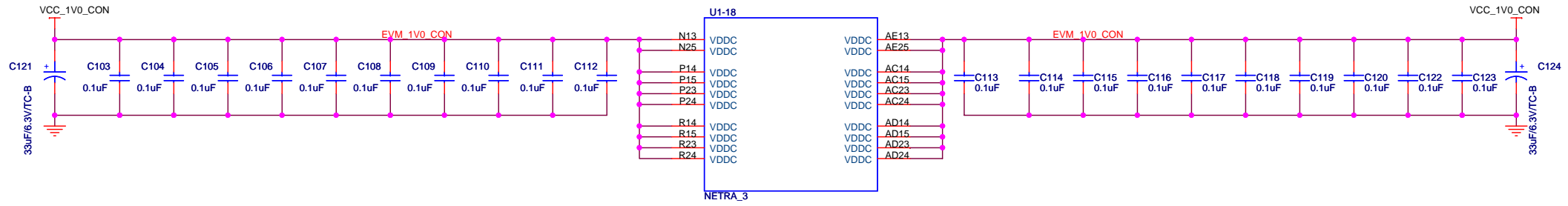
(IFORCE)RSV9

(VSENSE)RSV7

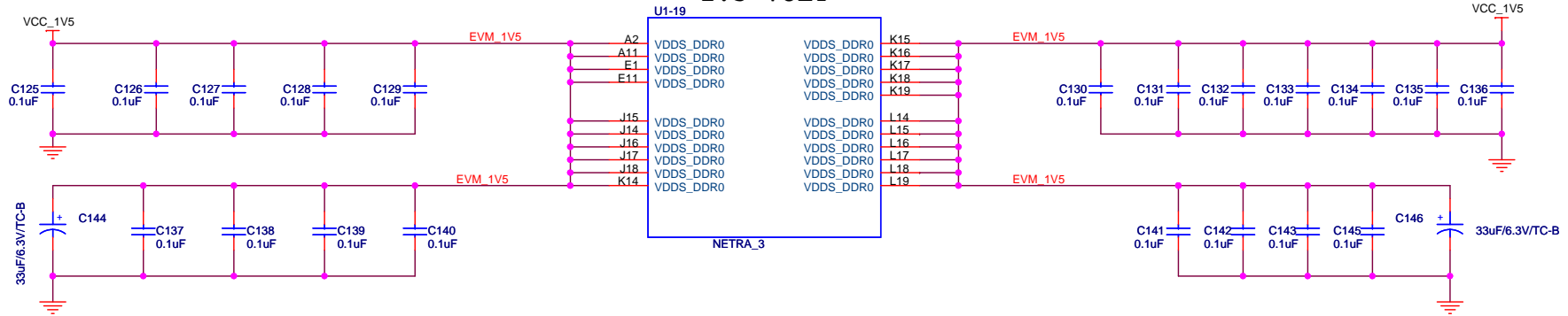
NETRA_3

UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA POWER PINS			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Wednesday, September 28, 2011	Sheet 16 of	48

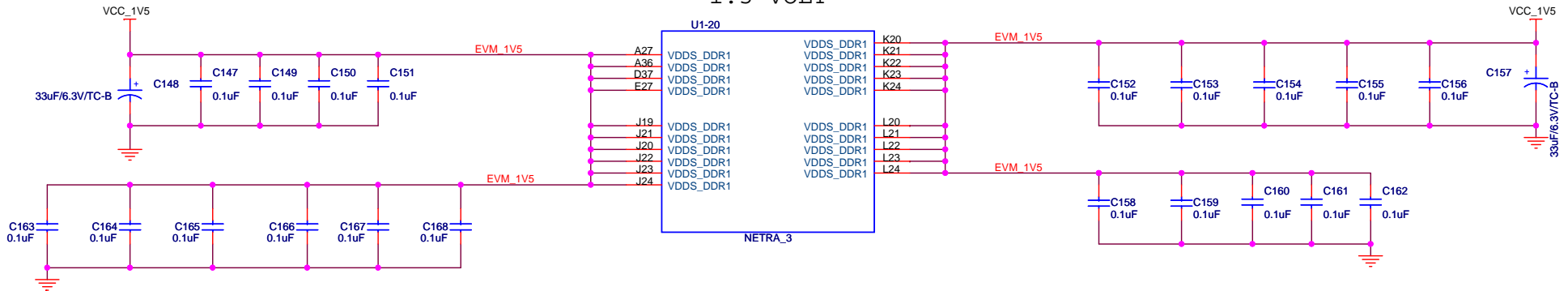
1 VOLT



1.5 VOLT

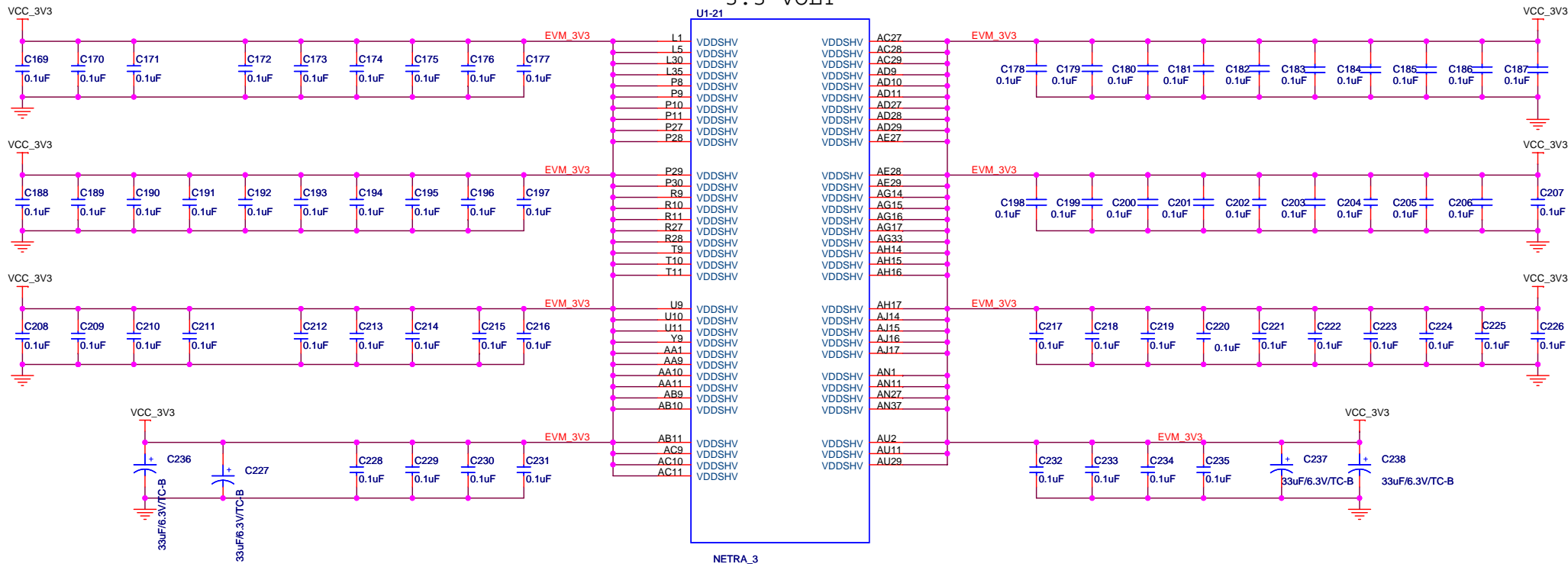


1.5 VOLT

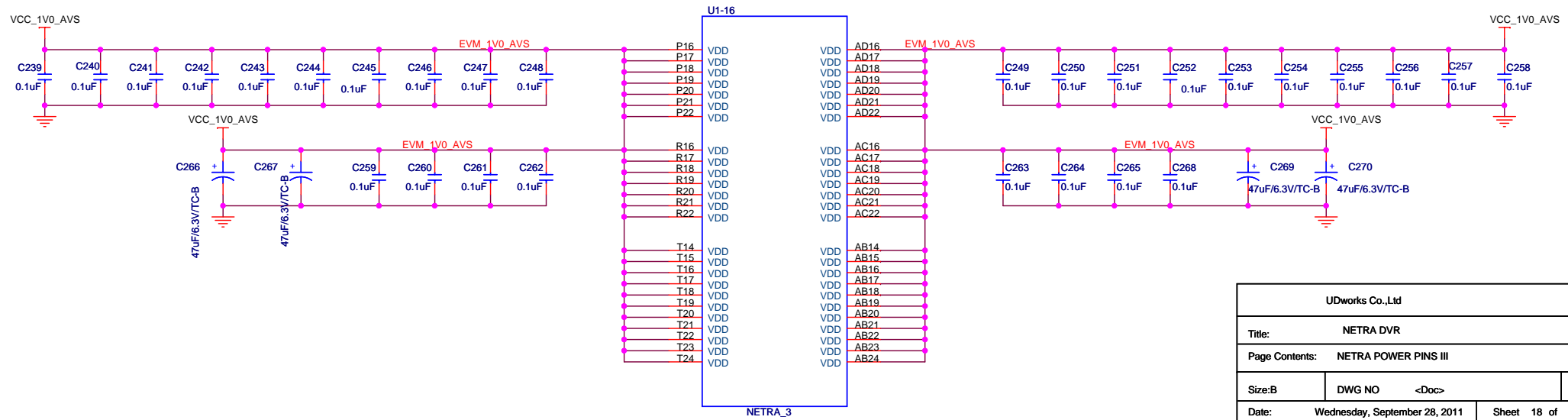


UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA POWER PINS II			
Size: B	DWG NO	<Doc>	Revision: A
Date:	Wednesday, September 28, 2011	Sheet 17 of	48

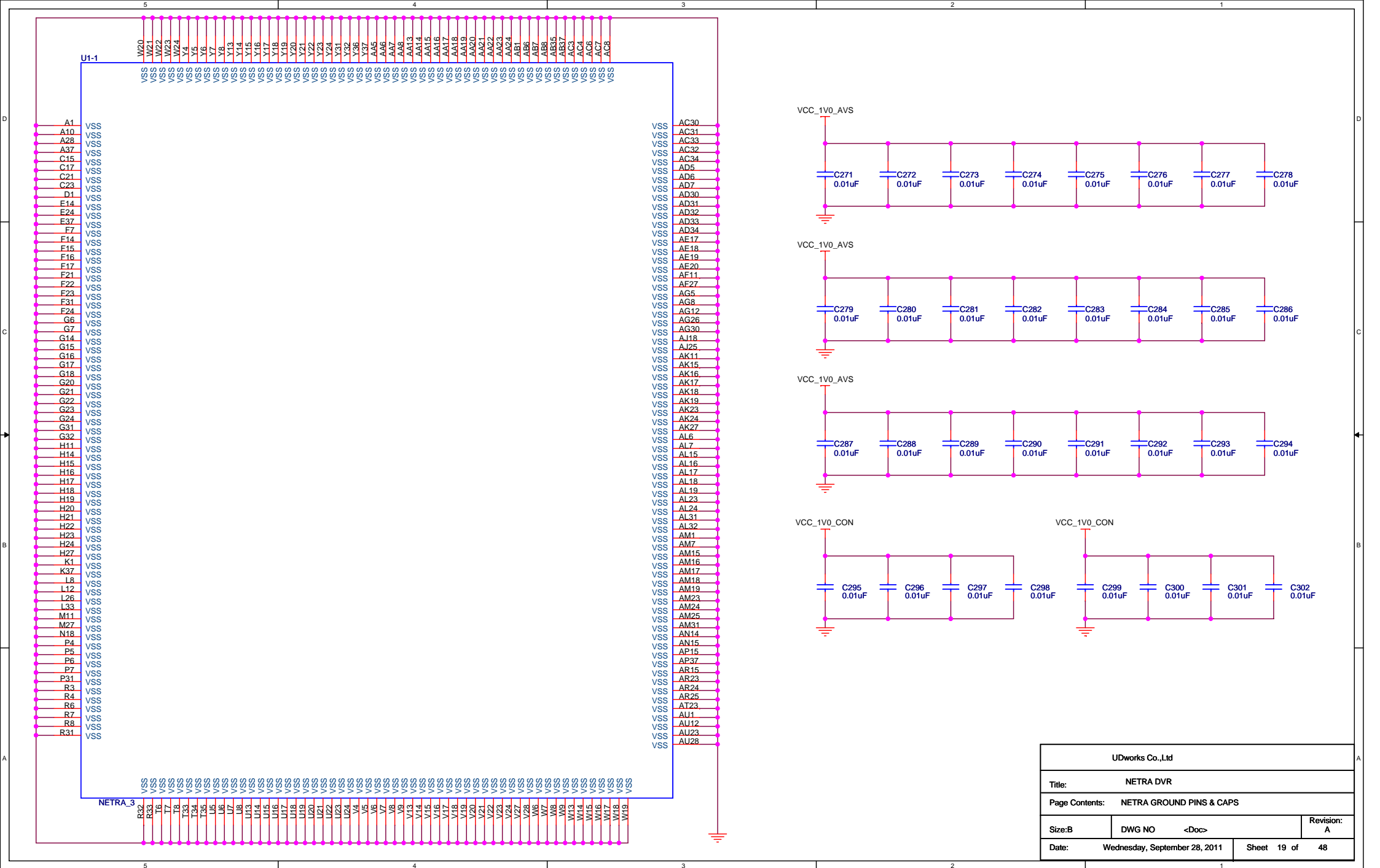
3.3 VOLT

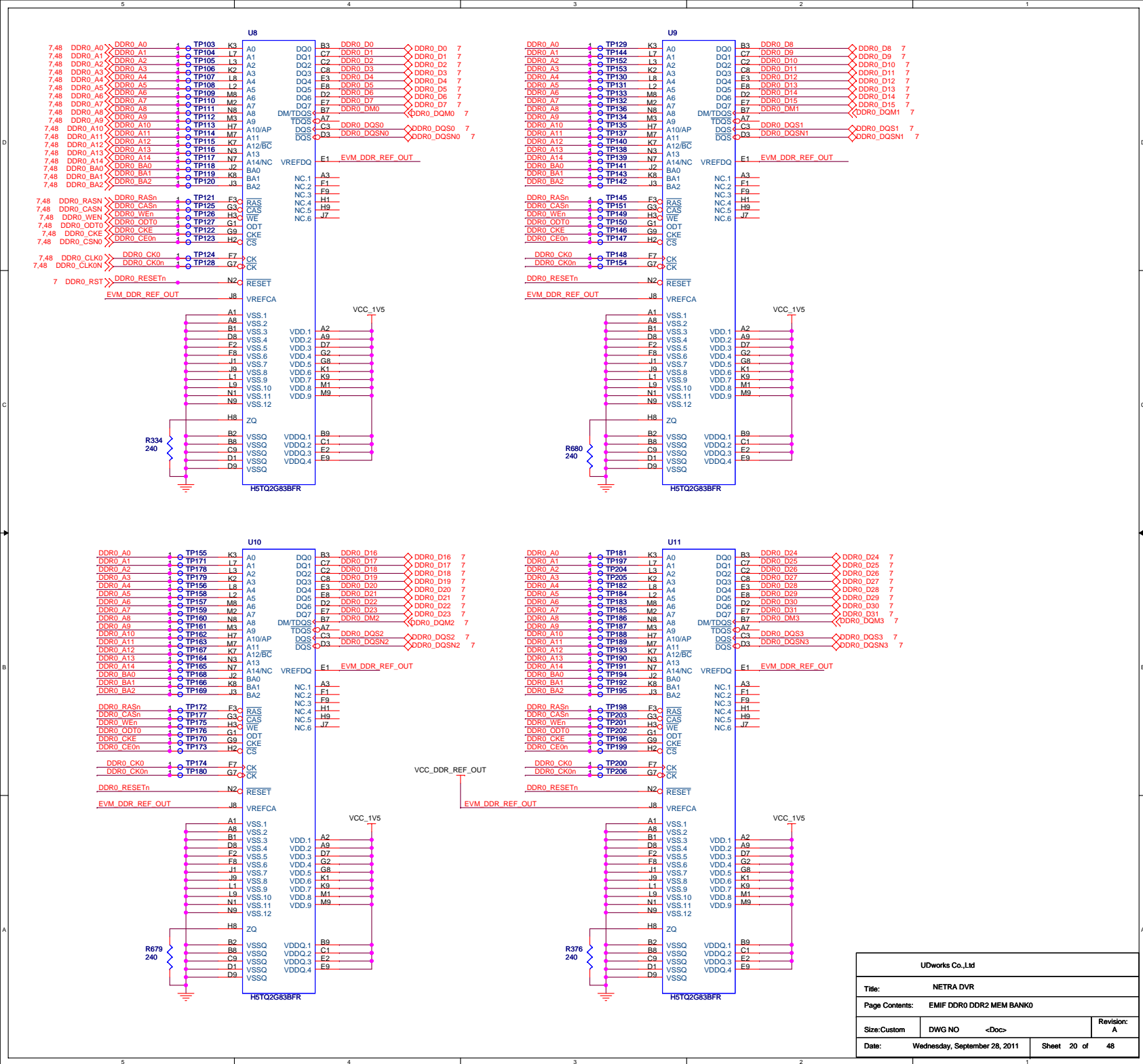


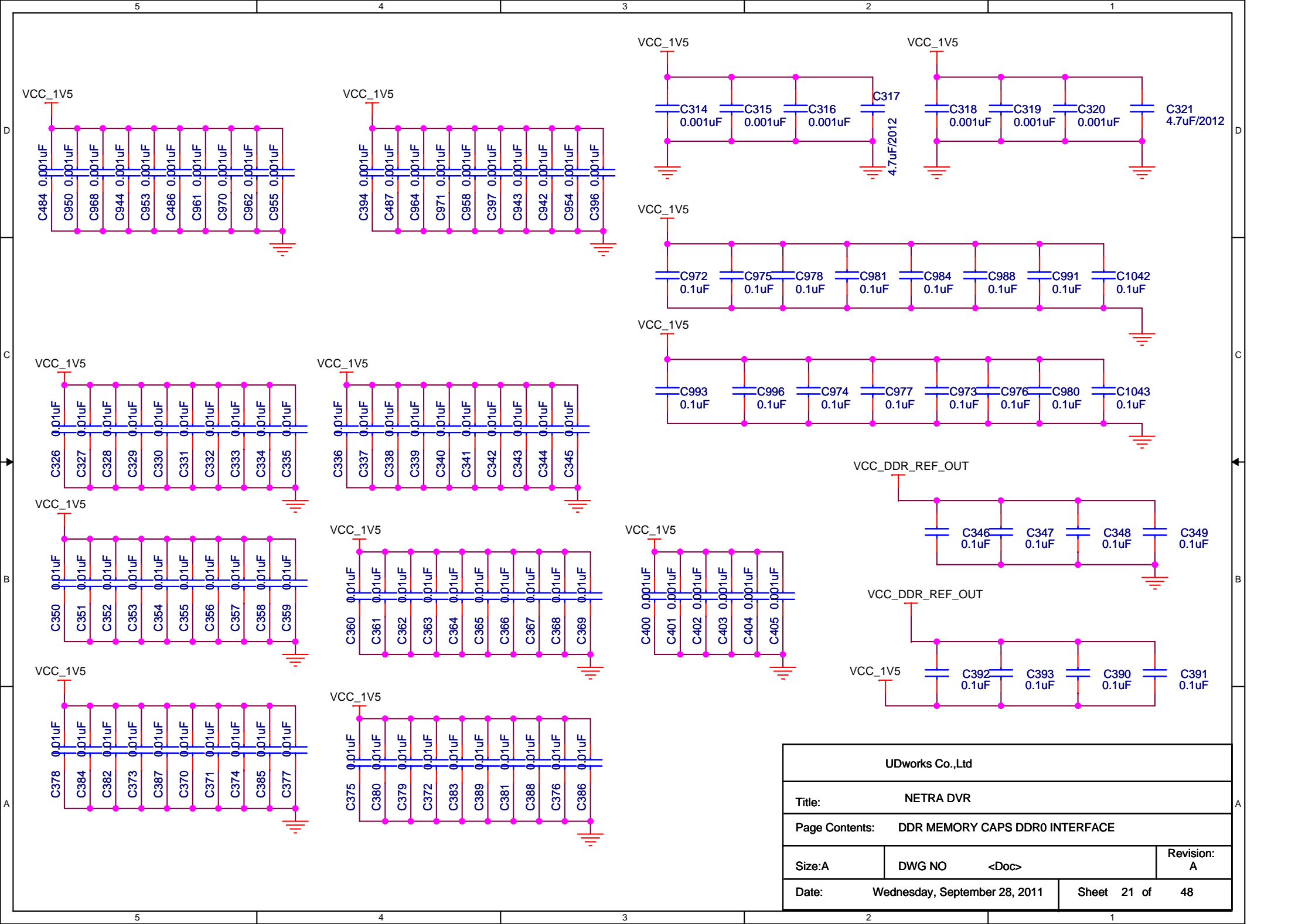
CORE AVS SUPPLY 1.0 VOLT

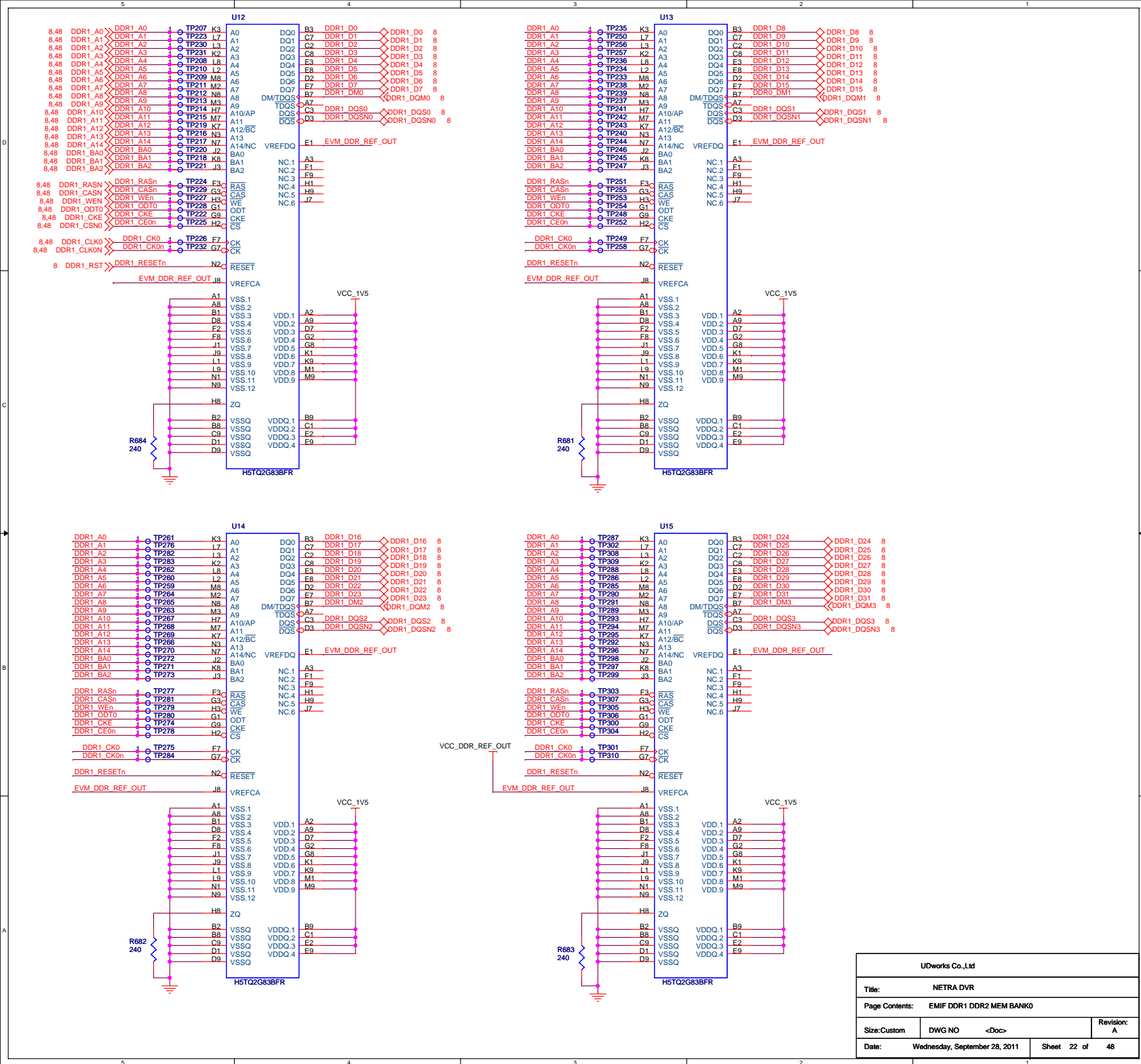


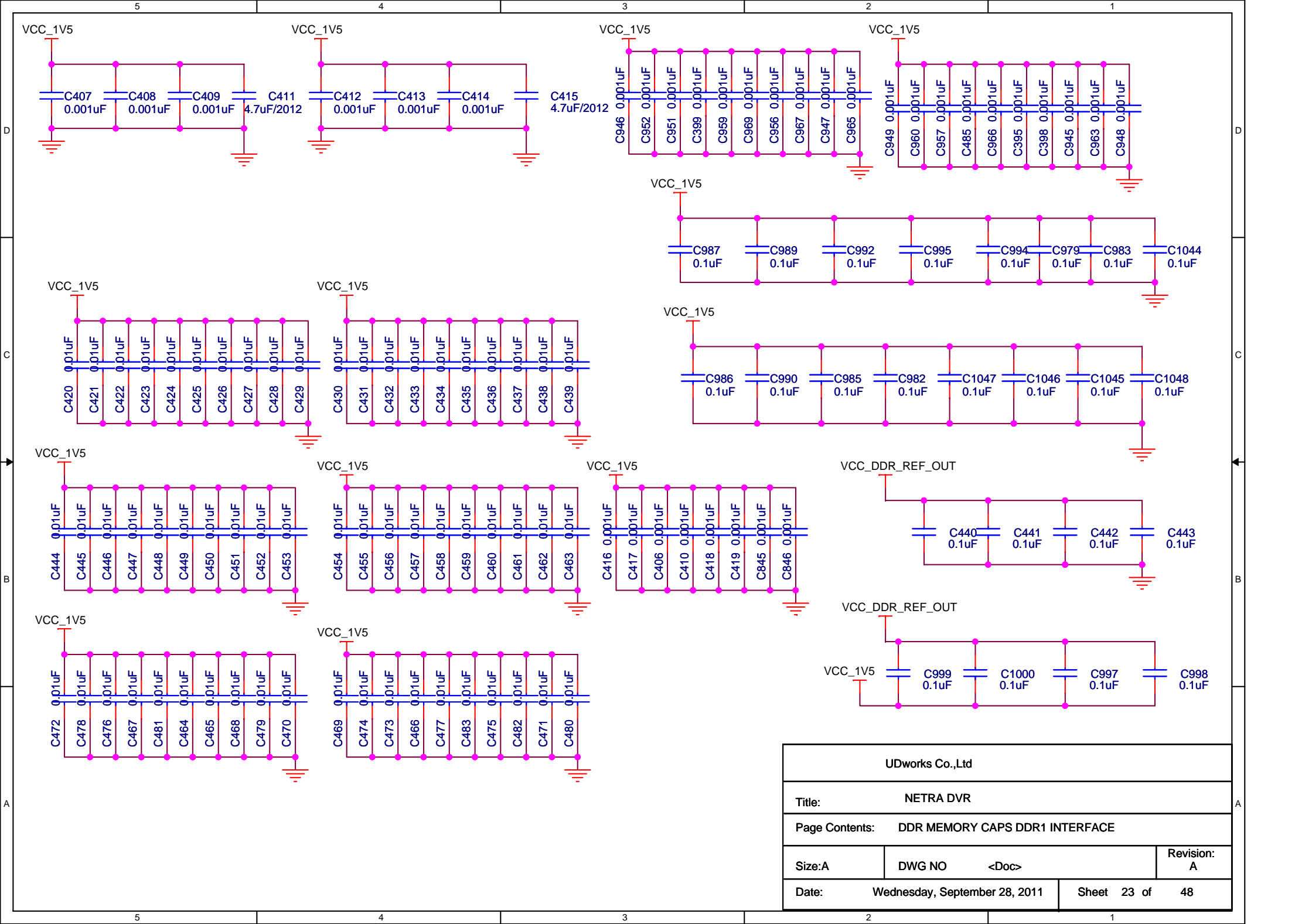
UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA POWER PINS III			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Wednesday, September 28, 2011	Sheet	18 of 48

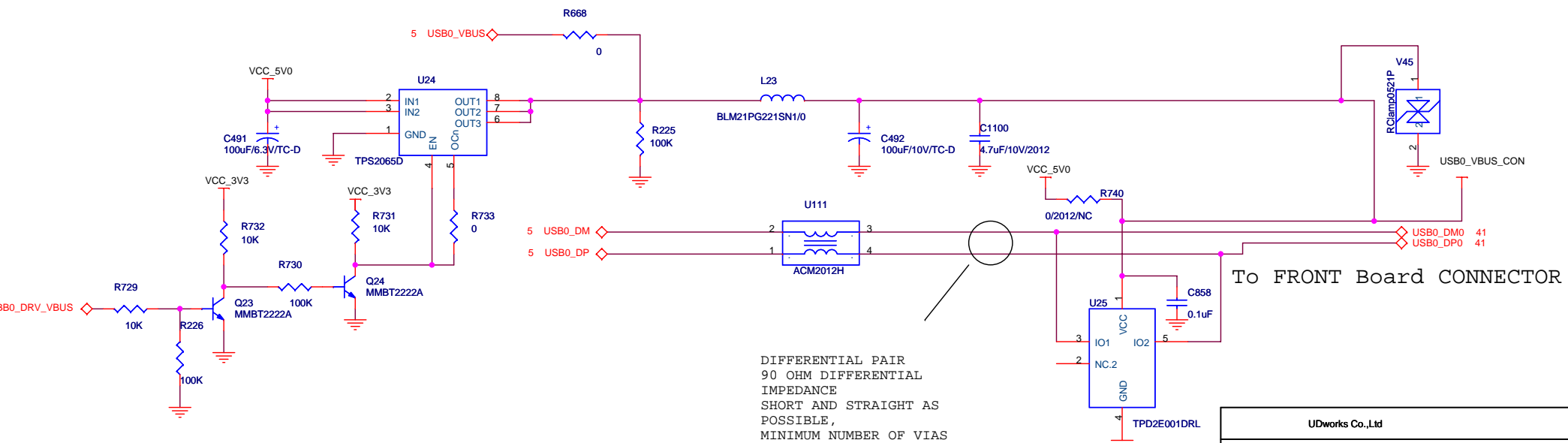
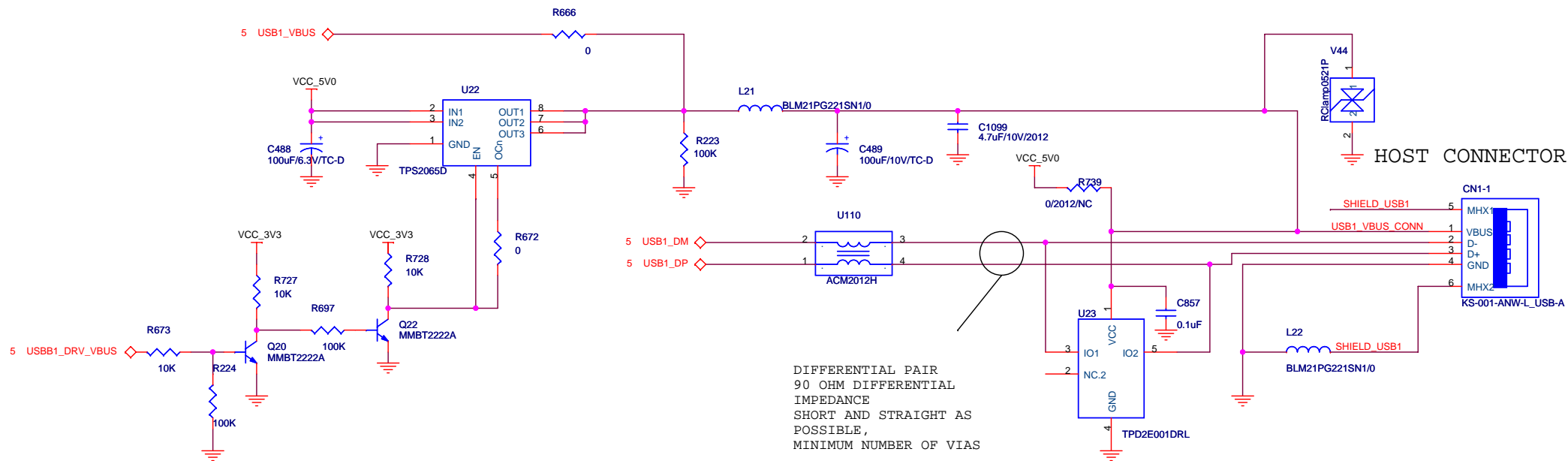




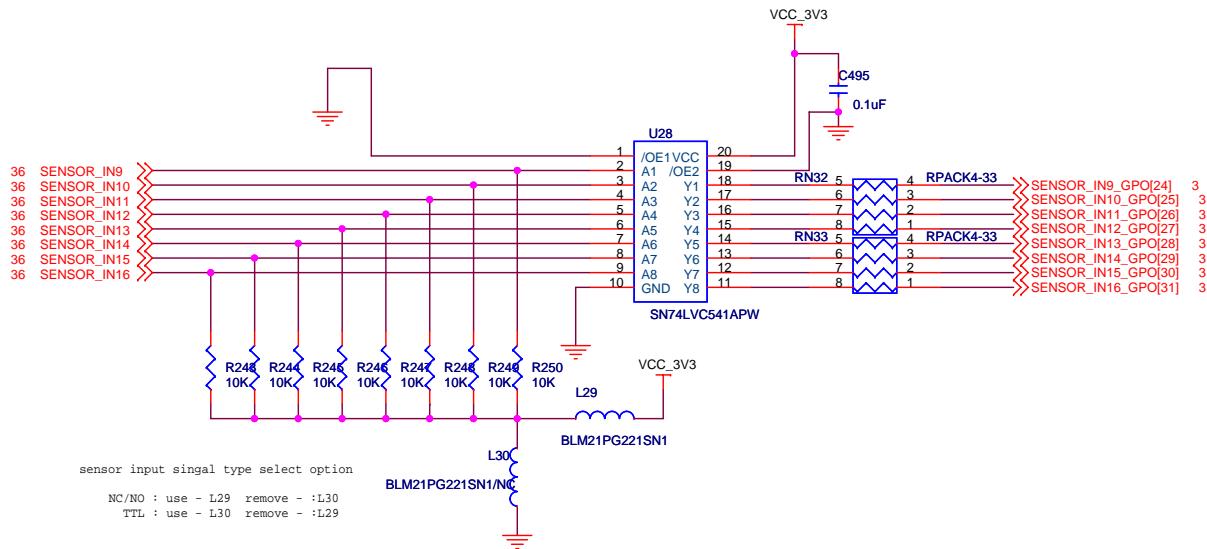
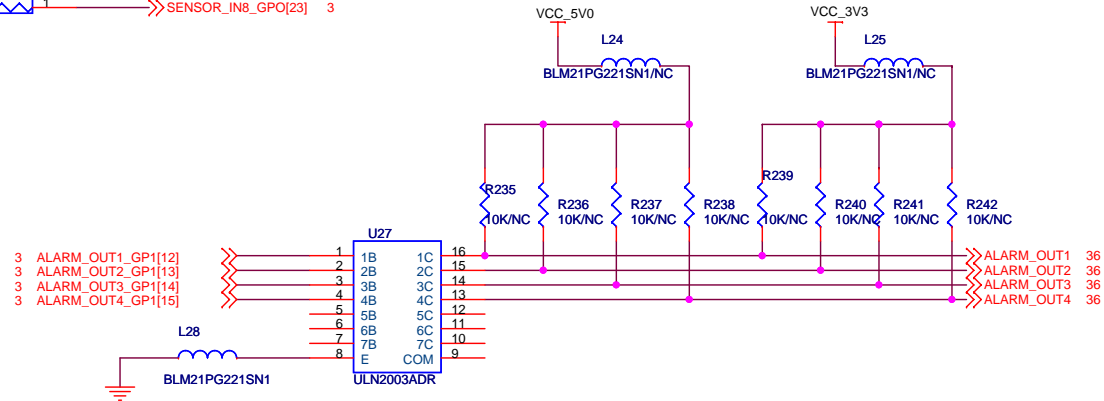
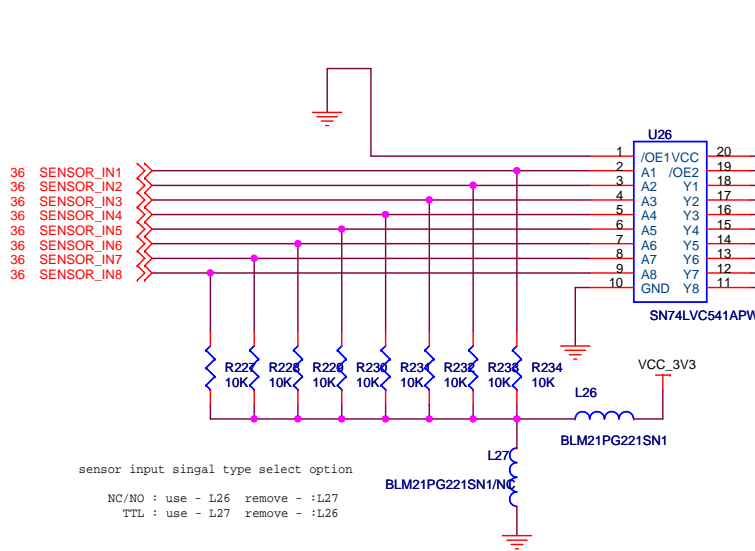




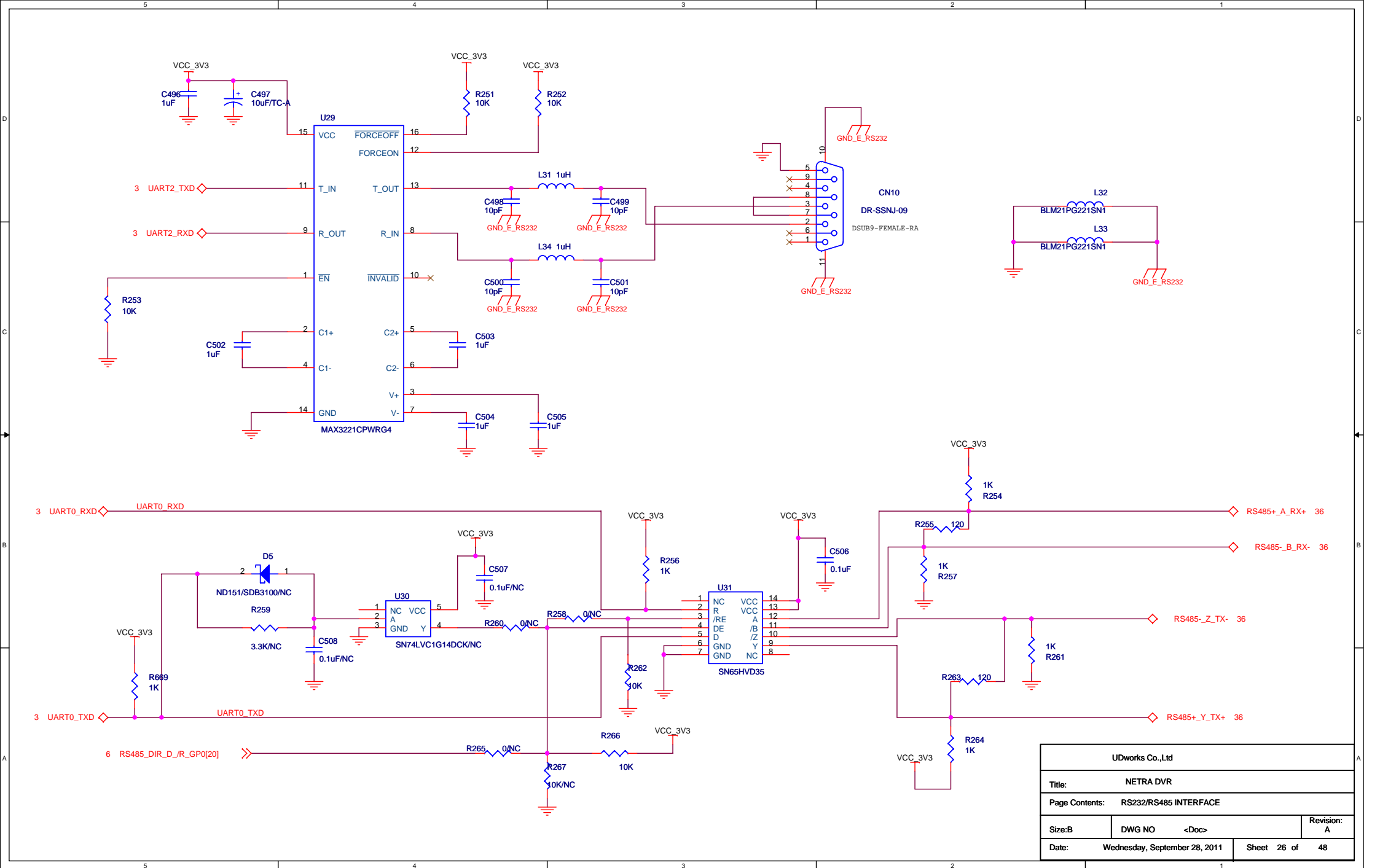




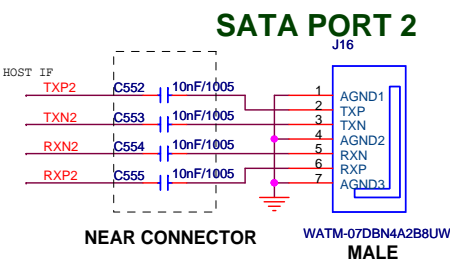
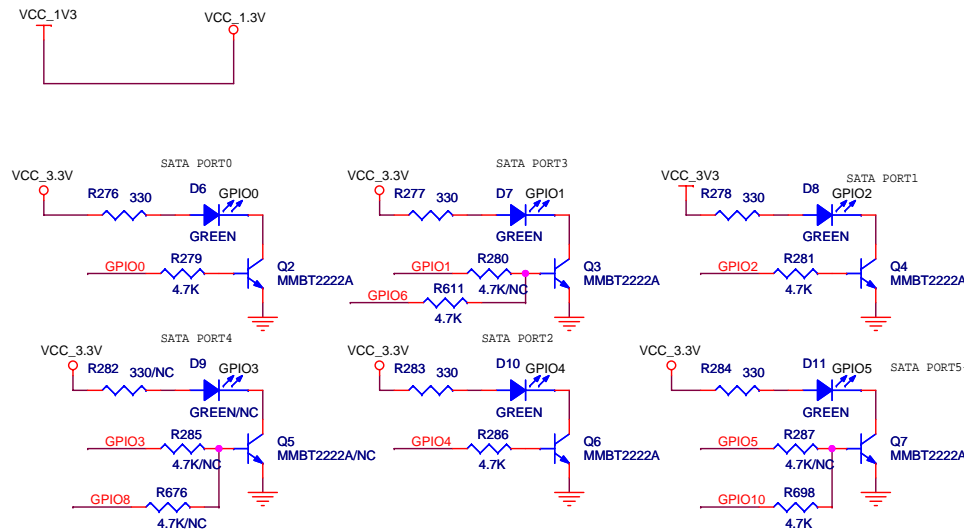
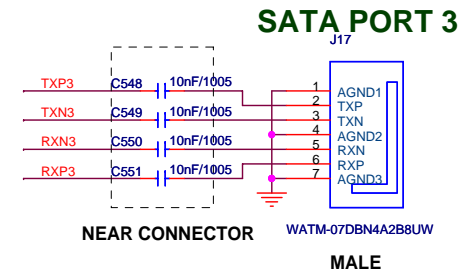
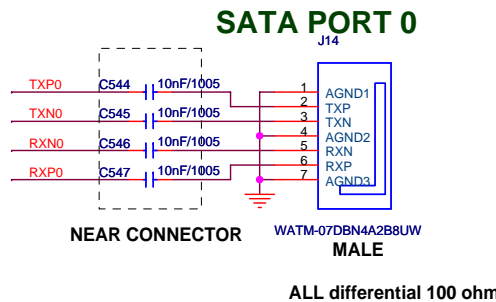
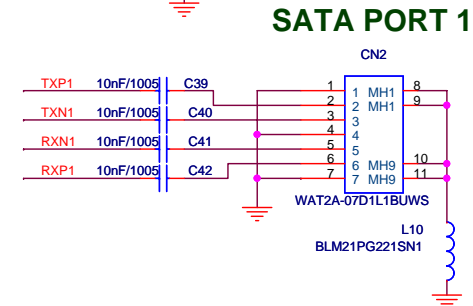
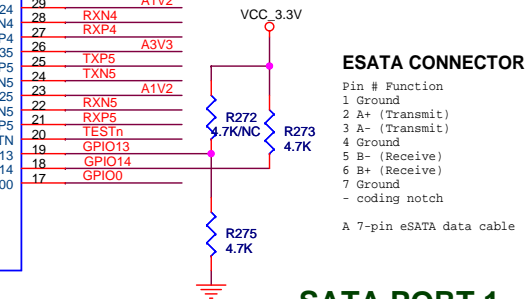
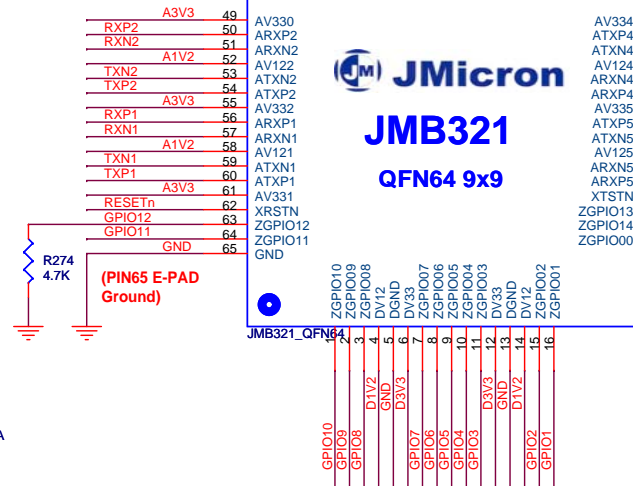
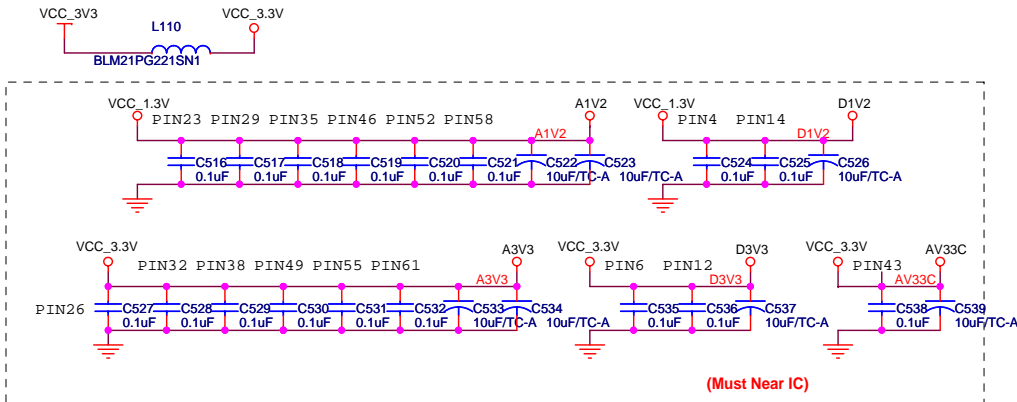
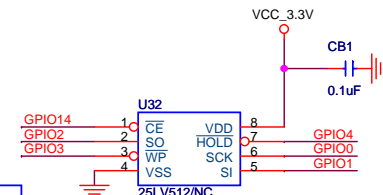
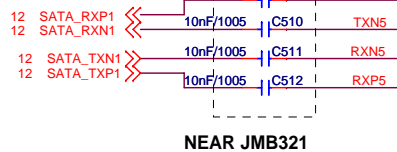
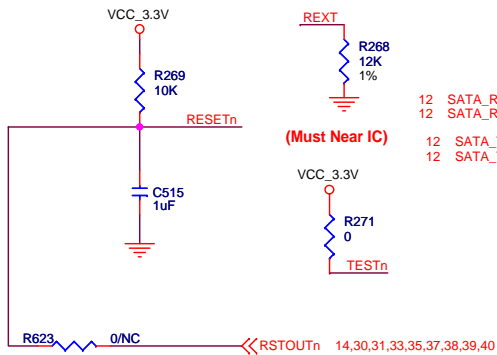
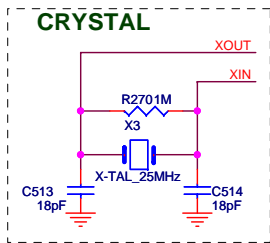
UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: USB INTERFACE CONNECTORS			
Size:B	DWG NO	<Doc>	Revision: A
Date: Wednesday, September 28, 2011	Sheet 24 of 48		



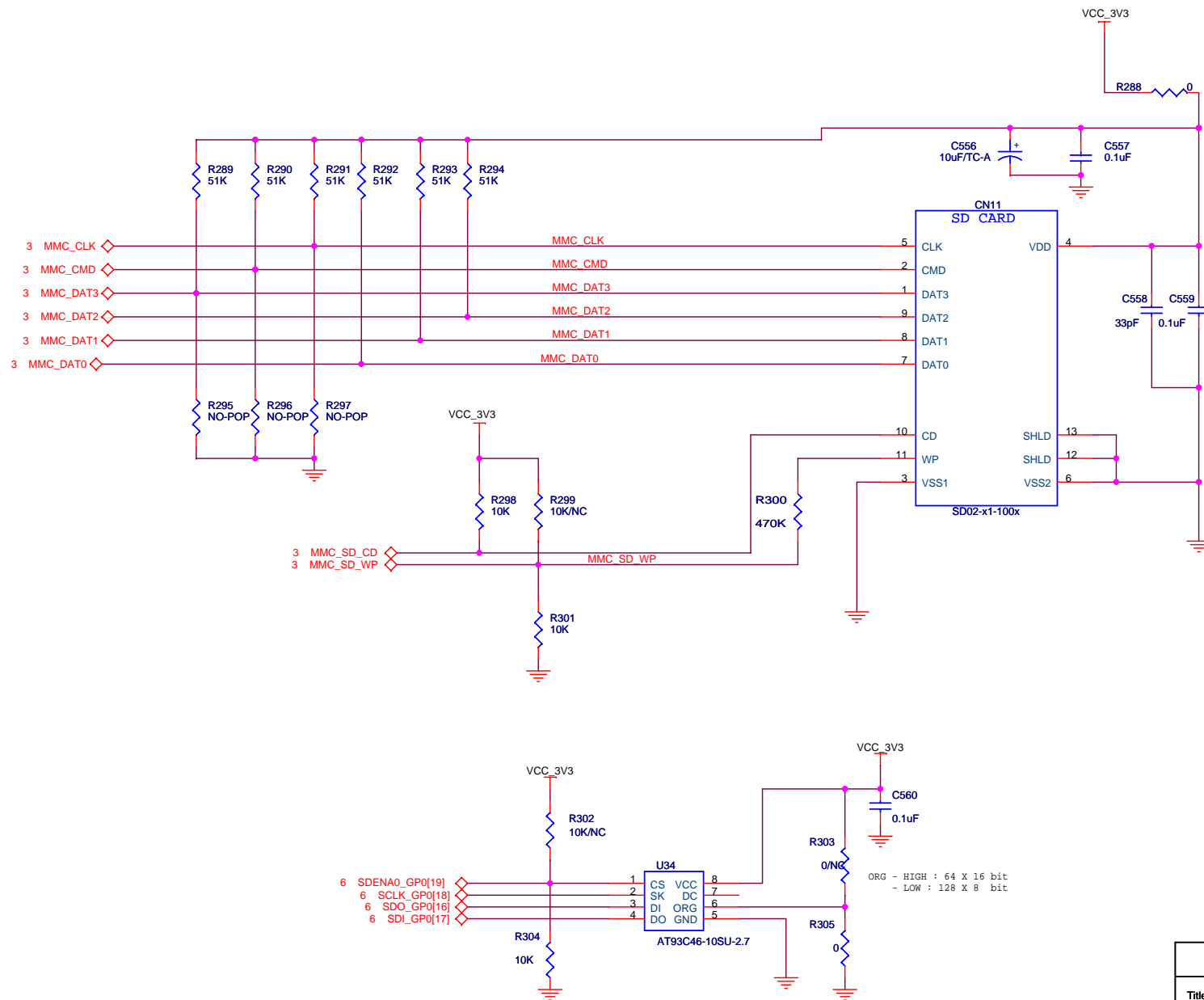
UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: SENSOR IN / ALARM OUT			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Wednesday, September 28, 2011	Sheet 25 of	48



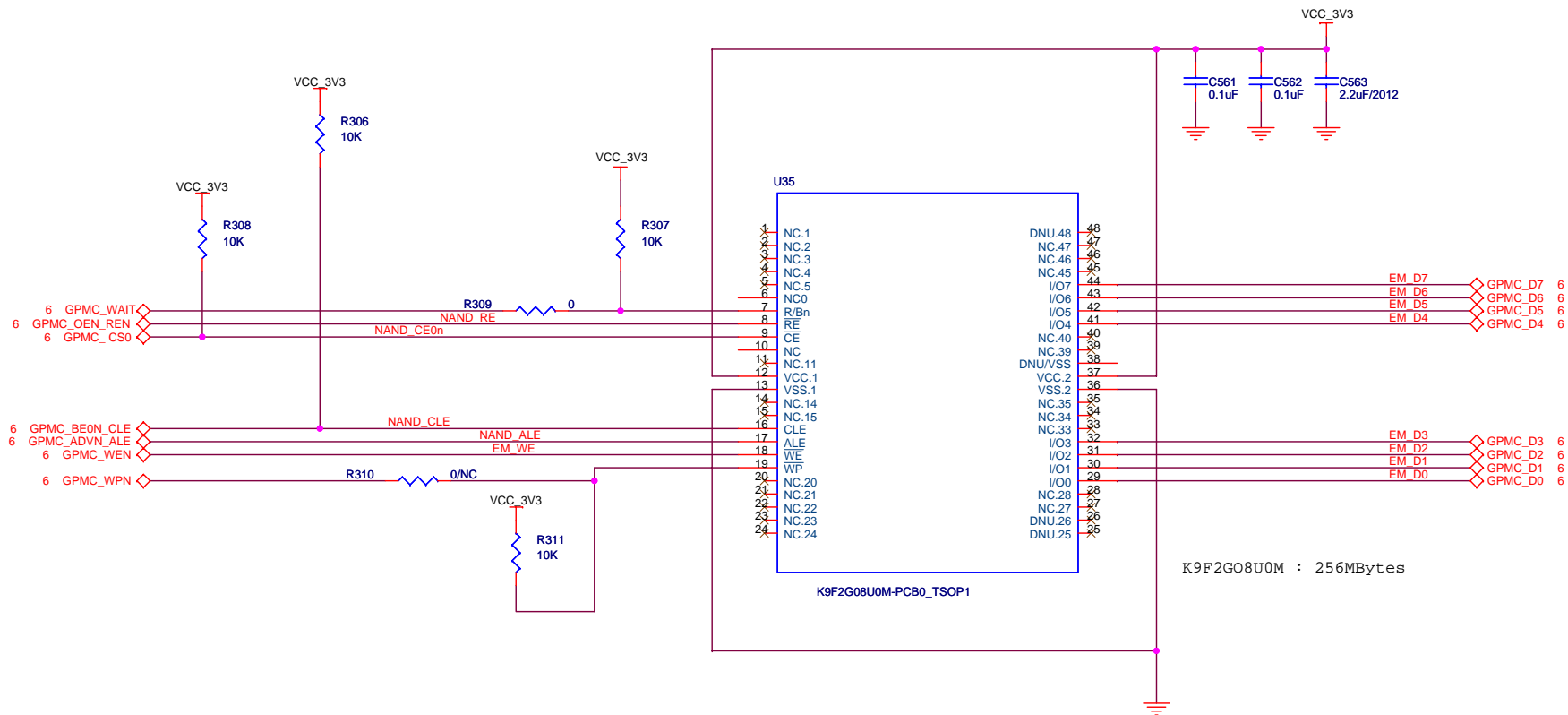
UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: RS232/RS485 INTERFACE			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Wednesday, September 28, 2011	Sheet 26 of	48



UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: SATA MULTIPLIER			
Size:B	DWG NO	<Doc>	Revision: A
Date: Wednesday, September 28, 2011	Sheet 27 of 48		

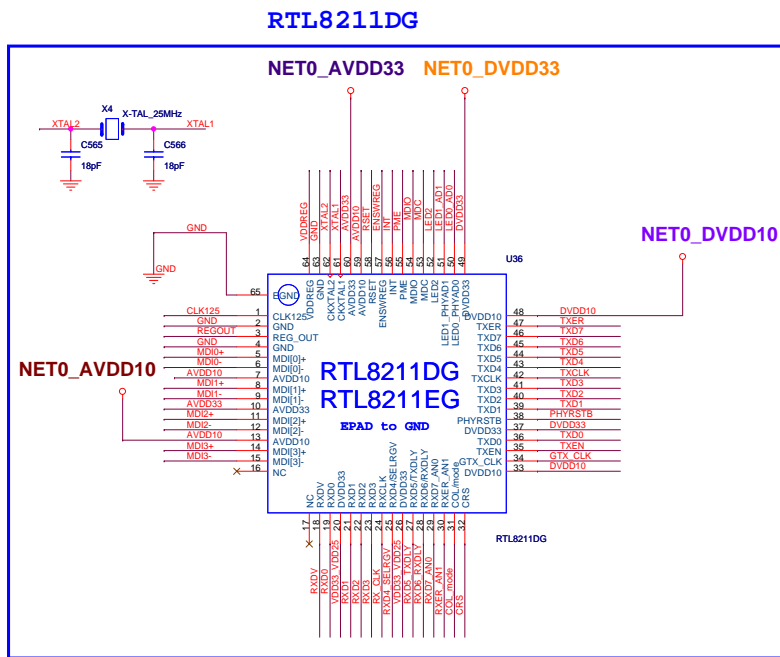


UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: SD/MMC INTERFACE/EEPROM			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Wednesday, September 28, 2011	Sheet 28 of	48



UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NAND FLASH			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Wednesday, September 28, 2011	Sheet 29 of	48

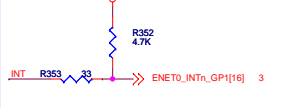
Place filter network close to RX_CLK.
Reserved for EMI



4.31 MDIO_MDIO MDIO

4.31 MDIO_MDCLK MDC

**Place filter network close to CLK125.
Reserved for EMI**



Connect ENSWREG to AVDD33 to enable Switching regulator or connect ENSWREG to GND to disable Switching regulator.

Diagram illustrating the configuration of pull-up and pull-down resistors for an 8-bit parallel bus (R335 to R342).

Top Section (Pull-up):

- Resistors R335, R336, R337, R338, R339, R340, R341, and R342 are connected to VDD3 and VDD25.
- Each resistor is labeled 4.7K.
- Text: "If use 2.5V RGMII please pull down"
- Text: "PULL UP: Config for all capability"

Bottom Section (Pull-down):

- Resistor R344 is connected to GND.
- Each resistor is labeled 4.7K.
- Text: "Pull down: GMII Interface"
- Text: "Pull up : RGMII Interface"

NETO_VDD33

10/100/1000 + Active

LED2

R313 0NC

C567 100pF/NC

R317 4.7K/NC

R326 510

R327 4.7K

LED0 AD9

Active

R642 4.7K/NC

R325 0

C568 100pF/NC

PHYAD0 = 0

LED : HIGH Active

GMII0_ACT_LED 32.41

C Reserve for EMI, close to LAN connector

LED1 AD1

10/100/1000

C569 100pF/NC

R332 510

R333 4.7K

PHYAD1 = 0

LED : High Active

GMII0_SPD_LED 32

VCC_3V3

NET0_DVDD33

VDD33 VDD25

NET0_AVDD33

L35

BLM18PQ221SN1D

C574 0.1uF

C570 0.1uF

C571 0.1uF

C572 0.1uF

C573 0.1uF

C577 0.1uF

C575 0.1uF

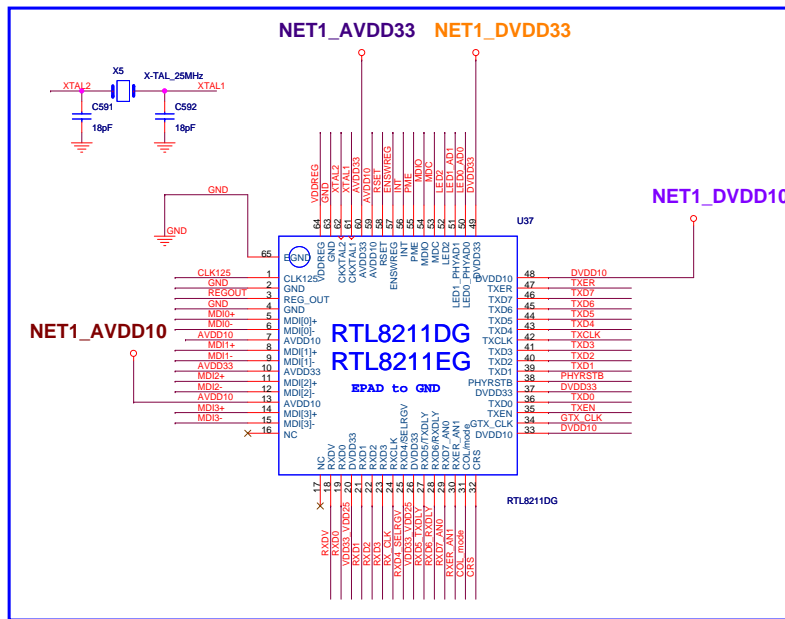
C576 0.1uF

C938 0.1uF

NET0_DVDD10

UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: ETHERNET INTERFACE PORT0			
Size:C	DWG NO <Doc>		Revision: A
Date:	Wednesday, September 28, 2011	Sheet 30 of	48

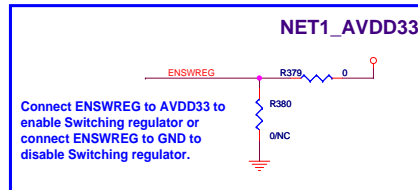
Place filter network close to RX_CLK.
Reserved for EMI



4.30 MDIO_MDIO MDIO

4.30 MDIO_MDCLK MDC

**Place filter network close to CLK125.
Reserved for EMI**



NET1_DVDD33

PHYRSTB

R392 4.7K

C614 0.01uF

R393 0/NC PCIRST RSTOUTn 14, 27, 30, 33, 35, 37, 38, 39, 4

NET1_DVDD33

R394 4.7K

R395

33

INT ENET1_INTn_GP1[17] 3

The diagram illustrates the pull-up and pull-down configurations for an RGMII interface. It shows three signal lines: **RXD4 SELRGV**, **RXD7 AN0 RXER AN1**, and **COL_mode**.

- RXD4 SELRGV:** A pull-up resistor **R377** (4.7KNC) is connected to **VDD4 VDDG5**. A dashed box labeled **R378** (4.7K) indicates a pull-down configuration.
- RXD7 AN0 RXER AN1:** Pull-up resistors **R381** (4.7K) and **R385** (4.7KNC) are connected to **VDD4 VDDG5**. Pull-down resistors **R382** (4.7KNC) and **R384** (4.7K) are connected to **GND**. A dashed box labeled **R383** (4.7K) indicates a pull-down configuration.
- COL_mode:** A pull-down resistor **R386** (4.7K) is connected to **GND**. A pull-up resistor **R387** (4.7KNC) is connected to **VDD4 VDDG5**.

Legend:

- Pull down:** GMII Interface
- Pull up:** RGMII Interface

the trace length from 22uF,0.1uF to pin64 must be within 0.5cm

[illegible]

VCC_3V3

C600 0.1uF

C596 0.1uF

C597 0.1uF

C598 0.1uF

C599 0.1uF

L39 BLM18PG22N1S1D

C603 0.1uF

C601 0.1uF

C602 0.1uF

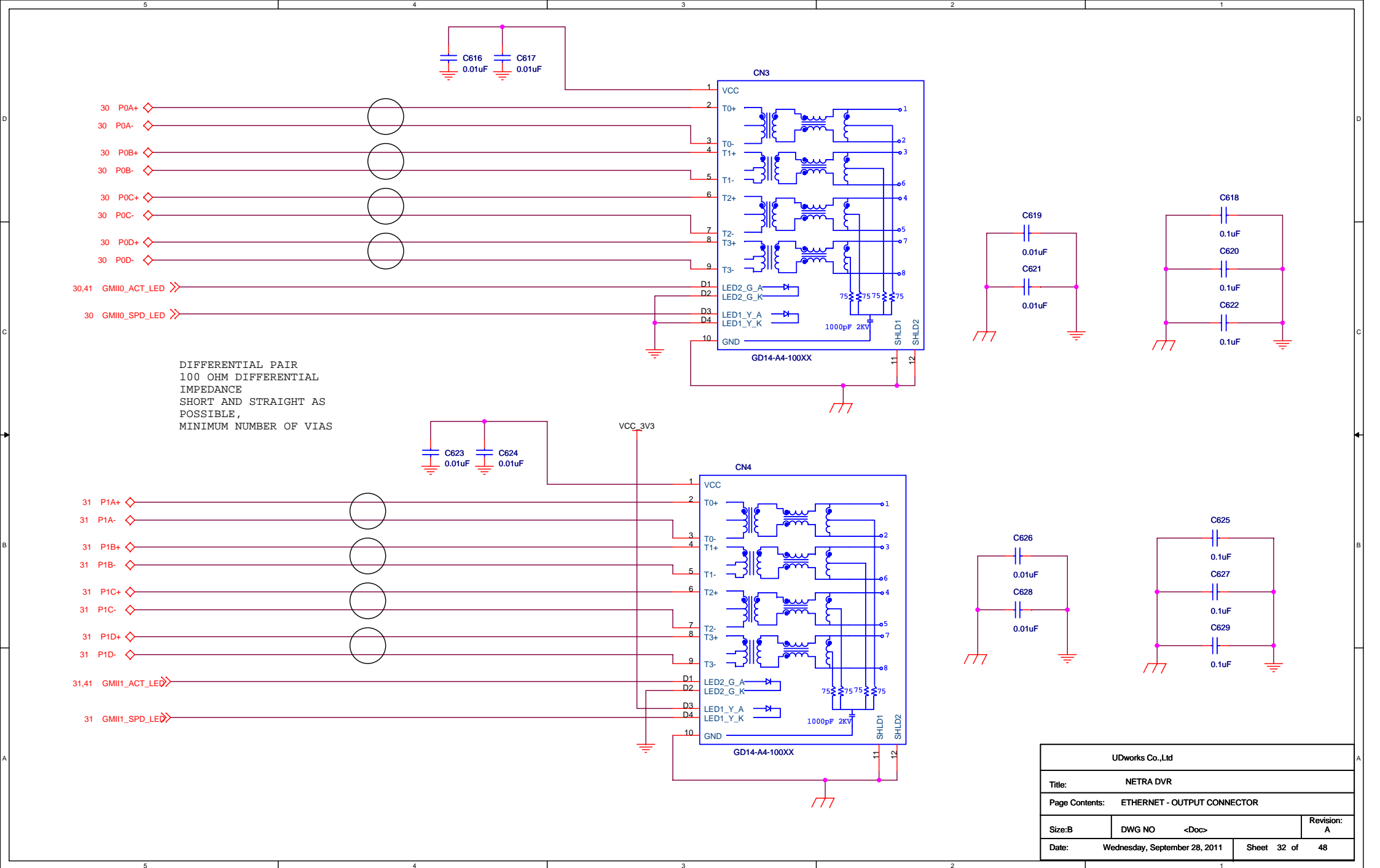
NET1_AVD033

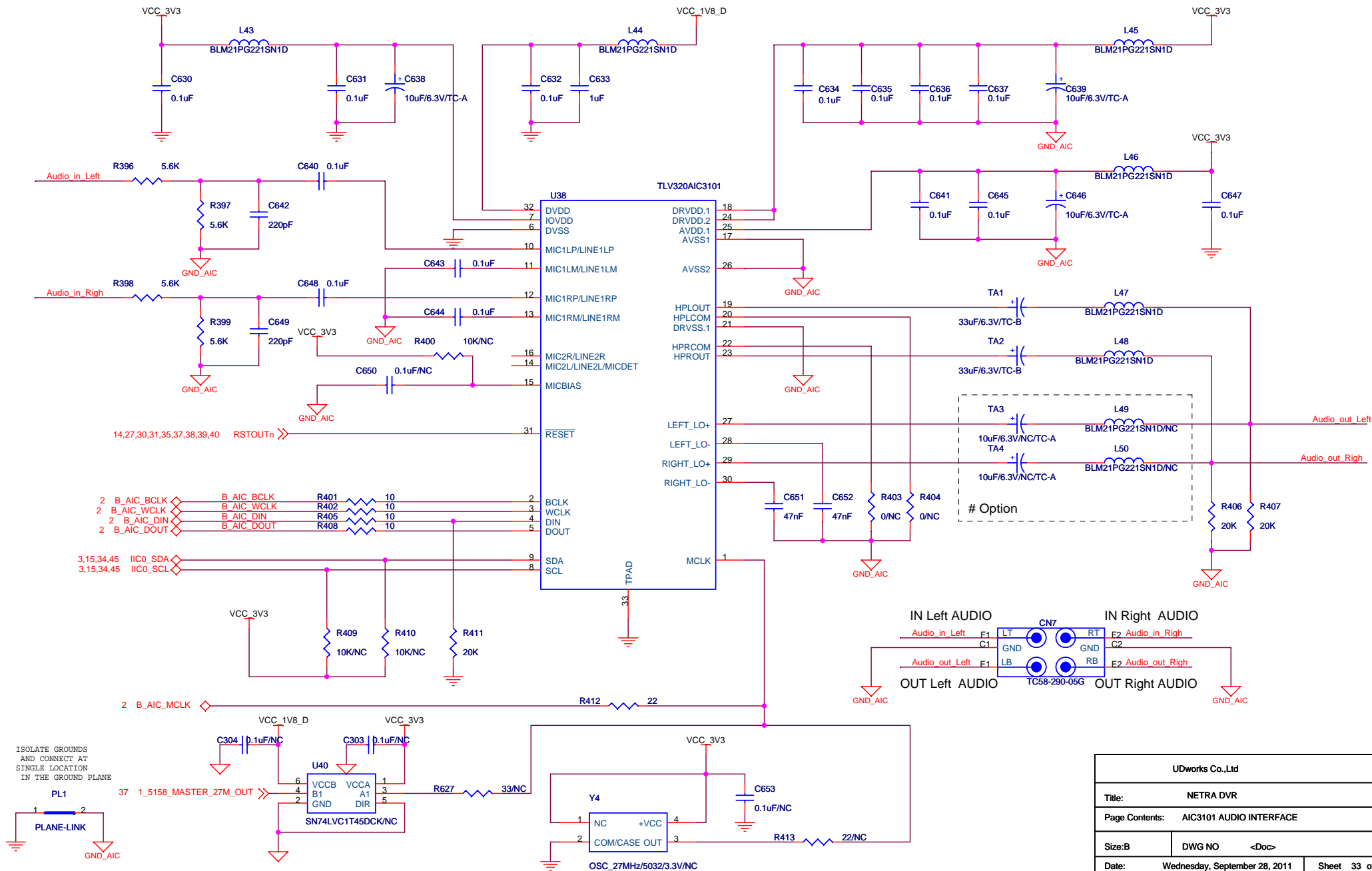
VDD033 VDD025

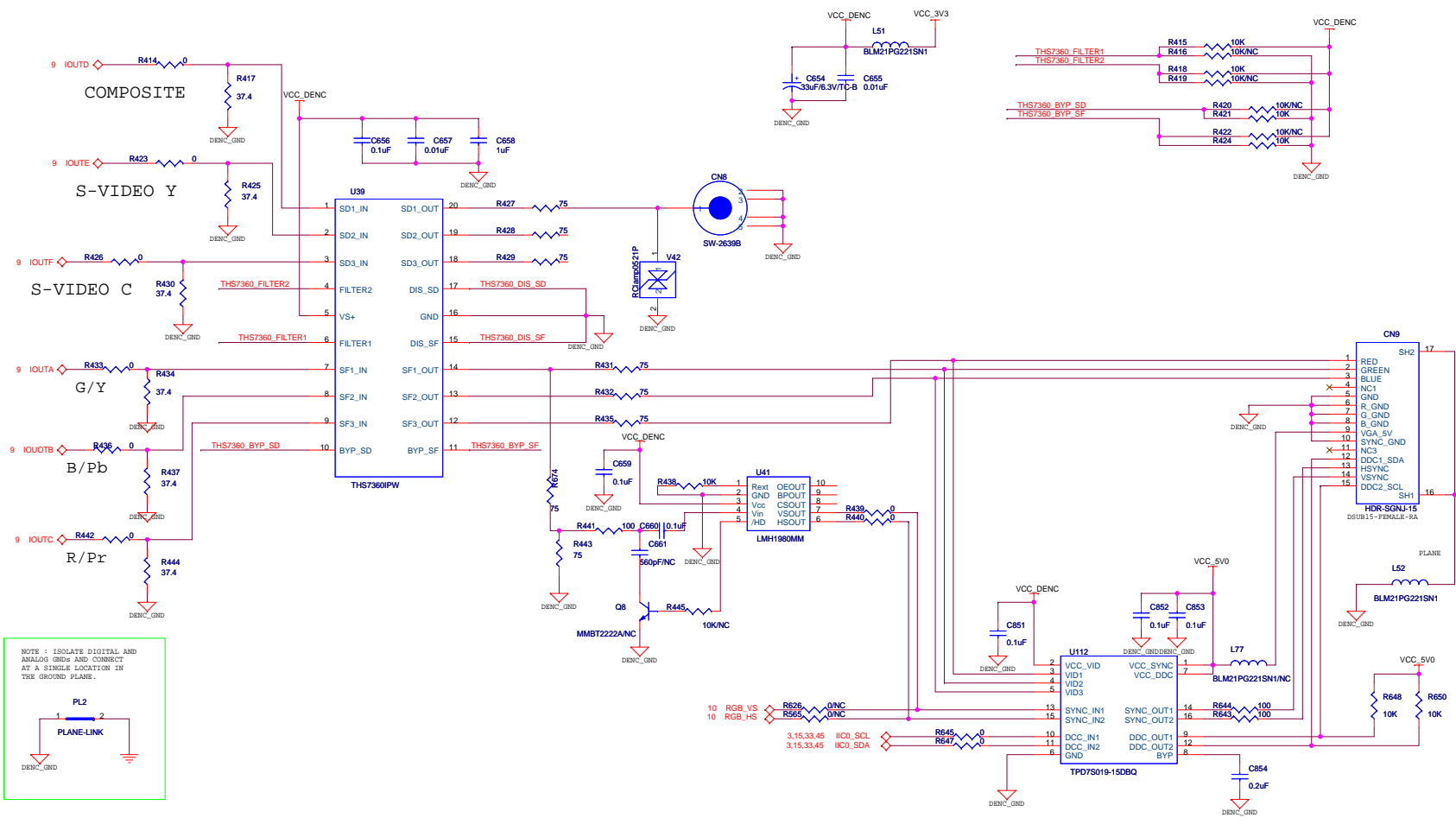
C940 0.1uF

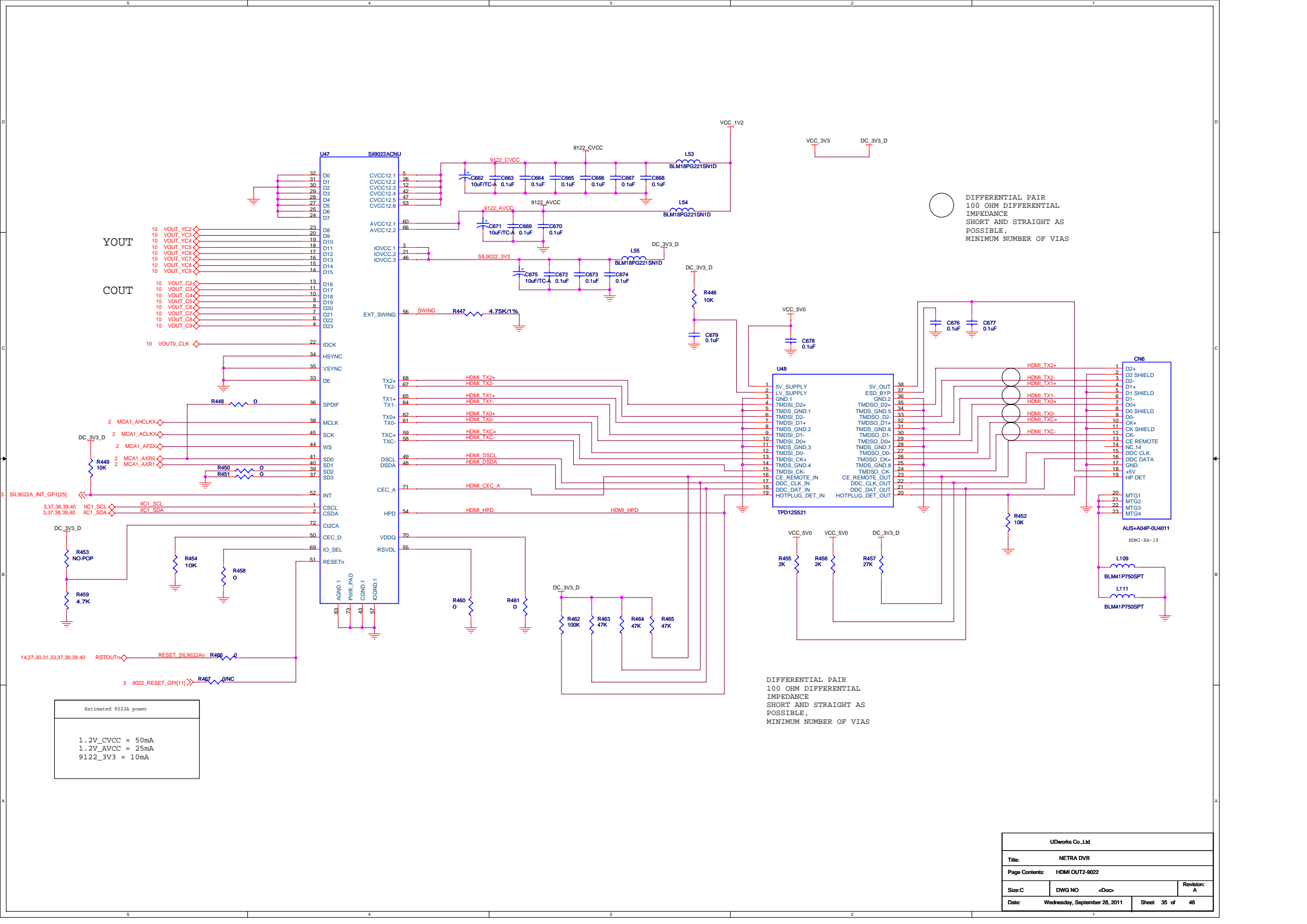
C939 0.1uF

UDworks Co.,Ltd		
Title: NETRA DVR		
Page Contents: ETHERNET INTERFACE PORT1		
Size:C	DWG NO <Doc>	Revision: A
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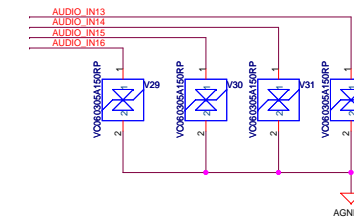
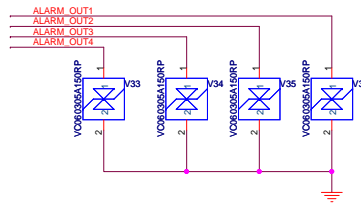
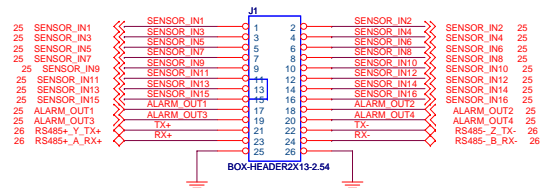
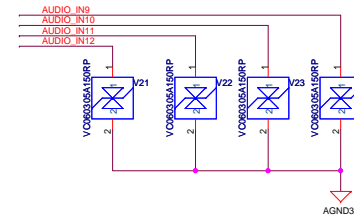
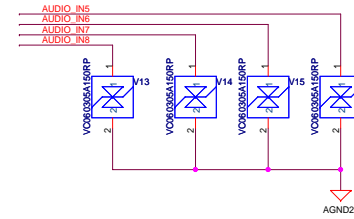
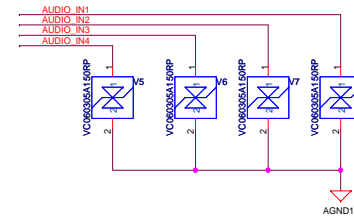
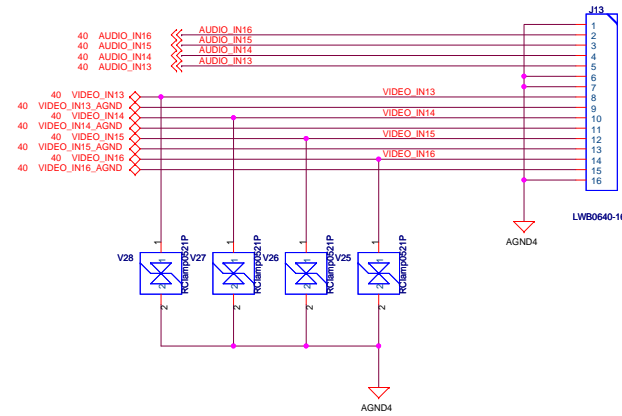
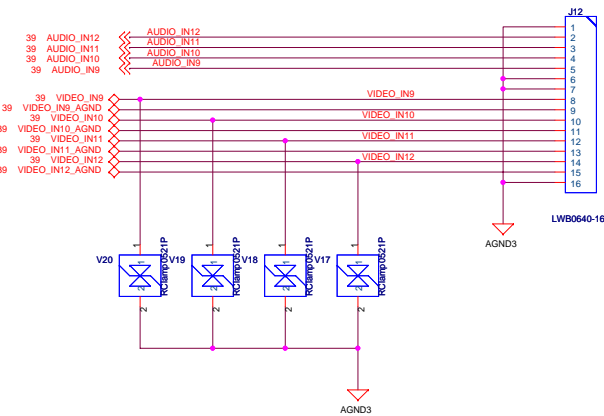
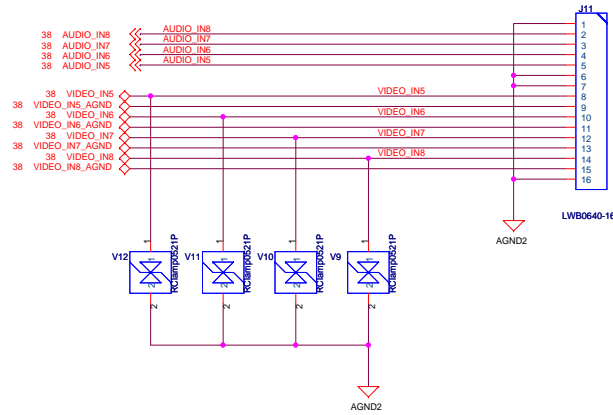
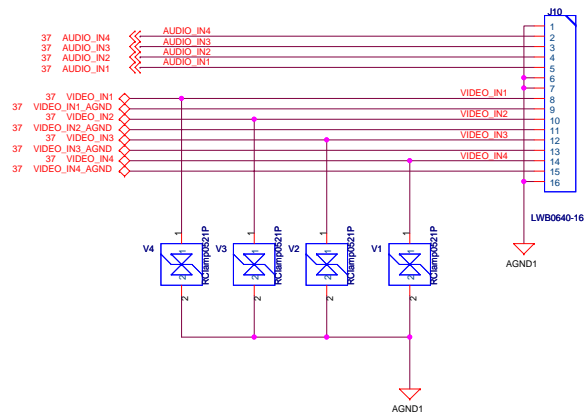


DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

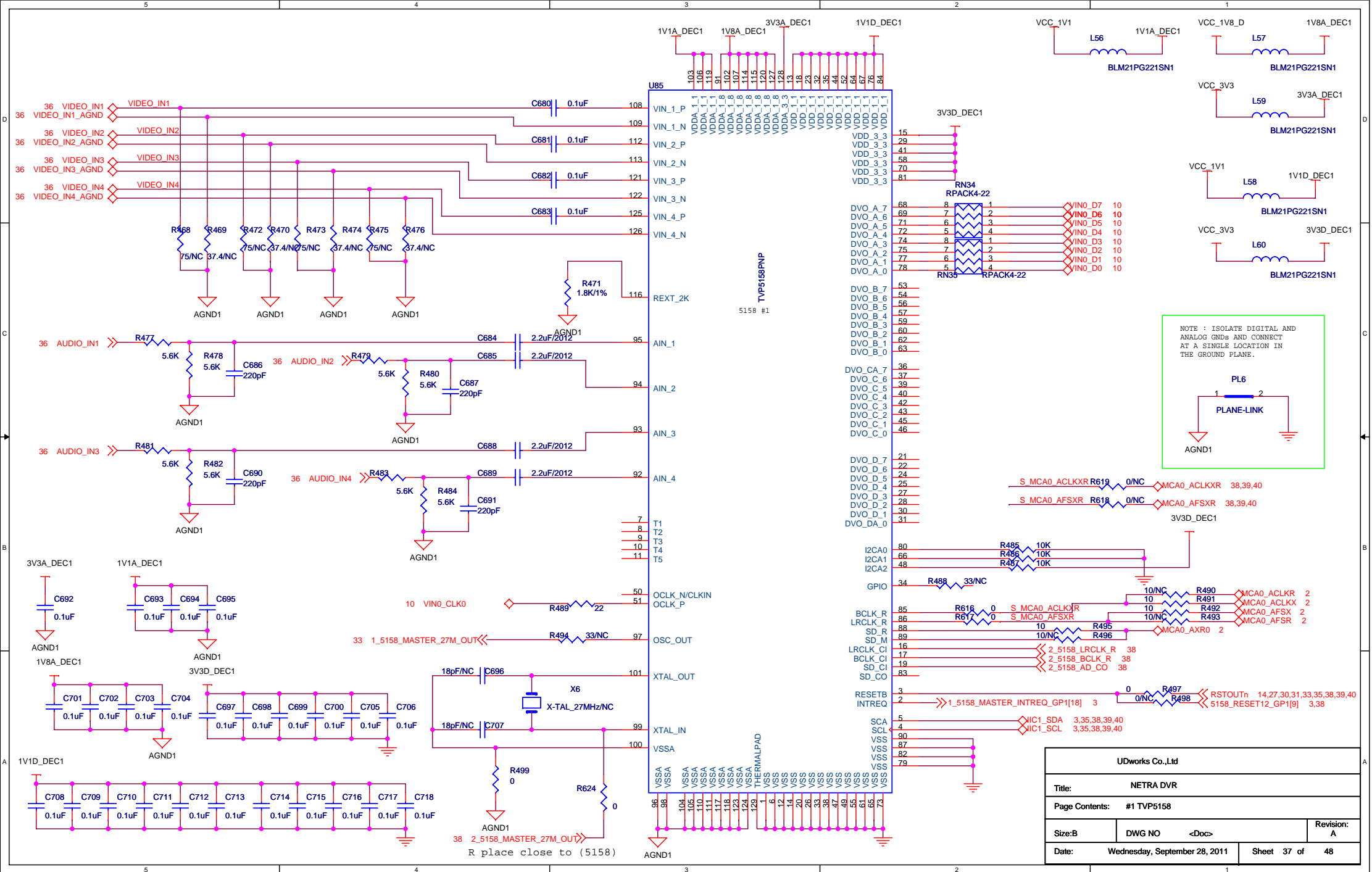
DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

Estimated 9022A power
1.2V_CVCC = 50mA
1.2V_AVCC = 25mA
9122_3V3 = 10mA

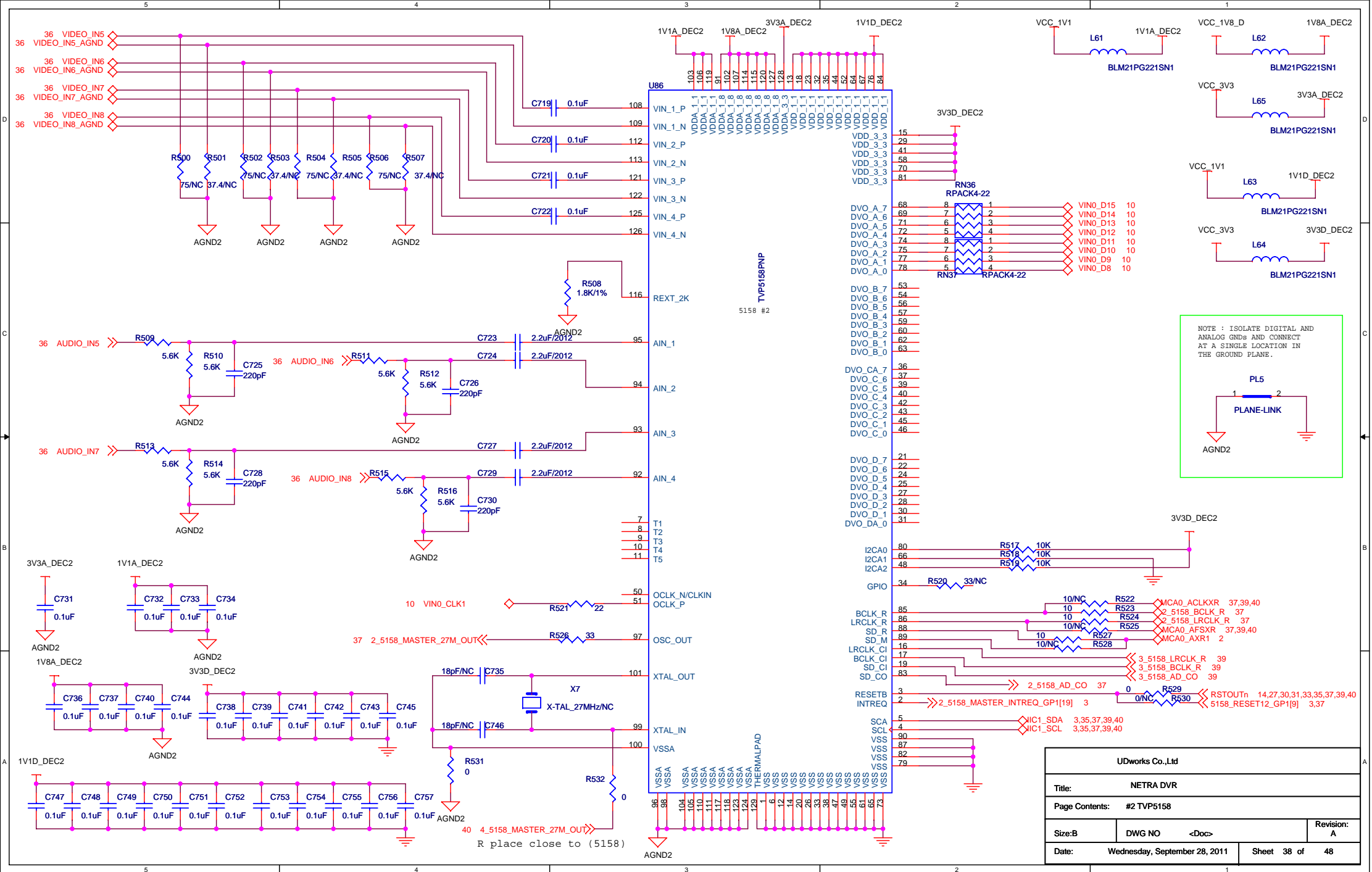
UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: HDMI OUT2-9022			
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UDworks Co., Ltd			
Title: NETRA DVR			
Page Contents: REAR BOARD IF			
Size: C	DWG NO	<Doc>	Revision: A
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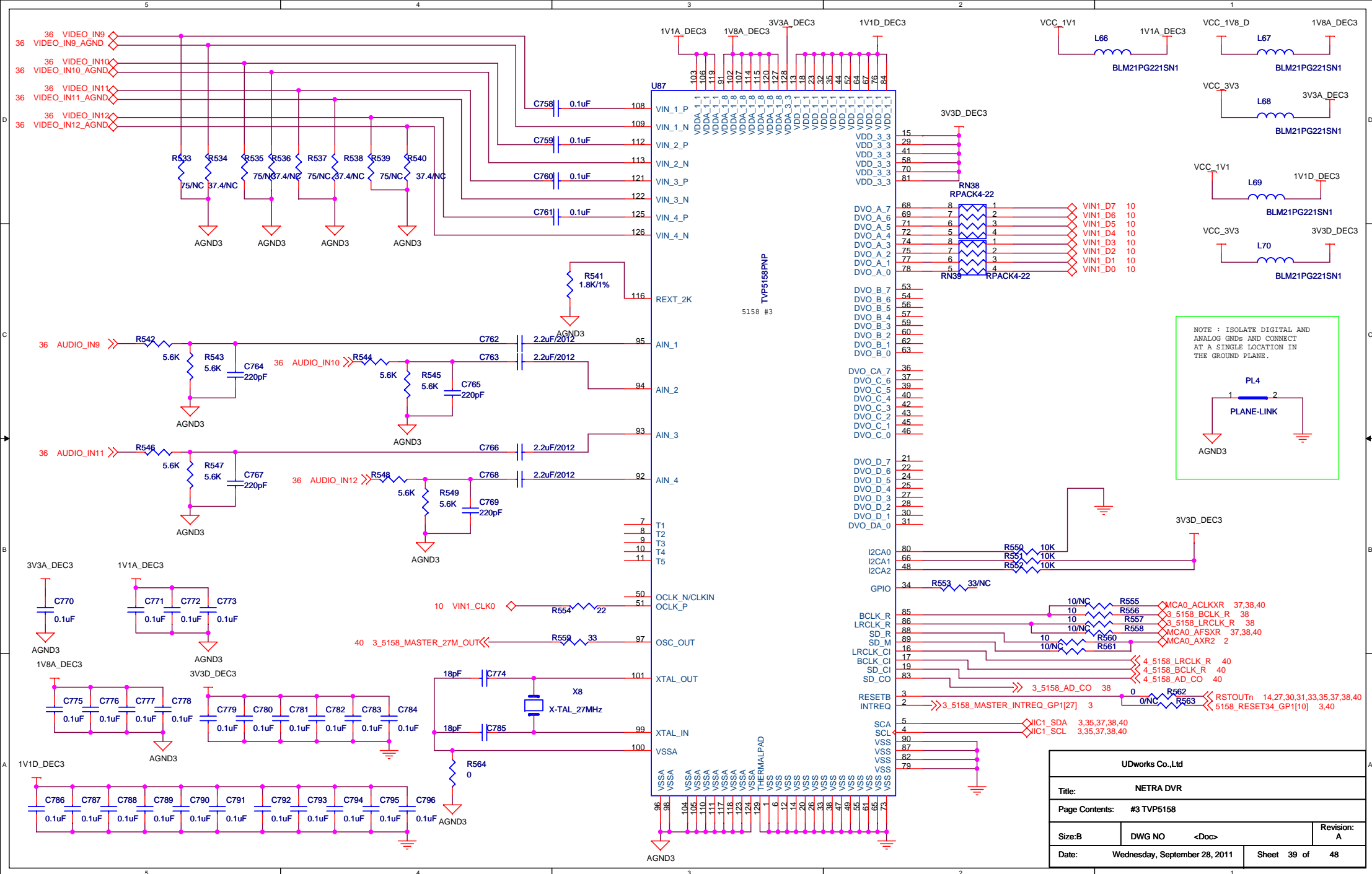


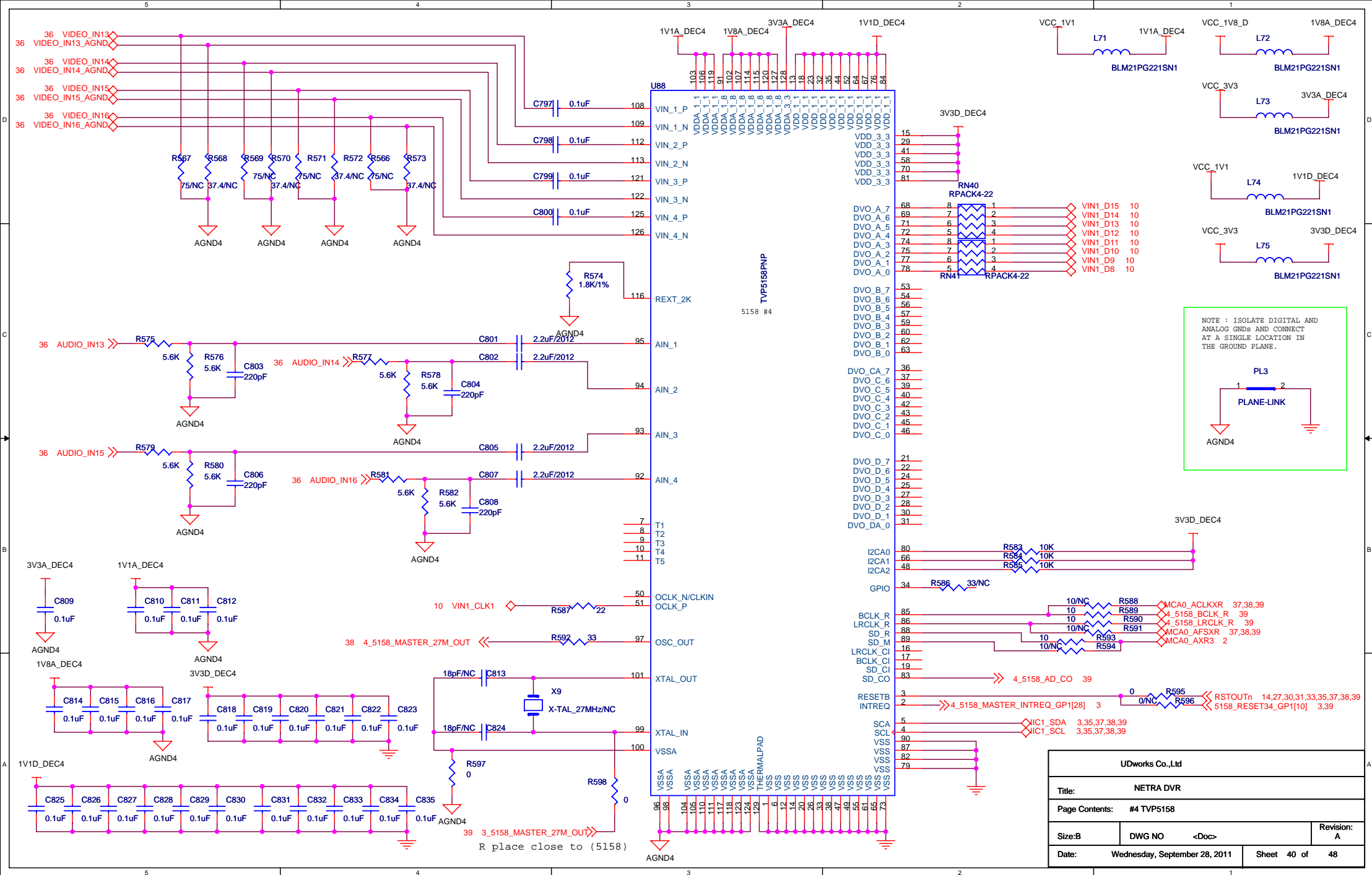
UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: #1 TVP5158			
Size: B	DWG NO	<Doc>	Revision: A
Date: Wednesday, September 28, 2011	Sheet 37 of 48		



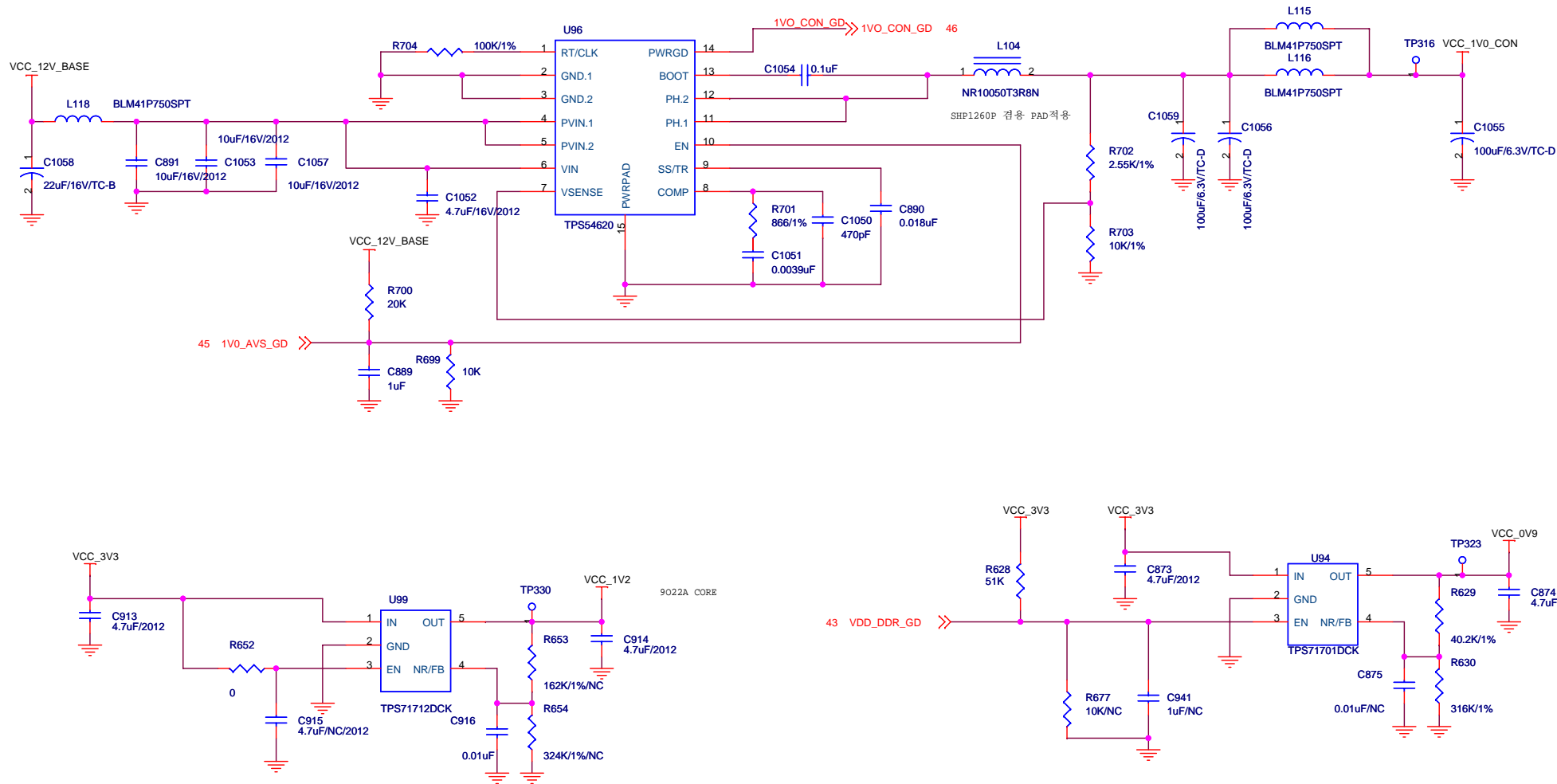
NOTE : ISOLATE DIGITAL AND ANALOG GNDs AND CONNECT AT A SINGLE LOCATION IN THE GROUND PLANE.

UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: #2 TYP5158			
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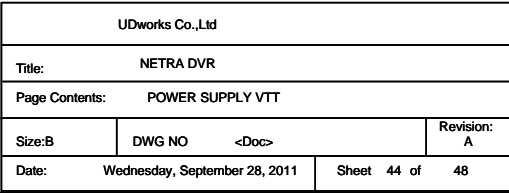


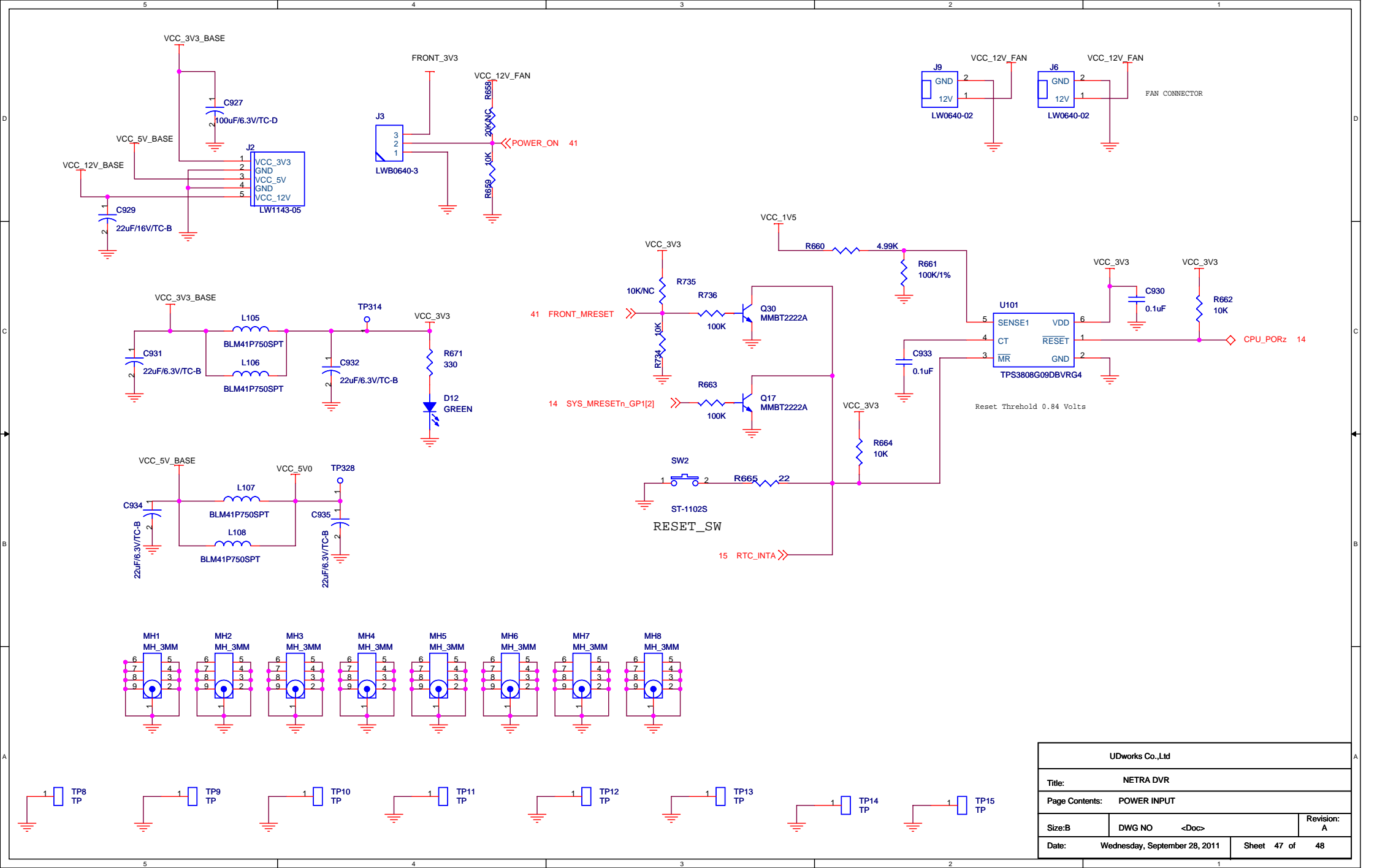


UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: #4 TYP5158			
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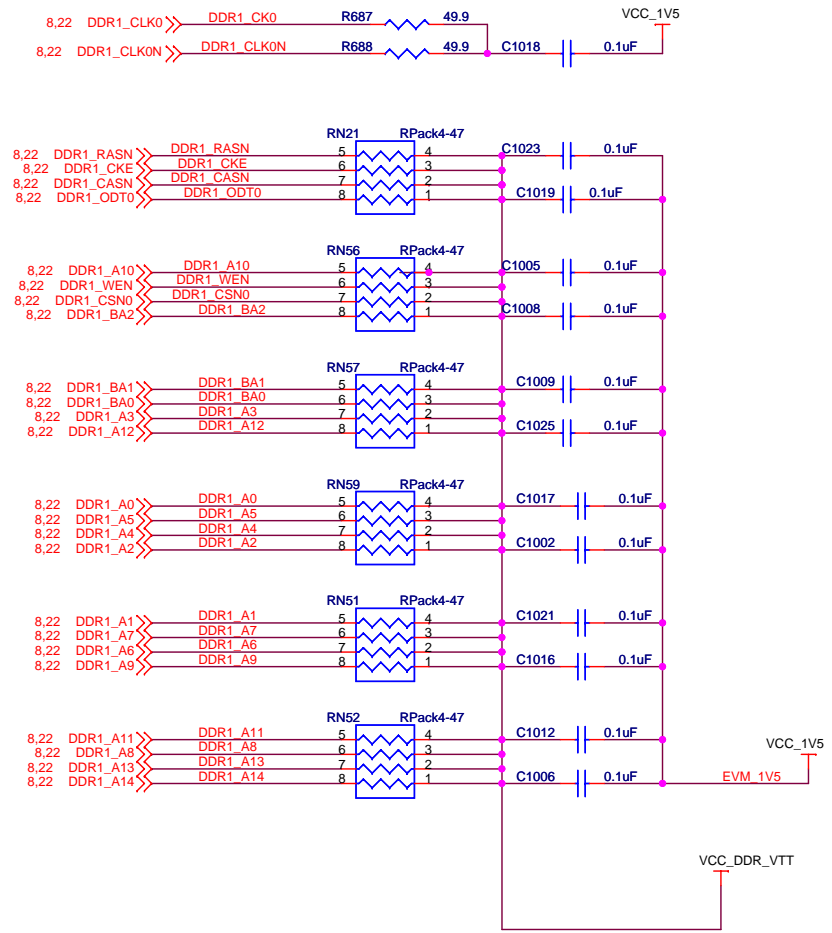
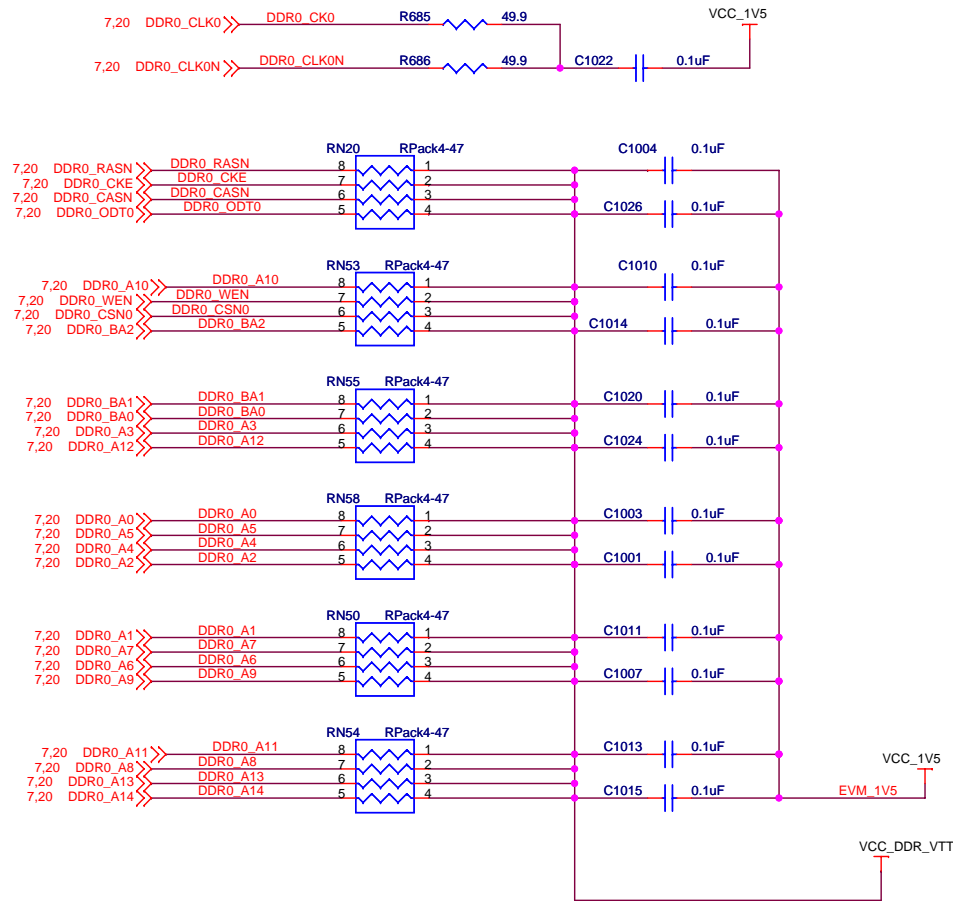


UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: POWER SUPPLY III			
Size:B	DWG NO	<Doc>	Revision: A
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UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: POWER INPUT			
Size:B	DWG NO	<Doc>	Revision: A
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UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: EMIF DDR0/1 DDR3 MEM			
Size:B	DWG NO	<Doc>	Revision: A
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