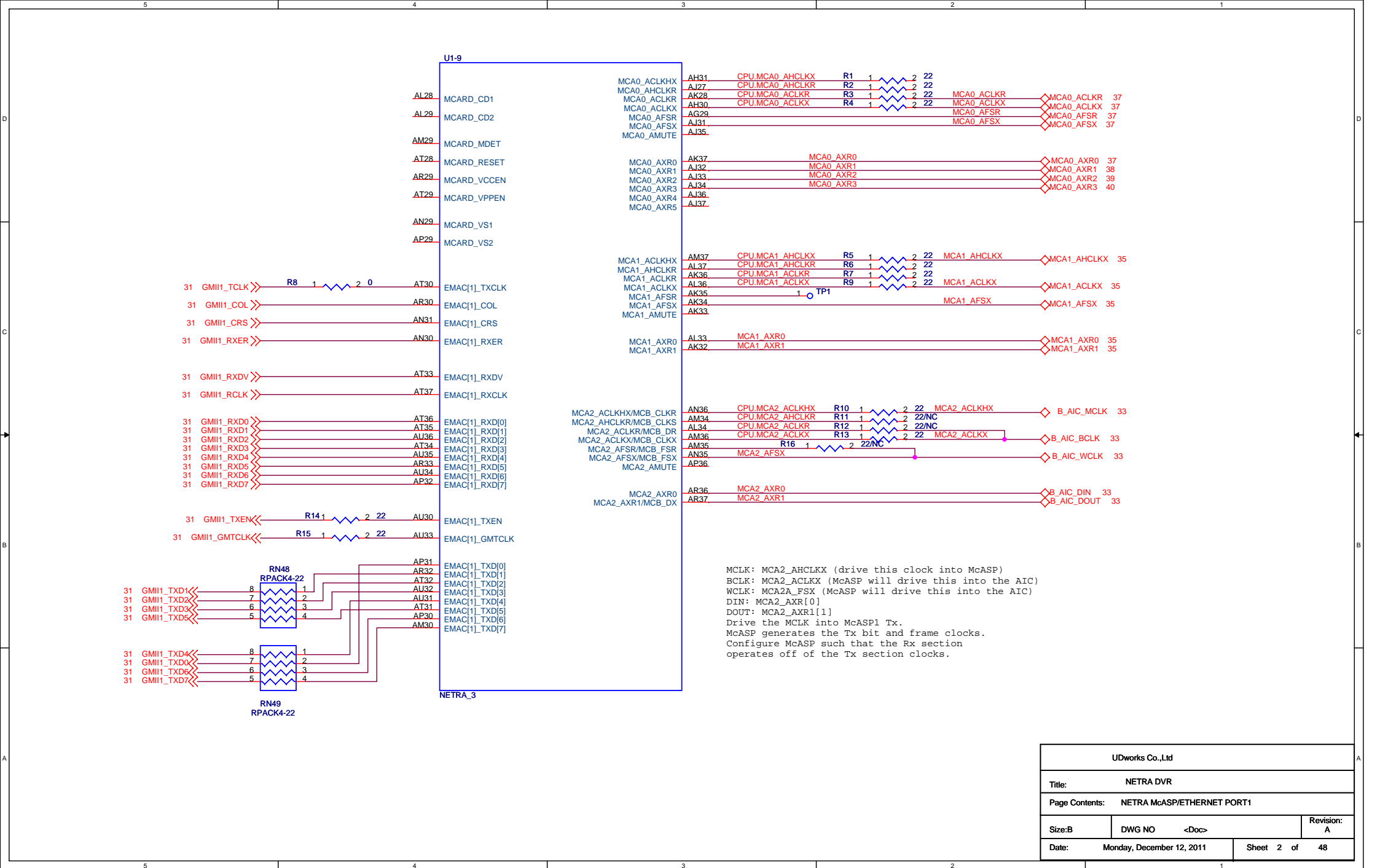
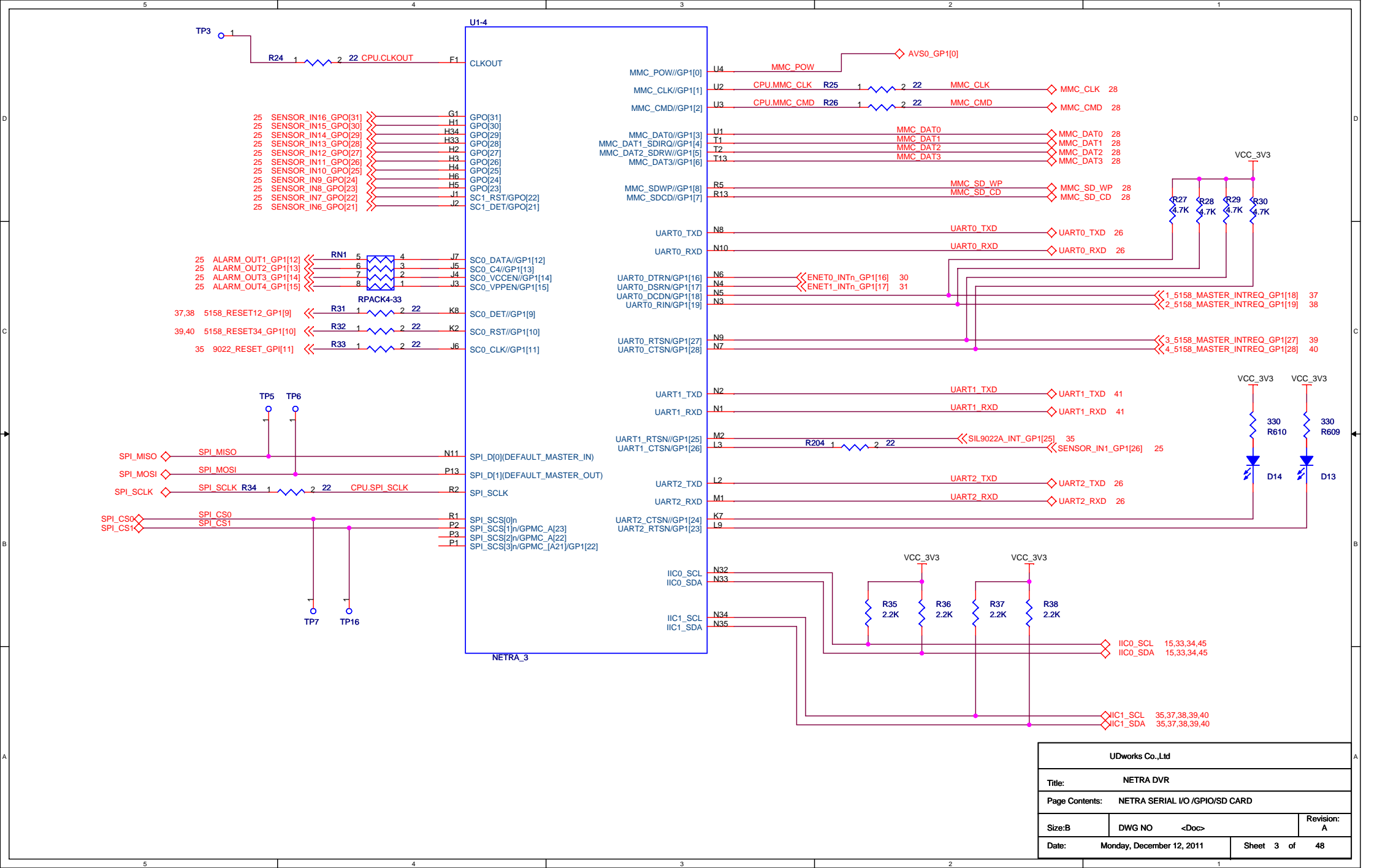


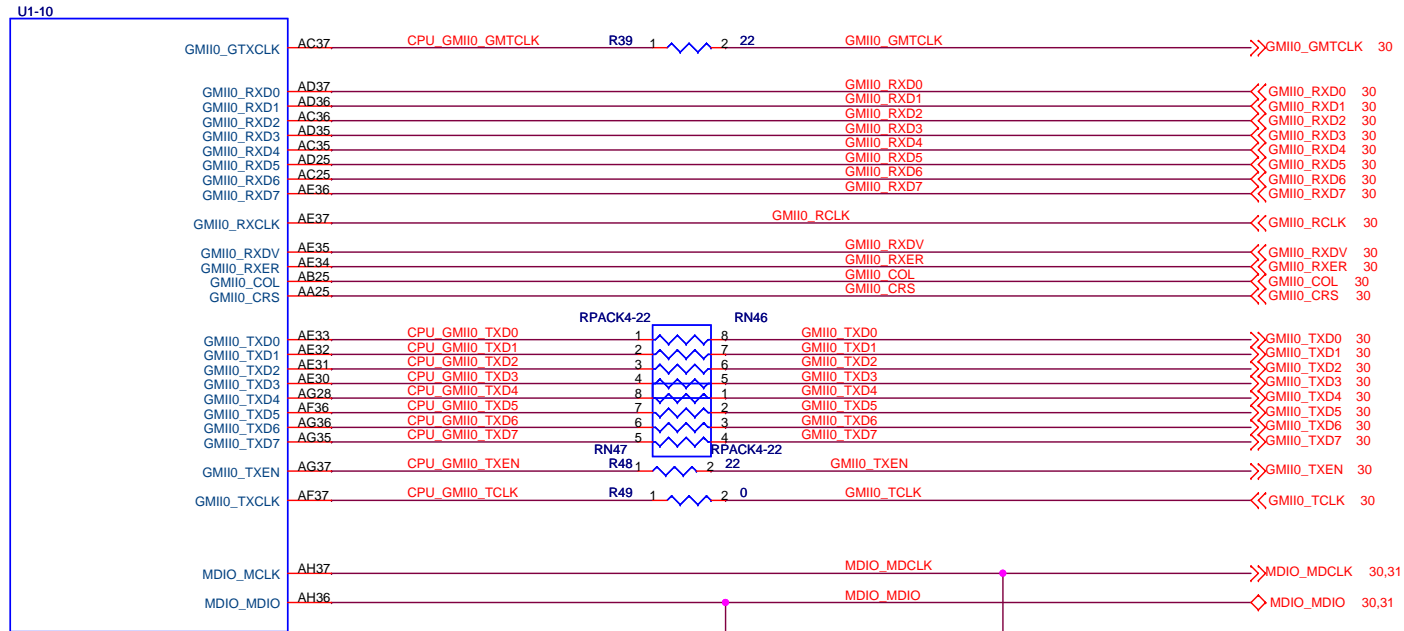
5					4					3					2					1									
Netra DVR RD																													
REV										DESCRIPTION										DATE					APPROVED				
A										Initial schematic for layout										07/12/2010					SDS				
rev0.2										change DDR2 to DDR3										12/02/2010					SDS				
rev0.3										change Q19, Q20(FDS8817) to FDS8812										01/25/2011					SDS				
rev0.3A										1. Modify SATA port LED GPIO numbers 2. Modify the Video Sync separator input circuit on the VGA output port. 3. Modify filter setting on the Video Amp(THS7360) 4. Change power devices (1V0_CON) 5. Change 5158 AUDIO IF MODE to cascade mode (McASP interface). 6. Change the Ethernet PHY initial Mode (Auto-negotiation enable) to the 100Mbit mode for GIGABIT mode issue. 7. Change the Capacitor value 22uF to 47uF (or add 22uF) on the Ethernet PHY's internal power. 8. Add reset signal on the AIC3101 audio Codec.										05/13/2011					SDS				
rev0.4										1. Change power devices (1V0_AVS, VCC_1.8V, VCC_1.1V, VCC_1.3V)										05/23/2011					SDS				
rev0.5										1. Modify VTT power enable signal. 2. Modify sync signals of the RGB(VGA) output for The PG2.0 netra. 3. Modify AC coupled capacitor value in the SATA port. 4. Change the ESD device in the USB port. 5. Change the TPS40400 PMBus address "00" to "70" (R706 : 10K -> 200K)										09/23/2011					SDS				
rev0.5A										1. eSATA port is changed to the JMB321's port1. Netra SATA port0 is connected to the SATA port (J15) for the ODD										09/26/2011					SDS				
rev0.5B										1. Add the signal for 1V0_con power enable. 2. Change value of components for the AVS power device										12/12/2011					SDS				
DWN										DATE										07/13/2010					SDS				
CHK										DATE																			
ENGR										DATE																			
ENGR-MGR										DATE																			
QA										DATE																			
MFG										DATE																			
NEXT ASSY										USED ON																			
APPLICATION										DATE																			
5					4					3					2					1									

UDworks Co.,Ltd									
Title: NETRA DVR									
Page Contents: TITLE PAGE									
Size:B		DWG NO <Doc>					Revision: rev0.5B		
Date: Monday, December 12, 2011		Sheet 1 of 48							



UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA McASP/ETHERNET PORT1			
Size: B	DWG NO	<Doc>	Revision: A
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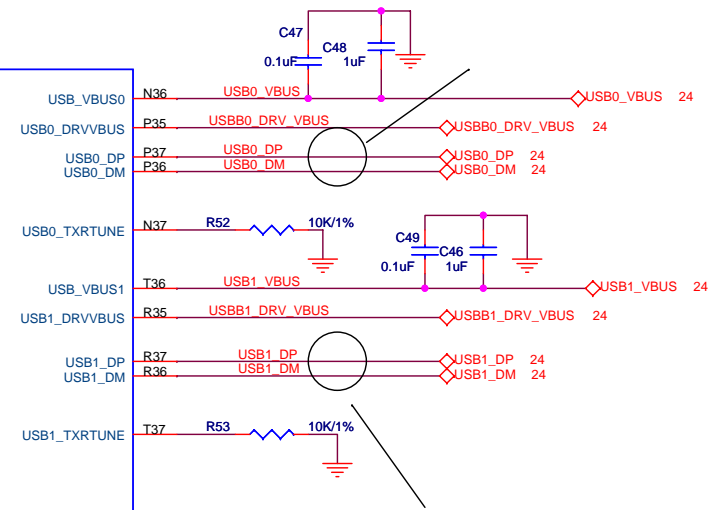
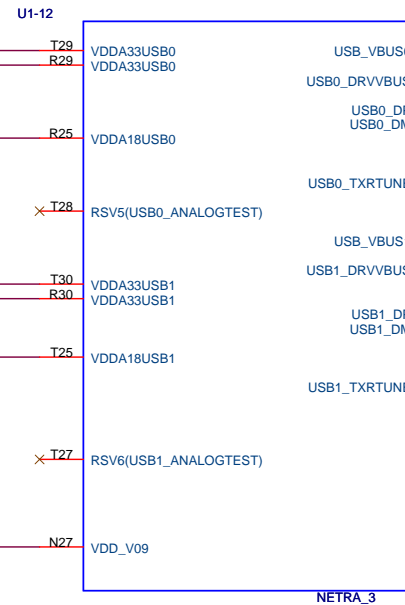
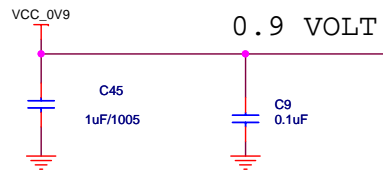
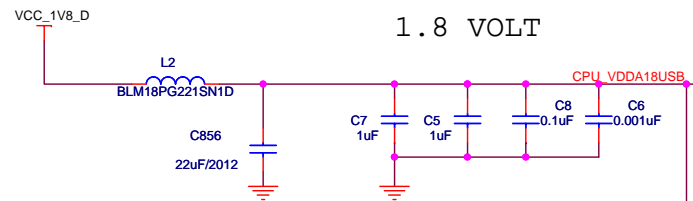
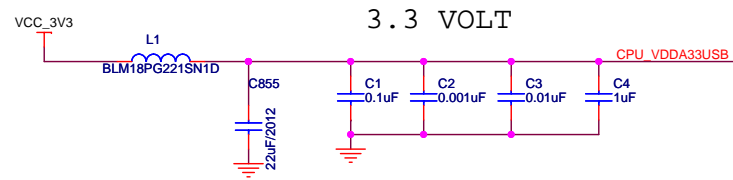




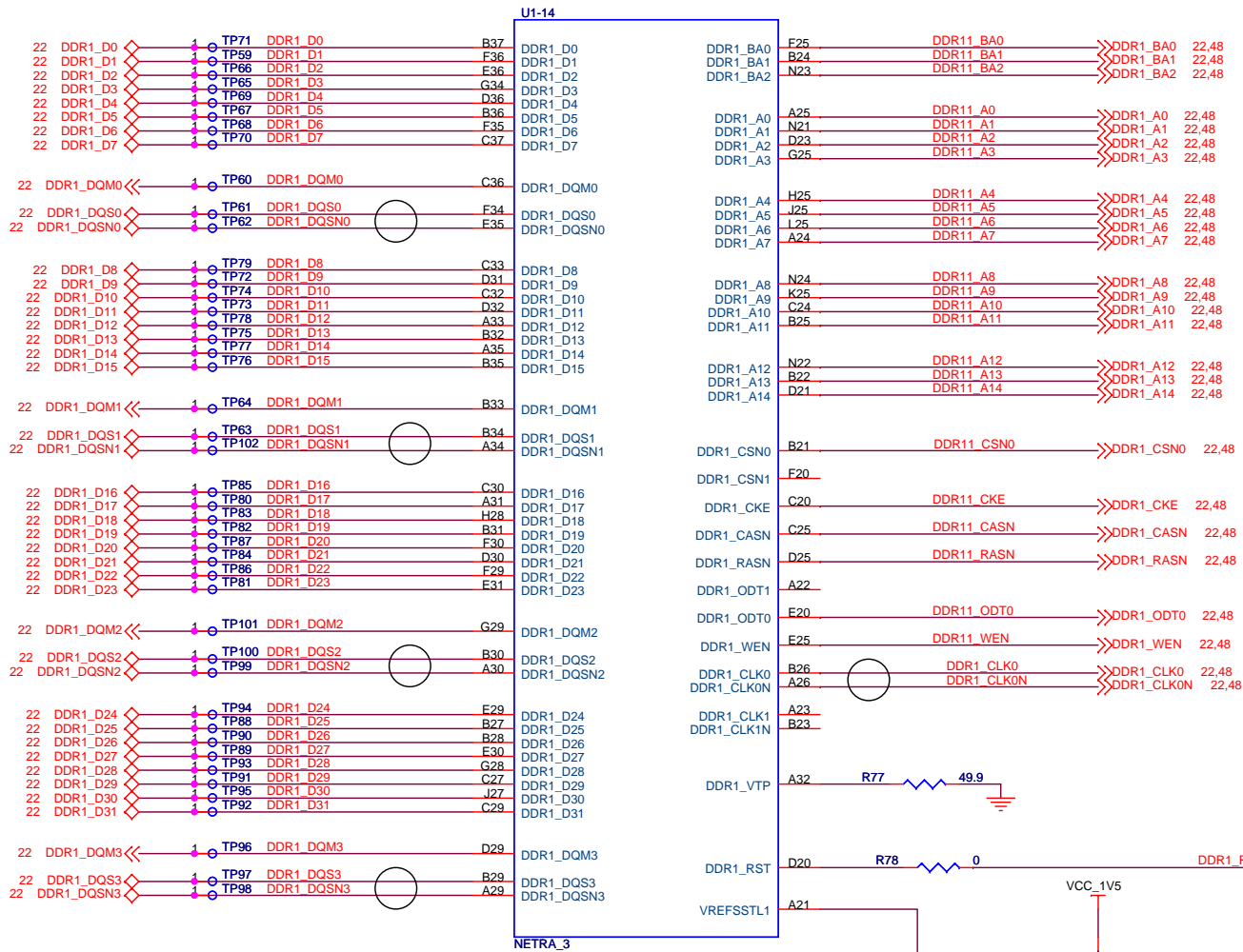
NETRA_3



UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA ETHERNET PORT0			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Monday, December 12, 2011		Sheet 4 of 48

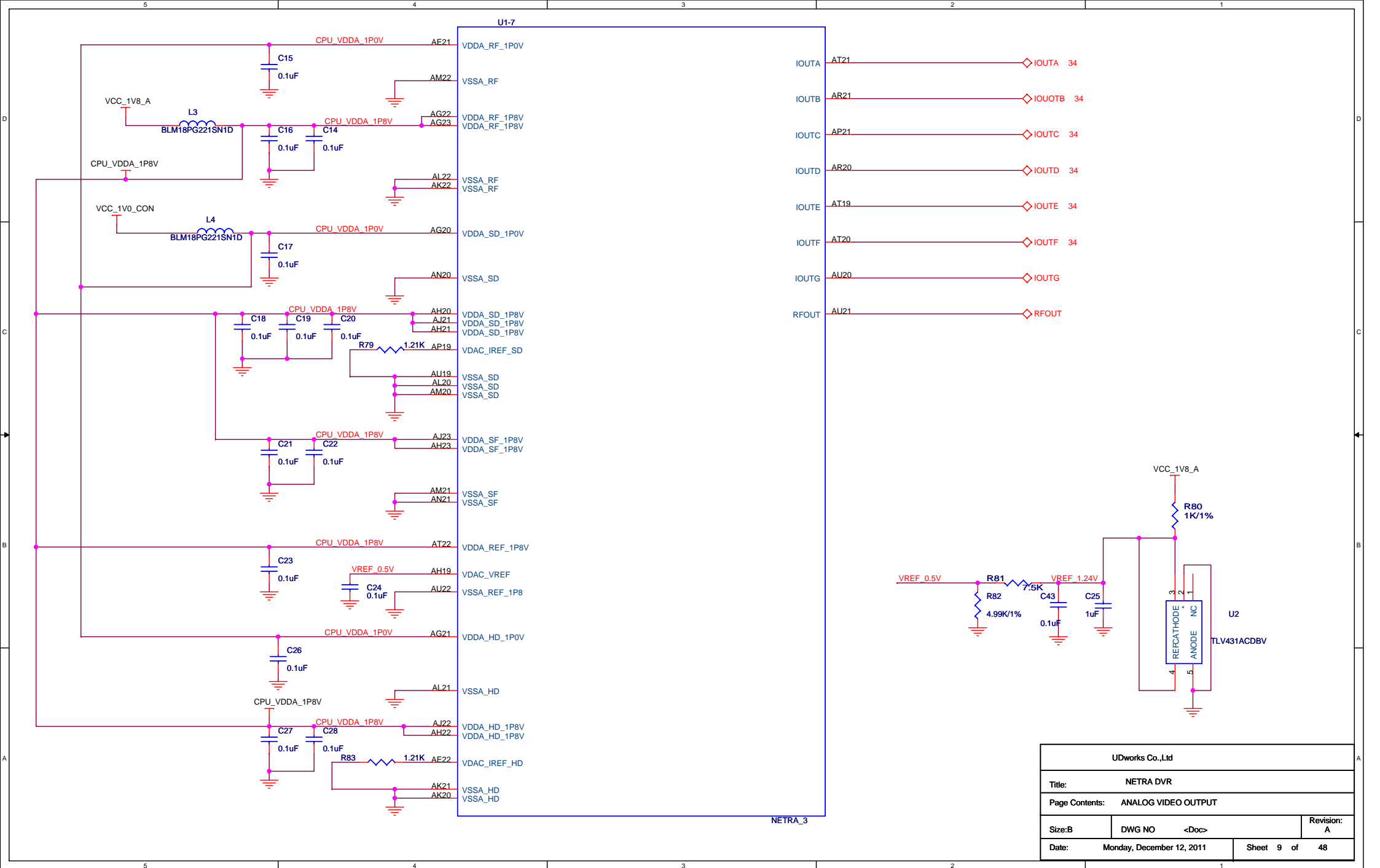


UDworks Co.,Ltd			
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Page Contents: NETRA USB			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Monday, December 12, 2011		Sheet 5 of 48

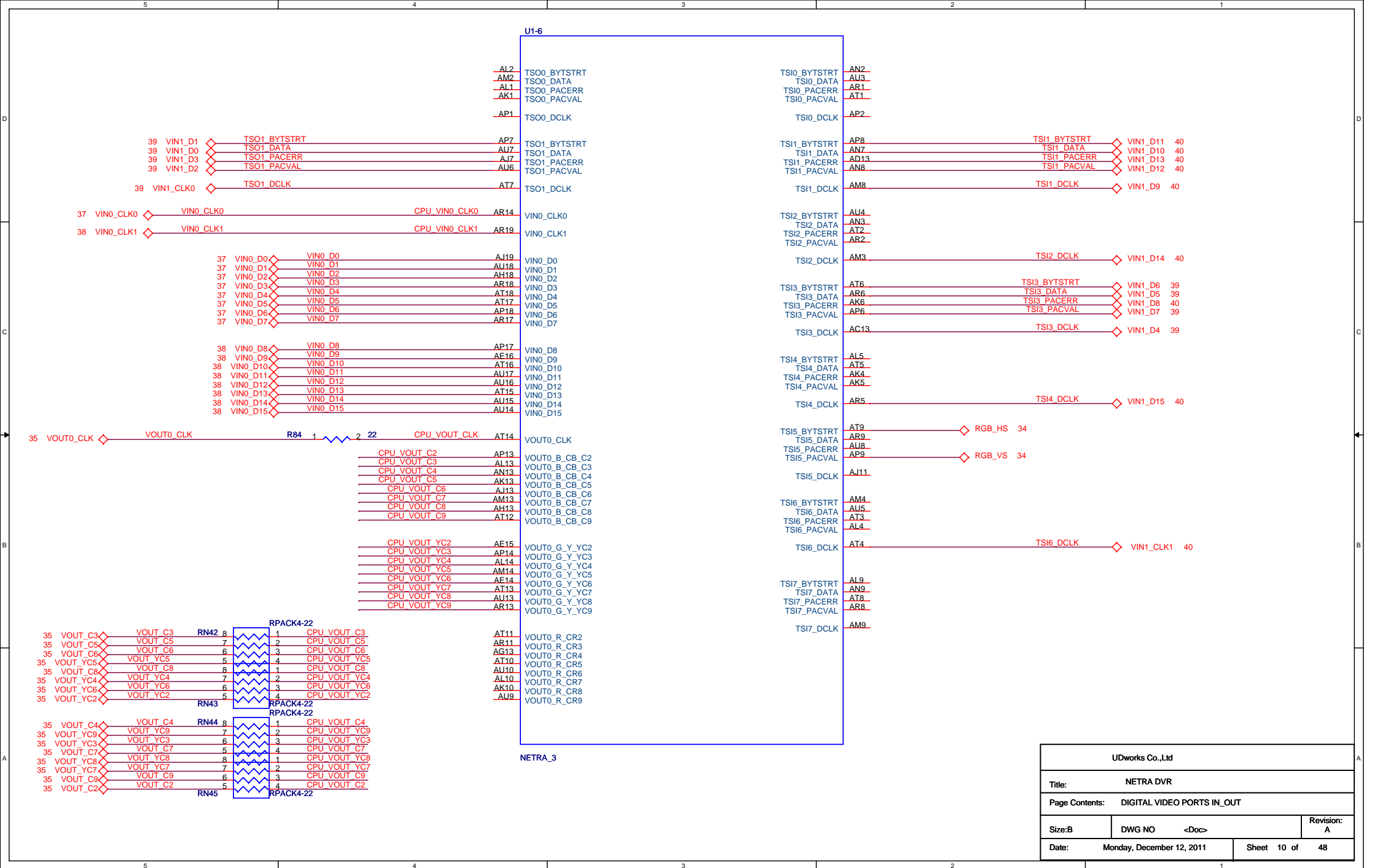


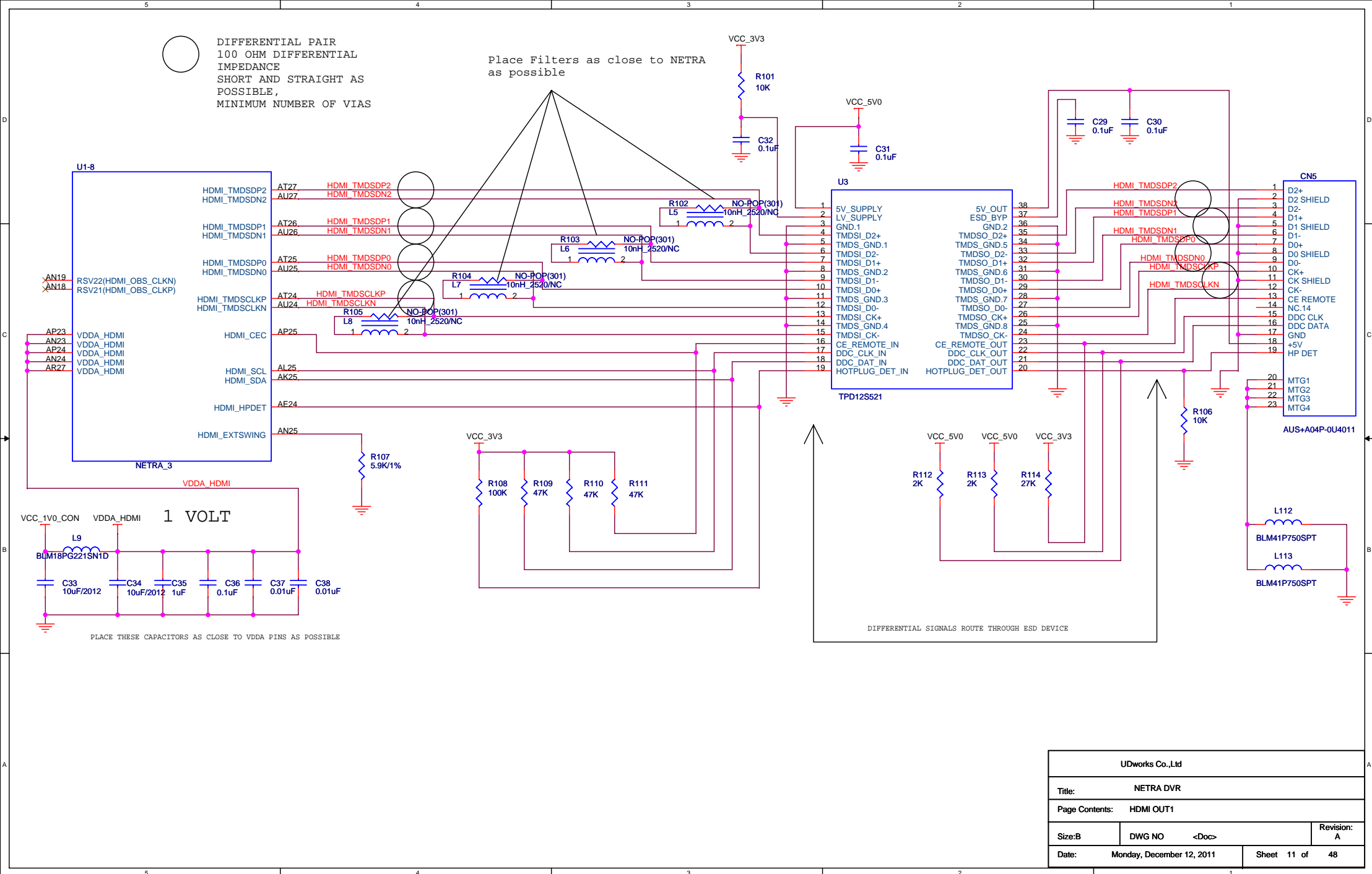
DIFFERENTIAL PAIRS

UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA DDR1 INTERFACE			
Size:B	DWG NO	<Doc>	Revision: A
Date: Monday, December 12, 2011	Sheet 8 of 48		

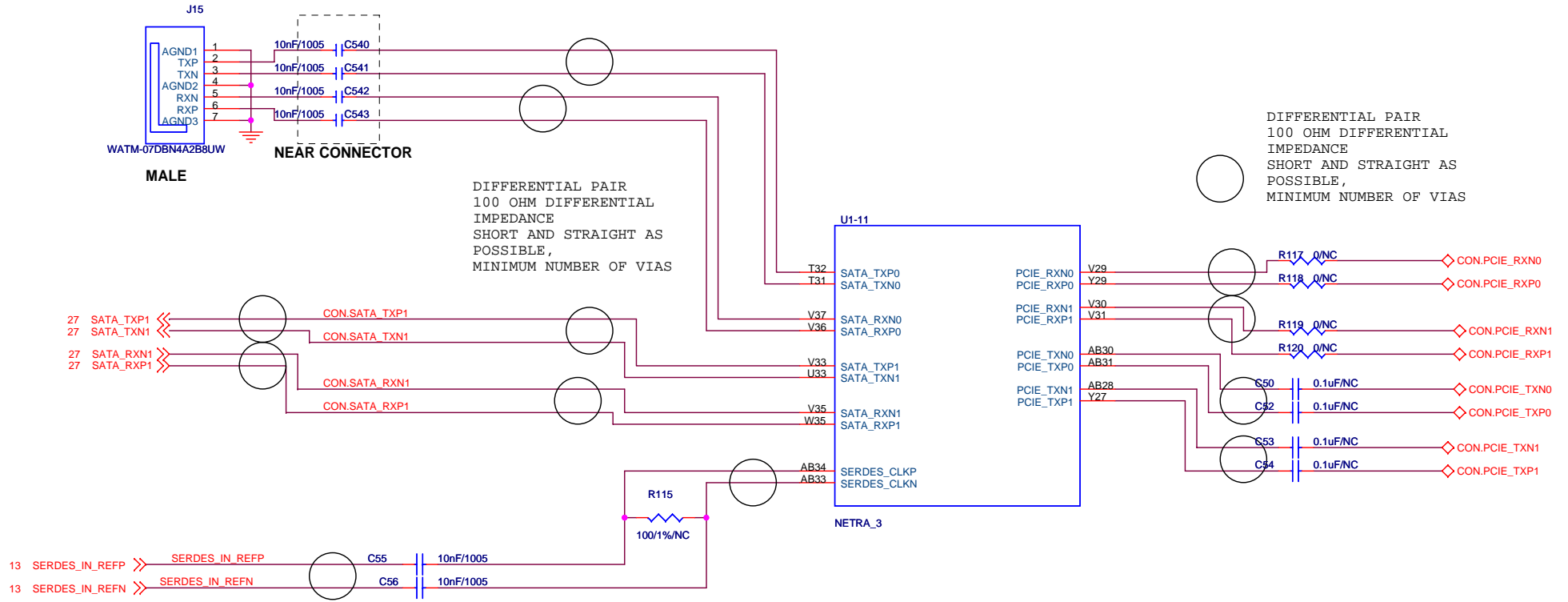


UDworks Co.,Ltd			
Title: NETRA DVR			
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Size:B	DWG NO	<Doc>	Revision: A
Date:	Monday, December 12, 2011		Sheet 9 of 48

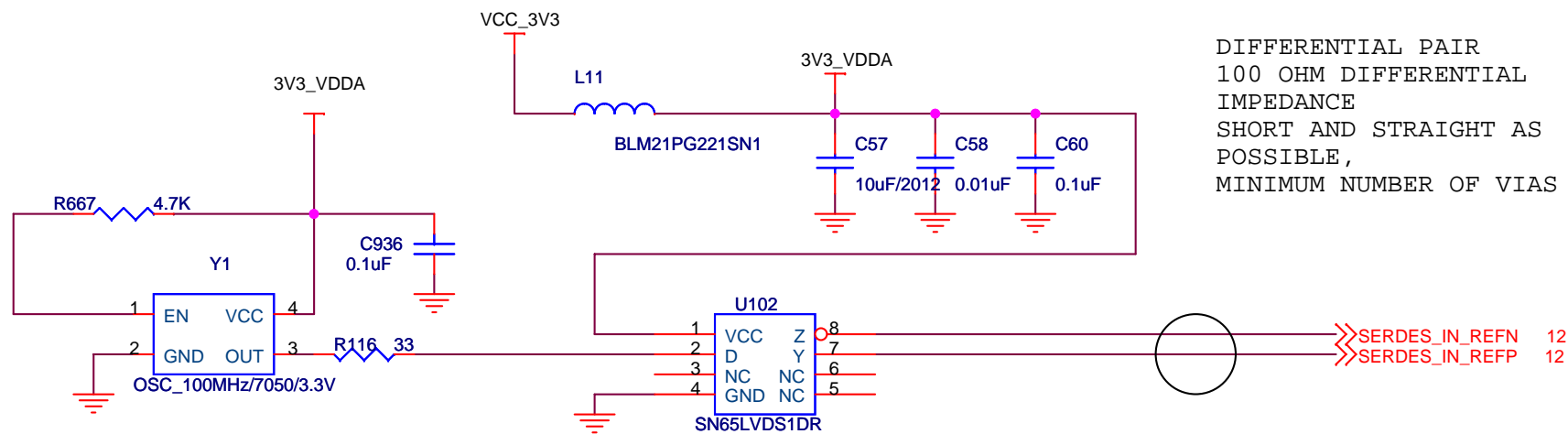




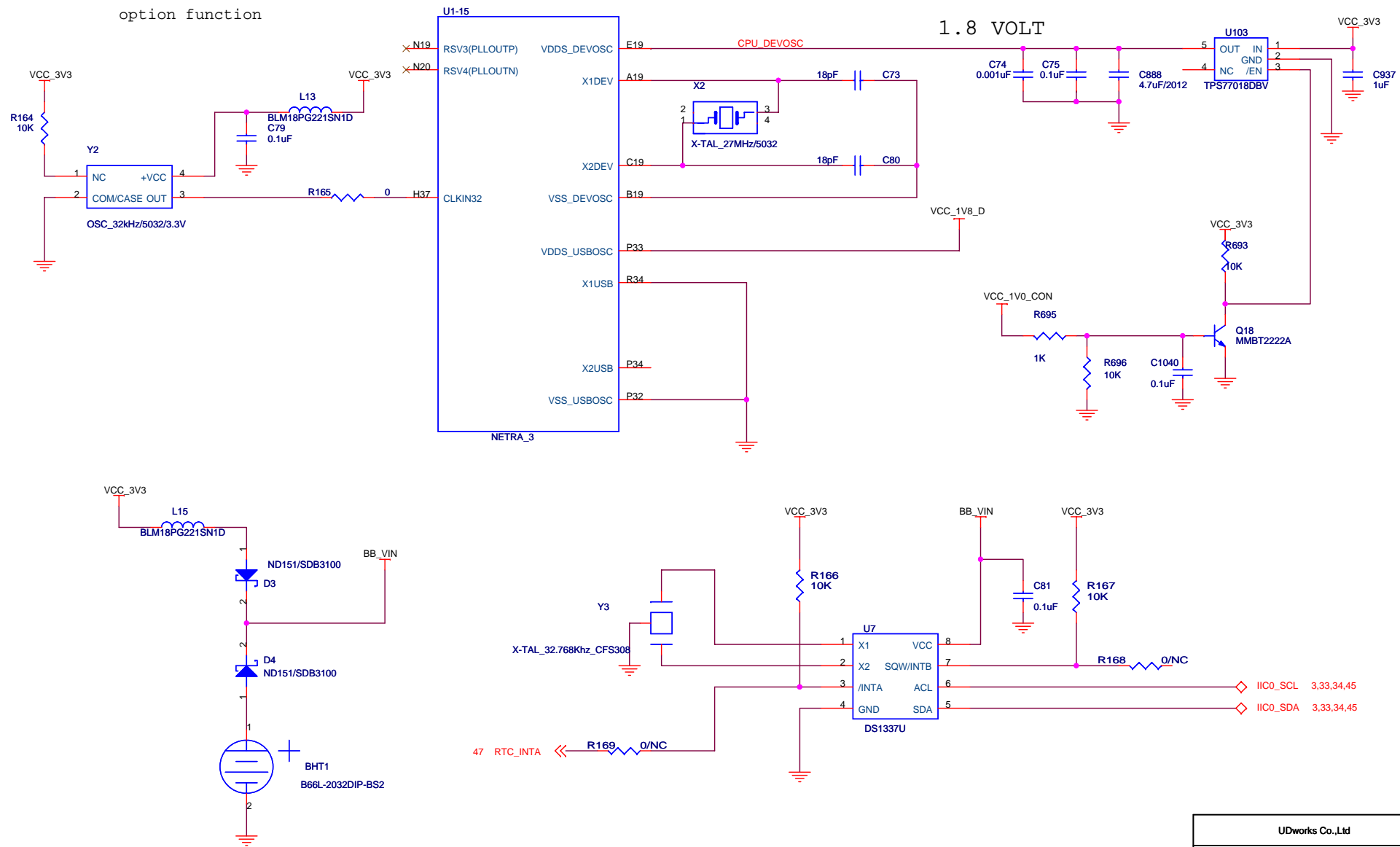
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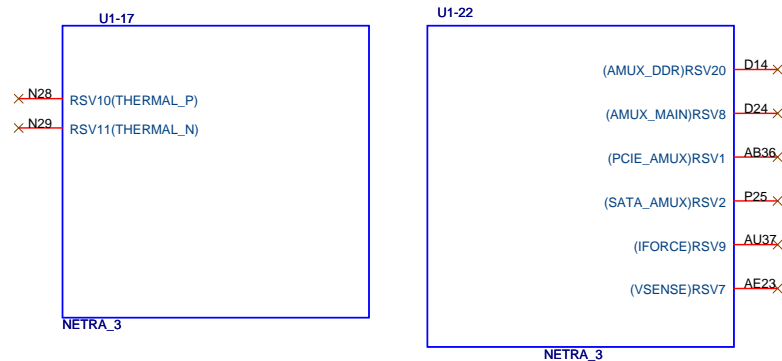
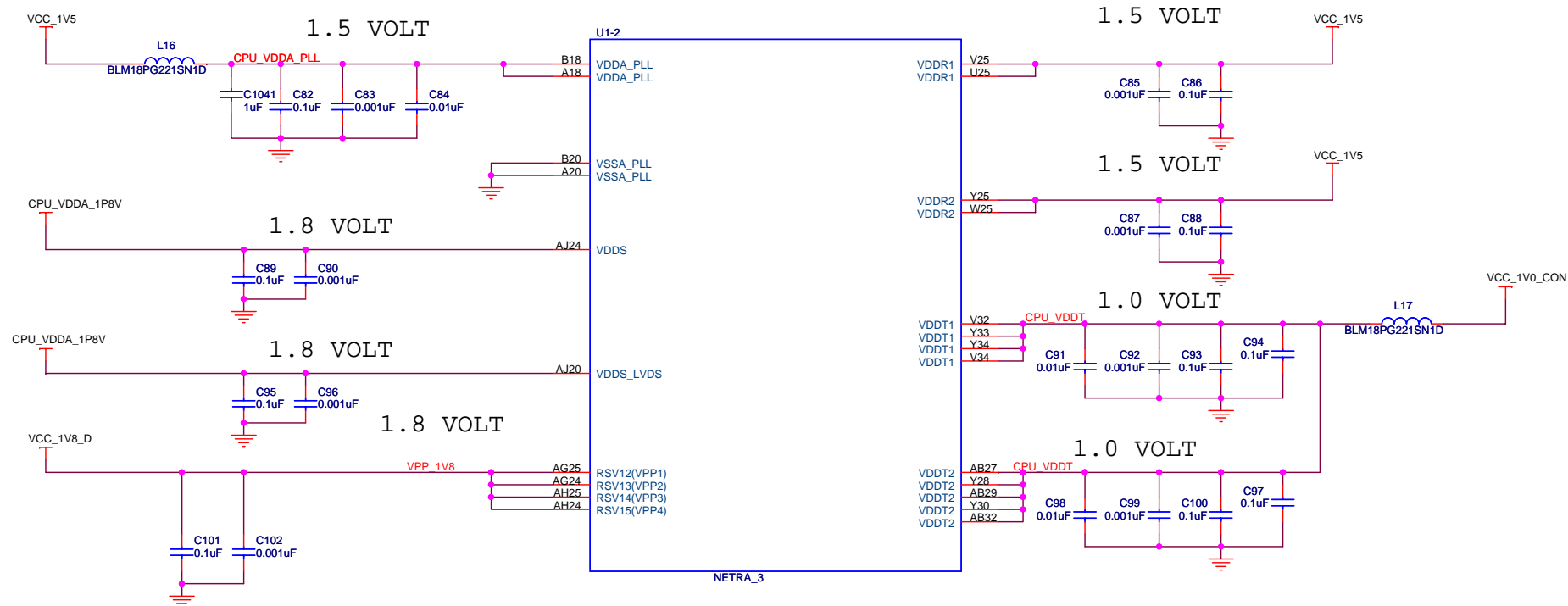
UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: SATA INTERFACE			
Size:B	DWG NO	<Doc>	Revision: A
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UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: SERDES CLOCKS			
Size:A	DWG NO	<Doc>	
Date:	Monday, December 12, 2011	Sheet 13 of	48

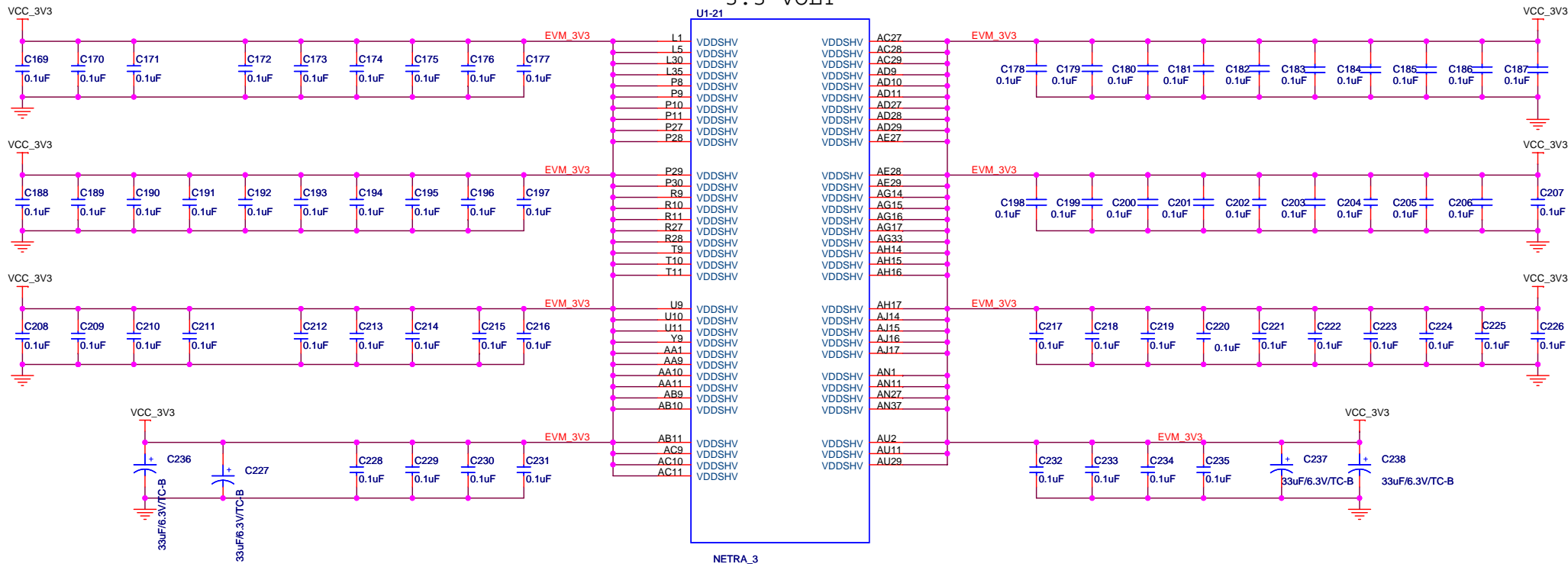


UDworks Co.,Ltd			
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Page Contents: NETRA CLOCKS/RTC			
Size: B	DWG NO	<Doc>	Revision: A
Date: Monday, December 12, 2011	Sheet 15 of 48		

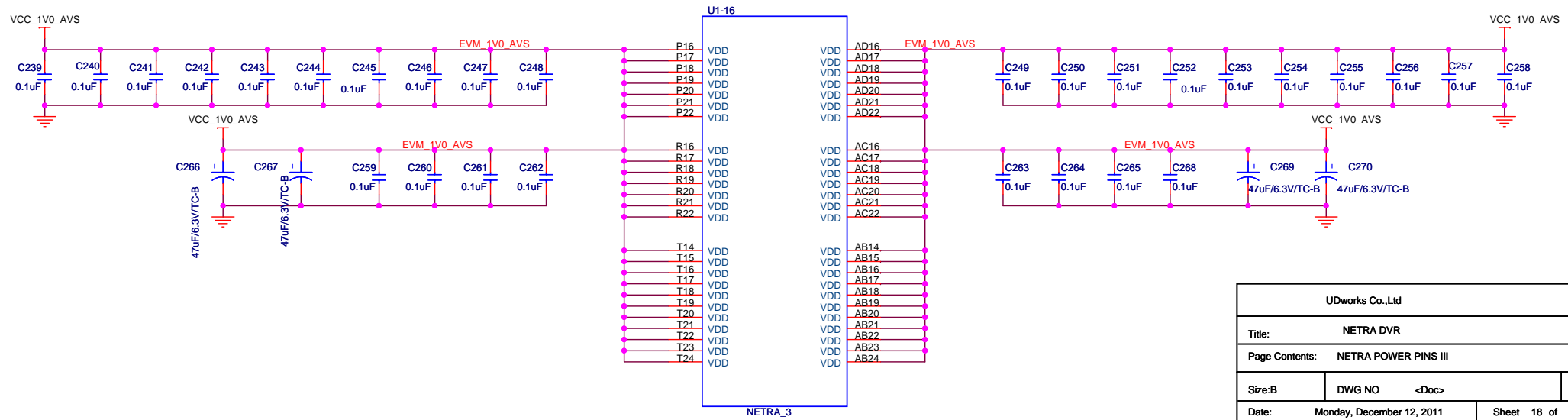


UDworks Co.,Ltd			
Title: NETRA DVR			
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Size:B	DWG NO	<Doc>	Revision: A
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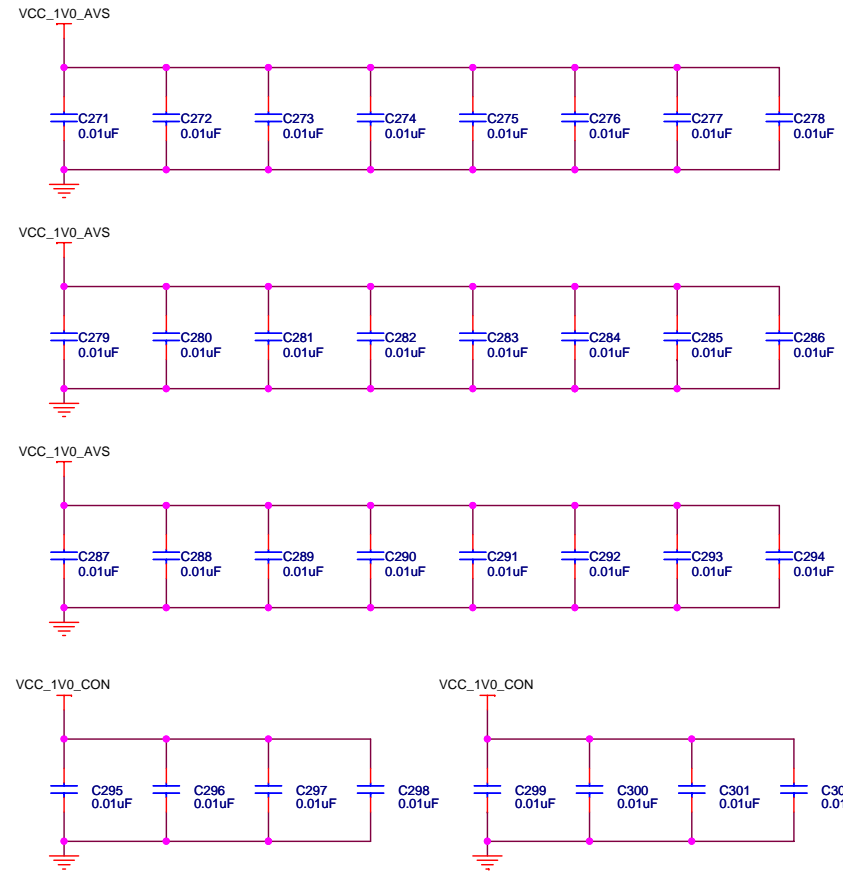
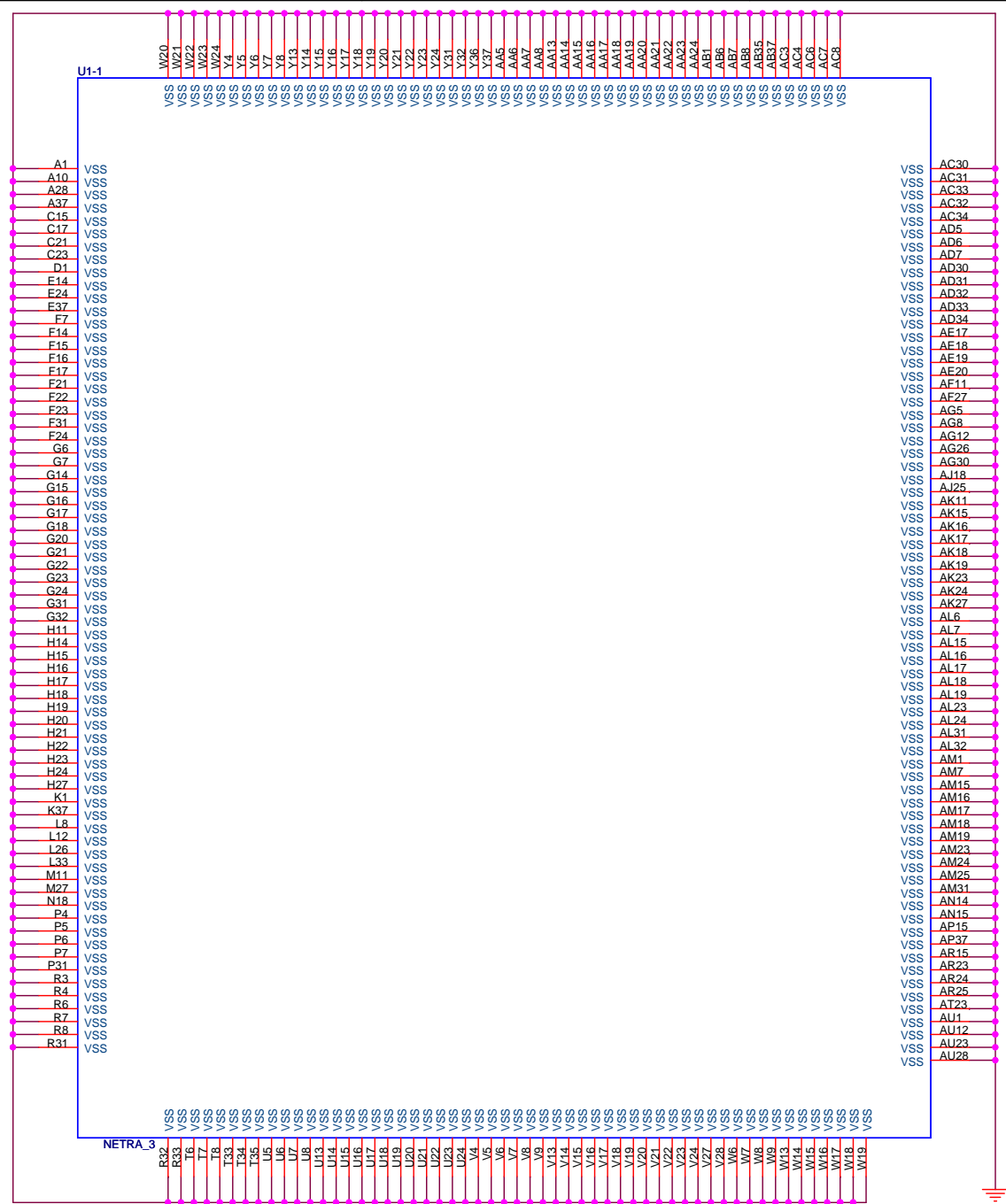
3.3 VOLT



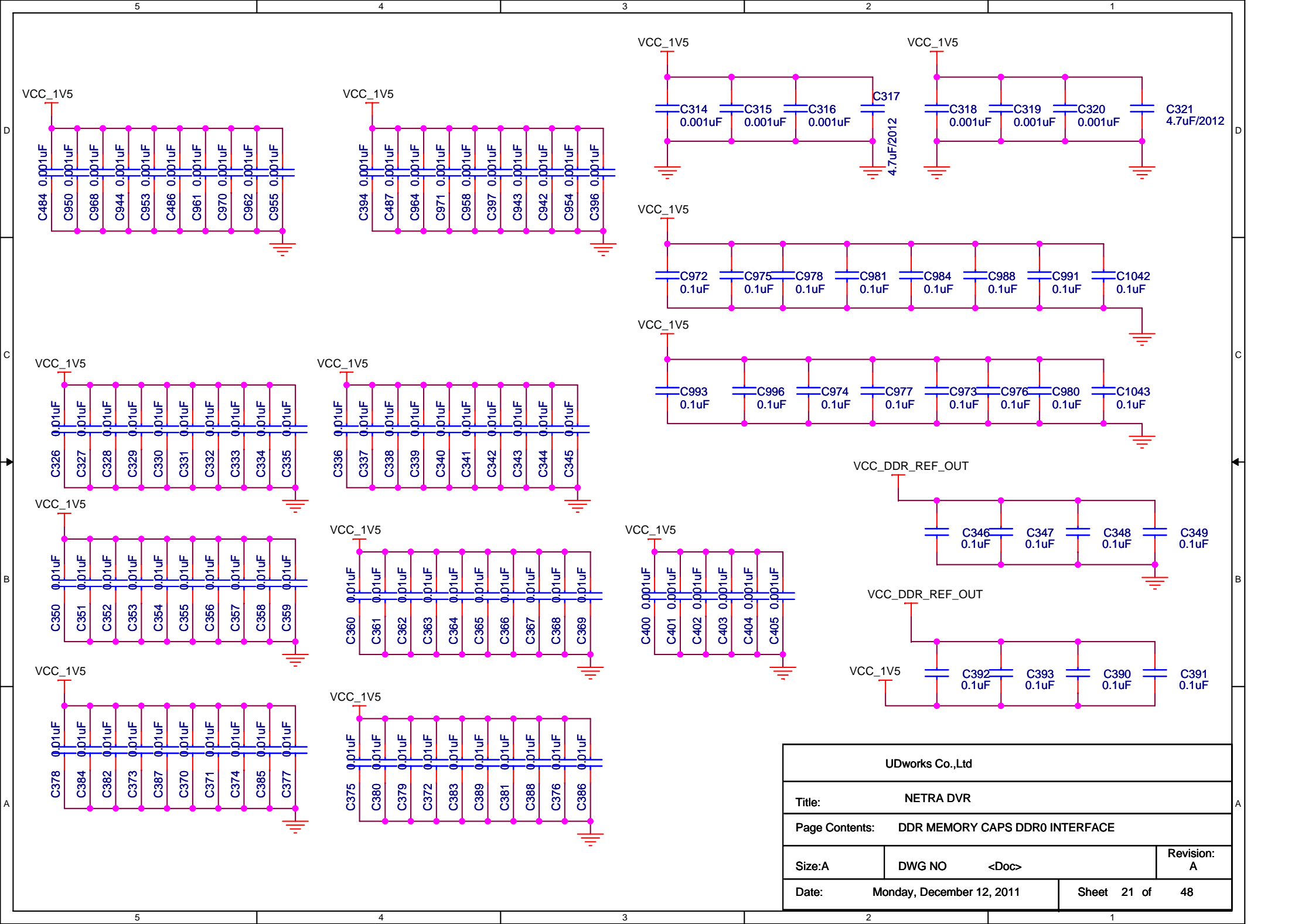
CORE AVS SUPPLY 1.0 VOLT

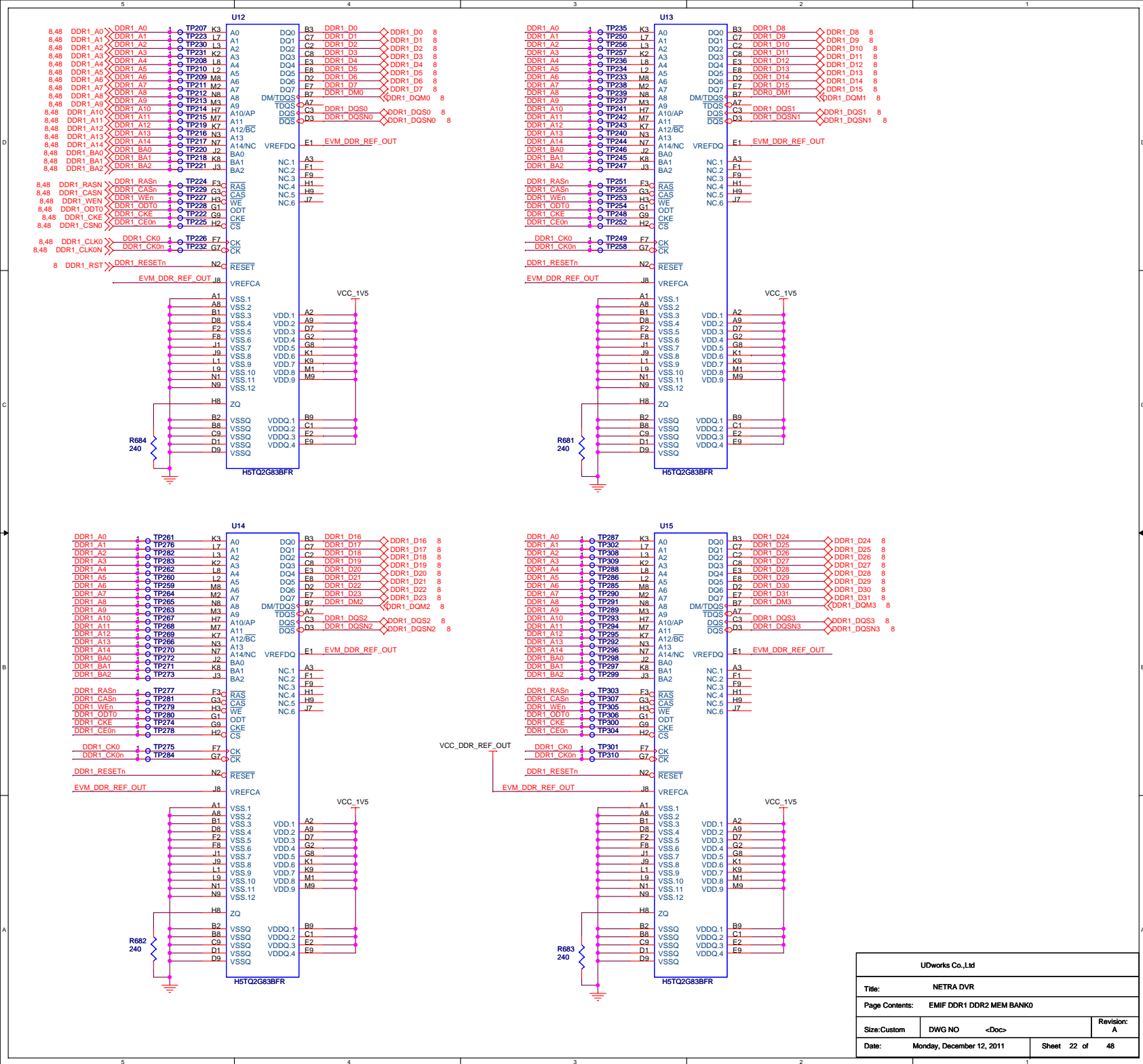


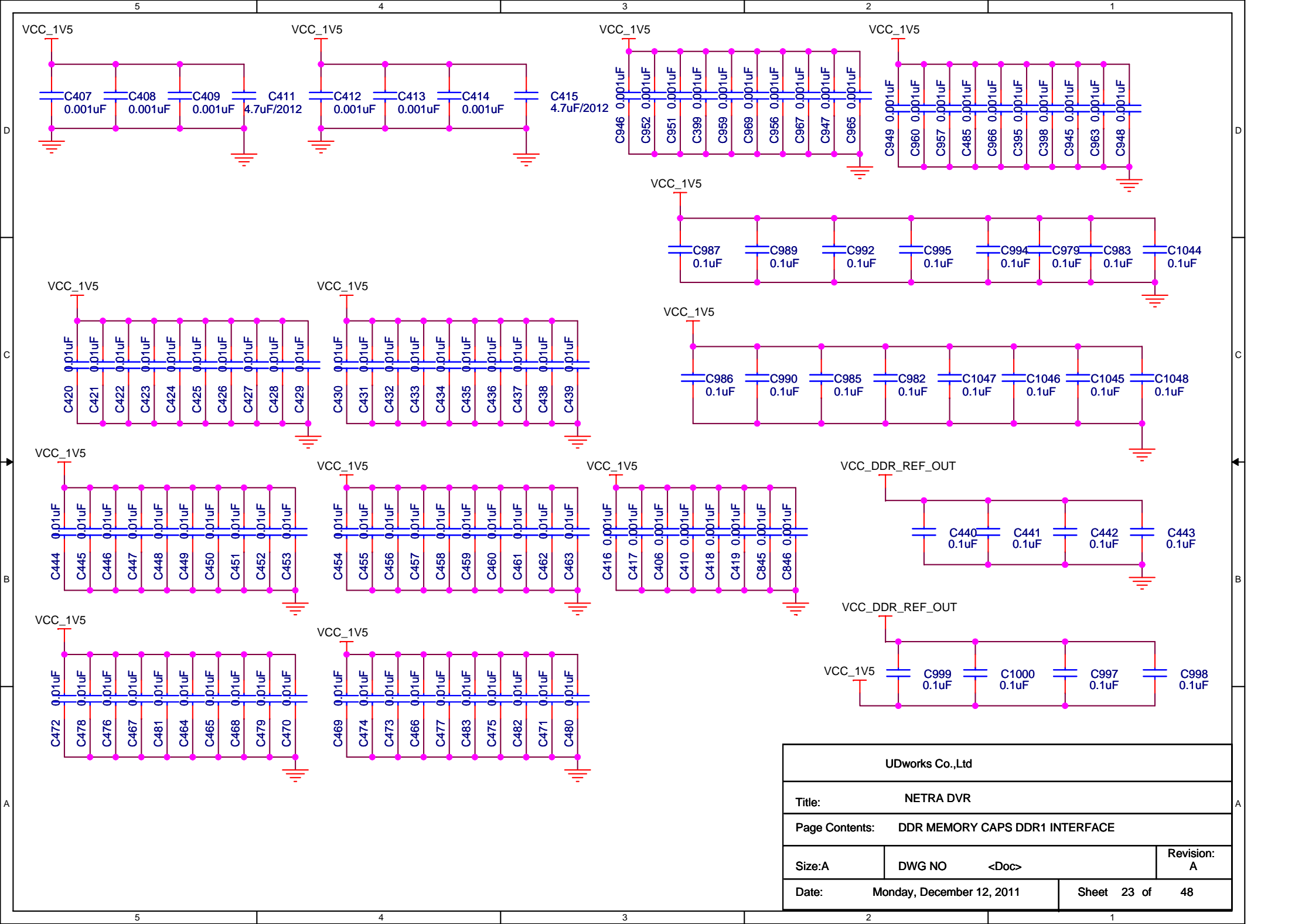
UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA POWER PINS III			
Size: B	DWG NO	<Doc>	Revision: A
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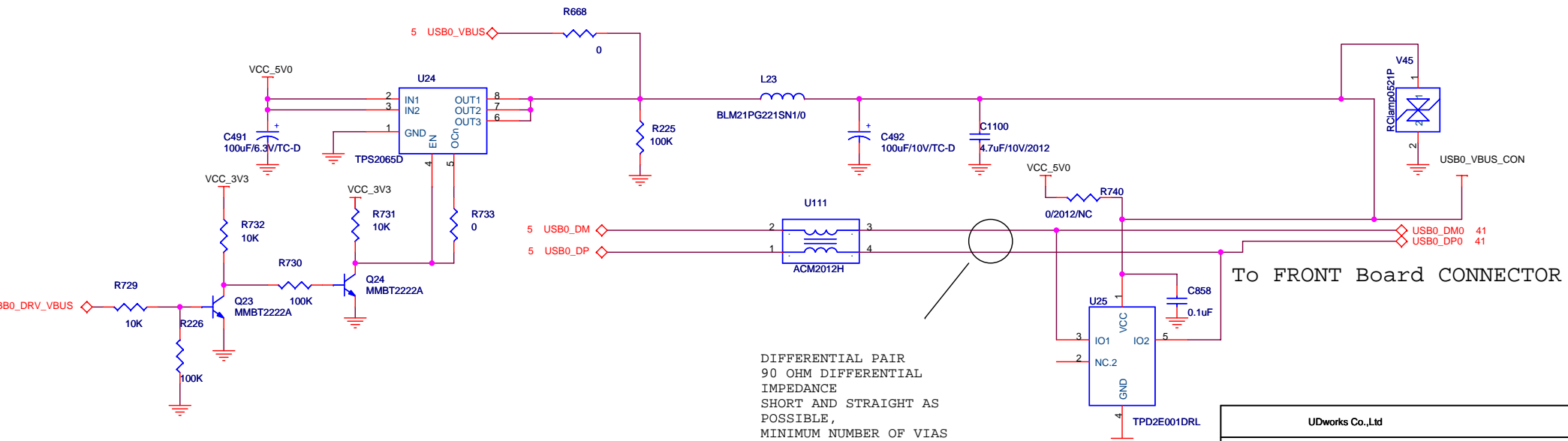
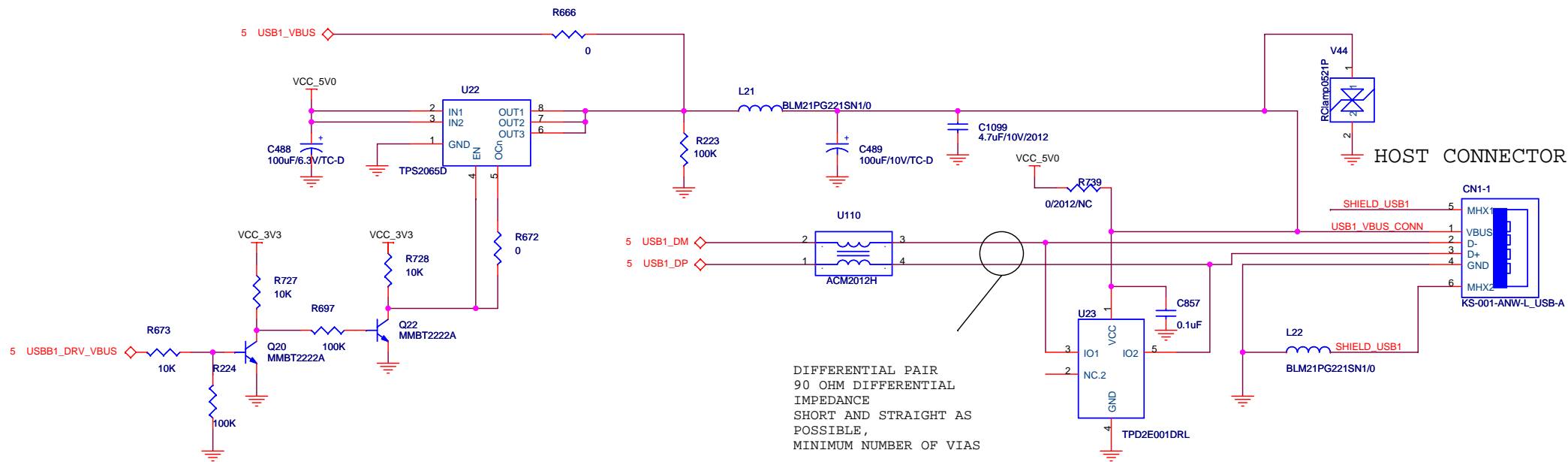


UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NETRA GROUND PINS & CAPS			
Size: B	DWG NO	<Doc>	Revision: A
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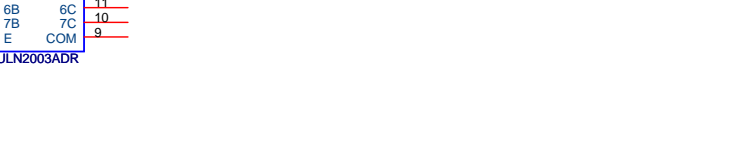
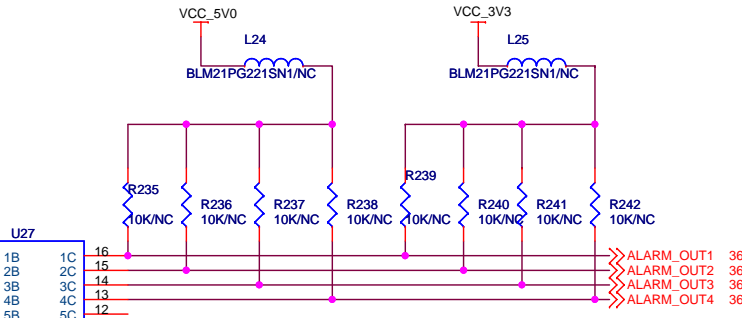
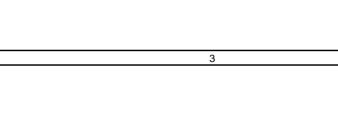
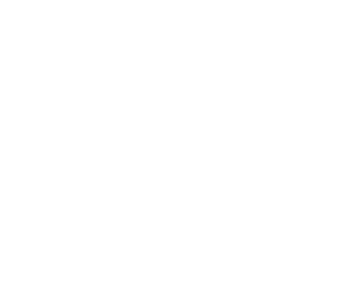
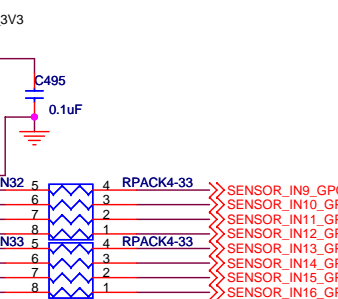
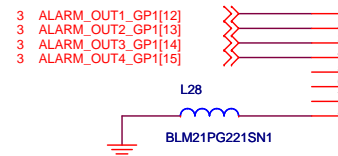
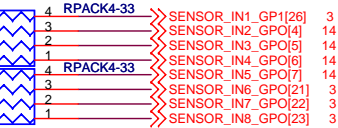
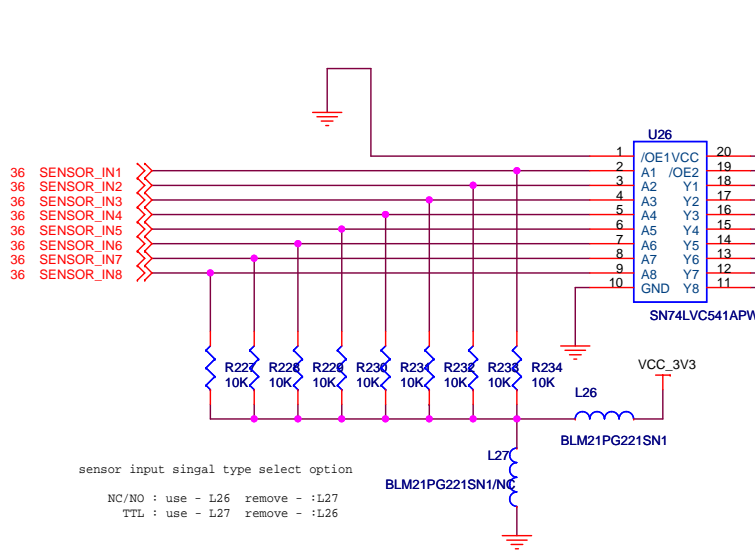




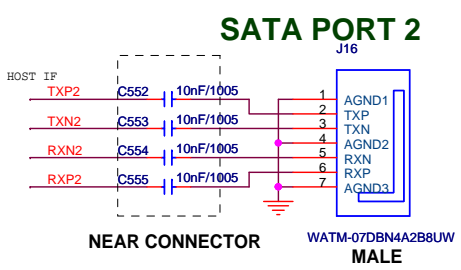
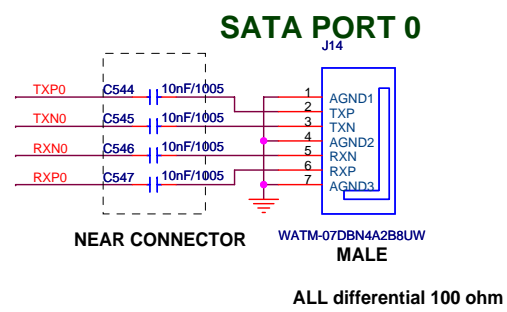
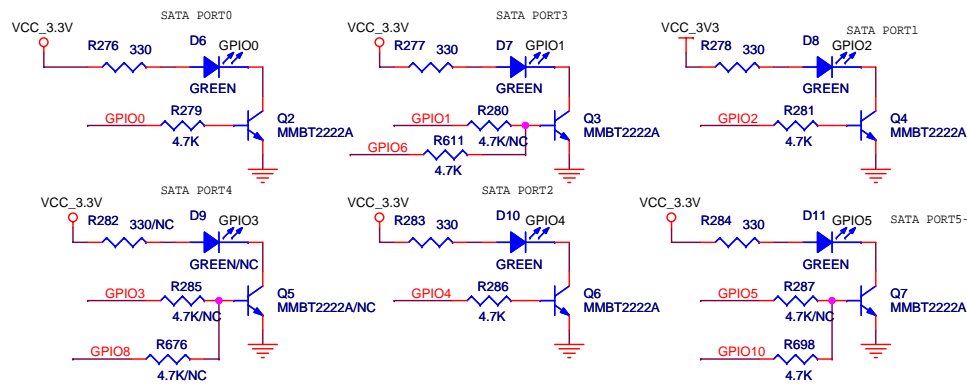
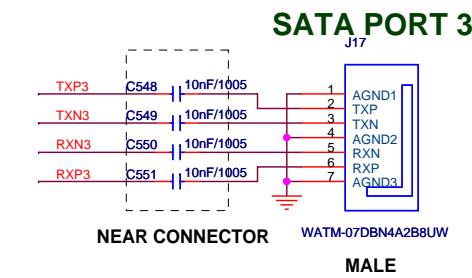
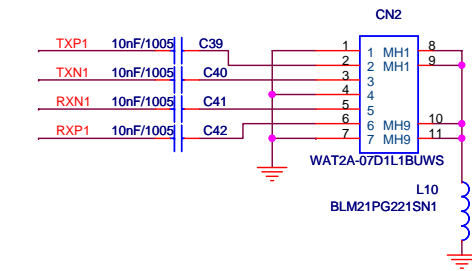
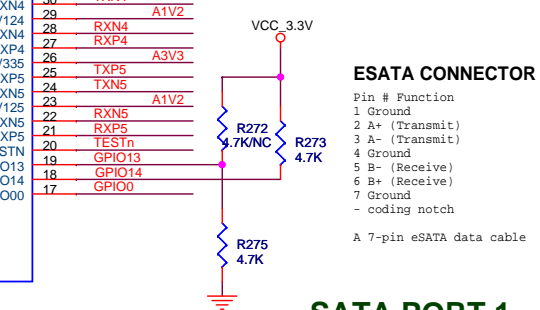
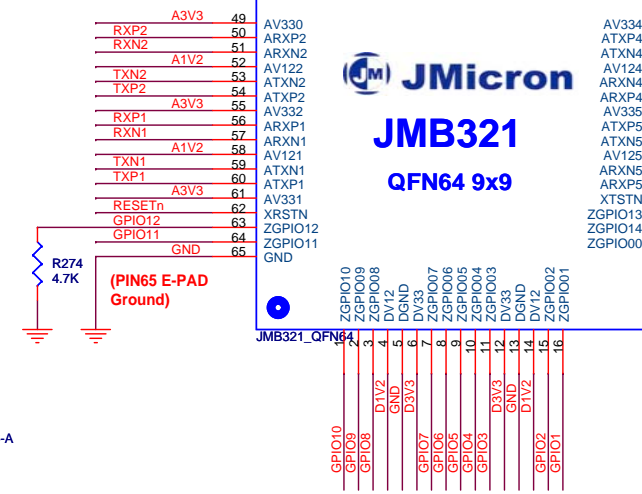
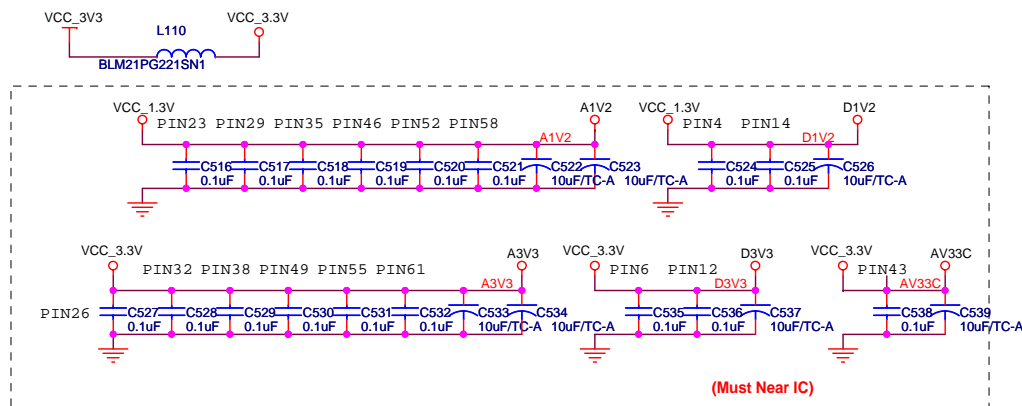
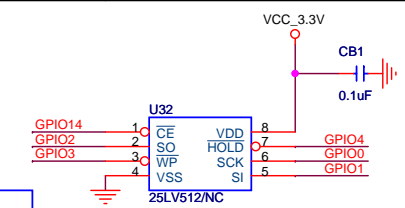
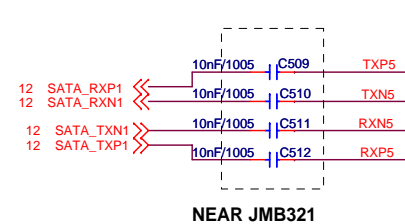




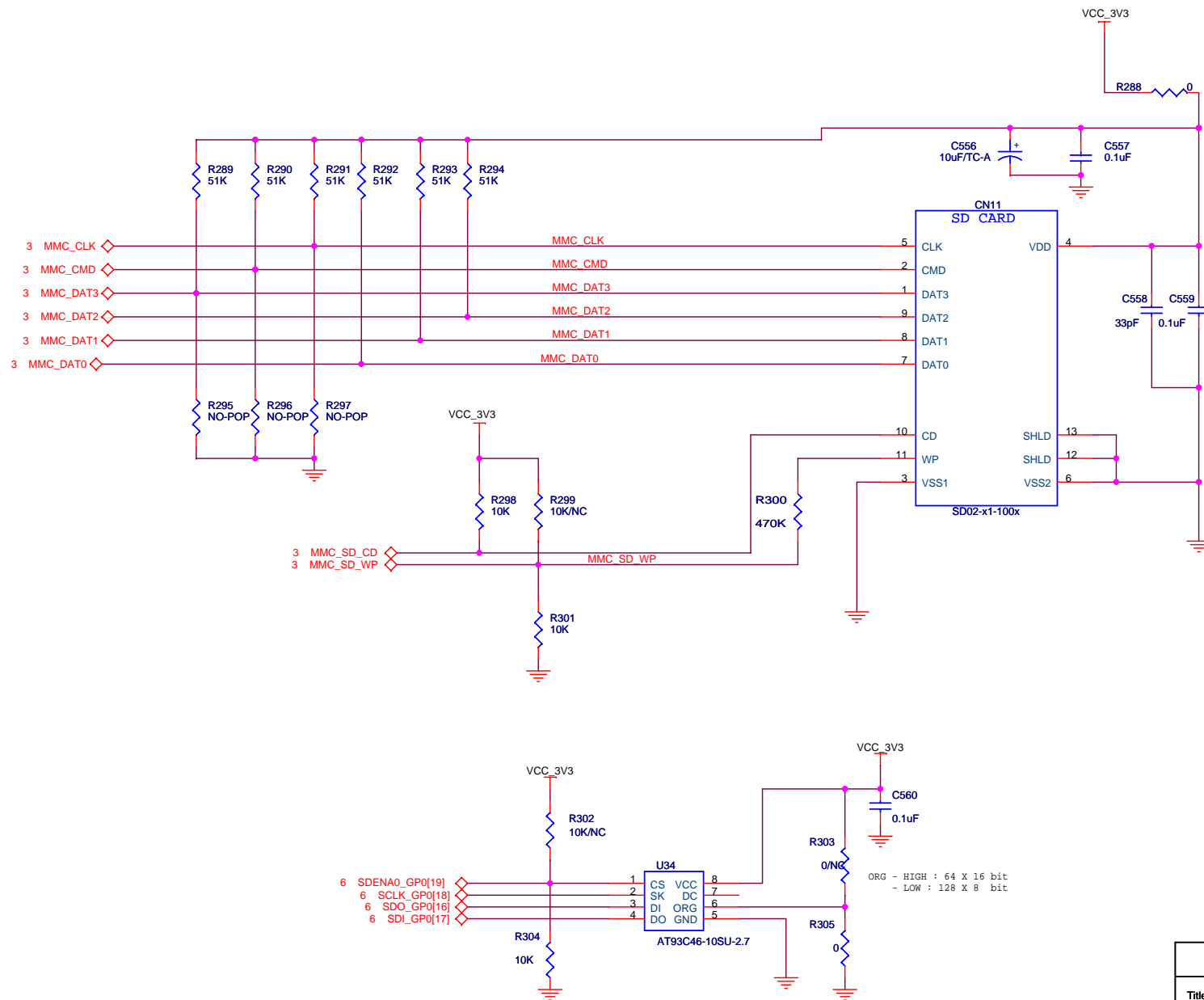
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Page Contents: USB INTERFACE CONNECTORS			
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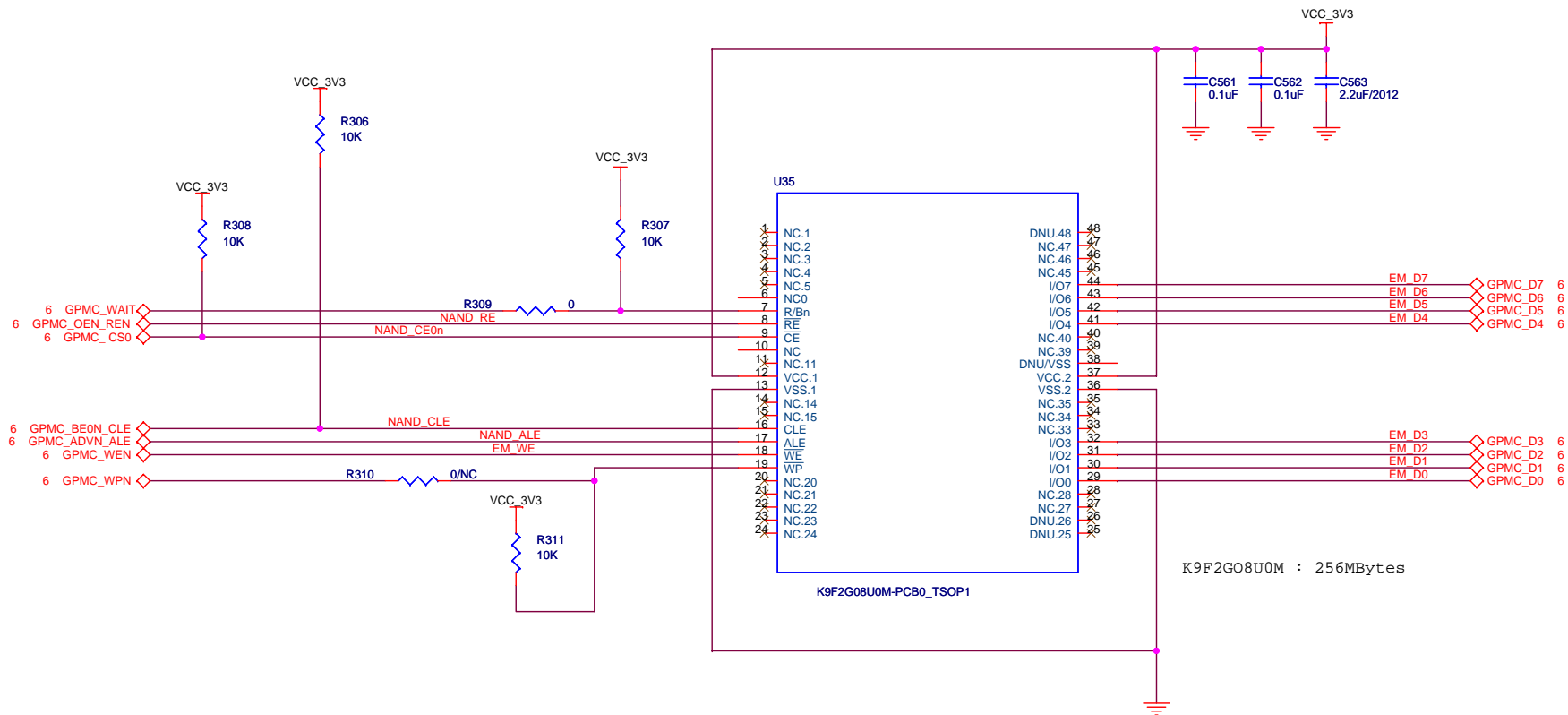
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Title: NETRA DVR			
Page Contents: SENSOR IN / ALARM OUT			
Size:B	DWG NO	<Doc>	Revision: A
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UDworks Co.,Ltd			
Title:		NETRA DVR	
Page Contents:		SATA MULTIPLIER	
Size:B	DWG NO	<Doc>	Revision: A
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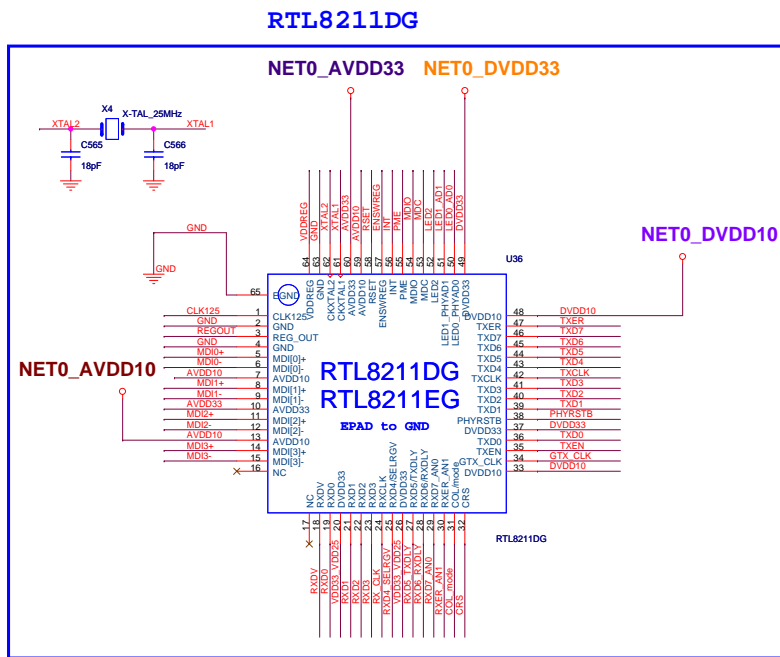


UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: SD/MMC INTERFACE/EEPROM			
Size:B	DWG NO	<Doc>	Revision: A
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UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: NAND FLASH			
Size:B	DWG NO	<Doc>	Revision: A
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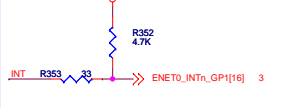
Place filter network close to RX_CLK.
Reserved for EMI



4.31 MDIO_MDIO ◇ MDIO

4.31 MDIO_MDCLK ≫ MDC

**Place filter network close to CLK125.
Reserved for EMI**



Connect ENSWREG to AVDD33 to enable Switching regulator or connect ENSWREG to GND to disable Switching regulator.

NET0_DVDD33

3.3V

R350 4.7K

C588 0.01uF

PHYRSTB

R351 330

D/NC

PCIRST

RSTOUTn 14, 27, 31, 33, 35, 37, 38, 39

3.3V

If use 2.5V RGMII please pull down

PULL UP: Config for all capability

Pull down: GMII Interface
Pull up : RGMII Interface

NETO_VDD33

10/100/1000 + Active

LED2

R313 0NC

C567 100pF/NC

R317 4.7K/NC

R326 510

R327 4.7K

PHYAD0 = 0
LED : HIGH Active

GMII0_ACT_LED 32.41

LED0 AD9

R642 4.7K/NC

R325 0

C568 100pF/NC

C Reserve for EMI, close to LAN connector

PHYAD1 = 0
LED : High Active

LED1 AD1

C569 100pF/NC

R332 510

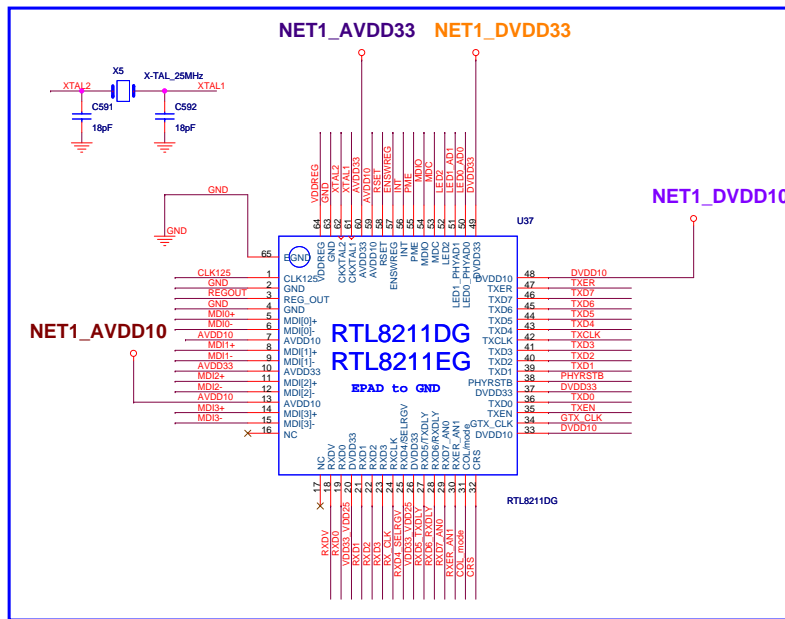
R333 4.7K

GMII0_SPD_LED 32

NET0_DVDD10

UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: ETHERNET INTERFACE PORT0			
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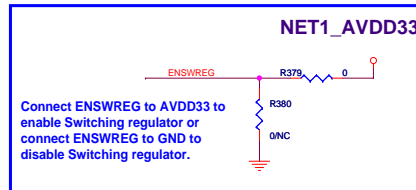
Place filter network close to RX_CLK.
Reserved for EMI



4,30 MDIO_MDIO MDIO

4,30 MDIO_MDC MDC

**Place filter network close to CLK125.
Reserved for EMI**



NET1_DVDD33

R392 4.7K

C614 0.01uF

R393

PCIRST

RSTOUTn 14, 27, 30, 33, 35, 37, 38, 39

NET1_DVDD33

R395

R394 4.7K

33

INT ENET1_INTn_GP1[17] 3

The diagram illustrates the pull-up and pull-down configurations for an RGMII interface. It shows three signal lines: **RXD4 SELRGV**, **RXD7 AN0 RXER AN1**, and **COL_mode**. The **RXD4 SELRGV** line is connected to **VDD3 VDD25** via a 4.7kΩ resistor (R377) and has a 4.7kΩ resistor (R378) connected to **VDD3 VDD25** at the other end. The **RXD7 AN0 RXER AN1** line is connected to **VDD3 VDD25** via a 4.7kΩ resistor (R381) and has a 4.7kΩ resistor (R382) connected to **VDD3 VDD25** at the other end. The **COL_mode** line is connected to **VDD3 VDD25** via a 4.7kΩ resistor (R385) and has a 4.7kΩ resistor (R387) connected to **VDD3 VDD25** at the other end. A dashed box labeled "PULL UP: Config for all capability" encloses the pull-up resistors for the **RXD7 AN0 RXER AN1** and **COL_mode** lines. A dashed box labeled "Pull down: GMII Interface" encloses the pull-down resistors for the **RXD7 AN0 RXER AN1** and **COL_mode** lines. A dashed box labeled "Pull up : RGMII Interface" encloses the pull-up resistors for the **RXD7 AN0 RXER AN1** and **COL_mode** lines. A ground symbol is shown at the bottom left.

NET1_DVDD10

the trace length from 22uF,0.1uF, 4.7uH to pin3 must be within 0.5cm

NET1_AVDD33

the trace length from 22uF,0.1uF to pin64 must be within 0.5cm

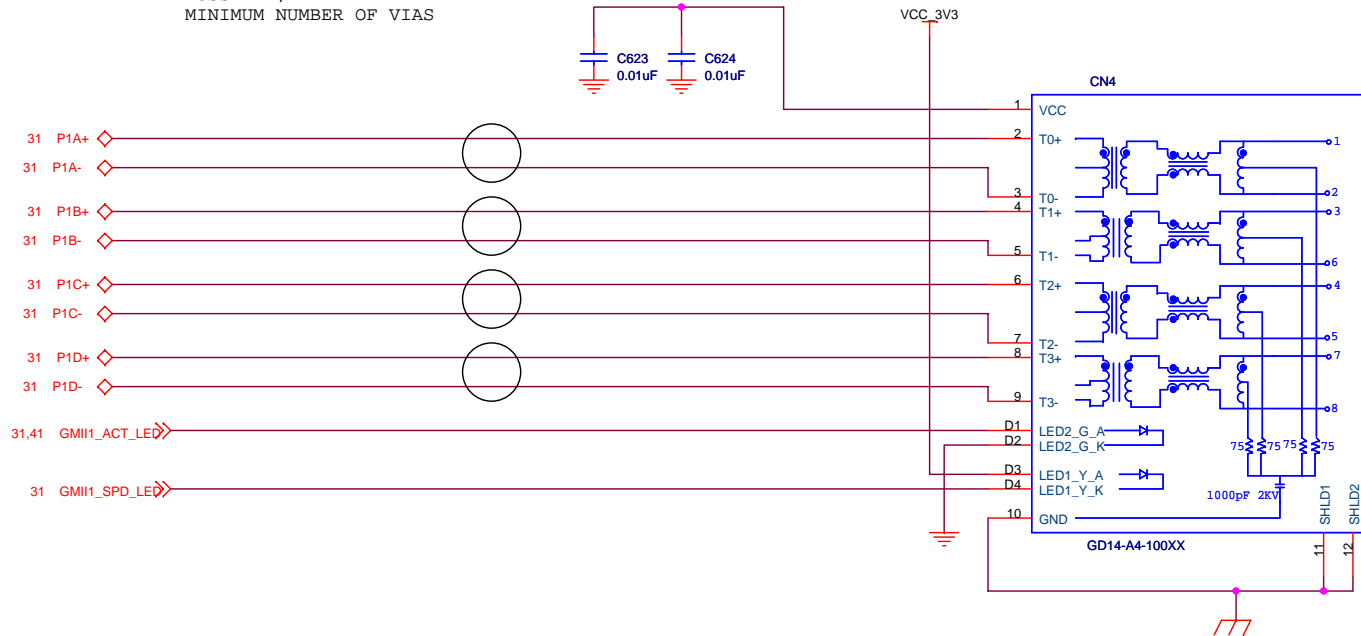
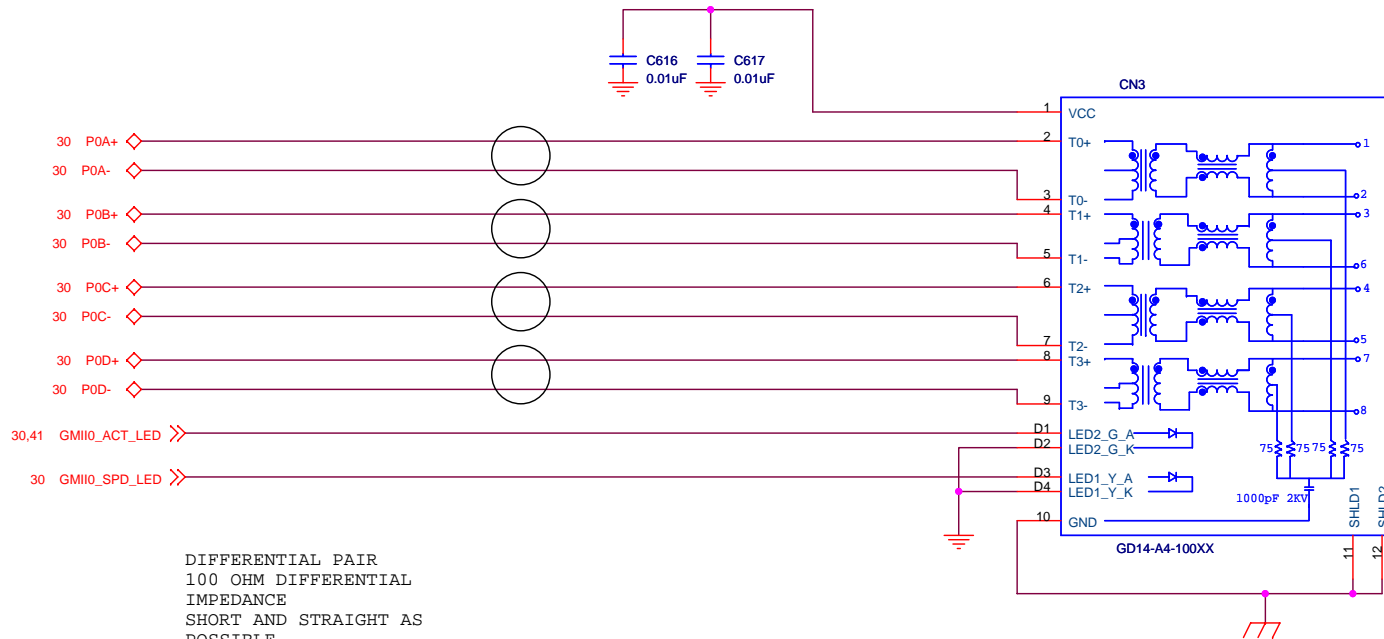
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Title: NETRA DVR			
Page Contents: ETHERNET INTERFACE PORT1			
Size:C	DWG NO	<Doc>	Revision

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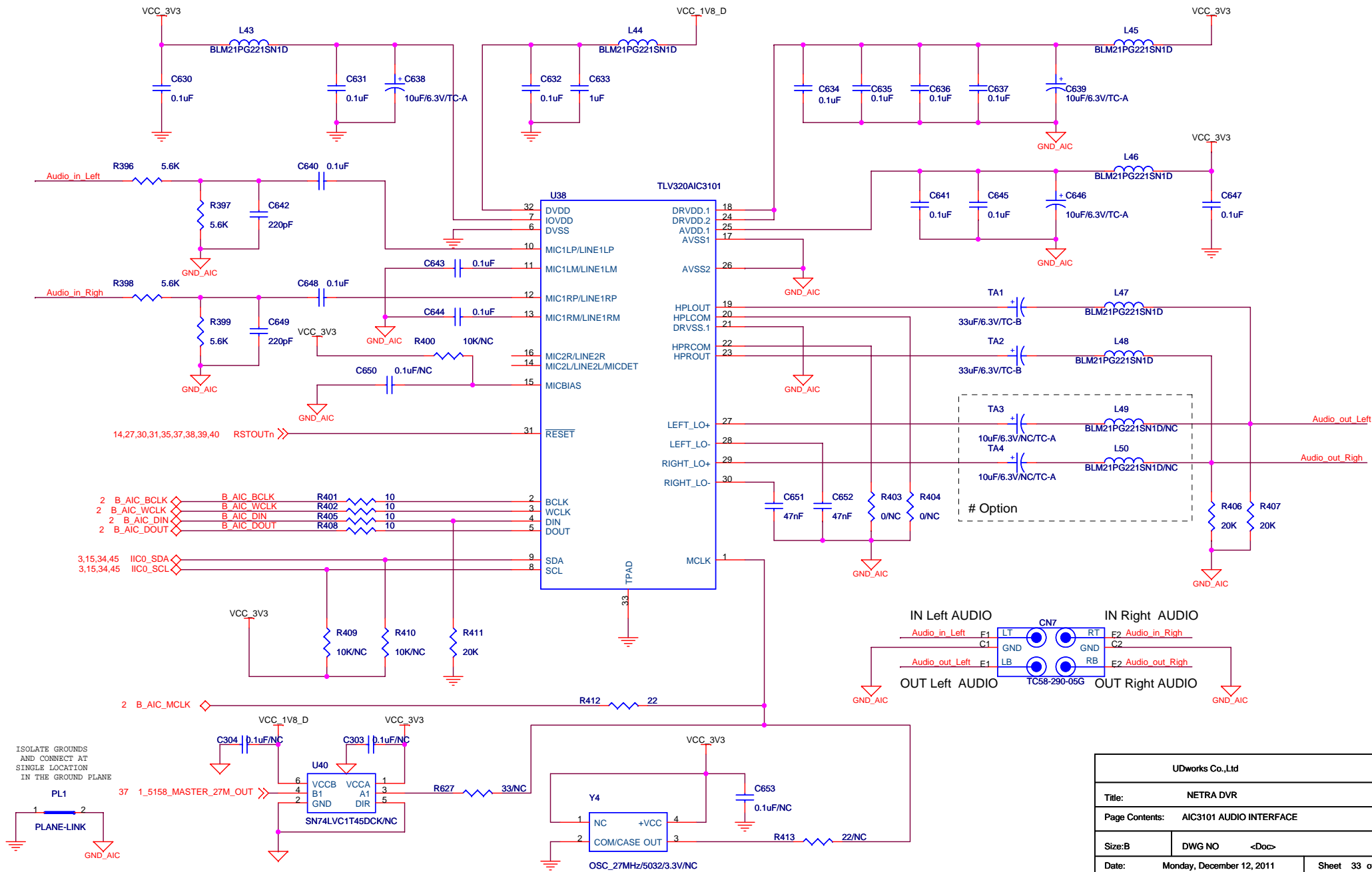
The schematic diagram illustrates the power supply section for the NET1_AVD33. The input is VCC_3V3, which is connected to a series of capacitors (C560, C586, C587, C588, C589) and an inductor (L39, BLMT18PG221SN1D) to filter the input. The output of the regulator is VDD33_VDD25, which is also decoupled with capacitors C940 and C939. The capacitors are labeled with their values: C560 (0.1uF), C586 (0.1uF), C587 (0.1uF), C588 (0.1uF), C589 (0.1uF), C940 (0.1uF), and C939 (0.1uF). The inductor L39 is labeled with its part number BLMT18PG221SN1D.

NET1_DVDD10

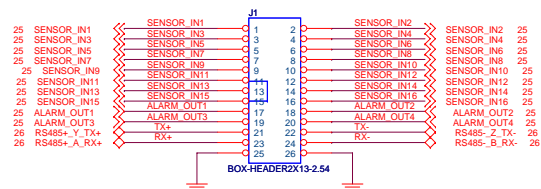
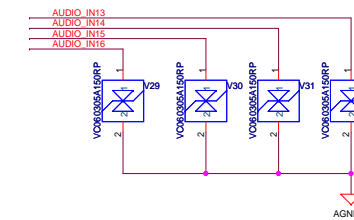
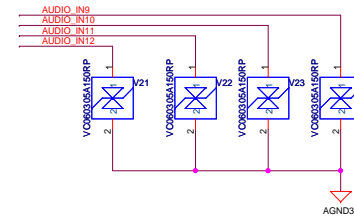
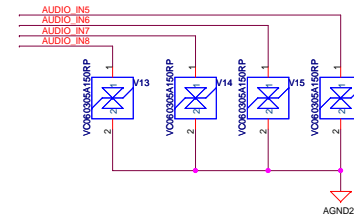
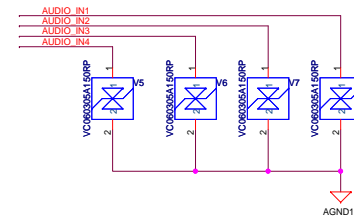
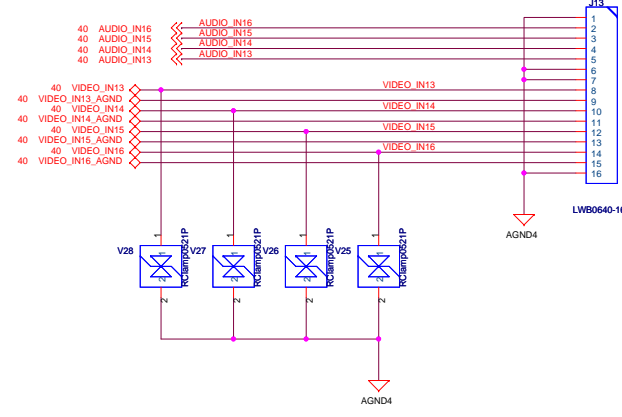
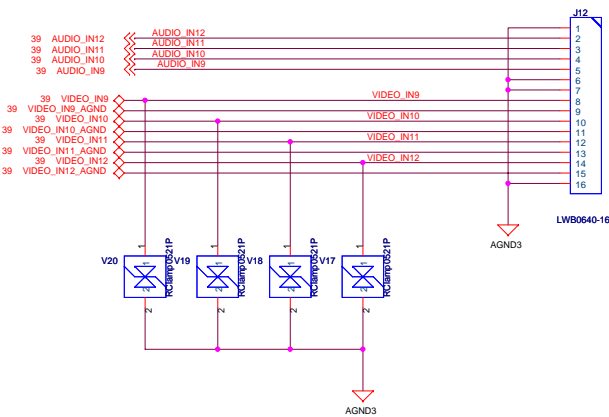
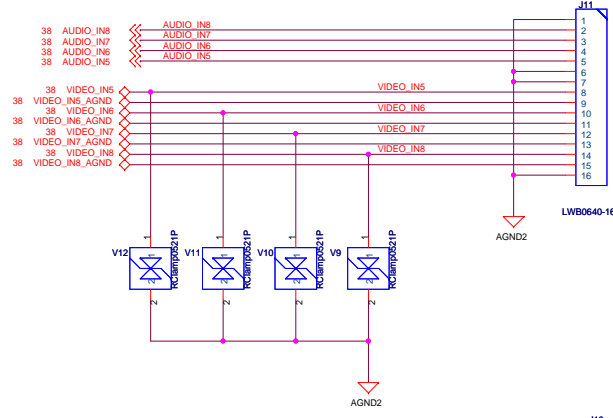
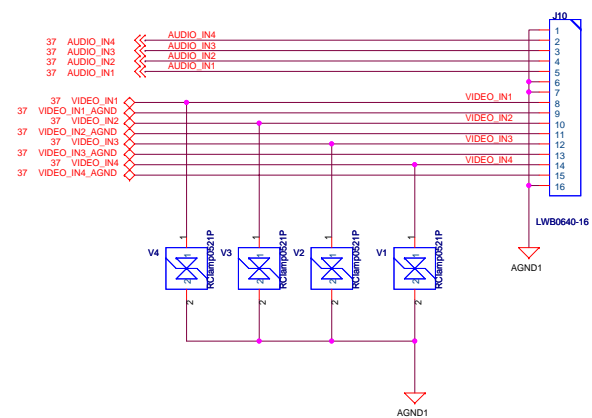
UDworks Co.,Ltd		
Title: NETRA DVR		
Page Contents: ETHERNET INTERFACE PORT1		
Size:C	DWG NO <Doc>	Revision: A
Date:	Monday, December 12, 2011	Sheet 31 of 48



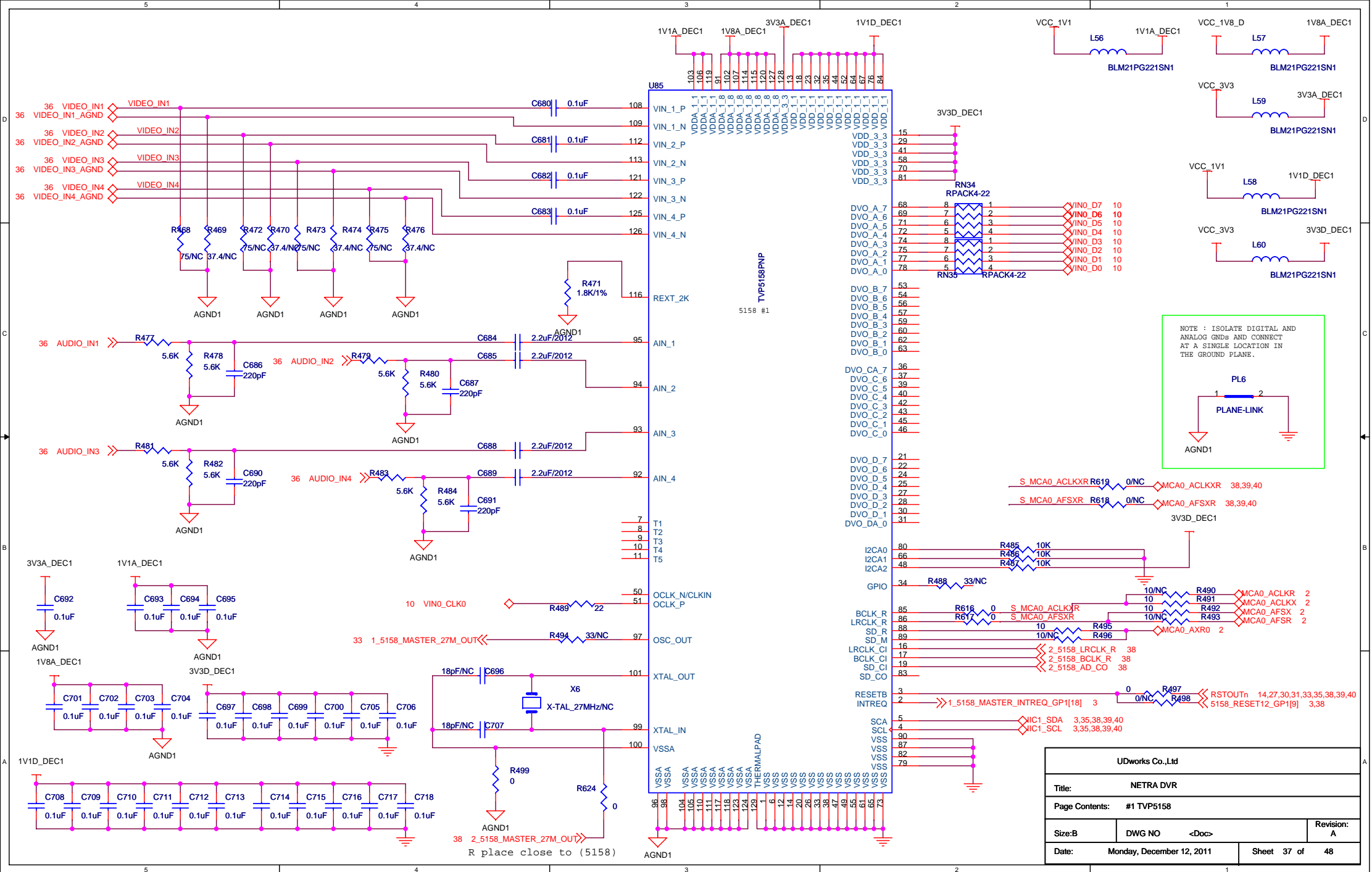
UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: ETHERNET - OUTPUT CONNECTOR			
Size:B	DWG NO	<Doc>	Revision: A
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UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: AIC3101 AUDIO INTERFACE			
Size:B	DWG NO	<Doc>	Revision: A
Date: Monday, December 12, 2011	Sheet 33 of 48		

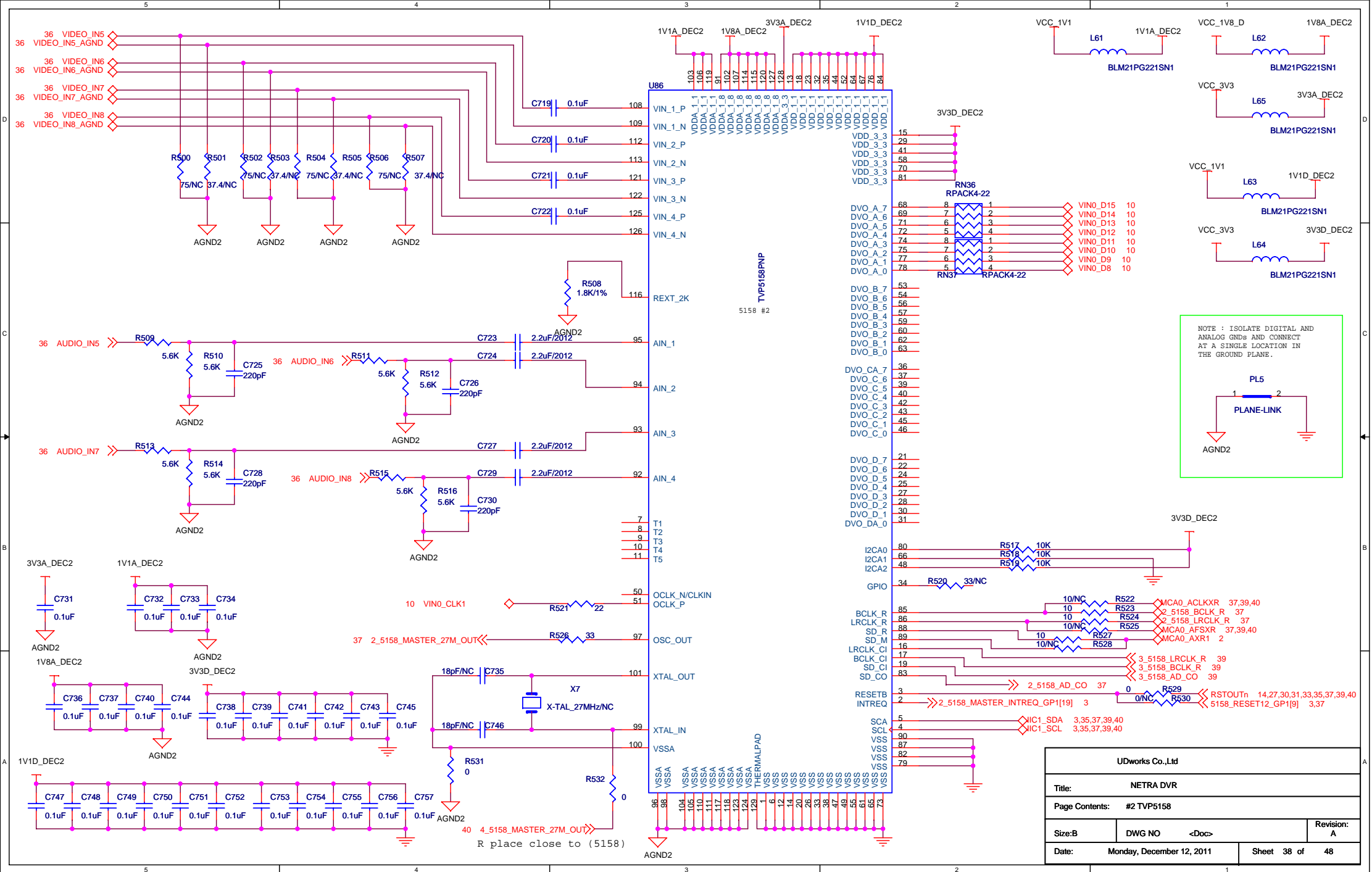


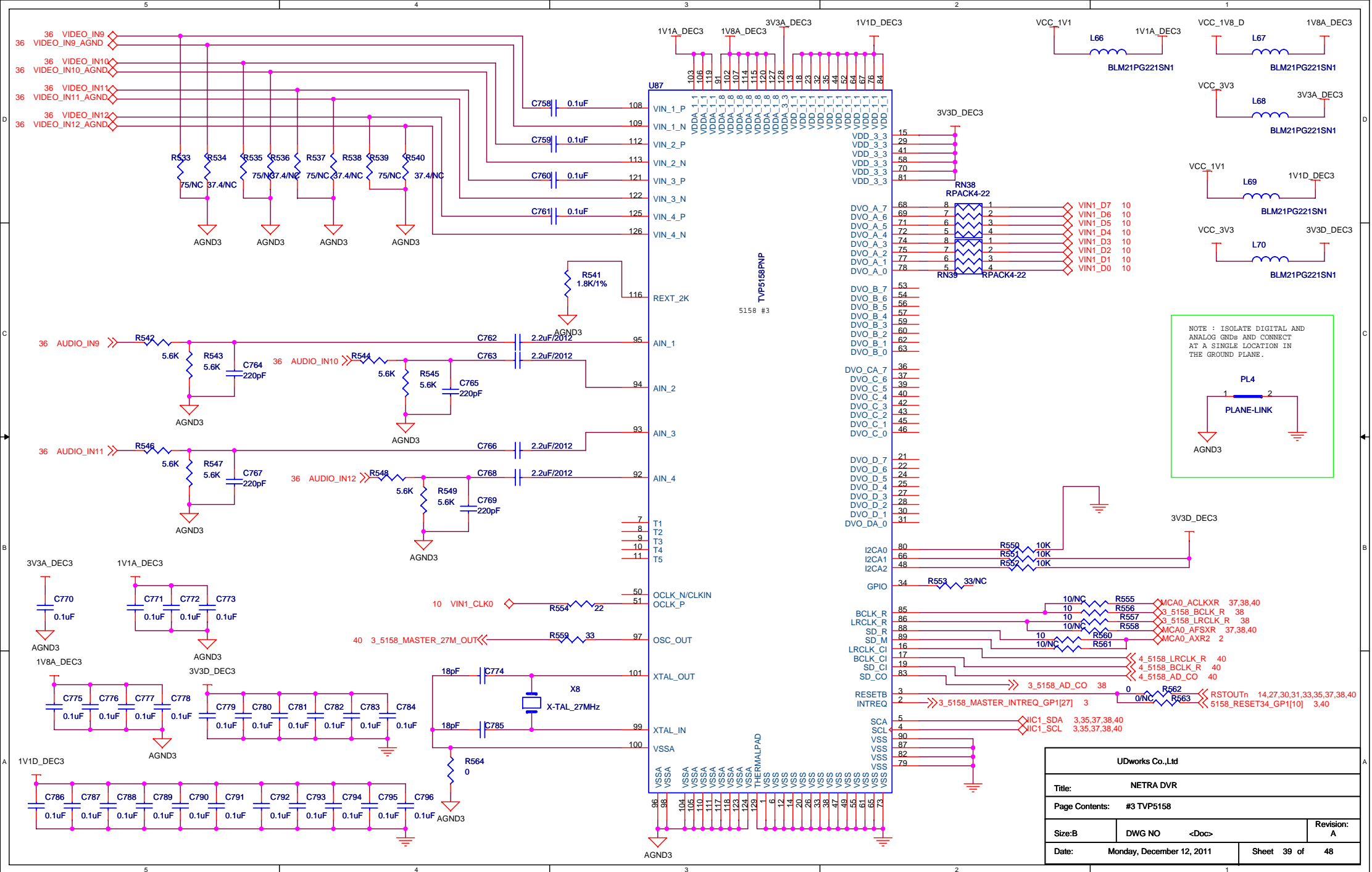
UDworks Co., Ltd			
Title: NETRA DVR			
Page Contents: REAR BOARD IF			
Size: C	DWG NO	<Doc>	Revision: A
Date: Monday, December 12, 2011	Sheet 36 of 48		



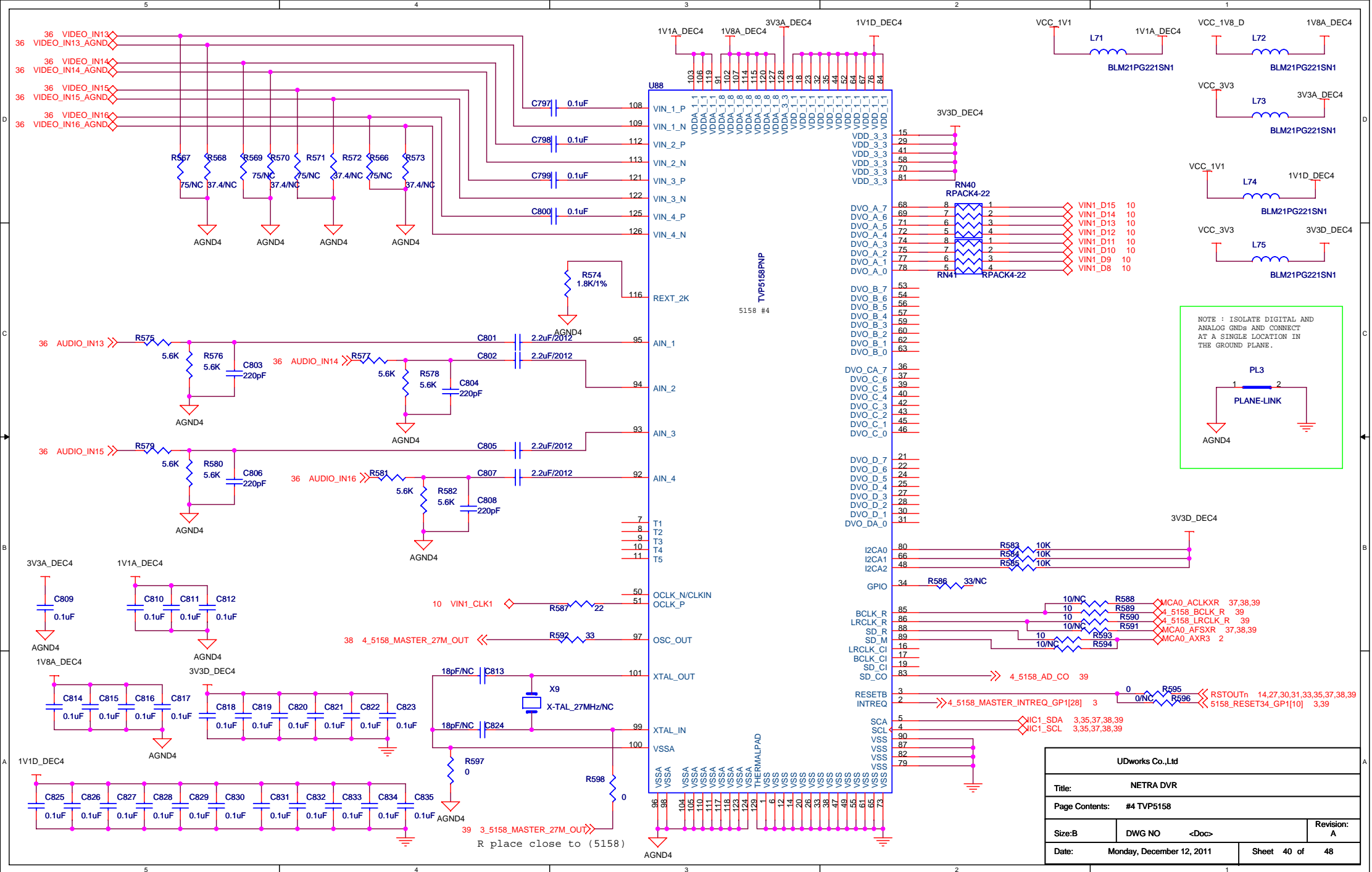
NOTE : ISOLATE DIGITAL AND ANALOG GNDs AND CONNECT AT A SINGLE LOCATION IN THE GROUND PLANE.

UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: #1 TVP5158			
Size: B	DWG NO	<Doc>	Revision: A
Date: Monday, December 12, 2011	Sheet 37 of 48		

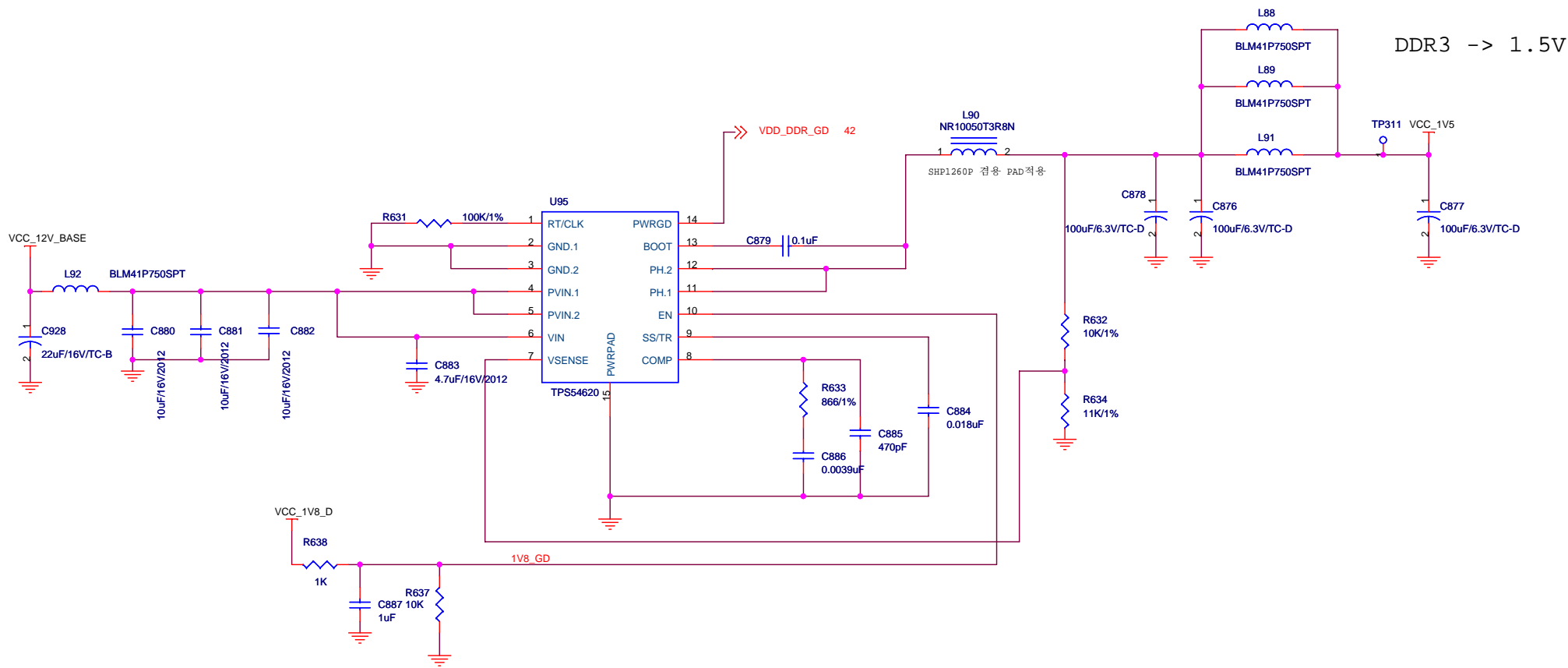




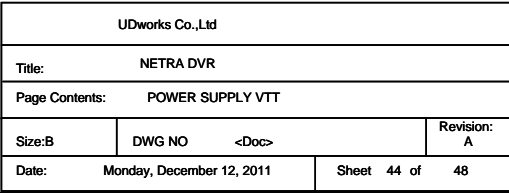
UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: #3 TYP5158			
Size: B	DWG NO	<Doc>	Revision: A
Date: Monday, December 12, 2011	Sheet 39 of 48		

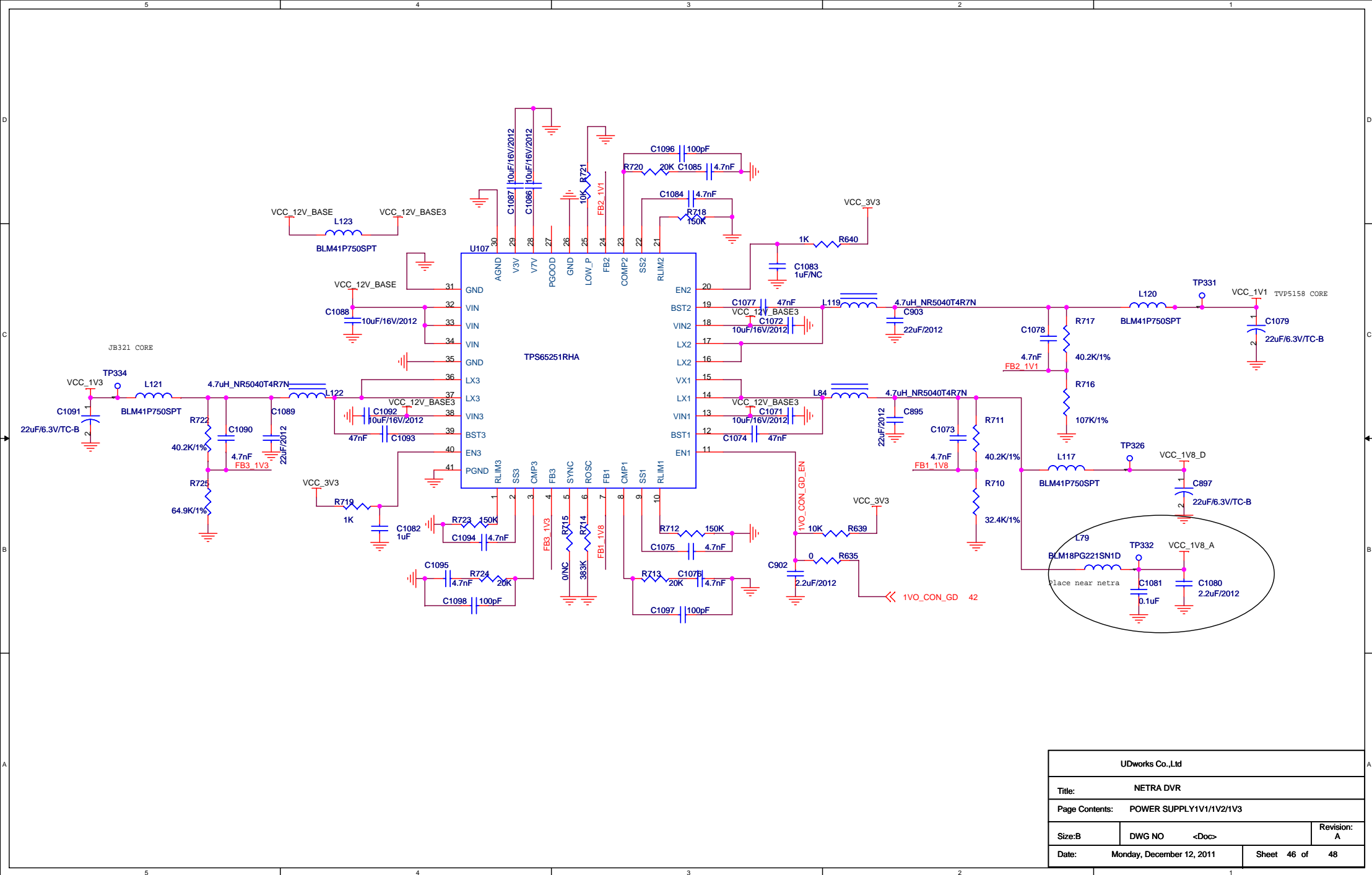


UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: #4 TVP5158			
Size: B	DWG NO	<Doc>	Revision: A
Date: Monday, December 12, 2011	Sheet 40 of 48		

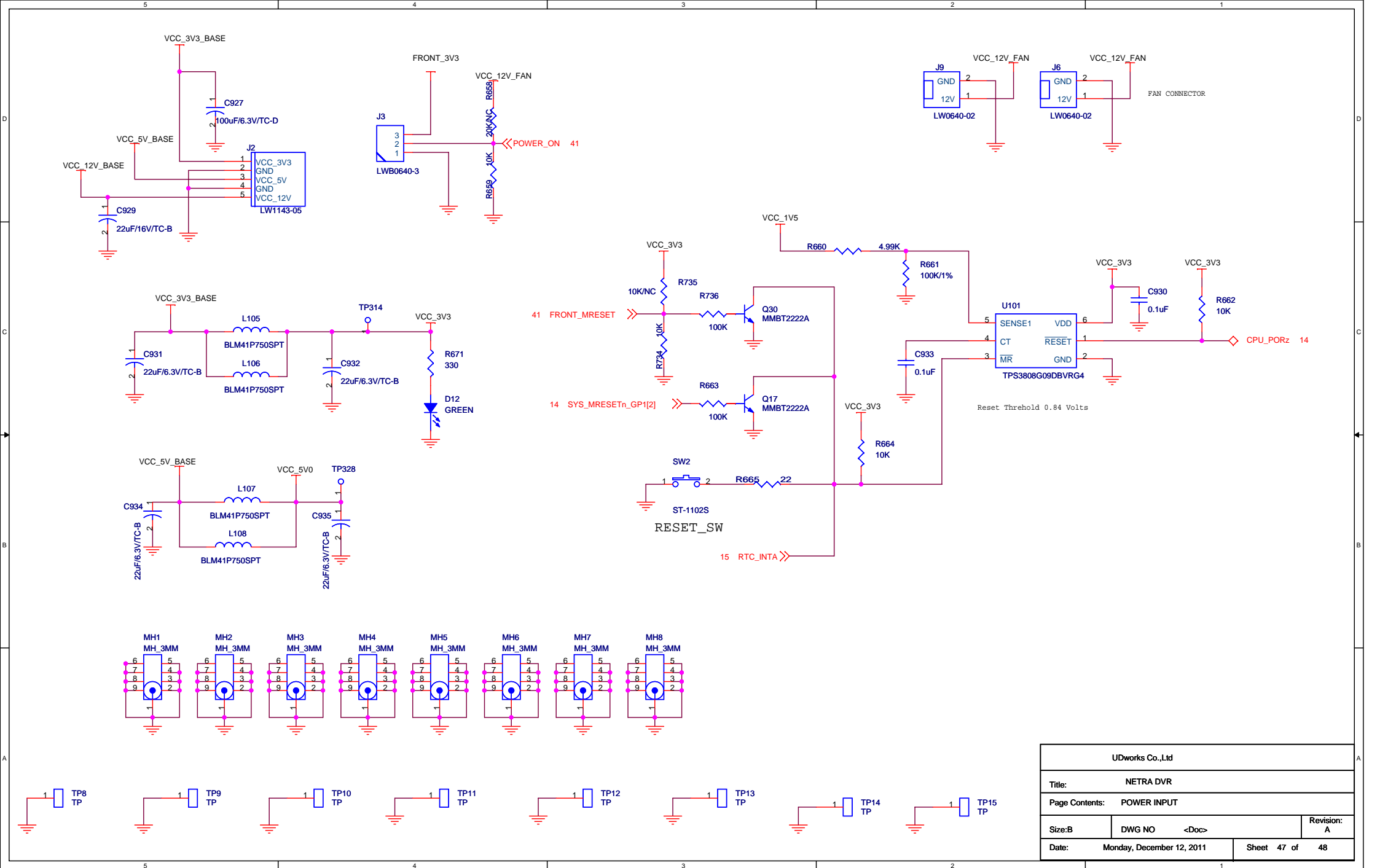


UDworks Co.,Ltd			
Title:		NETRA DVR	
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Size:B	DWG NO	<Doc>	Revision: A
Date:	Monday, December 12, 2011		Sheet 43 of 48

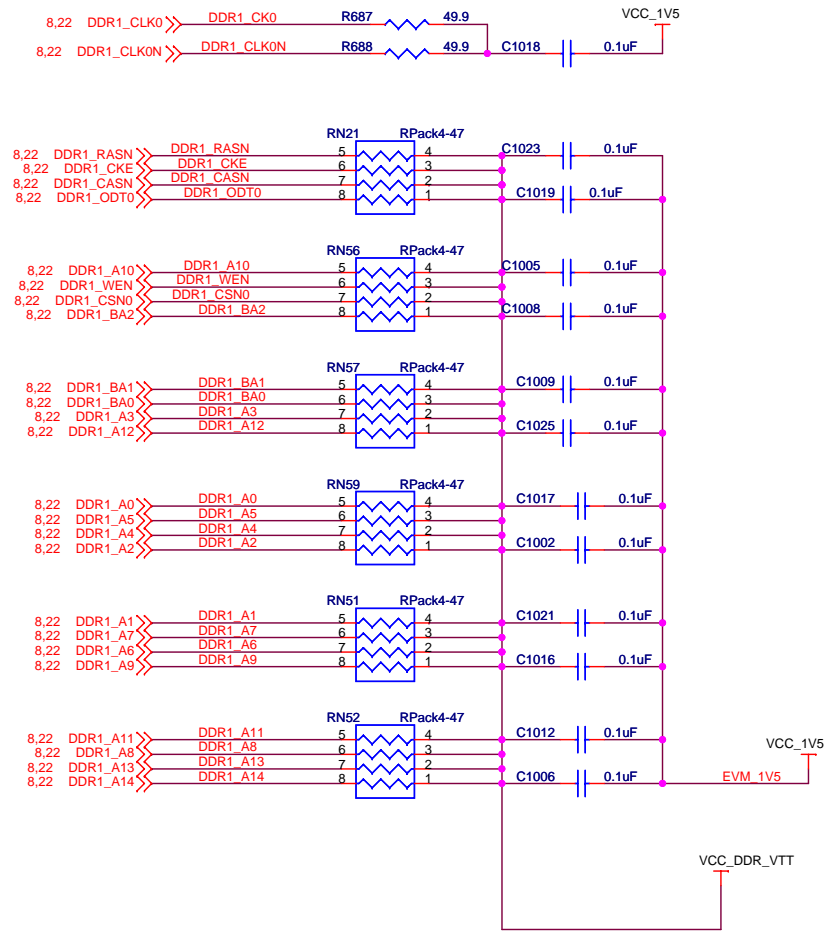
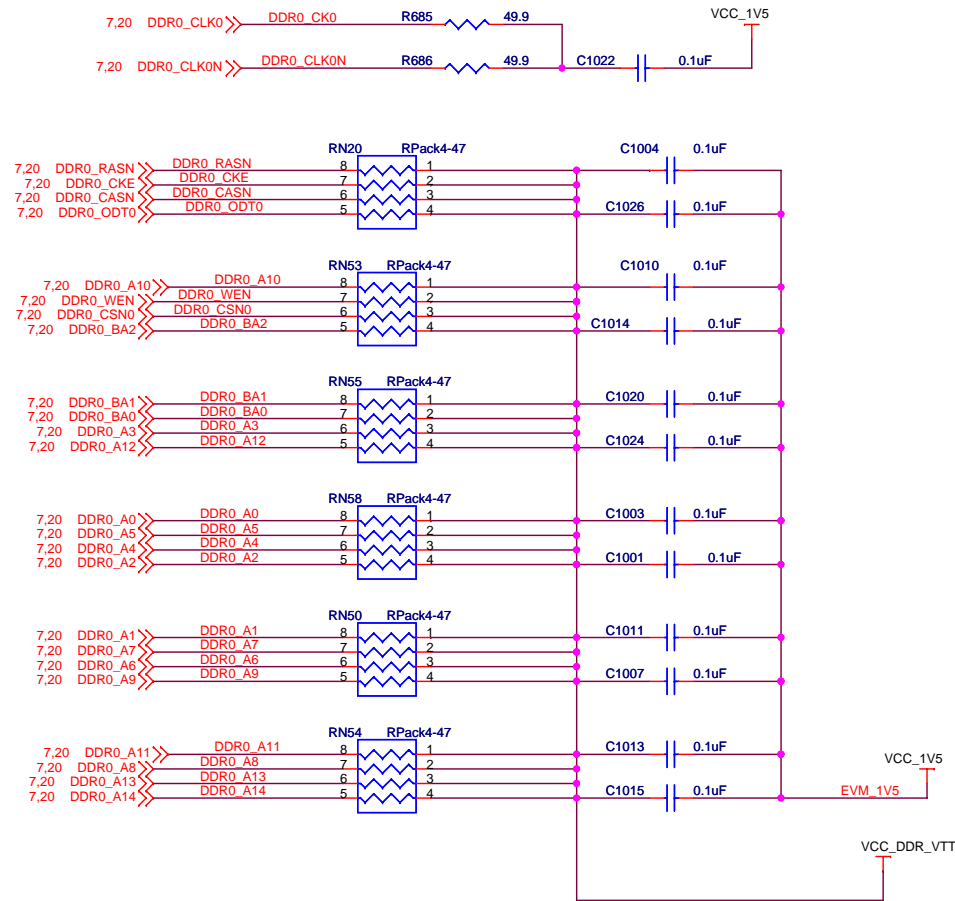




UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: POWER SUPPLY1V1/1V2/1V3			
Size:B	DWG NO <Doc>		Revision: A
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Title: NETRA DVR			
Page Contents: POWER INPUT			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Monday, December 12, 2011	Sheet 47 of	48



UDworks Co.,Ltd			
Title: NETRA DVR			
Page Contents: EMIF DDR0/1 DDR3 MEM			
Size:B	DWG NO	<Doc>	Revision: A
Date:	Monday, December 12, 2011	Sheet 48 of	48