DM8168 – DVR Reference Design

H/W USER GUIDE - Rev 0.6 (May 15th 2012)

--Preliminary

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Revision History (h/w)

Main board Version	Date	DVRRD H/W Revision History
Rev0.1	2010.08	Initial version
Rev0.2	2010. 12	Change DDR2 to DDR3 Modify some power circuit
Rev0.3	2011.02	SENSOR_IN1's GP number is changed.(GP0[3] -> GP1[26]) GP0[3] is tied to ground with pulled down resister
Rev0.3A	2011.05	1. Modify SATA port LED GPIO numbers 2. Modify the Video Sync separator input circuit on the VGA output port. 3. Modify filter setting on the Video Amp(THS7360) 4. Change power devices (1V0_CON) 5. Change 5158 AUDIO IF MODE to cascade mode (McASP interface). 6. Change the Ethernet PHY initial Mode (Auto-negotiation enable) to the 100Mbit mode for GIGABIT mode issue. 7. Change the Capacitor value 22uF to 47uF (or add 22uF) on the Ethernet PHY's internal power. 8. Add reset signal on the AIC3101 audio Codec. 9. Change the Nand Flash (K9F8GO8U0M : 1GByte) to K9F2GO8U0M(256MByte).
Rev0.4		1. Change power devices (1V0_AVS, VCC_1.8V, VCC_1.1V, VCC_1.3V)
Rev0.5	2011.09	1. Modify VTT power enable signal. 2. Modify sync signals of the RGB(VGA) output for future function. 3. Modify AC coupled capacitor value in the SATA port. 4. Change the ESD device in the USB port. 5. Change the TPS40400 PMBus address "00" to "70" (R706 : 10K -> 200K)

Main board Version	Date	DVRRD H/W Revision History
Rev0.5A	2011. 10	1. The eSATA port is changed to the SATA PM(JMB321) port1. 2. The Netra SATA0 port is changed to the ODD SATA port.
Rev0.5B	2011. 12	1. Add the signal for 1V0_con power enable. 2. Change value of components for the AVS power device.
Rev0.6	2012, 05	1. Modify value R644, R646 (100 ohm -> 22 ohm). 2. Modify power of the TPD7S019 (U112). 3. Add pull down 2.1kohm on the WD signal 4. Change value of components for the AVS power device

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1 DM8168 DVR Reference Design

The intention of this document is provide a single document from which user can get know how to use the DVRRD.

1.1 Hardware setup

1.1.1 DM8168 DVR RDK Package Contents

Figure 1. DM8168 DVR RDK Package Contents

1.1.2 DM8168 DVR RDK Front Panel

Figure 2. DM8168 DVR RDK front panel

POWER SWITCH

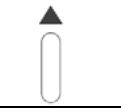
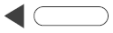
No.	Marking	Function1(Short Press)	Function2(Long Press)
0	⏻	Power On	Power Off

KEYPAD

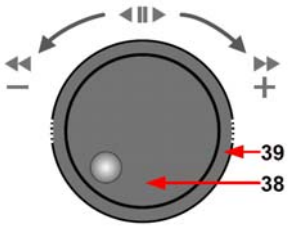
No.	Marking	Function1(Short Press)	Function2(Long Press)
1	1	Ch1 Camera Enable / Disable	
		Input character “1” in Text mode	
2	2	Ch2 Camera Enable / Disable	
		Input character “2” in Text mode	

3	3	Ch3 Camera Enable / Disable Input character “3” in Text mode	
4	4	Ch4 Camera Enable / Disable Input character “4” in Text mode	
5	5	Ch5 Camera Enable / Disable Input character “5” in Text mode	
6	6	Ch6 Camera Enable / Disable Input character “6” in Text mode	
7	7	Ch7 Camera Enable / Disable Input character “7” in Text mode	
8	8	Ch8 Camera Enable / Disable Input character “8” in Text mode	
9	9	Ch9 Camera Enable / Disable Input character “9” in Text mode	
10	10	Ch10 Camera Enable / Disable Input character “A” in Text mode	
11	11	Ch11 Camera Enable / Disable Input character “B” in Text mode	
12	12	Ch12 Camera Enable / Disable Input character “C” in Text mode	
13	13	Ch13 Camera Enable / Disable Input character “D” in Text mode	
14	14	Ch14 Camera Enable / Disable Input character “E” in Text mode	
15	15	Ch15 Camera Enable / Disable Input character “F” in Text mode	
16	16	Ch16 Camera Enable / Disable Input character “G” in Text mode	
17	LIVE	Change Live mode Input character “H” in Text mode	

18	SEARCH	Change Playback mode	
		Input character “I” in Text mode	
19	SCR	Change Screen Layout	
		Input character “J” in Text mode	
20	FULL	reserved	
		Input character “K” in Text mode	
21	PREV	Display for Previous camera	
		Input character “L” in Text mode	
22	NEXT	Display for Next camera	
		Input character “M” in Text mode	
23	SEQ	Change to camera automatically	
		Input character “N” in Text mode	
24	◀◀	Fast Rewind on playback	
		Input character “O” in Text mode	
25	⏮	Rewind on playback	
		Input character “P” in Text mode	
26	▶/II	Play or pause on playback	
		Input character “Q” in Text mode	
27	⏭	Forward on playback	
		Input character “R” in Text mode	
28	▶▶	Fast Forward on playback	
		Input character “S” in Text mode	
29	■	Stop on playback	
		Input character “T” in Text mode	
30	PTZ	reserved	PTZ is only supported by UI.
		Input character “U” in Text mode	
31	REC	Urgency Record	
		Input character “V” in Text mode	
32	SETUP	Call Setup Window	
		Input character “W” in Text mode	

33		Move Up	
34		Move Left Back space	
35		Select or Enter	
36		Move Right	
37		Move Down	

Jog Shuttle



No.	Marking	Function
38		JOG : Fast forward or Fast rewind on playback
39		SHUTTLE : playback speed control

Remote Control(option)

No.	Marking	Function
40		IR : Remote control(1)

USB PORT

No.	Marking	Function
41		USB 1 PORT (note: the lower port is reserved.)

ODD

No.	Marking	Function
42		Eject/Insert
43		DOOR : Media insert

LED

No.	Marking	Function
44		Power On Indicator
45		Record HDD Indicator
46		Network Connect Indicator

NOTE) (1) **not implemented.**

DM8168 DVR RDK Rear Port

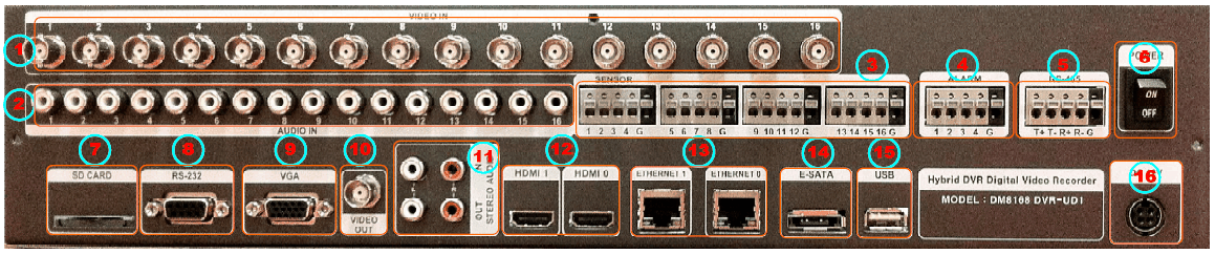


Figure 3. DM8168 DVR RDK Rear Port

No.	FUNCTION	No.	FUNCTION
1	Video input channel 1~16	9	VGA port
2	Audio input channel 1~16	10	Composite Video output
3	Sensor input(TTL LEVEL) ch1~16	11	Stereo Audio input / output
4	Alarm Output(NO,NC)-open collector ch1~4	12	HDMI output 2ports
5	RS-485 port	13	10/100/1000 Ethernet 2ports
6	DVR Main power switch	14	e-SATA Port
7	SD CARD interface port	15	USB Port
8	RS-232 port	16	DC 12V input

1.1.3 Installation DM8168 DVR RDK

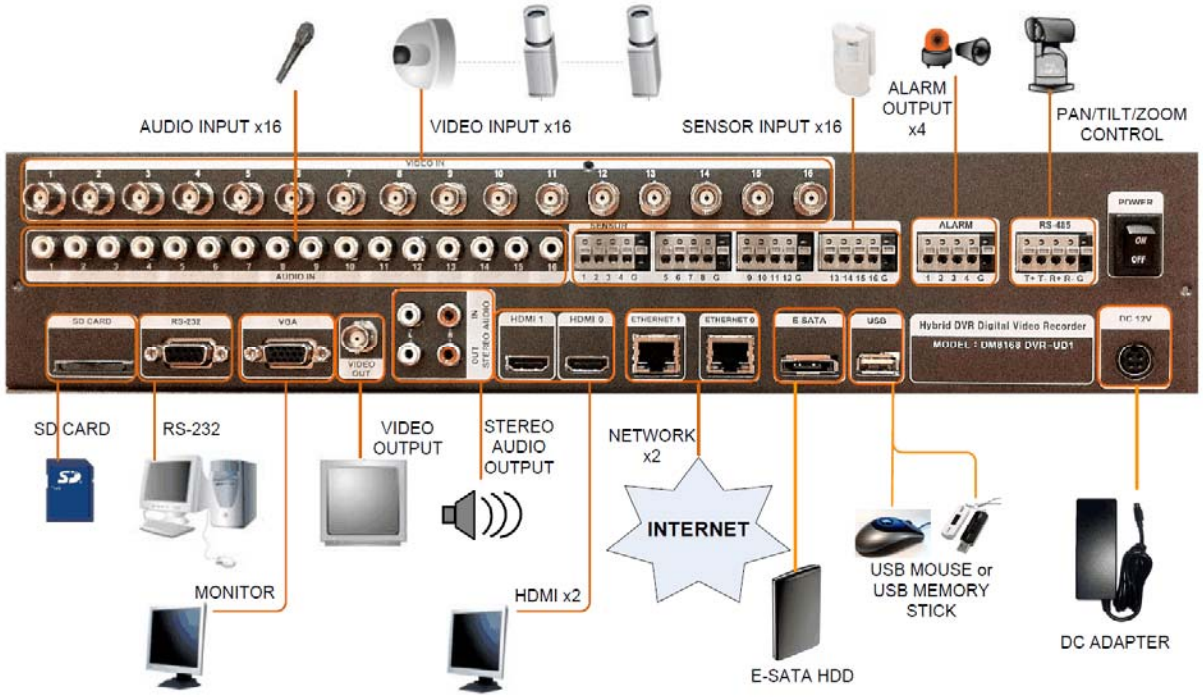


Figure 4. Installation DM8168 DVR RDK

1.2 INTRODUCTION

1.2.1 Features of the DVRRD

The DM8168 DVRRD is a standalone DVR reference Design for the TMS320DM8168 processor.

DVRRD Rev0.6 Block diagram

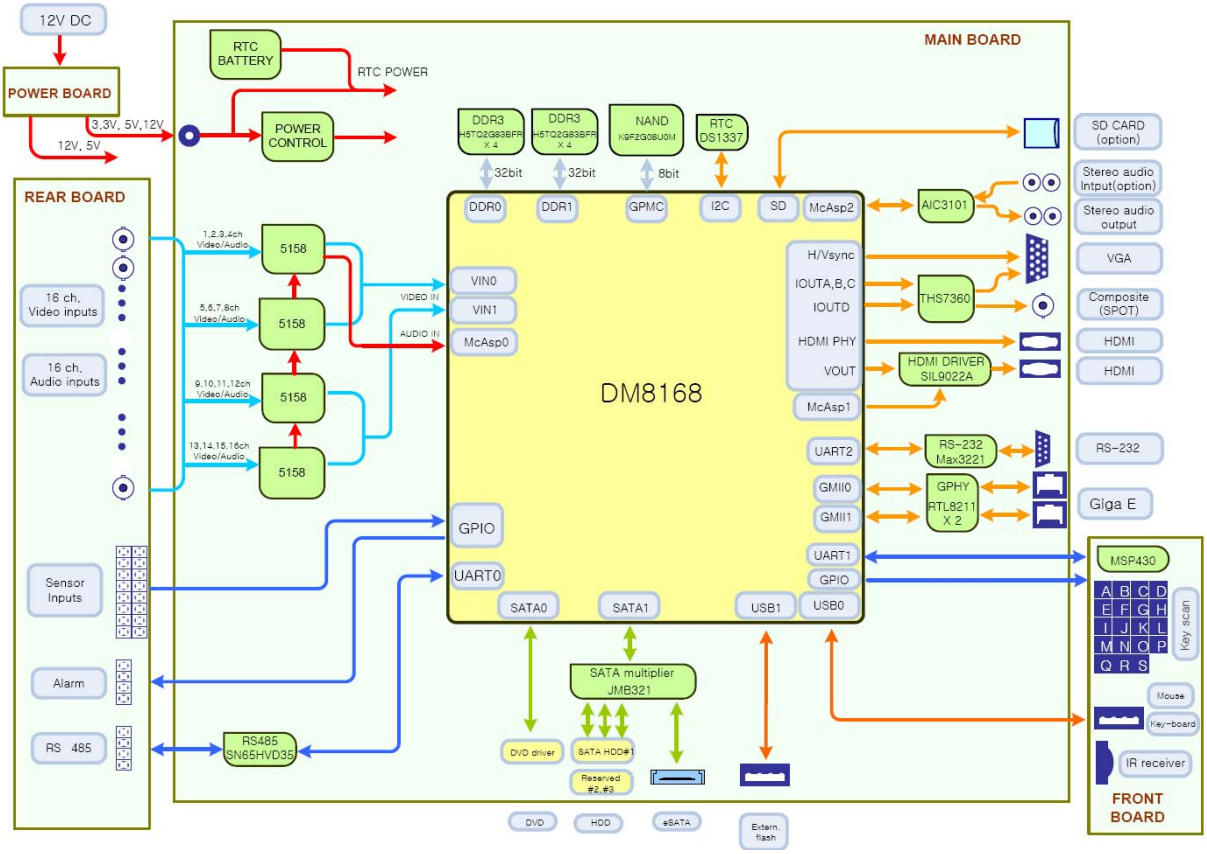


Figure 5. DVRRD Block diagram

key Features

- ❑ A Texas instruments TMS320DM8168 process with an ARM Cortex –A8 RISC MPU operating up to 1.2GHz, a C674x VLIW DSP (1GHz) and three programmable High-Definition Video Image Coprocessor (HDVICP2) Engine.
- ❑ Max 16 video input ports - composite.
- ❑ Video output – Composite, RGB (VGA monitor), HDMI 2PORTS.
- ❑ Up to 2GBytes of DDR3 DRAM
- ❑ 256Mbyte NAND Flash, 128Byte EEPROM.
- ❑ Max 16 Audio input port.
- ❑ RS-232 1port, RS-485 1port
- ❑ Sensor input 16ports, Alarm output 4ports
- ❑ 41 keys input
- ❑ USB 2.0 2-ports

- SATA interface 4 ports
- eSATA interface 1 port
- 10/100/1000 Ethernet interface 2 ports

1.2.1.1 Supplied Hardware

The DVRRD includes the following hardware items:

- DVRRD main board
- DVRRD front board (key pads, IR receiver, USB 1 port)
- DVRRD rear board(Video 16 input connector, Audio 16 input connector, sensor 16 input connector, alarm 4 port connector, rs-485 1port connector)
- DVRRD power board(output :3V, 5V, 5V, 12V
  Input : 12VDC)

1.2.1.2 Supplied Schematics files

The DVRRD includes the following schematics:

- DVRRD main board – Orcad(dsn file) and pdf(gerber file)
- DVRRD front board – Orcad(dsn file) and pdf(gerber file)
- DVRRD rear board – Orcad(dsn file) and pdf(gerber file)
- DVRRD power board – Orcad(dsn file) and pdf(gerber file)

1.3 Physical Description

1.3.1 Main Board

1.3.1.1 Board Layout

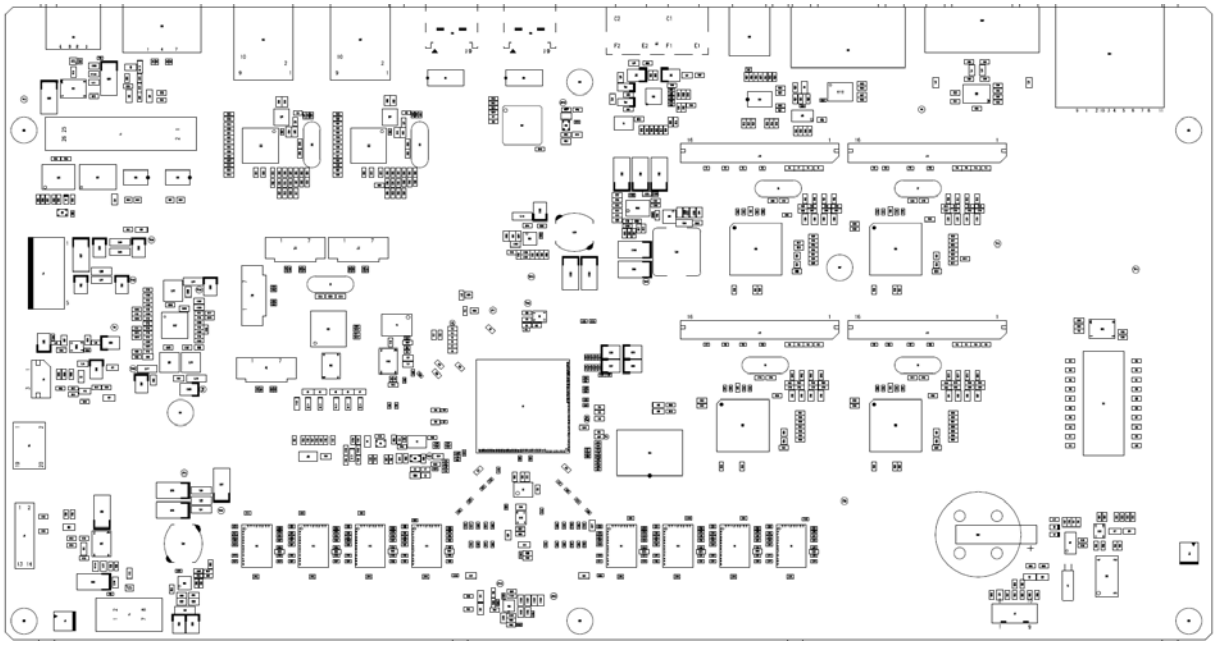


Figure 6. Main Board (Rev0.6) Layout Top side

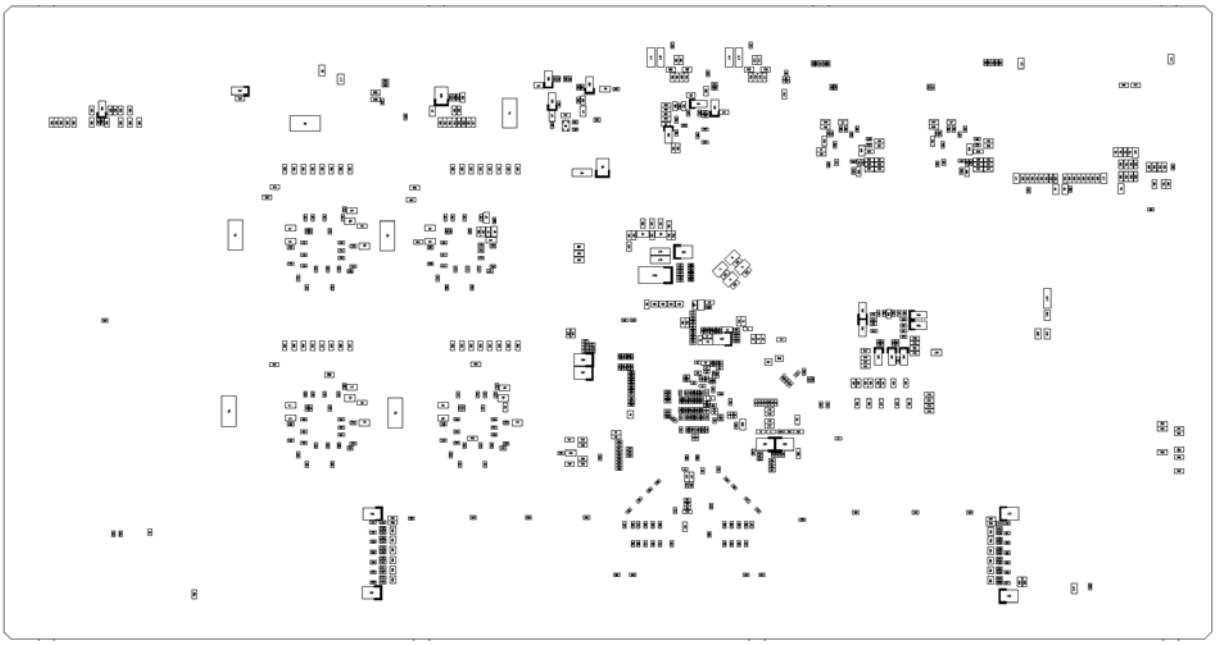
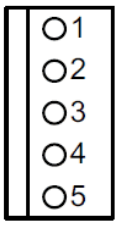


Figure 7. Main Board (Rev0.6) Layout Bottom side

1.3.1.2 Power

1.3.1.2.1 J2 (Power Connector)

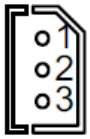


PIN#	Signal
1	3.3V
2	GND
3	5V
4	GND
5	12V

Figure 8. Power connector

J2 is connected to Power Board (J1) via cable.

1.3.1.2.2 J3 (Power Control Connector)

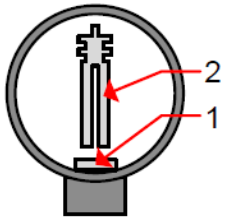


PIN#	Signal
1	GND
2	POWER_ON
3	FRONT_3V3

Figure 9. Power control

J3 is connected to Power Board(J6) via cable.
Power board is controlled by Front power switch thru J3 connector.

1.3.1.2.3 BHT1 (Battery Holder)

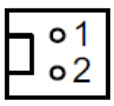


PIN#	Signal
1	3V
2	GND

Figure 10. Battery holder

BHT1 provides backup power to the RTC(U7:DS1337) when the power is not applied to the main board.

1.3.1.2.4 J6, J9 (Case Fan Power Connector)



PIN#	Signal
1	GND
2	12V

Figure 11. Case fan power

J6, J9 are connected to Case Fan via cable.

1.3.1.2.5 SW1(Boot Mode Switch)

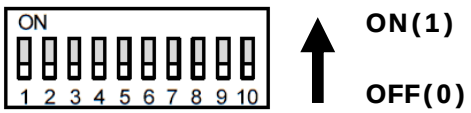


Figure 12. Boot Mode switch

SW1 boot terminal signal function

SW1 NUMBER	SIGNAL NAME	DESCRIPTION
1	BTMODE[0]	Boot Mode Selection pins
2	BTMODE[1]	
3	BTMODE[2]	
4	BTMODE[3]	
5	BTMODE[4]	
6	CS0MUX[0]	GPMC CS0 default Address/Data multiplexing mode. 00 = Not multiplexed 01 = A/D muxed 10 = A/A/D muxed 11 = Reserved
7	CS0MUX[1]	
8	CS0BW	GPMC CS0 default Data bus Width input. 0 = 8bit data bus 1 = 16bit data bus
9	CS0WAIT	GPMC CS0 default GPMC Wait enable input. 0 = Wait disabled 1 = Wait enabled
10	NOT USED	

Boot Mode function table is as follows.

BTM [4]	BTM [3]	BTM[2]	BTM[1]	BTM[0]	First	Second	Third	Fourth
0	0	0	0	1	UART2	XIP w/WAIT	MMC	SPI
0	0	0	1	0	UART2	SPI	NAND	NANDI2C
0	0	0	1	1	UART2	SPI	XIP	MMC
0	0	1	0	0	EMAC	SPI	NAND	NANDI2C
0	0	1	1	1	EMAC	MMC	SPI	XIP
0	1	0	0	0	PCIE_32			
0	1	0	0	1	PCIE_64			
0	1	1	1	1	GP Fast Ext.	UART	EMAC	PCIE_64
1	0	0	0	0	XIP	UART	EMAC	MMC
1	0	0	0	1	XIP w/WAIT	UART	EMAC	MMC
1	0	0	1	0	NAND	NANDI2C	SPI	UART
1	0	0	1	1	NAND	NANDI2C	MMC	UART
1	0	1	0	0	NAND	NANDI2C	SPI	EMAC
1	0	1	0	1	NANDI2C	MMC	EMAC	UART
1	0	1	1	0	SPI	MMC	UART	EMAC
1	0	1	1	1	MMC	SPI	UART	EMAC
1	1	0	0	0	SPI	MMC	PCIE_32	
1	1	0	0	1	SPI	MMC	PCIE_64	
1	1	1	1	1	GP Fast Ext	EMAC	UART	PCIE_32

1.3.1.2.6 SW2(RESET Switch)

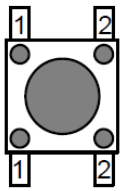


Figure 13. Reset switch

SW2 is a push button switch that will reset DM8168.

1.3.1.3 JTAG Interface

1.3.1.3.1 J5 (14 pin JTAG Connector)

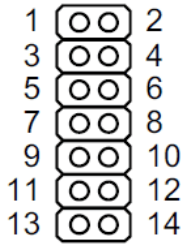


Figure 14. 14Pin JTAG Interface

PIN#	Signal	PIN#	Signal
1	TMS	2	TRSTn
3	TDI	4	TDIS(GND)
5	TVD(VCC_3V3)	6	KEY(NC)
7	TDO	8	GND
9	TCKRTN	10	GND
11	TCLK	12	GND
13	EMU0	14	EMU1

When using this type JTAG controller, assert TRSTn to initialize the device after power up and externally drive TRSTn high before attempting any emulation or boundary scan operations.
Following the release of RESETn, the low-to-high transition of TRSTn must be seen to latch of EMU1 and EMU0.
By Default JTAG MODE is configured to ICE PICK MODE.(EMU[1:0]="11")

1.3.1.3.2 J4 (20 pin ARM JTAG Interface, reserved)

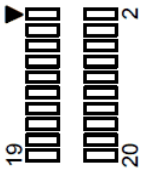


Figure 15. 20pin ARM JTAG Interface

PIN#	Signal	PIN#	Signal
1	TMS	2	TRSTn
3	TDI	4	GND
5	VCC_3V3	6	NC
7	TDO	8	GND
9	RTCK	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1
15	EMU_RSTn	16	GND
17	EMU2	18	EMU3
19	EMU4	20	GND

1.3.1.4 Video and Audio Input

1.3.1.4.1 J10, J11, J12, J13 (Analog Video and Audio Input)

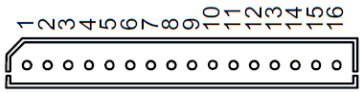


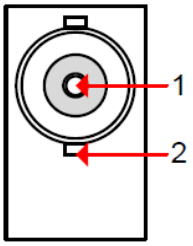
Figure 16. Analog Video and Audio Input

PIN#	J10 Signal	J11 Signal	J12 Signal	J13 Signal
1	AGND	AGND	AGND	AGND
2	AUDIO_IN4	AUDIO_IN8	AUDIO_IN12	AUDIO_IN16
3	AUDIO_IN3	AUDIO_IN7	AUDIO_IN11	AUDIO_IN15
4	AUDIO_IN2	AUDIO_IN6	AUDIO_IN10	AUDIO_IN14
5	AUDIO_IN1	AUDIO_IN5	AUDIO_IN9	AUDIO_IN13
6	AGND	AGND	AGND	AGND
7	AGND	AGND	AGND	AGND
8	VIDEO_IN1	VIDEO_IN5	VIDEO_IN9	VIDEO_IN13
9	VIDEO_IN1_AGND	VIDEO_IN5_AGND	VIDEO_IN9_AGND	VIDEO_IN13_AGND
10	VIDEO_IN2	VIDEO_IN6	VIDEO_IN10	VIDEO_IN14
11	VIDEO_IN2_AGND	VIDEO_IN6_AGND	VIDEO_IN10_AGND	VIDEO_IN14_AGND
12	VIDEO_IN3	VIDEO_IN7	VIDEO_IN11	VIDEO_IN15
13	VIDEO_IN3_AGND	VIDEO_IN7_AGND	VIDEO_IN11_AGND	VIDEO_IN15_AGND
14	VIDEO_IN4	VIDEO_IN8	VIDEO_IN12	VIDEO_IN16
15	VIDEO_IN4_AGND	VIDEO_IN8_AGND	VIDEO_IN12_AGND	VIDEO_IN16_AGND
16	AGND	AGND	AGND	AGND

J10, J11, J12 and J13 are interfaced to the TVP5158.
Each connector is connected to Rear board(J1,J2,J3 and J4) via cable.

1.3.1.5 Video and Audio Out

1.3.1.5.1 CN8 (Composite Output)



PIN#	Signal
1	Composite Video signal
2	GND

Figure 17. Composite video out

Composite video output with BNC connector.

1.3.1.5.2 CN7 (VGA, DSUB-15PIN)

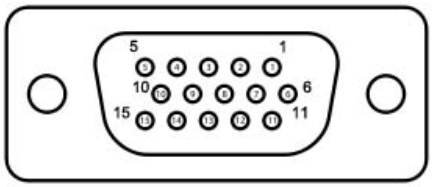


Figure 18. VGA output

PIN#	Signal	Description	PIN#	Signal	Description
1	DAC_ROUT	RED	9	NC	
2	DAC_GOUT	GREEN	10	GND	SYNC GND
3	DAT_BOUT	BLUE	11	NC	
4	NC		12	NC	
5	GND	GND	13	HSYNC_OUT	HSYNC
6	GND	RED GND	14	VSYNC_OUT	VSYNC
7	GND	GREEN GND	15	NC	
8	GND	BLUE GND			

Connect this video output to monitor so that live, playback pictures would be monitored.

1.3.1.5.3 CN5, CN6 (2 Ports HDMI Output)

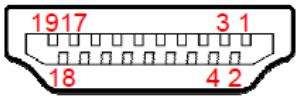


Figure 19. HDMI output

PIN#	Signal	Description	PIN#	Signal	Description
1	D2+	TMDS Data2+	11	CK SHIELD	TMDS Clock Shield
2	D2 SHIELD	TMDS Data2 Shield	12	CK-	TMDS Clock-
3	D2-	TMDS Data2-	13	CE REMOTE	CEC(control)
4	D1+	TMDS Data1+	14	NC.14	Reserved(N.C. on device)
5	D1 SHIELD	TMDS Data1 Shield	15	DDC CLK	SCL(DDC clock)
6	D1-	TMDS Data1-	16	DDC DATA	SDA(DDC data)
7	D0+	TMDS Data0+	17	GND	DDC/CEC Ground
8	D0 SHIELD	TMDS Data0 Shield	18	+5V	+5 V Power
9	D0-	TMDS Data0-	19	HP DET	Hot Plug Detect
10	CK+	TMDS Clock+			

1.3.1.5.4 CN7 (AUDIO In/Out, 4Ports RCA Connector)

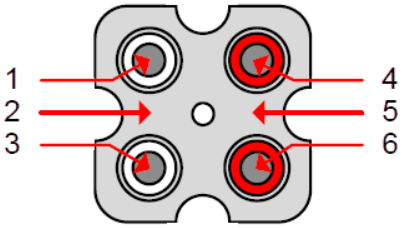


Figure 20. Audio interface

PIN#	Signal	Description
1	F1	AUDIO IN LEFT
2	C1	GND
3	E1	AUDIO OUT LEFT
4	F2	AUDIO IN RIGHT
5	C2	GND
6	E2	AUDIO OUT RIGHT

1.3.1.6 Communication Interface

1.3.1.6.1 CN3, CN4 (2 Ports Ethernet, RJ45 Jack)

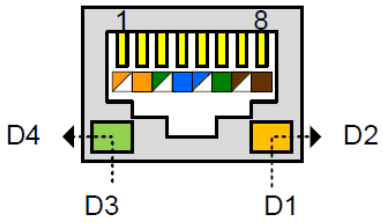


Figure 21. Ethernet Interface(RJ45)

PIN#	Signal	Description
1	TPFOP	TXP
2	TPFON	TXN
3	TPFIP	RXP
4		
5		
6	TPFIN	RXN
7		
8		
D1	3.3V	LED POWER
D2	ACT	Green LED control
D3	3.3V	LED POWER
D4	LINK	Yellow LED control

CN3 and CN4 are interfaced to each Ethernet PHY chip U36 and U37.
Connect an Ethernet cable with RJ45 jack to the DVR connector.
ACT LED indicate that there is transmit or receive activity after Link UP.
LINK LED will be off when link is failed.

1.3.1.6.2 CN10 (RS-232 Connector, DB-9)

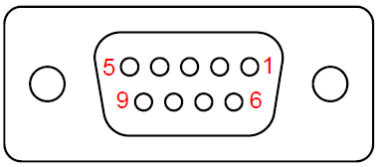


Figure 22. RS-232 Interface

PIN#	Signal
1	
2	TXD
3	RXD
4	
5	GND
6	
7	
8	
9	

DM8168's UART2 is used for console Port(RS-232) true DB-9 connector, CN10.

1.3.1.7 USB Interface

1.3.1.7.1 CN1 (Rear panel USB, USB A-Type Single)

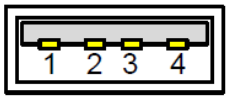


Figure 23. USB Interface

PIN#	Signal	Description
1	USB_P2	5V
2	USB_DM1	DM(DSPORT 1)
3	USB_DP1	DP(DSPORT 1)
4	VUSB_GND	GND

1.3.1.7.2 J7(Front panel USB, 8pin Headerbox)

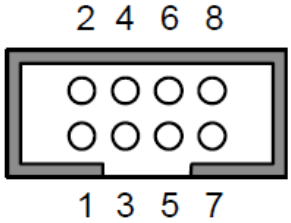


Figure 24. Front USB Interface

PIN#	Signal	Description
1	NC	
2	USB0_VBUS_CON	+5V
3	NC	
4	USB0_DM	DM
5	NC	
6	USB0_DP	DP
7	GND	
8	GND	GND

J7 is connected to front board(J6) via cable.

1.3.1.8 Storage Interface

1.3.1.8.1 J14, J15, J16, J17 (4 SATA Ports)

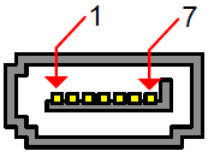


Figure 25. SATA Interface

PIN#	J14 Signal SATA Port0	J15 Signal ODD SATA Port	J16 Signal SATA Port2	J17 Signal SATA Port3	Description
1	GND	GND	GND	GND	GND
2	TXP0	TXP0(DM8168)	TXP2	TXP3	SATA TXP0,2,3(JMB321)
3	TXN0	TXN1(DM8168)	TXN2	TXN3	SATA TXN0,2,3(JMB321)
4	GND	GND	GND	GND	GND
5	RXN0	RXN1(DM8168)	RXN2	RXN3	SATA RXN0,2,3(JMB321)
6	RXP0	RXP1(DM8168)	RXP2	RXP3	SATA RXP0,2,3(JMB321)
7	GND	GND	GND	GND	GND

J14, J15, J16 and J17 are connected to SATA HDD/ODD via cable.

1.3.1.8.2 CN2 (eSATA, SATA PORT1 of JMB321)

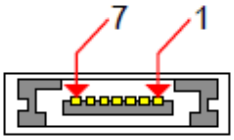


Figure 26. E-SATA Interface

PIN#	Signal	Description
1	GND	GND
2	SATA_TXP1	SATA TXP1(JMB321)
3	SATA_TXN1	SATA TXN1(JMB321)
4	GND	GND
5	SATA_RXN1	SATA RXN1(JMB321)
6	SATA_RXP1	SATA RXP1(JMB321)
7	GND	GND

CN2 is connected to SATA port1 of the JMB321.

1.3.1.8.3 CN11 (SD CARD)

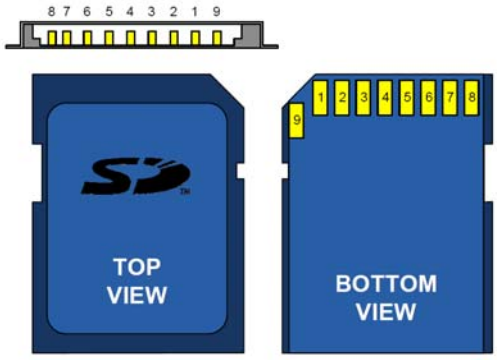


Figure 27. SD Card Interface and SD Storage

PIN#	Signal	Description
1	CD/DAT3	Card detection / Connector data line 3
2	CMD	Command/Response line
3	Vss1	GND
4	Vdd	Power supply
5	CLK	Clock
6	Vss2	GND
7	DAT0	Connector data line 0
8	DAT1	Connector data line 1
9	DAT2	Connector data line 2

CN11 is the connector for SD Storage.

1.3.1.9 Front board Interface

1.3.1.9.1 J8(10Pin 2mm Headerbox)

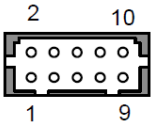


Figure 28. Front board Interface

PIN#	Signal	Description
1	nPWR_OFF	Main power on/off input
2	GND	GND
3	NC	Reserved
4	FRONT_TXD	Front board UART TXD
5	FRONT_RXD	Front board UART RXD
6	GND	GND
7	GP1[21]	PWR_SHUTDOWN_READY
8	MRESET	MAIN RESET(reserved)
9	FRONT_3V3	+3.3V Output to Front board
10	ETH_ACT	Ethernet Active indicator signal

J8 is connected to Front Board (J5) via cable.

1.3.1.10 Rear board Interface

1.3.1.10.1 J1(26Pin Headerbox)

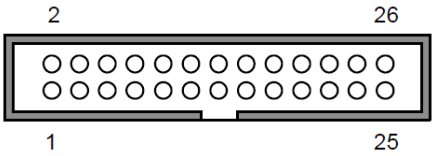


Figure 29. Rear board Interface

PIN#	Signal	Description	PIN#	Signal	Description
1	SENSOR IN1	Sensor Input 1	2	SENSOR IN2	Sensor Input 2
3	SENSOR IN3	Sensor Input 3	4	SENSOR IN4	Sensor Input 4
5	SENSOR IN5	Sensor Input 5	6	SENSOR IN6	Sensor Input 6
7	SENSOR IN7	Sensor Input 7	8	SENSOR IN8	Sensor Input 8
9	SENSOR IN9	Sensor Input 9	10	SENSOR IN10	Sensor Input 10
11	SENSOR IN11	Sensor Input 11	12	SENSOR IN12	Sensor Input 12
13	SENSOR IN13	Sensor Input 13	14	SENSOR IN14	Sensor Input 14
15	SENSOR IN15	Sensor Input 15	16	SENSOR IN16	Sensor Input 16
17	ALARM OUT1	Alarm out 1	18	ALARM OUT2	Alarm out 2
19	ALARM OUT3	Alarm out 3	20	ALARM OUT4	Alarm out 4
21	TX+	RS485 TX+	22	TX-	RS485 TX-
23	RX+	RS485 RX+	24	RX-	RS485 RX-
25	GND	GND	26	GND	GND

J1 is connected to Rear board (J5) via cable.

1.3.2 Front board

1.3.2.1 Board Layout

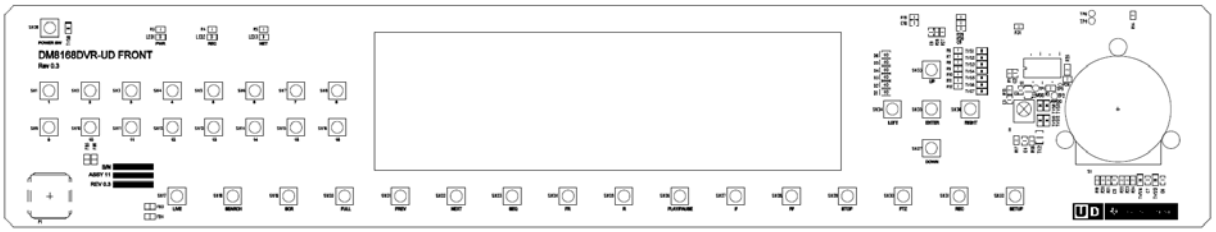


Figure 30. Front Board(Rev0.3) Layout Top Side

Figure 31. Front Board(Rev0.3) Layout Bottom side

1.3.2.2 KEY Matrix

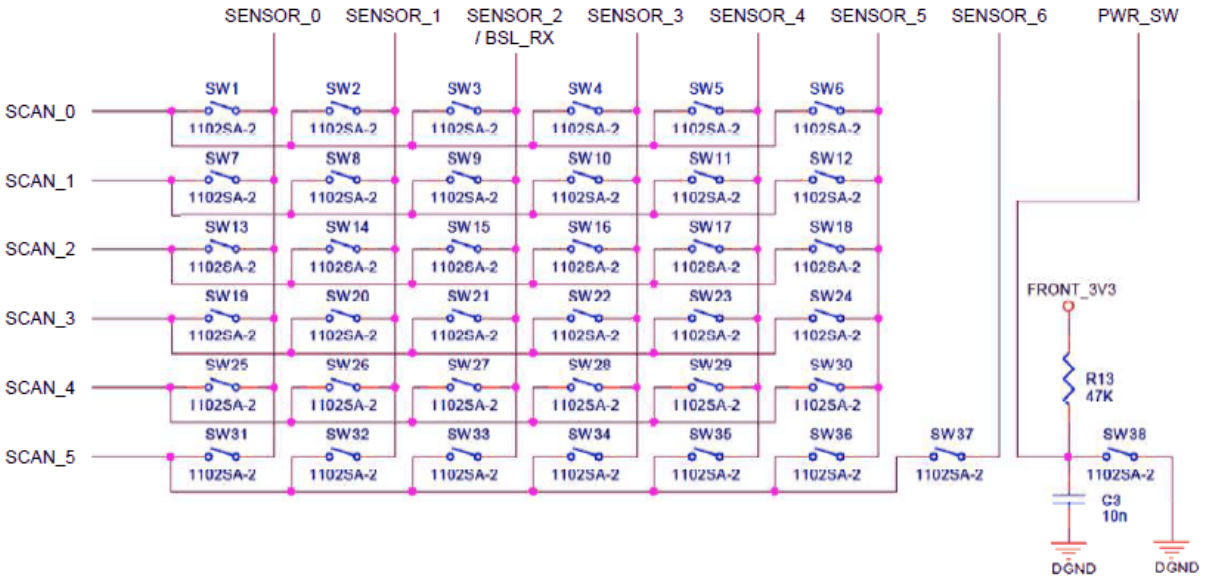


Figure 32. Front board key matrix circuit.

1.3.2.3 Power Jumper

1.3.2.3.1 J2(power input select)

Figure 33. Front board power select jumper

PIN#	Signal	Description
1	FRONT_3V3	Front board +3.3V
2	VCC_TOOL	VCC from Tool

Front board can be supplied 3.3V by a MSP430 Emulation Tool when Main board doesn't supply 3.3V.

1.3.2.4 Debug Interface

1.3.2.4.1 J3(Spy-Bi-Wire and BSL)

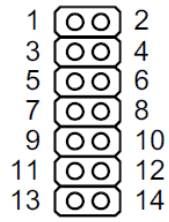


Figure 34. Front board debug interface

PIN#	Signal	PIN#	Signal
1	SBWTDIO	2	VCC_TOOL
3	NC	4	NC
5	NC	6	NC
7	SBWTCK	8	TEST
9		10	
11		12	BSL_TX
13		14	BSL_RX

J3 is MSP-FET430UIF flash emulation tool interface connector for MSP430.

1.3.2.5 Main Board Interface

1.3.2.5.1 J5 (Main board control interface)

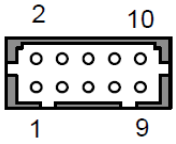


Figure 35. Main board control interace

PIN#	Signal	Description
1	MAIN_PWR_ON	Main board power on
2	GND	GND
3	NC	Reserved
4	FRONT_TXD	Front board UART TXD
5	FRONT_RXD	Front board UART RXD
6	GND	GND
7	PWR_SHUTDOWN_READY	Power shutdown ready
8	GIO	General I/O(reserved)
9	FRONT_3V3	+3.3V Output to Front board
10	ETH_ACT	Ethernet Active

J5 is connected to Main Board(J8) via cable.

1.3.2.6 USB Interface

1.3.2.6.1 J6 (Main board USB Interface, 8Pin Headerbox)

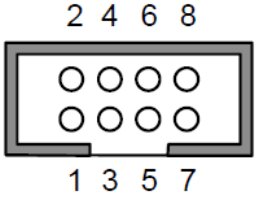


Figure 36. Front board USB Interface from main board

PIN#	Signal	PIN#	Signal(Reserved)
1	USB_P1	2	USB_P2
3	USB_DM1	4	USB_DM2
5	USB_DP1	6	USB_DP2
7	VUSB_GND	8	VUSB_GND

J6 is connected to main board(J7) via cable.

1.3.2.6.2 P1(Dual Port USB Connector)

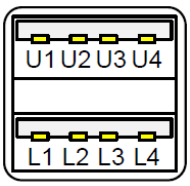


Figure 37. Dual port USB connector

PIN#	Signal	Description	Port
U1	USB_P1	5V	TOP
U2	USB_DM1	DM(DSPORT 1)	
U3	USB_DP1	DP(DSPORT 1)	
U4	VUSB_GND	GND	
L1	USB_P2	5V	Bottom (reserved)
L2	USB_DM2	DM(DSPORT 2)	
L3	USB_DP2	DP(DSPORT 2)	
L4	VUSB_GND	GND	

P1 is for the USB Device like USB mouse.

1.3.3 Rear Board

1.3.3.1 Board Layout

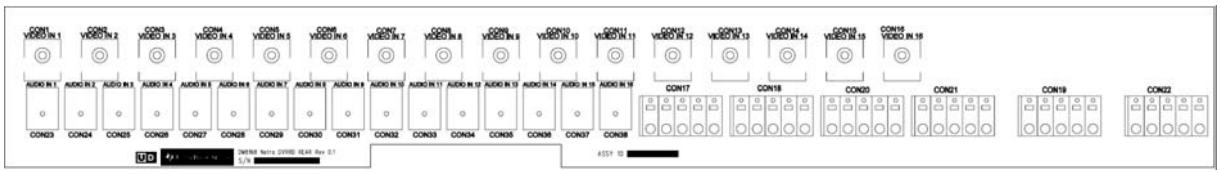


Figure 38. Rear Board(Rev0.1) Layout Top Side

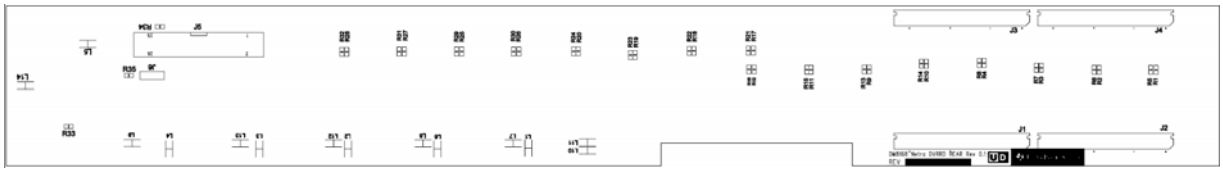


Figure 39. Rear Board(Rev0.1) Layout Bottom Side

1.3.3.2 Main Board Interface

1.3.3.2.1 J1, J2, J3, J4 (Main board Video and Audio Interface)

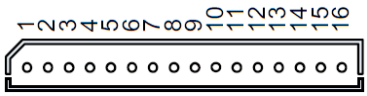


Figure 40. Main board video and audio interface

PIN#	J1 Signal	J2 Signal	J3 Signal	J4 Signal
1	AGND	AGND	AGND	AGND
2	AUDIO_IN4	AUDIO_IN8	AUDIO_IN12	AUDIO_IN16
3	AUDIO_IN3	AUDIO_IN7	AUDIO_IN11	AUDIO_IN15
4	AUDIO_IN2	AUDIO_IN6	AUDIO_IN10	AUDIO_IN14
5	AUDIO_IN1	AUDIO_IN5	AUDIO_IN9	AUDIO_IN13
6	AGND	AGND	AGND	AGND
7	AGND	AGND	AGND	AGND
8	VIDEO_IN1	VIDEO_IN5	VIDEO_IN9	VIDEO_IN13
9	VIDEO_IN1_AGND	VIDEO_IN5_AGND	VIDEO_IN9_AGND	VIDEO_IN13_AGND
10	VIDEO_IN2	VIDEO_IN6	VIDEO_IN10	VIDEO_IN14
11	VIDEO_IN2_AGND	VIDEO_IN6_AGND	VIDEO_IN10_AGND	VIDEO_IN14_AGND
12	VIDEO_IN3	VIDEO_IN7	VIDEO_IN11	VIDEO_IN15
13	VIDEO_IN3_AGND	VIDEO_IN7_AGND	VIDEO_IN11_AGND	VIDEO_IN15_AGND
14	VIDEO_IN4	VIDEO_IN8	VIDEO_IN12	VIDEO_IN16
15	VIDEO_IN4_AGND	VIDEO_IN8_AGND	VIDEO_IN12_AGND	VIDEO_IN16_AGND
16	AGND	AGND	AGND	AGND

J1, J2, J3 and J4 are each connected to main board (J10, J11, J12 and J13) via cable.

1.3.3.2.2 J5 (Main board Sensor, Alarm, RS-485 Interface, 26Pin Headerbox)

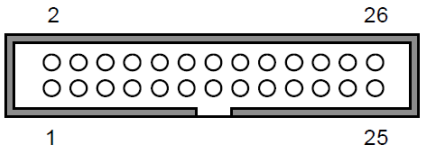
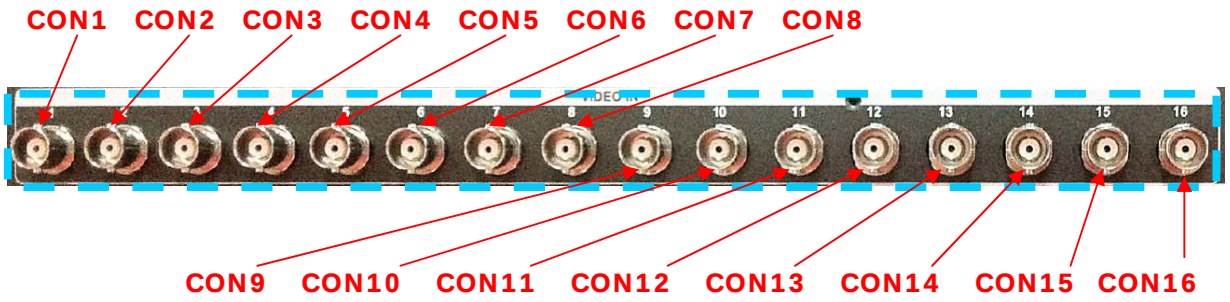


Figure 41. Main board Sensor, Alarm, RS-485 Interface

PIN#	Signal	Description	PIN#	Signal	Description
1	SENSOR IN1	Sensor Input 1	2	SENSOR IN2	Sensor Input 2
3	SENSOR IN3	Sensor Input 3	4	SENSOR IN4	Sensor Input 4
5	SENSOR IN5	Sensor Input 5	6	SENSOR IN6	Sensor Input 6
7	SENSOR IN7	Sensor Input 7	8	SENSOR IN8	Sensor Input 8
9	SENSOR IN9	Sensor Input 9	10	SENSOR IN10	Sensor Input 10
11	SENSOR IN11	Sensor Input 11	12	SENSOR IN12	Sensor Input 12
13	SENSOR IN13	Sensor Input 13	14	SENSOR IN14	Sensor Input 14
15	SENSOR IN15	Sensor Input 15	16	SENSOR IN16	Sensor Input 16
17	ALARM OUT1	Alarm out 1	18	ALARM OUT2	Alarm out 2
19	ALARM OUT3	Alarm out 3	20	ALARM OUT4	Alarm out 4
21	TX+	RS485 TX+	22	TX-	RS485 TX-
23	RX+	RS485 RX+	24	RX-	RS485 RX-
25	GND	GND	26	GND	GND

J5 is connected to main board (J1) via cable.

1.3.3.3 Video In

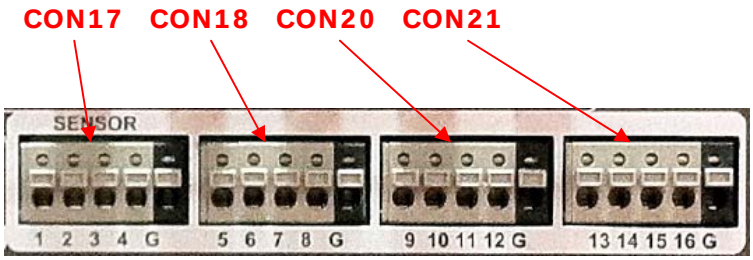


CON1~CON16 is video signals input with BNC jack.
Connectors are connected to Main board video input interface(TVP5158 Video input).

1.3.3.4 Audio In

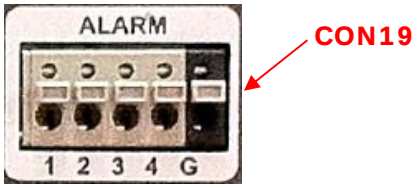
CON23~CON38 are audio signals input with RCA jack.
Audio signals are connected to Main Board (J10, J11, J12 and J13) via rear board (J1, J2, J3 and J4).

1.3.3.5 Sensor In



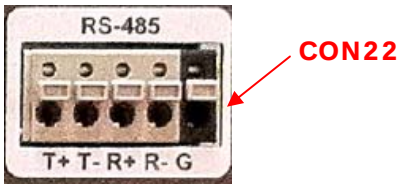
External devices event signal is connected to sensor input.
Mechanical or electrical switches can be wired to the sensor Inputs and GND connectors.
SENSOR_IN signals are connected to Main Board (J1) via rear board (J5).

1.3.3.6 Alarm out



The DVR system signals can be connected to external system for alarm events.
ALRAM_OUT signals are connected to Main Board(J1) via rear board(J5).

1.3.3.7 RS 485



The RS485 interfcace can be used to control PTZ(PAN, TILT, ZOOM) cameras.
RS485 signal is connected to Main Board(J1) via rear board(J5).

1.3.4 Power Board

1.3.4.1 Board Layout

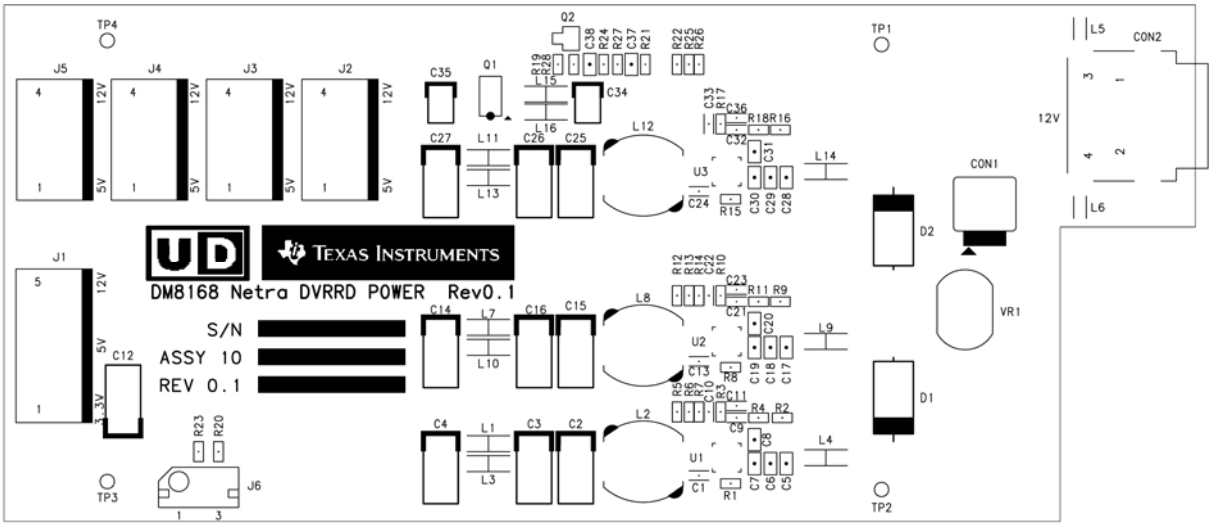


Figure 42. Power Board (Rev0.1) Layout Top Side

Figure 43. Power Board (Rev0.1) Layout Bottom Side

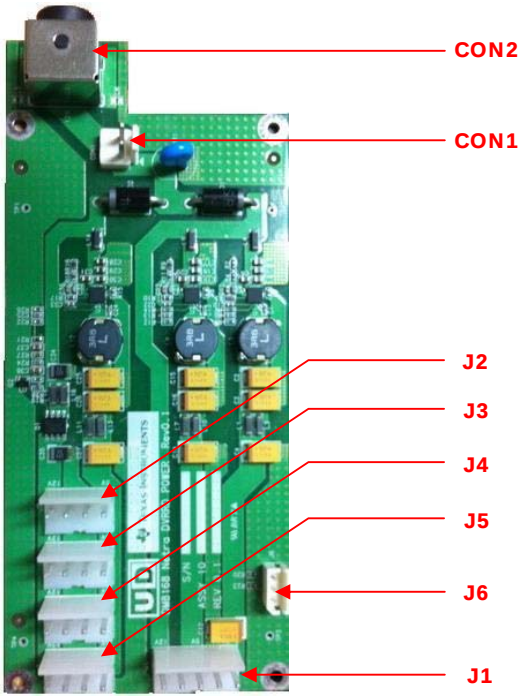


Figure 44. Power Board Picture

1.3.4.2 Power Input

1.3.4.2.1 CON2 (Adapter Input Connector)

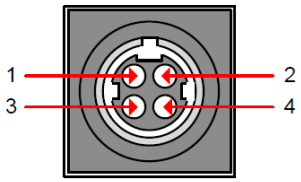


Figure 45. +12V Adapter connector of Power board

PIN#	Signal
1	12V
2	12V
3	GND
4	GND

CON2 is DC Power Jack for 12V Input.
CON2 can be connected to +12V Adapter.

1.3.4.3 Power Switch

1.3.4.3.1 CON1

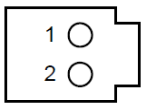


Figure 46. Power switch of Power board

PIN#	Signal
1	12V IN
2	VCC of Power board

CON1 is connected to DC Power ON/OFF Switch via cable.

1.3.4.4 Power Output

1.3.4.4.1 J1

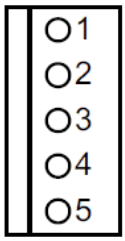


Figure 47. Main board power connector

PIN #	Signal
1	3.3V
2	GND
3	5V
4	GND
5	12V

J1 is Main board power connector.
J1 is connected to mainboard(J2) via power cable.

1.3.4.4.2 J2, J3, J4, J5

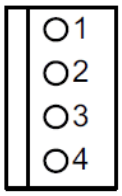


Figure 48. HDD Power connector

PIN #	Signal
1	5V
2	GND
3	GND
4	12V

J2, J3, J4 and J5 are HDD power connector.
These can be connected to Power connector of the SATA HDDs via each SATA power cable.

1.3.4.5 Power control

1.3.4.5.1 J6

Figure 49. Power control connector

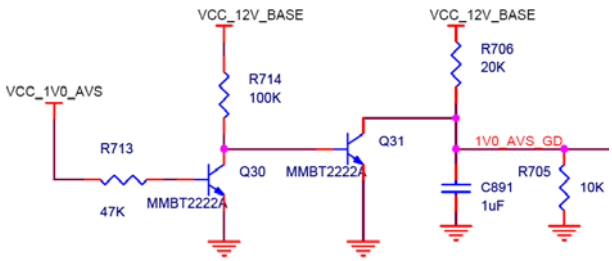
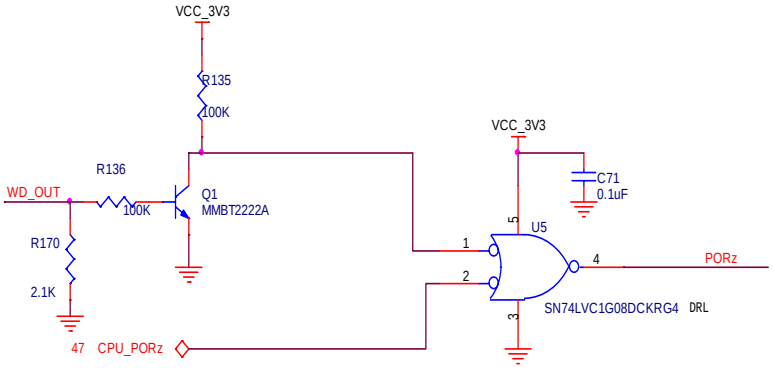
PIN#	Signal
1	GND
2	POWER_ON
3	FRONT_3V3

J6 is Power control connector.
J6 is connected to main board (J3) via cable.

1.4 ERRATA

1	Revision(s) Affected	Rev0.2 and earlier
	Details	The GP0[3]/TCLKIN cannot be used as General-purpose input.
	Workaround	Remove RN30 Note1: If the RN30 is removed, the Sensor1~4 cannot be used.
2	Revision(s) Affected	Rev0.3
	Details	The TLV320AIC3101 has no reset input signal.
	Workaround	Must be jumped between U38(31pin) and the RSTOUTn signal
3	Revision(s) Affected	Rev0.5 and earlier(refer to DM816x errata:SPRZ329)
	Details	When the board is powered on, the Ethernet PHY chip auto-negotiates and establishes a link at either 10/100/1000 Mbps speed, if the link is established at 1Gbps, the Ethernet boot does not work for PHY chips(RTL8211DG) that do not provide the TxCLK clock signal. In these case, the Ethernet boot fails and the 1Gbps mode does not work.
	Workaround	There is no H/W workaround for this issue. Ensure that the PHY does not auto-negotiate to 1Gbps by default, until boot occurs. At a later stage, the second-level bootloader or OS driver can enable 1-Gbps mode in the PHY via MDIO and restart auto-negotiation to switch to gigabit mode. A PHY chip might provide an input pin to disable/enable 1-Gbps mode by default, which can be overridden by using MDIO register settings.
4	Revision(s) Affected	Rev0.3 and earlier
	Details	VGA output quality is poor. Ths7360's filter selection is wrong
	Workaround	Remove : R416(10K), R419(10K), R443(75) Populate: R415(10K), R418(10K) Rev0.3A is changed it.
5	Revision(s) Affected	Rev0.3 and earlier
	Details	Netra McASP driver does not support non-cascaded mode(TVP5158 Audio interface)
	Workaround	It is changed the McASP mode to cascade mode in Rev0.3A. There is not a schedule to update driver(for non-cascaded mode) yet.
6	Revision(s) Affected	Rev0.3 and earlier
	Details	USB disconnection is happened in Some of boards, because of unstable AVS power.

		Unstable AVS power affects the 5V power Level and the Netra detect dropping of the 5V power (under 4.7V), Then the Netra disable the USB_DRVVBUS signal.
	Workaround	Add 330uF on the tps40041 input side (on the C893 or the C894). It will be changed AVS power device in Rev0.4.
7	Revision(s) Affected	Rev0.3 and earlier
	Details	Ethernet port is unstable in Some of boards Because of there is unstable 1.05V that is internal Switch Regulator's output of the RTL8211.
	Workaround	Change C582, C587, C608, C615 (22uF) to 47uF.
8	Revision(s) Affected	Rev0.5 and earlier
	Details	Ethernet port does not work When gigabit mode. When the PHY(RTL8211) does not provide the TxCLK to the NETRA in the GIGA mode, Mac of the NETRA Does not work.
	Workaround	1. Change PHY's Auto-Negotiation configuration. Before : AN[1:0] ="11" (auto-negotiation enable) After : AN[1:0] ="10" (100M mode) Port0 : Remove R340, Populate R338(4.7K). Port1 : Remove R382, Populate R381(4.7K). 2. Update Uboot binary After the MAC working, Updated Uboot binary can enable Auto-negotiation in the PHY via MDIO and restart auto-negotiation to switch to gigabit mode enable.
9	Revision(s) Affected	Rev0.4 and earlier
	Details	High Level of the TPS51200's EN control input signal must be Min 1.7V. But the input high level is just 1.4V now. Even if TPS51200 is run well now. It must be modified.
	Workaround	Remove R690 (10K), but it is just temporary solution. Rev0.5 will be modified the high input level as Min 1.7V
10	Revision(s) Affected	Rev0.3A
	Details	1V0_CON Power (U96)'s enable signal (1V0_AVS_GD) is not connected to any control signal. So, U96 is always enabled.
	Workaround	The 1V0_AVS_GD signal must be modified as below schematic.

		
11	Revision(s) Affected	Rev0.3A and earlier
	Details	Some SATA AC coupled Capacitors have wrong value.
	Workaround	Remove : C45, C47, C49, C51 Modify value (0.1uF -> 10nF): C39, C40, C41, C42, C55, C56.
12	Revision(s) Affected	Rev0.5B and earlier
	Details	SATA Link speed issue. If the SATA3 (6Gbps) HDD is connected to the PM(JMB321) SATA port, Link speed is set to 1.5Gbps. And If some SATA3 (6Gbps) HDDs are connected to the Netra SATA port, Link is fail.
	Workaround	Use jumper for limitation link speed up to 3Gbps on the SATA3 (6Gbps) HDD. Then, link speed is set to 3Gbps
13	Revision(s) Affected	Rev0.5B, Rev0.5A and Rev0.5
	Details	VGA out issue. VGA output is unstable with some monitors. The Hsync and the Vsync signal are not good.
	Workaround	Modify value(100 ohm -> 22 ohm) : R644, R643
14	Revision(s) Affected	Rev0.5B and earlier
	Details	When PORz is asserted, the WD_OUT is held high. So. The system would not come out of reset.
	Workaround	Add a pull down 2.1Kohm (R170) on the WD_OUT. 
15	Revision(s) Affected	Rev0.5B, Rev0.5A and Rev0.5

<table>
<tr><td></td><td>Details</td><td>There are wrong powers on the TPD7S019(U112)</td></tr>
<tr><td></td><td>Workaround</td><td>
<table>
<tr><td></td><td>Current(wrong)</td><td>Correction</td></tr>
<tr><td>U112-2 (VCC_VID)</td><td>VCC_DENC</td><td>VCC_5V0</td></tr>
<tr><td>U112-7 (VCC_DDC)</td><td>VCC_5V0</td><td>VCC_DENC</td></tr>
</table>

It will be modified in the Rev0.6.</td></tr>
<tr><td>16</td><td>Revision(s) Affected</td><td>Rev0.6 and earlier</td></tr>
<tr><td></td><td>Details</td><td>There are two options for VGA sync signal
1. Use LMH1980MM to re-generate the H/V SYNC from RGB signal(R439, R440), this is valid for PG1.1(Netra version) or earlier version.
2. Use the H/V SYNC directly from the Netra (R625, R565), this is valid for PG2.0(Netra version) or above version.</td></tr>
<tr><td></td><td>Workaround</td><td>Refer to below table option.
<table>
<tr><td>Board version</td><td>Sync separator(U41) (1)</td><td>H/V SYNC directly from the Netra</td></tr>
<tr><td>Rev0.4 and earlier</td><td>supported</td><td>Not supported</td></tr>
<tr><td>Rev0.5/0.5A/0.5B with PG1.1</td><td>supported</td><td>Not supported</td></tr>
<tr><td>Rev0.5B with PG2.0</td><td>Not Supported
Remove :
R439, R440</td><td>Supported
Populate :
R625, R565</td></tr>
<tr><td>Rev0.6</td><td>Not supported</td><td>Supported</td></tr>
</table>

Note (1) The sync separator is temporary solution for the PG1.1 that don’t support the H/V sync signal.</td></tr>
</table>