Hardware Manual

Renesas R-Car

M3 Starter Kit Pro

(RTP0RC7796SKBX0010S)

H3 Starter Kit Premier

(RTP0RC7795SKBX0010S, RTP0RC77951SKBX010S)

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Rev.2.0 June 2017

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

R-Car Starter Kit H3/M3 Overview

June 5, 2017

In this document, read
R-Car Starter Kit Premier (RTP0RC7795SKBX0010S) Device is R-Car H3 ver1.1.
R-Car Starter Kit Premier (RTP0RC77951SKBX010S) Device is R-Car H3 ver2.0.
R-Car Starter Kit Pro (RTP0RC7796SKBX0010S) Device is R-Car M3.

Renesas Microcomputer

1. Overview

1.1 Introduction

The R-Car H3/M3 is an SOC that features the basic functions for next-generation car navigation systems.

The R-Car H3/M3 includes:

R-Car H3 ver1.1 R-Car H3 ver2.0

- Four 1.5-GHz ARM® Cortex®-A57 MPCore™ cores,
- Four 1.2-GHz ARM® Cortex®-A53 MPCore™ cores,
- Memory controller for LPDDR4 with 32 bits × 4 channels,
- 1channel for RGB888 output and 1channel for LVDS,
- Serial ATA interface,

R-Car H3 ver1.1

- 4 channels MIPI-CSI2 Video Input, 2 channels digital Video Input,
- USB3.0 x 2ch and USB2.0 x 3ch interfaces,

R-Car H3 ver2.0

- 3 channels MIPI-CSI2 Video Input, 2 channels digital Video Input,
- USB3.0 x 1ch and USB2.0 x 4ch interfaces,

R-Car M3

- Two 1.5-GHz ARM® Cortex®-A57 MPCore™ cores,
- Four 1.3-GHz ARM® Cortex®-A53 MPCore™ cores,
- Memory controller for LPDDR4 with 32 bits × 2 channels,
- 1channel for RGB888 output and 1channel for LVDS,
- 2 channels MIPI-CSI2 Video Input, 2channels digital Video Input,
- USB3.0 x 1ch and USB2.0 x 2ch interfaces,

R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3

- Three-dimensional graphics engines,
- Video processing units,
- Sound units,
- PCI Express interface,
- CAN interface, and
- EtherAVB.

Note: ARM and Cortex are registered trademark of ARM Limited. All other brands or product names are the property of their respective holders.

1.2 List of Specifications

1.2.1 ARM Core

Item	Description
System CPU Cortex-A57 R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• L1 I/D cache 48K/32 Kbytes, R-Car H3 ver1.1 R-Car H3 ver2.0 • ARM Cortex-A57 Quad MPCore 1.5 GHz • L2 cache 2 Mbytes R-Car M3 • ARM Cortex-A57 Dual MPCore 1.5 GHz • L2 cache 1 Mbytes R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3 • NEON™/VFPv4 supported • Security extension supported • Virtualization supported • ARMv8 architecture
System CPU Cortex-A53 R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	R-Car H3 ver1.1 R-Car H3 ver2.0 • ARM Cortex-A53 Quad MPCore 1.2GHz R-Car M3 • ARM Cortex-A53 Quad MPCore 1.3GHz R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3 • L1 I/D cache 32/32 KBytes, L2 cache 512 KBytes • NEON™/VFPv4 supported • Security extension supported • Virtualization supported • ARMv8 architecture
Debug and Trace R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• JTAG/SWD I/F supported • ETM-A57/A53 supported (each CPU) • ETF 16 KBytes for program flow trace (each cluster)

1.2.2 External Bus Module

Item	Description
External Flash Controller R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• Supports RPC(Reduced Pin Count) flash memory or 2x QSPI flash memory Maximum Frequency 160MHz(320MB/s) for RPC, 80MHz(160MB/s) for 2x QSPI
External Bus Controller for DDR4 SDRAM (DBSC4) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	R-Car H3 ver1.1 R-Car H3 ver2.0 • 4 channels (32-bit bus mode) • LPDDR4 can be connected directly. • Memory Size: Up to 8GB (*) R-Car M3 • 2 channels (32-bit bus mode) • LPDDR4 can be connected directly. • Memory Size: Up to 4GB (*) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3 • Auto Refresh/Self Refresh/Partial Array Self Refresh supported • Auto Pre-charge Mode • DDR Back Up supported (*) SOC function supports 4GB memory size per channel , But DRAM vendor don’t provide 16Gbit LPDDR4 SD-RAM now • Cache memory for DDR-Memory access efficiency • Decompression of visual near lossless compressed image • Memory access protection for secure/safety regions

1.2.3 Internal Bus Module

Item	Description
AXI-bus R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• On-chip main bus — Bus protocol : AXI3 with QoS control — Frequency: 400 MHz — Bus width: 512 bits/256 bits/128 bits — CoreLink™ CCI-Kipling Cache Coherent Interconnect — Bus protocol: AMBA®4 ACE™ and ACE-Lite™ — Frequency: 800 MHz — Bus width: 128 bits
Direct Memory Access Controller for System (SYS-DMAC) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• 16 channels for PERW domain (SYDM0) • 32 channels for PERE domain (SYDM1, 2) • Address space: 4 GBytes on architecture • Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes • Maximum number of transfer times: 16,777,216 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
Boot R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• System startup with selectable boot mode at power-on reset • In on-chip ROM boot, RPC or QSPI serial ROM boot is supported. • Program downloaded to internal memory (System RAM) Autorun function for the downloaded program

Item	Description
Direct Memory Access Controller for Audio (Audio-DMAC) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• 32 channels • asdm0: 16 channels • asdm1: 16 channels • Address space: 4 GBytes on architecture • Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes • Maximum number of transfer times: 16,777,216 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
Audio-DMAC-Peripheral-Peripheral R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• Audio-DMAC (for transfer from Peripheral to Peripheral) • 29 channels + 29 (extended) channels for audio domain • Data transfer length: longword (4 Bytes) • Transfer count: Transfer count is not specified (DMA transfer is made from the transfer-start to transfer-stop settings.) • Transfer request: Selectable from on-chip audio peripheral module request • Priority: round-robin mode • Interrupt request: not supports interrupt request to CPU at the end of data transfer
Interrupt Controller (INTC) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	INTC-SYS — 7 interrupt pins which can detect external interrupts — Fall/rise/high level/low level detection is selectable — On-chip peripheral interrupts: Priority can be specified for each module — Max. 480 shared peripheral interrupts supported — 16 software interrupts that have been generated and 6 private peripheral interrupts supported — 32-level priority selectable — Trust Zone supported

1.2.4 Internal Memory

Item	Description
System RAM R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	— RAM of 384 KBytes

1.2.5 Display Units

Item	Description

Item	Description	
Display Unit (DU) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	Display channel	R-Car H3 ver1.1 R-Car H3 ver2.0 4 independently controllable channels R-Car M3 3 independently controllable channels
	Interface	R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3 • LVDS 1 channel • Digital RGB 1channel (8-bit precision for each RGB color)
	LVDS interface (1ch)	• Output: compliant with TIA/EIA-644; five pairs of differential output (four pairs of data and one pair of clock) • Operating frequency: Dotclk 148.5 MHz
	Screen size and number of composite planes per channel	• Maximum screen size: 3840x2160 • Number of planes specifiable: 5
	CRT scanning method	Non-interlaced
	Synchronization method	Master
	Internal color palette	• Includes four color palette planes which can display 256 of 260 thousand colors at the same time.
	Output display numbers	R-Car H3 ver1.1 R-Car H3 ver2.0 • Four output channels (resolutions for different displays) R-Car M3 • Three output channels (resolutions for different displays) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3 • Output on rising and falling edges of the synchronizing signal (resolution for the same display) • 8-bit precision for each RGB color
	Blending ratio settings	Number of color palette planes with blending ratio: 4
	Dot clock	Switchable between external input and internal clock
	Color management	Following functions will be supported by Renesas software portfolio. • γ correction, gain correction • Applies correction of color (skin color adjustment and color correction set in memory) in terms of color phase, brightness, and chromaticity for a specified range of colors or for the full range of colors • 1D LUT, 3D LUT, 1D Histogram, Color space conversion

Item	Description	
Video Input Module (VIN) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	MIPI-CSI2 interface	R-Car H3 ver1.1 R-Car H3 ver2.0 • 3 channels (4lane x 2channels, 2lane x 1channel) R-Car M3 • 2 channels (4lane x 1channel, 2lane x 1channel) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3 • Interleaving by 4 VC(virtual channel) supported • Filtering by DT(data type) supported • YUV422 8/10bit, RGB888,Embedded 8bit, User Defined 8bit are supported • 1.5Gbps/Lane
	digital interface	• 2 channels (RGB/YCbCr) • Dotclk 100MHz • ITU-R BT.601 interface: 8-, 10- (same size only (not scaling)), or 12-bit (same size only (not scaling)) YCbCr422, RGB666, 24-bit RGB888 • ITU-R BT.656 interface: 8-, 10- (same size only (not scaling)), or 12-bit (same size only (not scaling)) YCbCr422 • ITU-R BT.1358 interface: 16-, 20- (same size only (not scaling)), or 24-bit (same size only (not scaling)) YCbCr422 • ITU-R BT.709 interface: : 8-, 10- (same size only (not scaling)), or 12-bit (same size only (not scaling)) RGB666, RGB888, YCbCr422 About Digital RGB channel usage combination , Please refer as follows cases. CASE1 VIN-A8bit + VIN-B8/12/16 CASE2 VIN-A12bit + VIN-B8/12/16 CASE3 VIN-A16bit + VIN-B8/12
	Capturing function	Up to 8 input images can be captured (using VC, DT filtering)
	Clipping function	Up to 4096x4096
	Horizontal scaling	Up to two times, but only scaling down is possible for HD1080i or HD1080p data.(one input only)
	Vertical scaling	Up to three times, but only scaling down is possible for HD1080i or HD720P data.(one input only)
	Output format	RGB-565, ARGB-1555, YCbCr422, RGB888, YCbCr420 YC separation, and extraction of the Y component

1.2.6 Video Processing

Item	Description

Item	Description
Video Signal Processor (VSPI) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	R-Car H3 v1.1 VSPI has the following features. 3 sets of VSPI are integrated. 250 Mpix/s process rate (input rate) per 1 VSPI R-Car H3 v2.0 VSPI has the following features. 2 sets of VSPI are integrated. 500 Mpix/s process rate (input rate) per 1 VSPI R-Car M3 VSPI has the following features. 1 set of VSPI is integrated. 500 Mpix/s process rate (input rate) per 1 VSPI R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3 (1) Supports Various Data Formats and Conversion — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying (2) 4K (3840 pixels x 2160 lines) Video Processing — Up and down scaling with arbitrary scaling ratio — Super resolution processing — Image rotation/reversal function: Reverses an image vertically/horizontally or rotates it by 90°/270° (3) 4K (3840 pixels x 2160 lines) Picture Quality/Color Correction with 1D/3D Look Up Table(LUT) Following functions will be supported by Renesas software portfolio. — Dynamic γ correction and gain correction — Correction of color (to adjust skin tones or colors in memory) ➢ Hue, brightness, and saturation adjustment ➢ 1D and 2D histogram (4) Visual near lossless image compression supported — 50% of bandwidth is diminished

Item	Description
Video Signal Processor (VSPB) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	R-Car H3 v1.1 VSPB has the following features. 2 sets of VSPB are integrated. 250Mpix/s process rate (input rate per layer) per 1 VSPB. R-Car H3 v2.0 VSPB has the following features. 2 sets of VSPB are integrated. 500Mpix/s process rate (input rate per layer) per 1 VSPB. R-Car M3 VSPB has the following features. 1 set of VSPB is integrated. 500Mpix/s process rate (input rate per layer) per 1 VSPB. R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3 (1) Supports Various Data Formats and Conversion — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying (2) 4K (3840 pixels x 2160 lines) Video Processing — Blending of 5 picture layers and raster operations (ROPs) (3) Visual near lossless image compression supported — 50% of bandwidth is diminished
Video Signal Processor (VSPD) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	R-Car H3 ver1.1 VSPD has the following features. 4 sets of VSPD are integrated. R-Car H3 ver2.0 VSPD has the following features. 2 sets of VSPD are integrated. R-Car M3 VSPD has the following features. 3 sets of VSPD are integrated.
Video Decoding Processor for inter-device video transfer (VSPDL) R-Car H3 ver2.0	VSPDL has the following features. 1 set of VSPDL is integrated. **(1) Supports two display output interfaces** — Up to Full HD resolution for LIF0 display — Up to 1280x960 resolution for LIF1 display — Color space conversion and changes to the number of colors by dithering — Color keying **(2) Supports various data formats and conversion** — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying — Supports combination between pixel alpha and global alpha — Supports generating pre multiplied alpha

Item	Description
Video Codec Processor (VCP4) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	The VCP4 is a multi-codec module which provides encoding and decoding capabilities on the basis of multiple video coding schemes, e.g.,H.265/HEVC, H.264/AVC, MPEG-4, MPEG-2 and VC-1. This IP (Intellectual Property) is a multi codec that processes the frame or each field by controlling software for VCP4 executed on host CPU. • The VCP4 has the following features: Support for multiple codecs H.265/HEVC MP (Main Profile) decoding H.264/MPEG-4 AVC HP (High Profile) and MVC SHP (Stereo High Profile) encoding and decoding H.262/MPEG-2 MP (Main Profile) decoding MPEG-4 ASP (Advanced Simple Profile) decoding VC-1 SP/MP/AP (Simple, Main, Advanced Profile) decoding H.263 Baseline decoding DivX decoding (Home Theater*, HD1080*, and Plus HD Profiles) *: QMC and 1-warping point GMC are supported RealVideo8/9/10 decoding VP8 encoding and decoding • Support for up to 4K resolutions (H.265 and H.264 only) Multiple channel processing: When iVDP1C is used: (H.264/H.265 1920 x 1080p x 120 fps), or (H.264/H.265 1920 x 1080p x 30 fps) + (RealVideo8/9/10 1920 x 1080p x 30 fps), or (H.264/H.265 1920 x 1080p x 60 fps) + (Others 1920 x 1080p x 30 fps), or (H.264/H.265 1920 x 1080p x 30 fps) + (Others 1920 x 1080p x 60 fps) When iVDP1C is not used: (H.265 1920 x 1080p x 120 fps) + (H.264 1920 x 1080p x 120 fps), or (H.265 1920 x 1080p x 120 fps) + (H.264 1920 x 1080p x 30fps) + (RealVideo8/9/10 1920 x 1080p x 30 fps), or (H.265 1920 x 1080p x 120 fps) + (H.264 1920 x 1080p x 60 fps) + (Others 1920 x 1080p x 30 fps) (H.265 1920 x 1080p x 120 fps) + (H.264 1920 x 1080p x 30 fps) + (Others 1920 x 1080p x 60 fps) Note: “1920 x 1080p x 120 fps” can be replaced as “3840 x 2160p x 30 fps”. “1920 x 1080p x 60 fps” can be replaced as “1280 x 720p x 120 fps”. “1920 x 1080p x 30 fps” can be replaced as “1280 x 720p x 60 fps”. Maximum performance will change with securable bus bandwidth. • Data handling on a picture-by-picture basis Encodes/decodes data one picture (frame or field) at a time. • High picture quality Supports the H.264 high-efficiency coding tools (CABAC, 8 x 8 frequency conversion, and quantization matrix). High-efficiency motion vector detection by a combination of discrete search and trace search Highly efficient real-time intra-prediction by Prediction from Original Image (POI) Optimal-mode selection by Rate-Distortion (RD) cost evaluation Picture quality control based on activity analysis results which match visual models • Low power dissipation Dynamically disables the clocks for the entire VCP4. Dynamically disables the clocks for individual submodules. • Includes its own reference data cache • Lossless image compression for reference picture is supported • Use the software from Renesas to handle VCP4 functions.

Item	Description
Fine Display Processor (FDP1) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	The FDP1 is the de-interlacing module which converts the interlaced video to progressive video, and has the following features. R-Car H3 ver1.1 (1) Supports 3 channels 250 Mpix/s process rate (input rate) per 1 FDP1 R-Car H3 ver2.0 (1) Supports 2 channels 500 Mpix/s process rate (input rate) per 1 FDP1 R-Car M3 (1) Supports 1 channel 500 Mpix/s process rate (input rate) per 1 FDP1 R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3 (2) Supports various data formats — Input: YCbCr444/422/420 — Output: YCbCr444/422/420 and RGB/αRGB (3) 4K (3840 pixels x 2160 lines)video processing performance (4) High image quality de-interlacing algorithm — Motion adaptive de-interlacing — Accurate still detection — Diagonal line interpolation (DLI) (5) Visual near lossless image compression supported — 50% of bandwidth is diminished

1.2.7 Sound Interface

Item	Description

Item	Description	
Sampling Rate Converter Unit (SCU) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	Overall specification	• Includes ten SRC modules — Supports the quality suitable for audio sound (THD+N -132dB) : six modules — Supports the quality suitable for voice sound (THD+N -96dB) : four modules • The SRC module is capable of correcting phase change and delay (timing jitter) generated during data transfer over external memories or external devices. • The channel count conversion unit (CTU), mixer (MIX), and digital mute and volume function (DVC) can be used on two fixed output channels.
	Sampling rate conversion (SRC)	• Capable of asynchronous sampling rate conversion • Supports resolutions up to 24 bits • Two kinds of filter type for SRC. — Supports the quality suitable for audio sound (THD+N -132dB): Realized the filter by passband -1dB@0.4575FS, cutoff -18dB@0.5FS. — Supports the quality suitable for voice sound (THD+N -96dB): Realized the filter by passband -1dB@0.4561FS, cutoff -72dB@0.5FS. (Characteristics of each filter is written in the equivalent/up-sampling cases.) • Automatically generates antialiasing filter coefficients • For monaural to eight-channel sound sources
	Channel count conversion unit (CTU)	• Downmixing and splitter functions — Conversion of eight input channels into four output channels — Conversion of six input channels into two output channels — Conversion of two input channels into four sets of two output channels — Conversion of one input channel into eight sets of one output channel — No conversion
	Mixer (MIX)	• Mixing (adds) two to four sources into one • Ratio for adding sources is selectable • Ratio is dynamically changeable • Mixing with volume ramp is available (ramp period is selectable)

Item	Description	
	Digital volume and mute function (DVC)	• Volume control function including digital volume, volume ramp, and zero-crossing mute • The digital volume function is specified by a 24-bit fixed-point value within the range from 0 to 8 times (mute, or -120 to 18 dB) • The volume ramp function can be used for soft mute, fade-in, fade-out, or desired volume adjustment • The volume ramp period can be changed within the sampling range from the 0th to 23rd power of 2 • The zero-crossing mute function silences the sound at the zero-crossing point of the audio data

Item	Description	
Serial Sound Interface Unit (SSIU) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	Overall specification	• Includes ten SSI modules functioning as interfaces with external devices. — Supports short and long formats — Supports TDM format (six modules of ten modules can be used for this function) • Max. 16 independent monaural sound sources in a TDM format can be in TDM format.
	Serial sound interface (SSI)	• 10 channels • Max frequency 15MHz • Operating mode: non-compressed mode (Not support compressed mode) • Supports versatile serial audio formats (I2S/left justified/right justified) • Supports master/slave functions • Programmable word clock, bit clock generation functions • Multichannel format functions (up to four channels) • Supports 8-/16-/18-/20-/22-/24-/32-bit data formats • Supports TDM mode • Supports WS continue mode • The DMA controller or interrupts control the transfer of data to and from the SSI module. • Supports short and long frames for monaural data (valid data lengths are 8 and 16 bits) • Up to nine independent clock signals can be input.
Audio Clock Generator (ADG) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	Selection or division of audio clock signals	

1.2.8 Storage

<table>
<tr><th>Item</th><th>Description</th></tr>
<tr><td>USB2.0 Host (EHCI/OHCI)
R-Car H3 ver1.1
R-Car H3 ver2.0
R-Car M3</td><td>R-Car H3 ver1.1
• 3 channels (Host only 2 channels/Host-Function 1channel)
• USB Host (EHCI/OHCI) 4LINK
R-Car H3 ver2.0
• 4 channels (Host only 2 channels/Host-Function 2channel)
• USB Host (EHCI/OHCI) 4LINK
R-Car M3
• 2 channels (Host only1 channels/Host-Function 1channel)
• USB Host (EHCI/OHCI) 2LINK
R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3
• (USB3.0 module also can be used as USB2.0)
• Compliance with USB2.0
• USB Function 1LINK
• Supports On-The-Go (OTG) function Rev2.0 complying with 2 protocols:
+ Session Request Protocol (SRP).
+ Host Negotiation Protocol (HNP).
• Compliance with USB2.0 (High-Speed)
• Interrupt request
• Internal dedicated DMA
• Compliance with Battery Charging function Rev1.2:
+ Charging Port (Host): CDP, SDP are supported (Not support DCP).
+ Portable Device (Function) is supported.</td></tr>
<tr><td>USB3.0 Host Controller
R-Car H3 ver1.1
R-Car H3 ver2.0
R-Car M3</td><td>R-Car H3 ver1.1
• USB 3.0 DRD 2 channel
R-Car H3 ver2.0
• USB 3.0 DRD 1 channel
R-Car M3
• USB 3.0 DRD 1 channel
R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3
• This module can be use as USB2.0 as follows
<table>
<tr><th>Core</th><th>Super Speed</th><th>High Speed</th><th>Full Speed</th><th>Low Speed</th></tr>
<tr><td>Host</td><td>√</td><td>√</td><td>√</td><td>√</td></tr>
<tr><td>Peripheral</td><td>√</td><td>√</td><td>√</td><td></td></tr>
</table>
• Supports SS/HS/FS/LS. xHCI</td></tr>
<tr><td>Serial-ATA Gen3
R-Car H3 ver1.1
R-Car H3 ver2.0</td><td>• Serial ATA Standard Rev3.2 supported
• 6.0-Gbps (Gen3) transfer rate supported</td></tr>
<tr><td>rawNAND Controller
R-Car M3</td><td>• The NAND Flash Memory Interface controller implements the function of a high level interface to one NAND flash device. It supports the functionality of the high speed NAND Flash devices described in the ONFI 1.x specifications.</td></tr>
</table>

1.2.9 Network

Item	Description
CAN-FD R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• 2 interfaces • 8 Mbps(CAN clock 400MHz)
PCIE Controller R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• PCI Express Base Specification Revision 2.0 • 1 Lane x 2 channel • PHY integrated
Ethernet AVB-IF R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• Supports IEEE802.1BA, IEEE802.1AS, IEEE802.1Qav and IEEE1722 functions • Supports transfer at 1000 Mbps and 100 Mbps • Magic packet detection • Supports Reception Filtering to separate streaming frames from different sources • Supports interface conforming to IEEE802.3 PHY-RGMII (Reduced Gigabit Media Independent Interface) • RGMII v1.3

1.2.10 Timer

Item	Description
RCLK Watchdog Timer R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• 1 channel • Internal 16-bit watchdog timer operated by RCLK • Programmable overflow time-period: more than 1 hour count capable
SystemWatchDog R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• 1 channel • Internal 16-bit watchdog timer • Programmable overflow time period: maximum 1[h]: initial counter value 180[s]
Compare Match Timer Type0 (CMT0) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• 2 channels • 32-bit timer (16 bits/32 bits can be selected) • Source clock : RCLK clock • Compare match function provided • Interrupt requests
Compare Match Timer Type1 (CMT1) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• 8 channels • 48-bit timer (16 bits/32 bits/48 bits can be selected) • Source clock : RCLK/system clock • Compare match function provided • Interrupt requests

Item	Description
Compare match timer 2 (CMT2) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	(same as CMT1)
Compare match timer 3 (CMT3) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	(same as CMT1)
Timer Unit (TMU) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• 15 channels • 32-bit timer • Auto-reload type 32-bit down counter • Internal prescaler • Interrupt request • 2 channels for input capture

1.2.11 Peripheral Module

Item	Description
I2C Bus Interface for DVFS (I2C for DVFS) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• 1 DVFS channel for dedicated buffer. • Supports single master transmission/reception • Interrupt request • Automatic transfer by wakeup / overdrive request
I2C Bus Interface (I2C) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	• 7 channels • 4 channels for buffers with a slew rate (channel 0,3,4,5 for dedicated buffers), • 3 channels for LVTTL buffers (channels 1,2,6 for ordinary buffers) • NXP I2C bus interface method supported • Master/slave functions • Multi-master functions • Transfer rate up to 400 kbps supported • Programmable clock generation from the system clock • I2C pins switchable with IIC pins (just above) • Master and Slave function DMA supported

Item	Description	
Serial communication interface with FIFO (SCIF) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	Overall specification	• 6 channels • Asynchronous, clock-synchronized modes • Asynchronous serial communication mode The SCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). There is a choice of eight serial data transfer formats. — Data length: 7 bits or 8 bits — Stop bits: 1 bit or 2 bits — Parity: Even/odd/none — Receive error detection: Parity, framing, and overrun errors — Break detection: A break is detected when a framing error lasts for more than 1 frame length at Space 0 (low level). When a framing error occurs, a break can also be detected by reading the RX pin level directly from the serial port register (SCSPTR). • Clock synchronous serial communication mode The SCIF performs serial data communication synchronized with a clock. This feature enables serial data communication with other LSIs that support synchronous communication. There is a single serial data communication format for clock synchronous serial communication. — Data length: 8 bits — Receive error detection: Overrun errors • Full-duplex communication capability The SCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 16-stage FIFO buffer structure, enabling continuous serial data transmission and reception. • On-chip baud rate generator, enabling any bit rate to be selected The SCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock. • Eight interrupt sources • The SCIF has eight types of interrupt sources. receive-data-ready, receive-FIFO-data-full, break, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out and enables any of them to be requested independently.

Item	Description	
Serial Communication Interface with FIFO (SCIF) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3	Overall specification	• DMA data transfer When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer. • In asynchronous mode using channels 0 and 1, modem control functions (RTS and CTS) are stored. • RTS and CTS are not implement for SCIF2 • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • In asynchronous mode, a receive data ready (DR) or a timeout error (TO) can be detected during reception.
Clock-Synchronized Serial Interface with FIFO (MSIOF) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3		• 4 channels • Max. speed: 66MHz (at specific multi pinset/channel) • Internal 64-Byte transmit FIFOs/internal 256-Byte receive FIFOs • Supports master and slave modes • Internal prescaler • Supports serial formats: IIS, SPI (master and slave modes) • Interrupt request, DMAC request
High Speed Serial Communication Interface with FIFO (HSCIF) R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3		• 5 channels • Asynchronous serial communication mode • Capable of full-duplex communication • On-chip baud rate generator, enabling any bit rate to be selected • Eight interrupt sources • DMA data transfer • Modem control functions (HRTS# and HCTS#) are stored. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • A receive data ready (DR) or a timeout error (TO) can be detected during reception.
PWM R-Car H3 ver1.1 R-Car H3 ver2.0 R-Car M3		• 7 channels • High-level width (10 bits) of PWM output can be set. • High-level periods (10 bits) of PWM can be set. • Periods in the range from two to 2^{24} × 1024 cycles of the Pϕ clock can be set. • Continuous pulse or single pulse output selectable

R-Car Starter Kit H3 / M3 Hardware Manual

Publication Date: Rev.2.0 June 1, 2017

Published by: Renesas Electronics

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M3 Starter Kit Pro

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