**Main Contributions:**

The article introduced a new type of hardware description language. Instead of using state machine in VHDL or Verilog, the BSV can get rid of it, and using only rules to make a hardware system work. The main strength of this new language is this special rule syntax. Maybe these rules are not efficient as before to describe the hardware, but it makes the hardware language more like a software language. This makes the cooperation of the hardware group and software group in a same project much more easier and reduced a huge amount of communication cost. Also, seems the rules have a better performance in some test, but realistically the hardware is always depending on the structure, so the test seems not very important.

**My Thoughts:**

I had some idea familiar with this before, which try make VHDL more like a software language, and get rid of the state machine. This paper made a good progress on this, and I can see a huge potential of this kind of language in a large project group being very useful. Also, this could make the software engineer’s job easier when they try to understand the hardware when the base level optimization is available.

But, I think a new language need a new user group to support it, which means there won’t be a lot of people using it, considering the BSV is focusing on the software engineering group, which is a group contains very few people. So, I think if they want to keep going, maybe change the user group they are trying to face is a good idea, EE or ECE student seems good choices for them.

Also, the limitation. All their examples are simple, no large circuit among those examples. I think this kind of auto state format will cause some trouble in large system contains a lot of variables. And since it’s not like VHDL, there will be a hard time for the engineers to figure out how to solve them. During this time, they might lose a lot of users.

**Positive Point:**

A creative idea!

**Negative Point:**

Maybe they need to choose some user group to re-direct this system.