**Main Contributions:**

The author of the paper noticed that the memory system they are using at that time has a problem, which multiple copies of the data inside the main storage among the caches could be distributed. There are massive solutions, but the paper provided a cleaner and more consistent solution. The difference made this system so special is instead of every processor fetch the data from the main storage when they don’t have it, they will get the data from the other caches if the data already fetched by other processor. This will significantly reduce the resource spend on maintaining multiple copies the same. The design is proved at the simulation level, and already been sent to the foundry. There will be another testing paper after they got the chip.

**My Thoughts:**

The thing impressed me the most is their design of the bus usage. They find a use, which ignored by all the company and designers for a long time, of a resource that has been there for such a long time (I assume this because there is already a standard, and manufacturers already offering it. But yeah, it can be only 6 months or less, but still creative enough). The design first time made a cache get data from other caches, instead of the main storage. This will make the maintain process easier and free tons of resources used to keep the data across all the caches all the same.

It had its limitation. As the paper indicated, the idea hasn’t been tested in the real environment, and not sure what’s the real performance really like, but it has the simulation, so it’s not that big of a deal. Though, I think they really need to talk about some the problems could possibly happen. This will make all the experiment and validation of the system much easier to others.

The no clock design is another thing I think that could be improved. They assume the data all comes in at the same time, but for real design, it can be different time. Maybe they can at least give an external clock design for the chip since their special usage of the bus.

**Positive Point:**

The idea of make bus an inhibit device to other caches. I think it’s so creative at that time.

**Negative Point:**

Even the logic and structure is great, mention some disadvantages and problems could happen would be ideal.