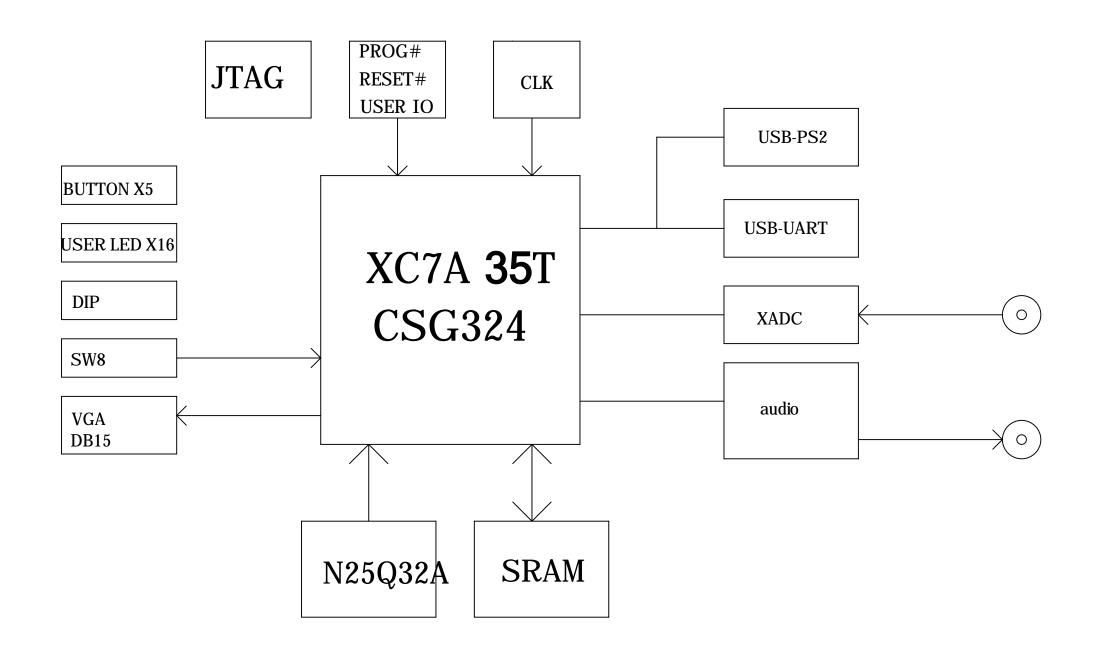
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6	DISPLAY_UART_BT
7	FPGA_POWER
8	POWER
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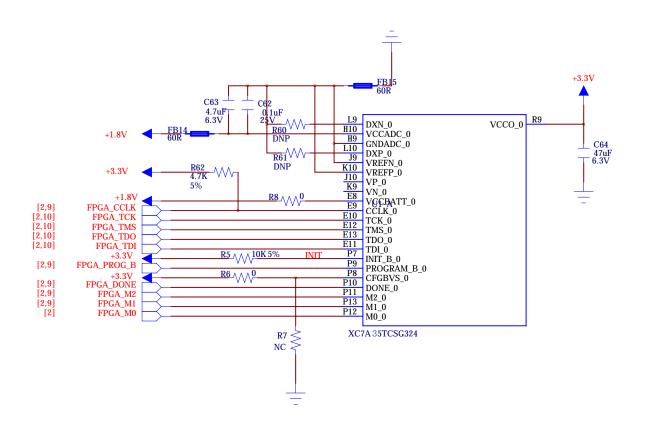
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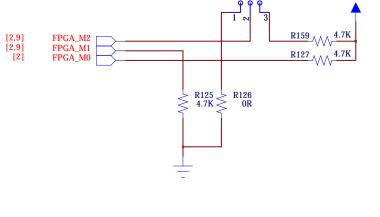




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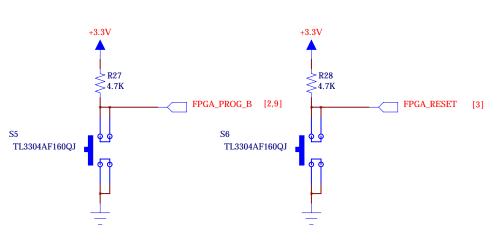
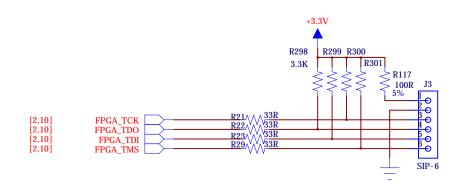
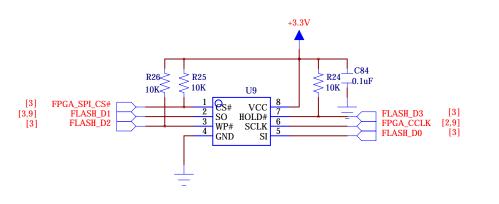
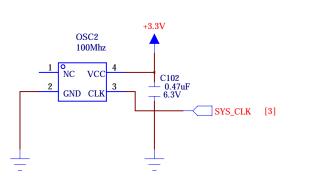
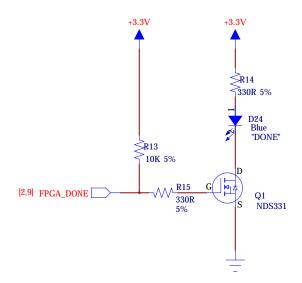


Table 2-1: 7 Series FPGA Configuration Modes **Configuration Mode** M[2:0] **Bus Width CCLK Direction** Master Serial 000 Output x1 Master SPI x1, x2, x4 Output 001 Master BPI 010 x8, x16 Output Master SelectMAP 100 x8, x16 Output JTAG Not Applicable x1 101 Slave SelectMAP x8, x16, x32⁽¹⁾ 110 Input Slave Serial⁽²⁾ 111 x1 Input

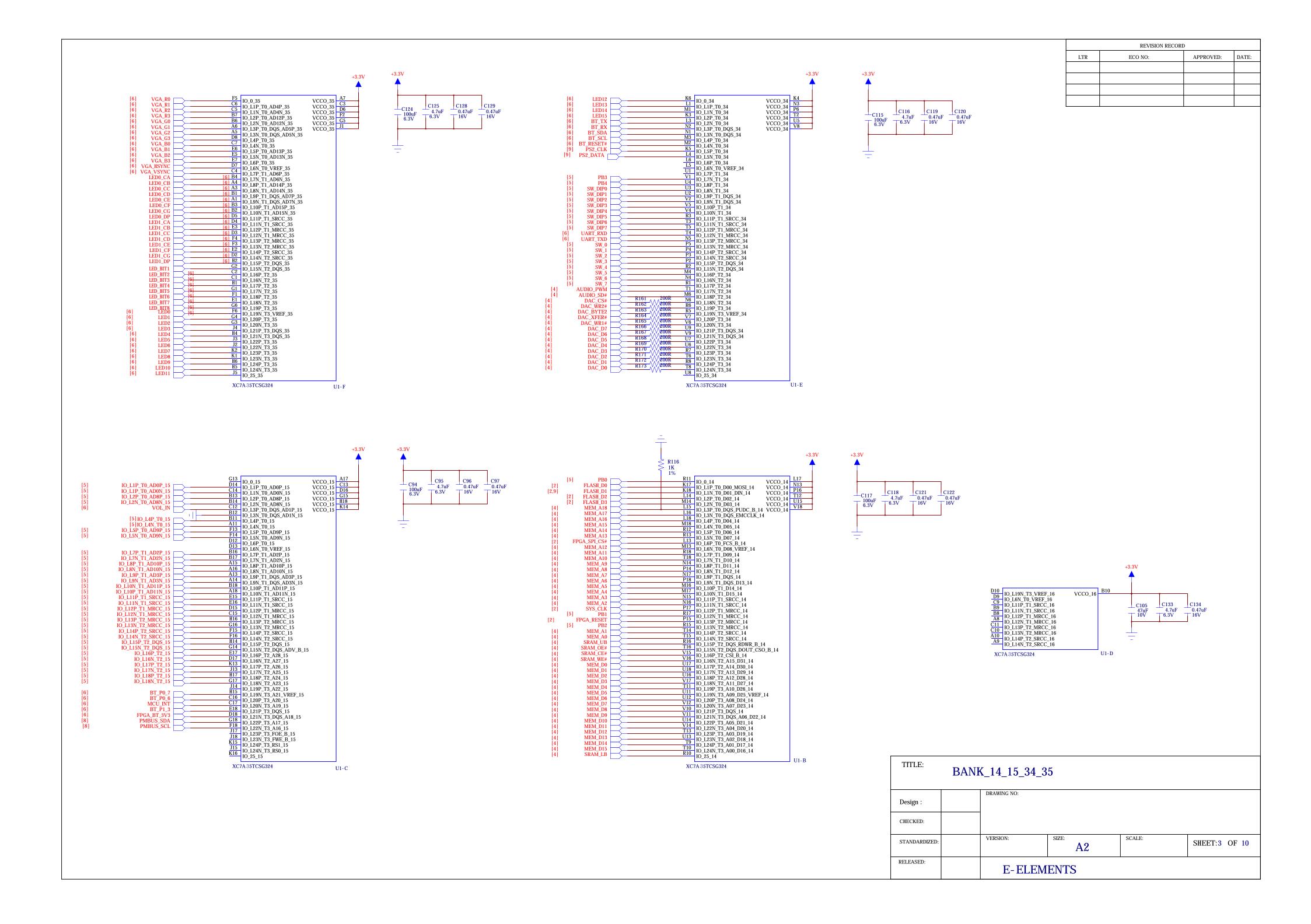




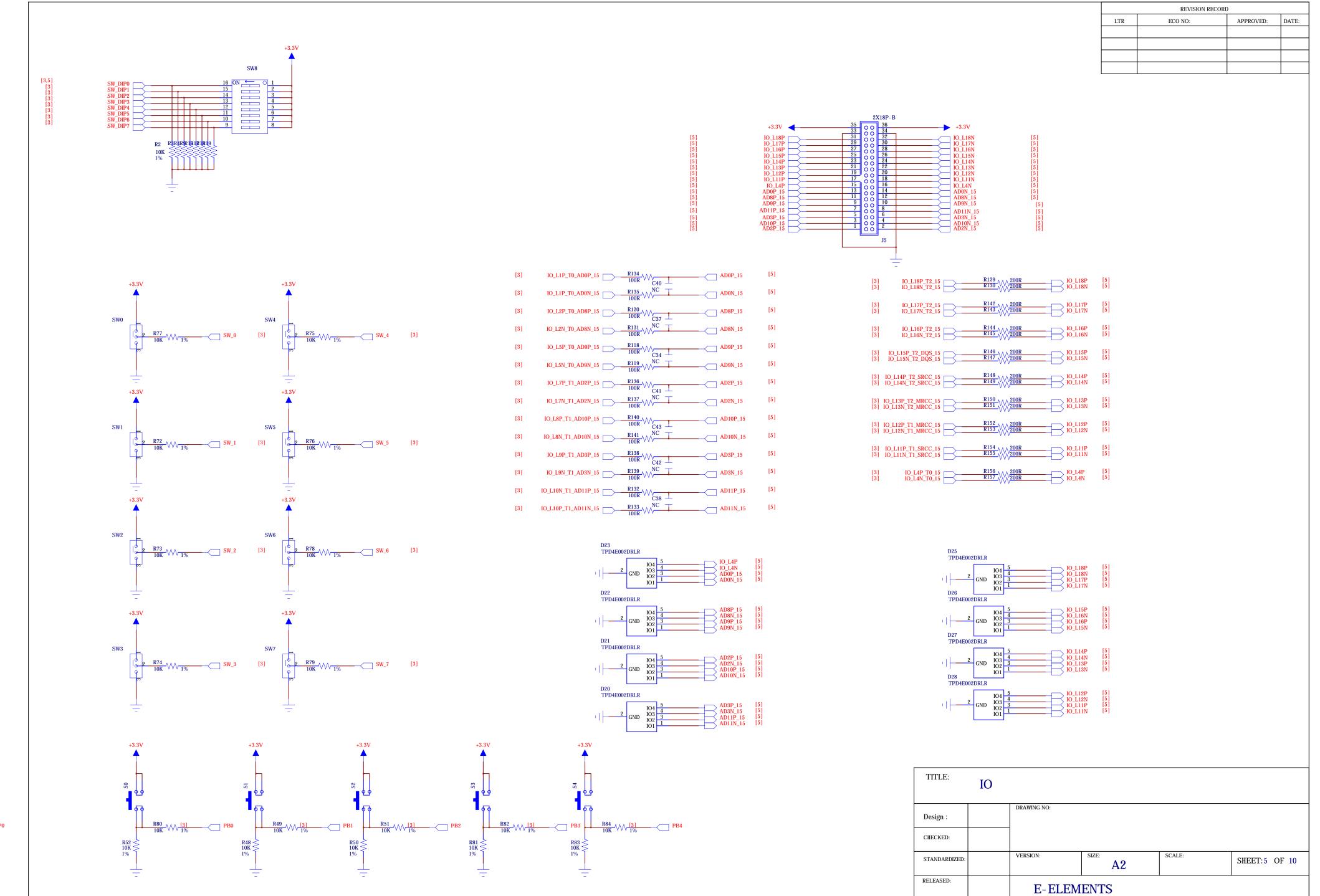




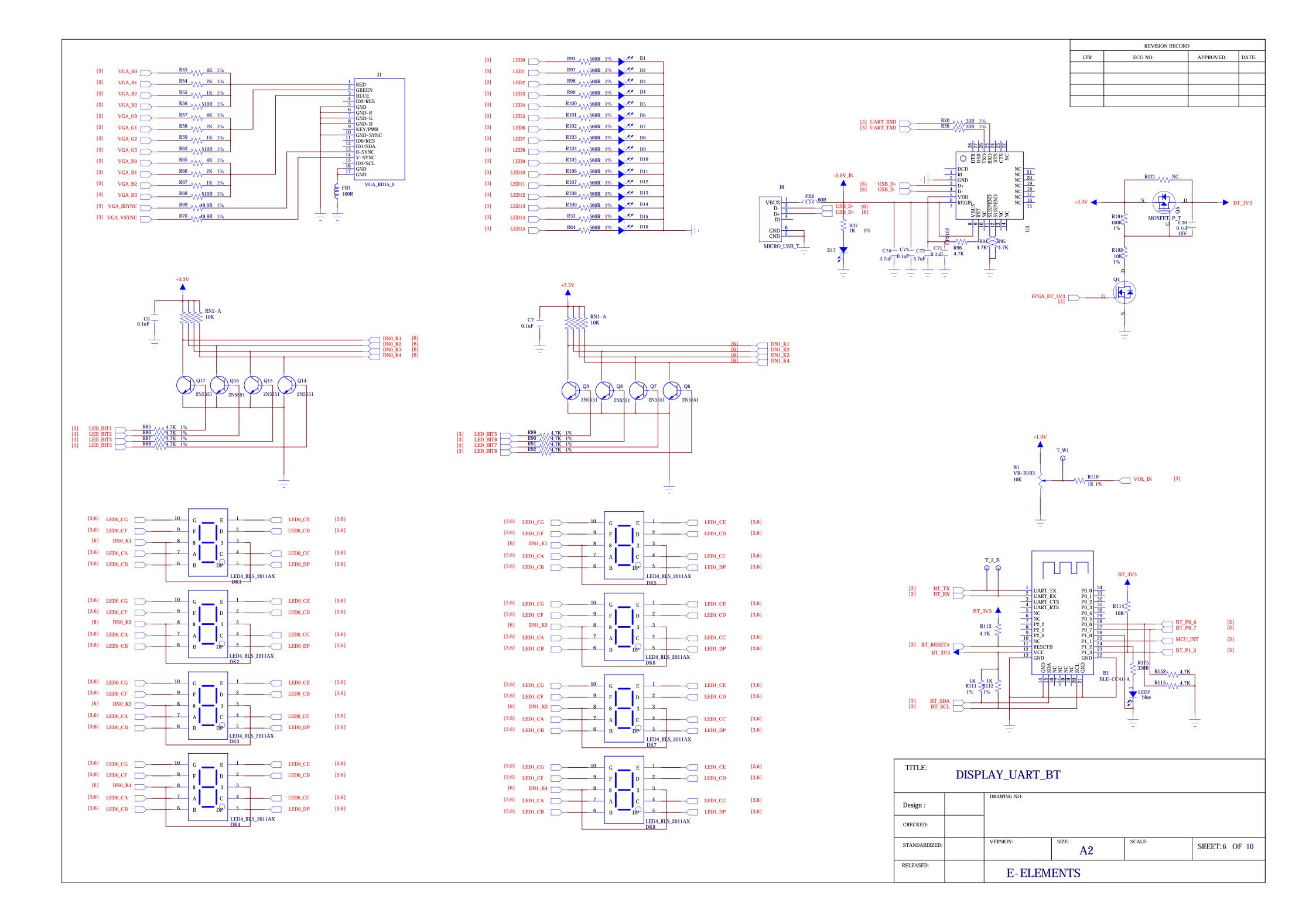
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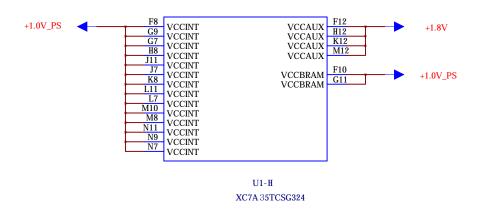
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+3.3V +3.3V U4		
MEM A0 A3 A0 VDD E1 D6 C35 C36 A2 VDD A2 A2		
MEM A3 B3 A3 MEM A4 B4 A4 L/O0 MEM A5 C3 A5 L/O1 MEM A6 C4 A5 L/O2 MEM A7 D4 A6 L/O2 MEM A7 D5 MEM D2		
MEM A3 B3 MEM A4 B4 MEM A5 C3 MEM A6 C4 A5 MEM A7 D4 MEM A7 D4 MEM A8 B2 MEM A8 B2 MEM A9 B3 MEM A9 B3 MEM A10 B4 MEM A10 B4 MEM A11 B5 MEM A11 B5 MEM A12 G3 MEM A12 G3 MEM A13 C4 MEM A14 F3 MEM A14 F3 MEM A14 F3 MEM A16 E4 MEM A16 E4 MEM A17 D3 A16 MEM A16 E4 MEM A17 D3 A16 MEM A17 D3 A16 MEM A18 B3 MEM A18 B3 MEM A19 D2 MEM D5 MEM D6 MEM D6 MEM D7 MEM D9 MEM D1		
MEM A10		
MEM A14 F3 A15		
	+5.0V L3 2.2uH	
3 SRAM_OE# A2 OE GND E6 3 SRAM_WE# G5 WE GND OE OE GND OE OE OE GND OE OE OE OE OE OE OE O	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	
[3] SRAM_UB B2 UB NC H6 H6 E3	$\frac{6}{\text{VCC}}$ CAP $\frac{3}{\text{C85}}$ $\stackrel{\text{C85}}{\leftarrow}$	+5.0V +5.0V
IS61WV51216BLL-10MI	MC34063A	
	R227 3K C86 C99 C98 0.1uF 0.1uF 0.1uF	
		<u> </u>
	+5.0V	
	U20	
+3.3V	[3] DAC CS# \Box 1 \Box 1 \Box 20	DAC_BYTE2 [3] DAC_WR2# [3]
$\begin{array}{c} \text{R128} \\ \text{1.3K NC} \end{array} \geqslant \begin{array}{c} +5.0\text{V} \\ \hline \end{array}$	3	DAC_XFER# [3] DAC_D4 [3] DAC_D5 [3]
AUDIO_PWM R42 R41 C9 R45 C15 C15 C15 C15 C15 C15 C15 C15 C15 C1	[3] DAC_DO 7 DI0(LSB) DI6 13 13	DAC_D6 DAC_D7 [3] R230 \(\frac{1}{2} \)
R43 R71 AUDIO_SD# [3,4] J12 R47	DAC0832-S020	_
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	-5.0V +5.0V	+ LM324 J2 U11-A 1 VOUT 0832 1
4 -IN AD8591ART-REEL 1 GND		5 † U11-B 7
Barrel Jack SJ-3523-SMT 1012591	$\begin{array}{c c} R231 & \nearrow & R124 \\ \hline 1.2K & 0 \text{ nc} \\ 1\% & 1\% & 1\% \end{array}$	+5.0V -
R39 =	DAC_VREF [4]	10 9 - U11-C 8 - LM324
	R229 4.7K 1%	-5.0V
	1%	13 12 U11-D 14 LM324
+5.0V +5.0V		
C24 $C26$ $C27$ $C28$		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	TITLE: SRAM_AUDIO	
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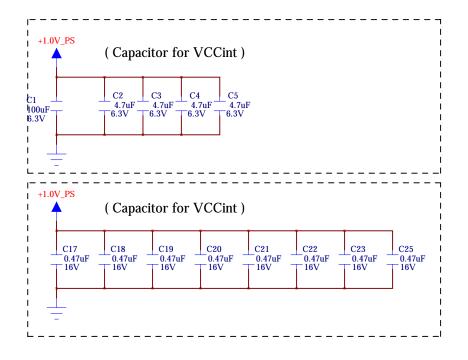


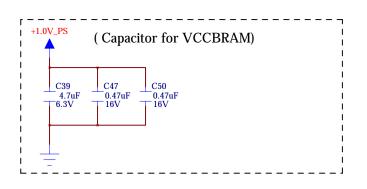
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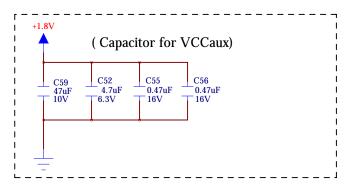


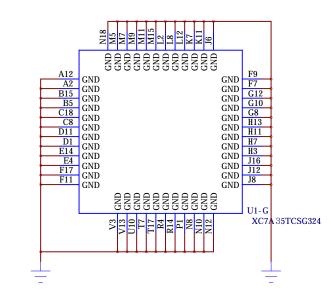
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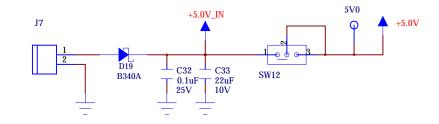


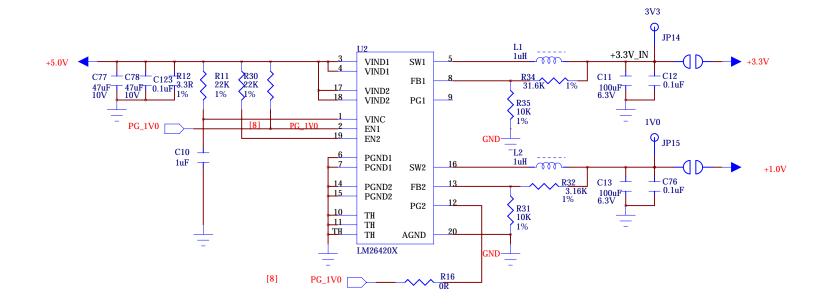


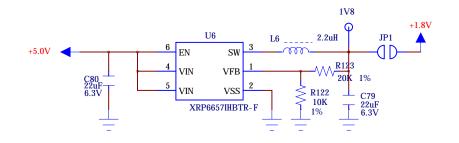


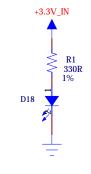
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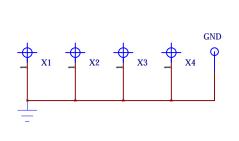
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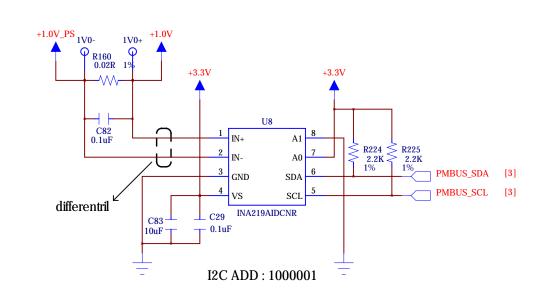












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